

DfT for full accessibility of multi-step analog to digital converters.

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DfT for Full Accessibility of Multi-Step Analog to Digital Converters

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ABSTRACT

This paper reports a Design for Testability (DfT) technique, which provides necessary diagnostic capability for signature-based and functional testing of multi-step analog to digital converters. The proposed approach permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range allowing full observability and controllability of the device under test. The proposed DfT can be used for engineering pre-characterization as well, and can easily be interfaced to standards like I²C and IEEE 1149.1 TAP controllers. Experimental evidence is provided on the 12 bit multi-step analog to digital converter fabricated in standard single poly, six metal 0.09- μ m CMOS.

INTRODUCTION

Modern Systems-on-Chip (SoC) integrate digital, analog and mixed-mode modules, e.g. mixed-signal, or RF analog and digital, etc., on the same chip. This level of integration is further complicated by the use of third-party cores obtained from virtual library descriptions of the final IC block. Furthermore, the variety and number of cores and their nature type, e.g. analog, complicate the testing phase of individual blocks, of combinations of blocks and ultimately of the whole system. Additionally, the large number of parameters required to fully specify the performance of mixed-signal circuits such as analog to digital converters (ADCs) and the presence of both analog and digital signals in these circuits make the testing expensive and time consuming task. Design for Testability (DfT) and Built in Self Test (BIST) techniques are aimed at increasing observability and controllability for reducing test cost and improving test quality. The most common approach for DfT of analog circuits is to partition a system into sub-blocks to have access to internal nodes such that each isolated sub-block receives the proper stimuli for testing [1]. In [2] a DfT is presented that is oriented at testing sub-blocks of a filter such that each stage is tested by increasing the bandwidth of the other stages. This is done by adjusting the switching scheme in the case of switched-capacitor filters, or by bypassing the filter capacitors using additional MOS transistor switches. The problem with the latter approach is that MOS transistors switches are in the direct signal path of the filter degrading the performance. To overcome this limitation a switched opamp structure with two operational modes, test and normal, depending upon a digital control signal, is proposed in [3], where the opamp is used at the interface between any two sub-blocks. An enhanced approach similar to [3] that makes use of an opamp with duplicated input stages is proposed in [4]. Other DfT schemes include ADCs with self-correction capability [5]. A DfT scheme suitable to detect parametric faults in switched-capacitor circuits based on a circuit that can compute *all* the capacitor ratios that determine the transfer function of the filter [6] and a charge redistribution ADC [7] is reported.

Unlike previous approaches that test the analog circuit only for functionality, we advocate the use of analog structural testing [8] as well. Our approach consists of exciting the circuit under test with a DC or low-frequency stimulus to sample the response at specified

times to detect the presence of a fault. The DC-transient waveform can be formed from piecewise-linear segments that excite the circuit's power supply, biasing, and/or inputs. To facilitate this kind of testing, it is preferable to observe the current (or voltage) signatures of individual cores instead of observing the current (or voltage) signature of the whole analog SoC. Furthermore, the proposed DfT approach, which is extension on [9], permits multi-step ADC re-configuration in such a way that all sub-blocks are tested for their full input range allowing full functional observability and controllability. In our implementation there are no switches in the (analog) signal path from core to core, and the test bus is actually shunted with the signal path. The core prior to the core under test is turned off through the I/O register-controlled switch controlling core's biasing network and the local clock and power-down signal. To estimate performance errors, we employed the steepest-descent method (SDM) algorithm [10], since it requires a small number of operations per iteration and does not require a correlation function calculation nor matrix inversions. Moreover, to enhance observation of important design and technology parameters, such as temperature, threshold voltage, etc., and to update the algorithm parameter estimation, dedicated sensors are embedded within the functional cores [11-12].

MULTI-STEP ADC

The input signal is sampled by a three-times interleaved sample-and-hold (S/H), eliminating the need for re-sampling of the signal after each quantization stage. As shown in Figure 1, the S/H splits and buffers the analogue delay line sampled signal that is then fed to three A/D converters (ADCs), namely, the Coarse (4 bits), the Mid (4 bits) and the Fine (6 bits). The quantization result of the Coarse A/D converter is used to select the references for the mid quantization in the next clock phase. The selected references are combined with the held input signal in two dual-residue amplifiers, which are offset calibrated. The Mid A/D converter quantizes the output signals of these mid-residue amplifiers. The outputs from both Coarse and Mid A/D converters are combined in order to select proper references for the fine quantization. These references are combined with the sampled input signal in two, also offset calibrated, dual-residue amplifiers. The amplified residue signals are applied to a Fine A/D converter.

In multi-step ADC, high linearity is obtained by extensive usage of correction and calibration procedures. Providing structural DfT and BIST capabilities to this kind of ADCs is difficult since the effects of correction mechanism must be taken into account. Overlap between the conversion ranges of two stages have to be considered, otherwise, there may exist conflicting operational situations that can either mask faults or give an incorrect fault interpretation. For at-speed testing of the analogue performance of the ADC converter it is imperative to have all 12 digital outputs and the two out of range signals available at the device pins without much interference from other IP cores. Furthermore the output signals of the Coarse, Mid and Fine ADCs need to be observable too. The ADCs are tested separately - at a lower speed - which enables the use of standard industrial analog waveform generators. To allow coherent testing the clock signal of the ADC needs to be fully controllable by the tester at

all times. Adding all these requests together leads to an output test bus that needs to be 14 bits wide. The connections of the test bus are not only restricted to the test of the analogue part. For digital testing the test bus is also used to carry digital data from scan chains.

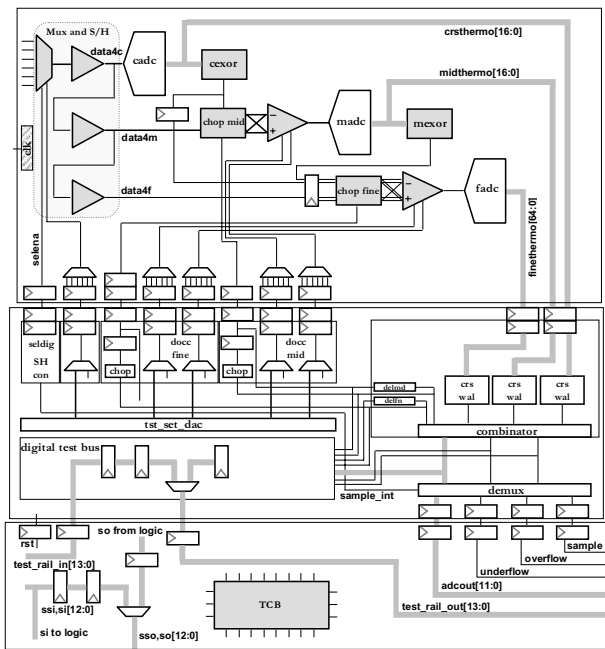


FIGURE 1. BLOCK DIAGRAM OF THE MULTI-STEP ADC AND TEST CONTROL CIRCUITRY

DFT IMPLEMENTATION

The test-shell contains all functional control logic, the digital test-bus, a test control block (TCB) to control testability within the ADC and a CTAG isolation chain for digital IO to and from other IP/cores as illustrated in Figure 1. Further, logic necessary for creating certain control signals for the analog circuit parts, and for the scan-chains a bypass mechanism, controlled by the TCB, is available. All TCB sections consist of a shift register and a shadow (or update) register as shown in Figure 2. The shift register is implemented using standard D-type flip-flops, while the shadow register includes an asynchronous reset function which will be, by default, active during the device functional mode.

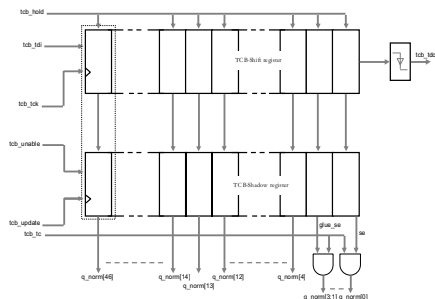


FIGURE 2. TCB IMPLEMENTATION

The control reset must be directly from an IC pin, and as such a dedicated pin is required. Several control signals are available: *i*) the asynchronous reset for the TCB, which directly controls the shadow register, *ii*) the input to the shift-register portion of the TCB and is

used to load the required test mode data, *iii*) the clock of the shift-register, *iv*) the signal, which is connected to the clock ports on the update register and is used to transfer the contents of the shift-register to the update register, *v*) the signal used to disable the shift function of the shift-register, *vi*) the signal, which toggles the set signal to control normal and shift mode, *vii*) the data output of the TCB, which can be connected to the input to the shift-register portion of a preceding TCB block, or can be directly tied to an IC pin and *viii*) the output signals of the TCB. It is possible to switch from any (test) mode to any other (test) mode without having to go through the TCB reset state. To provide an output for the TCB-block, an anti-skew flip-flop on the negative edge of the shift-register clock is added to the last TCB-Shift register. The ADC-TCB contains a total of 215 bits, divided over 211 normal slices and 3 slices which are gated with the scan control signal. The logic after the shadow flipflop(s) determines the slice type. To isolate digital test-shell as a separate core for testing, the digital I/O's of the core are provided with hold circuits (controlled by the local test control block bits) according to the CTAG protocol (Figure 3).

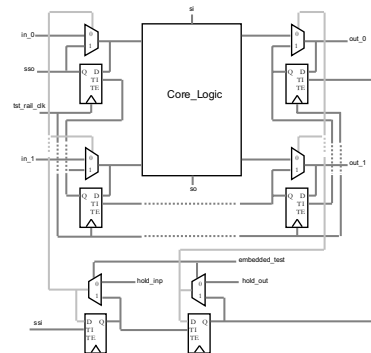


FIGURE 3. CTAG ISOLATION WITH EMBEDDED TEST IMPLEMENTATION

Since the separate ADCs have to be verified, it is necessary to fix the circuit during testing in such a way that all ADCs are tested for their full input range. In the analog part, there are seven scan chains of which four need special attention. To set the inputs of the separate ADCs at the wanted values, a chain is available in the switch-ladder circuit. So, for mid-range ADC measurements, it is necessary to fix the Coarse ADC values since they determine mid-range ADC references, and for testing of the Fine ADC both Coarse and Mid ADCs decisions have to be predetermined. The response of the individual ADCs is then routed to the test bus. The subDAC settings are controlled by serial shift of data through a scan chain that connects all subDAC registers in serial as shown in Figure 4. In order to create extra margin in the timing, signals are shifted half a period, which translates as running on a negative clock in application mode. To avoid the problems, which can arise by integrating this chain in a much longer chain in the larger system, the polarity of the clock control signal can be switched at will. In the gating of the clock is an override by the scan-enable signal, so that if the fix signal has been set accidentally still new values can be shifted in or through the chain, without the need for reprogramming the TCB. The needed inversion for application mode is done locally in the switch ladder logic followed by a local clock-tree, needed for the 128 flip-flops and one anti-skew element. It is possible to freeze the contents of the subDAC registers in normal mode and shift out the data via the scan chain to capture the current subDAC settings. A Test Control Bit is required per subDAC to adjust (increase) the reference current to obtain an optimal fit of the subDAC output range to the ADC input range. Beside the chain in the control logic for the switch ladder, the second chain available is in the coarse and mid exor block, which

consists of test-points implemented in an analog way with tri-state inverters as shown in Figure 5 for two coarse bits. In normal application these test-points do not have a function, and the clock for those flip-flops is switched off. During scan-tests, when the clock for the test-points is running, the application values are sampled.

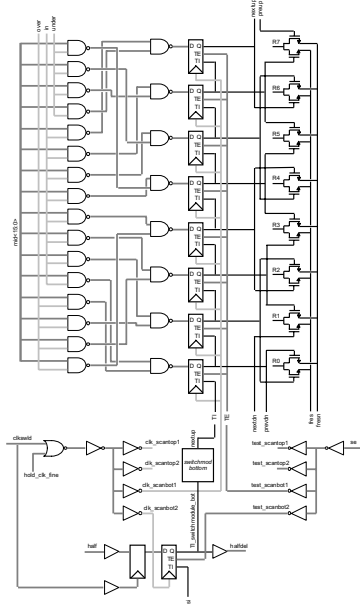


FIGURE 4. CONTROL LOGIC FOR THE SWITCH LADDER

The third scan chain available facilitates supply current readings of individual cores [9] by turning on/off the biasing network of the cores under consideration in an individual manner. By placing the switches at the ground nodes of the core's biasing circuit and not at the ground nodes of the analog core itself, an impact on the core's bias point due to voltage drop caused by switch on-resistance is limited. To ensure that a core is totally off, e.g. that it does not have floating nodes, a local power-down and local clock-down signals are made available.

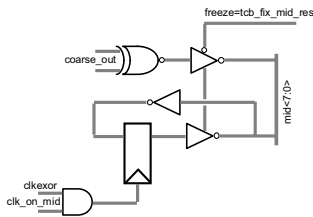


FIGURE 5. TEST POINT STRUCTURE OF COARSE EXOR

For nanometer CMOS ADCs, the large number of metal layers with increasing metal densities, prevents physical probing of the signals for debug purposes. Since parameter variations depend on unforeseen operational conditions, chips may fail despite they pass standard test procedures. To facilitate on-chip observation of parameter variation, dedicated sensors are embedded within the ADC [11-12]. All analog sensing and processing as well as the conversion into a digital format is done locally. The fourth scan chain available transports data to and from the sensors. Through the scan chain a sensor is activated, its settings are controlled, and the timing window is set.

TEST RESULTS

A prototype layout of the multi-step ADC is shown in Figure 6. The ADC converter with dedicated sensors is fabricated in standard single poly, six metal 0.09- μm CMOS with the core area of 1.4 mm^2 . One temperature sensor (located at the top right corner) and a total of 125 DLPMS, which are divided into specific groups, have been placed in and around the partitioned multi-step ADC. Each group of sensors target specific error source. The ADC operates at 1.2 V supply voltage and dissipates 200 mW (without output buffers). The ADC has no missing codes and the differential nonlinearity (DNL) remains within $\pm 1\text{LSB}$. The DNL and INL plots, obtained for a low-frequency input signal and sampled at 60 MS/s, are shown in Figure 7 and 8. Spectral signature and SNR versus magnitude for 100 kHz input signal sampled at 60 MS/s are illustrated in Figure 9 and 10.

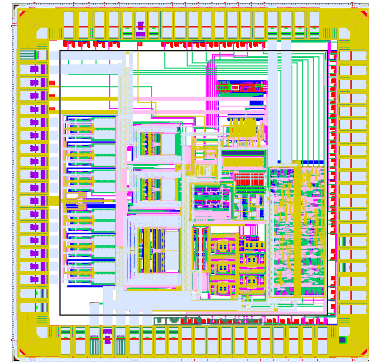


FIGURE 6. PROTOTYPE LAYOUT

Test results for Coarse, Mid, Fine and Total ADC are shown in Table 1. Since there is no feedback from Mid and Fine ADCs to the coarse result value, it is not necessary to set these two ADCs at the fixed value to test Coarse ADC. Calibration DAC settings do not show in coarse ADC results; the calibration system however should remain operative. Random calibration cycles are not allowed to prevent interference with test results. The response of the Mid ADC cannot directly be tested using the normal ADC output data due to an overlap in the ADC ranges. Nevertheless, by setting the coarse exor output signals using the scan chain through this block, known values are assigned to the mid switch. The residue signals are now used to verify the Mid ADC separately by observing the Mid ADC output bits via the test bus. For the Mid ADC test the chopper signals required for calibration need to be operative. After completing the Mid ADC test, the chopper signal have to be verified by setting the chopper input to the two predefined conditions and analyze the Mid ADC data to verify offsets. Because Calibration DAC settings do show in Mid ADC results, the DAC is set to a known value to prevent interference with Mid ADC test results. Similarly to the Mid ADC, the Fine ADC can not be monitored directly due to the overlap in the ADC ranges. Through the available scan chains in the coarse exor and the switchladder, control signals are applied to the both Mid and Fine switch. The predefined input signals are extracted when the ADC work in normal application mode with a normal input signal. At a certain moment the scan chains are set to a hold mode to acquire the requested value. Now, the residue signals derived through the predefined input signals evaluate the Fine ADC performance. For the Fine ADC test the chopper signals need to be active. To verify offsets, similar procedure as in Mid ADC is followed. The calibration DAC settings have to be known and set to a known value to prevent interference with test results. The digital control block for all three tests operates normally; provides clock pulses, chopper signals and sets the calibration DACs in a known condition.

CONCLUSION

The realization of a CMOS 12-b multi-step ADC incorporating a Design-for-Testability technique has been presented. We have shown that adding testing capability does not degrade the converter performance and has low impact on area and power consumption. The feasibility of the DfT for on-line and off-line testing has been verified by experimental measurements from the Silicon prototype.

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	Coarse	Mid	Fine	Total
I_{DD}	35 mA	35 mA	60 mA	165 mA
DNL	± 0.4 LSB	± 0.5 LSB	± 0.6 LSB	± 0.7 LSB
INL	± 0.6 LSB	± 0.6 LSB	± 0.9 LSB	± 1.0 LSB
THD	-24.7 dB	-26.1 dB	-35.8 dB	-73 dB
SNR	28.3 dB	25.5 dB	37.4 dB	67 dB

TABLE I – TEST RESULTS

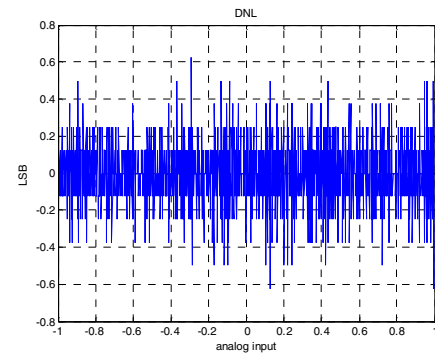


FIGURE 7. DNL CURVE AFTER CALIBRATION. DEFECTS RESULT MAINLY FROM ERRORS IN FINE ADC

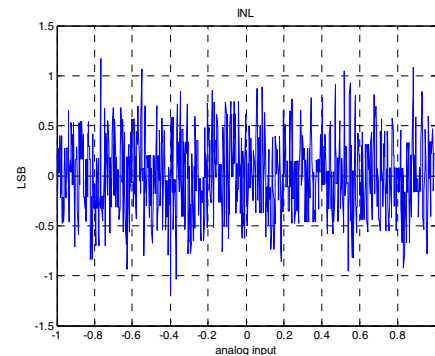


FIGURE 8. INL CURVE AFTER CALIBRATION. THE INL IS MAINLY CAUSED BY THE LADDER NON-LINEARITY.

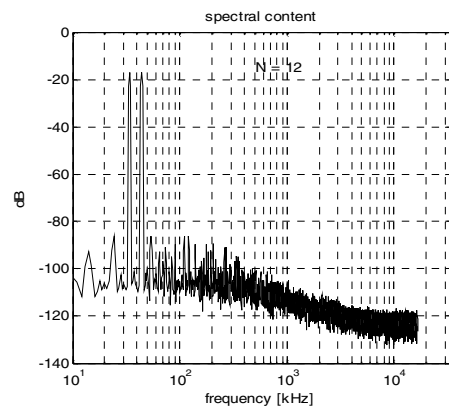


FIGURE 9. ADC SPECTRAL SIGNATURE

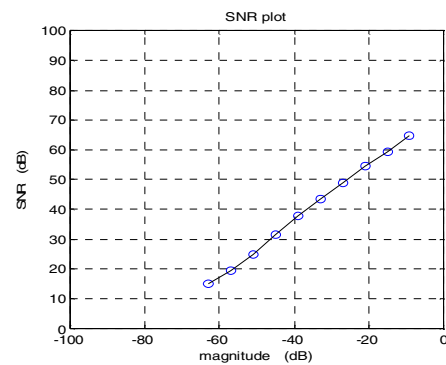


FIGURE 10. SNR VERSUS MAGNITUDE FOR $f_{in}=100$ KHZ.