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# Analog Automatic Test Pattern Generation for Quasi-Static Structural Test

Amir Zjajo, *Member, IEEE*, and José Pineda de Gyvez, *Fellow, IEEE*

***Abstract*—A new approach for structural, fault-oriented analog test generation methodology to test for the presence of manufacturing-related defects is proposed. The output of the test generator consists of optimized test stimuli, fault coverage and sampling instants that are sufficient to detect the failure modes in the circuit under test. The tests are generated and evaluated on a multistep ADC taking into account the potential fault masking effects of process spread on the faulty circuit responses. Similarly, the test generator results offer indication for the circuit partitioning within the framework of circuit performance, area and testability.**

***Index Terms*—Analog ATPG, analog test, parametric fault model, structural test.**

## I. Introduction

COMPLEX SoC products include analog and mixed-signal IPs which need to be testable. Since these IPs are embedded in the SoC, it is difficult to access all of their ports and as such existing test practices are not always applicable, or need to be revised. This implies also that test times need to be reduced to acceptable limits within the digital-testing time domain; it also implies the incorporation of DfT, BIST, and silicon debug techniques. For these SoCs, many of the tests exercised at final test are being migrated to wafer test, partly because of the need to deliver known good dies before packaging, and partly because of the need to lower analog test costs.

Structural, fault-orientated testing [1], [2] is a convenient mean to avoid functional testing at wafer-level test. Several studies [3]–[7] have revealed that faults which shift the operating point of a transistor-level analog circuit can be detected by inexpensive DC testing or power supply current monitoring. In [3], a DC test selection procedure was presented where the detection criteria included the effect of parameter tolerance with a linear approximation around the nominal values. In [4], to include the effect of parameter tolerance during testing, the test generation problem is formulated as a Minimax optimization problem, and solved iteratively as successive linear programming problems. An approach for the fault detection based on Bayes decision rule for DC testing is presented in [5] by combining the *a priori* information and the information from testing. Principle component analysis is applied for the calculation of the discrimination function in the case of the measurements being dependent. In [6], the measurement events are classified according to the regions that data fall into and the statistical profiles of the measurable parameters for each parametric fault are obtained. By iteratively conducting the tests and applying the Bayesian analysis, the occurrence probability of each fault is found. The parametric fault simulation and test vector generation in [7] utilizes the process information and the sensitivity of the circuit principal components in order to generate statistical models of the fault-free and faulty circuit. The Bayes risk is computed for all stimuli and for each fault in the fault list. The stimuli for which the Bayes risk is minimal, is taken as the test vector for the fault under consideration. By employing the Neyman–Pearson statistical detector [8], which is a special case of the Bayes test, we provide a workable solution when the *a priori* probabilities may be unknown, or the Bayes risk may be difficult to evaluate or set objectively.

The fault model presented in this paper is based on altering the dc biasing conditions of the circuit under test. A wrongly biased circuit generates many of the functional faults encountered in analog circuits. This approach, based on experimental results [9], shows a good correlation with functional testing. With the Karhunen–Loève expansion method [10] hereby proposed, the parameters of the transistors are modeled as stochastic processes over the spatial domain of a die, thus making parameters of any two devices on the die, two different correlated random variables.

The paper is organized as follows. Section II focuses on the automated flow of the analog test pattern generator. Section III discusses the quasi-static nodal voltage approach, the Neyman–Pearson detector and test stimuli optimization algorithm. In Section IV, the influence of the modeled parametric faults on linearity and supply current behavior of a two-step analog-to-digital converter (ADC) is examined. Finally, Section V provides a summary and the main conclusions.

## II. Test Strategy Definition

In our approach, the circuit under test is excited with a quasi-static stimulus to sample the response at specified times to detect the presence of a fault. The waveform is systematically formed from piecewise-linear ramp segments that excite the circuit's power supply, biasing, reference and inputs, which forces the majority of the transistors in the circuit to operate in all the regions of operation and, hence, provide bias currents rich in information. To apply the power-supply-current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques, since the method requires more than a simple coarse observation of abnormal currents at the power supply network. Analog faulty behaviours are

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TABLE I
MOST KEY PARAMETERS AT $V_{BS} = 0$ V

| $W/L$=10/0.18 | | | $W/L$=10/0.18 | | | Unit |
|---|---|---|---|---|---|---|
| $p$ | $\mu$ | $\sigma$ | $p$ | $\mu$ | $\sigma$ | |
| $V_{T0,N}$ | 516.92 | 10.44 | $V_{T0,P}$ | 481.148 | 10.103 | mV |
| $K_{0,N}$ | 422.53 | 10.34 | $K_{0,P}$ | 518.538 | 13.109 | $mV^{1/2}$ |
| $K_N$ | 446.967 | 8.461 | $K_P$ | 451.971 | 17.434 | $mV^{1/2}$ |
| $\beta_N$ | 26.334 | 1.290 | $\beta_P$ | 6.775 | 0.261 | $mA/V^2$ |
| $W_{eff,N}$ | 10.034 | 0.010 | $W_{eff,P}$ | 10.034 | 0.010 | μm |
| $L_{eff,N}$ | 0.108 | 0.005 | $L_{eff,P}$ | 0.143 | 0.005 | μm |
| $I_{DS,,lin}{}^a$ | 1.354 | 0.018 | $I_{DS,,lin}{}^c$ | 0.402 | 0.018 | mA |
| $I_{DS,,sat}{}^b$ | 6.035 | 0.226 | $I_{DS,,sat}{}^d$ | 2.914 | 0.226 | mA |

a. $I_{DS,lin}$ at $V_{GS} = 1.8$ V and $V_{DS} = 0.1$ V c. $I_{DS,lin}$ at $V_{GS} = -1.8$ V and $V_{DS} = -0.1$ V
b. $I_{DS,sat}$ at $V_{GS} = 1.8$ V and $V_{DS} = 1.8$ V d. $I_{DS,sat}$ at $V_{GS} = -1.8$ V and $V_{DS} = -1.8$ V

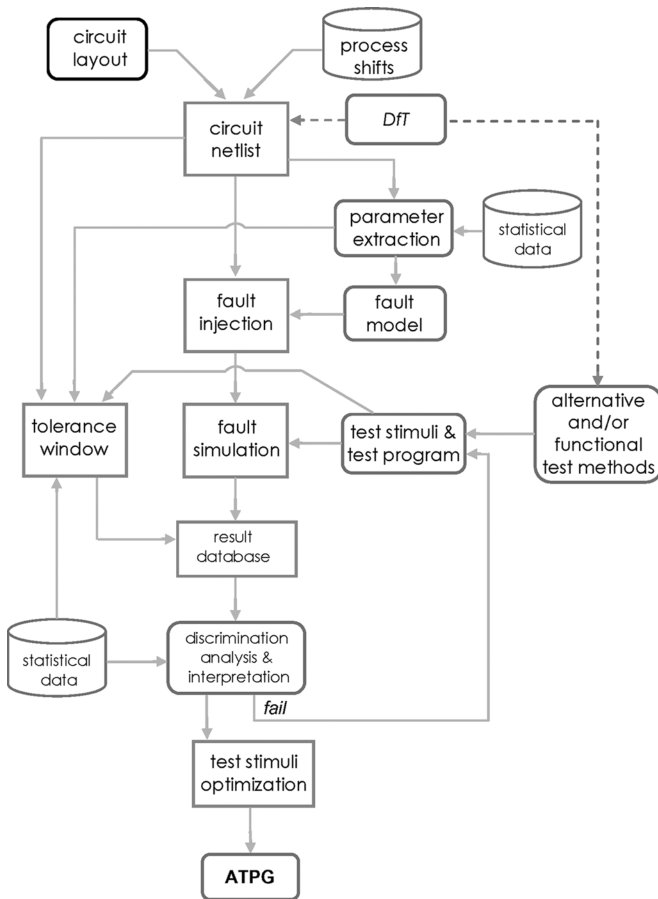


Fig. 1. ATPG—proposed top-level flow diagram.

not so pronounced as those in the digital case, and due to the resolution limitations of the power-supply-current observation technique, the device under test has to be subjected to a design for testability methodology which consists of partitioning the circuit to reach better current observability.

The proposed top-level test generation flow diagram is shown in Fig. 1. First, a tolerance window is derived according to test stimuli and test program. The circuit is simulated without any faults and the results of this test are saved in a database. The next step is to sequentially inject the selected faults into the circuit and simulate according to the same test stimuli and test program as used to derive the tolerance window. All simulation results are saved in the database, from where the fault coverage can be calculated in conformance with the tolerance window and discrimination analysis. To derive necessary stimuli for the ATPG, the test stimuli optimization is performed on the results available in the database.

## III. Quasi-Static Structural Test

### A. Network Analysis and Global Process Variations

General differential-algebraic equations, which describe the circuit's electrical behavior, have been widely investigated [10]–[12]. The results cover, among other issues, unique solvability, feasibility of numerical methods as well as stability properties. A procedure such as [10], allows us to decompose the circuit's unknowns (node voltages, currents through branches) into a differential component $y$ for time dependent solutions and an algebraic component $z$ for quasi-static analysis. The nominal voltages and currents $z_0$ are obtained by [12]

$$z_0 = -B^{-1}\left(C_Q y_0 - F_Q\left(i_{(0)}, v_{(0)}\right)\right) \tag{1}$$

where $B$, $C_Q$ and $F_Q$ are functions of the deterministic initial solution related to linear and nonlinear couplings among the circuit's devices, $y_0$ is an arbitrary initial state of the circuit and $i \in \Re^{n(I)}$ and $v \in \Re^{n(V)}$ are the independent current and voltage sources, respectively. It is assumed that for each process parameter $p$, e.g., threshold voltage, transconductance etc., there is only one solution of $z_0$. However, due to process variations, the manufactured values of process parameters will differ; hence, we model the manufactured values of the parameters $p_i \in \{p_1, \ldots, p_m\}$ for transistor $i$ as a random variable

$$p_i = \mu_{p,i} + \sigma_p(d_i) \cdot p(d_i, \theta) \tag{2}$$

where $\mu_{p,i}$ and $\sigma_p(d_i)$ are the mean value and standard deviation of the parameter $p_i$, respectively, $p(d_i, \theta)$ is the stochastic process corresponding to parameter $p$, $d_i$ denotes the location of transistor $i$ on the die with respect to a point origin and $\theta$ is the die on which the transistor lies. This reference point can be located, say in the lower left corner of the die, or in the center, etc. As way of example, Table I shows some typical transistor parameters $p$ with their mean and spread values.

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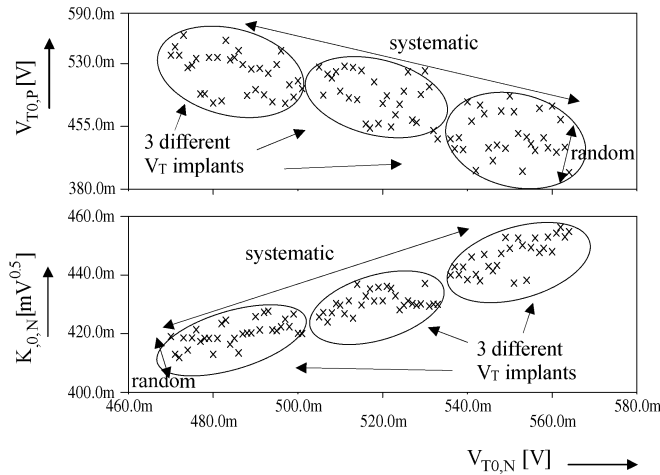


Fig. 2. a) $p$-channel threshold voltage, $V_{TO,P}$, versus $n$-channel threshold voltage, $V_{T0,N}$; measured on two hundred transistor pairs from the same batch; b) body-effect factor, $K_{0,N}$, versus threshold voltage, $V_{T0,N}$; for two hundred $n$-channel transistors from a batch with three different implantations to adjust the threshold voltage.

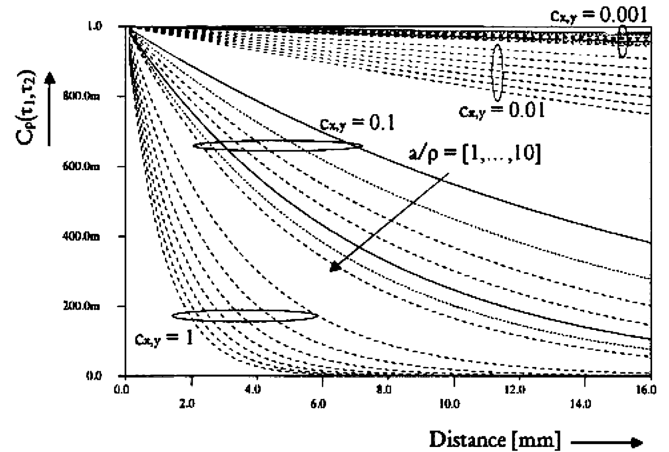


Fig. 3. Behavior of modeled covariance functions using $M = 5$ for $a/\rho = [1, \ldots, 10]$.

## B. Spatial Correlation Model

The availability of large data sets of process parameters obtained through parameter extraction allows the study and modeling of the variation and correlation between process parameters, which is of crucial importance to obtain realistic values of the modeled circuit unknowns. As an illustration we first show in Fig. 2 the parameter statistics of a batch with three different threshold-adjust implantations (identical for both $n$- and $p$-channels).

A random process can be represented as a series expansion of some uncorrelated random variables involving a complete set of deterministic functions with corresponding random coefficients. A commonly used series involves spectral expansion [13], in which the random coefficients are uncorrelated only if the random process is assumed stationary and the length of the random process is infinite or periodic. The use of Karhunen–Loève expansion [10] has generated interest because of its bi-orthogonal property, that is, both the deterministic basis functions and the corresponding random coefficients are orthogonal [14], e.g., the orthogonal deterministic basis function and its magnitude are, respectively, the eigenfunction and eigenvalue of the covariance function.

Assuming that $p_i$ is a zero-mean Gaussian process and using the Karhunen–Loève expansion, $p_i$ can be written in truncated form (for practical implementation) by a finite number of terms $M$ as

$$p_i = \mu_{p,i} + \sigma_p(d_i) \cdot \sum_{n=1}^{M} \sqrt{\vartheta_{p,n}} \xi_{p,n}(\theta) f_{p,n}(d_i) \tag{3}$$

where $\{\xi_n(\theta)\}$ is a vector of zero-mean uncorrelated Gaussian random variables and $f_{p,n}(d_i)$ and $\vartheta_{p,n}$ are the eigenfunctions and the eigenvalues of the covariance matrix $C_p(d_1, d_2)$ of $p(d_i, \theta)$. Without loss of generality, consider for instance two transistors with given threshold voltages. In our approach, their threshold voltages are modeled as stochastic processes over the spatial domain of a die, thus making parameters of any two transistors on the die, two differently correlated random variables. The value of $M$ is governed by the accuracy of the eigen-pairs in representing the covariance function rather than the number of random variables.

Unlike previous approaches, which model the covariance of process parameters due to the random effect as a piecewise linear model [15], or through modified Bessel functions of the second kind [16], we represent the covariance (Fig. 3) as a linearly decreasing exponential function

$$C_p(d_1, d_2) = \left(1 + \eta_{d_{x,y}}\right) \cdot \gamma \cdot \left(e^{-c_x|d_{x1} - d_{x2}| \cdot c_y|d_{y1} - d_{y2}|/\rho}\right) \tag{4}$$

where $\eta$ is a distance based weight term, $\gamma$ is the measurement correction factor for the two transistors located at Euclidian coordinates $(x_1, y_1)$ and $(x_2, y_2)$, respectively, $c_x$ and $c_y$ are process correction factors depending upon the process maturity.

For instance, in Fig. 3 $c_{x,y} = 0.001$ relates to a very mature process, while $c_{x,y} = 1$ indicates that this is a process in a ramp up phase. In (4) $\rho$ is the correlation parameter reflecting the spatial scale of clustering defined in $[-a, a]$, which regulates the decaying rate of the correlation function with respect to distance $(d_1, d_2)$. Physically, lower $a/\rho$ implies a highly correlated process, and, hence, a smaller number of random variables are needed to represent the random process and correspondingly, a smaller number of terms in the Karhunen–Loève expansion. This means that for $c_{x,y} = 0.001$ and $a/\rho = 1$ the number of, transistors that need to be sampled to assess, say a process parameter such as threshold voltage is much less than the number that would be required for $c_{x,y} = 1$ and $a/\rho = 10$ because of the high nonlinearity shown in the correlation function.

One example of spatial correlation dependence and model fitting on the available measurement data of Fig. 2 through Karhunen–Loève expansion is given in Fig. 4. For comparison purposes, a grid-based spatial-correlation model is intuitively simple and easy to use, yet, its limitations due to the inherent accuracy-versus-efficiency necessitate a more flexible approach, especially at short to mid range distances [16].

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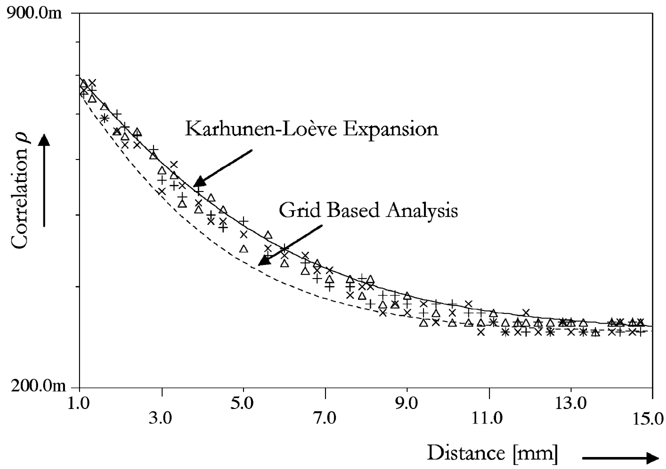


Fig. 4. Spatial correlation dependence of Fig. 2.

### C. Defect and Fault Model Definition

From a statistical modeling perspective, global variations affect all transistors in a given circuit equally. Thus, systematic parametric variations can be represented by a deviation in the parameter mean of every transistor in the circuit, which can be seen as a "defect." We introduce now a defect model, $\varsigma_p = f(.)$, accounting for voltage and current shifts due to random manufacturing variations in transistor dimensions and process parameters defined as

$$\varsigma_p = f(\nu, W^*, L^*, p^*) \tag{5}$$

where $\varsigma_p = f(.)$ is the function of changes in node voltages and branch currents, $\nu$ defines a fitting parameter estimated from the extracted data, $W^*$ and $L^*$ represent the geometrical deformation due to manufacturing variations, and $p^*$ models electrical parameter deviations from their corresponding nominal values, as defined in (3), e.g., altered transconductance, threshold voltage, etc. This defect model is used to generate a corresponding circuit fault model by including the term $\varsigma_p$ of (5) into (1), written in matrix form as

$$\Xi = z_0 \times \varsigma_p \tag{6}$$

where $z_0$ is a matrix of the nominal data and $\varsigma_p$ a random vector accounting for device tolerances. Basically, the fault model of (6) shifts the dc nodal voltages (dc branch currents) out of their ideal state based on the random and systematic variations of the process technology. While the functional behavior of a circuit in the frequency domain may not be linear, or even in the dc domain as a result of a nonlinear function between output and input signals, observe that as long as the biasing and input conditions of the circuit under test remain quasi-static the faulty nodal voltage (branch current) of (6) follows a Gaussian distribution as posed in (3). An obvious limitation of the fault model of (6) is that it cannot capture a faulty transient behavior of the circuit under test.

Based on the central limit theorem, to completely characterize Gaussian data in (6) probabilistically, we need to calculate the means and correlations by calculating the first and second-order moments through expectation. Even if the random variable is not strictly Gaussian, a second-order probabilistic characterization yields sufficient information for most practical problems. To make the problem manageable, the system in (6) is linearized by a truncated Taylor approximation assuming that the magnitude of the random defect $\varsigma_p$ is sufficientl small to consider the equation as linear in the range of variability of $\varsigma_p$, or that the nonlinearites of the electrical fault, $\Xi$, in the case of quasi-static dc biasing are so smooth that they might be considered as linear even for a wide range of $\varsigma_p$. We need now to compute the autocorrelation function of each nodal voltage (branch current) for each of the process parameters to estimate a tolerance window that helps us define whether the circuit is faulty or not. The autocorrelation of $\Xi$ for a quasi-static time period is then calculated as

$$C_{\Xi\Xi} = J_0 \times C_{\varsigma\varsigma} \times J_0^T \tag{7}$$

where $J_0$ is the Jacobian of the initial data $z_0$ evaluated at $p_i$ and $C_{\varsigma\varsigma}$ is the symmetrical covariance matrix whose diagonal and off-diagonal elements contain the parameter variances and covariances as defined in (4), respectively. Following (7), the boundaries of quasi-static node voltage $\Xi_r$ with mean value $\mu_{\Xi r}$ are expressed with

$$[\Xi_{r,\min}, \Xi_{r,\max}] = \mu_{\Xi_r} \pm \sum_k \sum_m \{|C_{\Xi_r \Xi_r}|^{\max}\} \tag{8}$$

for any $p_i \in \{p_1, \ldots, p_m\}$ of $i \in \{i_1, \ldots, i_k\}$ transistors connected to node $r \in \{r_1, \ldots, r_q\}$. Per definition, setting the quasi-static node voltage $\Xi_r$ outside the allowed boundaries in (8) designates the faulty behavior. To obtain a closed form of moment equations, Gaussian closure approximations are introduced to truncate the infinite hierarchy. In this scheme, higher order moments are expressed in terms of the first and second-order moments as if the components of $\Xi$ are Gaussian processes.

### D. Discrimination Analysis

As each branch current is a Gaussian random variable in linear combination of parameter variations, the power supply current due to the voltage deviation at the node $r$, denoted as $I_{DDn}^r$ ($n$ samples) is, therefore, also a Gaussian distributed random variable, and its derivatives to all process parameters $\partial I_{DDn}^r / \partial p_i$ can easily be found from its linear expression of parameters. To avoid notation clustering, $I_{DDn}$ denotation is further used in the paper.

Derivation of an acceptable tolerance window for $I_{DDn}$ is aggravated due to the overlapped regions in the measured values of the error-free and faulty circuits, resulting in ambiguity regions for fault detection. To counter this uncertainty, the Neyman–Pearson test [8], which is based on the critical region $C^* \subseteq \Omega$, where $\Omega$ is the sample space of the test statistics, offer the largest power of all tests with significance level $\alpha$

$$C^* = \{(I_{DD1}, \ldots, I_{DDn}) : l(I_{DD1}, \ldots, I_{DDn}|G, F) \leq \lambda\} \tag{9}$$

where $I_{DD}$ is an observation sample, $l()$ is a likelihood function, and $G$ and $F$ denote the error-free and faulty responses,

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respectively. For the threshold $\lambda$ to be of significance level $\alpha$, we need

$$P = \{(I_{DD1}, \ldots, I_{DDn}) \in C^* | P(G)\} = \alpha$$
$$P\left(\bar{I}_{DD} \geq \lambda | I_{DD} \sim N(\mu, \sigma^2/n)\right) = P\left(Z \geq \frac{\lambda - \mu_G}{\sigma_G/\sqrt{n}}\right) = \alpha \quad (10)$$

where $\mu_G$ and $\sigma_G$ are mean and variance of the error-free response. $P(Z < z_{(1-\alpha)}) = 1-\alpha$, and $z_{(1-\alpha)}$ is the $(1-\alpha)$-quantile of $Z$, the standard normal distribution. From (10), it follows that the test $T$ rejects for

$$T = \frac{\bar{I}_{DD} - \mu_G}{\sigma_G/\sqrt{n}} \geq z_{(1-\alpha)}. \quad (11)$$

To incorporate the Neyman–Pearson lemma, the first step is to choose and fix the significance level of the test $\alpha$ and establish the critical region of the test corresponding to $\alpha$. This region depends both on the distribution of the test statistic $T$ and on whether the alternative hypothesis is one- or two-sided. Based on this statistics, a decision is made to accept or reject the data sample.

### E. Test Stimuli Optimization

Two approaches [17] to test stimuli ordering are considered: In the first stage, the test stimuli are ordered so that the test stimuli detecting the most-faulty parameters that are detected by no other test stimuli are performed first (the test stimuli are ordered in descending order of unique coverage values). In the second stage, going from top to bottom, test stimuli, which do not increase the cumulative coverage, are moved to the bottom of the list. Because some test stimuli are eliminated from the test stimuli set before the test stimuli's are ordered, both algorithms are heuristic, and both can handle circuits with many more specifications at much less computation cost.

Following the steps described in this section, the total time required for fault injection $t_{\text{injection}}$, fault simulation $t_{\text{simulation}}$, discrimination analysis $t_{\text{discrimination}}$ and test stimuli optimization $t_{\text{optimization}}$ can be expressed as

$$\begin{aligned} t_{\text{injection}} &= N_{\text{nodes}} \cdot t_{\text{swap}} \\ t_{\text{simulation}} &= N_{\text{bias}} \cdot N_{\text{supply}} \cdot N_{\text{input}} \cdot N_{\text{reference}} \\ &\quad \cdot t_{\text{circuit}} + t_{\text{tolerance}} \\ t_{\text{discrimination}} &= N_{\text{faults}} \cdot t_{\text{analysis}} \\ t_{\text{optimization}} &= N_{\text{permutation}} \cdot N_{\text{faults}} \end{aligned} \quad (12)$$

where $t_{\text{swap}}$, $t_{\text{circuit}}$, $t_{\text{tolerance}}$, and $t_{\text{analysis}}$ is a time required to introduce the fault into circuitry, simulate the circuit netlist, derive the boundaries of circuit response and perform the Neyman–Pearson test, respectively. $N_{\text{nodes}}$ denote the number of the nodes in the circuit, $N_{\text{bias}}$, $N_{\text{supply}}$, $N_{\text{input}}$ and $N_{\text{reference}}$ designate the number of bias, supply, input and reference nodes where a quasi-static stimulus is applied, respectively, $N_{\text{faults}}$ indicate the number of the faults and $N_{\text{permutation}}$ designate the number of permutations of the test stimuli set.

## IV. Application Example

The proposed method is evaluated on static performance measures of a 12-bit multistep analog-to-digital converter (ADC) described in [18], consisting of time-interleaved sample and hold (S/H) circuit, 5-bit coarse and 8-bit fine ADC and sub-DAC. The overall converter employs around 5000 transistors within an analog core and consists primarily of low-power components, such as low-resolution quantizers, switches and open-loop amplifiers.

The results shown in the next sections were obtained with limited area overhead (approximately 5%), primarily from additional biasing transistors and routing, and at negligible extra power consumption since these bias transistors are not used in normal functional node. Performance loss is insignificant as no switches are placed in the signal path. The total test time required at wafer-level manufacturing test based on current-signature analysis is in $3 \sim 4$ ms range per input stimuli. As the ATPG results show, for the entire ADC 10 input stimuli are required, which results in a total test time for the quasi-static test of at most 40 ms. This pales in comparison to around 1 s needed to perform histogram-based static or approximately 1 s for FFT-based dynamic ADC test. Note that time required to perform these functional tests depends on the speed of the converter and available postprocessing power.

### A. Power-Scan Chain DfT

The *power-scan chain* [19] DfT technique shown in Fig. 5 is used to assist quasi-static testing as a means to provide observability at the core's power supply and output terminals and at exciting the core under test. The DfT consists of an Analog Test Input Bus to provide input stimuli to the core under test, an Analog Test Output Bus to read out the stimuli response, an Analog Supply Network to read out currents in the power line and two Shift-register controllers to turn on/off individual cores and to select/deselect input/output test busses, respectively.

The analog test bus interface is implemented through the IEEE 1149.4 analog test bus extension to 1149.1, and the serial shift register is a user register controlled by an IEEE Std 1149.1 TAP controller [20], which allows access to the serial register, while the device is in functional mode. Furthermore, such controller creates no additional pin counts since it is already available in the SoC. To facilitate supply current readings of the individual cores, the biasing network of the cores under consideration are turned on/off in an individual manner. Overhead in area is minimum as only the biasing network is modified at the cost of only a few transistors $(D_1, D_{21}, \ldots, D_{T1}, \ldots, D_{61}, \ldots D_{T5})$ per observed stage. The supply currents of the individual cores can be found from the difference between the supply currents found for the different codes, clocked in from left to right out of the bias shift register. The supply current readings are performed at the core's nominal operating conditions.

### B. Fine ADC

To demonstrate the proposed concept, let's concentrate on the fine ADC (Fig. 6), which numbers approximately 1800 transistors. For illustration, two faults as defined by (6) are inserted, at the output $\Xi_{r1}$ and at the input biasing node $\Xi_{r2}$ of first stage

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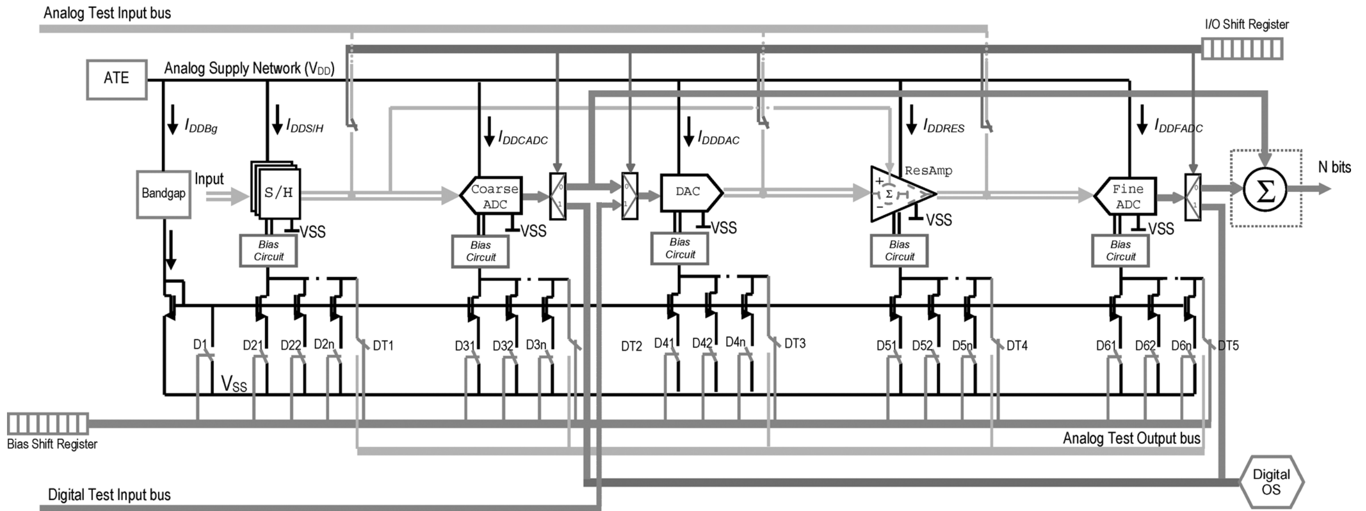


Fig. 5. Conceptual overview of power-scan chain DfT implemented in the two-step ADC.

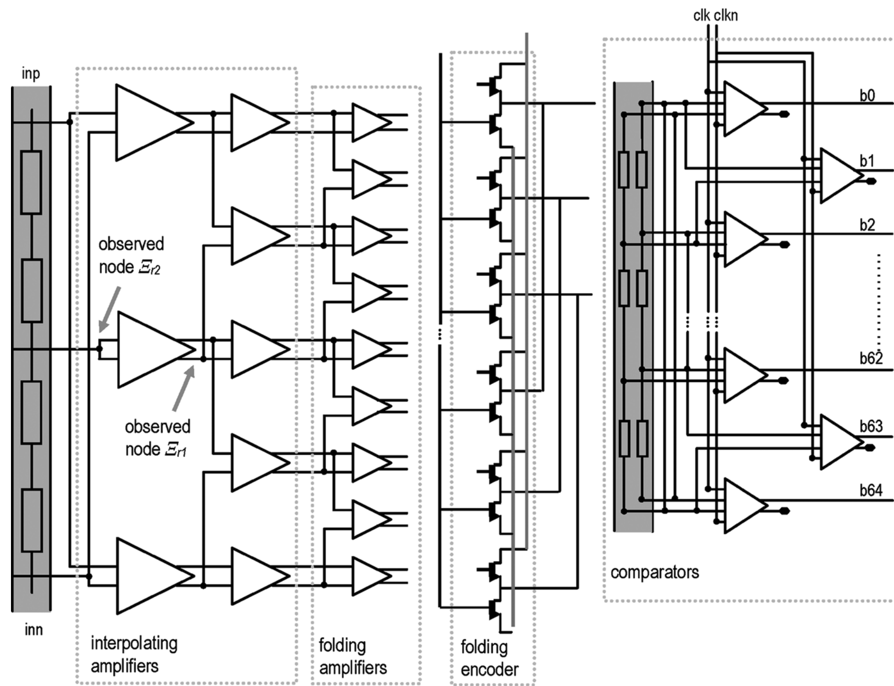


Fig. 6. Schematic of the fine ADC. Two observed nodes, at the input and output of the first stage preamplifier are shown.

amplifier. This fault injection sets the node voltage outside the permitted node variation range characterized by (8) as illustrated in Fig. 7 and leads to easily spotted integral nonlinearity (INL) errors as shown in Fig. 8.

Now, let us look at the influence of the modeled fault at the power supply current $I_{DD}$. As shown in Fig. 9, inserting the fault at the observed nodes and simulating at nominal input values will lead to a deviation in the supply current, although, as seen for the fault at the negative output node $\Xi_{r1}$ a large ambiguity region within error-free $P(G)$ and faulty $P(F)$ circuit probabilities make any decision subject to an error. However, by concurrently applying a linear combination of the inputs stimuli (the input signal, the biasing, reference and the power supply voltage) one can find the operating region where uncertainty due to the ambiguity regions for both modeled faults is reduced (Fig. 10), and, thus, the corresponding probability of accepting the faulty circuit as a error-free is decreased. Next, we set the significance level of the test $\alpha$, and based on the distribution of the test statistics (11) we formulate the Neyman–Pearson critical (rejection) region $C^*$.

Continuing with the example illustrated in Fig. 10, where $P(G): I_{DDn} \sim N(1.946\ \text{mA}, 0.23\ \text{mA})$ and $P(F): I_{DDn} \sim N(2.16\ \text{mA}, 0.25\ \text{mA})$ for the fault at node $\Xi_{r1}$, the critical region $C^*$ for the test to be of significance level $\alpha = 0.1$

$$\alpha = P\left(Z \geq \frac{\lambda - \mu_G}{\sigma_G/\sqrt{n}}\right) = 1 - \Phi\left(\frac{\lambda - \mu_G}{\sigma_G/\sqrt{n}}\right) = 0.1. \quad (13)$$

Hence, from standard normal tables

$$\Phi\left(\frac{\lambda - \mu_G}{\sigma_G/\sqrt{n}}\right) = 0.9 \Rightarrow \frac{\lambda - \mu_G}{\sigma_G/\sqrt{n}} = 1.282 \quad (14)$$

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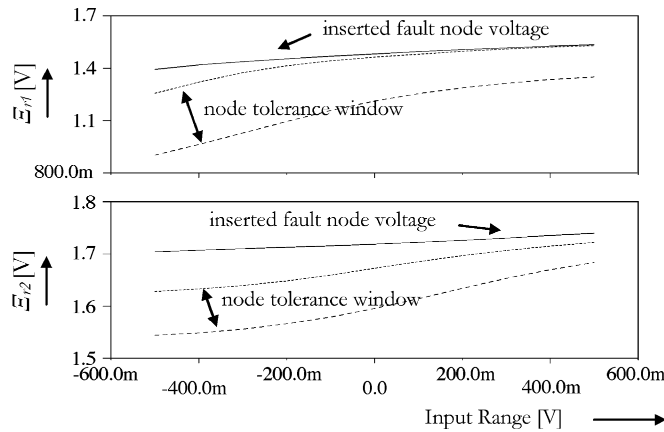


Fig. 7. Fault insertion and their relation towards tolerance window defined in (8).

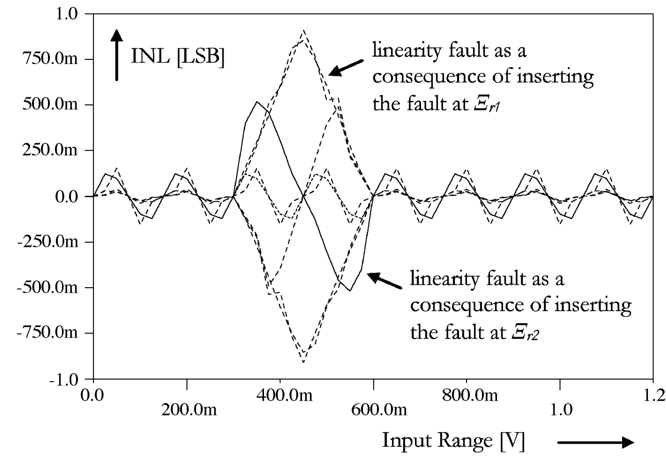


Fig. 8. Integral nonlinearity when faults are inserted in the first stage preamplifier.

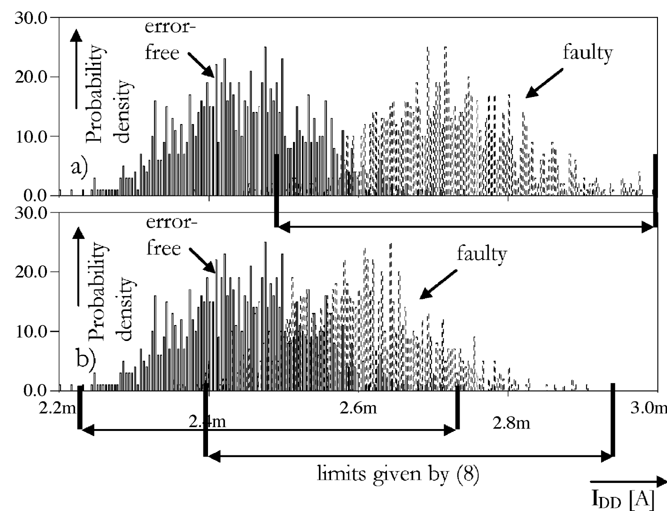


Fig. 9. Preamplifier $I_{DD}$ histogram plot at nominal input values for the error-free and for a) fault at node $\Xi_{r2}$ and b) $\Xi_{r1}$.

leading to the critical region of

$$C^{*}=\left\{(I_{DD1,\ldots,}I_{DDn}):\overline{I}_{DD}\geq\mu_{G}+1.282\frac{\sigma_{G}}{\sqrt{n}}=2.01\text{ mA}\right\} \quad (15)$$

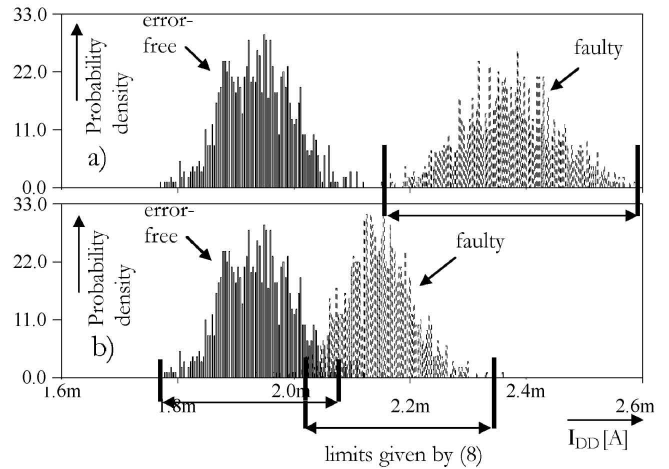


Fig. 10. Preamplifier $I_{DD}$ histogram plot after ATPG optimization for the error-free and for a) fault at node $\Xi_{r2}$ and b) $\Xi_{r1}$.

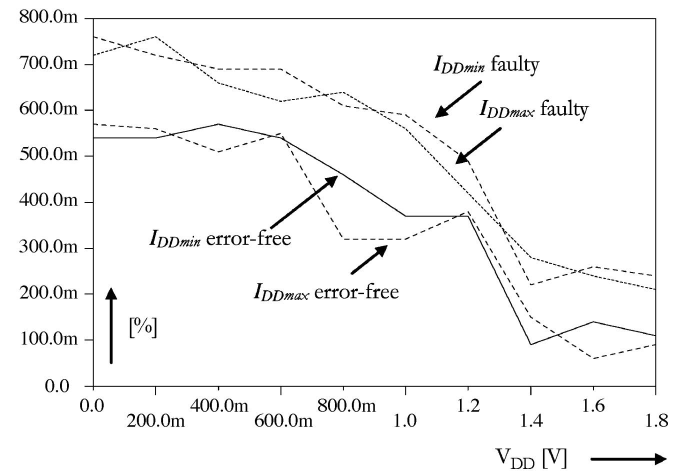


Fig. 11. Difference in percentage [%] between Monte Carlo analysis and limits given by equation (8) for the supply current $I_{DD}$ of the error-free and faulty circuit as function of the supply voltage $V_{DD}$. $IDD_{\max}$ and $IDD_{\min}$ denote the tails of the probability function.

where $\mu_G$ and $\sigma_G$ are mean and variance of error-free power supply current. Thus, the circuit will be specified as a faulty if its power supply current value $I_{DDn}$ is higher or equal to the threshold $\lambda$. A comparable discrimination analysis is performed for all circuit's power supply current values generated as a consequence of inserting the faults at all nodes in the circuit in the entire range specified in the test program. The probabilities $P(G)$ and $P(F)$ as specified in (8) match the spread of more than 2000 Monte Carlo iterations, while allowing multiple order of magnitude CPU time savings. Fig. 11 displays the accuracy of using (8) for a power supply sweep.

In the entire fine ADC a total of 2198 faults, corresponding to a similar number of nodes, are injected in the fault-free circuit netlist, and simulated according to the test stimuli and the specified test program. The results of the test generator offer an indication for the required circuit partitioning through power-scan DfT, within the framework of circuit performance, area and testability. The tests are performed hierarchically and influenced by circuit architectural aspects, such as feedback among

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TABLE II
FINE ADC TEST RESULTS

| | Nr of faults | Fault coverage [%] | | |
|---|---|---|---|---|
| | | α=0.05 | α=0.1 | α=0.2 |
| 1st Stage Amplifiers | 45 | 81.5 | 100 | 100 |
| 2nd Stage Amplifiers | 119 | 56.3 | 68.9 | 70.6 |
| 1st and 2nd Stage Amplifiers | 164 | 67.8 | 78.8 | 84.9 |
| Folding Stage Amplifiers | 102 | 76.5 | 82.4 | 84.3 |
| Total without Folding Encoder | 266 | 68.4 | 78.2 | 93.5 |
| Folding Encoder | 96 | 66.7 | 85.4 | 85.4 |
| Total without DfT | 362 | 68.3 | 79.9 | 81.1 |
| Total with DfT (43 transistors) | 362 | 100 | 100 | 100 |
| Comparators Block | 1836 | 70.4 | 80.1 | 93.2 |
| Total Fine ADC | 2198 | 69.9 | 80.1 | 91.3 |

TABLE III
S/H TEST RESULTS

| | Nr of faults | Fault coverage [%] | | |
|---|---|---|---|---|
| | | α=0.05 | α=0.1 | α=0.2 |
| S/H 1 | 74 | 94.6 | 97.3 | 100 |
| S/H 2 | 74 | 98.6 | 100 | 100 |
| S/H 3 | 74 | 93.2 | 95.9 | 100 |
| Bias Circuit | 10 | 100 | 100 | 100 |
| Output Switches | 12 | 91.7 | 100 | 100 |
| Total | 244 | 95.5 | 97.9 | 100 |

TABLE IV
COARSE ADC TEST RESULTS

| | Nr of faults | Fault coverage [%] | | |
|---|---|---|---|---|
| | | α=0.05 | α=0.1 | α=0.2 |
| Preamplifier 1st stage Block | 54 | 25.9 | 57.4 | 81.5 |
| Preamplifier 2nd stage Block | 51 | 100 | 100 | 100 |
| Total without DfT | 105 | 61.9 | 78.1 | 90.5 |
| Total with DfT (21 transistors) | 105 | 100 | 100 | 100 |
| Comparators Block | 891 | 70.3 | 79.1 | 89.5 |
| Total Coarse ADC | 996 | 69.5 | 79.0 | 88.3 |

sub-blocks. Notice that the use of DfT, as shown in Table II, increases the fault coverage of the preamplifer stages and folding encoder to 100%. The undetected faults in the inactive parts of the comparator's decision stage and storage latch, expose the limitations of the quasi-static approach, due to the dynamic nature of the response. After test stimuli optimization, only 2 test stimuli are needed to achieve designated fault coverage from a given input stimuli ramps.

### *C. Signature Based Testing of Sample and Hold (S/H), Coarse ADC and Sub-DAC*

The rest of the observed ADC has been evaluated following the similar principles. The sample and hold (S/H) units are monitored in open-loop to prevent fault masking due to the feedback and common-mode regulation. The results with the DfT in place are shown in Table III. After test stimuli optimization, only five test stimuli are needed to achieve 95.5% fault coverage from the given input stimuli's ramps.

The fault coverage of 73.5, 81.3, and 90.6% for the probability $\alpha = 0.05, 0.1, 0.2$, respectively, is accomplished with only 2 optimized test stimuli for the 996 injected faults in the 5-bit coarse ADC as shown in Table IV.

Once again the faults responsible for the fast dynamic behavior of the comparators were not entirely captured by our approach. After test stimuli optimization, only two test stimuli's are needed to achieve the previously indicated fault coverage.

The total fault count for the resistor-ladder based sub-DAC is 323. Adapted ramp-down and ramp-up at the top and bottom of the reference ladder and adapted ramp-down (digital code from $2^N - 1$ to 0) and ramp-up (digital code from 0 to $2^N - 1$) at the input of the DAC have been offered and the current through the resistor ladder was measured. The fault coverage we obtained shows that the resistor-based DAC is not suitable for current signature-based testing without additional, application specific, adjustments.

## V. CONCLUSION

We presented an inexpensive structural methodology that intends to facilitate test pattern generation at wafer level test, thereby providing a quantitative estimate of the effectiveness and completeness of the testing process. The proposed fault model utilizes the sensitivity of the circuit's quasi-static node voltages to process variations and consequently the current deviance so as to differentiate the faulty behavior. To overcome system-test limitations of the structural current-based testing, the device-under-test is partitioned into smaller blocks with only limited additional hardware by means of the power-scan DfT technique. As the results indicate, most quasi-static failures in various blocks of the 12-bit multistep ADC, depending on the degree of partitioning, are detectable through power-supply current structural test offering more then twenty fold reduction in test time in comparison to more traditional, functional histogram-based static or FFT-based dynamic ADC test.

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