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Power Dissipation Minimization in RF Front Ends

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***Abstract*—In mobile and portable wireless devices, it is important to have low power dissipation so as to maximize battery life. As the overall power dissipation of a device is dominated by the radio frequency (RF) front end rather than the digital circuit, low-power RF front end design has become a very hot topic in both research and implementation. In this paper, we propose a design method to minimize the power dissipation of a RF front end. Specifically, given the overall specifications of gain, linearity and noise figure of a front end, we derive the optimal specification for each building block of the RF front end such that the overall power dissipation is minimized. By using a specific example of a front end consisting of a couple of cascaded circuit blocks using 90nm CMOS technology, we demonstrate that significant reduction in power dissipation can be achieved using the proposed design method.**

I. Introduction

In the past decade, there has been a rapid growth of mobile wireless devices in our everyday life, such as cellular phones, laptops. Most of these devices use batteries as power sources, hence, low power dissipation is essential. As the power dissipation of the radio frequency (RF) front end contributes a major part of the overall power dissipation in these devices, low-power RF front end design has been and will continue to be a very important topic in both research and implementation [1] [2].

Figure 1 illustrates a block diagram of a typical wireless receiver, which consists of an antenna, an RF front end, an analog to digital converter (ADC) and digital domain processing blocks. In the RF front end, the received signal from the antenna is first passed through the RF filter, which passes the signal in the desired frequency band while suppresses the out-of-band signals. The filtered signal is amplified using the low noise amplifier (LNA) and then mixed with the carrier signal generated from the local oscillator (LO) and converted to a lower frequency. The low frequency signal goes through a low-pass channel filter, whereby the out-of-channel signal is further suppressed and the filtered signal is then passed to the automatic gain controller (AGC).

In practical design of the RF front end, the specifications usually dictate an overall gain, noise figure (NF) and linearity (normally in terms of the third order interception point (IP3)). Based on these overall specifications, the specifications for different circuit blocks of the front end such as LNA, mixer and filters are derived. For a given overall front end specification, there are trade-offs between the specifications of different circuit blocks and the overall power dissipation.

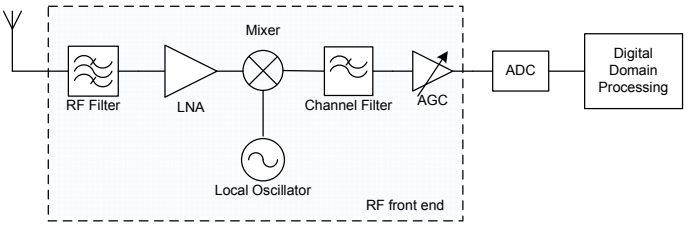

Fig. 1. Block diagram of a wireless receiver.

The minimization of the front end power dissipation is thus an optimization problem of finding the optimal combinations (trade-offs) of the circuit block specifications given that the overall front end specifications must be met. However, the trade-offs among different circuit blocks depend on the IC technology, the circuit topology, desired specifications and probably many more parameters [1]. This usually results in a very large number of possible combinations, which makes the optimization intractable. Attempts have been made to generate all possible circuit topologies [3] and to automatically find optimal parameter values [4]. However, these methods cannot cope with the typical complexity of front end circuit blocks in realistic periods of time. The growing demand for low-power front end demands new design methods.

It was shown in [5] that by using structure independent transforms (SIT), it is possible to trade linearity, gain and power dissipation of any circuits, independent of circuit topology, desired specifications and so on. With this, we are able to deal with the power dissipation minimization on a more abstract level. Specifically, we can consider the RF front end as a cascade of circuit blocks. For each circuit block, we have a library of finite possible circuit topologies. For each of these possible circuit topologies, we quantify its power efficiency using a single parameter, which we call the effective figure of merit (EFOM). The EFOM depends on circuit topology, IC technology *etc*. Using SIT, we can transform a particular circuit topology in a library to a circuit with desired specifications, without changing the EFOM. With these libraries and SIT's , the minimum-power front end design can be found using the following three steps:

1) For each circuit block, select from the corresponding circuit library the circuit that gives the best EFOM and that meets boundary conditions and requirements such as IC process, supply voltage, reverse isolation, *etc*.

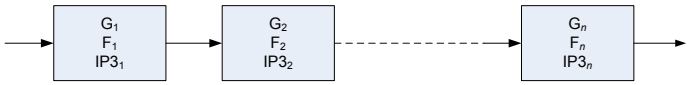

Fig. 2. A front end with cascaded circuit blocks.

2) Given the EFOM's of all chosen circuit blocks and the overall specifications of the front end, find the optimal combination of the circuit block specifications that minimize the power dissipation.
3) Use SIT to transform the chosen circuit for each circuit block to a circuit with the optimal specification.

Both step 1 and step 3 are straightforward. In this paper, we study how to find the optimal combinations of circuit block specifications as in step 2. This optimization problem for a cascade of two circuit blocks was solved in [1]. In this paper, we present a general solution for a front end with an arbitrary number of cascaded circuit blocks. We show that the optimization problem can be solved using Lagrange's multiplier theorem and has closed-form solutions. By considering a specific example of a front end consisting of an LNA , a mixer and an output buffer from recently published 90nm CMOS designs, we show that significant reduction in power dissipation can be achieved using the proposed design method.

The rest of this paper is organized as follows. We present the system model in Section II. The power minimization problem is formulated in Section III, it's closed-form solution is presented, and the derivation of this solution is deferred to the appendix. In Section IV, we use a specific example to demonstrate the reduction in power dissipation that can be achieved and the concluding remarks are given in Section V.

II. System Model

In this paper, we consider an RF front end consisting of a cascade of circuit blocks such as amplifiers, mixers, filters [1]. Figure 2 shows a front end with n cascaded blocks. We use G_i, F_i and IP3_i to denote the power gain, the noise figure and the IP3 of block i respectively. We also use G_{tot}, F_{tot} and IP3_{tot} to denote the overall specifications for the whole front end. The relationship between G_{tot} and G_i is given by

$$G_{\text{tot}} = \prod_{i=1}^{n} G_{\text{i}}. \tag{1}$$

The overall noise figure F_{tot} is related to the noise figure of each individual circuit block by Friis' formula [6]

$$F_{\text{tot}} - 1 = \sum_{i=1}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j}. \tag{2}$$

The overall IP3 can be obtained as

$$\text{IP3}_{\text{tot}} = \frac{1}{\sum_{i=1}^{n} \frac{\prod_{j=1}^{i-1} G_j}{\text{IP3}_i}}. \tag{3}$$

It was shown in [7] that assuming unilateral gains and matching, the power dissipation for block i can be approximated by,

$$P_i = \frac{f_i}{\kappa_i} G_i \text{IP3}_i, \tag{4}$$

where f_i is the power limiting bandwidth for block i. For a circuit block with a dominant pole, this is equal to the bandwidth of the circuit block. We use κ_i to denote the power linearity parameter for block i that depends on circuit topology, IC technology, etc. This parameter allows us to quantify the power efficiency of different circuit topologies in the same technology. Thus, we call κ the effective figure of merit (EFOM) for a particular circuit topology for a given technology. By using structure independent transforms (SIT), we can transform a particular circuit topology to a circuit with desired specifications in gain and IP3 without changing the value of EFOM [5]. Using (4), the overall power dissipation of the front end can be straightforwardly written as

$$P_{\text{tot}} = \sum_{i=1}^{n} P_i = \sum_{i=1}^{n} \frac{f_i}{\kappa_i} G_i \text{IP3}_i. \tag{5}$$

III. Problem Formulation and Solution

Given specifications on the overall gain, noise figure and IP3, there exist multiple combinations of gains, noise figures and IP3's of different circuit blocks that meet the overall specifications. The power dissipations for these combinations are obviously different. The goal in this paper is to find the optimal combination such that the overall power dissipation is minimized.

We assume that a library of "good" circuit blocks is available, from which the front end will be constructed. For each circuit block in the library, the parameters κ and F are known, which can be easily obtained in practice by circuit simulation. Moreover, depending on application, the power limiting bandwidth for each circuit block f_i is also known in advance. Therefore, the optimization problem can be formulated mathematically as follows:

Given:

$$\kappa_i > 0,\quad f_i > 0,\quad F_i > 1,\quad F_{\text{tot}} > 1,\quad G_{\text{tot}} > 0,\quad \text{IP3}_{\text{tot}} > 0$$

Find:

$$P_{\text{min}} = \min_{\substack{(G_1, G_2, \cdots, G_n) \\ (\text{IP3}_1, \text{IP3}_2, \cdots, \text{IP3}_n)}} \left(\sum_{i=1}^{n} \frac{f_i}{\kappa_i} G_i \text{IP3}_i \right)$$

Subject to:

$$G_{\text{tot}} = \prod_{i=1}^{n} G_{\text{i}} : \quad \text{gain constraint}$$

$$F_{\text{tot}} - 1 = \sum_{i=1}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j} : \quad \text{noise figure constraint}$$

$$\text{IP3}_{\text{tot}} = \frac{1}{\sum_{i=1}^{n} \frac{\prod_{j=1}^{i-1} G_j}{\text{IP3}_i}} : \quad \text{IP3 constraint}$$

The analytical solution of this optimization problem, as reported in the appendix of this paper, was first derived by A.J.E.M. (Guido) Janssen in 1999, when he was working at Philips Research Laboratories in Eindhoven. However, up to now, this result only received partial exposure in public literature, except in [7]. Denoting the gains of all circuit blocks by a vector $\mathbf{g} = [G_1, G_2, \cdots, G_n]$, this optimization problem can be solved in the following two steps:

- Step 1: For a given gain vector $\mathbf{g}$, find the optimal distribution of IP3's that leads to minimum power dissipation $P_{\text{min}|\mathbf{g}}$ subject to the IP3 constraint in (3).
- Step 2: Find the minimum power dissipation $P_{\text{min}} = \min\left(P_{\text{min}|\mathbf{g}}\right)$ among all possible gain vectors $\mathbf{g}$ that satisfy the total gain and noise figure constraints, i.e. $G_{\text{tot}} = \prod_{i=1}^{n} G_{\text{i}}$ and $F_{\text{tot}} - 1 = \sum_{i=1}^{n} \frac{F_i - 1}{\prod_{j=1}^{i-1} G_j}$.

Using Lagrange's multiplier, the minimum power dissipation in step 1 can be found as

$$P_{\text{min}|\mathbf{g}} = \text{IP3}_{\text{tot}} \left(\sum_{i=1}^{n} \sqrt{\frac{f_i}{\kappa_i} \prod_{j=1}^{i} G_j} \right)^2, \tag{6}$$

and the optimal distribution of IP3's is given by

$$\text{IP3}_i^o = \text{IP3}_{\text{tot}} \sqrt{\frac{\kappa_i \prod_{j=1}^{i} G_j}{f_i}} \frac{\sum_{j=1}^{n} \sqrt{\frac{f_j}{\kappa_j} \prod_{k=1}^{j} G_k}}{G_i}. \tag{7}$$

The optimization in step 2 can be solved using Lagrange's multiplier method too. The final optimal gains for different circuit blocks are given by:

$$\begin{aligned} G_1^o &= \sqrt[3]{\frac{\kappa_1 (F_2 - 1)^2}{f_1}} \frac{1}{F_{\text{tot}} - F_1} \sum_{j=1}^{n-1} \sqrt[3]{\frac{f_j}{\kappa_j} (F_{j+1} - 1)} \\ G_i^o &= \sqrt[3]{\left(\frac{F_{i+1} - 1}{F_i - 1}\right)^2 \frac{f_{i-1}}{\kappa_{i-1}} \frac{\kappa_i}{f_i}} \quad \text{for } i = 2, \cdots, n-1 \\ G_n^o &= \frac{G_{\text{tot}} (F_{\text{tot}} - F_1)}{\sum_{j=1}^{n-1} \sqrt[3]{\frac{f_j}{\kappa_j} (F_{j+1} - 1)}} \sqrt[3]{\frac{f_{n-1}}{\kappa_{n-1}} \left(\frac{\kappa_1}{f_1} \frac{1}{F_n - 1}\right)^2} \end{aligned} \tag{8}$$

Substituting the optimal gain distribution into (7), the optimal IP3 specifications are given by

$$\text{IP3}_i^o = \text{IP3}_{\text{tot}} \sqrt{\frac{\kappa_i \prod_{j=1}^{i} G_j^o}{f_i}} \frac{\sum_{j=1}^{n} \sqrt{\frac{f_j}{\kappa_j} \prod_{k=1}^{j} G_k^o}}{G_i^o}. \tag{9}$$

Finally the minimum front end power dissipation is given by

$$P_{\text{min}} = \text{IP3}_{\text{tot}} \left(\sqrt{\frac{f_n}{\kappa_n} G_{\text{tot}}} + \frac{\left(\sum_{i=1}^{n-1} \sqrt[3]{\frac{f_i}{\kappa_i} (F_{i+1} - 1)} \right)^{3/2}}{\sqrt{F_{\text{tot}} - F_1}} \right)^2 \tag{10}$$

The mathematical details of solving the optimization problem are given in the Appendix at the end of the paper.

From (10), we can see that given the overall specifications of G_{tot}, IP3_{tot} and F_{tot}, there are a couple of ways in reducing the minimum front end power dissipation. The most straightforward way is to choose circuit blocks with larger EFOM (κ_i). Another way is to choose the noise figure of the first block F_1 to be significantly smaller than the overall noise figure F_{tot}. This is because when F_1 is close to F_{tot}, a large gain G_1 is required at the first block to bring down the noise figure contributions from all subsequent blocks. This higher gain mean more power dissipation. Moreover, higher G_1 also means that signal amplitude after the first block is high, which results in a higher linearity requirement and again means higher power dissipation.

IV. Numerical Results

In this section, we use a numerical example to illustrate the reduction in power dissipation that can be achieved using the proposed design method. In particular, we study a typical front end consisting of three cascaded circuit blocks using 90 nm CMOS technology, an LNA [8], a mixer [9] and an output buffer [10]. The specifications of the three circuit blocks and the overall specifications of the front end are shown in Table I.

TABLE I
Specifications for a front end with 3 circuit blocks using 90nm CMOS technology.

	LNA	Mixer	Output Buffer	Overall
Gain (dB)	16	10.2	0	26.2
Noise Figure (dB)	1.7	9.1	16	2.4
IIP3 (dBm)	4	10.7	19	-9.6
f_i designed (MHz)	1500	2100	500	
$\kappa(\times 10^9)$	7.65	17.8	1.22	
Pow. Diss. (mW)	19.6	14.5	32.5	

We consider the front end in this example for IEEE 802.11b/g wireless LAN systems operating in the 2.4 GHz ISM band. In this case, the power limiting bandwidth is thus 100 MHz for the LNA, 2.5 GHz for the mixer and 30 MHz for the output buffer. With the new power limiting bandwidth, the power dissipations for the three circuit blocks become 1.31 mW, 17.3 mW and 1.95 mW respectively and the total power dissipation without optimization is 20.5 mW. After using the proposed optimization method, the optimal distribution of gain and linearity is summarized in Table II. We can see that the overall specifications on gain, linearity and noise figures are still met. The power consumption is reduced by about 50% from 20.5 mW to 10.0 mW. Note that this reduction can be achieved when optimizing purely for low power dissipation, whereas in practice there might be other considerations such as robustness, die area, stability *etc.* that might be traded off against the lowest possible power dissipation. Nevertheless, for such trade-offs, it is also very valuable to know the minimum power dissipation that is achievable.

TABLE II
Optimized gain linearity distribution for the front end.

	LNA	Mixer	Output Buffer	Overall
Gain (dB)	21.1	1.5	3.6	26.2
Noise Figure (dB)	1.7	9.1	16	2.4
IIP3 (dBm)	-0.9	14.3	17.7	-9.6
f_i (MHz)	100	2500	30	
Pow. Diss. (mW)	1.31	17.3	1.95	20.5
Opt. Pow. Diss. (mW)	1.36	5.28	3.37	10.0

Using the same front end example considered in Table I, we study how the difference between F_{tot} and F_1 affects the minimum power dissipation, P_{min} of the front end. Figure 3 shows the minimum power dissipation for different total noise figures. Here, we sweep the total noise figure F_{tot} from 1.8 dB to 5 dB, while keeping G_{tot}, IP3_{tot} and individual noise figure and κ for each circuit block fixed. Notice from (8)

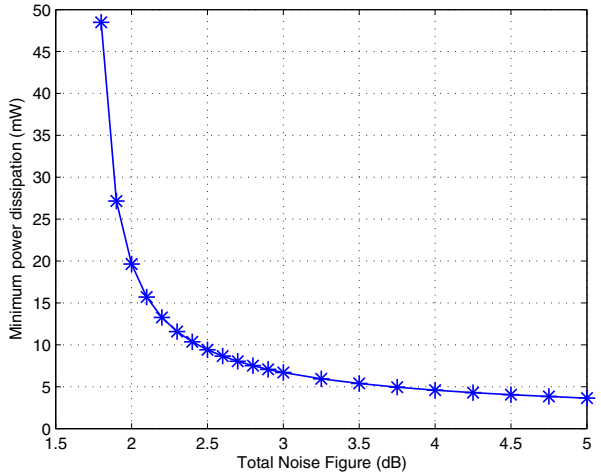

Fig. 3. Minimum power dissipation for different total noise figure values for a fixed $F_1 = 1.7$ dB.

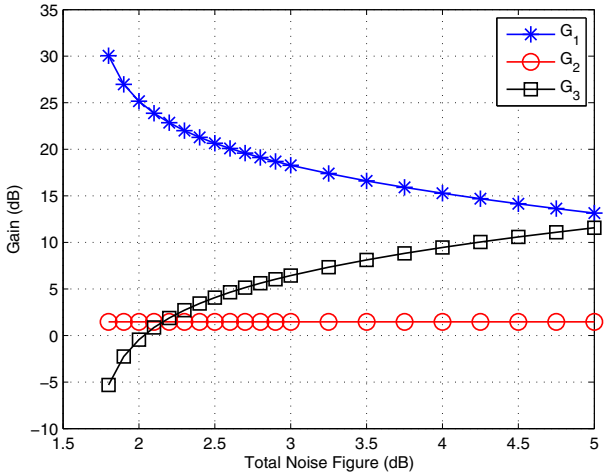

Fig. 4. Optimal Gain for different circuit blocks for different total noise figure values for a fixed $F_1 = 1.7$ dB.

and (9) that the optimal gains and IP3 for each circuit block will change due to the changing F_{tot}. From the figure, we can see that the power dissipation rises significantly when F_{tot} becomes close to the noise figure of the first circuit block $F_1 = 1.7$ dB. This is because when F_{tot} gets closer to F_1, the additional noise figure contribution allowed from subsequent blocks gets smaller. When the noise figures of subsequent blocks are fixed, this implies that G_1 must be increased significantly as shown in (2), which leads to higher power dissipation. This is confirmed by Figure 4, in which we plot the optimal gains of different circuit blocks. We can see that G_1 increases very quickly as F_{tot} gets smaller than 2.5 dB. Notice that G_2 remains constant because it is independent of F_{tot}. In addition, when G_1 increases, the amplitude of the signal at circuit blocks 2 and 3 increases. Therefore, as shown in Figure 5, the linearity requirements, i.e. IP3_2 and IP3_3, for blocks 2 and 3 also increase, which again leads to higher power dissipation. This is consistent with the discussion we had at the end of Section III.

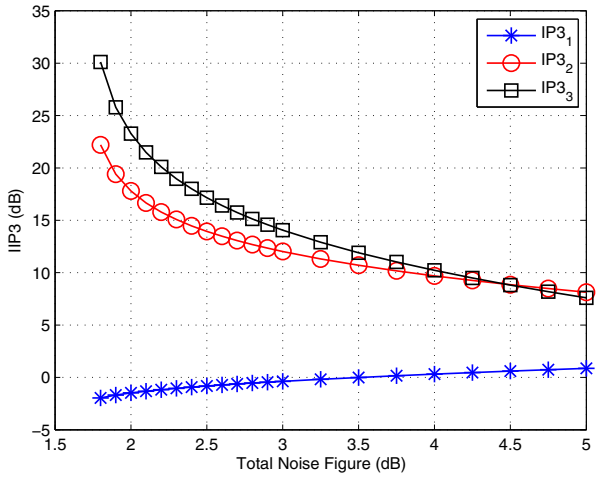

Fig. 5. Optimal IP3 for different circuit blocks for different total noise figure values for a fixed $F_1 = 1.7$ dB.

V. Conclusion

In this paper, we presented a method to minimize the power dissipation of a RF front end consisting of cascading circuit blocks. With given overall specifications on gain, noise figure and IP3, we showed that the optimal combinations circuit blocks specifications that minimizes the front end power dissipation can be obtained by concatenation of two applications of Lagrange's multiplier method. With an example of a front end consisting of an LNA, a mixer and an output buffer from state-of-the-art 90 nm CMOS technology, we show that a significant reduction of the front end power dissipation can be achieved using the proposed method.

Acknowledgment

We would like thank Dr. ir. A.J.E.M. (Guido) Janssen from Eindhoven University of Technology for the elegant solution of the optimization problem and for his help in improving the quality of this paper.

Appendix
Derivation of the optimal gain and linearity specifications for different circuit blocks

For ease of notation in the derivation, we define the following variables:

- $x_i = G_i\text{IP3}_i$: the output IP3 of circuit block i;
- $y_i = \prod_{j=1}^{i} G_i$: the partial gain from circuit block 1 to i.
- $\zeta_i = \frac{f_i}{\kappa_i}$.

With this, the Step 1 of the optimization problem in Section III can be written equivalently as

• `Step 1: For a given` $\mathbf{y} = [y_1, y_2, \cdots, y_n]$, `find` $\mathbf{x} = [x_1, x_2, \cdots, x_n]$ `that minimizes` $P_{\text{tot}|\mathbf{y}}(\mathbf{x}) =$

$\sum_{i=1}^{n}\zeta_i x_i$, subject to: $\sum_{i=1}^{n}\frac{y_i}{x_i} = \frac{1}{\text{IP3}_{\text{tot}}}$ (the IP3 constraint).

Using a Lagrangian multiplier λ, we define the cost function in step 1 as

$$\mathcal{J}_1(\mathbf{x},\lambda) = P_{\text{tot}}(\mathbf{x}) - \lambda\left(\sum_{i=1}^{n}\frac{y_i}{x_i} - \frac{1}{\text{IP3}_{\text{tot}}}\right). \quad (11)$$

The minimum of $P_{\text{tot}}(\mathbf{x})$ occurs when

$$\nabla_{\mathbf{x}}\mathcal{J}_1(\mathbf{x},\lambda) = 0, \quad (12)$$

or, equivalently, when

$$\nabla_{\mathbf{x}}P_{\text{tot}}(\mathbf{x}) = \lambda\nabla_{\mathbf{x}}\left(\sum_{i=1}^{n}\frac{y_i}{x_i}\right). \quad (13)$$

This gives

$$\zeta_i = -\lambda\frac{y_i}{x_i^2}, \quad (14)$$

and so $x_i = \sqrt{-\lambda\frac{y_i}{\zeta_i}}$. Substituting this into (5), we get that the minimum power is given by

$$P_{\text{min}|\mathbf{y}}(\mathbf{x}) = \sum_{i=1}^{n}\zeta_i x_i = \sqrt{-\lambda}\sum_{i=1}^{n}\sqrt{\zeta_i y_i}. \quad (15)$$

Notice that to satisfy the IP3 constraint, we have

$$\frac{1}{\text{IP3}_{\text{tot}}} = \sum_{i=1}^{n}\frac{y_i}{x_i} = \frac{1}{\sqrt{-\lambda}}\sum_{i=1}^{n}\sqrt{\zeta_i y_i}, \quad (16)$$

and this gives that the minimum power dissipation for a given $\mathbf{y}$ and IP3_{tot} is given by

$$P_{\text{min}|\mathbf{y}} = \text{IP3}_{\text{tot}}\left(\sum_{i=1}^{n}\sqrt{\zeta_i y_i}\right)^2 = \text{IP3}_{\text{tot}}\left(\sum_{i=1}^{n}\sqrt{\zeta_i\prod_{j=1}^{i}G_j}\right)^2. \quad (17)$$

.

Then, step 2 of the optimization problem can be written as

- Step 2: Minimize

$$P_{\text{min}|\mathbf{y}} = \texttt{IP3}_{\texttt{tot}}\left(\sum_{i=1}^{n}\sqrt{\zeta_i y_i}\right)^2$$

subject to $y_0 = 1$, $y_n = G_{\text{tot}}$ (the gain constraints) and $\sum_{i=0}^{n-1}\frac{F_{i+1}-1}{y_i} = F_{\text{tot}}$ (the noise figure constraint).

Again, for the ease of notation in step 2, we define the following variables:

- $a_i = F_{i+1} - 1$, for $i = 0, \cdots, n-1$;
- $a = F_{tot} - 1$;
- $z_i = \sqrt{y_i}$ and $\mathbf{z} = [z_1, \cdots, z_n]$.

Now the minimum power dissipation for a given $\mathbf{y}$ can be re-written as

$$\begin{aligned} P_{\text{min}|\mathbf{y}} &= \text{IP3}_{\text{tot}}\left(\sum_{i=1}^{n}\sqrt{\zeta_i}z_i\right)^2 \\ &= \text{IP3}_{\text{tot}}\left(\sqrt{\zeta_n G_{\text{tot}}} + \sum_{i=1}^{n-1}\sqrt{\zeta_i}z_i\right)^2. \end{aligned} \quad (18)$$

Notice that both IP3_{tot} and $\sqrt{\zeta_n G_{\text{tot}}}$ in (18) are constants. Therefore, the minimization of $P_{\text{min}|\mathbf{y}}$ is equivalent to the minimization of

$$Q(\mathbf{z}) = \sum_{i=1}^{n-1}\sqrt{\zeta_i}z_i. \quad (19)$$

Moreover, using the new variables, the noise figure constraint is given by $\sum_{i=0}^{n-1}\frac{a_i}{y_i} = a$. This is equivalent to

$$\sum_{i=1}^{n-1}\frac{a_i}{y_i} = a - a_0 \triangleq c,$$

as $y_0 = 1$ and $a_0 = F_1 - 1$ is a constant. Now, step 2 of the optimization problem can be simplified to

- Step 2': Minimize

$$Q(\mathbf{z}) = \sum_{i=1}^{n-1}\sqrt{\zeta_i}z_i$$

subject to $\sum_{i=0}^{n-1}\frac{a_i}{z_i^2} = c$.

Using a Lagrangian multiplier μ, we can write the cost function in step 2' as

$$\mathcal{J}_2(\mathbf{z},\mu) = Q(\mathbf{z}) - \mu\left(\sum_{i=1}^{n-1}\frac{a_i}{z_i^2} - c\right). \quad (20)$$

Again, at the minimum of $Q(\mathbf{z})$, we have $\nabla\mathcal{J}_2(\mathbf{z},\mu) = 0$ or equivalently

$$\nabla_{\mathbf{z}}Q(\mathbf{z}) = \nabla_{\mathbf{z}}\left(\sum_{i=1}^{n-1}\sqrt{k_i}z_i\right) = \mu\nabla_{\mathbf{z}}\left(\sum_{i=1}^{n-1}\frac{a_i}{z_i^2}\right). \quad (21)$$

This gives

$$z_i = \sqrt[3]{-2\mu}\sqrt[3]{\frac{a_i}{\sqrt{\zeta_i}}}. \quad (22)$$

Using the noise figure constraint, we get

$$\sum_{i=1}^{n-1}\frac{a_i}{z_i^2} = \sum_{i=1}^{n-1}\frac{a_i}{\frac{(-2\mu a_i)^{2/3}}{\zeta_i^{1/3}}} = c, \quad (23)$$

and $\sqrt[3]{-2\mu} = \frac{1}{\sqrt{c}}\sqrt{\sum_{i=1}^{n-1}a_i^{1/3}\zeta_i^{1/3}}$. Substituting this into (22), we get the minimum power dissipation given by

$$\begin{aligned} P_{\text{min}} &= \text{IP3}_{\text{tot}}\left(\sqrt{\zeta_n G_{\text{tot}}} + \sum_{i=1}^{n-1}\sqrt{\zeta_i}z_i\right)^2 \\ &= \text{IP3}_{\text{tot}}\left(\sqrt{\zeta_n G_{\text{tot}}} + \frac{1}{\sqrt{c}}\left(\sum_{i=1}^{n-1}\sqrt[3]{a_i\zeta_i}\right)^{3/2}\right)^2 \\ &= \text{IP3}_{\text{tot}}\left(\sqrt{\frac{f_n}{\kappa_n}G_{\text{tot}}} + \frac{\left(\sum_{i=1}^{n-1}\sqrt[3]{\frac{f_i}{\kappa_i}(F_{i+1}-1)}\right)^{3/2}}{\sqrt{F_{\text{tot}}-F_1}}\right)^2. \end{aligned} \quad (24)$$

Similarly, the optimal gain distribution can be obtained as

$$
\begin{aligned}
G_1^o &= z_1^2 = \sqrt[3]{\frac{\kappa_1 (F_2-1)^2}{f_1}} \frac{1}{F_{\text{tot}} - F_1} \sum_{j=1}^{n-1} \sqrt[3]{\frac{f_j}{\kappa_j}(F_{j+1}-1)} \\
G_i^o &= \frac{z_i^2}{z_{i-1}^2} = \sqrt[3]{\left(\frac{F_{i+1}-1}{F_i - 1}\right)^2 \frac{f_{i-1}}{\kappa_{i-1}} \frac{\kappa_i}{f_i}} \quad \text{for } i = 2, \cdots, n-1 \\
G_n^o &= \frac{G_{\text{tot}}}{z_{n-1}^2} = \frac{G_{\text{tot}} (F_{\text{tot}} - F_1)}{\sqrt[3]{\frac{f_1 (F_2-1)^2}{\kappa_1}} \left(\sum_{j=1}^{n-1} \sqrt[3]{\frac{f_j}{\kappa_j}(F_{j+1}-1)} \right)} \cdot \\
&\qquad \cdot \frac{1}{\left(\prod_{j=2}^{n-1} \sqrt[3]{\left(\frac{F_{j+1}-1}{F_j - 1}\right)^2 \frac{f_{j-1}}{\kappa_{j-1}} \frac{\kappa_j}{f_j}} \right)} \\
&= \frac{G_{\text{tot}} (F_{\text{tot}} - F_1)}{\sum_{j=1}^{n-1} \sqrt[3]{\frac{f_j}{\kappa_j}(F_{j+1}-1)}} \sqrt[3]{\frac{f_{n-1}}{\kappa_{n-1}} \left(\frac{\kappa_1}{f_1} \frac{1}{F_n - 1} \right)^2}
\end{aligned} \tag{25}
$$

and, finally, the IP3 distribution is given by

$$
\text{IP3}_i^o = \frac{x_i}{G_i} = \text{IP3}_{\text{tot}} \sqrt{\frac{\kappa_i \prod_{j=1}^{i} G_j^o}{f_i}} \frac{\sum_{j=1}^{n} \sqrt{\frac{f_j}{\kappa_j} \prod_{k=1}^{j} G_k^o}}{G_i^o}. \tag{26}
$$

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