Expanding Thermal Plasma Deposition of a-Si:H Thin Films for Surface Passivation of c-Si Wafers,

molecule and polymer materials such as Alq_3 (Tris(8-hydroxyquinolinato)aluminium), MEH-PPV and conducting polymer PEDOT:PSS (Poly(3,4-ethylenedioxythiophene) poly(styrene sulfonate)); (2) polymeric barrier film such as cyclic olefin copolymer (COC) and Teflon®; and (3) nanocomposite materials based on TiO_2 and metal nanoparticles that serve as brightness enhancement layers and transparent conducting electrodes.

The deposited films are characterized by SEM (scanning electron microscopy) and FTIR (Fourier-transform infrared spectroscopy), photo- and electroluminescence. We will also present the comparison of film properties as they depend on different mid-infrared laser choices, such as a picosecond, tunable free electron laser (FEL), Er;YAG laser and picosecond optical parametric oscillator (OPO).

4:00pm **TF-ThA7 Room Temperature Synthesis of Silica and SiO_2-TiO_2 Composites for use as Barrier and Anti-Reflection Coatings**, ***P.C. Rowlette***, *C.A. Wolden*, Colorado School of Mines

Thin film oxides are ubiquitous in photovoltaics, serving as transparent electrodes, passivation layers, optical coatings, and moisture permeation barriers. Pulsed plasma enhanced chemical vapor deposition (PECVD) was used to deliver digital control of SiO_2, TiO_2, and $Si_xTi_yO_z$ composites at room temperature. Sub-angstrom control of SiO_2 deposition rate was demonstrated by varying the $SiCl_4$ density at low exposure levels (~250 L). No impurities were detected by XPS or FTIR, and the high film quality was confirmed by etch rate measurements. Crack-free SiO_2 films have been deposited on polymer substrates, and we are currently assessing their barrier performance.

Next, SiO_2-TiO_2 composites were formed by pulsed PECVD using $SiCl_4$ and $TiCl_4$ as precursors. The refractive index of the SiO_2-TiO_2 material system spans a large dynamic range (n: 1.4 – 2.4), and as such is of great interest for optical coatings. Alloy formation was investigated by maintaining constant delivery of one precursor while varying the second. Film composition was assessed by spectroscopic ellipsometry, XPS, and FTIR. It is shown that the alloy composition and refractive index can be tuned continuously over this broad range using pulsed PECVD. These two precursors were found to be highly compatible, with the alloy growth rate simply reflecting the sum of the contributions from the two individual precursors. The digital control over both thickness and composition offered by pulsed PECVD was demonstrated through room temperature synthesis of antireflection (AR) coatings for crystalline silicon solar cells. One, two, and three-layer AR coatings based on the range of indices offered by the SiO_2/TiO_2 system were designed and optimized to minimize the reflectance across the visible spectrum. AR coatings based on these designs were then fabricated, and in each case the measured optical performance was found to be in excellent agreement with model predictions. The integrated reflectance across the visible spectrum was reduced from 39% for uncoated wafers to 2.5% for the 3-layer AR coating.

4:20pm **TF-ThA8 Expanding Thermal Plasma Deposition of a-Si:H Thin Films for Surface Passivation of c-Si Wafers**, ***A. Illiberi***, *V. Verlaan, M. Creatore, W.M.M. Kessels, M.C.M. van de Sanden*, Eindhoven University of Technology, The Netherlands

We investigated the material properties of expanding thermal plasma deposited a-Si:H thin films, providing a record-low surface recombination velocity of 1.6 cm/s (at injection level of 1 10^{15} cm^{-3}). a-Si:H thin films with different thicknesses have been deposited at a high deposition rate (1.2 nm/s) on both sides of low resistivity (1-5 Ohm cm), 260μm thick, *n*- and *p*-type c-Si FZ wafers. The material properties of a -Si:H films have been characterized by Fourier Transform Infrared diagnostic and Spectroscopic Ellipsometry. The surface passivation of the wafers has been determined by photoconductivity decay measurements of the effective carrier lifetime. The investigation points out that the growth of ETP a-Si:H films begins with the formation of a thin porous layer (< 10 nm) with a refractive index of 3.9 (at 2 eV) and a microstructure parameter (R*) of 0.50. Despite the open network formation at the a-Si/c-Si interface, a 7 nm a-Si:H film achieves a recombination velocity as low as 12 cm/s (at $1 \cdot 10^{15}$ cm^{-3} injection level on n-type wafers). The good passivation is probably due to the large hydrogen content of the a-Si:H film, which terminates dangling bonds present on the c-Si surface. After this initial growth, a dense a-Si:H network develops with a refractive index of 4.3 (at 2 eV) and R* = 0.03. The surface recombination velocity decreases linearly with the a-Si:H thickness, achieving a record value of 1.6 cm/s (at $1 \cdot 10^{15}$ cm^{-3} injection level) for 90 nm thick a-Si film on n-type wafers. As compared to hot wire CVD and radiofrequency PECVD techniques, ETP is capable to deposit thin a-Si:H films with outstanding surface passivation at higher temperature (250° C) and higher deposition rate (1.2 nm/s). The stability in time of surface passivation has been investigated. Effective carrier lifetime is found to decrease following a stretched exponential. Photo-electronic properties of a-Si:H are know to relax in time in a similar fashion. These results therefore suggest a correlation between the photo-electronic properties of the a-Si:H/c-Si interface and a-Si:H bulk material.

4:40pm **TF-ThA9 Effect of Oxygen Incorporation on the Properties of CdS/CdTe Interface and the Device Properties**, ***R.G. Dhere***, *J.N. Duenow, S.E. Asher, Y. Yan, M. Young, T.A. Gessert*, National Renewable Energy Laboratory

The development of CdTe solar cells over the last 35 years has been advanced by introducing various modifications in the fabrication process such as post-deposition $CdCl_2$ heat treatment and CdS deposited by chemical-bath deposition (CBD). The presence of oxygen during various stages of CdTe/CdS device fabrication is also known to benefit device performance. The first devices reported by Kodak to have efficiencies greater than 10% were fabricated by close-spaced sublimation (CSS) in oxygen ambient. $CdCl_2$ heat treatment, crucial for achieving high efficiency, is usually carried out in ambient containing O_2. In previous studies on devices fabricated using CBD CdS, CSS, and sputtering, the interdiffusion at the CdS/CdTe interface was correlated to the presence of O_2 in CBD CdS. We have fabricated devices with sputtered CdS films that have efficiencies near 14%, comparable to our baseline devices using CBD CdS. In this paper, we present our recent work on CdTe devices using CdS prepared by sputtering and CBD. For sputtered CdS films, we varied O_2 content in the sputtering ambient from 0% to 3%. CdTe films were deposited by CSS in oxygen ambient and conventional physical vapor deposition in high vacuum. We will present detailed characterization of the CdS/CdTe interdiffusion at the interface. Specifically, we used secondary-ion mass spectrometry for samples fabricated under different conditions to investigate the dependence of interdiffusion characteristics on oxygen ambient during fabrication. We will also present the results of our transmission electron microscopy analysis on the structural properties of the CdS/CdTe interface and its correlation to the microstructure of CdS deposited by both techniques as well as oxygen in the fabrication process. We will fabricate devices using the samples from these studies and characterize the devices using standard current-voltage analysis. We will then analyze the results to correlate the device properties to the interface properties.

5:00pm **TF-ThA10 Large-Scale Simulations of Nanoimprint Lithography**, ***M. Chandross***, *G.S. Grest*, Sandia National Laboratories

The production of surfaces with controllable/tunable nanostructures over large areas and at throughputs practical for commercial applications can be very difficult. Two processes of recent interest have been step-flash imprint lithography (SFIL) and nanoimprint lithography (NIL) in which nanoscale masks are imprinted into polymeric materials to create features with nm-scale resolution. Empirical approaches are currently the norm for industrial scale-up but are often prohibitively time-consuming and expensive. Modeling and simulation can decrease manufacturing process design cycle time enormously, as has been proven in many industry segments.

Here we present our activities specifically with regard to nanopatterning by detailed large-scale simulations of nanolithographical processes in which rigid molds are imprinted into liquid oligomers that are subsequently hardened. We use a generic polymer model that can be applied to both SFIL, in which the oligomers are cross-linked by exposure to UV irradiation, and NIL, in which the liquid is hardened by lowering the temperature below the glass transition. Multiple stamps are inserted into melts of liquid oligomers at a temperature above the glass transition. The melts are either quenched or croslinked and the systems are equilibrated. Stamps are then either removed at constant velocity to study the effects of stress and adhesion on resulting features, or simply deleted to study the effects in the limit of zero stress. We vary the size and pitch of the stamps in order to study the resolution limits of both methods.

5:20pm **TF-ThA11 All through Stencil MOSFET Fabrication**, ***L.G. Villanueva***, *O. Vazquez-Mena*, EPFL, Switzerland, *J. Montserrat*, IMB-CNM-CSIC, Spain, *K. Sidler, V. Savu*, EPFL, Switzerland, *J. Bausells*, IMB-CNM-CSIC, Spain, *J. Brugger*, EPFL, Switzerland

The fabrication of micro and nano devices using standard processing techniques is mainly based on the pattern transfer of designs onto a substrate. These standard techniques use pre-patterned resists that selectively expose certain parts of the substrate either to material deposition or implantation or to an etching process. The use of resist processes implies the coating, exposure, development and removal of the resist and also imposes certain restrictions regarding the materials and substrates to pattern (e.g. only flat substrates are acceptable). An alternative to resist-based processes is the use of stencil lithography (SL), which relies on the use of a shadow mask membrane, and has already been proved to achieve sub-micrometer resolution for metallization, and more recently for direct-etching and ion-implantation. In this abstract we present the combination of