A 13.56 MHz RFID system based on organic transponers

A 13.56-MHz RFID System Based on Organic Transponders

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***Abstract*—RFID tags based on organic transistors are described, discussing in detail the IC blocks used to build the logic and the radio. Tags energized and read out at 13.56 MHz, *de facto* standard frequency for item-level identification, have been tested and enabled for the first time multiple-object identification, using different 6-bit codes. A complete 64-bit transponder, the most complex organic RFID tag reported to date, operates at 125 kHz and employs 1938 transistors.**

***Index Terms*—Organic integrated circuits, organic thin-film transistors (OTFTs), passive RFID, pentacene, radio-frequency identification (RFID), RF-DC conversion.**

I. Introduction

THE range of applications of radio frequency identification (RFID) tags is rapidly growing. Starting from the traditional markets of ticketing and supply chain management, RFIDs will be used in the coming years to allow identification of more and more kinds of goods in retail shops. To facilitate this trend, low-cost RFID systems need to be built. Nowadays very small silicon RFID chips costing few dollar cents are a reality, but these components need to be assembled with antennas to build the full RFID transponder. Until now the cost of antennas and assembly does not seem to have come down as much as one would desire.

An attractive solution to this problem would be to manufacture antenna and electronics on the same substrate (possibly the wrapping of the item to be identified) using in-line production techniques like printing [1]. Electronics made with organic transistors is a low-temperature technology based on materials available in fluid form and can be produced using printing techniques [2]. Organic electronics could thus enable the production of complete ultra-low-cost RFID tags. However, the level of complexity and performance achieved by organic RFID tags manufactured using printing and even lithography is still not sufficient to enable real-world applications. Fully functional 15-bit code generators [3] and 13.56-MHz RFID radios able to send a square wave signal to the reader [4] have been demonstrated using lithographic production processes. In this paper, we present more advanced results, publishing for the first time [5]:

- organic RFID transponders able to send multi-bit identification messages to the base station using the standard frequency for silicon-based item-level RF identification: 13.56 MHz
- complex identification codes (64-bit) generated by RF-powered organic tags.

The paper is organized as follows. Sections II–IV provide an overview of the technology of organic transistors, a summary of their electrical performance and a description of the main circuit building blocks used in the tags. Sections V and VI present the tags we fabricated and their performance, and Section VII summarizes the conclusions.

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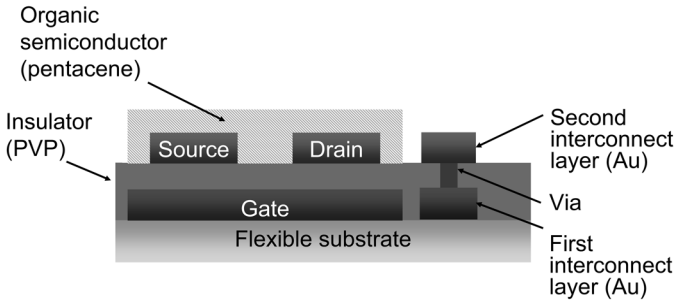

Fig. 1. Cross-section of an organic thin-film transistor.

II. Organic Integrated Circuits Technology

All integrated circuits described in this paper have been manufactured on a 150-mm process line using a 25-μm-thick polyimide foil as substrate. The foil is laminated on a rigid support to facilitate handling and the different production steps. Thin film transistors (TFTs) are fabricated using a bottom gate structure, as shown in Fig. 1 [6]–[8]. A 50-nm Au layer is deposited onto the substrate and patterned using standard photolithographic techniques and wet etching to build the transistor gates and a first interconnect layer. An insulating polymer is then spin-coated onto the wafer and holes are photochemically defined into the insulator to host the vertical interconnects (vias). A second Au layer is deposited on the stack and patterned to define the source and drain contacts together with a second interconnect layer and the vias. A solution of a precursor of the organic semiconductor pentacene is spin-coated on top of the stack, and the precursor film is converted to pentacene using standard procedures described in [9]. The semiconducting

TABLE I
TYPICAL ELECTRICAL PROPERTIES OF THE ORGANIC TFTS USED TO BUILD LOGIC CIRCUITS

Electrical parameter	Value	Measurement conditions
V_t [V]	2.5	
g_m[S]	3.1×10^{-8}	V_{gs} = 0V, V_{ds} = -20V
	1.1×10^{-6}	V_{gs} = -20V, V_{ds} =-20V
R_{out}[Ω]	5.3×10^{8}	V_{gs} = 0V, V_{ds} between -20V and -2V
f_t [kHz]	20	V_{gs} = 0V, V_{ds} = -20V
	740	V_{gs} = -20V, V_{ds} =-20V

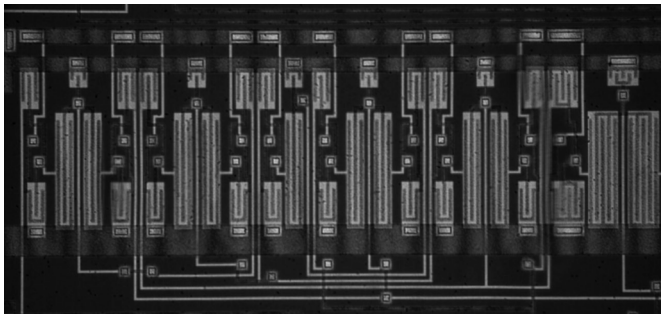

Fig. 2. Micrograph of an organic D-flip-flop.

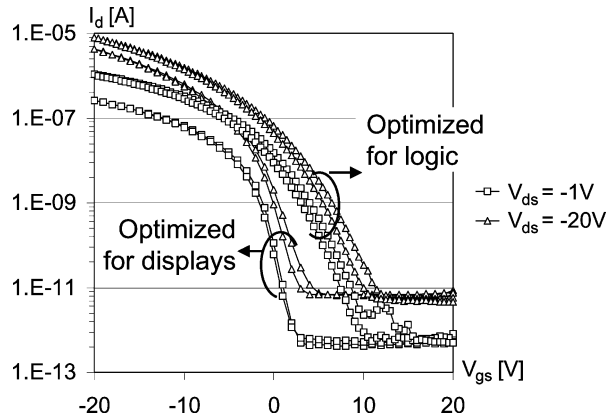

Fig. 3. $I_d - V_{gs}$ characteristics of two organic transistors, one optimised for display applications and the other optimised for logic. V_{gs} is swept from 20 V to -20 V and vice versa, to show that hysteresis is negligible.

material is removed from the areas outside the transistor gates to provide high insulation from transistor to transistor. The film carrying the transistors can be diced and released from the support when the process is complete without damaging the electronics. The rigid supports can be reused.

Transistor gate length can be scaled down to 1 μm [6], but the circuits described in this paper use a minimum feature size of 4 μm. The channel length is 4 μm, source and drain fingers are 4 μm wide, and vias have 4 μm by 4 μm contacts within a 12 μm by 12 μm overlap of the first and second interconnect layer (Fig. 2). The 150-mm technology described allows integration of complex circuits made with organic transistors. Fig. 2 shows a micrograph with a detail of one of our circuits.

III. CHARACTERISTICS AND MODELLING OF THE ORGANIC INTEGRATED TRANSISTORS

Pentacene, like most air-stable organic semiconductors, is p-type in ambient conditions: in our technology we thus have only p-type transistors. As one can see in Fig. 3, organic TFTs are operated between an "on" state, where the p-type semiconductor is accumulated of majority carriers at the interface with the dielectric ($V_{gs} < V_{fb}$), and an "off" state where the semiconductor film is progressively depleted of holes ($V_{gs} > V_{fb}$). As a consequence, the threshold voltage V_t for an organic transistor can be assumed to be equal to the flat band voltage V_{fb} of the gate-insulator-semiconductor system. In organic transistors, the threshold voltage cannot be controlled using ion implants to dope the semiconductor as in silicon technology; however, different applications often require different threshold values.

If mobile ions or trapped charge in the gate dielectric can be neglected, the threshold voltage is given by [10]

$$V_t = V_{fb} = \phi_{ms} - \mathrm{Q}_f/C_i = \phi_m - (\chi + E_g/2q + \psi_B) - \mathrm{Q}_f/C_i \quad (1)$$

where ϕ_{ms} is the difference in work function between the metal and the semiconductor, determined by the work function of the metal ϕ_m, the semiconductor electron affinity χ, the bandgap E_g and the difference ψ_B between the Fermi level and the intrinsic Fermi level. Q_f is the surface concentration of fixed charges at the gate dielectric/semiconductor interface and C_i is the unit area gate capacitance. According to (1) the threshold voltage can be modified choosing suitably:

- the work function of the gate material;
- the doping level of the semiconductor, which will reflect on the Fermi level of the semiconductor;
- the fixed charge at the semiconductor-insulator interface.

In our technology, we can adjust the threshold voltage (Fig. 3) changing the nature and the quantity of the chemicals added to the semiconducting film before the conversion step. In this way, one can influence the doping level (and possibly also the electrical properties of the semiconductor-insulator interface). Thin film transistors developed to become switches in active matrix displays [11], [12] will have a steep subthreshold slope and $V_t \approx 0$ V (Fig. 3), to act as much as possible as ideal switches. Transistors used in p-type static digital logic will be normally on (Fig. 3), in order to provide an adequate load to build logic gates, as will be explained in Section IV.

The main electrical properties of the organic TFT developed to build logic and shown in Fig. 3 are summarized in Table I.

Assuming that charge transport is a thermally activated tunnelling of holes between localized states in an exponential density of states (Variable Range Hopping), one can accurately model the transistor characteristic in accumulation [13]. According to this model, the mobility in the accumulation regime depends on the gate voltage

$$\mu = \mu_0(-V_{gs} + V_t)^{\gamma} \text{ for } \mathrm{V}_{gs} < V_t \quad (2)$$

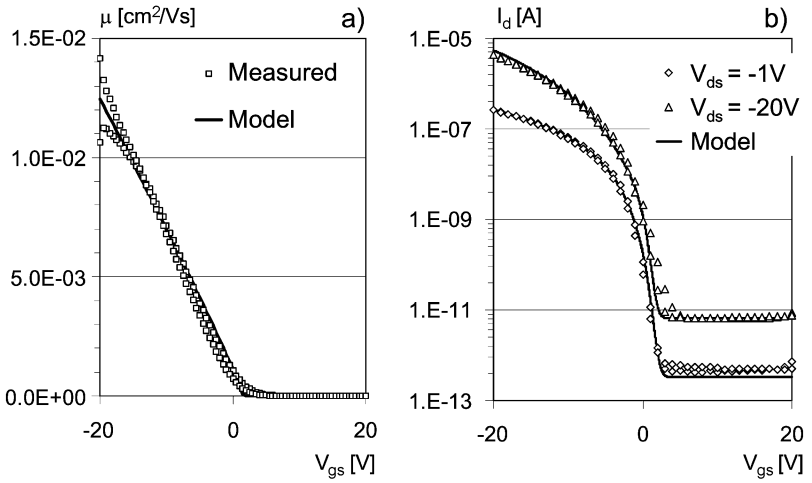

Fig. 4. (a) Mobility dependence on V_{gs}, measured (open symbols) and modelled (continuous line) using (2). The measurements are obtained sweeping V_{gs} from 20 V to -20 V and vice versa. (b) Measured (open symbols) and modelled (continuous line) transfer characteristic. All regimes of operations are included in a nine-parameter model that also accounts for scaling [15].

where V_t is the threshold voltage, μ_0 is the mobility prefactor and γ is the mobility exponent. Equation (2) agrees well with experimental data for gate voltages within the commonly used supply range ($-20\ \mathrm{V} < V_{gs} < 0\ \mathrm{V}$), as shown in Fig. 4(a).

A complete model based on (2) and able to fit the static current–voltage characteristics of our organic TFTs under all bias conditions, using nine parameters, has been developed [Fig. 4(b)] [8], [14]. This model is used for transistor level simulation of the digital logic, together with a simple description of the device capacitances, inspired to standard silicon MOS device physics.

IV. Circuit Building Blocks

A. Logic Gates

In this subsection, we will describe the logic blocks used to build the code generators in the organic RFID chips. Readers who are interested in a more detailed discussion of organic logic gates should refer to [8], [15], and [16].

1) Inverters With Zero-V_{gs} Load: All logic gates used to build the digital circuits presented in this paper are based on the zero-V_{gs} load inverter. A circuit schematic of this inverter is presented in Fig. 5(a). An input-output characteristic is presented in Fig. 5(b). On this characteristic are shown the most relevant electrical properties: the stable logic high and low values (V_{high} and V_{low}), the trip voltage (V_{trip}, where $V_{\mathrm{in}} = V_{\mathrm{out}}$), the point of maximum gain (A_{max}) and the noise margin, defined as the side of the largest square that can be inscribed between the input-output characteristics and the mirrored characteristic that gives V_{in} as a function of V_{out} [drawn in light gray in Fig. 5(b)].

The load transistor, M_2, is connected to have $V_{gs} = 0$ V and is designed to be r_w times wider than the driver, M_1. When the input voltage V_{in} is high ($V_{\mathrm{in}} = \mathrm{Gnd}$), both M_1 and M_2 have $V_{gs} = 0$ V and the load transistor, which is wider, will pull down the output node V_{out} against the driver. The ratio r_w thus determines the value of V_{low}. When the input voltage V_{in} is low ($V_{\mathrm{in}} = -V_{dd}$), the driver transistor switches on and pulls up V_{out} against the weak load offered by M_2.

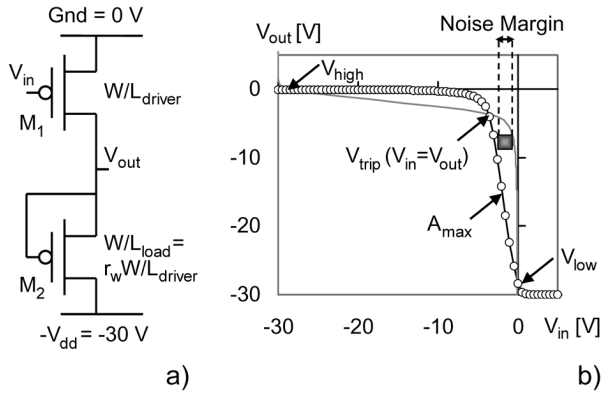

Fig. 5. (a) Schematic and (b) measured transfer characteristic (open symbols) of an inverter with zero-V_{gs} load.

In order to have sufficient noise margin, the separation between V_{high} and V_{low} must be maximized. At the same time the gain must be maximized. Unfortunately these design objectives put contrasting requirements on the width of the load transistor. If M_2 is made wider, V_{low} will be closer to $-V_{dd}$, while V_{high} will be only slightly changed. On the other end, a wider M_2 will decrease the resistance of the output node and therefore decrease the gain A_{max}. The maximum achievable gain is determined by the semiconductor mobility and the output resistance of the transistors (for a more detailed discussion the reader is referred to [15]).

As one can see by examining Fig. 5(b), the noise margin is severely limited by the asymmetric position of the trip point, which should ideally be ($V_{\mathrm{in}} = -V_{dd}/2$, $V_{\mathrm{out}} = -V_{dd}/2$). The fact that only one transistor threshold is available in our technology is responsible for this asymmetry. To assure sufficient pull-down current and reasonable switching speed to the inverter, the threshold voltage should be slightly positive, so that the zero-V_{gs} load transistor is on. On the other end, due to the positive threshold, the driver transistor is rapidly switched on enough to pull up the load when the input voltage is lowered, and the trip value is reached already for V_{in} still close to Gnd. The

TABLE II
WAFER-LEVEL STATISTICS OF THE NOISE MARGIN MEASURED FOR DIFFERENT KINDS OF INVERTERS ($V_{dd} = 30$ V)

Type of inverter		Average noise margin [V]
Zero V_{gs} load		2.04
Diode load		0.64
Diode load with level shifter	V_{ss} = 7V	1.84
	V_{ss} = 10V	2.05
	V_{ss} = 13V	2.03

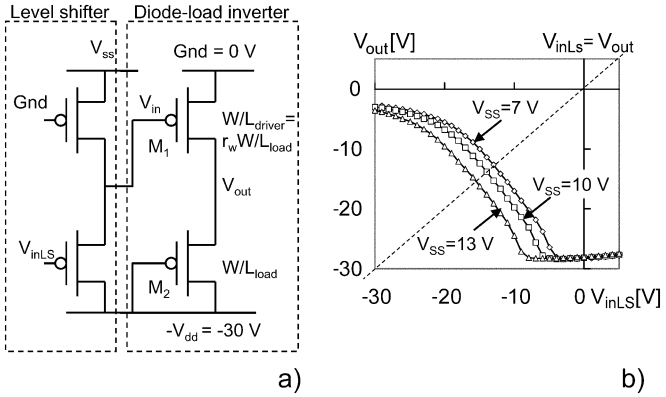

Fig. 6. (a) Schematic and (b) measured transfer characteristic of an inverter with diode load and level shifter.

trade-off between pull-down speed and position of the trip point (*i.e.* noise margin) is the most difficult to solve when tuning the technology parameters. In this work, we choose $V_t = 2.5$ V (Table I) and $r_w = 8$, obtaining at $V_{dd} = 30$ V a typical noise margin of 2 V (Table II) and a pull-down speed in the range of 1 ms with fan-out of one. It is interesting to note that one would prefer to have a negative threshold for the driver transistor. This would shift the transfer characteristic of Fig. 5(b) to the left, improving the symmetry of the trip point and hence the noise margin.

2) Inverters With Diode Load and Level Shifters: The alternative two-transistor inverter, where the load M_2 is a diode-connected transistor, is shown in Fig. 6(a). To ensure proper functionality, in this inverter the driver must be r_w times wider than the load.

The diode-load inverter is much faster than the zero-V_{gs} inverter presented in the previous subsection, because of the larger pull-down current. However, the low resistance of the output node decreases the gain and, for our technology, results in very low noise margin (as can be seen in Table II). This situation can be improved by cascading a level shifter stage to the input (or the output) of the diode-load inverter, as shown in Fig. 6(a) [17]. The level shifter translates the input-output characteristic of the diode-load inverter towards the left, improves the symmetry of the trip point and results in better noise margin [see Fig. 6(b) and Table II]. The impact of the level shifter on the dynamic behavior of the complete logic gate is limited, thanks to the significant pull-up and pull-down currents flowing in the level-shift branch [Fig. 6(a)]. Using diode-load inverters with level shifters we were indeed able to build 32-stage shift registers (a total of 1888 transistors) working at a clock speed of 5 kHz [16], one of the highest speeds reported to date for complex organic circuits. Summarizing, these inverters guarantee good speed and sufficient noise margin, but they necessitate an additional, adjustable power supply V_{ss} and require more power than zero-V_{gs} inverters. The generation of an additional low-impedance rail would add complexity to the RFID chip, and the higher power dissipation would negatively affect the reading distance of the RFID system. This considered, we decided to postpone the use of diode-load logic with level shifters in RFID systems to further developments, where a higher switching speed will be needed for the logic.

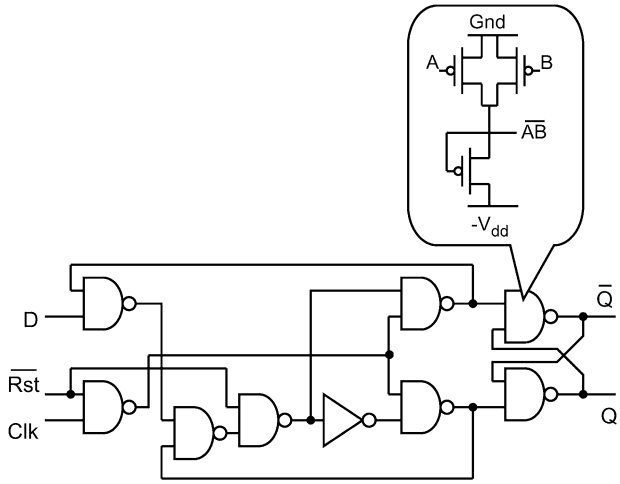

Fig. 7. Schematic of a D-flip-flop with active-low asynchronous reset (Rst). The inset shows the transistor level schematic of a NAND gate.

3) Other Logic Blocks: By adding a second driver transistor to the zero-V_{gs} inverter, one can easily build logic NAND gates (Fig. 7). Using inverters and NAND gates together, any combinatorial and sequential function can be generated. The schematic of the D-flip-flop with asynchronous reset used in the code generator described in Section VI is also shown in Fig. 7.

B. Radio-Frequency Part of the Identification Transponders

1) Antennas for Low-Cost RFID and Rectifier Circuits: Ultra-low cost antenna solutions are of fundamental importance in building low-cost RFID transponders. Due to the low mobility observed in present organic semiconductors (10^{-2} to about 1 cm^2/Vs), state-of-the-art organic semiconductor devices are able to rectify the incoming RF power only at the two lower bands used in identification: 125 kHz and 13.56 MHz [18], [19]. In this subsection, we will analyse the advantages and disadvantages of capacitive and inductive RF energy transmission at these frequencies.

In our technology, diodes are formed using transistors identical to the ones used to build logic (Fig. 8). To keep a simple flow chart and avoid additional process steps, we do not use dedicated vertical Schottky diodes [4], [18].

A schematic drawing of an RFID system based on capacitive coupling is shown in Fig. 8(a). M_1 is a p-type FET. It is diode-connected and rectifies the incoming RF voltage. Transistor M_2 is also diode-connected and provides a return path to the DC current flowing through M_1. The AC current injected in node 2 by the parasitic capacitances of transistor M_1 flows through the large decoupling capacitance $C_{\rm dc}$ ($C_{\rm dc} \approx 30$ pF for the code generators in Section VI, compared to the about 0.5 pF of the

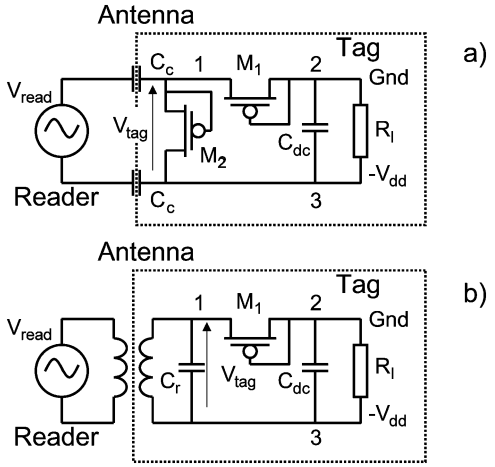

Fig. 8. Schematic drawing of an organic tag using (a) capacitive and (b) inductive coupling.

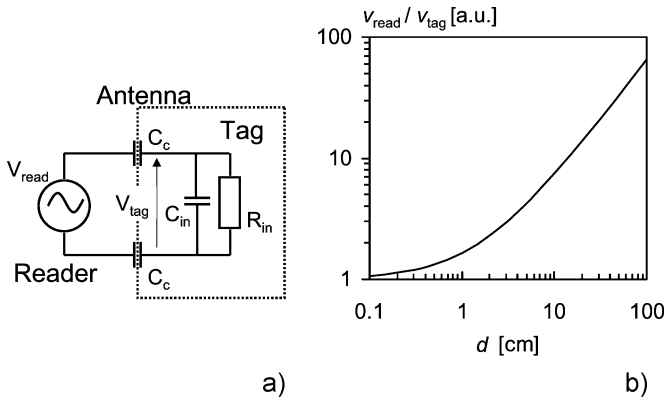

Fig. 9. (a) Equivalent circuit of a capacitive coupled tag and (b) reader voltage normalized to the tag voltage ($v_{\rm read}/v_{\rm tag}$) versus separation distance d.

total parasitic capacitances of M_1) and only minimally affects the DC voltage generated on the load.

In order to evaluate how far we can place a capacitive coupled tag from the reader antenna, we can replace the rectifier with its equivalent input impedance $R_{\rm in}//C_{\rm in}$ [Fig. 9(a)], following the approach described in [20]. The equivalent input capacitance can be approximately assumed equal to the C_{gs} in the linear regime of transistor M_1. Here we consider M_1 and M_2 to be identical and we assume that during a complete period $V_{\rm tag} = v_{\rm tag}\sin(\omega t)$ either M_1 or M_2 is on and in the linear regime ($V_{gs} = V_{ds}$ and $V_t > 0$). In our rectifiers, we will thus have $C_{\rm in} \approx 0.5$ pF. The equivalent resistance can be evaluated assuming the dissipation in the transistor M_1 and M_2 to be negligible with respect to the dissipation in the load, and equating the DC power dissipated on the load, $P_{\rm load}$, to the power dissipated on the equivalent resistance $R_{\rm in}$ by the incoming AC voltage:

$$v_{\rm tag}^2/(2R_{\rm in}) = P_{\rm load} -> R_{\rm in} = v_{\rm tag}^2/(2P_{\rm load}) \qquad (3)$$

Considering that the maximum load dissipation in our systems is $P_{\rm load} \approx 300\ \mu$W and that the minimum amplitude of the input voltage on the tag needed in our systems is (see Section V) $v_{\rm tag} \approx 60$ V, the minimum value of $R_{\rm in}$ will be $R_{\rm in} \approx 6$ MΩ. Using the equivalent circuit of Fig. 9(a) we can now plot a conservative estimate of the voltage amplitude needed on the reader antenna $v_{\rm read}$ to obtain a given voltage amplitude on the tag $v_{\rm tag}$, as a function of the coupling capacitance C_c, i.e., of the separation distance d between reader and tag antenna. The result for a frequency of the AC signal of 125 kHz and two equal coupling pads on the tag fitting the size of an ISO credit card (5 cm by 8 cm) is shown in Fig. 9(b). Considering that the minimum voltage amplitude needed on the tag, $v_{\rm tag}$, is about 60 V, and that practical readers will generate $v_{\rm read} < 1000$ V, the maximum reading range will be approximately 10 cm.

The advantage of capacitive coupling is that the antenna is a conductive pad of large cross-section, and presents limited ohmic losses. The capacitive coupling can thus be realized with ultra-low cost, highly ohmic antenna pads on the tag side, made with thin metallic layers or even printed with carbon charged inks [21], [22].

A schematic of an inductively coupled RFID system is shown in Fig. 8(b). In this system, the tag antenna forms a parallel resonant tank with the capacitance C_r. The resonant tank is tuned at the RF frequency used to transmit the power to the tag and, offering large impedance at resonance, maximizes the received voltage, allowing the rectifier M_1 to function properly at a much larger distance from the energizing antenna than a capacitive coupled solution. To give an example, the typical maximum reading distance at 13.56 MHz for an inductively coupled silicon tag of the size of a credit card is 1.3 m for a field strength of 0.115 A/m at 80 cm from the transmitter antenna (ISO 15963 standard, assuming a tag that needs less than 1 mW power and at least 3 V DC supply for proper operation [23]). Inductive coupling is preferred as long as the Q factor of the on-tag resonant tank can be made high ($\rm Q > 10$). At relatively low frequencies the antenna must have large inductance and a low DC resistance R_L to achieve a sufficient unloaded quality factor $\rm Q_L$ ($\rm Q_L = \omega L/R_L$). For a 120 loop antenna fitting on a credit card, a $\rm Q_L = 28$ at 125 kHz would require a DC resistance $R_L = 6.8\ \Omega$, or 3.1 m of 100 μm thick copper wire. Such an antenna would be expensive, and so in our system we preferred capacitive coupling, which allows low-cost energy transfer also at 125 kHz, in spite of the smaller reading range.

2) Modulator: The usual way to transmit the code from an RFID tag back to the reader is to modulate the current flowing between nodes 2 and 3 (Fig. 8) with a transistor in parallel to the load, whose gate is connected to $\rm Gnd$ or $-V_{dd}$ in synchronous with the code ("load modulation" [24]). In this way, the power dissipated in the load $P_{\rm load}$ changes, and according to (3), changes the equivalent input resistance $R_{\rm in}$. The change in the impedance connected to the tag antenna can be easily detected on the reader side, so that the code is transmitted back to the reader.

In the previous subsection, we analysed the basic rectifier circuit used for capacitive coupling. In this circuit, transistors are used as diodes. This allows us to combine the function of rectification and load modulation using the scheme shown in Fig. 10 to send the code to the reader. In this circuit [25], the gate of the transistor M_1 is connected to the high DC voltage $\rm Gnd$ or

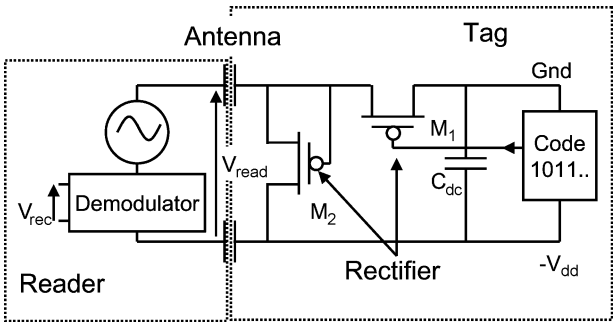

Fig. 10. Schematic of the capacitive coupled organic rectifier-modulator circuit.

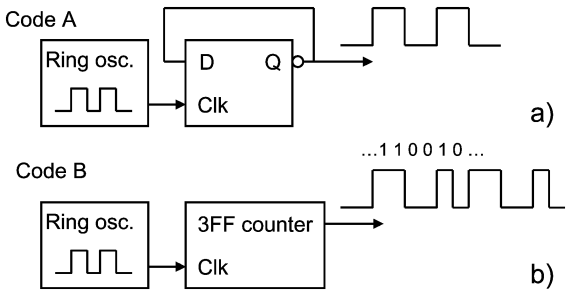

Fig. 11. Schematic of the two 6-bit code generators.

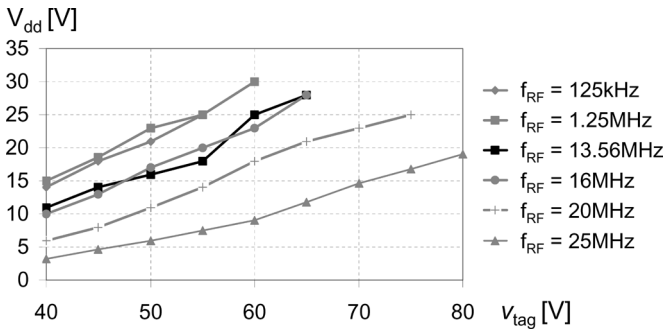

Fig. 12. Organic rectifier output V_{dd} measured for different amplitudes $v_{\rm tag}$ and frequencies $f_{\rm RF}$ of the incoming AC voltage.

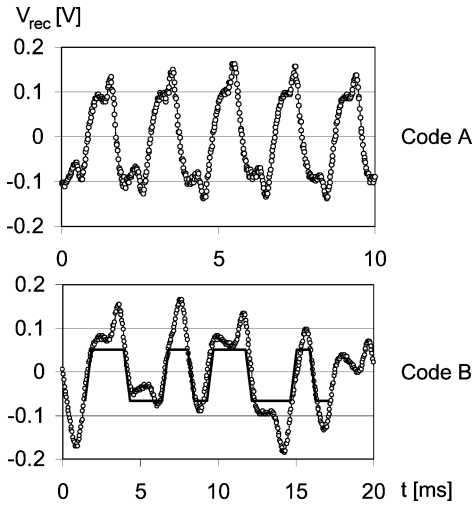

Fig. 13. Output codes of a "code A" and a "code B" tag energized and readout through a capacitive antenna using a 13.56-MHz RF voltage.

to the low one, $-V_{dd}$ depending on the value of the code generated. This alters the maximum V_{gs} applied to transistor M_1 during its conducting phase and causes a variation in load current and in $P_{\rm load}$ synchronous with the code, which is detected on the reader side.

V. 13.56-MHz Tags

A. Tag Architecture

In order to test the performance of our rectifier/modulator in realistic conditions, we designed and manufactured tags where this circuit is used together with small code generators. The tag "A" sends out a 1 0 1 0 1 0 ... sequence, generated by a ring oscillator connected to a toggle flip-flop to obtain a 50% duty cycle [Fig. 11(a)]. Tag "B" sends out a six-bit repetitive sequence 1 0 11 00 ... generated by a three flip-flop counter [Fig. 11(b)]. The two sequences can be easily distinguished.

B. Measurement Results

The rectifier circuit, loaded with code "A" and "B" generators, was measured for several frequencies of the incoming RF energy, $f_{\rm RF}$. In Fig. 12, the output DC voltage generated on the tag (V_{dd}) is recorded as a function of the amplitude of the voltage coupled to the tag antenna, $v_{\rm tag}$ and for different $f_{\rm RF}$. The results are very promising: the rectifier generates a sufficient DC output for the code generator (>20 V) for frequencies as high as 20 MHz. We also bonded code "A" and "B" tags to a capacitive antenna and measured on the reader side the code sent out by the complete transponders when energized with an RF wave at 13.56 MHz. Measurements were performed with the transponder in close proximity to the reader antenna. Results are given in Fig. 13: the two codes are clearly received and can be distinguished. This measurement is the first reported evidence of multi-bit RF identification of organic tags at 13.56 MHz [5]. The data rate is 1 kb/s for code "A" and 700 b/s for the code "B" tags, and the AC voltage on the tag antenna has an amplitude $v_{\rm tag} = 60$ V, generating a tag supply of $V_{dd} = 25$ V.

C. High Frequency Behaviour of the Rectifier-Modulator Circuit

The mobility measured in our transistors for $V_{gs} = -20$ V is $\mu \approx 10^{-2}$ cm^2/Vs [Fig. 4(a)]. If one would calculate the time of flight of a hole injected by the source to reach the drain, at $V_{gs} = V_{ds} = -100$ V (about the maximum bias reached in the rectifier transistor M_1), this would be

$$t_{\rm flight} = L^2/(\mu|V_{ds}|) \approx 160\ {\rm ns}. \quad (4)$$

According to this calculation, the rectifier should work only at frequencies much lower than $1/t_{\rm flight} = 6.25$ MHz, while Fig. 12 shows that the rectifier works at more than 20 MHz. The measured speed could be explained by the fact that the mobility increases with the gate bias (2). Unfortunately, a first experimental check shows that (2) is valid for $-V_{gs}$ as large as 30 or 40 V, but at higher gate bias the mobility tends to saturate to a constant value.

A better explanation comes from studying the time constant with which the charge sheet under the gate builds up, exponentially approaching its final value, after a change in V_{gs}. The time

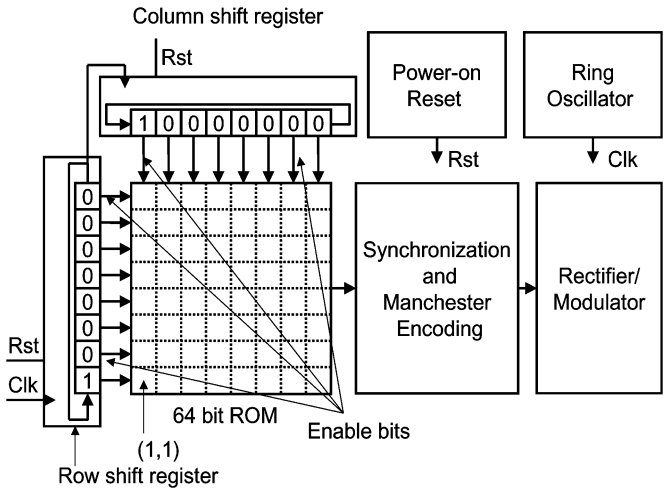

Fig. 14. 64-bit code generator schematic.

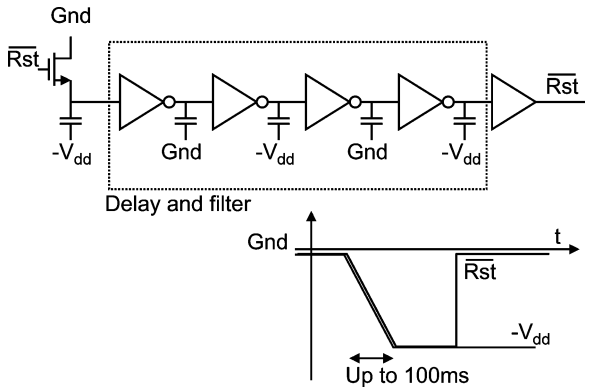

Fig. 15. Power-on reset schematic.

constant for this process was determined theoretically and experimentally to be [26]

$$\tau = L^2/\left(\mu|V_{gs}|\pi^2\right) = L^2/\left(\mu|V_{ds}|\pi^2\right) \tag{5}$$

This value, in our bias conditions, is a factor $\pi^2 = 9.87$ smaller than t_{flight} and might justify our experimental observations. In fact, when the charge sheet is accumulated under the gate, conduction will take place immediately between source and drain, which means that the time delay to switch on a diode-connected transistor is given by (5) rather than by (4). A more direct and detailed understanding of the measurements shown in Fig. 12, taking into account the specific geometry and bias conditions of our devices, is still needed, however.

VI. 64-bit Code Generators and Tags

A. Tag Architecture

The use of organic RFID in item level identification makes it necessary in many cases to be able to store and transmit a sizable amount of data. The electronic product code (EPC)[1], for instance, consists of 96 bits. It is still extremely challenging to build large code generators in organic technology. In order to demonstrate that organic electronics can be used to build tags for real-world applications, we designed and manufactured a 64-bit tag, consisting of a code generator and the rectifier-modulator circuit shown in Fig. 10. The architecture chosen for the 64-bit code generator is shown in Fig. 14. It has been selected for its optimum testability and the low probability of critical races. The 64-bit hardwired memory matrix is read out sequentially. Columns are enabled one by one from left to right and one row a time is read within the enabled column. At power-up the two barrel connected shift registers receive a reset. In this state, only one flip-flop per shift register is set and the first row and column are enabled. The data (1,1) is then synchronized with the clock and passed to the Manchester encoder and to the modulator. Each subsequent clock shifts up the row enable bit and sends the content of a new row in the first column to the modulator. After the enable bit reaches the highest position in the row shift register, it is shifted back to the lowest position while the column-enable bit is shifted to the right. In this way, the content of the entire memory is sent sequentially to the modulator. In a test version of the chip, all enable bits can be observed on a probe station and the memory can be read out generating enable bits from the outside.

The schematic of the power-on reset is shown in Fig. 15: it is simply a delay line that widens and shapes the power-on pulse seen between Gnd and $-V_{dd}$. No bandgap circuit is used.

A micrograph of the manufactured circuit is shown in Fig. 16. It contains 1938 transistors and measures 9 mm by 5 mm.

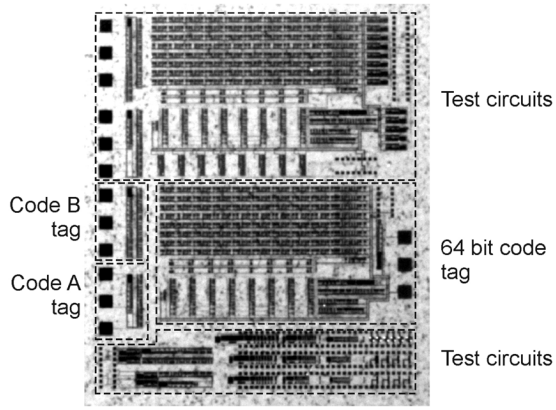

Fig. 16. Micrographs of the "code A", "code B", and 64-bit transponders.

B. Measurement Results

Fig. 17 shows the results of measurements performed on the row-enable shift register. The first two enable bits, D_0 and D_1, are plotted: enable bits are active low. An asynchronous external reset is applied (Rst active low): during this phase D_0 and D_1 are enabled and disabled respectively. The clock signal does not affect this state, as desired. When the reset is released the state of D_0 passes on to D_1 in one clock period and the whole cycle is repeated every eight-clock periods. The clock frequency is 300 Hz

[1]EPCglobal. [Online.] Available: http://www.epcglobalinc.org/

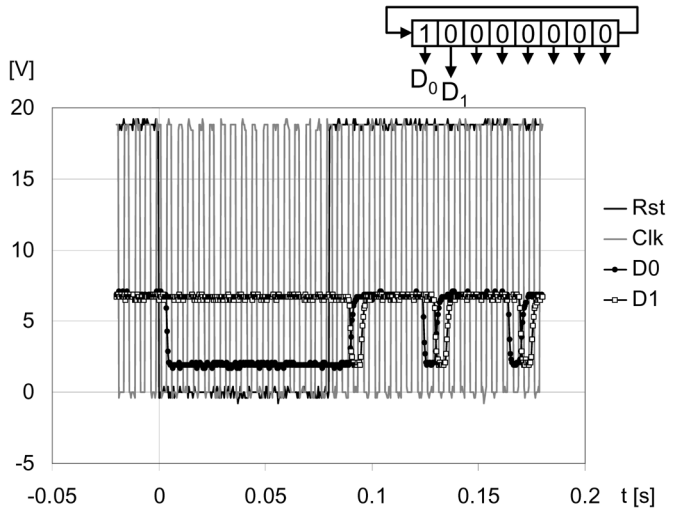

Fig. 17. Measurement of the row-enable shift register. $V_{dd} = 20$ V, $f_{\rm clk} = 300$ Hz.

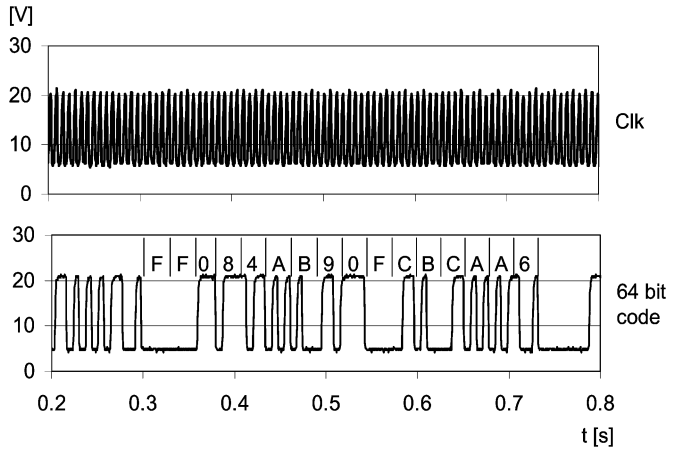

Fig. 18. Measured 64-bit code waveform compared to the bits stored in memory. $V_{dd} = 30$ V, bit rate 150 b/s.

and $V_{dd} = 20$ V. The output buffer used for off-chip measurements limits the voltage swing of D_0 and D_1. Fig. 18 demonstrates the complete functional 64-bit code generator. In this figure, we show the internally generated clock ($f_{\rm clk} = 150$ Hz, $V_{dd} = -30$ V) and the output code before the Manchester encoding. This code corresponds to the bits hardwired in the memory, which are superimposed to the electrical waveform. The 64-bit code generator was also measured together with the integrated rectifier-modulator. These tags work in air generating the Manchester code when in close proximity to the reader sending to its antenna a voltage amplitude $v_{\rm read} = 90$ V at 125 kHz.

VII. Conclusion

In this paper, we published for the first time multi-bit organic RFID transponders read-out using an RF frequency of 13.56 MHz. We also showed a fully functional 64-bit code generator complete with rectifier/modulator, one of the most complex organic circuits ever built, with its 1938 transistors. These results, coupled with the possibility of manufacturing with organic electronics a rewritable, non-volatile memory based on ferroelectric polymers [27], allow us to conclude that commercial item-level identification with organic tags at 13.56 MHz is now technically feasible. In order to fully exploit the low-cost potential of organic TFT technology, integration of tag electronics and antennas on the same substrate using in-line production processes should be pursued.

Acknowledgment

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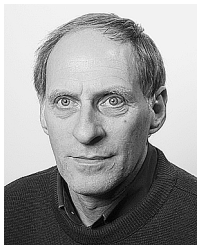

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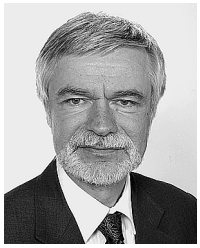

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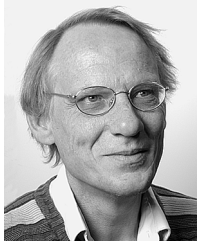

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