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A compact equivalent-circuit model for ferroelectric switching devices is derived from a general model for local charge displacements. The general model consists of a matrix of repeat units describing local dissipationless charge displacements (electrostatic channel), as well as dissipative charge displacements (electrochemical channel), the channels being coupled due to the electrical charge of the moving species. The derived model for ferroelectric charge displacements is used to simulate both hysteresis and transient characteristics, and applied to two devices: (i) a ferroelectric capacitor and (ii) a ferroelectric memory field-effect transistor. The circuits are programmed in SPICE-derived analysis software. We find that experimental hysteresis data obtained on $Pb(Zr,Ti)O_3$ ceramic capacitors and on thin-film transistors with a SnO_2:Sb semiconductor and a $Pb(Zr,Ti)O_3$ ferroelectric insulator can be reproduced and interpreted with the equivalent-circuit models. © *1999 American Institute of Physics.* [S0021-8979(99)02011-3]

I. INTRODUCTION

Ferroelectric material, once electrically polarized, remains polarized even in the absence of an electric field. This is due to hysteresis in the polarization response of the ferroelectric material to electric fields. Two remnant polarizations are available, of opposite polarity but equal magnitude. Data-storage devices with a ferroelectric component make use of these states. The two possible remnant polarizations are related to a logic ''0'' and ''1'', memory states that can be stored without needing a supply voltage or cyclic refreshing. The ferroelectric component can also offer a low programming voltage, radiation hardness, and nondestructive read out. Owing to these properties, ferroelectric memory devices such as ferroelectric random-access memories[1] and ferroelectric memory field-effect transistors (FEMFETs, see for example Refs. 2–4) are being developed.

Ferroelectric device models can be used to support the process of integration of devices such as FEMFETs within complicated circuitry, as well as provide deeper understanding of the device physics. In the absence of an analytical description of ferroelectric charge switching, models that approximate (part of) the switching process have been developed in the past.[5] Some models[6,7] consist of a set of physics-based operation equations to be evaluated by means of mathematical software. Other, so-called behavioral models[8–11] translate experimentally observed ferroelectric switching behavior into an equivalent circuit for device simulation. Here, we present a model that combines a phenomenological equivalent circuit with physics-based operation equations. Programmed by means of SPICE-derived device-simulation software,[12] the model is compact and requires minimal mathematical efforts. As examples we will show that the model can be used to reproduce the electrical characteristics of a ferroelectric capacitor and of a FEMFET.

II. CHARGE-DISPLACEMENT MODEL

In this section we explain the conceptual origin of our compact model for ferroelectric switching. It starts with the observation that the movement of charge in a material is partly accompanied by energy dissipation and partly dissipationless. For example, the polarization of core electronic states is dissipationless, while the hopping of free carriers or migration of ions involves the dissipation of energy. In a one-dimensional model the dissipationless charge movement is described by a serial arrangement of capacitors [Fig. 1(a)]. Nodal point i between capacitors C_{i+1} and C_i defines the *electrostatic potential* V_i at point x_i. The displaced charge per unit area Q_i displaced in capacitor C_i depends on the drop of electrostatic potential $V_i - V_{i-1}$.

Dissipative charge transport of particles of species s (e.g., electrons) is described by a serial arrangement of resistors [Fig. 1(b)]. At the nodal points i^s the *electrochemical potential* V_i^s of species s at position x_i is defined, assuming local thermal equilibrium. The current flowing through resistor R_i^s depends on the local drop of electrochemical potential $V_i^s - V_{i-1}^s$. The channel for dissipative transport of species s (R_i^s) is coupled to the electrostatic backbone (C_i) when species s carries electrical charge. The coupling strength—in our model given by $C_i^{\mathrm{DOS},s}$—is proportional to the local density of states per unit energy [see Fig. 1(c)].[13,14] For unit-charge particles $C_i^{\mathrm{DOS},s} = e^2 \times \mathrm{DOS}_s$, where DOS_s is the density of states for species s (units $\mathrm{m}^{-3}\mathrm{J}^{-1}$).

The equation describing the charge displaced in capacitors and the current flowing through resistors can be a linear as well as nonlinear function of the potentials, depending on

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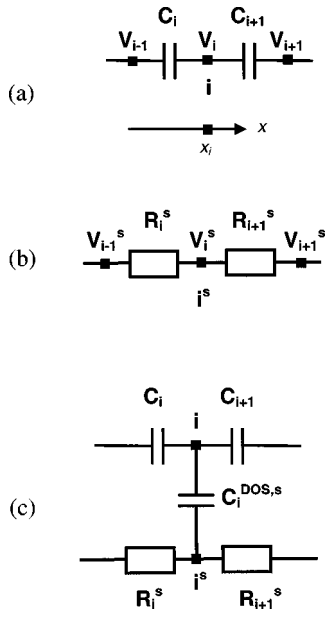

FIG. 1. Equivalent-circuit model of dissipationless (a) and dissipative (b) charge movement along a direction designated as the x direction. At $x=x_i$ an electrostatic potential V_i is defined at node i and an electrochemical potential V_i^s at node i^s for every species s of moving charge. The two types of charge-movement channels (a) and (b) are combined in panel (c). The capacitors $C_i^{\mathrm{DOS},s}$ relate to the local density of s-particle states in the material. When using this circuit to describe a one-dimensional system, the unit of C_i and $C_i^{\mathrm{DOS},s}$ is Farad. For a three-dimensional system the unit is $\mathrm{F/m^2}$.

the physical equations governing the charge movement. If more than one species is being transported, the model consists of parallel channels s that all link to the electrostatic channel (the backbone) at nodal points i^s with DOS capacitors $C_i^{\mathrm{DOS},s}$. In the following section we will explain how these principles can lead to a compact equivalent-circuit model of ferroelectric material.

III. FERROELECTRIC MODEL

Ferroelectric materials are characterized by bistable charge-displacement characteristics. The bistability is generally caused by off-centered ions in the atomic unit cell each of which can flip from one off-center position to the other when it has sufficient energy to overcome the energy barrier in between the two positions.[15] Thus, in its simplest form, the charge displacement in ferroelectric material involves the dissipative transport of one species of charge (i.e., ions) within the atomic unit cells. In Fig. 2 we propose a system of ferroelectric model units that represent atomic unit cells. The dissipative movement of ionic charge within unit i is modeled by resistor R_i. The ions cannot cross the unit-cell boundaries; the interaction with neighboring cells is of an electrostatic nature only, so that the channel of dissipative transport (the serial arrangement of R_is) is interrupted in between the ferroelectric units. The coupling between the movement of ions and the local electrostatic potential is described by capacitors $C_i'^{\mathrm{DOS,ion}}$ and $C_i^{\mathrm{DOS,ion}}$. Because of the inability of ions to cross the unit-cell boundaries, we use two of such DOS capacitors for one nodal point i while in Fig. 1 a single capacitor is used. It is a general property of ferroelectric materials that the polarization stabilizes at high applied electric field, so that the DOS capacitors are of a saturating nature. A bistable system is created when the resistors R_i have a strongly nonlinear current–voltage characteristic. An isolated unit of Fig. 2 allows for parallel transport of charge through the capacitor describing electrostatic charge displacement (C_i) and through the serial arrangement of two nonlinear capacitors ($C_i'^{\mathrm{DOS,ion}}$ and $C_i^{\mathrm{DOS,ion}}$) and a nonlinear resistor (R_i). This arrangement is summarized in Fig. 3, where R_i is denoted as R_{FE} and $C_i'^{\mathrm{DOS,ion}}$ and $C_i^{\mathrm{DOS,ion}}$ are represented by C_{FE}. The voltage across R_{FE} is given by V_1, the voltage across C_{FE} by V_2. Capacitor C_i is denoted as C_{diel}. This set is summarized by the symbol on the right, a ferroelectric capacitor with voltage drop $V_{\mathrm{FE}}=V_1+V_2$.

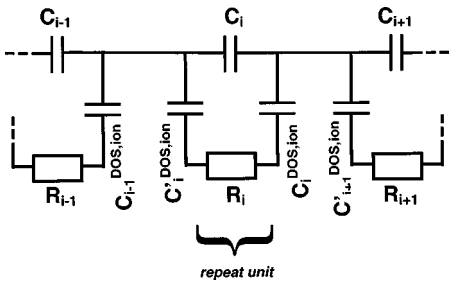

FIG. 2. Equivalent circuit for the ferroelectric-type movement of a single species of (ionic) charge. R_i describes dissipative charge movement. The capacitors $C_i^{\mathrm{DOS,ion}}$ and $C_i'^{\mathrm{DOS,ion}}$ define how this movement affects the local electrostatic potential. Dissipationless charge displacement is modeled by capacitor C_i.

Next we will choose functionalities for the three components of the ferroelectric model unit. This choice will involve smooth (analog) charge-displacement and energy-dissipation characteristics, although in principle the polarization states of a single atomic unit cell are discrete. In our model the smooth curves represent the average displacement; this average is the same for time averaging or ensemble averaging. Capacitor C_{diel} is a linear dielectric capacitor. We base our choice for the functionality of R_{FE} on the picture of bistable ions flipping at a threshold field. Thus, the switching current through R_{FE} should rapidly increase for $|V_1|$ above a threshold value V_α $(V_\alpha>0)$. As an example, we take

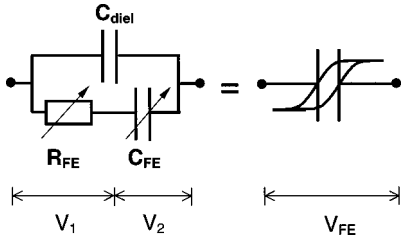

FIG. 3. Equivalent-circuit model for the charge displacement and energy dissipation in ferroelectric material, based on the model unit of Fig. 2. The two DOS capacitors are combined in C_{FE} while the dissipative-charge displacement resistor is denoted as R_{FE}. Both components are nonlinear. Electrostatic charge displacement is modeled by a linear dielectric capacitor, denoted as C_{diel} (cf. Fig. 2). The circuit is summarized by the hysteretic capacitor shown on the right.

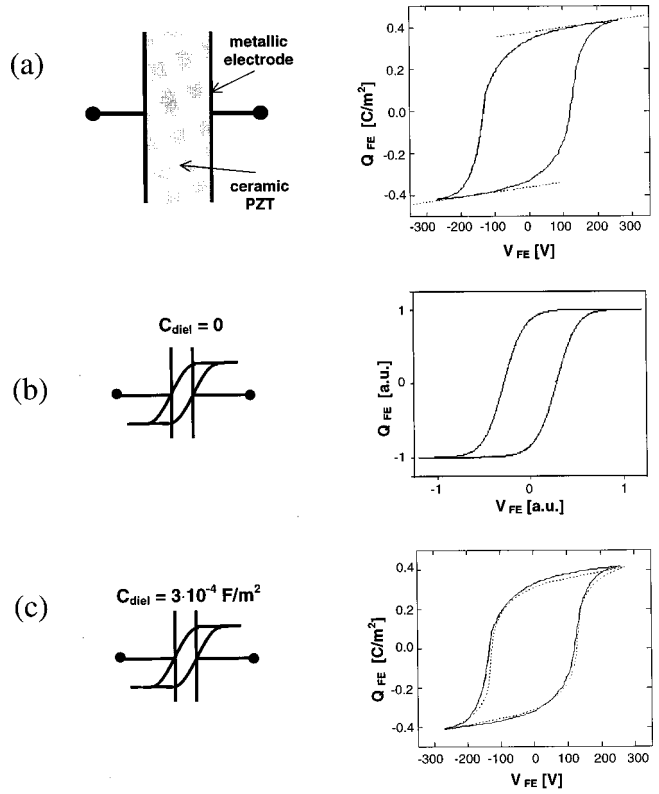

FIG. 4. (a) Schematic cross section of the ferroelectric capacitors studied and an experimental charge-displacement characteristic. The dielectric contribution to the charge displacement is accentuated by two dotted lines. The experimental graph was obtained on a capacitor of 180 μm ceramic $PbZr_{0.5}Ti_{0.5}O_3$ measured in a Sawyer–Tower (see Ref. 16) circuit at a sweeping frequency of 100 Hz. (b) Equivalent-circuit model of a ferroelectric capacitor and typical results of a simulation using this model without electrostatic charge displacement ($C_{\text{diel}}=0$) and $n=1$; $\alpha=0.02$. (c) Model circuit including electrostatic charge displacement. The model is used to fit the charge displacement characteristics of panel (a). Experiment: solid line; simulation: dotted line. Model-parameters $\alpha=0.02$; $n=0.5$; $V_\alpha=130$ V; $Q_R=0.28$; $Q_{\text{SAT}}=0.35$; $C_{\text{diel}}=3\times10^{-4}$ F/m^2; $I_0=4\times10^3$ A/m^2; sweep frequency 100 Hz.

$$R_{\text{FE}}: \quad I_{\text{FE}}=I_0\cdot\frac{\sinh\left(\dfrac{V_1}{\alpha V_\alpha}\right)}{\sinh\left(\dfrac{1}{\alpha}\right)}. \tag{1a}$$

I_0 is a normalization parameter. Parameter α ($\alpha>0$) controls the abruptness of ferroelectric switching at $V_1=\pm V_\alpha$. In case α is very close to zero, charge transport through R_{FE} can only occur if V_1 equals $\pm V_\alpha$, so that the charge displaced in the ferroelectric cell is given by $Q_{\text{FE}}(V_{\text{FE}})=Q_{\text{FE}}(V_2\pm V_\alpha)$. Consequently, the simulated hysteresis loop consists of two $Q_{\text{FE}}(V_2)$ loops shifted along the voltage axis by $\pm V_\alpha$. For larger values of α the transport of charge through R_{FE} also occurs for voltages that deviate from $\pm V_\alpha$; this phenomenon corresponds to ferroelectric depolarization. For the functionality of C_{FE} we choose

$$C_{\text{FE}}: \quad Q_{\text{FE}}=\text{sign}(V_2)\times Q_{\text{SAT}}\times\tanh\left(\frac{|V_2|^n}{2\delta}\right), \tag{1b}$$

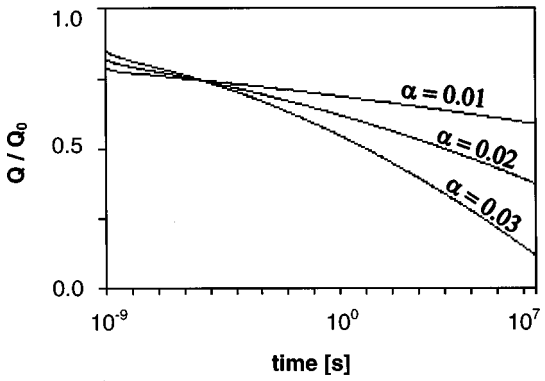

FIG. 5. Simulated time evolution of the ferroelectric charge displacement ($Q=Q_0$ at zero time; $Q_R<Q_0<Q_{\text{SAT}}$). Recorded with $V_{\text{FE}}=0$. The model circuit is that of Fig. 3. Note the very rapid partial depolarization between $t=0$ and 1 ns. In this period, the system relaxes towards the remnant situation, $Q=Q_R$. For smaller values of α, this initial depolarization becomes more pronounced.

$$\delta=\frac{V_\alpha^n}{\ln\left(\dfrac{1+Q_R/Q_{\text{SAT}}}{1-Q_R/Q_{\text{SAT}}}\right)}. \tag{1c}$$

These expressions stem from Miller's model equations of ferroelectric capacitors[6] and their specific form is chosen for mathematical convenience and applicability to the experimental data of Sec. IV. Q_{SAT} represents the saturation value of the ferroelectric charge displacement and Q_R the value at $V_2=V_\alpha$. An idealized, square hysteresis loop has $n\approx0$ and $\alpha\approx0$ with V_α equal to the coercive voltage and Q_R to the remnant polarization. For larger values of α, the hysteresis loop deviates from the shape of $Q_{\text{FE}}(V_2)$ and the apparent coercive voltage and remnant polarization are no longer equal to V_α and Q_R, respectively. Such deviations also occur when increasing the time needed for measuring one hysteresis loop (so, by decreasing the sweep frequency).

IV. SIMULATION RESULTS

A. Ferroelectric capacitor

In Fig. 4(a) experimental data are shown of a ferroelectric capacitor. Figure 4(b) presents a simulation for the serial arrangement of a nonlinear resistor (R_{FE}) and a nonlinear capacitor (C_{FE}), neglecting the dielectric contribution ($C_{\text{diel}}=0$). This is to show that the serial arrangement of these two components gives rise to hysteresis behavior with a nonzero coercive voltage, a nonzero remnant polarization, and to a saturating behavior at high applied voltages. The addition of the dielectric contribution [Fig. 4(c)] reproduces the experimentally observed characteristic. The sharpness of the switching-current onset at $V_1=\pm V_\alpha$, described by parameter α, is closely related to the retention of ferroelectric polarization in the absence of an external electric field ($V_{\text{FE}}=0$): low values of α relate to material that retains its polarization effectively, high values give depolarization in time. This is illustrated in the retention graph of Fig. 5, where the decrease of polarization is shown for our model ferroelectric unit at $V_{\text{FE}}=0$ over 16 time decades.

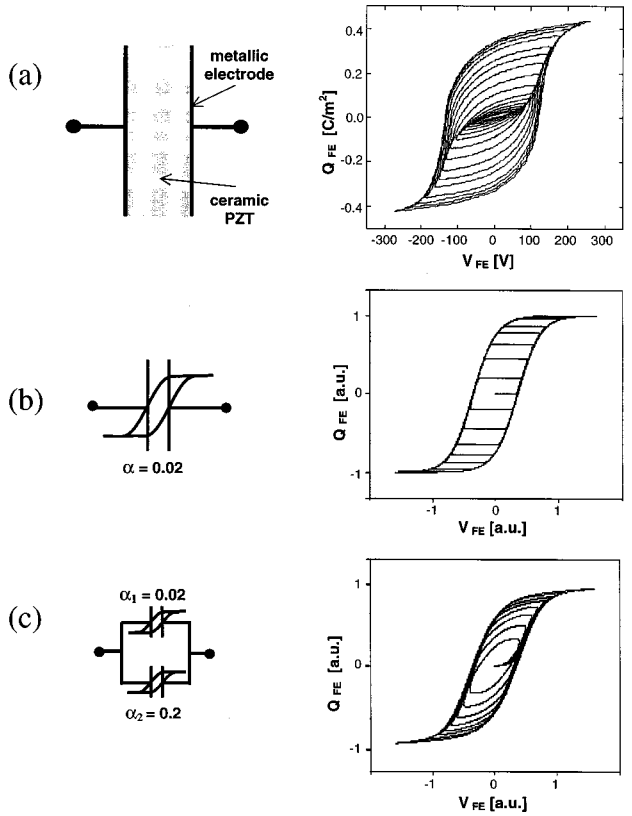

FIG. 6. (a) Left: Schematic cross section of the ferroelectric capacitors studied. Right: charge-displacement characteristics including subsaturated hysteresis loops. (b) Left: equivalent-circuit model of a ferroelectric capacitor. Right: simulation results of (sub)saturated hysteresis loops for $\alpha=0.02$, $n=1$, and $C_{\text{diel}}=0$. (c) Two ferroelectric modules with different α-values ($n=1$) and simulation results.

{The influence of α on the $Q(V_{\text{FE}})$ graphs is particularly notable for voltage sweeps with an amplitude that is insufficient to drive the ferroelectric polarization into saturation, so -called inner hysteresis loops or subsaturation loops. Figure 6(a) shows a set of experimental $Q-V$ curves including subsaturation loops. The loops have a dissimilar derivative $dQ_{\text{FE}}/dV_{\text{FE}}$ for given V_{FE} (the experimental observation that this derivative is similar among different subsaturated loops is described for example in Ref. 6). In fact, for simulations with a low value for α and $C_{\text{diel}}=0$ [Fig. 6(b)], the derivative is either that of the outer loop or zero. This is due to the fact that no charge is being displaced when the voltage across R_{FE} is lower than V_{α}. When a $C_{\text{diel}}>0$ is added, the zero-derivative sections turn into sections with a (constant) derivative equal to C_{diel} (not shown). The correspondence with the experimental results, especially in those sections, is improved when two dissimilar model units are combined as can be appreciated from Fig. 6(c) in which two units with a different value of α are combined. Possibly, nonuniformities in the material and effects like domain-wall movement and pinning generate the need for dissimilar model units. The use of two α-modules also results in two decay characteristics in the retention graph, one giving rise to fast decay of the polarization ($\alpha=0.2$) and one relating to a more slowly decaying component ($\alpha=0.02$). We note that the data of Teowee and co-workers[17] for Ti/Pb(Zr,Ti)O_3/Pt and

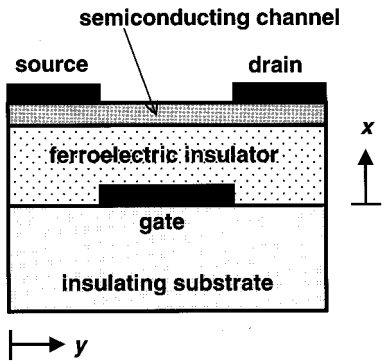

FIG. 7. Schematic cross section of a field-effect transistor with a ferroelectric insulator.

Ti/Pb(Zr,Ti)O_3/Zn capacitors are similar to the retention simulations of Fig. 6(c). The origin of the complex decay behavior may be the presence of nonuniform fields inside the capacitor (e.g. due a space-charge region near the interface or due to nonswitching layers) or structural inhomogeneities. The influence of depolarization in time is also seen when the measurement of a hysteresis loop is performed more slowly, resulting in a decrease of the apparent coercive voltage and a decrease of the apparent remnant polarization for decreasing sweep frequencies. This well-known property of ferroelectrics is reproduced by our simulations as well (not shown).

B. Ferroelectric transistor

We will next describe how a thin-film ferroelectric field-effect transistor, shown in Fig. 7 and described in detail in Ref. 3, can be simulated with a compact equivalent-circuit model such as shown in Fig. 1. We treat the case of small source-drain voltages, so that we only need to derive the equations for charge displacement in the ferroelectric material and the semiconductor layer along the normal of the semiconductor/ferroelectric interface (i.e., along the x axis). For the ferroelectric gate insulator we use the model of Fig. 4(c). A description of the band bending and charge accumulation/depletion in the semiconductor layer of thickness t must satisfy the Poisson equation[18]

$$\frac{\partial^2\Phi}{\partial x^2}=\frac{\rho(x)}{\epsilon}. \tag{2}$$

$e\Phi(x)=E_c(x)-E_F$ denotes the position of the conduction band edge (E_c) with respect to the Fermi level (E_F), $\rho(x)$ the associated charge density, and ϵ the dielectric constant of the semiconductor. We base our equivalent-circuit description of the n-type semiconducting material on the general model of Fig. 1(c). One moving charge species is involved, *viz*. electrons. No current is flowing in the x direction, so that the resistors in the electrochemical channel can be replaced by shorts. The nodal points i^s are at zero electrochemical potential, corresponding to the Fermi level of the semiconductor material. This yields the model displayed in Fig. 8(a). Parameter t is the thickness of the thin-film semiconducting layer. As is shown explicitly in the Appendix, the array

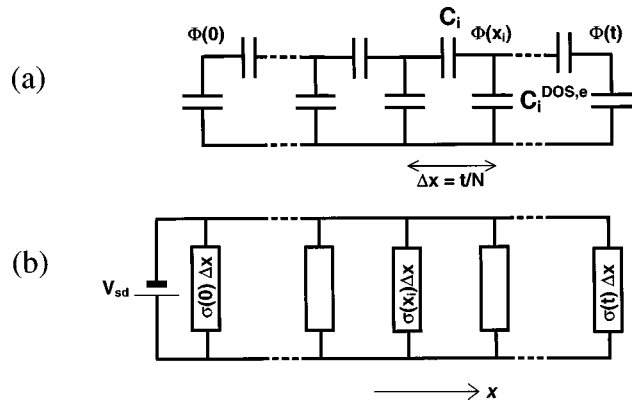

FIG. 8. Equivalent-circuit model of (a) the charge displacement in the x direction, and (b) the source-drain current as a function of x in the semiconducting layer of thickness t. Voltage $V_{SD}=V_S-V_D$ is applied on the channel electrodes, while $e\Phi(x_i)$ is the conduction-band bending in the semiconductor (in units of eV) at $x=x_i$. The band bending is calculated for N points from $x_0=0$ to $x_N=t$. The local source-drain conductivity is denoted as $\sigma(x_i)$.

solves Poisson's equation for N equidistant points x_i when we define for Q_i (on C_i) and $Q_i^{\mathrm{DOS},e}$ (on $C_i^{\mathrm{DOS},e}$)

$$Q_i=\frac{\epsilon}{\Delta x}\cdot[\Phi(x_i)-\Phi(x_{i-1})], \tag{3a}$$

$$Q_i^{\mathrm{DOS},e}=-e\Delta x\int_{-\infty}^{\infty}f(E)D(E-e\Phi(x_i))dE+q_0, \tag{3b}$$

with $f(E)$ the Fermi-Dirac distribution function and $D(E)$ the density of electron states (in $\mathrm{m^{-3}J^{-1}}$) in the semiconductor. Parameter q_0 ensures charge neutrality for zero gate–voltage. Since we are using a degenerately doped semiconductor material[19] we choose q_0 such that the Fermi level lines up with the conduction band edge at $\Phi=0$. We assumed that the influence of the source-drain voltage on the band bending is negligible, so that we can approximate the source-drain conductivity (σ) by counting the electrons in states above the conduction band edge (n_{cond}) and calculating $\sigma(x)=n_{\mathrm{cond}}(x)\times e\times\mu$ [see Fig. 8(b)]

$$\sigma(x)=e\mu\int_{e\Phi(x)}^{\infty}f(E)D(E-e\Phi(x))dE, \tag{4}$$

for n-type conduction with electron mobility μ. We assume that the conduction band shape is parabolic, i.e., $D(E)\sim(E-E_c)^{-1/2}$.[20] To model the grain boundaries in the polycrystalline semiconductor material a constant density of grain-boundary states ($D_{\mathrm{gr}}(E)=D_{\mathrm{gr}}$ for all energies) is added to the DOS. Grain-boundary states with an energy inside the semiconductor energy gap are assumed to have zero mobility; states above the gap are assumed to be part of the conduction band. The sheet conductance (G) of the transistor finally follows from

$$G=\int_0^t\sigma(x)dx\approx\sum_0^N\sigma(x_i)\Delta x. \tag{5}$$

This summation is performed by an array of resistors, see Fig. 8(b), each having a conductance equal to $\sigma(x_i)\Delta x$.

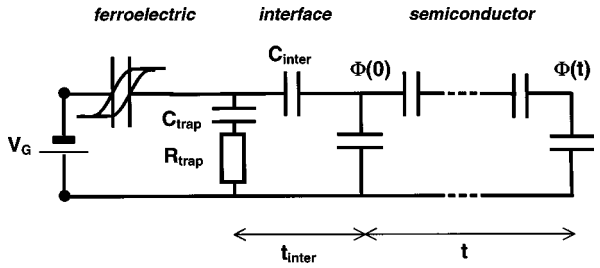

FIG. 9. As Fig. 8(a), with added elements to account for trapping sites, which are assumed to be especially significant near the ferroelectric/semiconductor interface ($x=0$). The dielectric capacitance of the interface region C_{inter} equals $\epsilon_{\mathrm{inter}}/t_{\mathrm{inter}}$.

So far, the model does not take into account charge injection into the insulating layer, which may occur in the presence of high electric fields. In our device the charge displacement is of the order of 0.1 $\mathrm{C/m^2}$, which gives rise to electric fields of the order of 10^9 V/m at the semiconductor/ferroelectric interface. These very high fields are expected to yield charge injection into localized states near the interface (see Ref. 21 for a discussion on charge injection into ferroelectric material). This effect modifies the transistor characteristics. The injected charge is localized and does not contribute to conduction along the semiconducting channel. Furthermore, the process of charge trapping and detrapping causes hysteresis in the conductance of the source-drain channel as a function of the displaced charge in the gate insulator. We model the interfacial trapping region by an interfacial insulating layer of thickness t_{inter} (see Fig. 9). The local density of trap states across the interfacial layer is described by capacitance C_{trap} (unit $\mathrm{F/m^2}$). Since the interfacial layer is an insulator the capacitors describing the density of nontrapped states may be neglected in this region. R_{trap} controls the threshold behavior and rate of trapping/detrapping of charge carriers, in a similar fashion as R_{FE} does in our ferroelectric model unit. We choose for the functionality of R_{trap} expression (1a) in which fit-parameter α is replaced by β, and switching-threshold V_α by trap/release-threshold V_β. To model the complete ferroelectric field-effect transistor, a single ferroelectric module[22] is connected to the interfacial region as shown in Fig. 9.

Let us now compare the experimental results [Fig. 10(a)] to our simulation results from the ferroelectric/semiconductor model [Fig. 10(b)]. The charge displacement curves (a1 and b1) have an apparent coercive voltage of 2 V. This voltage results from the coercivity of the ferroelectric layer and the coercivity of the charge trapping across the interfacial layer. The apparent remnant polarization ($\sim$0.08 $\mathrm{C/m^2}$) is a factor of two smaller than the value of Q_R. This reduction is caused by the band bending in the semiconductor layer, giving a partial depolarization of the ferroelectric material at zero externally applied voltage (see for example Ref. 3). The sense of rotation of the transfer characteristic (panels a2 and b2) indicates what mechanism determines the memory effect in the semiconductor layer. When the ferroelectric polarization dominates, the sign of the induced charge in the semiconductor upon voltage application is the same as the sign of the remnant charge when the voltage is

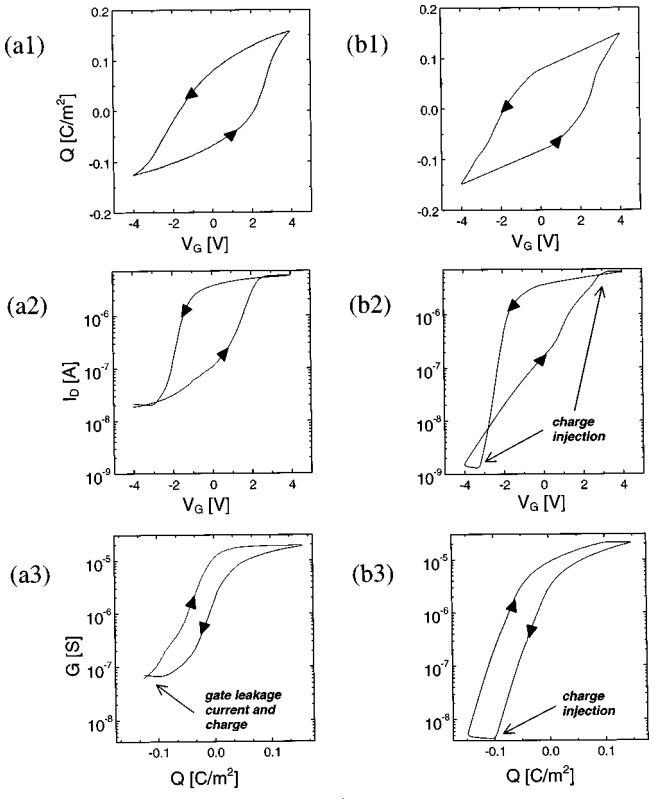

FIG. 10. Experimental graphs (a) and simulation results (b). Panel a1 and b1 show ferroelectric-type charge displacement per unit area (Q) inside a FEMFET channel as a function of gate–voltage (V_G). Panels a2 and b2 show the transistor transfer characteristics (drain-current I_D vs V_G). The source is at zero potential and $V_D=1$ V. The curves are combined in panels a3 and b3, showing the semiconductor sheet-conductance (G) vs Q for the measured data and simulation, respectively. The simulation curves were obtained with the following model parameters: $V_\alpha=2.2$ V, $I_\alpha=10^4$ A/m^2, $\alpha=0.02$, $Q_{\text{sat}}=0.22$ C/m^2, $n=0.4$, $Q_R=0.17$ C/m^2, $C_{\text{diel}}=0.02$ F/m^2, $\epsilon_r=10$, $\mu=1.3\times10^{-4}$ m^2/V s, $D_{\text{gr}}=8.5\times10^7$ F/m^3, $t_{\text{eff}}=2.5$ nm, $t_{\text{inter}}<5$ nm, $\epsilon_{\text{inter}}=50\ \epsilon_0$, $V_\beta=1.3$ V, $I_\beta=1$ A/m^2; $\beta=0.01$, $C_{\text{trap}}=1$ F/m^2, and $N=31$. Note the hysteresis in G due to trapping. Gate leakage currents dominate the conductance at negative gate voltages ($V_G<-2$ V). The experimental graphs were obtained on a thin-film transistor with a 144 nm $PbZr_{0.8}Ti_{0.2}O_3$ ferroelectric layer and a 15 nm-polycrystalline SnO_2 layer, doped with 4×10^{19} cm^{-3} Sb forming the transistor channel, passivated by a capping layer of 10 nm $BaZrO_3$. Panel 1a was determined with a Sawyer–Tower circuit (See Ref. 16) swept at 100 Hz. More details on the transistor fabrication can be found elsewhere (see Refs. 2, 3, 23, and 24).

removed (counter-clockwise rotation). When charge injection is the dominant memory mechanism, the sign of the charge induced by voltage application is opposite to the sign of the remnant charge (clockwise rotation). The counter-clockwise sense of rotation of our transfer characteristic proves that the memory effect is dominated by ferroelectric charge displacement and that charge injection is of minor importance.[3] At gate–voltages below -2 V the experimental transfer characteristic shows a higher current than the simulated curve due to the presence of a gate leakage current, which has not been included in the model. At the outer ends (for voltages higher than 3 V, and in the simulation also for voltages lower than -3 V) we find that the transfer characteristics show small loops. These loops point to the injection of charge into the interfacial layer between the semiconductor and the ferroelectric material.

In panels a3 and b3, the $Q-V_G$ and I_D-V_G curves are combined to a curve of the conductance of the source-drain channel (G) versus the charge density displaced in the gate insulator. The slope of the $G-Q$ curve in the high-conductivity (or accumulation) regime determines the electron mobility in the semiconducting channel; the deduced value (1.3×10^{-4} m^2/Vs) is in agreement with measurements of the Hall mobility in the same material.[19] The slope of the $G-Q$ curve at low conductivity (depletion or subthreshold regime) is given by the density of grain states D_{gr} and the effective semiconductor layer thickness t_{eff}. These parameters cannot be deduced independently from the measured curve. However, the semiconductor band bending required for the displacement of a given amount of charge increases for increasing t_{eff}; because the band bending in the semiconductor should be smaller than the applied gate voltage minus the voltage required for ferroelectric switching, we can deduce an upper limit for t_{eff} (so also a lower limit for D_{gr}). The deduced value is about 2.5 nm, which is of the same order as the Fermi wavelength of the charge carriers[19] and smaller than the nominal thickness of 10 nm. We attribute this difference to the granular nature of the semiconducting material[19] and to depletion effects near the semiconductor/capping interface. The fact that several nanometers of the film thickness do not contribute to the conduction is in agreement with our experience that laser-ablated thin films of SnO_2 with a nominal thickness below 10 nm show a strongly reduced conductivity compared to films of only slightly larger thickness. The fitted value of the density of grain-boundary states is 8.5×10^7 F/m^3, corresponding to a state density of 1.8×10^{20} cm^{-3}.[25] This value is in the expected range for polycrystalline material.[26,19] Finally, we observe hysteresis in panels a3 and b3 with a clockwise sense of rotation. This is caused by charge trapping in the interfacial layer between the semiconductor and the ferroelectric material. From comparison of experimental and simulation results, no precise value for C_{trap} could be concluded. The similarity between the $G-V_G$-curves for both sweep directions suggests that charge injection into the trapping layer occurs only at high gate voltages. Due to leakage currents in the same regime, it is difficult to estimate values for V_β, I_β, and C_{trap}. Thus, we have chosen them as to yield a sharp transition from zero trapping to complete trapping of all additional charges when $|V_G|\sim3$ V, indicated for example in panel b3 of Fig. 10.

V. SUMMARY AND DISCUSSION

This article describes a model for the electrical switching characteristics of ferroelectric material in devices such as capacitors and field-effect transistors. The model is based on a compact modeling concept of charge displacement as a function of position in a material, distinguishing dissipative and dissipationless currents. Dissipative transport is described by a channel of resistors; the current that flows

through the resistors depends on the drop of electrochemical potential inside the material. The dissipationless transport occurs in a channel of capacitors across which a drop of the electrostatic potential is present. The two channels are coupled by capacitors that relate to the local DOS inside the material. The model is used to derive a resistor/capacitor unit that reproduces the ferroelectric switching behavior of an atomic unit cell (Fig. 3). A serial arrangement of a capacitor of saturating nature and a resistor with an exponential current–voltage behavior yields ferroelectric-type charge-displacement characteristics. Important in this model unit is the degree of nonlinearity of the resistor (described by parameter α) which determines the sharpness of the onset of switching and the time-dependent depolarization of the material. A combination of fast and more slowly decaying polarization components (experimentally observed in Ref. 17 for example) can be simulated by utilizing multiple model units with differing values for α. Good agreement is obtained between experimental characteristics (i.e., charge displacement and transfer characteristics) of ferroelectric thin-film transistors and simulations based on our ferroelectric model combined with a model for the semiconductor and for the ferroelectric/semiconductor interface. The latter two models are derived from the same modeling concept that generated the ferroelectric unit. Charge displacement in the semiconductor channel is calculated along one dimension, sufficient to describe the linear regime of transistor operation ($V_{SD} \ll V_G$). The model can be straightforwardly extended to describe displacements in two or three dimensions by extending the network of Fig. 1. From the comparison between experiment and our model we conclude that at the most 25% of the nominal 10 nm thickness of the SnO_2:Sb layer (the transistor channel) is conductive. This we attribute to the granularity of and depletion effects in the semiconductor thin film.

In this work we have developed models describing ferroelectric-type, semiconductor-type, and injection-type charge displacement from a single concept model. This model takes into account fundamental material parameters such as the intrinsic DOS, the dielectric behavior, and dissipative charge transport. Therefore, it appears to be a versatile vehicle for modeling a variety of materials. Inhomogeneities in the material call for dissimilar model units to be connected to each other. As an example, several model units placed in a matrix will allow the study of multicell ordering phenomena such as ferroelectric domain wall movement. The existence of inhomogeneities does in principle endanger the compactness of the model. This situation occurs in highly disordered systems where charge transport is determined for example by percolation (the principle of which is a random matrix of dissimilar resistors[27]) or by variable-range hopping.[28] When sufficiently compact units can be defined, as in the case of our ferroelectric devices, compact modeling can be of great importance to simulate the behavior of the devices when embedded in larger electronic circuits, like for example in sensor systems or in memory chips.

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APPENDIX: THE CHARGE-DISPLACEMENT MODEL SOLVING POISSON'S EQUATION

Referring to Fig. 8, charge conservation yields

$$[\Phi(x_i)-\Phi(x_{i+1})]\times C_{i+1}+[\Phi(x_i)-\Phi(x_{i-1})] \times C_i+\Phi(x_i)C_i^{\mathrm{DOS}}=0. \tag{A}$$

From (3b) we have

$$\Phi(x_i)C_i^{\mathrm{DOS}}=\rho(x_i)\Delta x \tag{B}$$

so that

$$\frac{-\Phi(x_{i-1})+2\Phi(x_i)-\Phi(x_{i+1})}{\Delta x^2}=-\frac{\rho(x_i)}{C_i\Delta x}. \tag{C}$$

Here, the left-hand side corresponds to minus the second derivative of $\Phi(x)$ at $x=x_i$. C_i is defined by Eq. (3a) as $\epsilon/\Delta x$ so that Eq. (C) yields a discretization of the Poisson equation, Eq. (2).

[1] MRS Bull. **21**, 7 (1996).
[2] M. W. J. Prins, K.-O. Grosse-Holz, G. Müller, J. F. M. Cillessen, J. B. Giesbers, R. P. Weening, and R. M. Wolf, Appl. Phys. Lett. **68**, 3650 (1996).
[3] M. W. J. Prins, S. E. Zinnemers, J. F. M. Cillessen, and J. B. Giesbers, Appl. Phys. Lett. **70**, 458 (1997).
[4] Y. T. Kim and D. S. Shin, Appl. Phys. Lett. **71**, 3507 (1997).
[5] For a survey of several models of ferroelectric capacitors: A. Sheikholeslami and P. G. Gulak, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **44**, 917 (1997).
[6] S. L. Miller, R. D. Nasby, J. R. Schwank, M. S. Rodgers, and P. V. Dressendorfer, J. Appl. Phys. **68**, 6463 (1990); S. L. Miller, R. D. Nasby, J. R. Schwank, and M. S. Rodgers, *ibid.* **70**, 2849 (1991); S. L. Miller and P. J. McWorther, *ibid.* **72**, 5999 (1992).
[7] D.-Y. Chen, M. Azuma, L. D. McMillan, and C. A. Paz de Araujo, Proceedings of the ninth IEEE ISAF, Pennsylvania, 1994, edited by R. Pandey, M. Liu, and A. Safari, pp. 25–28; D.-Y. Chen, J. Gregory, T. S. Kalkur, C. A. Paz de Araujo, L. D. McMillan, and T. A. Robson, Integr. Ferroelectr. **5**, 265 (1994).
[8] A. K. Kulkarni, G. A. Rohrer, S. Narayan, and L. D. McMillan, Ferroelectrics **116**, 95 (1991).
[9] A. Sheikholeslami and P. G. Gulak, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **43**, 450 (1996).
[10] D. E. Dunn, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **41**, 360 (1994).
[11] J.-H. Cho, H.-T. Chung, and H.-G. Kim, Ferroelectrics **198**, 1 (1997).
[12] SPICE=Simulation program with integrated-circuit emphasis; for a recent overview of the history and features of SPICE-based simulation software, see e.g., A. Vladimirescu, *The Spice Book* (Wiley, New York, 1994).
[13] A familiar example of a DOS capacitor is the local charge density in a semiconductor conduction band; the formula $n=n_i\exp\{q(\psi-\phi_n)/k_BT\}$ describes how the local charge density depends on the difference between the local electrostatic potential (ψ) and the local electrochemical potential (ϕ_n, the quasi-Fermi level for electrons), for the case that the Fermi level is situated several times k_BT below the conduction band edge.[14]
[14] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[15] L. L. Hench and J. K. West, *Principles of Electronic Ceramics* (Wiley, New York, 1990).
[16] C. B. Sawyer and C. H. Tower, Phys. Rev. **35**, 269 (1930).

[17] G. Teowee, C. D. Baertlein, E. A. Kneer, J. M. Boulton, and D. R. Uhlmann, Integr. Ferroelectr. **7**, 149 (1995).
[18] Note the sign of the left-hand side of the equation, which differs from what is commonly used, because of our definition of $\Phi(x)$.
[19] M. W. J. Prins, K.-O. Grosse-Holz, J. F. M. Cillessen, and L. F. Feiner, J. Appl. Phys. **83**, 888 (1998).
[20] The integrals involving $D(E) \sim (E-E_c)^{-1/2}$ cannot be solved analytically. We have used both an approximation to the integrals valid for $\Phi > k_B T$ and a discrete set of points from a numerical solution in between which the circuit-analysis software interpolates. The results were sufficiently close to each other.
[21] J. F. M. Cillessen, M. W. J. Prins, and R. M. Wolf, J. Appl. Phys. **81**, 2777 (1997).
[22] Because subsaturation characteristics of the ferroelectric transistor are not included in the experimental data, the model contains for simplicity only one ferroelectric unit.
[23] J. B. Giesbers, M. W. J. Prins, J. F. M. Cillessen, and H. van Esch, Microelectron. Eng. **35**, 71 (1997).
[24] J. F. M. Cillessen, Ph.D. thesis, Twente University, The Netherlands, 1996.
[25] D_{gr} is expressed in F/m^3 so that D_{gr}/e (e being the electron charge) in m^{-3} eV^{-1}. By assuming an energy gap width of 3 eV this is converted into m^{-3}.
[26] J. C. Crawford and F. L. English, IEEE Trans. Electron Devices **ED-16**, 525 (1969).
[27] S. Kirkpatrick, Rev. Mod. Phys. **45**, 574 (1973).
[28] R. Zallen, *The Physics of Amorphous Solids* (Wiley, New York, 1983).