Ultra high data rate CMOS FEs

ULTRA HIGH DATA RATE CMOS FRONT ENDS

Reza Mahmoudi, , Arthur van Roermund
Department of Electrical Engineering, Eindhoven University of Technology, Eindhoven, the Netherlands

Abstract

The availability of numerous mm-wave frequency bands for wireless communication has motivated the exploration of multi-band and multi-mode integrated components and systems in the main stream CMOS technology. This opportunity has faced the RF designer with the transition between schematic and layout. Modeling the performance of circuits after layout and taking into account the parasitic effects resulting from the layout are two issues that are more important and influential at high frequency design. Performing measurements using on-wafer probing at 60GHz has its own complexities. The very short wave-length of the signals at mm-wave frequencies makes the measurements very sensitive to the effective length and bending of the interfaces. This paper presents different 60GHz corner blocks, e.g. Low Noise Amplifier, Zero IF mixer, Phase-Locked Loop, A Dual-Mode Mm-Wave Injection-Locked Frequency Divider and an active transformed power amplifiers implemented in CMOS technologies. These results emphasize the feasibility of the realization 60GHZ integrated components and systems in the main stream CMOS technology.

1. INTRODUCTION

Driven by customer demands, the last two decades have experienced unprecedented progress in wireless portable devices capable of supporting multi-standard applications. The allure of “being connected” at anytime anywhere and desire for untethered access to information and entertainment “on the go” has set

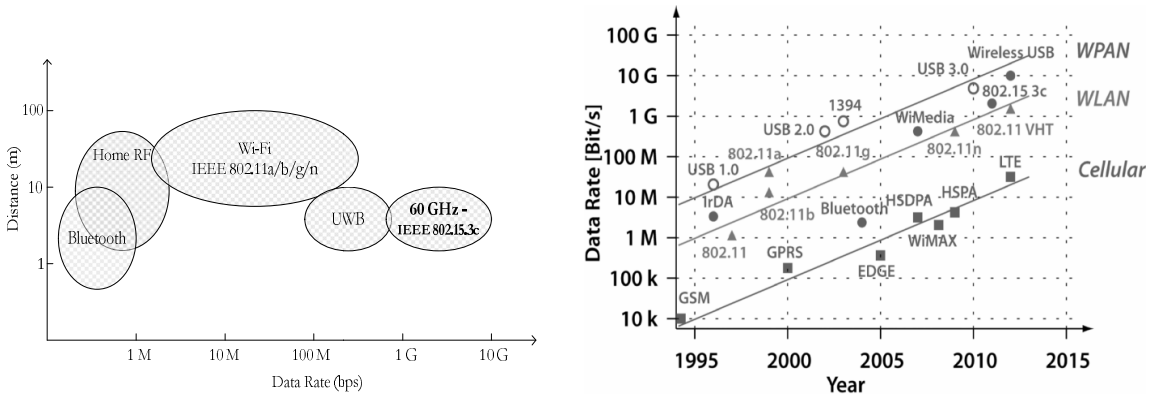


*Figure 1: left: Data Rate and distance comparison for different WPAN and WLAN technologies. Right Increasing data rate trend according to Edholm’s law [*Ref 2*]*

the ever increasing demand for higher data rates. As shown in Figure 1, contemporary systems are capable of supporting light or moderate levels of wireless data traffic, as in Bluetooth and wireless local area networks (WLANs). However, they are unable to deliver data rates comparable to wired standards like gigabit Ethernet and high-definition multimedia interface (HDMI)[Ref *1*]. Furthermore, as predicted by Edholm's law [Ref *2*], the required data rates (and associated bandwidths) have doubled every eighteen months over the last decade. This trend is shown in Figure 1 for cellular, wireless local area networks and wireless personal area networks for last fifteen years.

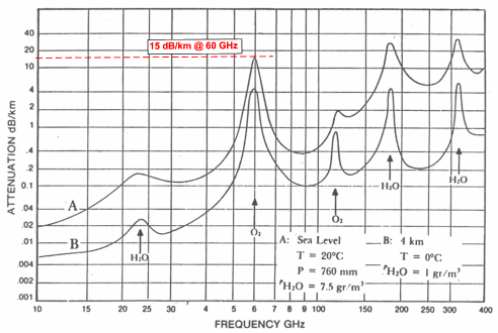


Figure 2: Gaseous absorption at 60 GHz.

In 2001, spurred by the increasing demand of high data rate applications and limitations of current wireless technologies, a 7 GHz contiguous bandwidth was allocated world-wide by the FCC. The regional regulatory bodies allocated local frequency bands with slight shift and defined the maximum effective isotropic radiated power (EIRP). The maximum allowed EIRP at 60 GHz is much higher than other existing WLANs and WPANs. This is essential to overcome the higher space path loss (according to classic Friis formula) and oxygen absorption of 10-15 dB/km as shown in Figure 2. These two loss mechanisms dictate the use of 60 GHz for short range multi-gigabit per second transmission. The attenuation also means that the system provides inherent security, as radiation from one particular 60 GHz radio link is quickly reduced to a level that does not interfere with other 60 GHz links operating in the same vicinity.

Using the 60 GHz band for high data rate and indoor wireless transmission, a multitude of potential applications can be envisioned. The high definition multimedia interface (HDMI) cable could be replaced by a wireless system, transmitting uncompressed video streams from DVD players, set-top boxes, PC's to a TV or monitor. Current wireless HDMI products utilize the 2.5 and 5 GHz unlicensed spectrum where bandwidth is limited. As a result, these systems implement either lossy or lossless compression, significantly adding component and design cost, digital processing complexity and product size. Typical distance between these gadgets is 5 to 10 meters and this communication can be point-to-point or point-to-multi-point. The span of the potential services and applications in conjunction with the maturity of the main stream CMOS technology have stimulated the large activity for the realization the required corner blocks and systems in the cheap main stream CMOS process technology at 60GHz.

Designing at 60GHz requires dealing with multiple challenges which might be irrelevant or negligible at low frequency designs. One of the most important

challenges of 60GHz circuit design occurs in the transition between schematic and layout. Modeling the performance of circuits after doing the layout and taking into account the parasitic effects resulting from the layout are two issues that are more important and influential at high frequency design. The pronounced impact of parasitics at such high frequencies makes it more difficult to obtain the desired level of performance from the circuits. In addition, the necessity of accurate modeling of the parasitic effects brings about another design complexity. In fact, these complexities lead to the necessity of an iterative shift of the design focus from the schematic to the layout and vice versa, rendering the design a more time consuming process.

The electromagnetic modeling of complex structures including the skin effect, substrate loss and the coupling impact of adjacent components is another issue which is sometimes impractical with the currently available simulation software, as they may require immense computational power. Therefore, the question facing the designers is whether the currently available software and tools are computationally capable of including all the layout impacts in their prediction of the performance of the circuits and how such predictions can be accurate regarding all the aforementioned limitations and the accentuated impact of layout-level issues.

Performing measurements using on-wafer probing at 60GHz has its own complexities. The very short wave-length of the signals at mm-wave frequencies makes the measurements very sensitive to the effective length and bending of the interfaces. Especially to perform on-wafer measurements one must pay utmost attention to the rigidity of the interfaces connected to the probes to keep all the connection lengths and orientations constant during the whole period of the measurement and calibration. Also special care must be taken to preserve the position of the probes on the bondpads and impedance standard substrates, since the measurement accuracy can be very much dependent on the positioning and landing of the probes. Another difficulty of mm-wave measurements arises from the overwhelming cost of equipment needed for instrumentation.

2. A NOISE AND S-PARAMETER MEASUREMENT SETUP

The very short wave-length of the signals at these frequencies makes the measurements very sensitive to the effective length and bending of the interfaces. Especially to perform on-wafer measurements one must pay utmost attention to the rigidity of the interfaces connected to the probes to keep all the connection lengths and orientations constant during the whole period of the measurement and calibration. Also special care must be taken to preserve the position of the probes on the bondpads and impedance standard substrates, since the measurement accuracy can be very much dependent on the positioning and landing of the probes.

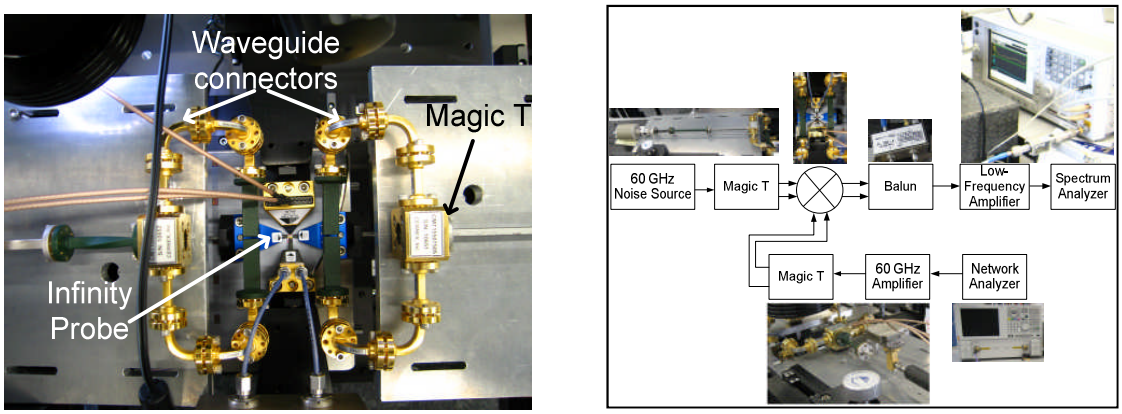


Figure 3: Left: The waveguide-based setup including two magic-Ts for measuring a double-balanced mixer. Right: Noise measurement setup for the mixer.

In this section, measurement setups are introduced which use waveguide interfaces to provide the required rigidity in the vicinity of the probes and utilize magic-T single-ended-to-differential converters to facilitate the measurement of differential circuits. The noise measurement of a 60GHz double-balanced zero-IF mixer (see section 4)and the noise and s-parameter measurement of a differential 60GHz LNA (see section 3), using the introduced setup, are explained in the following sections.

2.1. Noise Measurement Of A Double-Balanced Mixer

The waveguide setup used for on-wafer measurement of the differential circuits is illustrated in Figure 3. In the case of the zero-IF mixer, four probes are needed. The probe on the top of the picture is an eye-pass probe used for biasing. The probe at the bottom of the picture is a GSGSG microprobe suitable for up to 50GHz measurements and used here at the IF output of the DUT mixer. The other two probes on the left and right side are infinity GSGSG probes suitable for mm-wave signals and used here at the RF and LO differential inputs of the mixer. The waveguide structures are mounted on metal plates which are screwed to the probe station, preventing all kinds of unintentional movements in the setup.

Figure 3. shows the block diagram of the setup used for the noise measurement using Y-factor method [Ref *4*]. The network analyzer is used as a signal generator to produce the LO signal. The 60GHz noise source is connected via an isolator and a waveguide to the magic-T and then to the RF port of the mixer. The differential IF output of the mixer is converted to single-ended via a hybrid and then connected to the spectrum analyzer via a low-

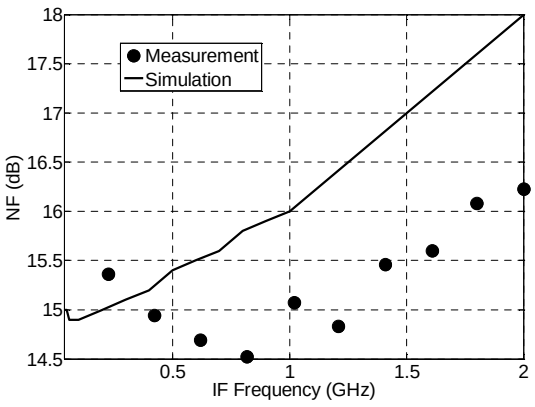


Figure 4: Measured and simulated noise figure of the mixer.

frequency amplifier which covers 30MHz-4GHz. The spectrum analyzer is set to Noise Figure mode and DUT is specified as a downconverter with a 60GHz LO.

The RF frequency range is set to 30MHz-2GHz. The 60GHz noise source generates noise only in the range of 60GHz to 75GHz. Therefore, another noise source, capable of generating noise in the IF range, is needed for calibration of the output path and the spectrum analyzer. Fig. 3 shows the block diagram of the noise calibration setup. The low-frequency amplifier is essential for obtaining good calibration results by amplifying the noise. Since two different noise sources are used, the ENR (excess noise ratio) list of the two noise sources must be manually entered in the ENR table of the spectrum analyzer. Both noise sources are controlled by the spectrum analyzer. The effect of the low-frequency amplifier and the cable, connecting the IF balun to the low-frequency amplifier, is automatically taken into account during the measurement; because they are in the calibration setup. However, the impact of the IF balun and the RF interfaces between the 60GHz noise source and the input of the DUT must be manually calculated after the measurement.

The loss of the combination of the magic-T, waveguide structure, and the infinity probe can be measured via two methods. The first employes a delta measurement and utilizing the network analyzer as a signal generator, the amplitude of the 60GHz signal is measured by the spectrum analyzer. Since the spectrum analyzer does not support 60GHz measurement, a preselected millimeter mixer is used to downconvert the 60GHz signal to the range of the spectrum analyzer. Keeping the same amplitude for the signal generated by the network analyzer, the magic-T and the probes are introduced into the setup. A through of an impedance standard substrate is used between the probes.

The difference in the readings of the two steps gives the loss of the introduced interface. Assuming a negligible loss for the through and equal loss for the two probes and magic-Ts, the loss of the RF interface, used between the noise source and the mixer input, can be calculated by dividing this number by two. In the second method, two one-port calibrations are performed using the network analyzer. First a cable, used in the next step for connecting the network analyzer to the magic-T and probe, is calibrated and the calibration dataset is saved. Then an on-wafer one-port calibration is performed using an impedance standard substrate and including the magic-T and the probe in the setup. Again the calibration dataset is saved. Having the two datasets, the magic-T and probe combination is characterized. The results are the same as the first method (delta measurement). After calculating the impact of the IF balun, the magic-T and waveguides, and the infinity probe, the final noise measurement results are obtained as shown in Figure 4. The measurement results are close to the simulations.

2.2. Noise Measurement Of A Differential Lna

The noise measurement of the 60GHz LNA is impeded by the fact that the output of the LNA is at a higher frequency than supported by the spectrum analyzer. Even the preselected mixer of previous section cannot be used here because the Noise Figure mode of the spectrum analyzer does not support it and it cannot be used with an external LO either. Therefore a passive mm-wave mixer is used in the noise measurement setup, as shown in Figure 5, to downconvert the output of the LNA to the range of the spectrum analyzer. The passive mixer can be included in the calibration setup as shown in Figure 5, making the post-measurement calculations much easier. The measured noise is in close agreement with the simulated values as shown in Figure 6.

2.3. S-Parameter Measurement

Performing s-parameter measurements on differential circuits with a two-port network analyzer is also facilitated by utilizing the magic-Ts. As shown in Fig. 8, each port of the network analyzer is connected to a magic-T and then to the probes. SOLT (Short-Open-Load-Through) calibrations are performed on a standard impedance substrate, suitable for GSGSG probes. Then the impedance standard substrate is replaced by the DUT and the measurement is done. The measured transducer gain of the 60GHz LNA, using this setup, is compared with simulation results in Figure 6. Conforming to the following considerations can promote the accuracy of the measurements and calibrations:

- Accurate definition of the impedance standard substrate in the network analyzer or the software which controls the network analyzer
- Precise positioning of the probes on the bondpads or on the impedance standard substrate
- Repeating the calibration after some period due to invalidity of the calibration results after a certain period
- Using undamaged samples of impedance standard substrate

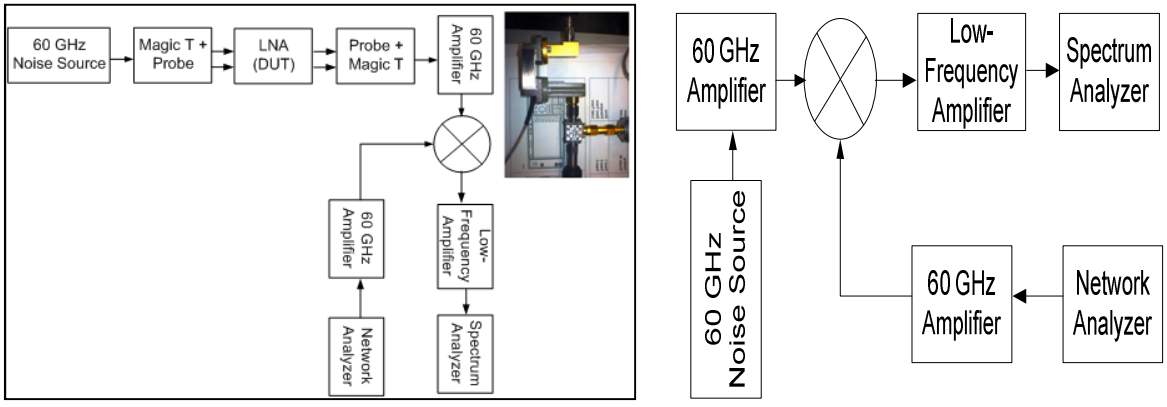


Figure 5: Left: LNA noise measurement setup. Right: Noise calibration for the LNA

Employing waveguide-based measurement setup enabled performing an accurate and repeatable measurements on 60GHz receiver components. The fixed waveguide structures, specially provided for the probe station, serve for the robustness of the setup as they circumvent the need for cables, which are by nature difficult to rigidify, in the vicinity of the probes. Taking advantage of magic-Ts, it is possible to measure differential mm-wave circuits with a two-port network analyzer rather than using a much more expensive four-port one. Furthermore, the differential circuit can be driven by a single-ended noise source necessary for the noise measurement. The noise and s-parameter measurements performed on a 60GHz mixer and LNA yield consistent results with the simulations.

3. FULLY BALANCED 60 GHZ LNA

The market demand for RF transceivers providing communication links of several Gb/s data rate motivates the use of the broadband WPAN ISM band at 60 GHz. These systems require receivers with a low noise figure (NF) and flat band response because of the complex modulation scheme. Combination of low NF, sufficient bandwidth, high gain and low voltage operation are important properties of LNAs. The design of mm-wave LNAs in CMOS causes many challenges because of lossy passives and the Miller capacitance. Several LNAs have been reported in recent years [Ref 9]. To defeat the loss in the passives, SOI technology [Ref 6]. This section describes a fully differential 60 GHz LNA (Figure 7) in bulk CMOS employing transformer feedback resulting in a flat and broadband response. Miller effect is defeated using gate-drain capacitance neutralization [Ref 10], which is achieved when the following equation is satisfied (n is the transformer turn ratio and k is its coupling).

$$\frac{n}{k} \approx -\frac{C_{gs}}{C_{gd}}, n = \sqrt{\frac{L_d}{L_s}} \qquad (1)$$

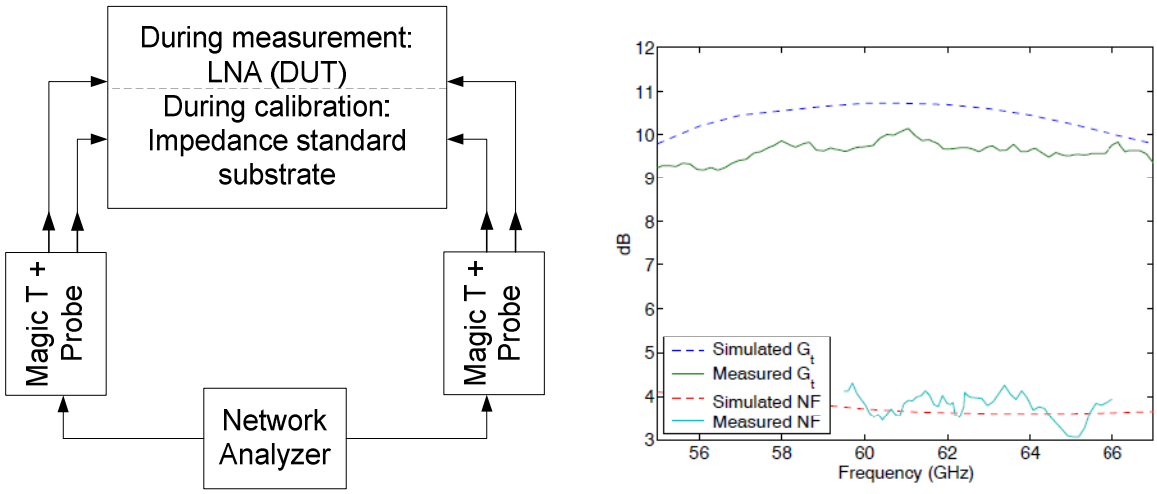


Figure 6: Left: S-parameter measurement and calibration setup of a differential two-port circuit. Right: Measured and simulated noise figure and transducer gain of the 60GHz LNA

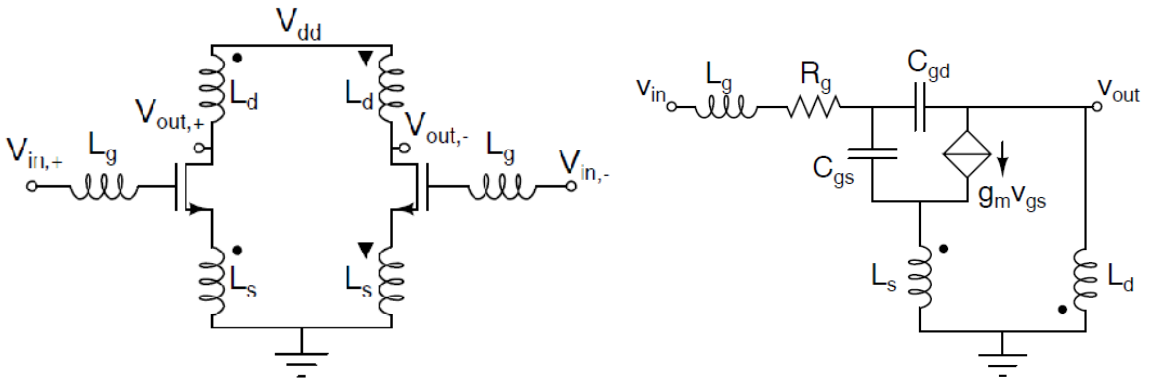


*Figure 7: Left: Circuit of the V-V transformer FB LNA as discussed in [*Ref 10*]. The coupling is indicated by the symbols next to the coils. Right: Small signal circuit of the V-V transformer feedback LNA. For reasons of clarity the single ended circuit is shown.*

3.1. Design Procedure

Main design goal for the LNA is low NF combined with a high gain. Both are a function of MOS transistor bias and width, passives choices, and source impedance Zsrc. The MOS transistor bias was chosen as a compromise between noise and gain performance. The small signal circuit is shown in Figure 7.

3.2. Transformer Specifications and Voltage Gain

To achieve C_{gd} neutralization, the transformer turn ratio n divided by the coupling factor k should be equal to the ratio between C_{gs} and C_{gd} with a negative sign (1), which is approximately 2.3 in the used technology.To maximize gain, the turn ratio should be as high aspossible and Ls should resonate with ($n2C_{gd}$ + C_{gs}) to tune out these parasitic capacitances. The former leads along with (1) to a high |k| (which is ±1 at maximum), and the latter sets the inductance value for the inductors used in the transformer. The resulting voltage gain then converges to n. Given a certain MOS transistor width at the chosen bias the transformer properties are thereby known.

3.3. Transformer Design

The transformer used in the LNA was constructed using EM simulation software (ADS Momentum). The resulting structure is shown in Figure 8. The transformer has been optimized to have high |k| and high Q-factor inductors [Ref *11*]. To satisfy equation (1) a turn ratio n of 1.8 has been chosen along with a coupling factor k of - 0.76. The simulated Q-factors of the inductors are higher than 10 at the frequency of interest. Simulated values for L_d and L_s are respectively 137 pH and 42 pH. A patterned shield has been placed underneath the transformers to reduce substrate coupling.

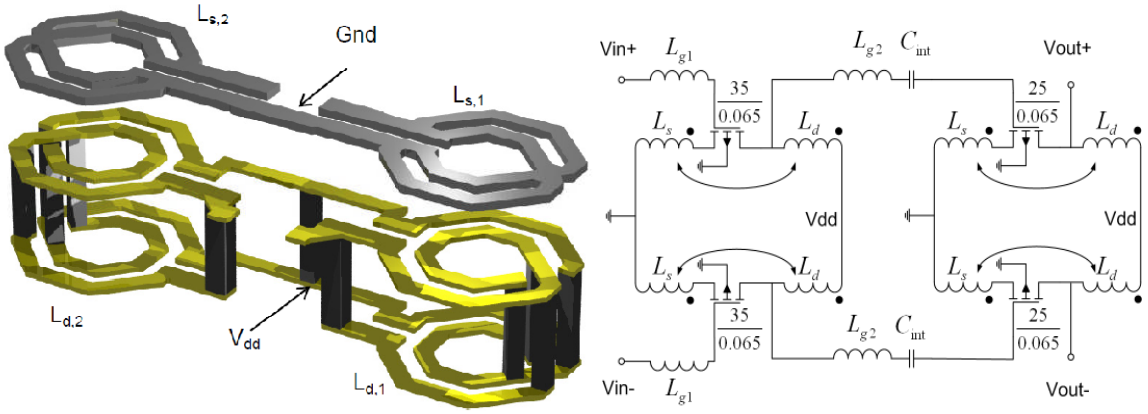


Figure 8: Left: Used transformer structure. For reasons of clarity the vias connecting the two bottom metals are only shown at the beginning and at the end of the metal strips. In reality many vias are distributed along the metal lines. The top inductor (L_s) connects two metal lines in parallel to lower the inductance and increase the Q-factor. The lower inductor (L_d) has two turns. The two inductors are placed exactly on top of each other to achieve the highest possible coupling ($|k| \leq 1$). The width of the metal lines is chosen to be 3 µm. Right: The schematic of the realized two stages LNA.

3.4. Layout Consideration

In Figure 8 the layout of the core of the LNA is shown. At the left the differential input of the first stage is shown and at the right the differential output of the second stage. The two stages are connected to each other with a DCblocking capacitor between the output of TF1 and the input of Lg2. All RF interconnects longer than 10µm used were simulated in ADS Momentum and Cadence RCextraction was used for all other structures. Lg1 and Lg2 are approximately 110 pH and 150 pH respectively. The transistors are indicated in Figure 9and are situated underneath the metal lines connecting the transformer structures. Transistor width stage 1 is 35 µm and stage 2 is25 µm. The vertical lines surrounding the transformers are the DC power lines and biasing of the LNA. Coplanar waveguides with shielding have been used to connect the different components to each other. This results in low coupling to the substrate and between components. The input and output of the LNA are connected to bondpads using CPWs (see Figure 9). This results in losses and an impedance shift. The resulting source and load impedance of the circuit at the input and output indicated in Figure 9 is approximately 37 + j10 Ω. Open-short-load structures are added to de-embed the circuit. A lot of effort has been put into making the design as symmetrical as possible to reduce common mode.

3.5. Simulation Results

The design consisted of an iterative process between circuit simulations, EM simulations and RC-extraction. After the first circuit simulation a Gt of 13 dB with a NF of 3.1 dB was simulated at 61 GHz. The IIP3 of the LNA was

approximately 2.6 dBm with a 1 dBc of -11.8 dBm. After EM-simulation and RC-extraction the performance changed due to the parasitic effects. Gt decreased by 2.3 dB to 10.7 dB and the NF increased by 0.5 dB to 3.6 dB. These simulation results are shown in Figure 5. The IIP3 increased to 4 dBm and the 1 dB compression point increased to -9.8 dBm. The simulated Gt variation in the band of interest is smaller than ± 0.15 dB and the 3 dB bandwidth is approximately 50 - 73 GHz which is approximately 37 % of the center frequency at 61GHz. The simulated power consumption is 35 mW at 1.2 V supply and 0.8 V gate bias. All simulations were performed using a source impedance of 30 Ω, which was chosen as a compromise between NF and Gt. This is not equal to the conventional 100 Ω for a differential topology. This is because the antenna could be connected directly to the LNA, allowing a different antenna (source) impedance.

3.6. Measurements And Verifications

To verify the behavior of the LNA a number of measurements were performed using a differential measurement setup. DC power consumption is seen to be equal to the simulated value of 35 mW. The NF and sparameters are verified independently by the Technical University Eindhoven and NXP Research. The S-parameters were measured using Agilent E8361A PNA. Calibration was verified using WinCal XE software. After de-embedding the measured Gt with Zsrc = 30 Ω is 10 dB at 61 GHz (Figure 6). The measured in-band deviation is ± 0.25 dB. The s12-parameter is below -47 dB over the entire measured band of 55 - 67 GHz and the group delay is ≈ 20 ps and behaves constant over the band of interest. The differential stability factor (K-factor) stays above 30 in the measured band. In common mode, the maximum transducer gain is equal to -2 dB resulting in a CMRR of 12 dB. The s12- parameter is below -42 dB, and K-factor stays above 70 in this case.

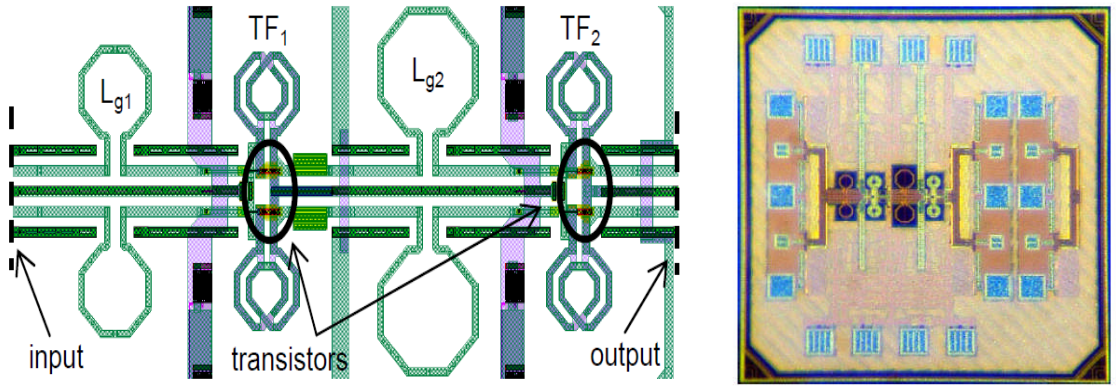


Figure 9: Left: Layout of the LNA (330 x 170 μm^2). Shown are only the top metal layers to clarify the structure. Patterned shields are used underneath the inductors, transformers and coplanar waveguides (not shown). In and output reference planes are indicated by the dashed lines. Right: Total LNA chip with bondpads and one de-embedding structure. Size die = 960 x 980 μm, size LNA = 330 x 170 μm^2.

TABLE I BENCHMARKING

Reference	Process	Topology	G_t (dB)	NF (dB)	3 dB BW	IIP_3 (dBm)	V_{dd} (V)	P_{DC} (mW)
[5]	90 nm	3 stage CS	15	4.4	10 %	N/A	1.3	4
[6]	65 nm (SOI)	2 stage casc.	12	8	22 %	N/A	2.2	36
[7]	90 nm	2 stage casc.	14.6	<5.5	25 %	-6.8	1.5	24
[8]	65 nm	2 casc. + 1 CS	22.3 (A_v)	6.1	13 %	N/A	1.2	35
[9] (LNA + mixer, HG)	45 nm	2 stage casc.	26	6	N/A	-12	1.1	23
This work	**65 nm**	**2 stage CS**	**10**	**3.8**	**37 %**	**4**	**1.2**	**35**

NF was measured in the band 59.5 – 66 GHz (Figure 6). Zsrc during this measurement is equal to 37 + j10 Ω, while the input reflection coefficient for the noise source stays below -15 dB. The average measured value in this band is equal to 3.8 dB. To the author's knowledge this is the lowest value found in literature around 60 GHz. NFmin of the circuit is found to be 3.7 dB using a load-pull setup in NXP. During this measurement the source impedance for NFmin was also verified with the simulated value. 13BC.

The measured IIP3 is equal to 5 dBm at 57.5 GHz and 4 dBm at 60 GHz which is in close agreement with the simulation. Measured 1 dBc is -4.6 dBm and deviates from the simulated value because in simulation a Zload of 100 Ω was used.

3.7. Benchmarking

The performance of existing 60 GHz LNAs is compared with this work in table 1. The LNAs presented in [Ref *5* to Ref *7*] are single ended, and [Ref *8*] has a differential output. It is seen the work presented in this section shows the lowest NF along with the highest bandwidth. The relative low gain isbecause only 2 CS stages are used. The use of feedback results in a high IIP3.

4. 60 GHz Zero-IF Mixer utilized with a three Dimensional Tuning

The zero-IF receiver architecture is a promising candidate for mm-wave high data rate communication. While offering the possibility of low-cost and compact solutions for receivers operating in the license-free band around 60GHz, zero-IF architecture suffers from problems such as dc offset, flicker noise, and second order intermodulation distortions. In this section the wideband minimization of second order intermodulation distortions (IMD2) in a 60GHz mixer is investigated. Multi-Gbps applications envisioned for 60GHz band require the zero-IF mixer to provide around 1GHz of IF bandwidth. Therefore, any IMD2 cancelation mechanism applied to such a mixer must be functional across a wide frequency range. Thus, narrowband IMD2 cancelation techniques are not beneficial in this case. However, conventional single-parameter and double-parameter tuning techniques appear to be ineffective for high IF bandwidth applications. Therefore, in this section a three-parameter tuning method is proposed and is shown both in theory and measurement to be effective in wideband cancelation of IMD2.

4.1. Second Order Intermodulation Mechanisms

Downconversion mixer is normally the main contributor to second order nonlinearity distortions in a zero-IF receiver. The low-frequency second-order distortions generated in the RF path preceding the mixer can easily be filtered by RF coupling or band-pass filtering. Figure 10 shows a typical Gilbert-cell-like mixer used in this article [Ref *12*]. Input RF voltage is applied via two RF-coupling capacitors to the switching stage. The transistors M1-M4 are responsible for switching and downconverting the RF signal. At the output, the downconverted signal is converted from the current domain to voltage domain by means of the resistors (R_L). The C_L capacitors represent the input capacitance of the following stage as well as the parasitics of the switching transistors at the output node. The differential output IMD2 voltage ($V_{imd2,out}$), comes from two sources: 1) the common-mode output IMD2 current combined with output load mismatch and 2) the differential-mode output IMD2 current, as defined in (2).

$$I_{imd\,2CM} = \frac{I_{imd\,2,1} + I_{imd\,2,2}}{2}, I_{imd\,2Diff} = I_{imd\,2,1} - I_{imd\,2,2} \qquad (2)$$

where, $I_{imd2,1}$ and $I_{imd2,2}$ are as shown in Figure 10. The differential output IMD2 voltage is described as a function of these currents in (3):

$$V_{imd\,2out} = I_{imd\,2,1} Z_{L,1} - I_{imd\,2,2} Z_{L,2} \qquad (3)$$

where, $Z_{L,1}$ and $Z_{L,2}$ are the impedances seen from V_{out}^{+} and V_{out}^{-} nodes to the RF ground respectively as shown in (4), where, R_{out} is the resistance seen from the output node.

$$Z_{Li} = \frac{R_{outi}}{1 + R_{outi} C_{Li}\, j\omega} \qquad (4)$$

Defining a nominal value for output impedance as in (5), the differential output IMD2 voltage can be rewritten as a function of common-mode and differential-

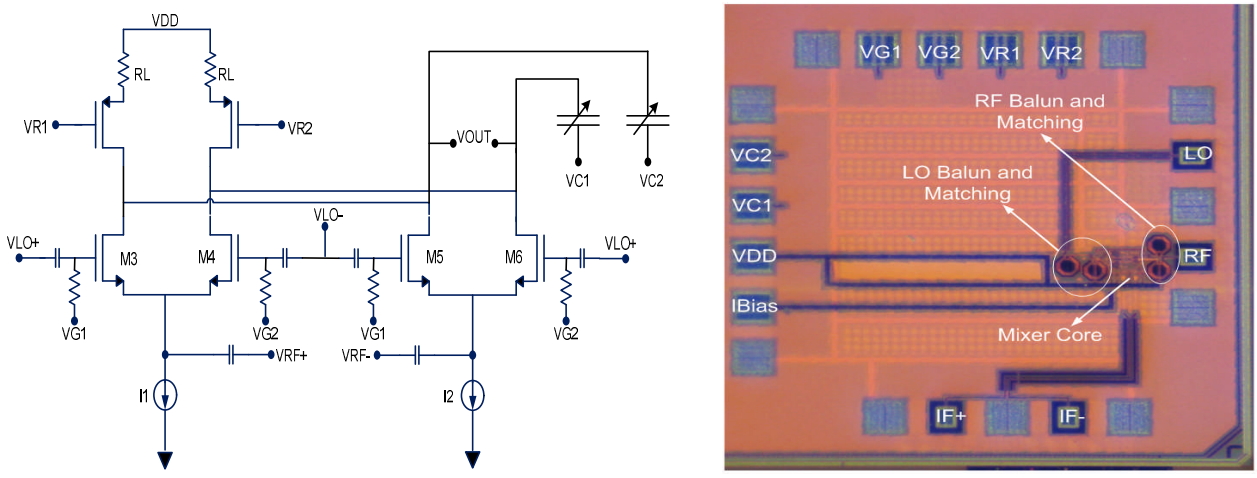


Figure 10: Left: Circuit schematic of the Gilbert-cell-like mixer with tunable output impedance and tunable gate biasing. Right: Die photo of the mixer

mode output IMD currents as depicted in (6).

$$Z_{L,1} = Z_L(1+\delta z_L)$$
$$Z_{L,2} = Z_L(1-\delta z_L) \quad (5)$$

$$V_{imd\,2out} = 2I_{imd\,2CM} Z_L \delta z_L + I_{imd\,2Diff} Z_L \quad (6)$$

I_{imd2CM} is a function of the input-stage and switching stage even-order nonlinearities and is present at the output current even if there is no mismatch in the circuit. However, it can be vanished in the differential output voltage by a perfect matching between Z_{L1} and Z_{L2}.

Three mechanisms are responsible for generation of Iimd2DIF: self-mixing, input stage nonlinearity combined with switching pair mismatches, and switching pair nonlinearity combined with its mismatches [3]. Self-mixing is a result of the leakage of RF signal to the LO and vice versa. This mechanism is in general a function of the layout parameters and its contribution is zero in an ideally matched fully balanced downconverter. However, in practice any kind of mismatch in the LO or RF paths can activate this mechanism. The contribution of second and third mechanisms is determined by the mismatch between transistors in the switching pair [Ref 13]. The mismatch between the two transistors in a differential pair can be represented by an equivalent voltage offset at the gate of one of them [Ref 14]:

$$V_{off} = \Delta V_T + \frac{\partial f}{\partial \beta}\Delta\beta + \frac{\partial f}{\partial \theta}\Delta\theta \quad (7)$$

$$f = \frac{\theta}{\beta} I_{DS}\left(1+\sqrt{1+\frac{2\beta}{\theta^2 I_{DS}}}\right)+V_T \quad (8)$$

where, I_{DS} is the biasing current of the transistor, $\beta=\mu_n C_{ox} W/L$, θ is the factor taking into account the velocity saturation effect, and V_T is the threshold voltage. Therefore, these mechanisms can only be activated if there is mismatch between the switching stage transistors and the effective mismatch between transistors can be controlled by modifying the threshold voltage or biasing voltage of the gates of transistors. The latter approach, as a circuit-level parameter tuning, is

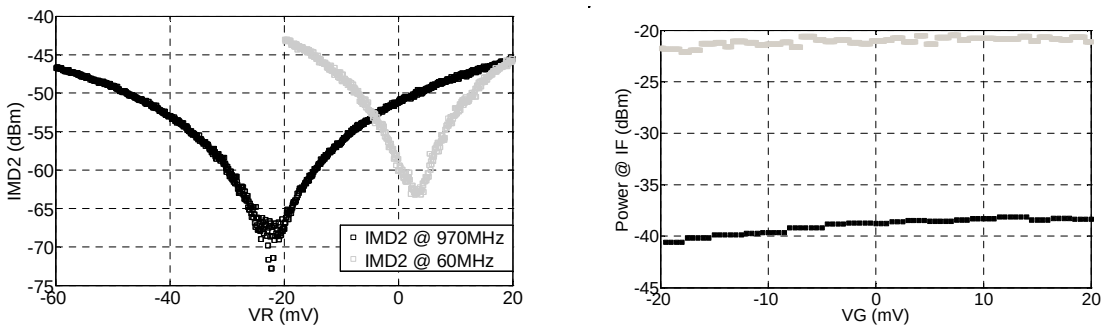


Figure 11: Left: IMD2 vs. a) variable resistance control voltage b) varactor control voltage.

considered in this work to avoid the requirement for very accurate tuning of the threshold voltage in the process.

4.2. Wideband Imd2 Cancellation

Vimd2out can be minimized by tuning different parameters. Single-parameter tuning methods can adjust Voff to vary Iimd2DIF [Ref *15*]. They can also adjust output resistance mismatches (δRout) or output capacitance mismatches (δCL) to vary δzL [Ref *16*]-[Ref *17*]. To make the two terms in (6) cancel out each other by tuning only one parameter, the following should be satisfied:

$$\delta z_L = \frac{\delta R_{out} - R_{out} C_L \delta C_L j\omega_b}{(1 + R_{out} C_L j\omega_b)} = -\frac{I_{imd2Diff}}{2 I_{imdCM}} \tag{9}$$

where, ω_b is the IMD2 frequency at the output of the mixer. Higher powers of δR_{out} and δC_L are neglected in this approximation of δz_L. However, choosing only one parameter to tune, can only satisfy (9) at one single frequency point, because for each frequency the tunable parameter has a different optimum.

Even a two-dimensional tuning involving δR_{out} and δC_L is not sufficient [Ref *17*], because it can only set (6) to zero at a single frequency point. Of course one might suggest using higher order filters as Z_L which can annul (6) at multiple frequency points, but that would complicate the baseband filter design and the parameters needed to be tuned increase with the required flatness of IMD2 over the IF band.

The approach chosen in this work is tuning all three parameters at the same time. This will result in simultaneous nullification of both terms in (6) as shown in (10). Since both δR_{out} and δC_L are set to zero in this approach, nullification of δz_L is (ideally) frequency-independent. Due to narrowband assumption of interferer at RF, V_{off} can be chosen in a way that all three mechanisms responsible for $I_{imd2Diff}$ can cancel out each other.

$$\delta z_L = \frac{\delta R_{out} - R_{out} C_L \delta C_L j\omega_b}{(1 + R_{out} C_L j\omega_b)} = 0, I_{imd2Diff}\left(V_{off}\right) = 0 \tag{10}$$

4.3. Circuit Design

Variable resistors and varactors are added to the output, to provide tunability of the output impedance as required by (10). Variable resistors are in the simple form of series transistors biased in the triode region. The biasing of the gates of the switching pair transistors, can be adjusted separately for each half-circuit as required by (10).

The circuit is designed and fabricated in CMOS 45nm technology and the die photo is shown in Figure 10. The supply voltage (VDD) is 1.1V. VR1 and VR2, which control the value of the variable resistors, are differentially tuned around 100mV. VC1 and VC2 control the varactors to tune the output capacitance and are differentially tuned around 500mV. VG1 and VG2 tune the biasing voltage of the gate of switching pair transistors and are differentially tuned around 0.9V.

IBias draws 300μA and with a current mirror translates approximately the same current to I1 and I2 in Figure 10. Therefore the circuit in Figure 10 draws less than 600μA from VDD. The complete chip includes the mixer core shown in Figure 10 as well as two active baluns and matching networks at RF and LO inputs. In addition an IF buffer is used at the IF output to drive the 50 Ohm load of the measurement equipment. Four inductors are used in the design. Two of them are used in the input matching networks and the other two are the loads of active baluns.

4.4. Measurement And Experimental Results

To test the capability of IMD2 cancelation across a wide IF frequency range, a three-tone out-of-band signal is applied to the RF input of the mixer to emulate an out-of-band interferer. The three tones are at 61.07GHz, 61.130GHz, and 62.1GHz. The LO signal is at 60GHz. Therefore, the resulting IMD_2 terms are at 60MHz and 970MHz which are measured as a function of the tuning parameters. There is another IMD2 term at 1030MHz which is considered as out-of-band and is not measured. The closest fundamental term of the downconverted interferer is at 1070MHz which is also measured as a function of tuning parameters to see how much the conversion gain can be affected by IMD_2 cancellation. One of the IMD_3 terms is also measured to observe the variation of IMD_3 due to IMD_2 cancelation.

First of all, the single-parameter tuning is examined. Figure 11Figure 12 shows the variation of IMD_2 as a function of the control voltage of the variable resistors. This voltage is varied differentially around a common value of 100mV. IMD2 at 60MHz is minimized at around 5mV whereas IMD2 at 970MHz is minimized at around -20mV. In fact, when IMD2 at 970MHz is minimized, IMD2 at 60MHz is significantly degraded. The same problem is observed when only one of the other two parameters, VG or VC, is tuned .Figure 11 shows the variation of IMD2 when VR and VC are changed simultaneously while keeping VG equal to zero. VR is swept from -40mV to 40mV in steps of 0.5mV and in each step VC is swept from -300mV to 300mV in steps of 5mV. According to Figure 12 IMD2 at 60 and 970MHz are never at the lowest points simultaneously, proving the inefficiency of two-dimensional tuning in this case.

However as shown in Figure 12 when VG is also tuned an optimum point can be found where both 60MHz and 970MHz IMD2 terms can be reduced to -70dBm. In this case three-dimensional tuning improves the IMD2 components at 60 and 970MHz by 10 and 20dBm respectively.

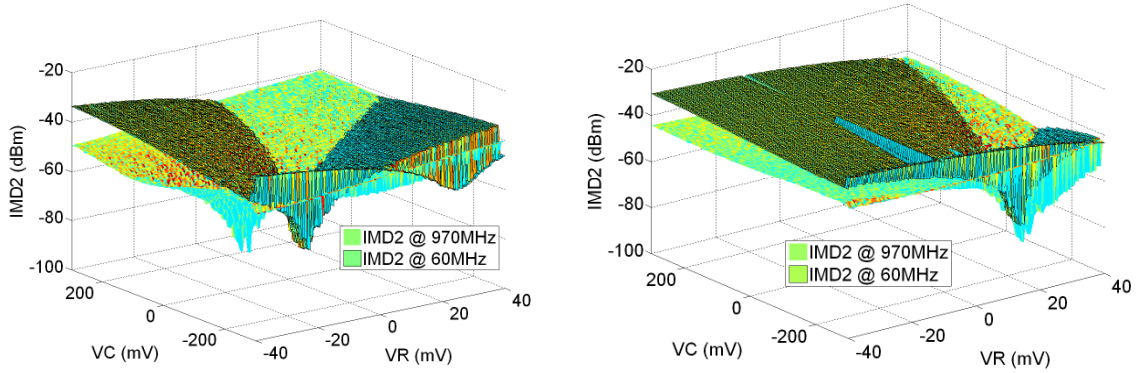


Figure 12: Left: IMD2 tuning by simultaneous variation of VC and VR while keeping VG constant at 0. IMD2 tuning by simultaneous variation of VC and VR while keeping VG constant at -10mV

These results demonstrate both in theory and measurement that a three-dimensional tuning is beneficial for wideband cancelation of second order intermodulation distortions (IMD2) in a zero-IF downconverter. The resistance and capacitance at the output of the mixer as well as the gate biasing of the switching pairs are tuned together to suppress IMD2 across a wide bandwidth. A 60GHz zero-IF mixer is designed and measured on wafer to show that the proposed tuning mechanism can simultaneously suppress two IMD2 tones with a frequency difference of 910MHz while having minor effect on conversion gain and third order intermodulation distortions.

5. A 40-GHz Phase-Locked Loop for 60-GHz Sliding-IF Transceivers

Figure 13a illustrates a generalized two step down-conversion, sometimes also referred to as sliding-IF architecture. The incoming RF signal f_{RF} is first down-converted by mixing with the RF local oscillator signal $f_{RF\text{-}LO}$ producing a difference component at $f_{RF} - f_{RF\text{-}LO}$. The second down-conversion to baseband is achieved by using the output of the prescaler $f_{IF\text{-}LO}$. The factor 'M' is an integer frequency multiplier which usually has a range between 1 and 3. The value of 1

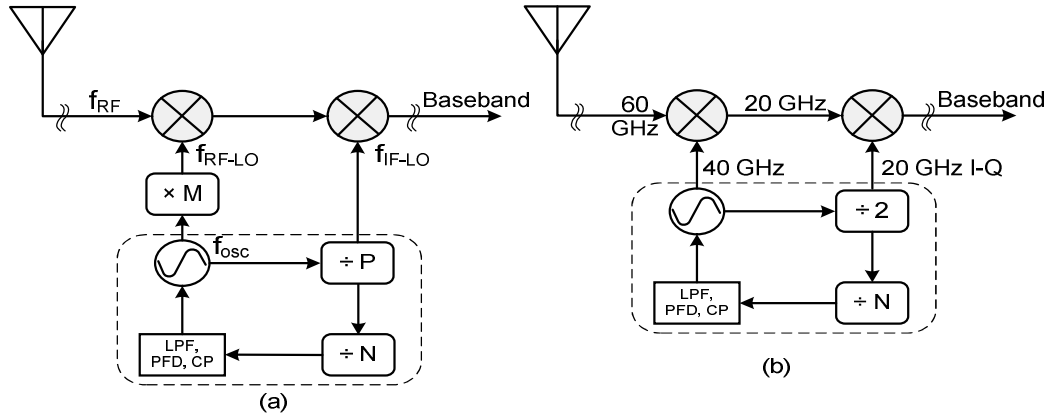


Figure 13: Generalized PLL architecture for 60 GHz transceivers

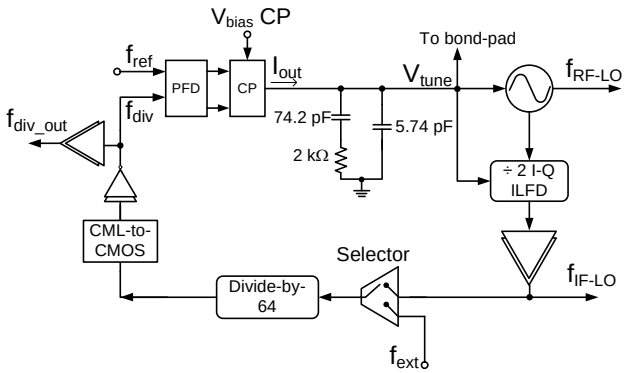


Figure 14: 40 GHz PLL block diagram

implies a direct connection between the oscillator and the mixer, whereas the values 2 and 3 imply a frequency doubler and tripler, respectively. The factor 'P' is the division ratio of the prescaler and can also have a value between 1 and 3. The overall division ratio of the synthesizer is separated into 'P' and 'N' as the prescaler requirements and utilization in mm-wave synthesizers is distinct from the lower frequency divider chain. The frequency conversion to baseband is carried out as:

$$f_{RF} - f_{osc} \times M = \frac{f_{osc}}{P} \quad , f_{osc} = f_{RF}\left(\frac{P}{MP+1}\right) \tag{11}$$

Using different values for M and P between 1 and 3 in (11) yields synthesizers operating at different frequencies. For instance, for M=1, P=1 the synthesizer operates at 30 GHz and provides both the RF-LO and IF-LO signals. This architecture is termed as "half-RF" and offers the lowest possible LO without doublers or triplers. However, it has two major drawbacks: third harmonic image and LO-IF feed-through. Other demonstrated combinations include M=3, P=2 and M=2, P=2. The former operates the synthesizer at ~17 GHz and using a frequency tripler to down-convert the RF signal to 8.5 GHz. The conversion to baseband is by using the outputs of the prescaler [Ref *18*]. The latter uses a 24 GHz PLL and 48 GHz and 12 GHz as the first and second down-conversion steps. In this paper, a fully integrated 40 GHz PLL is presented (using M=1, P=2) as shown in Figure 13b and Figure 14.

The required quadrature IF-LO is provided by the prescaler to down-convert the 20 GHz IF signal to baseband. This architecture prevents the need for doubler or tripler circuits as they tend to be lossy at these frequencies and typically do not provide quadrature outputs. Furthermore, it provides a good trade-off between tuning range and phase noise requirements and enables to satisfy the IEEE 802.15.3c channelization requirements.

5.1. Circuit Design

Frequency synthesizers operating below 10 GHz can utilize broadband static prescalers, so there is no issue of synchronization between the VCO and the prescaler (together termed as PLL front-end) as the latter can easily cover the

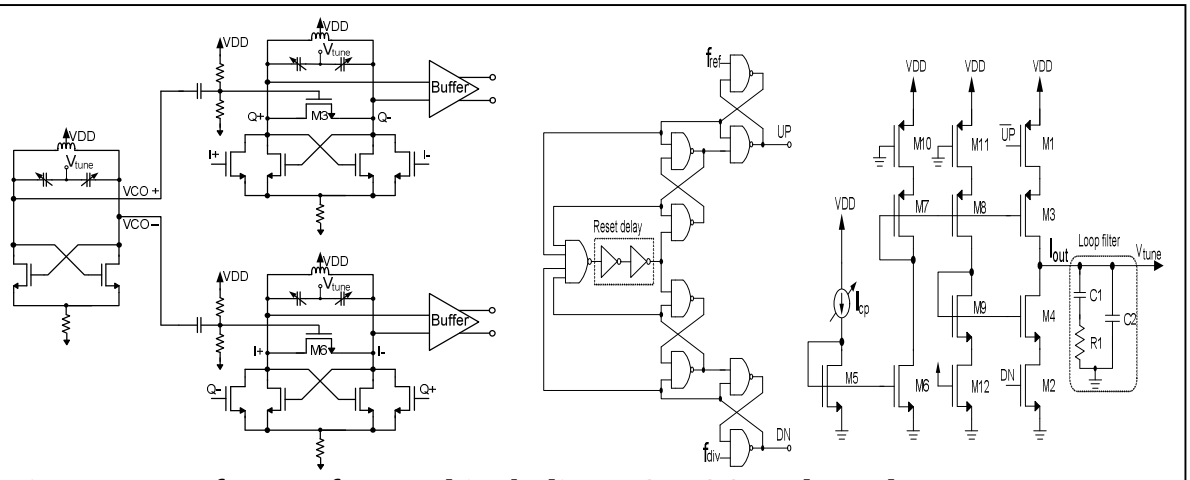
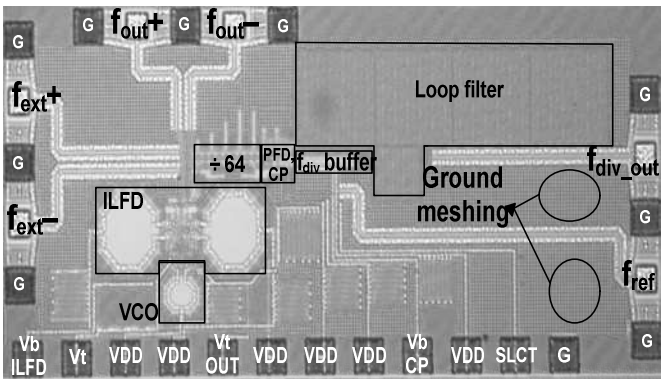


Figure 16: Left: PLL frontend including LC-VCO and quadrature ILFD. Middle: PLL backend components, PFD. Right: charge pump.

complete tuning range of the VCO. In contrast, mm-wave synthesizers generally use LC based VCOs and prescalers, and their frequency selectivity necessitates careful alignment of their respective working ranges. Any frequency mismatch due to design inaccuracy or layout parasitics can reduce the effective operation range of the synthesizer or, in worse case, make it completely devoid of locking. The complete schematic of the PLL front-end is shown in Figure 16. The 40 GHz VCO shown on the left hand side is based on an NMOS-only cross coupled topology and the tank is formed by a top metal single-turn inductor and a varactor setup. The maximum and minimum capacitances are 106 fF and 30 fF resulting in a C_{max}/C_{min} ratio of 3.53. The Q-factor of the varactor setup is between 6 and 20, for a tuning voltage of 0 to 1.2 V. The post-layout simulation of the VCO yields a frequency tuning range (FTR) from 38 to 45GHz (16%). The VCO consumes 5mA from a 1.2V supply and the peak-to-peak amplitude is about 1.5V.

The quadrature injection locked frequency divider is also shown in Figure 16. The differential outputs of the VCO are injected to the input transistors M3 and M6 present in the two separate stages of the ILFD which are coupled in anti-



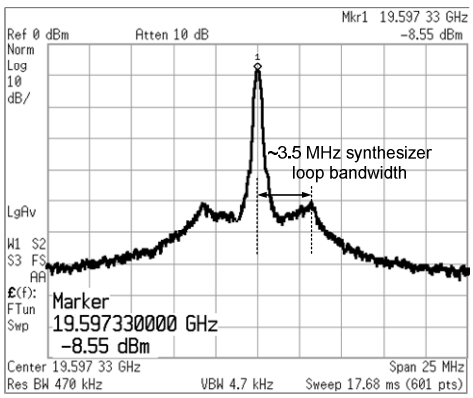


Figure 15: Left: Die micrograph of 40 GHz PLL. Right: Figure 6. Close-in spectrum of a locked PLL frequency.

Table II: Performance summary and comparison of PLL

Reference	[Ref *19*] ISSCC 10	[Ref *20*] ISSCC 08	[Ref *21*] JSSC 07	[Ref *22*] ISSCC 07	This work
Tech. [nm]	65 CMOS	90 CMOS	130 CMOS	90 CMOS	65 CMOS
Supply [V]	1.2**	1.2	1.5	1.2	1.2
VCO range [GHz]	17.5 to 20.94 (17.9%) 35 to 41.88 (17.9%)	39.1 to 41.6 (6.2%)	45.85 to 50.6 (9.8%)	58 to 60.4 (4.1%)	38.2 to 43.6 (13.2%)
Phase Noise [dBc/Hz]	-100 (at 20 GHz)	-90 (@ 1MHz)	-72 (@1 MHz)	-85.1 (@1 MHz)	-89.7 (@ 1MHz)
fref [MHz]	36	50	45.1	234.1	300
Ref. spurs [dBc]	-50	-54	-40 to -27	-50.4	-42
Power [mW]	80	64*	45.8*	80	22.8*
Area [mm^2]	1.6x1.9	1.77x0.87	1.16x0.75	0.95x1	1.67x 0.745

* Excluding buffers, ** Supply for PFD and CP is 1.8V

phase to generate 90° spaced outputs. As the output swing of the VCO is sufficiently large, buffers are not required between the ILFD and VCO, which greatly simplifies the routing during layout and decreases the power consumption of the overall system.

The divide-by-64 block consists of six cascaded divide-by-2 stages which are optimized individually for low power consumption and required output power.Each divide-by-2 stage is based on current-mode-logic (CML) D-latches in negative feedback. The differential small-swing output from the last stage is converted to rail-to-rail square pulses for comparison in the PFD by means of a differential to single-ended converter followed by a pair of inverters.

5.2. Layout And Technology

The PLL is fabricated (Figure 15) in TSMC bulk CMOS 65nm LP (low-power) process having six metallization layers. The process offers MIM capacitors and poly-silicon resistors. The measured f_T of NMOS and PMOS transistors is 140 GHz and 80 GHz, respectively. The layout is done compactly to avoid parasitics, especially in the PLL front-end. Due to bond-pad limitation, only the ILFD output is measured. Transmission lines are used for all RF inputs and outputs. These TL's are coplanar waveguide based with lateral ground plane consisting of all metal layers. The width of the TL is 5µm and spacing from the ground plane is 4.22µm. The total chip-area of the synthesizer including bond-pads is 1.67 x 0.745 mm^2.

5.3. Measurement Results

The PLL is measured on wafer using Agilent PSA (E4446A) and LeCroy real-time oscilloscope (Wave Master 830Zi). The free-running center frequency of the PLL is observed at 20.2 GHz and the VCO and ILFD consume 5 mA and 9 mA from a 1.2 V supply, respectively. The divide-by-64 block is included in the circuit by keeping the selector voltage HIGH and the divided frequency of ~315

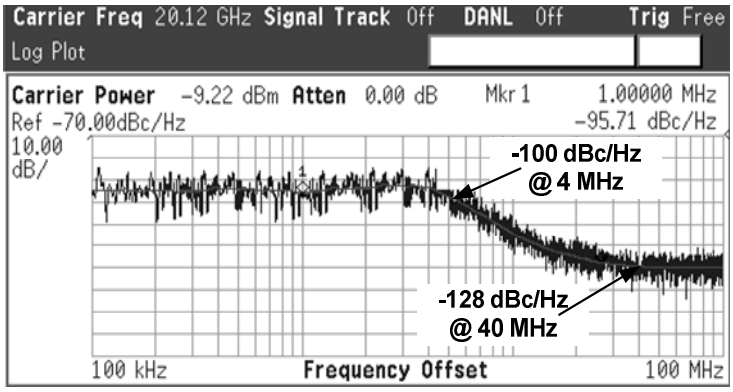


Figure 17: Measured phase noise of the PLL

MHz is observed on the oscilloscope. The divide-by-64 circuit consumes 6 mW and the corresponding output buffer which is a cascade of four inverter stages consumes 2 mW. Both, the divided signal and the reference signal are observed on the oscilloscope. The reference signal is varied in steps from 290 - 344MHz, which corresponds to an output frequency of 18.5 to 22 GHz (or 37 to 44 GHz at the VCO output). From these values, the ILFD output of the synthesizer locks between 19.1 to 21.8 GHz. The corresponding locked frequency range at the VCO output is 38.2 to 43.6 GHz. Thus, the PLL can down-covert a 60GHz signal within a range of 57.3 to 65.4 GHz, thus covering all the four high-rate PHY (HRP) channels of the IEEE 802.15.3c standard. A locked spectrum for a reference frequency of 306.2 MHz is shown in Figure 15.

In a typical PLL, the sideband spectrum noise is cleaned-up within the loop bandwidth which is evident by the highlighted area in Figure 15. The loop bandwidth estimated from the screenshot is about 3.5 MHz as opposed to the calculated value of 4MHz. The output power of -8.55 dBm also includes the 1.5 to dB of cable and other measurement related losses.

The phase noise of the synthesizer is measured by the spectrum analyzer at the ILFD output and reflects its loop performance. Figure 17 shows one typical plot for a locked frequency of 20.12 GHz from 100 kHz to 100 MHz. The value at 1

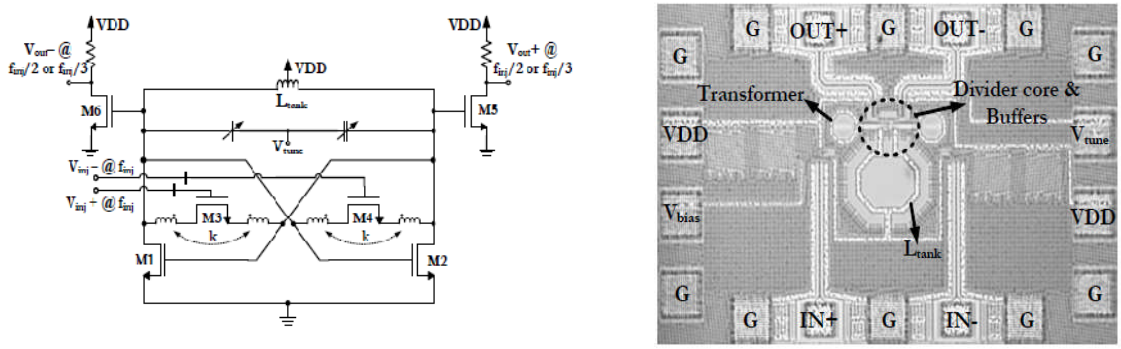


Figure 18: Left: Dual-mode ILFD circuit schematic and output buffer. Right: Chip micrograph of DM-ILFD

MHz, 4 MHz and 10 MHz offset from the carrier is -95.7, -100 and -118 dBc/Hz, respectively. The first of the above values is the in-band phase noise (within the loop bandwidth), the second at the calculated loop bandwidth (forming the "knee") and the third corresponds to the out-of-band phase noise. The variation of phase noise over the synthesizer operation range is + 2.5 dB. The phase noise at the VCO output (at double the frequency, i.e. 42.24 GHz) can be estimated by adding 6 dB to the above mentioned values, resulting in -89.7, -94 and -112 dBc/Hz at 1 MHz, 4 MHz and 10 MHz offsets from the carrier, respectively. The presented PLL is compared with published works in Table II. It is the only design which covers all four HRP channels of the IEEE 802.15.3c standard. It demonstrates the lowest power consumption with the second highest locking range.

6. A DUAL-MODE MM-WAVE INJECTION-LOCKED FREQUENCY DIVIDER

The proposed ILFD shown in Figure 18 achieves dual-mode operation by preserving both even and odd harmonics, and features an increased locking range by improving both injection efficiency and varactor tunability. The former is achieved by direct differential injection via M3-M4, at the same time enhancing noise immunity as well as symmetric loading for a differential VCO. De-tuning of the Miller capacitances, introduced for the first time in an ILFD, improves the input-output transfer of the injection signal and cancels out the fixed tank capacitance, thus widening the locking range. This is achieved by a transformer feedback, which further accomplishes input matching without need for extra components.

In addition, the over-drive voltage of the injection transistors M3-M4 is increased resulting in an enhancement of their effective transconductance.

AC and transient simulations were used to determine the optimum transformer and injection-transistor parameters for achieving a wide locking range with minimum input power.The center-tap inductor of the LC-tank is a 9μm wide single-turn top-metal coil having an inductance of 192 pH and a Q-factor of ~28 around 20 GHz. The varactors provide a capacitance tuning of 150-39 fF and a Q-factor of 8 20, for a tuning voltage of 0-1.2 V. Operating at 0.8V, the circuit is

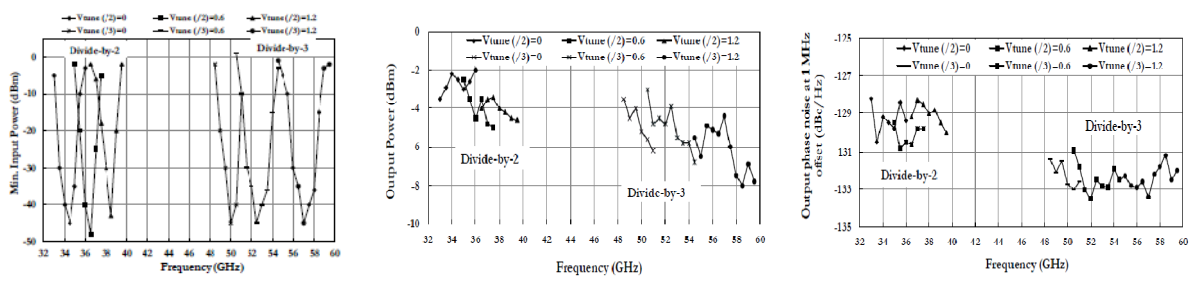


Figure 19: Left: Measured input sensitivity of DM-ILFD in divide-by-2 and divide-by-3 mode. Middle and Right: Measured output power and phase noise variation in the two division modes for different tuning voltages:

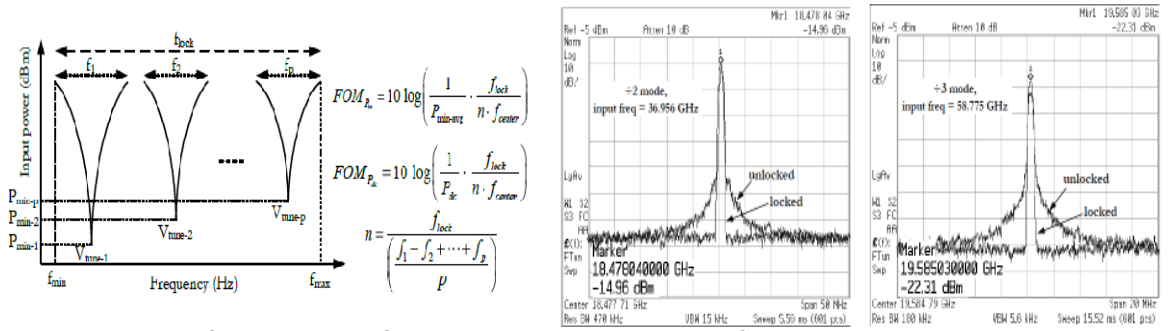


Figure 20: Left: Figure-of-merit principle and definitions. Middle and Right: Measured locking operation in the two division modes.

also suitable for future CMOS processes. The RF-input is AC coupled on-chip and the output employs a 50Ω matched differential common-source buffer (M5-M6) for measurement purposes. he basic purpose of the transformer, as mentioned, is to transfer the injection signal without loss to the drain and source of M3-M4 for signal-mixing. As the required inductance is below 100pH, a small structure with high self-resonance frequency could be chosen. In order to achieve high coupling and Q-factor, the top two metal layers (Me6, Me5) are used and placed exactly on top of other (Figure 18). Me1 is placed below the transformer to improve substrate isolation and reduce capacitive coupling to the substrate.

6.1. Layout and technology

Figure 18 shows the micrograph of the 65nm bulk-CMOS DM-ILFD IC. A separate transformer along with de-embedding structures (open, short, load) is also fabricated. Coplanar transmission lines, wideband 50Ω matched including the bond-pads, are used at input and output. The core DM-ILFD circuit occupies 200x150µm2 and the total chip area is 800x500µm2. The transformer is smaller than a 'ground' bond-pad and only occupies 54x52 µm2.

6.2. Measurement Results

The measured inductances of the primary and secondary coils of the transformer are 70 and 88pH at 60 GHz, and 62 and 80pH at 35 GHz . At 60 GHz, the measured values differ by 3 and 14pH compared to the corresponding EM-simulated (in Momentum and Sonnet V12) values. The measured coupling factor at the two frequencies is 0.69 and 0.67, respectively. The input sensitivity curves of the DM-ILFD are shown in Figure 19. The free-running frequency of the DM-ILFD lies between 16.8 and 19.2 GHz for a tuning voltage (Vtune in Figure 18) of 0–1.2V while consuming 4mW from a 0.8V supply. A shift in center frequency due to an estimated ~50fF interconnect capacitance is observed. In divide-by-2 mode, with an input power less than -2 dBm, the locking range for each Vtune is about 3 GHz (8.27%) and total operating range is 33–39.5 GHz (17.93%). In divide-by-3 mode, the required input power is less than +1dBm whereas the locking range for each Vtune is about 4 GHz (7.4%), and the total operating range is 48.5–59.5 GHz (20.4%).

Table III: Comparison With Published Results of ILFD.

Ref	CMOS Tech. (nm)	Division ratio	Op. Fteq (Gliz)	LR. (%)	Pmin-avg (dBm)	Pdc (mW)	Ph. Noise (dBc/Hz @ 1 MHz)	Factor 'n'	FOM_{Pin}	FOM_{Pdc}
[Ref 25] ASSCC 07	130	3	66 - 72	9.1	-13	2	-120.8	1.63	30.4	12.6
[Ref 26] MWCL 09	65	3	48.8 - 54.6	11.2	-55.2	3	-115	5	69.7	8.7
[Ref 27] WITS 08	90	2	35.7 - 54.9	42.3	-26	0.8	-118.4	1	52.2	27.2
[Ref 28] MWCL 08	130	2	25 - 31.2	22	-39	1.86	-130	1	62.4	20.7
[Ref 29] ISSCC 09	130	2 3	35.6 - 39.3 53.8 - 57.8	9.8 7.1	-18 -12	3.12	-133.7 -131.5	1.57 2	35.9 28.9	13.0 12.0
This work	65	2 3	33 - 39.5 48.5 - 59.5	17.9 20.4	-45.3 -45	4 4	-130.6 -132	2.29 2.86	64.2 63.5	12.9 12.5

Figure 19 shows an example of the locking operation. A maximum variation of +3 dB and +1.15 dB is observed in the de-embedded output power and phase noise over the complete operating range as shown in Figure 19 for different tuning voltages in the two division modes. The phase noise at a locked output of 19.05 and 16.6 GHz in divide-by-2 and divide-by-3 mode is -130.6 and -13dBc/Hz at 1 MHz offset, respectively. These values are within + 0.2dB to the theoretical 6 and 9.5 dB difference (due to frequency division) from the generator phase noise.

6.3. ILFD Figure-Of-Merit

For proper comparison to state-of-the-art ILFDs, two new figure-of-merits (FOMs) are introduced here. Varactor tuning is widely adopted to increase the operating range of ILFDs [Ref *25*-Ref *26* and Ref *29*]. It is noticed, however, that two different definitions are used for locking ranges obtained with [Ref *24*] or without [Ref *26*] varactor tuning. Therefore, an appropriate comparison demands a FOM incorporating the number of required varactor tunings to cover the complete operating range. Furthermore, input injection power and DC power consumption are important benchmarks that should be reflected in the FOMs. To this end, the total locking range is divided (Figure 20) into p parts f_1, f_2,…, f_p, related to tuning voltages V_{tune-1}, V_{tune-2} ,…, V_{tune-p} and minimum input powers P_{min-1}, P_{min-2} ,…, P_{min-p}. Averaging both locking range and minimum input power leads to $f_{avg}= (f_1+ f_2+…+ f_p)/p$ and $P_{min-avg}= (P_{min-1}+ P_{min-2} +…+ P_{min-p})/p$. The total locking range (flock) thus equals n x f_{avg}. $FOMP_{in}$, also shown in Figure 20, reflects the injection efficiency by assessing the average injection power $P_{min-avg}$ (in watts) required for an average relative tuning range (f_{avg}/f_{center}), and $FOMP_{dc}$ reflects the tuning efficiency by assessing the DC power consumption needed for the same average relative tuning range.

Both FOMs comprise n and clearly, a lower value of n is preferred. It should be noted that without varactor tuning n equals 1. A higher FOM value indicates a better ILFD. A comparison with reported designs using the proposed FOMs and underlying parameters is shown in Table III. The $FOMP_{in}$ of the presented DM-

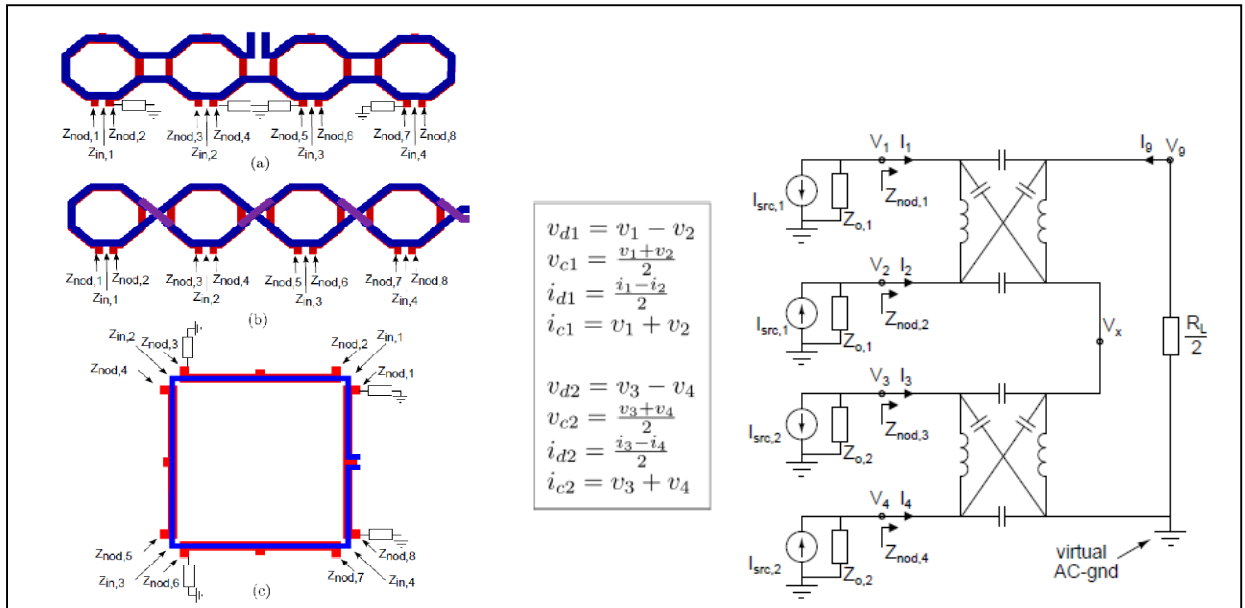


Figure 21: Left: DAT topologies. (a) Inline non-alternating topology with center output [Ref 33]. (b) Inline alternating topology with side output [Ref 33]. (c) Ring topology [Ref 30]. Primary inductors are in red and secondary inductors are in blue. Right: Simplified equivalent half-circuit diagram of Figure 18 (a).

ILFD, in divide-by-2 and 3 mode, is 28 and 34.5 dB better than the dual-mode ILFD in [Ref *29*] (ISSCC 2009), reflecting a considerable improvement in injection efficiency whereas the $FOMP_{dc}$ is comparable. Compared to the single-mode dividers, the 20.4% operating range of the DM-ILFD in divide-by-3 mode is better than [Ref *25*]-[Ref *26*], resulting in a better or comparable $FOMP_{in}$. The $FOMP_{dc}$, on the other hand, is lower than single-mode ILFDs in [Ref *27*]-[Ref *28*]. Finally, the operating range of 11 and 6.5 GHz at 60 and 35GHz can easily cover the respective mm-wave bands of a multi-mode synthesizer.

7. Fully Integrated 60GHz Distributed Transformer Power Amplifier

Realization of high speed short-range wireless communication systems has motivated the employment of the available6 GHz bandwidth around 60 GHz. Cost effective solutions for those applications can be achieved through the realization of fully integrated transceivers comprising the digital circuits in the main stream CMOS technology. However the low breakdown voltage of the active devices and the poor quality factor of passive components in CMOS technology have complicated the realization of power amplifiers capable of achieving the required output power and decent efficiency. The achievement of high power levels demands the realization of high ratio trans-impedance matching networks which declines the efficiency. As an alternative, one may use of distributed transformer power amplifier [Ref *30*] which enables simultaneous power combining and impedance matching. The inequality of transformers' input impedances engenders common-mode and unequal differential voltage-swings

which might prevent the achievement of maximum output power. To surmount these problems we present two universal methods by adding auxiliary tuning components and introducing different device size for each combining stage, instead of complicating the transformer design [Ref *31*], [Ref *32*].

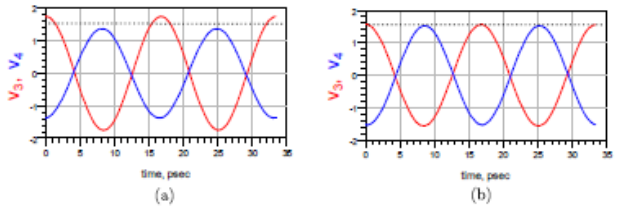


Figure 22: RF-voltages at nodes 3, 4 related to Figure 21(c). (a) beforeCM-compensation. (b) after CM-compensation. The dashed line indicates VRF;max.

7.1. DAT TOPOLOGIES

DAT topology is composed of two sets of magnetically coupled inductors from which the secondary is connected to the output and the set of primaries are connected to amplifiers, creating power combining stages. Since DAT topologies accumulate the voltages of all combining stages, proper performance of DAT demands the achievement of maximum voltage swings of each stage and processing negligible common-mode component. A literature survey reveals the existence of different DAT topologies [Ref *30*], [Ref 33], shown in Figure 21, which share a common problem regarding the inequality of input impedances.This inequality can occur between the values of differential input ports ($Z_{in;i}$) as well as between the individual nodes of those ports ($Z_{nod;i}$).

The latter engenders unbalanced voltage swings at the output of differential amplifier stages (common-mode component), while the former imposes unequal voltage swings among those differential amplifier stages due to unequal loadline terminations [Ref *34*]. This inequality might occur due to a combination of three mechanisms; different physical distances of power combining stages towards the output port (see Figure 21), asymmetric physical position of input nodes with respect to the virtual AC grounding and asymmetric interwinding capacitances (see Figure 21).

Table IV: Results Examples Common-Mode Compensation

Fig. 21		$Znod,1$	$Znod,2$	$Znod,3$	$Znod,4$
(a)	U	9.2+j7.8Ω	17.9 -j3.4Ω	17.4+j3Ω	25.2 -j5Ω
	C	11.3+j5.7Ω	12.5-j5.1Ω	19.6 -j0.3Ω	19.6-j7.8Ω
(c)	U	12.7+j1.5Ω	8.8 -j1.3Ω	7.7+j0.6Ω	10.2 -j0.2Ω
	C	10.9+j1.4Ω	9.2 -j0.1Ω	8.7 -j0.9Ω	8.9-j0.3Ω

Table V: Results Example Load-Line Adjustment By Device Scaling.

$W1 = W4$	$W2 = W3$	$Zin,1 = Zin,4$	$Zin,2 = Zin,3$
293 μm	293 μm	23.6 + j0.5Ω	17.3 + j0.6Ω
293 μm	258 μm	21.9 + j0.1Ω	18.5 + j0. 15Ω

Notice here that the AC grounding results from the differential output. Without loss of generality, Figure 21 illustrates the half-circuit diagram of Figure 21. Different voltage levels can be noticed at nodes V_5 and V_x with respect to the virtual AC

ground. These differences in combination with the asymmetric values of interwinding capacitances create common mode voltages and unequal differential voltage swings.

A. Compensating Common-Mode Effect

In order to alleviate the impact of the common-mode effect, one can use the biasing connection at the center tap of the primary inductors. However the impact of this method is depending on the DAT topology and its contribution could be turn to be positive or negative. Furthermore one can adjust the transformer layout for a reduction of common mode effect. However these methods impose complex and iterative design procedure. To surmount the common mode effect, we propose the insertion of auxiliary components, e.g. capacitances and resistances, for equalization of node impedances. Employing mixed-mode parameters facilitates the determination of the common and differential components of each input port. A general analyzing procedure targeting zero common-mode voltages leads to a set of required conditions. As an example the required conditions in relation to Figure 21 (a) with use of Figure 21 can be formulated as:

$$Z_{cd11} + Z_{cd12} = 0, \; Z_{cd22} + Z_{cd21} = 0 \qquad (12)$$

In which $Z_{cd;ij}$ represents the differential to common impedance-parameters of the transformer. Employing the equivalent circuit, presented in Figure 21, enables the determination of the values and the location of auxiliary components. The result of this example is presented alongside another example regarding an implemented ring variant ([Ref *35*], Figure 21 (c)) in TSMC 65nm CMOS technology at table IV with the location of auxiliary components shown in Figure 21. In table IV ’U’ denotes the uncompensated node impedances and ’C’ denotes the compensated node impedances. For the latter example the RF voltages at nodes 3, 4 are shown in Figure 22 before (a) and after (b) compensation.

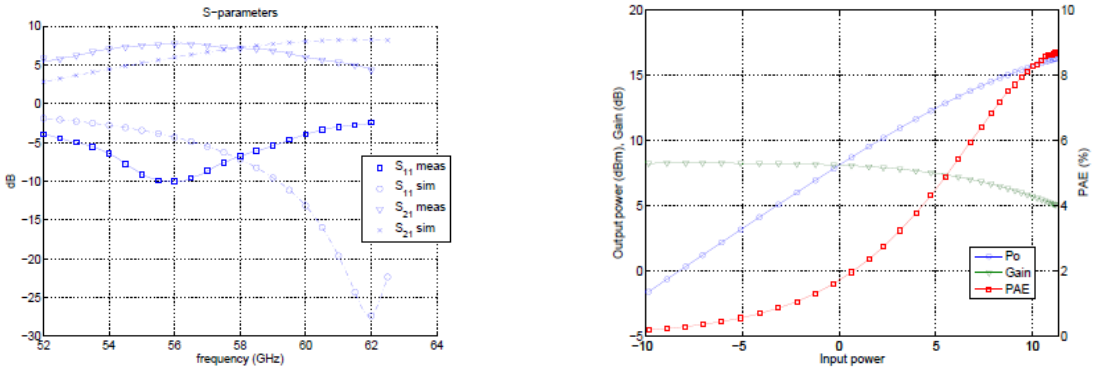


Figure 23: Left: S-parameters at Vdd=1.8V and Idc=178mA. Right: Output power, power gain and PAE at 60 GHz for Vdd=1.8V and Idc=178mA.

B. Compensating Unequal Differential Voltage-swings.

Assuming the negligible effect of common mode, one may compensate the inequality of voltage swings between different combining stages. This goal can be achieved by combining currents and voltages as is suggested in [Ref *32*]. However, this method complicates the design procedure for achievement of a higher output level where a larger trans-impedance ratio is necessary. In conventional amplifier design, the required relation between the voltage and current swing is dictated by the impedance value of the output termination. However the existing magnetic and capacitive coupling between different stages of DAT topology facilitates the implementation of a new approach. This property enables adjusting the voltage swing of one stage by means of altering the amplitude and phase of current flows at the other amplifier stages. Taking benefit of this distinguishing property, an equalization of the voltage swings can be achieved by consciously introduction of inequality in the physical dimension (e.g. width) of the implemented amplifiers which in turn alters the required loadlines for achievement of maximum output swing for each stage. Table V represents the optimized transistor sizes with resulting load-line values of the ring variant, mentioned in the previous section. After applying compensation the voltage swings become approximately equal.

7.2. Circuit Design

Due to the restriction on the layout size, a compact two stage inline alternating structure has been implemented in TSMC 45nm CMOS technology. Cascoded differential pair topology forms the core of the combining stages. These amplifiers are operating in Class A, providing maximum gain and linearity. Minimizing interconnection loss has been achieved by an appropriate arrangement of the transistors. Transistors' width of the first and the second combining stage are respectively 150¹m and 160¹m and they are biased according to the 0.29mA/um guideline for achievement of optimal linearity. Fulfilling the DC-electro-migration design rules has imposed a larger line-width of the primary (red) windings. An optimal transformer design has been carried out in

Table VI: Comparison With Reported Pas In Literature

Reference	Description	Gain	bandwidth 1dB/3dB (GHz)	Output power 1dB/sat (dBm)	PAE max (%)	Technology
[Ref 34]	3-stage DAT Cascode	26	55-71 / NA	14.5 / 18	12.2	90 nm
[Ref 37]	2-Stage Cascode	16	55-65 / NA	12.7 / 14.5	25	SOI 65 nm
[Ref 38]	3-Stage Differential CS	15.8	NA / 57-62	2.5 / 11.5	11	65 nm
[Ref 39]	3-stage DAT Cascode	15.5	NA / 53-68	11.5 / 18	3.6	65 nm
[Ref 40]	3-Stage CS	19	NA / 51-61	NA / 7.9	19.4	45 nm
[Ref 41]	2-Stage push pull	6	50-67 / NA	11 / 13.8	7	45 nm
[Ref 42]	2-Stage Single-ended Cascode	16	50-60 / 47-60	7.6 / 12	12.3	45 nm
[Ref 43]	2-Stage Differential Cascode	20	55-65 / NA	11.2 / 14.5	14.4	45 nm
This work	**1-stage DAT Differential Cascode**	**6**	53-59 / NA	**13.2 / 163**	**8.7**	**45 nm**

Momentum and it has lead to an achievement of 76% efficiency, primary inductors of 70pH and a secondary inductor of 157pH. A T-junction power divider delivers the required power level to each amplifier stage and has angles of 45º to reduce the length and losses. A pair of LC-matching networks together with the power divider transforms the 4.6-j8.7Ω amplifiers input impedances into 100Ω. The large ratio of the required trans-impedance matching networks reduces the overall bandwidth. This affect might be alleviated by adding pre-amplifiers which will raise the impedance level of the amplifier input ports. The required passive and distributed components have been designed in Agilent Momentum and in **Error! Reference source not found.** the chip photograph of the realized PA is shown with a core-size of 210µm x 270µm.

7.3. Measurement Results

Small-signal Measurements

On-wafer small signal measurements are carried out using a 67GHz Agilent PNA and Cascade Microtech infinity probes with integrated baluns with a supply voltage of 1.8V and atotal bias-current of 178mA. Figure 23 shows the simulated results alongside the measured results in which a maximum measured gain of 7.8dB can be observed at 56GHz. Noticeable is a discrepancy at peak and notch frequency of |S21| and |S11|, respectively. Measurement results reveal a 1dB-bandwidth of 5.5GHz (from 53.6 to 59.1 GHz).

Large-signal Measurements

Due the inaccuracy involved with the modeling of passive components, a small discrepancy has been observed between the simulated and the measured load-line terminations. A proper measurement of the output power level has then been carried out by employing a 60GHz Focus MPT load-pull system. Verification between the simulated and measured optimum load reflection coefficients reveal a discrepancy only in the phase component of 45º. The measured value of the 1dB compression output power at the reference plane directly after the transformers' output shows only a 0.7dB discrepancy between load-pull system and nominal 100- termination.

The large signal measurement has resulted in a 1dB compression point of 13.2dBm, a saturated power level of 16.3dBm and a maximum PAE of 8.7% which are illustrated in Figure 23. In the definition of the latter the power gain is taken into account. Employing 60GHz Agilent signal generator, 67GHz Agilent PNA and Agilent Spectrum Analyzer in combination with the 60GHz Focus MPT load-pull system has facilitated the realization of an accurate two tone measurement setup. The two tone measurement results reveal an 18.7dBm of OIP3 for a center frequency of 60.02GHz and a tone-spacing of 40MHz. Table VI summarizes the performance of the presented differential DAT power amplifier alongside the latest reported CMOS power amplifiers at 60GHz. This table shows that the presented work has a good output power level and a moderate efficiency in respect to the reported amplifiers.

8. CONCLUSION

The parasitic effects due to layout, which are more influential at high frequencies, are taken into account by performing automatic RC extraction and manual L extraction. The long signal lines are modeled with distributed RLC networks. The problem of substrate losses is addressed by using patterned ground shields in inductors and transmission lines. It is observed that accurate simulation of all these parasitic effects is sometimes very time consuming or even infeasible. For instance electromagnetic simulation of a transformer in the presence of all the dummy metals is beyond the computational capability of existing EM-simulators.

The on-wafer measurements on the 60GHz circuits designed in this work are performed using a waveguide-based measurement setup. The fixed waveguide structures, specially provided for the probe station, serve for the robustness of the setup as they circumvent the need for cables, which are by nature difficult to rigidify, in the vicinity of the probes. Taking advantage of magic- Ts, it is possible to measure differential mm-wave circuits with a two-port network analyzer rather than using a much more expensive four-port one. Noise, s-parameter, and phase noise measurements are performed using the mentioned setups.

However, in practice, we have succeed to realize different 60GHz corner blocks with excellent performance. These results have proven the capability of the main stream CMOS technology combined with proper and time consuming design procedure for the realization of 60GHz RF corner blocks.

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