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A Forward Body Bias Generator for Digital CMOS Circuits with Supply Voltage Scaling

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Abstract— We propose a new fully-integrated forward body bias (FBB) generator that holds its voltage constant relative to the (scalable) power supply of a digital IP. The generator is modular and can drive distinct digital IP block sizes in multiples of up to 1mm^2 . The design has been implemented in 90nm low-power CMOS. Our basic unit for driving digital IP blocks up to 1mm^2 occupies a silicon area of 0.03mm^2 only. The generator completes a 500mV FBB voltage step within $4\mu\text{s}$. The bandwidth of the design is 570kHz . The active current of the FBB generator alone is about $177\mu\text{A}$ for a nominal process, 1.2V supply and 85°C . The standby current is as low as 72nA at 27°C .

I. INTRODUCTION

Modern digital integrated circuits are sensitive to process variability that impacts circuit performance and power consumption. In recent years, post-silicon tuning has shown to be effective to counteract process variability, or to trade-off power-performance [1-2]. Well-known post-silicon tuning techniques are supply voltage scaling (VS) and body biasing (BB). VS is primarily used to reduce active power at the expense of a lower circuit performance [1]. BB is typically used for leakage reduction or performance tuning [1-2]. Two BB approaches exist, namely reverse body bias (RBB) and forward body bias (FBB). RBB increases the threshold voltage, (V_{th}) which lowers leakage at a gate delay penalty. Contrarily, FBB reduces V_{th} which lowers gate delay at a leakage cost. VS and BB can also be combined to achieve collective benefits [1].

The convergence of multiple applications into a single device drives integrated circuit solutions that are both high performance and power efficient. Post-silicon tuning techniques enable the definition of new operating modes, where each mode targets a different power-performance trade-off. Our focus is on the application of FBB for improving circuit performance. When a circuit is active, FBB is preferred over VS to enhance performance due to its lower dynamic power penalty. The joint use of FBB and VS is preferred over VS alone for achieving low-power operation. When a circuit is in standby, the leakage power is dominant and FBB should not be applied. This motivates the application of FBB dynamically at runtime [3].

FBB requires a voltage generator circuit to generate the required N-well and P-well bias, respectively. The trend towards higher integration densities in modern chips favors a fully integrated solution to enable more cost-effective system solutions. From an industrial perspective the generator should comply with the following requirements: *i)* It should be digitally controllable to simplify system integration. *ii)* The FBB voltage generation should be transparent to any voltage scaling approach, i.e., the amount of applied FBB should be constant relative to the supply voltage (V_{DD}) of the circuit. *iii)* The FBB generator should be powered off from the always-on nominal core supply. Finally, *iv)* a FBB generator should have low power consumption, and small area occupation.

Several FBB generators have been proposed in the literature, but none of them meet all of the aforementioned requirements. Tschanz et al. presented an adaptive body bias (ABB) voltage generator [2]. The main drawback of their implementation is that FBB is applied only to PMOS transistors to avoid the use of a triple well technology. Likewise, the FBB voltage is V_{DD} -dependent, as well as the need for a voltage level higher than V_{DD} . Choi and Shin proposed a more sophisticated solution for providing body bias voltages to multiple macros in the design [4]. However, their solution also requires voltage levels higher than the core V_{DD} and lower than V_{SS} , mainly for generating RBB, and also for this design, the FBB voltage is V_{DD} -dependent. Sumita et al. presented another ABB generator [5]. However, it has similar constraints as the one proposed in [4]. Komatsu et al. proposed a FBB generator for enabling self-adjusted FBB [6]. Their solution cannot dynamically control the FBB voltage, while the generated FBB voltage is highly sensitive to V_{DD} and strongly temperature dependent. Other publications imply using a FBB generator without discussing in detail its implementation [7-9].

In contrast to prior art, our solution can meet all of the aforementioned requirements.

The remaining of this paper is organized as follows. In Section 2 we introduce the proposed FBB generation concept. Section 3 presents the FBB generator design. Section 4 shows

Fig.3 shows the circuit diagram of the pre-driver. The input stage is implemented by a double input pair to cover the wide input voltage range as provided by the RDAC, especially when the digital IP has a voltage scalable supply. A cascoded gain stage is used to achieve high gain. The pre-driver can be turned-off by the ENB signal. In this case, the outputs $outp$ and $outn$, are clamped to V_{DD} and V_{SS} , respectively.

The expandable drive unit is implemented by a rail-to-rail class AB output stage, which can maintain a small current in steady state and that is able to offer a large current during a transient. Such output stage is very convenient for driving large capacitive loads due to its current source/sink capability. Fig.4 (left) shows a circuit diagram of a drive stage for providing the P-well bias to the digital IP. The output stage for providing the N-well bias is similar, except that the switches are connected to V_{DD} and V_{DDIP} , respectively. Circuit stability is accomplished using a Miller compensation scheme embedded in the output stage unit. When multiple drive units are used, output stages are placed in parallel which maintains the ratio between maximum load capacitance and Miller capacitance to be constant, thereby ensuring stability.

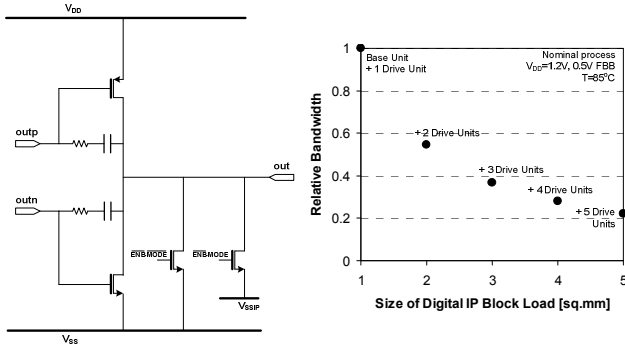


Figure 4. (left) Circuit Diagram of the P-well Output Stage of the Voltage Buffer, (right) Generator Bandwidth vs. Digital IP Block Dimension

The switches are indicated along with their control signals. The switches are used to clamp the output to fixed potentials when the voltage buffer is turned-off. This ensures that the digital IP block is always properly body biased.

Multiple output stages can be connected to the pre-driver. The number of output stages to be used depends on the size of the digital IP block. The pre-driver with one output stage is suitable for driving a digital IP block size of 1mm^2 . Two output stages can drive a digital IP block of up to 2mm^2 , etcetera. In this way we have created an expandable output stage, and offer a re-usable FBB generator solution to drive digital IP blocks of different sizes. The collection of one output stage for P-well and N-well is referred to as drive unit. Fig.4 (right) shows the relative bandwidth of the generator as function of the digital IP block dimension and number of drive units. Observe that the bandwidth reduces for larger digital IP block that require more drive units.

IV. CIRCUIT LAYOUT

Fig.5 shows the layout of the proposed FBB generator design in 90nm low-power CMOS technology. The base unit contains the reference circuit, the RDAC and decoders, and the pre-driver. The drive unit is connected to the base unit by

abutment. The total area of the base unit and drive unit is $250\mu\text{m}$ by $125\mu\text{m}$. The reference circuit, RDAC and decoders, pre-driver and output stage consume 24%, 30%, 14%, and 32% of the total area, respectively. The area of the drive unit alone is $80\mu\text{m}$ by $125\mu\text{m}$. Additional drive units can be connected to each other by abutment. Alternatively, they can be spatially distributed in the overall chip layout while hooked up to the base unit.

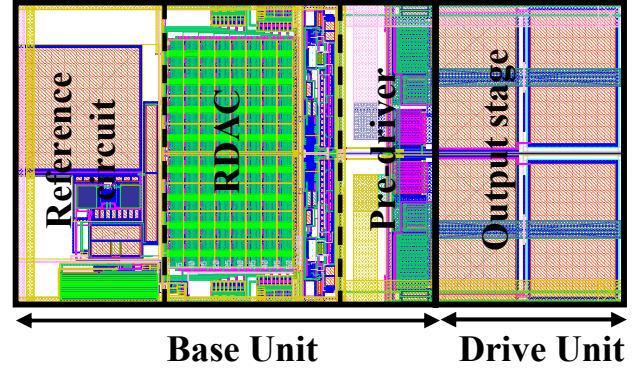


Figure 5. Layout of the FBB Generator

V. CIRCUIT SIMULATION RESULTS

Spectre circuit simulations have been performed for the base unit with a single drive unit while driving a digital IP block of 1mm^2 . Such digital IP block contains approximately 300K equivalent gates. The total well capacitance and current for both N-well and P-well has been extracted as function of FBB, and process-voltage-temperature conditions. We account for contributions from transistors and junction diodes. For a 1mm^2 digital IP block, we obtained $C_{Lpw}=1\text{nF}$, $C_{Lmw}=1.8\text{nF}$, $I_{Lpw}=3.5\text{mA}$, and $I_{Lmw}=-2\text{mA}$ at 0.5V FBB. The respective process and operation conditions are: nominal process, $V_{DDIP}=1.2\text{V}$, and $T=85^\circ\text{C}$. Table 1 summarizes the main design characteristics of the FBB generator.

TABLE I. FBB GENERATOR DESIGN CHARACTERISTICS NOM.PROCESS, $V_{DD}=1.2\text{V}$, $T=85^\circ\text{C}$, 1MM^2 DIGITAL IP BLOCK AS LOAD

| Parameter | Unit | Base Unit + 1 Drive Unit |
|--------------------------|-------------------------|--------------------------|
| Circuit area | mm^2 | 0.03 |
| $I_{dd}^{(1)}$ | μA | 177 |
| I_{ddq} | nA | 356 (72@27°C) |
| Bandwidth ⁽²⁾ | kHz | 570 |
| Slew rate – P-well Rise | $\text{mV}/\mu\text{s}$ | 235 |
| Slew rate – N-well Rise | $\text{mV}/\mu\text{s}$ | 256 |
| Slew rate – P-well Fall | $\text{mV}/\mu\text{s}$ | 138 |
| Slew rate – N-well Fall | $\text{mV}/\mu\text{s}$ | 152 |

⁽¹⁾ I_{dd} at nominal BB, ⁽²⁾ Bandwidth at 0.5V FBB

Observe that the circuit area of the FBB generator is only a small fraction ($\sim 3\%$) of the digital IP block area. The considered configuration consumes about $177\mu\text{A}$ in active mode. In standby, it leaks about 72nA . Every additional drive unit increases the active and standby current by about $90\mu\text{A}$ and 54nA , respectively. The FBB generator has a bandwidth of 570kHz and a worst case slew rate of $132\text{mV}/\mu\text{s}$. From a

digital systems perspective, the FBB bandwidth can be interpreted as to how often can the IP block change its FBB voltage, while the slew rate indicates how fast is the FBB voltage available. This makes the circuit suitable for both dynamic and adaptive body biasing applications.

Fig.6 shows the simulation traces of the N-well and P-well voltage for the same conditions as before.

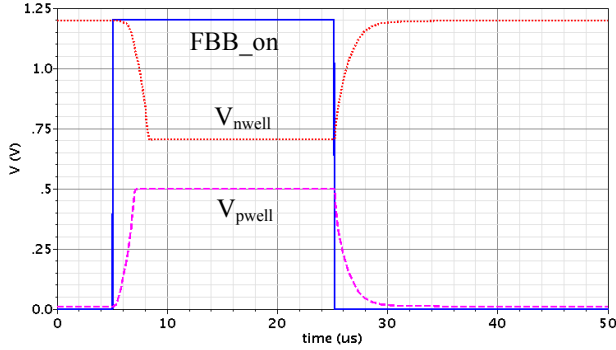


Figure 6. Transient Response of the FBB Generator to Generate a 0.5V FBB for both NMOS and PMOS Devices in a 1mm² Digital IP Block

Fig.7 demonstrates the operation of the FBB voltage generator along with a digital IP with voltage scaling (i.e. V_{DDIP} =scaled, $V_{SSIP}=V_{SS}$). In this example, the voltage scaling starts shortly after the FBB voltage generator is enabled at $t=5\mu s$. Observe that the N-well voltage follows V_{DDIP} to maintain 0.2V FBB when reducing V_{DDIP} from 1.2V down to 0.8V. This shows that the proposed voltage generator is suitable for use in power-managed digital circuit designs.

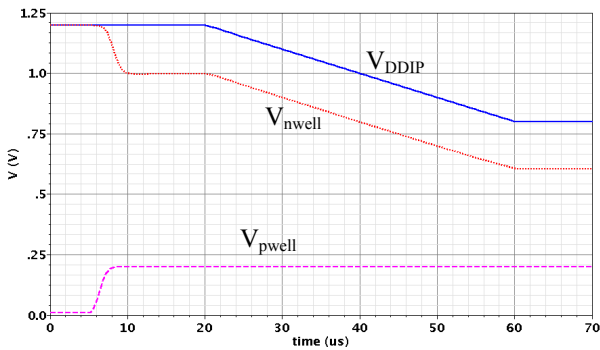


Figure 7. Application of the FBB Generator in Conjunction with a Digital IP Block with Voltage Scaling Enabled

The magnitude of the well currents depends on the size of the digital IP block under control and the temperature. We have analyzed the dependence between N-well/P-well voltage and N-well/P-well current. For this purpose, we have used the base unit with one drive unit for FBB generation. Fig.8 plots the obtained well voltages and current trends. This indicates the operational range of the FBB generator. Observe that both N-well and P-well voltages remain constant at 0.5V for well currents up to about 10mA. Such well currents are about 3x and 5x larger than the expected maximum P-well and N-well current for a 1mm² digital IP block, respectively (P-well: 3.5mA and N-well: -2mA at 85°C).

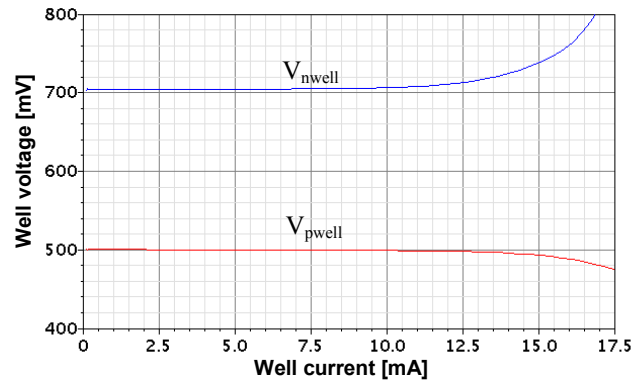


Figure 8. FBB Generator Load Regulation at 0.5V FBB for nominal process conditions, $V_{DD}=V_{DDIP}=1.2V$, $V_{SS}=V_{SSIP}=0V$, and $T=85^{\circ}C$

VI. CONCLUSION

In this paper we proposed a new fully-integrated forward body bias (FBB) generator that holds its voltage constant relative to the (scalable) power supply of a digital IP. The generator is modular and can drive distinct digital IP block sizes in multiples of up to 1mm².

The design has been implemented in 90nm low-power CMOS. Our basic unit for driving digital IP blocks up to 1mm² occupies a silicon area of 0.03mm². The generator completes a 500mV FBB voltage step within 4 μs . The bandwidth of the design is 570kHz. Finally, the active current is about 177 μA for a nominal process, 1.2V supply and 85°C. The standby current is as low as 72nA at 27°C.

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