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A Ka Band, Static, MCML Frequency Divider, in Standard 90nm-CMOS LP for 60 GHz Applications

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Abstract — This paper presents a broadband, static, 2:1 frequency divider in a bulk 90nm CMOS LP (low-power) technology with maximum operating frequency of 35.5 GHz. The divider exhibits an enhanced input sensitivity, below 0 dBm, over a broad input range of 31 GHz and consumes 24mA from a 1.2 V supply. The phase noise of the divider is -124.6 dBc/Hz at 1 MHz offset from the carrier.

Index Terms — CMOS integrated circuits, Current mode logic, Frequency conversion, Millimeter wave circuits, Phase locked loops.

I. INTRODUCTION

The ongoing research and development in the 60 GHz band has paved way for investigation of various possible transceiver architectures. Fig.1 shows a typical receiver architecture, which relies on sub-harmonic mixers and a 30 GHz phase locked loop. In such a tuning system the first stage of the frequency divider is a critical component due to requirements of high frequency, wide bandwidth and high input sensitivity.

The commonly used high frequency divider architectures are static, Miller and injection locked. Although, the latter two configurations can achieve high frequencies with low power consumption [5]-[6], they are inherently narrow band. Thus, they are not entirely

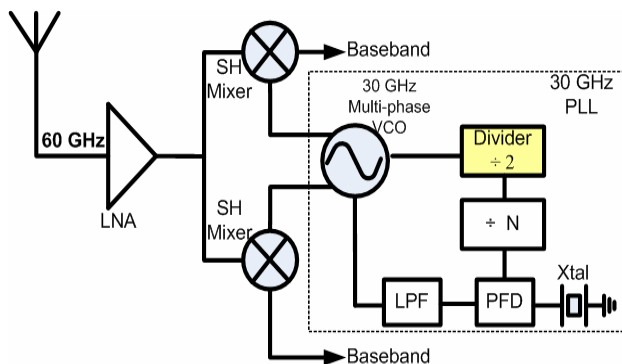


Fig. 1. Architecture of a 60 GHz receiver

suitable for the 7 GHz bandwidth required worldwide for the 60 GHz band. In comparison, static frequency dividers are broadband but consume more power. Another advantage of static dividers is the availability of highly matched quadrature outputs. The static frequency divider reported in [1] achieves a maximum operation frequency of 27 GHz in 120nm CMOS whereas dividers in [2], [3], [7] have been implemented in SOI technologies. They provide improved high frequency performance, however, CMOS SOI is not the mainstream technology choice. In this paper we present an improved static frequency divider with broadband operation. It is implemented in a bulk CMOS 90nm LP technology suitable for low-power, digital applications. As a key enabling component, a compact, stacked inductor is used in the latch and output buffers. The output buffers, based on f_T doublers are included for measurement purposes.

II. CIRCUIT DESIGN

The block diagram of a conventional 2:1 static frequency divider is shown in Fig.2. It consists of two cascaded (master and slave) D-latches. The D-latches are driven by anti-phase clock pulses and the dividing operation is achieved by connecting the inverted slave outputs to master D-latch inputs. Each D-latch is based on MOS current mode logic (MCML) and consists of data

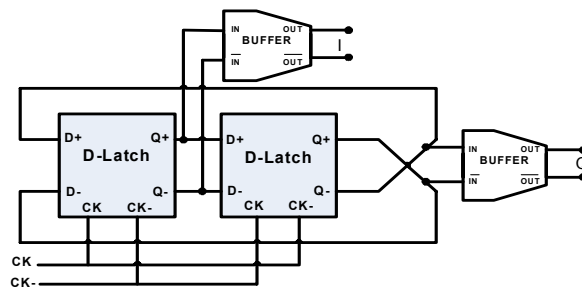


Fig. 2. Static frequency divider with output buffers

transistors: M1, M2 and latch transistors: M3, M4 as shown in Fig.3. The MCML logic is characterized by small voltage swings, thus high switching speed, constant power consumption and noise immunity due to complete differential architecture.

The maximum operating frequency of the divider depends on the speed of CML latches, which in turn is limited by technology, parasitic capacitances of devices and the layout parasitics. In this paper, effect of the latter two has been minimized by circuit optimization of the D-latch and optimal layout of the divider.

In comparison with earlier published designs [1]-[4], which employ similar dimensions for the data and latch transistors, this design has different dimensions for the same, as shown in Fig.3. The positive feedback between M3 and M4 implies that only a small current is required by the latch part to take a hard decision between high and low level of the output. Parametric simulations reveal that the optimum width of transistors M3 and M4 is 5/8 times the width of M1 (or M2). In addition, smaller latch transistors offer less parasitic capacitances at the output nodes of M1 and M2 and thus enhance the switching speed of charge transfer between them.

As the latch transistors do not require the same current as the data transistors, selecting different dimensions for transistors M6 and M7 controls the current distribution. The latter transistor is added to maintain the differential structure for the clock inputs and avoid any imbalance. The current consumption in the data and latch transistors is 12mA and 9 mA respectively. The optimal dimensions for transistor M6 and M7 are shown in Fig.3. The shunt peaking inductor L1, in series with resistor R_L, is included for broadband operation.

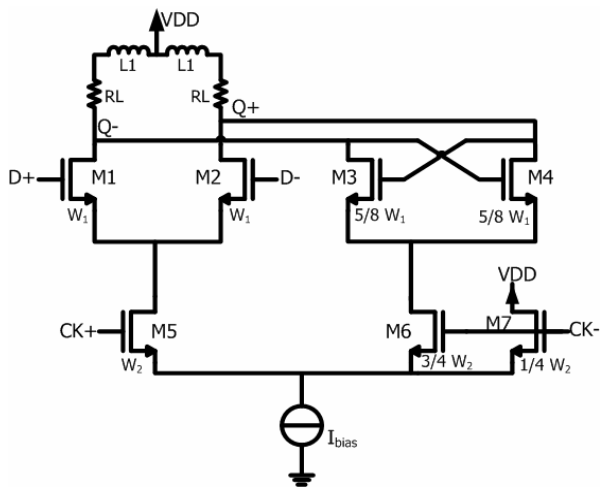


Fig. 3. Proposed D-Latch Circuit schematic

A. Stacked Inductor design

The shunt peaking inductor (L1) is implemented in a differential structure with the center point connected to VDD and has a value of 125pH. A high quality factor (Q) is not required as the load resistor connected in series with the inductor determines the effective Q. Therefore, the area of the inductor is minimized by realizing it as a stacked inductor (Fig.4) by using the top four-metallization layers. Metal 1 is used as a fish bone structure below the inductor for better isolation.

Compared to planar inductors, this structure offers less (up to 45%) parasitic capacitance. Two consecutive layers (e.g. M6 and M5) are displaced by one metal width by which, the parasitic capacitance is present only between even layers (M6, M4) and odd layers (M5, M3). The metal to substrate capacitance is also limited to M3. Assuming the metal lengths of each half turn of the inductor as l_1, l_2, \dots, l_{2n} , the metal width as W , metal to metal overlap capacitance as $C_{m-m}(k)$ and metal to substrate capacitance as $C_{m-s}(k)$ the total parasitic capacitance is estimated by the distributed capacitance model using (1) and (2).

$$d_k = \frac{\sum_{i=1}^k l_i}{2n} \quad (1)$$

$$C_{total} \approx \frac{1}{4} \sum_{k=n}^{n+1} C_{m-s}(k) \cdot l_k \cdot W \cdot (2 - d_k - d_{k-1})^2 + \frac{1}{4} \sum_{k=1}^{n-2} C_{m-m}(k) \cdot l_k \cdot W \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 + \frac{1}{4} \sum_{k=n+1}^{2n-2} C_{m-m}(k) \cdot l_k \cdot W \cdot (d_{k+2} - d_k + d_{k+1} - d_{k-1})^2 \quad (2)$$

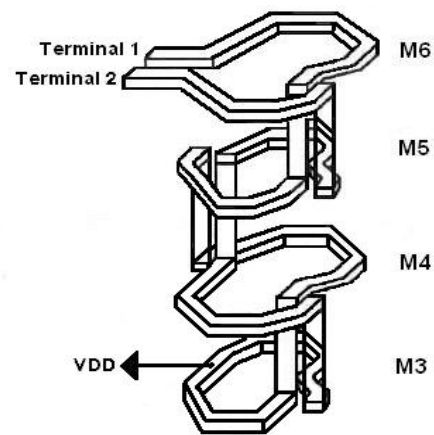


Fig. 4. Stacked inductor structure used for shunt peaking

B. Output Buffer

In many cases, output buffers excessively load the critical circuits, degrading their performance. This is true in case of a frequency divider, thus, the design of the output buffer attempts to minimize capacitive loading at the output nodes of the latches. It consists of a differential stage, modified into a f_T doubler stage by adding transistors M2 and M3 as shown in Fig.5. This setup approximately halves the C_{gs} capacitance as compared to a standard differential stage (keeping transconductance constant) and also increases the unity-gain bandwidth of the buffer. The compact shunt peaking inductor designed for the D-latch is re-used in the buffer without significant increase in area.

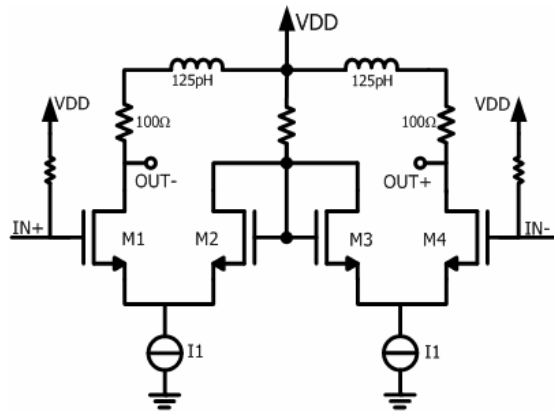


Fig. 5. Output buffer circuit schematic

III. LAYOUT AND TECHNOLOGY

A differential design is adopted both in the D-latch and output buffers; the layout is kept as symmetric as possible. The quadrature outputs use 50 transmission lines to the bond pads. Four RF output and two RF input pads are included for measurements. The circuit was fabricated in a 90nm, bulk, CMOS, LP technology, with six metallization layers. The transistors in this technology have a measured f_T and f_{max} of 107 GHz and 280 GHz respectively. Due to bond pad limitations the chip area is 0.9 x 0.7 mm. However, the active area is less than half of the above value. The chip micrograph is shown in Fig.6.

IV. MEASUREMENT RESULTS

The divider was measured on wafer with high frequency differential probes (GSGSG). A 180° hybrid coupler provides the required anti-phase clock inputs. The measured input sensitivity as a function of frequency is shown in Fig.7. The highest input sensitivity is measured

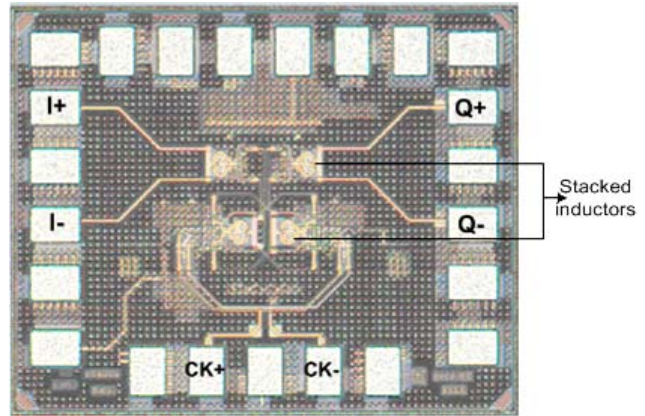


Fig. 6. Chip micrograph

at 24 GHz and the maximum operating frequency of the divider is 35.5GHz. The maximum frequency division is achieved at a power consumption of 14.4 mW per D-latch from a 1.2 V power supply. Each output buffer consumes 9.6 mW and the total power consumption is 48 mW.

The measured output spectrum at maximum frequency of operation is shown in Fig. 8. The output power of -40 dBm includes the losses from the cables and the 180° hybrid coupler (almost 30dB). Phase noise of the divider is a key performance parameter if it is to be integrated in a phase locked loop. The measured phase noise of the divider output (see Fig.9) is -124.6dBc/Hz at 1 MHz offset from the carrier (for an input CLK of 30 GHz). The input phase noise of the generator is -119.4dBc/Hz at double frequency and same carrier power.

Table 1 shows a comparison between some recently published, static frequency dividers. The presented divider exhibits a wider operating frequency range as compared to

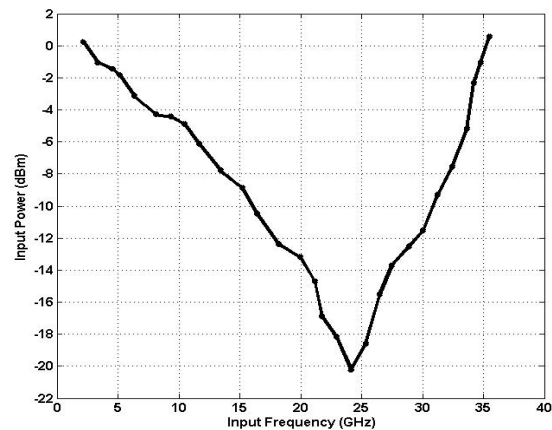


Fig. 7. Measured input sensitivity of the frequency divider

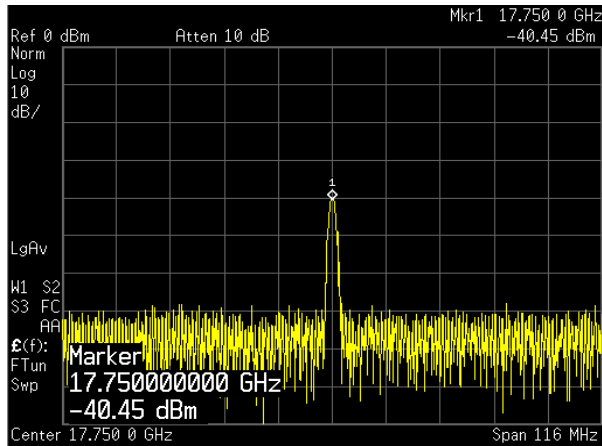


Fig. 8. Measured output spectrum for a 35.5 GHz input clock

SOI implementations in [2], [7] and lesser power consumption (excluding output buffers) than [1], [2], [3] and [7]. The improvement is a consequence of circuit optimization of the D-latch, the stacked inductor approach and the new output buffer implementation.

V. CONCLUSION

We have presented an improved Ka band, static frequency divider in a standard 90nm CMOS LP technology. A stacked inductor improves the maximum toggle frequency. Compared to planar inductors, this structure offers less (up to 45%) parasitic capacitance and is very compact. The highest input sensitivity is measured at 24 GHz and the maximum operating frequency of the divider is 35.5GHz. The maximum frequency division is achieved at a power consumption of 14.4 mW per D-latch from a 1.2 V power supply. Each output buffer consumes 9.6 mW and the total power consumption is 48 mW.

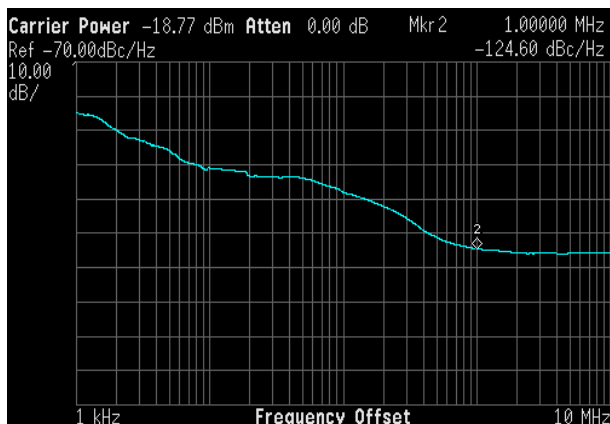


Fig. 9. Measured phase noise of the frequency divider

TABLE I
COMPARISON WITH PUBLISHED RESULTS

	Operating Freq Range (GHz)	Power Cons. (mW)	Freq. Range Below 0-dBm (GHz)	Phase Noise @1MHz (dBc/Hz)
[1] 120nm CMOS	2-27	30	24	N/A
[2] 0.12μm CMOS SOI	4-33	44.2	29	N/A
[4] 0.12μm CMOS	1-25	22.5	6	N/A
[3] 90 nm CMOS SOI	5-66	51	54	-102
[7] 90nm CMOS SOI	13-34	60	19	-127
This work 90nm CMOS	2-35.5	28.8	31	-124.6

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