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The fabrication of InP-based Photonic Integrated Circuits (PICs) is a complex process. The process used in the COBRA cleanroom in Eindhoven consists of 13 deposition, 10 lithography, 14 dry- and 7 wet-etching steps. Together with the intermediate cleaning, preparation and inspection procedures, the total process flow consists of 243 steps. In this paper we show how we created a robust modular process flow that can be used for a large variety of active- and passive circuits. These circuits can be fabricated together in multi-project wafer runs, allowing a drastic reduction of the fabrication costs making even small-volume production economically feasible.

Introduction

The Indium-Phosphide (InP) material system has a long history in photonic integrated circuits. Traditionally it was used for making telecom laser diodes, but it's potential for making more complex photonic integrated circuits was already explored in the 90's. The benefit of being able to integrate both active (lasers, amplifiers) and passive (waveguides, electro-optic phase shifters) components on a single chip still remains the best argument for choosing the InP platform for the fabrication of complex integrated circuits.

To create these circuits the fabrication process is much more complex than for the creation of single laser devices. The fabrication process must be capable of producing high performance amplifiers and lasers, but also needs to facilitate a large variety of passive waveguide circuitry (filters, splitters, phase modulators and reflectors). Because it is not feasible to develop a custom fabrication process for each circuit, we have developed what we call a *generic integration technology*, in which it is possible to realize a large variety of different components on a single chip using standardized building blocks[1].

Different waveguide types

The *generic integration technology* allows the designer to build basic active and passive components using both shallowly etched waveguides (for low loss interconnects and efficient amplifiers), deeply etched waveguides (for smaller bend radii and efficient phase shifter sections) and extra-deep etched waveguides (for broadband reflectors). A cross-section of the different basic waveguide types is shown in Fig. 1. The 500 nm thick waveguide layer consists of an InGaAsP quaternary layer with a bandgap wavelength of 1.25 μm (Q1.25). This layer is transparent for photons with a longer wavelength than 1.25 μm and those waveguides are therefore called passive. The active waveguides have either a bulk Q1.55, a Multi Quantum Well (MQW) or a Quantum Dot (QD) layer inside the waveguide layer. This active layer will either absorb or amplify

(depending on the applied electrical current) photons with a wavelength around 1.55 μm.
The highly doped InGaAs contact layer on top of the waveguides allows for efficient current injection in the active components (SOA) and is also used to operate the reverse-bias phase-shifting components. For the pure passive waveguides, however, this contact layer causes extra losses and should therefore be removed in the passive waveguides that don't require phase shifting. Furthermore, the conducting top cladding can also cause electrical problems when for example a forward biased amplifier is connected to a reverse biased phase shifter. Therefore we also offer an isolation waveguide, in which the highly doped part of the top cladding is removed.

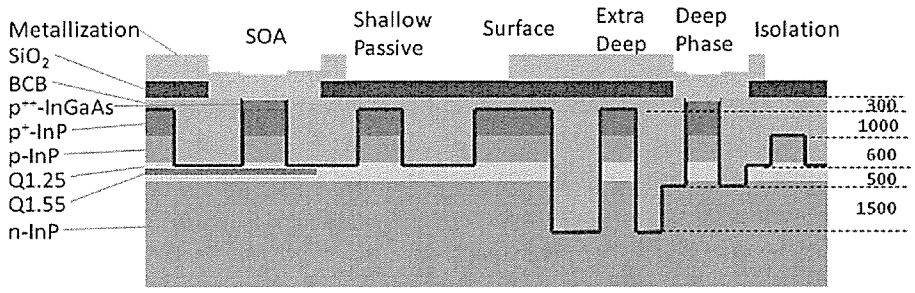

Figure 1: Schematic cross-section of the different waveguide types. The numbers on the right indicate the height difference in nm of the different etch levels.

Active-passive integration technology

To realize the integration of both the active and passive layer stacks a robust integration technology is required. An overview of the different available technologies is given in [2]. The butt-joint re-growth technology that we use requires about 40 processing steps of which most are used for cleaning the wafer before and after the lithography process that defines the active areas.

Stripping & cleaning

During the processing, a clean surface is very important. The best way of cleaning a wafer is by (selectively) etching away a small layer from the top by some chemical solution. In case of a freshly grown wafer, an especially for this purpose grown InP sacrificial layer can be removed by HCl etching. Further on in the process, a common way of removing any organic material is by O_2 plasma treatment (stripping). This also oxidizes the surface of the InP. This oxide layer can then be removed by diluted phosphoric acid (H_3PO_4:H_2O) (cleaning). This stripping and cleaning step removes approximately 2 nm of InP/InGaAsP material per cycle. Sometimes also a diluted HF dip is used to remove any silicon-like residues. These stripping and cleaning steps account for 70 of the 243 steps (29%) of the total fabrication cycle.

Waveguide lithography

To be able to connect the different waveguide types without very strict lithography alignment requirements, we first define the waveguide mask pattern in a 600 nm thick SiN hard mask layer by contact lithography and dry etching. It is important that this hard mask layer can withstand all the consecutive etching and cleaning steps, without

compromising the mask width and smoothness, hence the choice of material and the thickness of this layer.
The major part of the mask is defined by optical lithography, but some critical features, such as small DBR gap reflectors, may also be written by electron beam lithography. To combine these two lithography steps, a thin chromium layer is used as an intermediate mask layer in which the e-beam and waveguide patterns are transferred first, and then serves as an etching mask when transferring the whole pattern to the SiN layer afterwards. An example of such a process is shown in Fig. 2 [3]. By this time we have done 74 out of 243 steps.

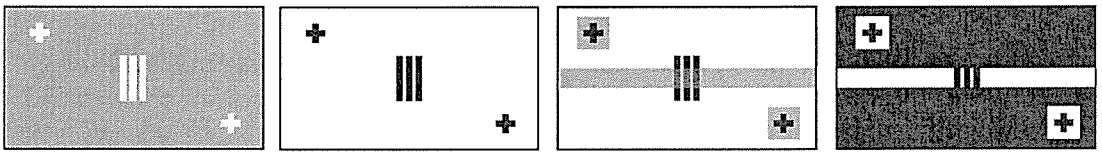

Figure 2: Lithography process. First, the DBRs are written by e-beam lithography (a), then the DBR pattern is etched into the chromium mask (b), then the waveguides are defined by optical lithography (c), and are also etched into the chromium mask (d).

Waveguide etching

When the waveguide mask is defined we can start etching the different waveguide shapes into the InP/InGaAsP layers. However, etching each different waveguide type directly to the final etch depth would require a very accurate alignment of the lithography steps defining the different waveguide types. Instead, we use a series of photo-lithography and etching steps in which we only etch the depth-difference between the different waveuigde shapes.
The first etch step (extra deep waveguides) is performed in an Inductively Coupled Plasma (ICP) system using a Cl_2:Ar:H_2 chemistry. This chemistry gives very smooth and straight sidewalls and has a high etch rate (>1 μm/min). Additionally, with this process we are able to etch narrow trenches (< 750 nm) without significant lag effect (reduction of etch depth in narrow openings) and is therefore very suitable for making high contrast DBR mirrors [3]. A downside of this etching chemistry is that the etch depth cannot be controlled very accurately
After the extra-deep areas are etched, the areas that need to end up at the normal deep etch depth (100 nm below the waveguide film) are etched (500 nm). In the 3rd etch step, the whole wafer is open and etched to a depth equal to the difference between the shallow etch depth and the isolation waveguide top edge (600nm). Before the 4th InP etch step, the SiN waveguide mask is removed on the isolation waveguides. When the mask is selectively removed, the whole wafer is etched 1000 nm, which is the difference between the top of the isolation waveguides and the top of the passive waveguides without contact layer. The same process is repeated for the removal of the contact layer from the passive waveguides and then the wafer is etched another 300 nm (5th and final InP etch step) to the final depth.
In contrast to the first InP etch step, steps 2-5 are performed using a CH_4:H_2 chemistry. In this process, the etch rate is much more controlled at about 100 nm/min for InP and about 80 nm/min for quaternary and ternary materials. This allows us to etch very

accurately to a certain depth. This is especially important for the shallow waveguides which should be etched to about 100 nm in the waveguide film.
After all these etching, lithography, and cleaning steps we have now arrived at fabrication step 163 out of 243.

Planarization

In order to make the alignment of the metallization structures less critical, we use a planarization scheme that allows us to contact the waveguides with very tolerant alignment. First we deposit a thin SiO_2 layer by PECVD to improve the adhesion of the planarizing polymer to the InP. We deposit a polymer, benzo-cyclobuthene (BCB), by spin coating and thermal curing. After that, the BCB layer is etched back gradually until the top of the highest waveguides (those with the contact layer still present) are just sticking out of the surface. Subsequently, another SiO_2 layer is deposited to assist in the adhesion of the metallization to the BCB. The contacts are then opened by another litho and etching process. This is now step 189 of 243.

Metallization

The Ti/Pt/Au (60/75/300 nm thick) contacts are realized using a lithography and lift-off process. Again, this lithography step does not require very accurate alignment, since only the waveguides with contact layer are sticking out of the BCB. The backside of the wafer gets the same metallization layer stack and the wafer is annealed at 325 °C for 90s.
If the circuit has components that require high and uniform current injection, a thicker metallization layer might be required. It is then possible to increase the gold thickness to about 1.5 μm by an electroplating process. This process involves first the sputtering of a thin Au seed layer, then a lithography pattern definition, followed by the electroplating process and the removal of the photoresist and etching back of the seed layer.
After the plating process we finally arrive at step nr. 243 and the wafer is ready to be cleaved and characterized.

Conclusion

In this paper we presented a fabrication process in which a large variety of integrated circuits can be realized. The process consists of 13 deposition, 10 lithography, 14 dry- and 7 wet-etching steps, and a lot of cleaning, surface preparation, baking and inspection steps. Although such a complicated process is difficult to develop, once such a process is set up, the fine-tuning cost that is required to get to a robust process with high yield can be shared over all users of the fabrication platform. It is therefore the ideal platform for the prototyping and small volume (pilot) production of complex PICs in InP.

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