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High-Performance InP-Based Photodetector in an Amplifier Layer Stack on Semi-Insulating Substrate

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Abstract—A waveguide photodetector (PD) based on semi-insulating (SI) indium phosphide (InP) was simulated, designed, and fabricated. The layer stack for this PD was optimized for use as an optical amplifier or laser and it can be combined with the passive components. By using an SI substrate and deep etching, a small, efficient, and high-speed PD was made, which allows for easy integration of source, detector, and passive optical components on a single chip. A 3-dB bandwidth of 35 GHz and 0.25 A/W external radio-frequency reponsivity is measured at 1.55-μm wavelength for a 1.5-μm-wide and 30-μm-long waveguide PD at -4-V bias voltage. The polarization dependence in the responsivity is less than 0.27 dB.

Index Terms—Photodetector (PD), semi-insulating (SI), semiconductor optical amplifier (SOA).

Fig. 1. (left) Active–passive butt-joint layerstack with specifications based on an SI substrate. The unit for the doping level is cm^{-3}. (right) Top view of the fabricated PD.

I. INTRODUCTION

MONOLITHIC integration of different optical building blocks, such as passive waveguide devices (PWDs), semiconductor optical amplifiers (SOAs), photodetectors (PDs), and modulators allows for flexible design of photonic integrated circuits. Previously, we reported on devices based on a combination of PWDs and SOAs, such as multiwavelength ring lasers [1] and mode-locked lasers [2]. This letter focuses on the performance of PDs fabricated in the SOA layer stack and operated by reversely biasing the pn-junction.

Others have presented PDs with increased sensitivity by monolithic integration of a waveguide PD and an SOA in a common layer stack [3]–[5]. In [3], a PD based on bulk material has achieved 20-GHz bandwidth, and in [5] the PD was based on multiquantum-well and achieved 40-Gb/s operation. However, the latter PD is highly polarization-dependent.

In this letter, we present a 35-GHz PD in a bulk SOA layer stack with smaller than 0.27-dB polarization dependence in the responsivity. The active–passive layer stack used for these PDs is shown in Fig. 1. The film layer thickness of the waveguide is 500 nm, both in the absorbing region and in the transparent region, in order to obtain single-mode operation in the transversal direction. The confinement factor multiplied by the material gain coefficient of the SOA/laser based on this layer stack is
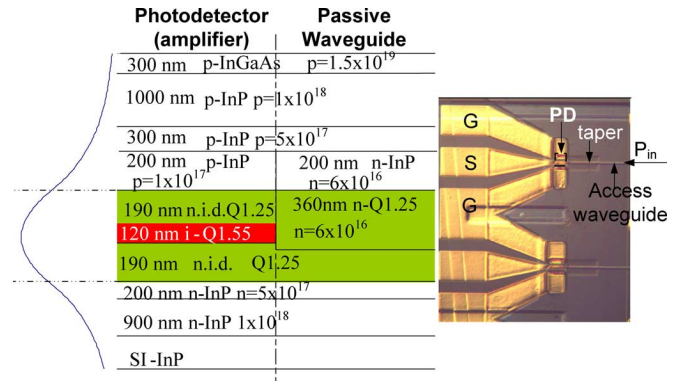
1.12×10^{-20} m^2 and the threshold current density is about 3 kA/cm^2 with cleaved facets at room temperature. One example which monolithically integrates a passive component (a wavelength duplexer), an SOA, and a PD based on this layer stack is the reflective transceiver [6]. It had a 750-μm-long SOA and achieved 5-dB fiber–fiber gain with 100 mA at the gain peak at 1530 nm. The bandwidth of the PD was limited to 14 GHz due to the N-substrate and the bonding wire. To obtain a higher radio-frequency (RF) bandwidth, a semi-insulating (SI) substrate was used to reduce the RF loss and the parasitic capacitance. To futher minimize the capacitance, this PD is small and etched through the film until the highly doped N–InP layer. The fabrication technology is completely compatible with the SOA/laser and the passive components. The measurement results show that a 30-μm (80 μm)-long, 1.5-μm-wide deeply etched PD can operate up to 35 GHz (28 GHz) with external RF responsivity up to 0.25 A/W (0.35 A/W) at a wavelength of 1.55 μm. The polarization dependence in the responsivity is less than 0.27 dB (0.2 dB).

II. SIMULATION

To estimate achievable bandwidth based on this layer stack, we calculate the transit time bandwidth (f_{tr}), the resistive–capacitive (RC) time (f_{RC}), and the total bandwidth (f_{total}) as a function of the waveguide width and length. The parameters and the equations for calculating the bandwidths and the series resistance of the waveguide PD with different size are given in Table I. The calculated f_{tr} for these PDs is 40 GHz. The parasitic capacitance C_p is about 12 fF extracted from the experiments. The simulated RC time bandwidth for different widths and lengths is shown in Fig. 2(left). The total bandwidth is primarily limited by the transit time for a 30-μm-long below 2-μm-wide device. The RC bandwidth is

TABLE I
EQUATIONS AND THE PARAMETERS USED FOR THE CALCULATION

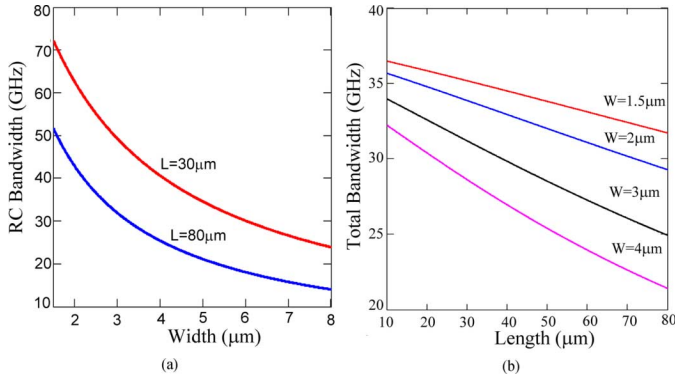| Equations	Parameters	Values
$f_{tr} \approx \frac{3.5 \cdot v_{tr}}{d_{dep}}$	v_e and v_h: electron and hole velocity	v_e: 6.0×10^6 cm/s, under high electric field
$\frac{1}{v_{tr}^4} = \frac{1}{2}\left(\frac{1}{v_e^4} + \frac{1}{v_h^4}\right)$	d_{dep}: depletion layer thickness	v_h: 4.0×10^6 cm/s, under high electric field
$f_{RC} =$	ε_r: relative permittivity	d_{dep}: calculated about 550 nm when the PD
$\frac{1}{2\pi((R_L+R_s)C_d+C_p R_L)}$	A: area of the junction	under -4 V bias voltage.
$\frac{1}{f_{total}^2} = \frac{1}{f_{tr}^2} + \frac{1}{f_{RC}^2}$	L and W: length and width of the device	ε: 13
$C_d = \frac{\varepsilon_0 \varepsilon \cdot A}{d_{dep}}$	μ_e and μ_h: electron and hole mobility	μ_h: 75 cm^2/s[7] in 1×10^{18}cm^{-3} p-InP
	R_p and R_n: p- and n-layer sheet resistance	μ_e: 1500 cm^2/s[7] in 1×10^{18}cm^{-3} n-InP
$R_{p,n} = \frac{d_{p,n}}{e\mu_h N_{p,d} W \cdot L}$	d_p and d_n: p- and n- layer thickness in the ridge	W_{gap}: 10 μm
$R_{gn} = \frac{W_{gap}}{e\mu_e N_d d_{gn} \cdot L}$	N_p and N_d: doping level of p- and n-InP	W_{c_p} equal to W for p-contact and W_{c_n} is
$R_{c_{p,n}} = \frac{\rho_{c_{p,n}}}{W_{c_{p,n}} \cdot L}$	R_{gn}: resistance from the ridge to n-contact within n-InP layer.	50 μm wide for n-contact
$R_{total} =$	W_{gap}: distance from the middle of the ridge to n-contact	ρ_c: measured 5×10^{-6} $\Omega \cdot$cm^2 for
$R_p + R_n + (R_{gn} + R_{cn})/2 + R_{cp}$	d_{gn}: the thickness of the unetched slab n-InP.	1.5×10^{19}cm^{-3} p-InGaAs contact and
	$R_{c_{p,n}}$: contact resistance between the metal and	1.0×10^{-3} $\Omega \cdot$cm^2 for 1×10^{18}cm^{-3} n-InP
	semiconductor material p-InGaAs and n-InP.	contact with 25 nm/75 nm/250 nm Ti/Pt/Au.
	ρ_c: resistance of the contact for p-InGaAs and n-InP.	R_L: 50 Ω load
	W_{c_p} and W_{c_n}: width of the contact	

Fig. 2. Simulated RC bandwidth (left) and the total bandwidth (right) based on the transit time and the RC time constant for PDs with different widths and lengths. The depletion layer thickness is calculated to be 550 nm under -4 V.

Fig. 3. Cross section of the PD and the corresponding resistance and capacitance in the PD.

the limiting factor for a device wider than 4 μm. The simulated total bandwidth based on the transit and RC time is shown in Fig. 2(right) for different widths and lengths. Based on these results, the width of the waveguide PD was designed 1.5 μm to achieve the best performance while normal optical lithography could still precisely define the waveguide. The calculated total resistance (R_{total}) is about 105 Ω (40 Ω) for 30-μm (80-μm) PD, and the RC bandwidth is about 70 GHz (50 GHz). Therefore, the estimated total bandwidth is 35 GHz (32 GHz) for 30-μm (80-μm)-long PD, mainly limited by the transit time. The cross-sectional view and distribution of the resistance and the capacitance of the PD is shown in Fig. 3.

To minimize the transmission loss, the access waveguide is 3 μm wide, shallowly etched, linearly tapered to the deeply etched 1.5-μm-wide PD.

III. FABRICATION

The epitaxial material was grown on an SI InP substrate by three-step low-pressure metal–organic vapor phase epitaxy at 625 °C. The first epitaxy finished with a 120-nm-thick SOA active InGaAsP layer ($Q1.55$, $\lambda_{gap} = 1.55$ μm), embedded between two quaternary confinement layers ($Q1.25$) with different doping levels, covered by a 200-nm-thick p-InP layer. Next, the active sections were defined by lithography and reactive ion etching (RIE) using a SiN$_x$ layer as the etching mask. In the second epitaxy 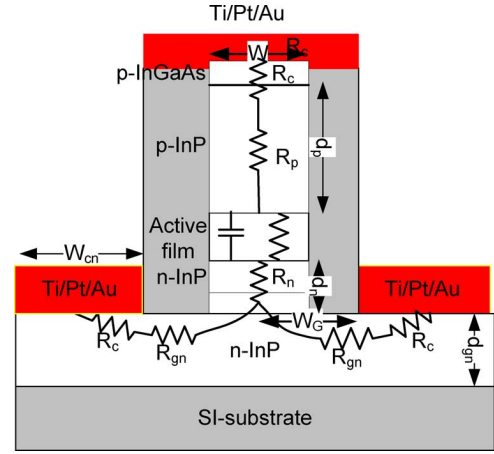step, a $Q1.25$ InGaAsP layer was selectively grown for the passive sections with the SiN$_x$ mask protecting the active sections. In the third epitaxy step, the p-doped InP cladding layers with graded doping level and the p-InGaAs contact layer were grown with a total thickness of 1300 nm. The typical reflectivity at butt-joint is lower than -40 dB, and the transmission loss is lower than 0.19 dB [8]. There are four different RIE etching steps in total, the etching until the SI-substrate for the ground–signal–ground (GSG) probe pads, deep etching until highly doped n-InP layer for the PD, shallow etching until 100 nm into the waveguide film layer for the access passive waveguide and p-contact layer removal from the passive waveguide (300 nm). Polyimide was spun for passivation and planarization. Before metallization, first we etched back the polyimide in a barrel etcher to expose the p-InGaAs contact layer. Afterwards, we used photoresist as a mask to protect the exposed p-contact, and etch the polyimide directionally to open the n-InP contact layer. To form the metal contact, Ti–Pt–Au were evaporated on the top p-InGaAs and the lateral grounds (n-InP) through lift-off. The gap distance between the p- and n-contact was designed 10 μm. To minimize the RF transmission loss, the contacts were electro-plated until the thickness of the gold was about 1.5 μm, which is three times larger than the skin depth. The photograph in Fig. 1 shows fabricated PDs with metal contacts, which were tapered from the PD to the GSG
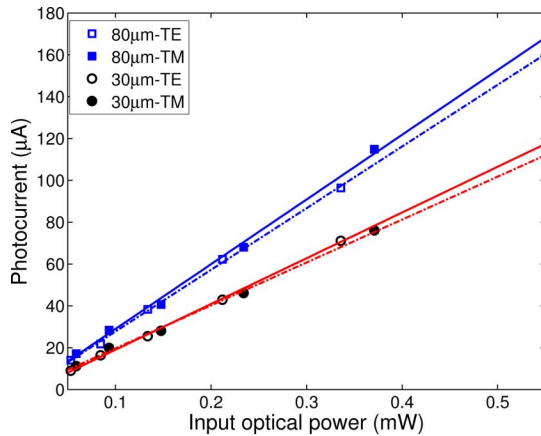
Fig. 4. Measured photocurrent of 30- and 80-μm-long PDs for both TE and TM polarization as a function of the input optical power ($P_{\text{laser}} \times R_{\text{facet}}$) at -4 V. The straight lines are linear fits.

Fig. 5. Frequency response of a 30-μm-long PD (gray) and an 80-μm-long PD (black).

probe pads which have a 100-μm pitch. The central contact is 70 μm wide. The access side was cleaved with about 33% and 26% facet reflectivity (R_{facet}) for transverse-electric (TE) and transverse-magnetic (TM) polarization.

IV. EXPERIMENTAL RESULTS

The optical signal is coupled into the waveguide via the cleaved facet of the chip. All measurements were performed using on-wafer probing. The deeply etched PDs exhibit low dark current, less than 50 nA at -4-V bias voltage for the PDs up to 80 μm long. To determine the external responsivity for different polarization states, a tunable laser was used as a light source, and the polarization was selected through a polarizer and coupled through a microscope-objective to the waveguide PD. The measured photocurrents for TE and TM at $\lambda = 1.55$ μm under -4 V are shown in Fig. 4 for two different lengths. The input optical power in Fig. 4 is the power from the laser (P_{laser}) multiplied by R_{facet} for TE and TM polarization. The 80-μm-long PD has a higher responsivity than 30-μm-long PD. The polarization dependence in responsivity for 30-μm (80-μm)-long PDs is small, less than 0.27 dB and (0.2 dB).

On-wafer S-parameter measurements are performed in the range of 10 MHz to 67 GHz with a lightwave component analyzer and a 50-GHz RF probe. The PD was biased at -4 V through a 65-GHz bias tee, and the injected wavelength from the lightwave analyzer is 1.55 μm with -1-dBm optical power before the lensed fiber. The measured small signal frequency response (optical–electrical) is given in Fig. 5. The vertical axis is the actual responsivity relative to 1 A/W at different frequencies. Thus the measured RF responsivity of 30-μm (80-μm)-long PD is about 0.25 A/W (0.35 A/W) at 10 MHz to 0.16 A/W (0.18 A/W) at 50 GHz. If we take 5 dB as fiber-chip coupling loss (1.5-dB uncoated facet, 3.5-dB mode mismatching), the internal quantum efficiency is about 64% (89%) at 10 MHz to 41% (46%) at 50 GHz. The measured 3-dB total frequency response is 35 GHz (28 GHz) for 30-μm (80-μm)-long PD, which is in good agreement with the simulated total bandwidth in Fig. 2. The oscillation in the measurement is due to the reflection between the RF probes.
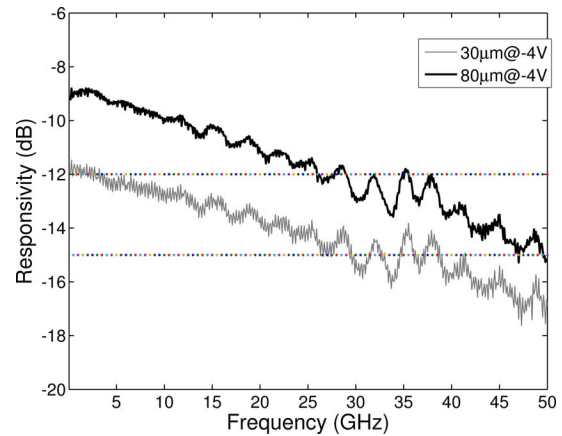
V. CONCLUSION AND DISCUSSION

By using an SI substrate and deep etching, a small-area waveguide PD based on an amplifier/laser layer stack achieved up to 35 GHz with 0.25 A/W external RF responsivity, and less than 0.27-dB polarization dependence. This result enables the monolithic integration of source and high-performance PD based on flexible butt-joint active–passive material without the need for a dedicated detector layer stack. It will be suitable for 40-Gb/s operation.

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