Analog fault diagnosis : a fault clustering approach

Analog Fault Diagnosis: A Fault Clustering Approach

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Abstract

A novel analog circuit fault diagnosis method is proposed. This method uses a neural network paradigm to cluster different faults. It is capable of dealing with the common fault models in analog circuits, namely the catastrophic and parametric faults. The proposed technique is independent of the linearity or nonlinearity of the circuit. The process parameter drifts and component tolerance effects of the circuit are well taken care of. Several fault diagnosis strategies for different problem complexities are described. The proposed methodology is illustrated by means of an Operational Transconductance Amplifier (OTA) example.

1: Introduction

Analog circuits have reached certain maturity in the past few decades. However, the analog fault diagnostic techniques are still very modest. For analog circuits, fault diagnostic techniques are more complex when compared to their counter parts in digital circuits for various reasons. The circuit component tolerance in fault free and faulty circuits, the nonlinearity properties of analog circuits and the limited access to the internal nodes of the circuit being the the major factors that contribute to its complexity. Many different analog fault diagnosis methods have been proposed [1]–[3], [9]–[13].

Current analog fault diagnostic techniques often suffer the additional problems of i) Increased silicon area and power consumption with built–in self test circuits [4], ii) The requirement of measurements of current and voltage signals at internal nodes and iii) The lack of good models to simulate the circuit under test.

We propose a nonconventional and more general approach capable to overcome the above limitations. The basic idea of this methodology consists of training a neural network paradigm. The training input vector has a set of data points consisting of families of simulated faulty as well as fault free behaviors of the circuit. These input vectors are called *signatures*. The neural network paradigm classifies these signatures into different clusters. The actual experimental vector called the *test vector*, obtained from the circuit under test, is then presented to the neural network. The network outputs the cluster of known signature(s) that best matches this test vector. This approach allows the testing as well as the diagnosis of the circuit. Several degrees of complexity of the proposed technique are introduced in this paper. The practical and theoretical aspects of this technique are verified and illustrated by means of an IC example.

2: Background

A Kohonen network is a feature mapping self–organizing neural network with unsupervised competitive learning [5]. The characteristics of this network is that it maps a given random input stimuli space to a *cluster* space composed of distinct cluster elements. For example, a Kohonen network can be used to highlight a letter, say, "A", from a given set of characters consisting of letters and numbers and written in any calligraphic style. After training, the network should be able to group all "A's" of various calligraphic styles in one single cluster.

Let us briefly describe the behavior of a Kohonen network. Fig. 1 shows its basic structure. The layer consists of N ordered processing elements each receiving n input signals x_1, x_2, x_3 ... x_n coming from an n–dimensional Euclidean space. A weight w_{ij} is

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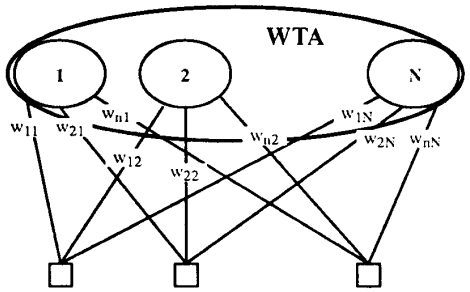


Fig. 1. Khonen Network Architecture

associated with the *jth* Kohonen processing element and the *ith* input signal. Each Kohonen processing element calculates a matching score M_i according to the formula : $Mj = D(W_j, X)$. Where $W_j = (w_{1j}, w_{2j}, w_{3j} \ldots w_{nj})^T$, $X = (x_1, x_2, x_3 \ldots x_n)^T$ and the function $D(a,b)$ is a distance measurement function. The Euclidean distance, $D(a,b) = |a - b|$, is a common measure used in many applications. Input signal vectors X, randomly taken from the input space, are presented to the network one at a time. The number of input vectors can be Q, $Q \leq N$. Once each Kohonen processing unit has calculated its matching score M_j, a competition takes place in the Winner Take All layer (WTA) to determine which of the units has the smallest matching score, i.e to find out the weight vector W_j that most closely resembles the input vector X. Matching score (M_j) ties are broken based on the processing unit index number. The unit with the smallest matching factor is called the *winner*. A unit can win for more than one input vector X or may not win at all. The winner for a particular vector(s) is said to represent that vector(s). The learning is implemented by updating the weights by a fraction η such that M_j is minimized. See Appendix for the algorithm.

3: Fault Diagnosis Methodology

3.1: Procedure

A set of signatures is obtained from sampling the response of the circuit for various behavioral conditions (BC). These BC's include the fault free case and a predefined set of faulty cases such as shorts and breaks. The responses (signatures) can be obtained by performing a frequency domain, time domain or a dc analysis using a circuit simulator such as HSPICE. Data is obtained by simulating the circuit with the fault induced and then by sampling the response at n different points. This procedure is repeated for each fault case and for the fault free circuit. We denote the set of data points as an *n–dimensional signature*. Next, a Kohonen network with n inputs and N processing elements, where N is the number of BCs and n is the dimensionality of the signature, is trained according to the algorithm described in Appendix. The Kohonen network maps the signatures from the initial random vector space onto the processing elements. This vector mapping property of the Kohonen network is used to classify the signatures, and thus, to identify the faults.

Fig 2. shows our fault–diagnosis procedure. A cluster table is generated by recording the winner processing unit for each input signature. If a unit wins for more than one signature, then the fault cases associated with those signatures are said to be *collapsing faults*. These faults cannot be isolated from each other using only these signatures. We denote the phenomenon of reducing the initial vector space, that includes all the signatures, to a vector space consisting of fewer signatures as *fault clustering*. If this new vector space represented by a unit consists of only a single signature, then the fault case associated with that signature can be isolated. This is referred to as *fault isolation*.

3.2: Optimal Sampling Points

A good criteria was proposed in one of the earliest techniques for constructing fault dictionaries for linear frequency dependent circuits [6]. This criteria has been used ever since [7-8]. As our technique involves ac, dc and transient analyses, an alternate method was developed. This technique is a compromise between a good representation of all the responses and the number of sampling points. Lesser sampling points implies smaller Kohonen networks and hence shorter training periods. The basic idea is to obtain the responses with a good number of sampling points and compute independent–sets of sampling points for each signature by taking the derivative of the curve and including the points at

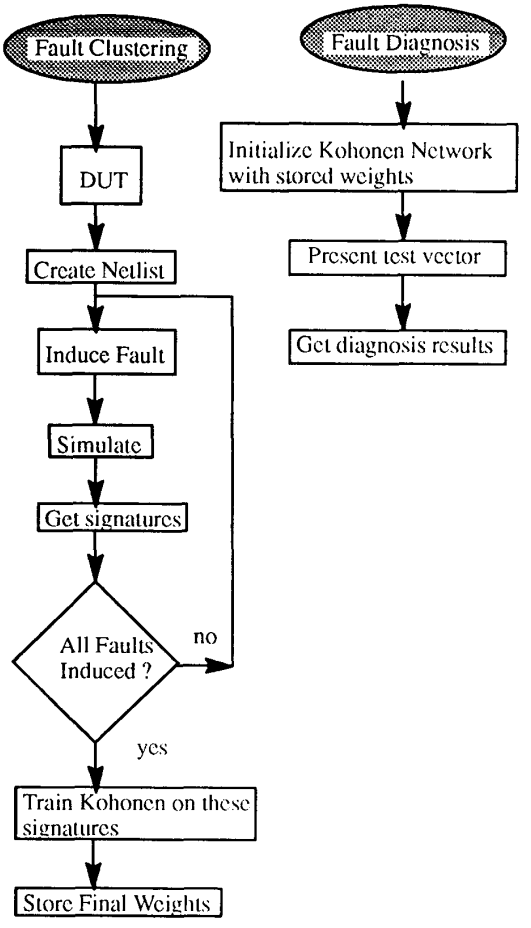


Fig. 2. Fault diagnosis procedure

which the absolute value of the derivative is greater than a reference parameter *deviation*. The set of optimal sampling points, consisting of all the points in the above independent–sets, is then obtained. The algorithm below implements the proposed method. Observe that the parameter *deviation* is adjustable and offers a degree of freedom to control the set of sampling points. A deviation of 5% is used in our experiment. Let Mi(t) is the magnitude of the signature at point t, S(i) is the initial set of points used to generate the curves and γ is the optimal sampling point set.

Step 1: For each signature i do
Compute deviation1 = $\{M_i(t) - M_i(t-1)]/M_i(t-1)\}*100$
Compute deviation2 = $\{M_i(t) - M_i(t-2)]/M_i(t-2)\}*100$
if deviation1 > *deviation*
Include t in the independent–set IS(i)
elseif
deviation2 > *deviation*
include t in independent–set IS(i)
Go to Step 1

Step 2: For each point p∈S(i)
if(p ∈ IS(i))
include p in γ.
Go to Step 2

Fig. 3 shows three curves which are generated with a set of

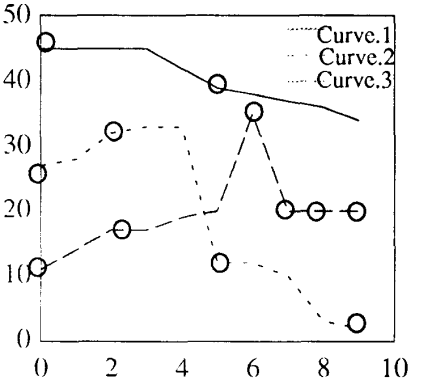


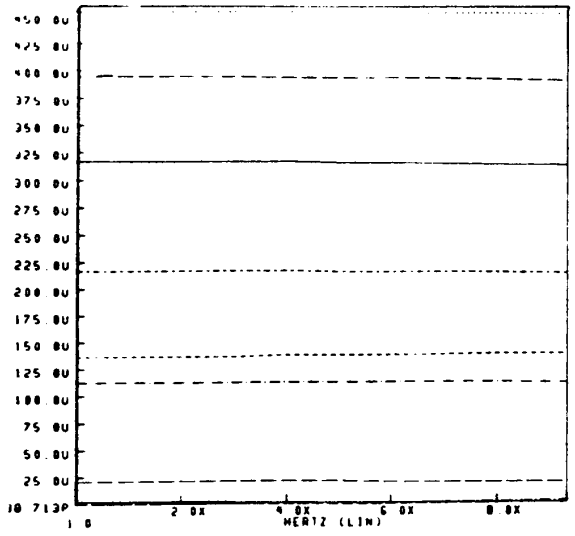
Fig 3: Optimal Sampling Points

ten points each. Applying the algorithm to these signatures yields the marked points for each signature. The γ set includes points 0, 2, 5, 7, 8, 9.

4: Practical Results

The techniques presented presented are tested on the OTA circuit shown in Fig 4a. A set of 11 BCs, listed in Table 1, is considered and the circuit is simulated using HSPICE. For illustration purposes, only single bridging faults are considered for verification of these techniques. The bridging faults are modeled by a 5Ω resistor. For the ease of measurement, the OTA is configured as shown in Fig. 4b. The output current is obtained from the ac analysis and the magnitude is plotted for each BC over a frequency

range of 1 to 10MegHz as shown in Plot 1.



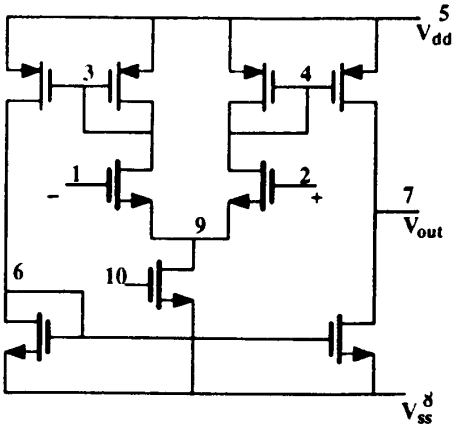
Plot. 1. Signatures of the OTA.

A broader classification of fault clusters is accomplished using the basic technique described above. However, a finer isolation of these clusters can be obtained by using a combination of Kohonen networks and/or multiple analyses. This strategy yields four categories:

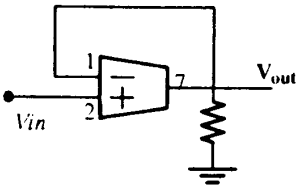
1) Single Kohonen Single Analysis (SKSA)
2) Multiple Kohonen Single Analysis (MKSA)
3) Single Kohonen Multiple Analysis (SKMA)
4) Multiple Kohonen Multiple Analysis (MKMA)

4.1: SKSA Approach:

This is the simplest of all the approaches. A possible fault classification is shown in Fig. 5. The ellipses represent a clustering of BCs. Here, the signatures are generated by simulating the circuit with each induced fault and by performing a dc, ac, or transient analysis sampling the response at the output node. The results obtained for the magnitude of the frequency response are shown in the second column of Table 2. We see that there are 8 clusters two of which indicate collapsing faults, namely BCs 0,9 and BCs 6,7,8. Similar results were obtained from a dc analysis, a phase analysis, and a transient analysis, though the contents of the clusters differed in each case.



(a)



(b)

Fig. 4. OTA
(a) Circuit (b) Configuration

Table 1. Behavioral Conditions

BC	Short Between Nodes
0	fault free
1	1–6
2	4–5
3	1–3
4	6–8
5	2–9
6	4–7
7	9–10
8	4–6
9	4–9
10	3–5

4.2: MKSA Approach :

In this approach more than one Kohonen network is used. The generic architecture is shown in Fig. 6. The boxes represent new Kohonen networks trained on the signatures corresponding to the magnitude of a frequency analysis. In this structure, the BCs yielding fault collapsing in the SKSA are used to train another Kohonen network to obtain further classification. As the vector space is now reduced to include only the signatures that are clustered together, the network now has to train on a more uniform distribution of signatures. The information from the signatures is utilized to the maximum possible extent in this approach.

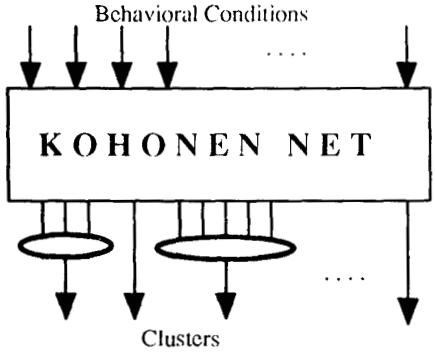


Fig. 5. SKSA Architecture

Considering the output of the two rectangular boxes marked *Magnitude* in Fig.7 the BCs 7 and 8, that are clustered together in the SKSA approach, are isolated from each other in this approach. We see that a classification better than the one obtained from the SKSA is achieved. This technique is quite inexpensive and can be used as a preprocessor to reduce the search space. This idea is analogous to the fault collapsing technique done in digital testing.

4.3: SKMA Approach:

This Single Kohonen Multiple Analysis technique yields a better classification of BCs. Under this approach, the same Kohonen network can be used (as the architecture is the same) for signatures of different analyses by re-initializing the weights. Different signatures can be obtained by *i)* performing a different analysis *ii)* taking the response at different access points in the circuit. The latter option is often more expensive than the first one as it has an overhead of a few more pads in the chip. For our experiments, the phase response of the circuit is used to obtain new signatures. The clustering done by this approach is shown in the 3rd column of Table 2. By inspecting the results of both analyses we can see that BCs 5 and 6 are now isolated. This does a better fault collapsing than the SKSA at the possible cost of additional analyses.

Table 2. SKSA and SKMA results

BC	Magnitude Winner	Phase Winner
0	2	4
1	9	4
2	0	4
3	3	4
4	7	4
5	5	3
6	4	9
7	4	4
8	4	4
9	2	4
10	6	4

4.4: MKMA Approach

A new set of signatures are generated only for those fault cases that are clustered together in the MKSA approach. The MKMA architecture represents a tree in which each Kohonen network can be trained on different analyses. In our experiments new sets of signatures are obtained from the phase response. These signatures are generated only for faults that are collapsing. In our case, for BCs 0, 8, 5 and 7. The depth of the tree, the number of Kohonen networks and the number of different analyses are the important factors in this method. These are the metrics used for comparison of the degree of classification obtained from the whole process. Fig. 7 shows that all the

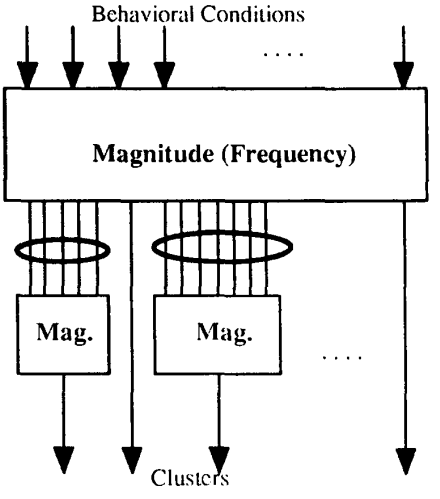


Fig. 6. MKSA Architecture

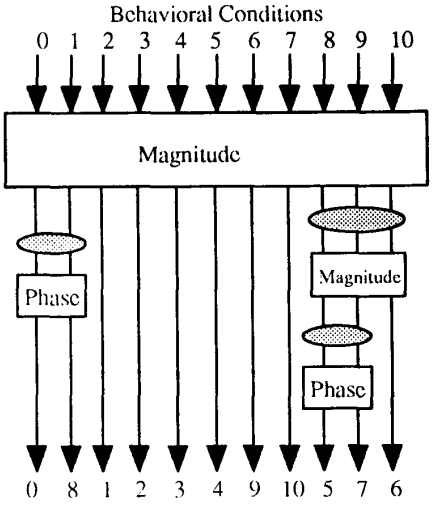


Fig. 7. MKMA Kohonen architecture for the OTA

BCs are in fact isolated. The depth of the tree depends on the response of the system, i.e the distribution of the signatures in the vector space, and need not necessarily depend on the number of fault cases considered. The latter observation is investigated with similar experiments using 18 BCs. We could see that all the faults were isolated and that the depth of the tree, the number of Kohonens and the number of analyses were the same for both experiments.

This method is self–sufficient as it can be repeated for a complete isolation of faults. Many techniques have been proposed that require node voltage and current measurements measurements [2]–[9]. This technique guarantees the minimum use of additional access points hence reducing computational complexity and silicon overhead. If the signatures obtained from the response of the circuit at its output node for different analyses do not provide the desired classification, the signatures can then be taken from the response at a different node which provides the desired classification. Then, this node can be used as an observation point. Thus, any access points for circuit observability, in addition to the output pad, can be determined by this approach.

4.5: Remarks And Observations

The fault diagnosis method presented in this paper has the following relevant features:

4.5.1: Process Variation Independency

Current Simulation Before Test (SBT) techniques are limited due to parameter drift and noise. Using these techniques, there is a chance that a given signature is not among the stored faults in the dictionary, in which case fault diagnosis is not possible. In our approach, as the mapping is from the signature vector space and not from the signature itself, effective diagnostic results are obtained if the parameter drift due to process variation and noise are approximately 7–10% of their nominal values. This feature was verified through the MKMA approach over a set of process parameters for the MOS transistors used in the OTA. Test signatures were obtained from the circuit with the process parameters changed to within 10% of their nominal value. The results obtained were the same as those obtained with test signatures obtained with the nominal process parameters.

4.5.2: Reduced Number of Access Points

In all the experimental results presented in this paper, only the circuit output is used to measure the response. The simulations with the OTA show that a complete fault diagnosis is possible without additional access points.

This is an important factor to consider when testing realistic systems.

4.5.3: Fault Model Independent

This technique can be used to diagnose any kind of faults: *i)* bridges *ii)* opens *iii)* soft faults *iv)* multiple faults *v)* faulty operating conditions.

4.5.4: Extension to Digital And Mixed Mode Circuits

The response of the circuit during the rise time and fall time can be used to generate *mixed-mode* signatures. Cluster tables can be generated using this technique for a digital and mixed mode circuit in a similar fashion as indicated through out the paper.

5: Conclusions

A powerful non-conventional analog fault diagnosis methodology has been proposed. The approach based on training a Kohonen (neural) network has the potential to deal with hard and soft faults, does not require additional overhead or additional silicon area of built-in self test circuits or access to internal nodes of the circuit under test. It has the potential to handle mixed mode circuits and multiple faults. Preliminary results using practical integrated circuits are very encouraging

6: Appendix

Kohonen Paradigm:

The algorithm used to implement the self organizing feature mapping Kohonen network for our fault diagnosis method is as follows:

1) Initialize weights randomly.

2) Present new input pattern.

3) Compute matching factor M_j:
compute distances D_j between the input and each output node j using $\sum_{i=0}^{N-1}(X_i(t) - W_{ij}(t))^2$

4) Select the output node with minimum distance.
Select j^* as the node with minimum distance.

5) Update weights to node j^* and its neighbors.
The neighborhood is defined by $NE(j)$. This has a radius of the entire processing units initially, and decreases monotonically with the iterations(t). As the processing units are uni-dimensional, the radius can be decreased in steps after certain iterations. The new weights for the winner are defined by the learning rule:
$W_{ij}(t+1) = W_{ij}(t) + \eta(\tau)(X_i(t) - W_{ij}(t))$
where $\eta(\tau)$ is any expression which decreases with t. We use the expression $\eta(\tau) = 1/(400 + t)$ in our application. The learning rule for the neurons in the neighborhood is the same as above except that the learning rate $\eta(\tau)$ will be a decreasing function of the radius as well. The expression

$$\eta = \frac{\eta(winner)}{distance\ of\ the\ unit\ the\ winner}$$

is used for the units that fall in the neighborhood.

6) Repeat by going to Step 2.

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