Prelayout interconnect yield prediction

Special Section Transactions Brief

Prelayout Interconnect Yield Prediction

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***Abstract*—Functional yield is a term used to describe the percentage of dies on a wafer that are not affected by catastrophic defects. Within the interconnect these defects are usually caused by particle contamination and are divided into bridging defects, which join adjacent wires and cuts, which result in broken wires. Functional yield is therefore determined by the geometry of the routing channels, how these channels are filled with wire and the distribution of defect sizes. Since the wire spacing and width are usually fixed and the distribution of defects within a mature production facility is well known, the problem reduces to estimating individual wire lengths for cuts and to estimating the overlapping distance that two wires share in neighboring sections of the routing grid for bridges. Previous work in this area has analyzed the problem by assuming that all wiring tracks are occupied with wire, leading to overestimates for the probability of failure due to both cuts and bridges. This paper utilizes statistical models of the placement/routing process to provide a more realistic approach for cut and bridge yield estimation. A comparison of the predicted probability of failure within each wiring layer with postlayout data indicate an average error of 20% for cuts and 26% for bridges.**

***Index Terms*—Critical areas, design, interconnect, reliability, Rent's rule, theory, yield.**

I. Introduction

The first contribution to the area of prelayout wiring analysis may be traced back to an early 1968 paper by Donath on the estimation of lower bounds for average wire lengths in optimally placed circuits [1]. This work, along with the publication of the 1971 paper by Landman and Russo [2] on the use of Rent's rule to estimate the numbers of pins needed by different partitions of a logic graph, led to a large number of influential papers in the 1970s and early 1980s on the analysis of package and on-chip wiring space requirements [3]–[6] and signal propagation delays [7]–[11]. Increasing wire densities in the late 80s saw the emergence of interconnect power dissipation as a new application area for system level interconnect prediction [12]–[15] and, more recently, the development of chemical mechanical polishing and the resulting rise in the number of wiring layers has resulted in many papers addressing the optimal design of multilevel interconnect systems [16]–[18] and via blocking models [19]–[21].

This paper continues in the tradition of this earlier analytical work by attempting to construct a predictive yield model capable of accommodating discontinuous technology changes. Although empirical components are kept to a minimum, the interconnect yield model presented in this paper requires three basic input parameters in order to capture the quality of the place and route algorithms used in the layout of the netlist: the placement Rent exponent p, the placement efficiency η_p, and the routing efficiency η_r.

The placement Rent exponent [2] is a measure of the quality of placement and lies in the range $0.5 \leq p \leq 1$ for all realistic layouts, with lower values indicating better placement quality and a value of unity corresponding to a random placement [22]. The amount of white-space introduced between cells by the placement algorithm to accommodate subsequent routing congestion is modeled by a placement efficiency parameter $\eta_p \leq 1$, so that the effective area of a cell is given by A_{cell}/η_p. Typical values lie in the range $0.5 \leq \eta_p \leq 1$. Finally, the routing efficiency η_r accounts for the fact that not all of the available wiring capacity in a given layer can be utilized by the router. This may be due to inefficiencies in the routing algorithm or the blocking effect of lower wires on access to higher wiring levels [19], [20].

Functional yield is determined by the sensitivity of a particular layout to the formation of catastrophic defects by wires being cut or bridged by a known distribution of defect sizes. This sensitivity is determined by the extent of the so-called critical areas [23], [24] and their computation is an essential step toward realistic yield prediction. As the field of defect and yield modeling evolves, the need for sophisticated tools for critical area prediction (not just computation) has appeared. This evolution goes from tools for critical area extraction of an existent layout [25]–[30], to tools for yield improvement through critical area optimization during the design's place and route phase [31]–[35], to the most recent efforts on pre-layout yield prediction [36]. The core of the previous work relies on statistical critical area characterization of existent layouts and then on using this information, through some parameter fitting, to attempt prelayout yield prediction. In general, for similar layout styles this approach works reasonably well, provided that the technology remains unchanged. The difference with the approach presented in this paper, is that the interconnect critical areas are predicted analytically. Thus, the approach is not constrained to one particular layout style or technology. With an analytical approach it is possible to study the interconnect manufacturability of a netlist under distinct routing strategies, including strategies for optimizing delay, power dissipation, area, etc. [37], [38]

Section II begins by providing an overview of the interconnect functional yield model. The basic concepts of cut and bridge defects are defined and the sensitivity of a design to these defects is described through the concept of critical areas. Section III then provides a summary of recent work on the prediction of global wire length distributions (pseudoplacement) and how these distributions are allocated to individual wiring layers (pseudorouting) to prepare for the results of Section IV. The paper concludes in Section V with a discussion of the sources of error in the model and directions for future work to make the model more robust.

II. Defect Sensitivity Analysis

In a mature process the principal mechanism for yield detraction is the presence of defects characterized by a known defect size distribution $F(x)$. The distribution is commonly described by a power law

$$F(x) = kx^{-\gamma} \quad \text{for } x_{\min} < x < \infty \tag{1}$$

where $x_{\min}$ is the minimum resolvable lithographic feature size, $\gamma \approx 3$ [39] and k chosen so that the area under the distribution is unity. In this form, $F(x)$ is interpreted as the probability that a single defect larger than $x_{\min}$ has a size in the range x to $x + dx$.

The presence of a defect does not necessarily lead to a catastrophic failure, however. For this to occur, the center of the defect must fall within a so-called critical area, whose extent depends on the defect size.

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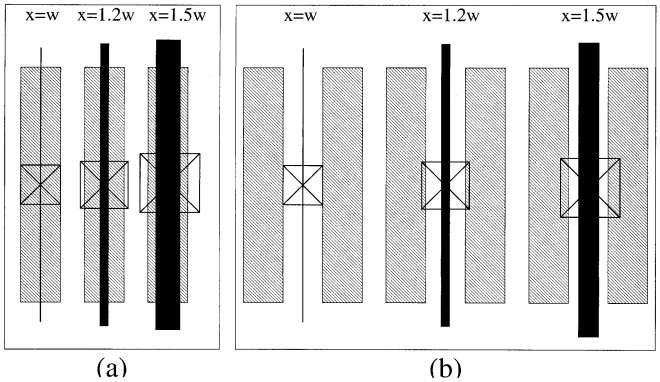

Fig. 1. Definition of critical areas for (a) cuts and (b) bridges.

Fig. 1(a) shows critical areas for cut defects, for several defect sizes. If the center of a defect with the specified size falls anywhere inside the critical black areas, then the wire (shown shaded) will be broken.

The size of the critical area for cuts is clearly zero if the size of the defect is less than the width of the wire and increases in proportion to the defect size for sizes greater than the wire width. For the nth wiring layer, characterized by wires of width w_n, the critical area for cuts inside a single wire of length ℓ, caused by defects of size $x > w_n$, is given by $(x - w_n)(\ell + x)$. In order to simplify the mathematical treatment, the approximation $\ell \gg x$ is made, so that the critical area may be approximated by $(x - w_n)\ell$. For many wires characterized by a length distribution $N(\ell)$, an approximation to the total critical area is obtained by summing the individual critical areas

$$A_{c_n}(x) = \begin{cases} 0 & \text{for } 0 \le x < w_n \\ (x - w_n)\sum_\ell N_n(\ell)\ell & \text{for } w_n \le x < x_{c_n} \\ A_{\text{chip}} & \text{for } x \ge x_{c_n} \end{cases} \quad (2)$$

where A_{chip} is the total die area. Since the critical area cannot exceed the total area available for wiring, A_{c_n} saturates at a defect size of

$$x_{c_n} = w_n + \frac{A_{\text{chip}}}{\sum_\ell N_n(\ell)\ell}. \quad (3)$$

This behavior is only approximate, however, and a more detailed description requires consideration of cuts induced in neighboring wires. The approximate behavior described by (2) is acceptable because the defect distribution decays as a cubic function of x and therefore the behavior of the critical area for large defect sizes exerts only weak influence on the probability of failure. For a more complete discussion of the effects of multiple wire interactions, the reader is referred to [23].

Fig. 1(b) indicates how the probability of a defect of size x causing a bridging defect increases with defect size if the center of the defect is located anywhere inside the critical area for bridges. In contrast to the cut model, it is not the length of the wire that determines the critical area, but rather the common length shared by two wires in adjacent sections of the routing grid m [40]. For a wiring layer characterized by a wire spacing s_n, the critical area for bridges between two wires sharing a run length m is given by $(x - s_n)(m + x)$. As with cuts, we assume $m \gg x$, so that the critical area may be approximated by $(x - s_n)m$ and that the critical areas for many wires simply sum

$$A_{b_n}(x) = \begin{cases} 0 & \text{for } 0 \le x < s_n \\ (x - s_n)\sum_m N_n(m)m & \text{for } s_n \le x < x_{b_n} \\ A_{\text{chip}} & \text{for } x \ge x_{b_n} \end{cases} \quad (4)$$

where $N_n(m)$ is the number of shared runs of length m in the nth wiring layer. As for the case of cuts, the critical area for bridges cannot exceed the area of the chip and it saturates at a value of

$$x_{b_n} = s_n + \frac{A_{\text{chip}}}{\sum_m N_n(m)m}. \quad (5)$$

The growth in the critical area for both cuts and bridges represents the fact that larger defects are more likely to cause catastrophic failures. The critical area may be reexpressed as a probability by dividing it by the area available for wiring A_{chip}, so that it may be interpreted as the probability that the presence of a defect of size x anywhere on the die causes a failure. In this form the critical area functions are referred to as sensitivities and are given by

$$S_{c_n}(x) = \begin{cases} 0 & \text{for } 0 \le x < w_n \\ \frac{(x-w_n)}{A_{\text{chip}}}\sum_\ell N_n(\ell)\ell & \text{for } w_n \le x < x_{c_n} \\ 1 & \text{for } x \ge x_{c_n} \end{cases} \quad (6)$$

and

$$S_{b_n}(x) = \begin{cases} 0 & \text{for } 0 \le x < s_n \\ \frac{(x-s_n)}{A_{\text{chip}}}\sum_m N_n(m)m & \text{for } s_n \le x < x_{b_n} \\ 1 & \text{for } x \ge x_{b_n} \end{cases} \quad (7)$$

for cuts and bridges, respectively.

From (6) and (7) one can infer that the sensitivity to cuts is greater than the sensitivity to bridges because, unless the router utilizes 100% of the routing channels, the total length of the wires must be greater than their total shared run length. However, test data from silicon foundries indicates that the number of short circuit faults is greater than break faults. This implies that the underlying defect mechanisms for cuts and bridges are different; the discussion of these mechanisms is out of the scope of this paper.

Finally, the probability of cut or bridge failure due to a single defect of size x, is given by the product of the probability that a single defect has size x and the probability that the defect is present in the critical area. By summing over all defect sizes, the probability of failure (POF) is obtained as follows:

$$\text{POF}_{c_n} = \int_{x_{\min}}^{\infty} F(x)S_{c_n}(x) \quad (8)$$

$$\text{POF}_{b_n} = \int_{x_{\min}}^{\infty} F(x)S_{b_n}(x) \quad (9)$$

for cuts and bridges, respectively.

III. Wire Length and Shared Wire Length Analysis

The first step toward the *a priori* estimation of the functions $N_n(\ell)$ and $N_n(m)$ used in the calculation of sensitive areas for cuts and bridges, respectively, is an estimate of the global wire length distribution $N(\ell)$. In addition to the number and size of the standard cells and the number of nets, two empirical parameters must be supplied to perform this calculation: the placement Rent exponent p and the placement efficiency η_p. For a discussion of how to employ these parameters for the estimation of the global wire length, the reader is referred to the planar model of [41].

This planar model is limited to the analysis of netlists constructed with identical cells connected by two-terminal nets. Although this is not a major limitation since 90% of the nets within a real netlist are two-terminal nets, the presence of higher-order n-terminal nets will necessarily lead to errors in our analysis. Since the focus of this paper is on the the accuracy of the yield model and not on the accuracy of

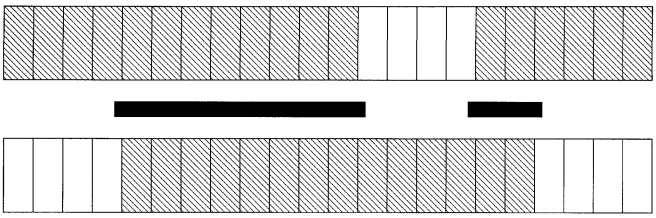

Fig. 2. Distribution of critical areas for bridges.

wire length estimation, we have chosen to employ a synthetic netlist constructed from cells connected by two-terminal nets.

The layer-dependent sensitivity to cuts, defined by (6), is dependent on the total intralayer wire length $\sum_\ell N_n(\ell)\ell$, rather than on the global wire length distribution $N(\ell)$. The allocation of $N(\ell)$ to different wiring layers may be accomplished by an algorithm which begins by calculating the maximum wiring capacity, L_{cap_n}, of each layer

$$L_{\mathrm{cap}_n} = \frac{A_{\mathrm{chip}}}{s_n + w_n} \quad \text{for } 1 < n < N_w \tag{10}$$

where N_w is the number of wiring layers, s_n is the wire spacing, and w_n is the wire width. The available wire capacity which may actually be used for routing is then found by multiplying the maximum wiring capacity by the routing efficiency η_r. The algorithm allocates wires from $N(\ell)$ to the first wiring layer, shortest wires first, until the available wiring capacity of the layer is reached. Then wires are allocated to the next highest layer and so on, until either all the wires are allocated, or the available capacity of the highest layer is exceeded, in which case the circuit is unconstructible.

The layer-dependent sensitivity to bridges, defined by (7), is dependent on the total shared run length $\sum_m N_n(m)m$. Although routing channels are layed out in a plane, the calculation of critical areas for bridges is essentially a one-dimensional (1-D) problem. Fig. 2 illustrates this idea by dividing the available wiring capacity of two adjacent routing channels into boxes of length equal to the critical dimension, which are referred to as routing segments. Contiguous shaded routing segments represent wires, while black boxes represent critical areas for bridges. Since the length of each routing segment is equal to the critical dimension, the total number of routing segments is equal to the total layer wire capacity and the total number of filled routing segments is equal to the total wire length (expressed in units of the critical dimension).

The existence of a black critical area between two routing segments requires that both the routing segment above and below the critical area are filled with metal. Clearly, if all of the routing segments are filled with metal, the probability of being filled is unity and the total shared run length is equal to the maximum channel capacity L_{cap_n}. In general, the probability of a segment being filled with metal, P_n, is given by the ratio of the total amount of wire, L_{tot_n}, allocated to the maximum wiring capacity

$$P_n = \frac{L_{\mathrm{tot}_n}}{L_{\mathrm{cap}_n}}. \tag{11}$$

Since L_{tot_n} cannot exceed $\eta_r L_{\mathrm{cap}_n}$, P_n cannot be greater than η_r.

If the probability that single segment is filled is independent of whether the segment in the channel below it is filled, then the probability of both segments being filled is given by the product of the individual probabilities P_n^2. Since the total number of routing segments is equal to L_{cap_n}, the total number of shared run lengths is given by

$$\sum_m N_n(m)m = L_{\mathrm{cap}_n} P_n^2. \tag{12}$$

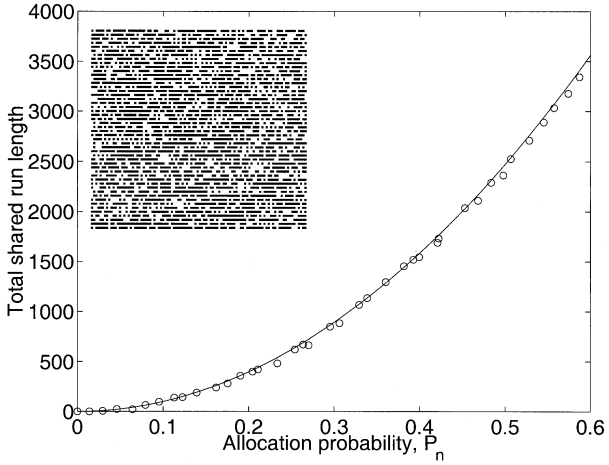

Fig. 3. Comparison of total shared run lengths predicted using (12) (indicated by solid line) with measured total shared run length (indicated by circles), as a function of allocation probability. Shown inset is a test layout generated by filling routing segments with probability $P_n = 0.6$.

Since $L_{\mathrm{cap}_n} = L_{tot_n}/P_n$ and $L_{\mathrm{tot}_n} = \sum_\ell N_n(\ell)\ell$, this may also be written as

$$\sum_m N_n(m)m = P_n \sum_\ell N_n(\ell)\ell. \tag{13}$$

The accuracy of this equation has been investigated by extracting total shared run lengths from sample layouts and comparing the data with the predictions. After allocating metal to routing segments, the layout was scanned to extract the total length of the critical areas between the channels. Fig. 3 plots as circles the extracted total shared run lengths as a function of P_n for 40 layouts, created using allocation probabilities ranging from zero to a maximum of $P_{n_{\max}} = \eta_r$. The allocation procedure corresponds to the allocation of a random distribution of wires to the layer and, at least for this distribution, the model appears to accurately predict the correct total shared run lengths.

IV. Experimental Procedure and Results

The synthetic netlist used in this study was characterized by 1024 identical cells of size $4 \times 4\ \mu(\mathrm{m})^2$, with 2048 two-terminal nets. An *a priori* estimate for the global length distribution of this netlist was made by assuming values for the Rent exponent and the placement efficiency. The selection of each of these three parameters is dependent on the particular software tools used for layout. In the experiments reported in this paper, Cadence Design Systems' Silicon Ensemble was used with placement performed by *QPlace* and routing by *WRoute*. For the synthetic netlists used in this study it was found that a value of $p = 0.8$ characterized the level of placement optimization and a placement efficiency of unity (zero white-space) allowed successful routing.

The wire lengths within this estimated distribution were allocated to the six-layer interconnect with wire widths and spacings listed in the first two rows of Table I. These geometry specifications allow the calculation of the available wire capacity by assuming a value for the routing efficiency in each layer. For the two-terminal synthetic netlists used in this study, it was found that the routing efficiency was approximately constant in each wiring layer at $\eta_r = 0.6$, a value in broad agreement with the data of Sai-Halasz [19].

The total length of wire allocated to each layer is listed as L_{tot_n} and the percentage of the available wiring capacity used is listed as $L_{\mathrm{tot}_n}/(\eta_r L_{\mathrm{cap}_n})$. For all fully utilized layers (1–5), the percentage of the available wiring capacity used is approximately 100%. However, in layer 6, all of the wires contained in $N(\ell)$ were allocated before the

TABLE I
RESULTS OF ALLOCATION PROCESS FOR THE TEST NETLIST WIRELENGTH ESTIMATE. ALL LENGTHS ARE EXPRESSED AS MULTIPLES OF A 0.16-μm CRITICAL DIMENSION

Layer n	1	2	3	4	5	6
w_n	2	2	2	2	4	4
s_n	2	2	2	2	4	4
$\eta_r L_{cap_n}$	96,000	96,000	96,000	96,000	48,000	48,000
L_{tot_n}	95,800	95,975	95, 350	95,150	47,350	26,225
$\frac{L_{tot_n}}{\eta_r L_{cap_n}}$	99.79%	99.97%	99.32%	99.11%	98.65%	54.64%

wire capacity of this layer was reached. This resulted in only 55% of the available wire capacity $\eta_r L_{\mathrm{cap}_6}$ being used.

The data of Table I were used to construct the predicted sensitivity graphs, shown in Fig. 4 as solid lines, for both cuts and bridges. For wiring layers one through four, the predicted sensitivities are identical and the curves are coincident. In order to compare the *a priori* predictions for the cut and bridge sensitivities with real data, a software tool called XLASER [28] was used to extract sensitive area data from the test netlist after layout. These data are represented by dashed lines in Fig. 4.

As discussed in Section II, sensitivity data may be expressed in terms of a POF using (8) and (9), if the defect size distribution is known. A minimum resolvable defect size of $x_{\min} = 0.13$ μm was assumed and this enabled the POF to be evaluated for each of the wiring layers. These data are listed in Table II. The average error in predicting the POF for cuts is 20%, while the average error for predicting the POF for bridges is 26%.

V. CONCLUSION

A new model for predicting the manufacturability of a netlist prior to layout has been presented. An *a priori* estimate of the wire length distribution is combined with a critical area model for cut and bridge defects to produce an estimate for the probability of failure due to the presence of a single defect in each wiring layer.

The three principle components of the model are: length prediction, layer assignment and critical area estimation. Each of these components introduces sources of error and the overall POF estimate is quite sensitive to the choice of Rent exponent p, the routing model and the routing efficiencies η_r in each wiring layer. The routing model allocated wires, shortest wires first, to the six wiring layers in a manner which reproduced the constant routing utilization observed in the actual layout of the circuit. The choice of a value of $p = 0.8$ for the Rent exponent cannot be rigorously justified, however, and represents a reasonable estimate based on experience with the place and route tool used in the experiments.

The models for both cuts and bridges are essentially first-order and neglect the possibility that a single defect could cut two, or bridge three, neighboring wires. The effects of these higher-order failure modes are observed in the deviation from linear behavior for the extracted (dashed line) data for large defect sizes in Fig. 4. The errors introduced into the POF model by not including these effects are minimal, however, because the POF is calculated by multiplying the sensitivity by the defect distribution function, which decays as x^{-3}. A preliminary analysis, which included second-order interactions, resulted in a change in the estimated POF by less than 10%.

A more significant source of error, especially for bridges, is the assumption that the wires are evenly distributed throughout the wiring layer. While this would seem to be a rational strategy for a router, our experience with the router used in these experiments has shown that the routing channels of partially filled wiring layers are not populated in this manner. This might explain why the predicted POF for bridges in Table II is consistently below the extracted POF (with an average

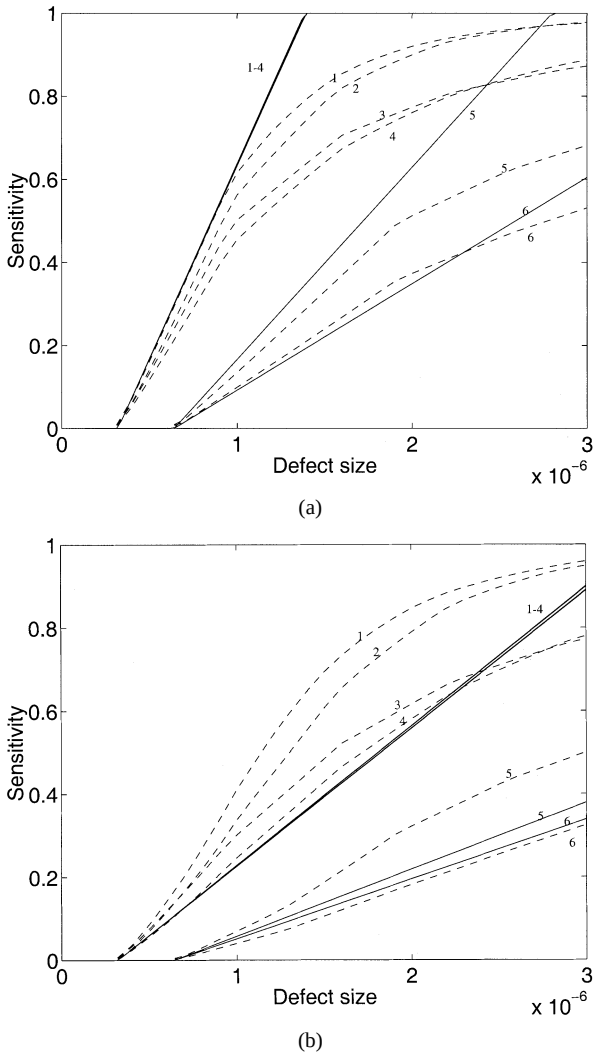

Fig. 4. Comparison of predicted and extracted sensitivities from test layout for (a) cut and (b) bridges. Solid lines represent predicted data and dashed lines represent extracted data. For wiring layers one through four, the predicted sensitivities are identical and the curves are coincident.

TABLE II
COMPARISON OF PREDICTED AND EXTRACTED POF FOR CUTS AND BRIDGES IN EACH WIRING LAYER

Layer n	1	2	3	4	5	6
CUTS						
Predicted POF_{c_n}	2.92%	2.92%	2.91%	2.90%	0.61%	0.34%
Extracted POF_{c_n}	2.80%	2.53%	2.09%	2.30%	0.49%	0.36%
BRIDGES						
Predicted POF_{b_n}	1.14%	1.14%	1.13%	1.13%	0.21%	0.21%
Extracted POF_{b_n}	1.82%	1.53%	1.17%	1.13%	0.28%	0.16%

error of 26%) for all the filled layers (one through five), but is above the extracted POF for the partially filled layer six.

The predicted POF for cuts, on the other hand, seems to be consistently above the extracted value with an average error of 20% (we do not believe the small underestimate for layer six to be statistically significant). Further experiments will be needed to identify the source(s) of these errors and much work needs to be done in order to make the predictions more robust and reliable. However, the ability to estimate the effects of design changes such as wire pitch and width on yield offers a powerful incentive to make further progress.

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