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# Course Development in IC Manufacturing

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**Abstract**—Traditional curriculum in electrical engineering separates semiconductor processing courses from courses in circuit design. As a result, manufacturing topics involving yield management, and the study of random process variations impacting circuit behavior are usually vaguely treated. The subject matter of this paper is to report a course developed at Texas A&M University to compensate for the aforementioned shortcoming. This course attempts to link technological process and circuit design domains by emphasizing aspects such as process disturbance modeling, yield modeling, and defect-induced fault modeling. In a rapidly changing environment where high-end technologies are evolving towards submicron features and towards high transistor integration, these aspects are key factors to *design for manufacturability*. The paper presents the course's syllabus, a description of its main topics, and results on selected project assignments carried out during a normal academic semester.

## I. INTRODUCTION

**I**NTEGRATED CIRCUIT manufacturability has received a great deal of attention in the last years. As technological processes are advancing towards submicron resolution features—with higher transistor integration on silicon taking place—the need to foresee the ease and feasibility of fabrication of IC designs is becoming a must.

IC manufacturability is no longer a practice exclusively belonging to industry. Nowadays, it is a flourishing area of academic research in which systematic solutions are sought for yield related problems. This presents a dramatic departure from the previous practice of ad-hoc research to address such problems [16], [28]. The result of this interaction is the emergence of methodologies for yield and fault prediction taking into account existent manufacturing conditions [18]. It is important to emphasize “existent manufacturing conditions” because IC design can no longer be seen as a task using ideal nominal values, but instead as a task where process variations and manufacturing disturbances must be taken into account. Despite the emphasis placed in manufacturability, traditional academic curricula do not include special purpose courses in this field [2], [11]. In all likelihood, this stems from the fact that in common engineering practices IC design and semiconductor process technology are two distinct and isolated domains. Typically, the design engineer is more accustomed to, say, behavioral and electrical simulations while the process engineer delves into the physical and chemical components of the technological process. As a result, EE related courses are also separate domains. One has, for instance, all the courses pertaining to IC design, e.g. Digital and Analog IC Design,

VLSI Systems, Logic Synthesis, etc., and on the process domain we have courses such as Microelectronic Circuit Fabrication, Microelectronic Device Design, etc.

At Texas A&M University, to address this problem, the traditional separate areas of IC design and semiconductor technology have been integrated into a new graduate level course named *Special Topics in IC Manufacturability*. This course addresses the study of process and design variables to determine the ease and feasibility of fabrication—or manufacturability—of integrated circuits. The course is composed of four main sections: (1) basic semiconductor processing technology and related disturbances; (2) functional yield prediction; (3) layout defect-sensitivity analysis; and (4) manufacturing fault analysis/debugging.

Obviously, given the nature of the topics, some of them could be a course by itself—actually this would correspond to the previously mentioned separation of courses by domains. The purpose of *Special Topics in IC Manufacturability* is to link the four sections, e.g. to present the impact of process disturbances on the IC performance, to study feasibility of fabrication through yield prediction and estimation, and to present design for manufacturability techniques. As process technology and circuit design are still separate domains, a meet in the middle strategy is pursued, i.e. we strive for a compromise between theory and practice, as well as, extent of theoretical coverage. The use of CAD tools throughout the course is strongly emphasized. This is an important aspect in the learning process as it provides an almost “turnkey” solution to specific application domains. As progress is made during the course, time and resources can be dedicated to understand and to manage more complex and practical problems, rather than to put all efforts on small “classic” examples.

The four sections of the course present the student with practical issues normally applied in industry and usually required by quality, product, and design engineering departments. As a matter of fact, the course is a response to industry's continuous need for qualified engineers in manufacturing positions. Ideally, these engineers have knowledge in defect engineering, circuit design, testing, failure analysis, and are capable of coordinating and monitoring production activities to ensure the product meets functional and performance requirements. However, it is rarely seen that a recently graduated engineer possesses all this knowledge. Quite often industry must also incur inexpensive training programs.

Sections 2 and 3 cover curriculum development and project assignments, respectively; a list of course objectives, and some project results are also included in these sections. Finally,

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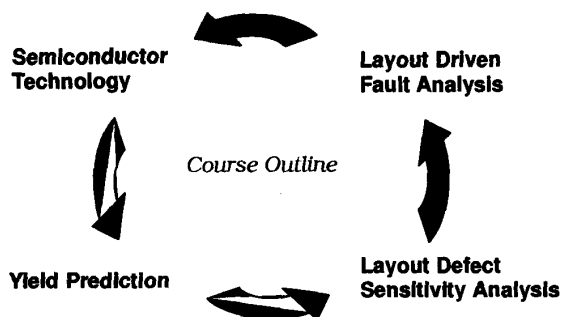


Fig. 1. Course outline.

## Syllabus

### Semiconductor Technology

- (1) Diffusion
- (2) Oxidation
- (2) Lithography
- (1) Implantation and Annealing
- (1) Etching and deposition
- (1) NMOS technology and typical control parameter values
- (1) CMOS technology and typical control parameter values
- (2) Acceptability regions
- (2) Process disturbances
- (1) Experiment planning
- (1) Project evaluation

### Functional Yield Prediction

- (1) Yield economics, manufacturability, and design strategies
- (1) Binomial and Poisson yield models
- (1) Defect density variations and statistics
- (1) Compound Poisson statistics
- (2) Negative Binomial yield model
- (1) Small area clustering
- (1) Practical examples
- (1) Redundancy and partially good chips
- (1) Project evaluation

### Layout Defect-Sensitivity

- (1) Spot defects and their size distributions
- (2) Probabilistic analysis of primitive faults (bridges, cuts)
- (2) Susceptible sites
- (3) Single-layer critical areas
- (2) Yield prediction based on critical area extraction
- (1) Project evaluation

### Layout Driven Fault Analysis

- (2) Technology and defect semantics
- (2) Defect-Fault relationships
- (2) Multiple-layer critical areas
- (2) Realistic Fault Extraction
- (1) Project evaluation

(x)-number of hours  
Total number of hours: 45

Fig. 2. Course syllabus.

a summary and discussion of achievements is presented in Section 4.

## II. COURSE DEVELOPMENT

The course is composed of four tightly coupled sections as illustrated in Fig. 1. The idea behind this structure is

## Semiconductor Processing

- (1) Understand the basic steps of semiconductor processing
- (2) Understand the role of control parameters in each process step
- (3) Design, construct and characterize an MOS technology
- (4) Understand the nature of process disturbances
- (5) Identify, relate and differentiate regions of acceptability in the design and process spaces
- (6) Identify and solve Design-Miscentering problems in real applications
- (7) Identify and solve Oversensitivity problems in real applications
- (8) Use CAD tools for statistical process and circuit simulations
- (9) Design statistical experiments
- (10) Optimize Parametric Yield from a process and circuit approach

Fig. 3. Course objectives for section "Semiconductor Technologies."

## Yield Analysis

- (1) Determine IC manufacturability, profitability, and design strategy of real applications through yield analysis
- (2) Identify, relate and derive yield models, e.g. Binomial, Poisson, Negative Binomial, Seeds, Dingwall, etc.
- (3) Understand the effects of defect clustering and defect density variations (inter and intra wafer) on yield modeling
- (4) Understand and identify the change of shape of the p.d.f. of defect densities to justify the use of Compound Poisson statistics
- (5) Use Compound Poisson statistics for yield modeling; identify different compounders, e.g. Gamma, delta, exponential, triangular, and rectangular to model the distribution of defects.
- (6) Compute and fit manufacturing yield to yield models in real applications
- (7) Apply the Negative Binomial model to predict yield of large area chips of real applications
- (8) Compute and predict the yield of partially good chips in real applications
- (9) Compute and predict levels of redundancy for yield optimization in real applications

Fig. 4. Course objectives for section "Functional Yield Prediction."

that in order to predict yield it is necessary to understand the underlying theory of *semiconductor technologies*, their process variations and manufacturing disturbances. However, estimating *yield* through a formula is not always sufficient, especially when the reasons of yield loss need to be inferred. Thus, rather than considering the IC just as a "black box," the geometrical properties of the IC are also taken into account. Consequently, advanced "design oriented" yield models based on manufacturing conditions and on the *defect tolerance of the IC layout* must be understood as well. Finally, inferring the reasons of yield loss is closely related to an extraction of defect induced faults. This can be accomplished using techniques such as *inductive fault analysis* and *multilayer critical areas analysis* in which it is also necessary (for the student) to have a solid basis in semiconductor technology/processing.

Although the semiconductor technology section might look straightforward for a student with a solid-state electronics

## Defect Sensitivity Verification

- (1) Differentiate between local and global defects. List their kinds, e.g. spot defects, misalignments, etc
- (2) List the types of spot defects: protrusion, intrusions, and isolated spots. Understand the effect of spot defects in real circuit designs
- (3) Identify and create necessary conditions for the occurrence of bridges and cuts in IC patterns taking into account local and global defects
- (4) Understand the concepts of "critical area" and "failure criterion"
- (5) Identify and extract susceptible sites from real layouts
- (6) Identify and extract critical regions from real layouts
- (7) Compute critical areas
- (8) Determine and use different defect size distributions to characterize manufacturing line conditions
- (9) Understand the concepts of defect-sensitivity and layout probability of failure
- (10) Relate yield and defect-sensitivity
- (11) Use CAD tools for critical area extraction and yield prediction. Evaluate real layouts according to their defect-sensitivity and manufacturing line conditions

Fig. 5. Course objectives for section "Layout Defect-Sensitivity Analysis."

background, the study of process and manufacturing disturbances on layout and circuit designs is not. The same applies for a student with a circuits and systems background who might be more familiar with circuit techniques but not with semiconductor technology development and its implications on VLSI designs. Naturally, to accommodate the variety of backgrounds, some prerequisites for the course have to be imposed. They are: at least one (under) graduate course in probability and statistics, and one (under) graduate course in VLSI design, or being registered therein—this freedom can allow us to offer the course at an undergraduate senior level or at a graduate junior level. The prerequisite course in probability and statistics is necessary for understanding the concepts managed in the yield prediction section. Similarly, a basic course on VLSI design is necessary for understanding the implications of process parameters, and for creating and interpreting real layouts.

Fig. 2 shows the syllabus. Notice that one hour of project reviews is planned at the end of every section. This is because the grading procedure is on a project basis—one project for each course's topic above mentioned. The projects are an essential part as they address practical problems. Rather than assigning short term homework, projects for 2–3 week time periods are given in parallel with the development of the course. This strategy allows students to actually put their hands on practical problems applying the theory covered in class, and frequently making use of CAD tools. Hence, this special session is meant to discuss methods, results, and "what if" situations of the project.

At the present time, there is not one textbook which actually fulfils all the requirements of this course. The recommended material include instructor's notes, diverse journal papers, and several research monographs [6], [17] [23], [29], [30]. From a pedagogical perspective it is very important to fix a

## Manufacturing Fault Debugging

- (1) Understand the concept of Inductive Fault Analysis. Create semantics for microelectronic technologies. Identify multi-layer conditions to analyze the origins of defect induced primitive faults, i.e. bridges, cuts, and piles.
- (2) Identify and create multi-layer susceptible sites in real layouts
- (3) Understand and use the concept of multi-layer failure criterion and sensitivity factors for each kind of spot defect
- (4) Identify and extract multi-layer critical regions from real layouts
- (5) Compute multi-layer critical areas
- (6) Create "defect induced faults" semantics for a given technology. Extract a realistic set of faults from real layouts. Rank the likelihood of occurrence of each fault according to its multi-layer critical area.
- (7) Obtain the likelihood of occurrence of each fault according to the manufacturing conditions using  $M_{sens}$ ,  $M_{size}$ , and  $M_{dens}$  measures.
- (8) Measure the likelihood of failure of each electrical node in a design using  $M_{sens}$ ,  $M_{size}$ , and  $M_{dens}$ .

Fig. 6. Course objectives for section "Manufacturing Fault Analysis."

set of learning goals, e.g. topics that students should master [12]. These objectives are shown later in the context of this presentation. The remainder of this section is dedicated to describe in more detail each one of the four areas of the course.

### A. Semiconductor Technology

Section 1, "Semiconductor Technology," is aimed at familiarizing students with the silicon layer structure of MOS technologies, the basic semiconductor process steps and each of their parameters. The class work covers topics on process models such as diffusion, oxidation, implantation, and lithography. Almost immediately after the beginning of the course, a project concerned with the development of an MOS technology using the statistical process simulator FABRICS and the Process Engineer Workbench is assigned [13], [14]. These tools were chosen instead of the more traditional tools such as SUPREME [1] because they are more interactive, offer visualization of cross-sections, and allow to input process disturbances to simulate a real manufacturing environment.

Technology development is taught in class using the simulator PED and following the outlines provided in the "Atlas of IC Technologies" [17]. This strategy allows to have interactive sessions in which doping profiles, oxide thickness, resist thickness, cross sections of the IC, etc., are easily checked to prove the correctness of the chosen process parameters. In this way, students learn typical process parameter values, understand the practical applications of the process models covered in class, and have a clear idea of typical values for layer thickness, pattern widths, 3D physical structure, etc. Maly's "Atlas of IC Technologies" is an excellent didactical vehicle in this respect.

Once the technology is mastered, the second topic in this section is parametric manufacturability. Concepts such as local and global defects are introduced, and the foundations for modeling random phenomena in semiconductor technologies are laid down. Hierarchical models for simulating process

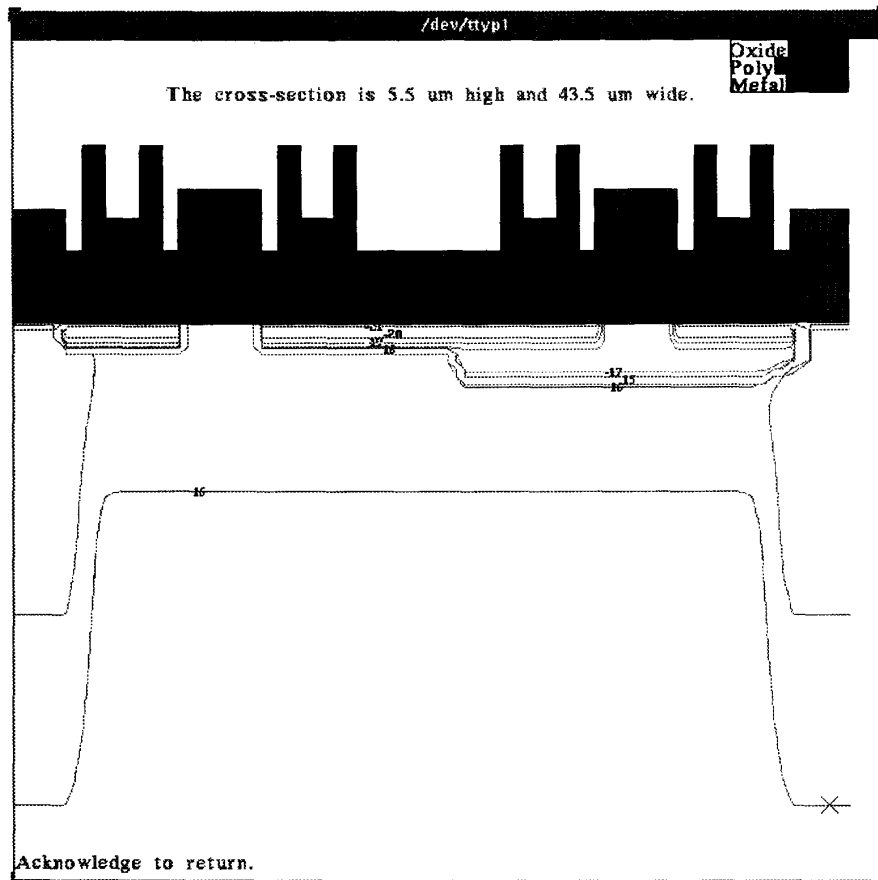


Fig. 7. Cross section of an NMOS IC developed with PED.

disturbances across chips, wafers, and wafer batches are presented, and intuitive concepts such as acceptability regions, manufacturing yield, probe yield, test yield, etc. are introduced as well [6]. These concepts serve as a preamble to analyze problems such as design miscentering and oversensitivity. A 2-level-factorial experiment planning is introduced as a means to capture systematically the effect of process variations on the output response of a circuit design. The list of objectives for this section of the course is shown in Fig. 3.

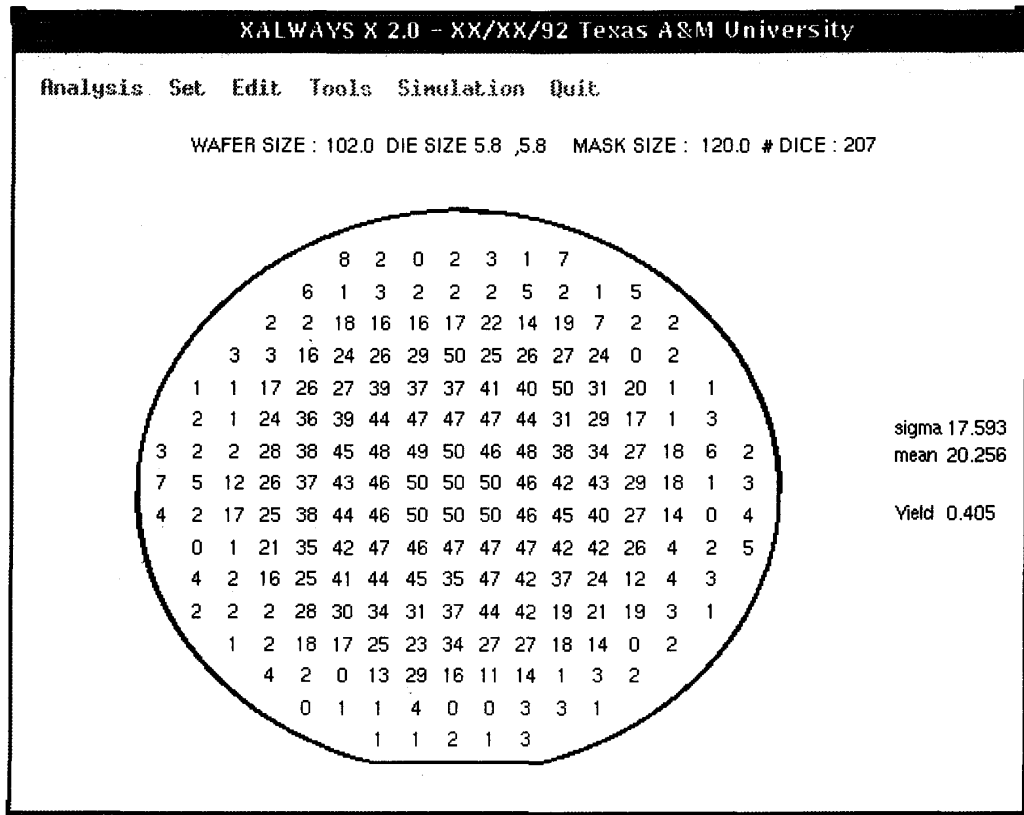
#### B. Functional Yield Prediction

Before developing yield formulae, a section on yield economics is covered in class. Several trade offs among level of integration, yield, profitability and technological costs are studied. By doing so, the important implications of predicting yield are highlighted in order to choose strategies for manufacturing profitable ICs. The situation in which a chip of, say,  $5 \times 10^6$  transistors and imaginary die size of  $1 \text{ cm}^2$ , fabricated relatively easily using today's gamut of layout synthesis tools is posed. Yet, careful judgement has to be exercised in fabricating this chip because its yield might be very low if not zero—a fact which can make it not feasible

to manufacture. The list of objectives correspondent to this section of the course is shown in Fig. 4.

The course moves on to cover the formulae evolution of yield prediction, beginning with binomial models, passing through Poisson statistics to the ultimate model the negative binomial formula [4], [24]. Broadly speaking, binomial models assume that the distribution of defects on the wafer is uniform, and that the number of defects is known. Neither of the two assumptions is completely correct, therefore Compound Poisson statistics were used to produce a more accurate model. Modeling the distribution of defects through the Gamma distribution leads to the negative binomial yield model. This model allows one to fit data by using a statistical parameter which describes the levels of defect clustering on the wafer. Environmental manufacturing conditions such as wafer to wafer and within wafer defect density variations [26] are formally presented through an analysis of p.d.f. of defect densities as a function of the chip area. This analysis serves as a basis to study Compound Poisson statistics which permits to capture the defect density variations aforementioned [19].

Two methods to obtain the negative binomial formula are covered in class, one is based on the use of Compound Poisson Statistics and the other on the analysis of small area clusters



(a)

Fig. 8. Wafer map analysis using XALWAYS: (a) history map.

[24]. The former method is used to highlight the effect of defect density variations; the latter one to study the effect of defect clustering in semiconductor technologies.

Today's levels of integration often require the use of redundancy, especially in highly structured designs such as RAMs. Therefore the course also includes a section on IC redundancy and partially good chips [27].

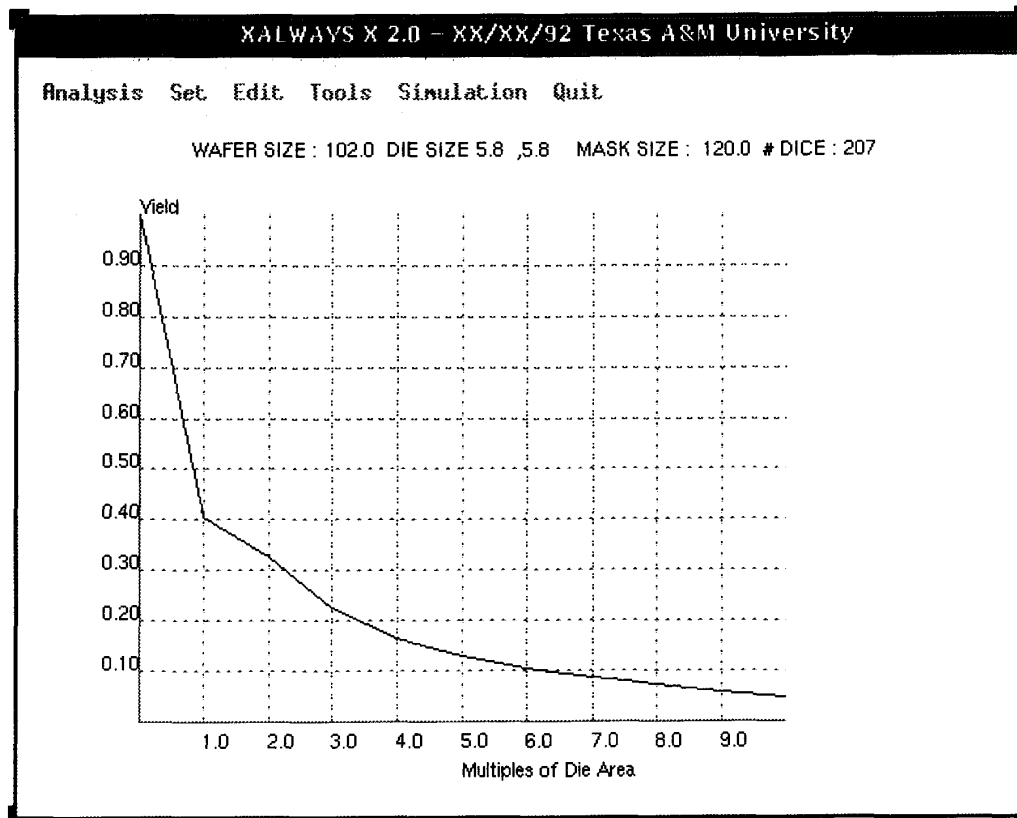
Although this section of the course is very theoretical, students put their knowledge into practice on the assigned project. There, they are asked to compare different yield formulae and to effectively apply each one of the models. One of the practical aspects in the project is to partition the wafer into small windows to fit yield data to the negative binomial model. The project uses the CAD tool XAlways for yield analysis [21]. This is an interactive tool for the analysis of yield information that makes use of graphical displays in the form of wafer maps to represent the spatial distribution of functional dice on the wafer. It offers facilities to obtain radial and angular yield analyses, wafer map yield analysis, etc.

### C. Layout Defect-Sensitivity Analysis

It is in this section of the course where semiconductor process and circuit design are linked. Yield formulae devel-

oped in the previous section are applied to real IC layouts to evaluate their defect-tolerance. The notion of spot defects as random phenomena characterized by a stochastic defect size distribution and a stochastic spatial distribution on wafers is introduced first. Next, a classification of various defect mechanisms such as protrusions and intrusions in different IC layers is presented to study their effects on their same layer of origin and on some other layers [15].

An important phase in "design oriented yield prediction and estimation" is critical area analysis [25]. Roughly speaking, a critical area is the area within which the center of a defect must fall in order to introduce a hard fault in the IC. A critical area analysis captures the "weak" regions of a design in the presence of spot defects. In other words, the critical area analysis essentially answers the question: "What is the likelihood that a bridge or a broken pattern will occur in the design assuming that a defect of radius  $r$  is present?" The course presents the conditions to create bridges and faults in the presence of global disturbances and spot defects [3]. Actually, these conditions are aimed as an introduction to the critical area analysis. Following this, a geometrical method for the extraction of single layer critical areas is covered. This latter method starts by extracting susceptible sites, defined as the places where a defect may potentially damage the



(b)

Fig. 8. (continued) Wafer map analysis using XALWAYS: (b) yield versus area.

functionality of the IC, and then goes over to the extraction of critical areas based on a deterministic algorithm [21] (see list of objectives in Fig. 5).

After the geometrical method is completed, the course links the critical area analysis with the manufacturing conditions. To this extent, the concept of defect-sensitivity is introduced, and several analytical defect size distributions are studied in conjunction with analytical yield formulae [8], [9]. As a result, a "design oriented" yield prediction methodology is developed which takes into account the layout, the process, and the environmental conditions of the manufacturing line. Several CAD tools are available for layout analysis [7], [21], [30]. We are currently using XLaser which is a tool used to extract critical regions from complex IC layouts [21]. The tool offers on-line visualization of critical regions, and also allows one to create interactive sessions for yield analysis tailoring the defect density and defect size distributions according to the user's needs.

#### D. Fault Debugging and Analysis

With the presentation of single-layer critical areas it is easy to extend the concepts to a multilayer approach. A multilayer approach is advantageous because it is possible to map the geometrical interaction between defect and layers

to a more comprehensive electrical level [10]. This in turn corresponds to a realistic extraction of defect induced faults. The course begins by highlighting the advantages of inductive fault analysis over traditional testing methods [7]. Emphasis is made on the fact that with this kind of analysis the simulation of all theoretically possible faults is avoided and that the simulation is carried out only on those faults that are likely to occur. Several methods are discussed for fault extraction, namely a Monte Carlo approach [30], an analytical approach [3], and a deterministic one [21] (see list of objectives in Fig. 6 for more details).

The foundations of technology and defect semantics are explained prior to going into the topic of multilayer critical area analysis. These semantics basically instruct the student on how to construct state clauses for each silicon layer structure of the technology, e.g. how to describe symbolically a metal-poly via, an enhancement transistor, a diffusion track, etc. Defects effecting silicon layer structures are also abstracted by constructing state clauses. With this preparation, students are able to set the conditions for primitive faults likely to occur in the technology disregarding the specifics of the IC layout. The Monte Carlo yield simulator VLASIC [30] is used for manufacturing fault analysis. It offers facilities such as to extract a list of faults based on the environmental conditions

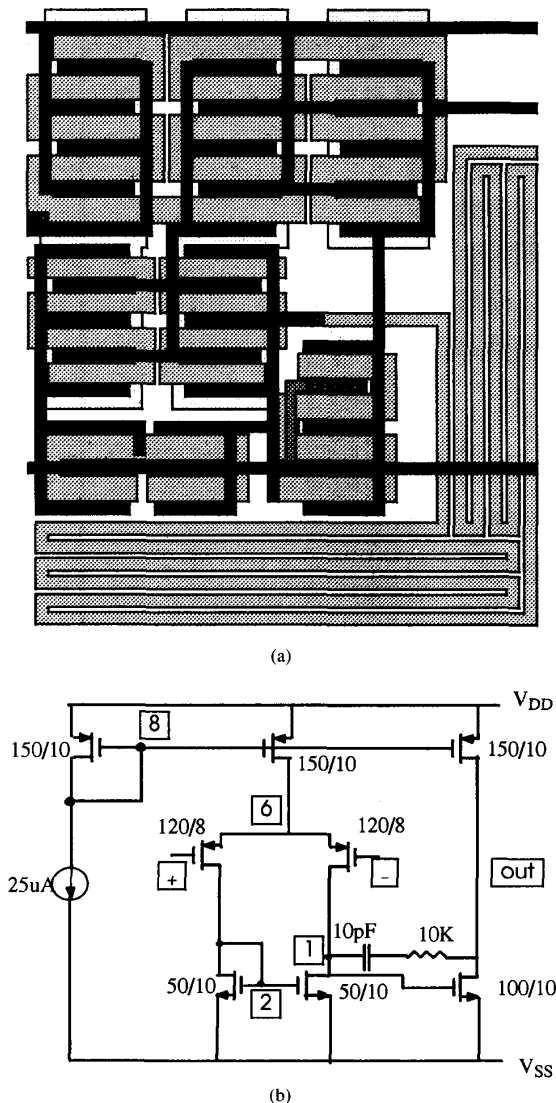


Fig. 9. Externally compensated operational amplifier: (a) layout; (b) circuit.

of the manufacturing line in order to analyze the functional yield of the design.

### III. PROJECT ASSIGNMENTS AND SOME RESULTS

**Project 1 "Semiconductor Technology Modeling":** The objective of this project is to familiarize students with processing aspects like temperatures, process rates, negative/positive lithography, doping concentration, etc. typical in semiconductor technologies. The process simulator PED is employed to create the technology and FABRICS to characterize the outcome. The particular assignment consists in developing an NMOS technology following the outline described in Sze [29]. Fig. 7 shows the steps and cross section obtained by one of the teams.

The learning goals involved in this project are to: (1) qualify the effect of a given process step on its corresponding MOS

electrical parameter; (2) quantify the use of control parameters such as dose and energy for ion implantation, temperatures and times for oxidation, etc.; and (4) identify which process outcomes are more likely to change as a result of processing other steps.

The second part of the project consists of characterizing the effect of process disturbances on the performance of an IC such as a two-stage Operational Amplifier. The learning goals of this part of the project are to: (1) quantify the percentage of process variation that has a negative impact on the design; (2) identify "design miscentering" or "oversensitivity" problems; and (3) develop experiment plans and to quantify the tolerance of the circuit to process variations.

**Project 2 "Functional Yield Modeling":** The goals of this project are to: (1) fit a given manufacturing yield to the Poisson and negative binomial models; (2) compare the effectiveness of both models; (3) make yield predictions based on a given manufacturing yield trend; and (4) carry out a cost analysis to study the feasibility of the product.

The central goal of the project is to determine the economical and technological feasibility of a new product based on cumulative wafer maps and on cost equations. As a particular case study, it is assumed that the wafer's chips are 16MB DRAMS occupying  $1 \text{ cm}^2$  of area, and that the current defect density is  $1 \text{ defect/cm}^2$ . The yield prediction is meant to study the feasibility of fabrication of 64 MB chips using the same technology and resolution features of the 16 MB product. Fig. 8(a) shows one cumulative wafer map in Xalways, and Fig. 8(b) a yield versus area curve extracted from this wafer map.

This project is very comprehensive. For instance, to be able to fit the manufacturing yield to the negative binomial model, students have to learn how to apply the windowing technique, and also have to solve non linear equations to fit data to the manufacturing yield. One interesting aspect involved in the negative binomial model is to be able to interpret the value obtained for the clustering parameter in terms of defect clustering by observing the actual wafers.

**Project 3 "Critical Area Analysis":** The objective of this project is to find an optimal set of design rules that will maximize yield. For this experiment, a layout with minimum resolution features, as compact as possible, has to be created. Yield maximization through design rule adjustment is then made possible by relaxing the pattern widths and spaces, i.e. by widening patterns and by increasing spaces among patterns. Naturally, the defect sensitivity is minimized by relaxing the initial design rules, however, it is questionable how much relaxation is optimal. To quantify this optimization, it is necessary to combine the defect-sensitivity with the environmental conditions of the fab line. The defect sensitivity analysis is carried out using XLaser which is a CAD tool to extract single layer critical areas and to predict layout yield.

Yield always increases when the design rule spacings and widths increase. Apparently this is a contradiction to the axiom "the larger the area the smaller the yield". However, yield can be improved by either reducing the layout probability of failure, or by reducing the IC area, or both, without altering the manufacturing conditions (defect size and defect density). This aspect is widely treated in the project. Similarly, students are



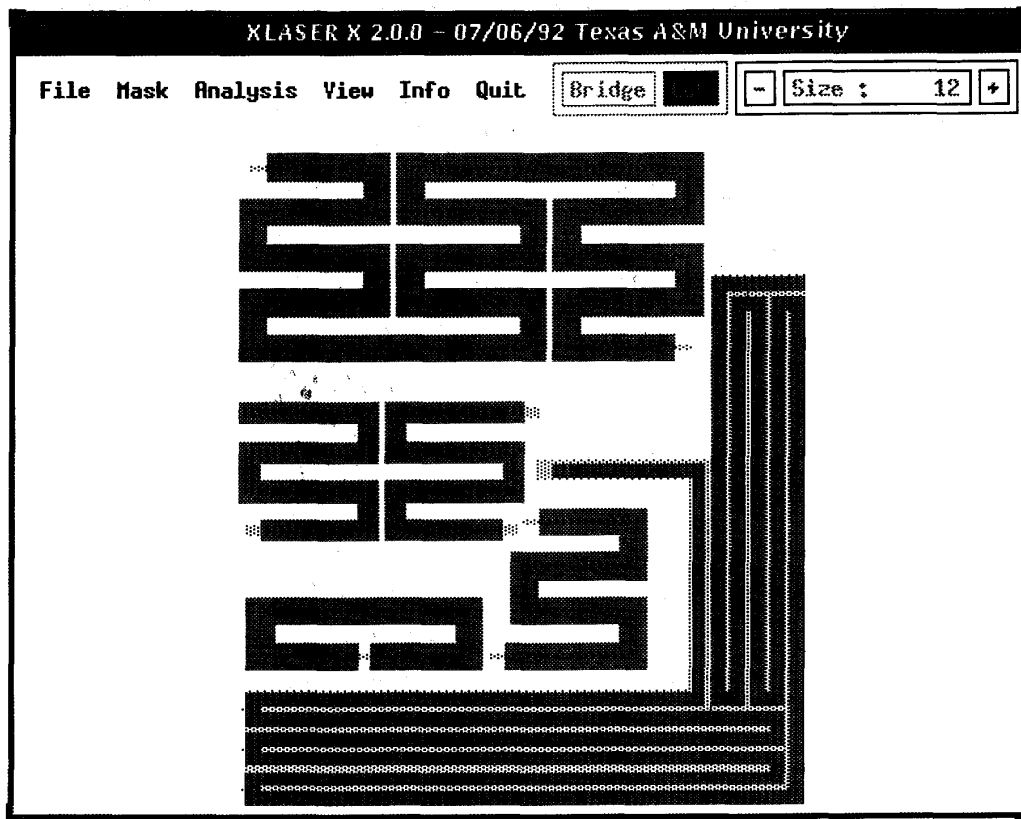


Fig. 10. Critical areas analysis using XLaser. The critical areas are for a defect of  $12\ \mu\text{m}$  in the poly layer.

also questioned on the effect that manufacturing conditions have on the layout. For instance, to qualify and to quantify distinct defect size distributions, to study the distribution's physical nature versus its corresponding analytical model, and to investigate the defect size distribution's impact on the IC layout.

The project leads the student to draw conclusions on design for manufacturability using design rule scaling laws. Trade offs such as scaling down imply less area, larger integration, but at the same time higher risk of having faults. The objective of this project is to find a good compromise between design rules, defect size and density distributions, and chip area. Fig. 9 shows the schematic diagram and layout of the Op Amp seen in class, Fig. 10 illustrates the use of the critical area extractor XLaser, and Fig. 11 shows the optimized design rules for minimum width and minimum spacing among patterns.

**Project 4 "Fault Analysis":** The concepts of inductive fault analysis and multilayer critical regions are put in practice in this project. The assignment consists of: (1) creating a simple layout; (2) extracting the realistic set of faults; (3) weighting the faults; and (4) redoing the layout to minimize the probability of failure. Minimizing a design's risk of failure is still an ad-hoc problem, however, through this project some guidelines are used. For instance, a spectrum with the likelihood of failure for each node is used to discover which nodes are less fault-tolerant [5]. Using this index, a

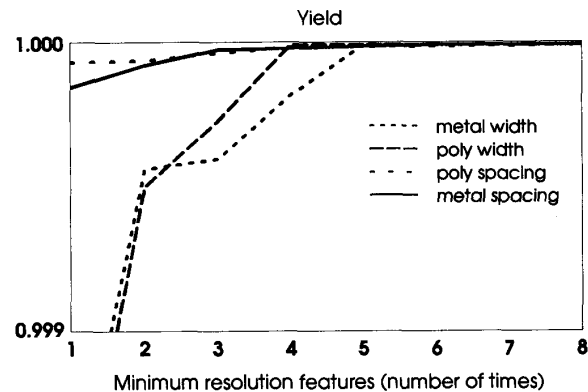


Fig. 11. Yield optimization by design rule relaxation.

second level in the minimization hierarchy is to extract the faults related to the node of interest which are more likely to occur. This fault extraction/weighting is carried out through a multilayer critical area analysis. Finally, the layout is modified and a new spectrum can be created. This procedure is repeated until the desired defect-tolerance is achieved. Fig. 12 shows some multilayer critical areas, and Fig. 13 shows the likelihood of failure for the layout of Fig. 9 before and after scaling it down by a factor of two.

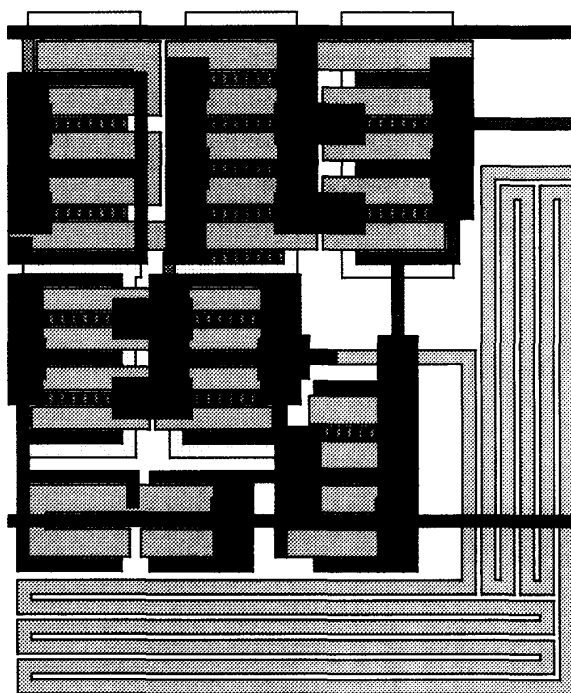


Fig. 12. Multilayer critical areas for a missing thick oxide defect of 5  $\mu\text{m}$ .

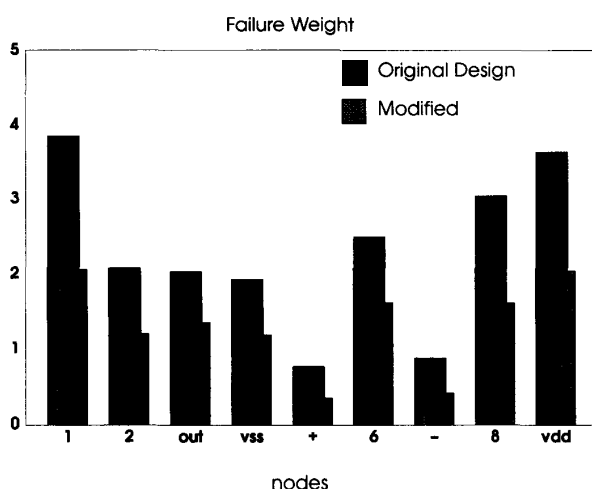


Fig. 13. Circuit design optimization. The histogram shows the likelihood of failure of each of the design's nodes before and after optimization.

#### IV. CONCLUSION

A course on IC manufacturability has been presented in this paper. This course is aimed at providing the student with fundamentals on yield prediction, and at studying the feasibility of fabrication of ICs. The course makes use of a "meet in the middle" strategy in order to link both semiconductor processing and circuit design domains. This strategy is actually a compromise between pure theoretical knowledge and practical issues. For instance, rather than covering vast theoretical material on semiconductor processing, emphasis is

placed on typical parameter values and methods that will allow the student to develop, and understand, a technology with the help of a process simulator. In a similar way, rather than covering pure circuit design and system architecture aspects in the design phase of an IC, practical aspects in design for manufacturability are highlighted, e.g. critical area extraction and inductive fault analysis.

Both processing and circuit domains are related in this course through the study of yield prediction and estimation. Emphasis is made on methods using analytical formulae and product dependent data (layout) to have accurate yield predictions. This, of course, involves topics in statistical characterization of the manufacturing line in terms of defect conditions. Practical aspects such as characterization of defect size distributions and defect density variations are covered in class.

This course is certainly not ultimate, it is meant to serve as an introduction to manufacturing issues from a circuit and process point of view. While the course is functional, more work is needed to develop a complete curriculum in manufacturing covering formal aspects of yield and testability. Usually, manufacturing courses are related to issues in quality control and originate mostly from an industrial engineering perspective. This course departs from this tradition by giving attention to electrical engineering aspects and by involving students with the use of CAD tools. In fact, it was seen that an important component in this course was the use of CAD tools. These tools give the students the ability to work in different areas without having to be experts in each of these. The techniques enable novice students to grasp complex issues such as extraction of manufacturing yield and wafer yield management, or the extraction of critical areas and realistic sets of faults. For those interested, XAlways and Xlaser may be obtained directly from the author.

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