An 11b pipeline ADC with dual sampling technique for converting multi-carrier signals

An 11b pipeline ADC with dual sampling technique for converting multi-carrier signals

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***Abstract*—This paper presents a dual sampling technique for analog-to-digital converters (ADCs) to convert multi-carrier signals more efficiently and proposes an 11b switched-capacitor pipeline ADC based on this technique. With the dual sampling technique, the input signal power of the ADC can be boosted without getting excessive clipping noise and the ADC can have a higher resolution over the critical low amplitude region. Hence the overall signal to thermal, quantization and clipping noise ratio is improved. The 11b pipeline ADC with the proposed technique achieves a wide input signal range of 2Vppd using a single 1.2V supply. Simulations show an improvement of about 5dB in SNDR and better than 10dB in MTPR compared to a conventional 11b ADC for converting multi-carrier signals.**

Keywords: analog-to-digital converters, pipeline ADC, multi-carrier signals, dual sampling technique

I. INTRODUCTION

The trend of achieving higher data throughput in both wired and wireless communication systems results in more and more demanding specifications on analog-to-digital converters (ADCs) in terms of sampling speed and resolution. Generally speaking, the power needed for an ADC to perform conversion increases linearly with sampling speed and exponentially with accuracy [1]. For conventional ADCs, the signal is "blindly" converted without any consideration of its statistical property, while theoretical studies show that optimal ADCs can be designed for the given signal statistics [2] [3]. Since many popular systems with high data rate (e.g. ADSL, WLAN, WiMAX, DVB-T) adopt multi-carrier transmission schemes and a high number of signal levels in the sub-carriers to increase spectral efficiency, there is opportunity to optimize ADCs for these systems. By exploiting the statistical properties of the signal, ADCs can be designed wisely to reduce the power consumption and implementation complexity while achieving a similar system performance.

In this paper, we introduce a dual sampling technique for ADCs to convert multi-carrier signals with high crest factor more efficiently and propose an 11b switched-capacitor pipeline ADC based on this technique. The dual sampling technique enables the ADC to have a wide input range which has a lot of advantages [4] [5] [6] and a better overall signal to thermal, quantization and clipping noise ratio compared to conventional ADCs with same resolution. This paper is organized as follows. Section II analyzes the statistical properties of multi-carrier signals and their impact on ADCs, and explains the principle and advantages of the proposed dual sampling technique. Section III describes the architecture of the proposed 11b pipeline ADC and its circuit implementation. Simulation results are provided in section IV and section V summarizes and concludes this paper.

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II. SIGNAL CHARACTERIZATION AND DUAL SAMPLING TECHNIQUE

A. *ADC input signal characterization*

Systems adopting multi-carrier transmission schemes have many advantages, including high spectral efficiency and ability to cope with severe channel conditions. But one undesirable property of these schemes is that their transmitted signal in time domain is observed to have large "peaks" when compared to their average power value. This is characterized by the crest factor (CF). This undesirable property requires ADCs to have a higher dynamic range in order to cope with the requirement of having a small probability of clipping events. Fig. 1 shows a section of a multi-carrier signal in time domain and its probability distribution function (pdf). Since the signal is a summation of a large number of narrowband signals with uncorrelated amplitude and phase, the resulting signal amplitude distribution is approaching a Gaussian distribution according to the Central Limit Theorem. In Fig. 1, it is clearly shown that the characteristics of a multi-carrier signal are far different from that of a single, full scale sinusoid signal.

In order to convert a multi-carrier signal with large crest factor properly, both quantization and clipping effects have to be carefully considered. Too much gain in the receiving front-

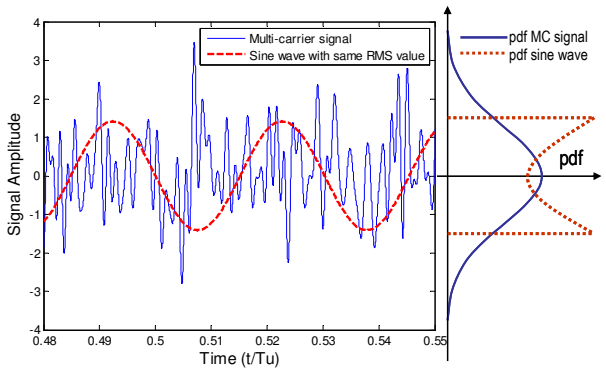


Figure 1. Multi-carrier signal versus single carrier signal in time domain and their amplitude probability distributions (pdf)

end will saturate the ADC and clip the signal, while insufficient gain will result in higher quantization noise with respect to signal power. Conventionally, a best compromise of clipping noise and quantization was found by backing off the input signal power by a large factor from the ADC full scale power level (e.g. 10dB power back-off for clipping probability less than 10^{-3}), in order to achieve an optimal signal to quantization and clipping noise ratio (SQCNR) [7]. For signals with large crest factors, this method leads to very inefficient use of the ADC's dynamic range and power.

B. *Principle of the dual sampling technique*

The principle of the proposed dual sampling technique is shown in Fig. 2. The input signal is split into a main signal and an auxiliary signal which is an attenuated version of the main signal. These two signals are sampled at the same time. Depending on the input signal level, one of them will be chosen to reconstruct the signal in the digital domain. The criterion is such that the signal in the main path is maximized to exploit the dynamic range of the quantizer efficiently and have more resolution over the main part of the signal range, while the auxiliary signal path provides coarsely quantized samples to replace the samples of the main signal that are clipped by the quantizer, hence avoiding excessive clipping noise. The sampled main signal has a better signal to quantization noise ratio (SQNR) while the sampled auxiliary signal has a better signal to clipping noise ratio (SCNR). When the signal is reconstructed properly in the digital domain, it has a better SQCNR compared to the one with the conventional method.

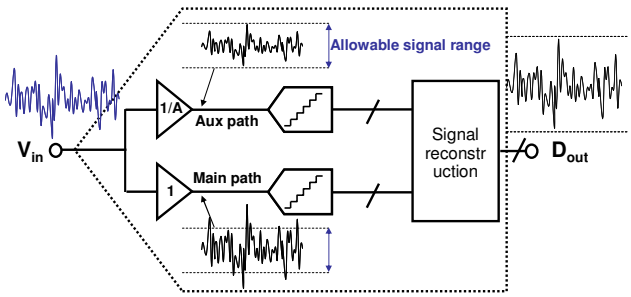


Figure 2. Block diagram of a ADC with the dual sampling technique

C. *Advantages of the dual sampling technique*

The SQCNR of ADCs with and without the dual sampling technique are

$$SQCNR_{conventional\_ADC} = \frac{P_{signal\_conventional}}{prob(x)\cdot n_{quant} + [1-prob(x)]\cdot n_{clip}} \quad (1)$$

$$SQCNR_{proposed\_ADC} = \frac{P_{signal\_proposed}}{prob_1(x)\cdot n_{quant1} + prob_2(x)\cdot n_{quant2} + [1-prob_1(x)-prob_2(x)]\cdot n_{clip}} \quad (2)$$

Where $P_{signal\text{-}proposed}$ and $P_{signal\text{-}conventonial}$ are the effective signal power of ADC with and without the dual sampling technique respectively; $prob_n(x)$ is the probability of the input signal within the allowable ADC input range; $n_{quant.}$ and n_{clip} are the quantization and clipping noise power respectively .

For signals with known statistical properties, optimal SQCNR for ADCs with and without the dual sampling technique can be found from Eq. (1) and (2). In order to make the analysis more clear, a comparison of the SQCNR of 11b ADCs with and without this technique is shown in Fig. 3. In this figure, the SQCNR versus input signal power is plotted. By properly choosing the attenuation factor (A) of the auxiliary signal path, the SQCNR of an ADC with the dual sampling technique can be substantially improved compared to the one without this technique. This observation is also valid for ADCs with arbitrary number of bits. Using ADCs with lower resolution to achieve a required system performance instead of higher resolution ADCs is much more power efficient, since generally power consumption of ADCs increases exponentially with resolution.

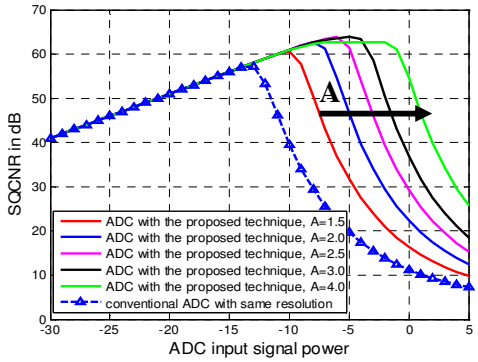


Figure 3. SQCNR versus input signal power (input signal amplitude Gaussian distributed and A is the attenuation factor of the aux signal path)

Besides better SQCNR, another advantage of this technique is that the ADC input signal power is boosted. Hence it allows a higher amount of thermal noise for a given signal to thermal noise ratio (STNR) which reduces the kT/C noise limitation in determining the capacitor size. In Fig. 3, it is shown that the ADC with the proposed technique at optimal SQCNR setting allows about twice the input signal swing compared to the conventional one, which can be translated to a four times reduction of the capacitors (in case not limited by matching) for a certain STNR, and a similar reduction of the power consumption.

III. PROPOSED 11B PIPELINE ADC WITH DUAL SAMPLING TECHNIQUE

A. *Proposed ADC architecture*

A general block diagram of a pipeline ADC is shown in Fig. 4. It consists of N cascaded stages in which each of them performs sample-and-hold, a coarse quantization, subtraction and amplification of the residue signal. The dual sampling technique is implemented in the first stage of the pipeline ADC. As shown in the bottom of Fig. 4, in this stage, there are two signal paths each consisting two signal scaling blocks and a passive sampling network, a detection block (a sub-ADC), a channel selection block (MUX), a subtraction and an amplification block. By doing an adaptive channel selection through MUX according to the input signal level, the residue

signal is maintained within the allowable output signal range of the amplifier. Therefore the stage's allowable input and output signal swing is decoupled. The backend pipeline stages are just conventional 1.5b stages and in total provide 10b resolution. In this design, the first stage is not preceded by a dedicated SHA, it is merged with the front-end sampling networks to reduce power consumption and achieve a larger input range.

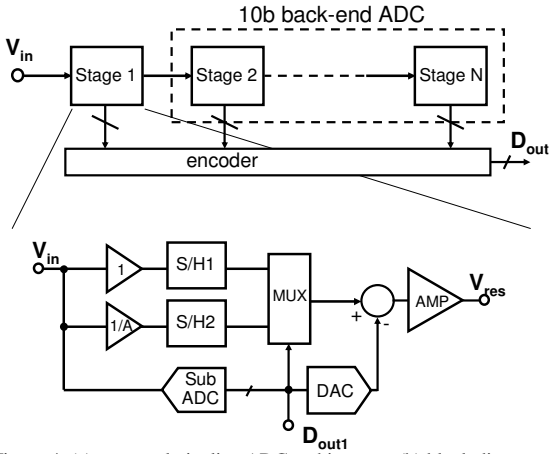


Figure 4. (a) a general pipeline ADC architecture; (b) block diagram of the first pipelined stage with dual sampling technique

B. *Ciruit implementation and operation*

The first stage is an improvement over the basic 1.5b pipeline architecture [8], incorporating the proposed dual sampling technique. In Fig. 5, a schematic representation of the first stage and its timing diagram are shown. Although it is designed and implemented as fully differential circuits, a single-ended version is shown for clarity. The signal scaling blocks are designed simply as resistor ladders. The resistor ladder in the auxiliary channel attenuates the input signal swing by a factor of 2.5 (an attenuation factor chosen for achieving a close to optimal SQCNR), while the one in the main channel keeps it unattenuated. The RC time constants in these two channels are designed to be the same to make sure that the bandwidth of the two channels match. The sampling networks are flip-around type switched-capacitor circuits, implementing the algorithms in Eq. (3). The OTA in this stage uses a folded cascode with gain boosting configuration which is similar to the one in [9].

During Φ_1, the signal is tracking by the sampling capacitors in both channels and the four-level flash ADC. At the falling edge of Φ_{1e}, the signal is sampled onto these sampling capacitors. Then at the rising edge of Φ_{latch}, the four-level flash ADC detects the signal level (4 decision levels and 5 possible output codes). After the decision is made, proper reference voltages (±Vref or Vcm) are chosen and connected to the sampling node of the capacitor for subtraction. At the same time, the sampling network (main or auxiliary) that holds the sample within the allowable range is connected through MUX to the output of the OTA for further conversion. The overall transfer function is shown in Eq. (3) and its input-output transfer curve in Fig. 6. Fig. 6b shows that the proposed stage

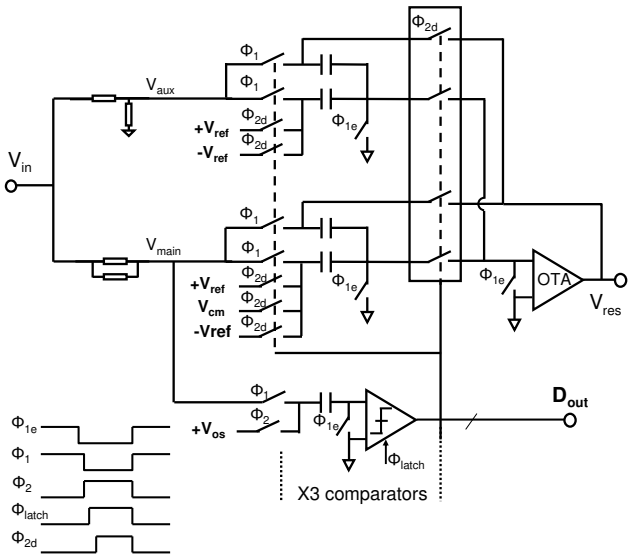
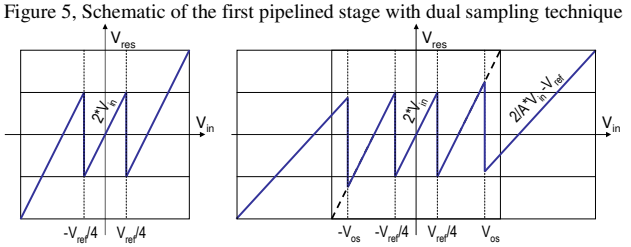


Figure 5, Schematic of the first pipelined stage with dual sampling technique



(a) (b)

Figure 6, (a) input-output transfer curve of a conventional 1.5b stage; (b) input-output transfer curve of the proposed stage (±Vos are the threshold voltages deciding which channel to be selected)

$$v_{res} = \begin{cases} 2\cdot\frac{v_{in}}{A} + v_{ref} & for\ v_{in} < -v_{os} \\ 2\cdot v_{in} + v_{ref} & for\ -v_{os} < v_{in} < -\frac{v_{ref}}{4} \\ 2\cdot v_{in} & for\ -\frac{v_{ref}}{4} < v_{in} < \frac{v_{ref}}{4} \\ 2\cdot v_{in} - v_{ref} & for\ \frac{v_{ref}}{4} < v_{in} < v_{os} \\ 2\cdot\frac{v_{in}}{A} - v_{ref} & for\ v_{in} > v_{os} \end{cases} \quad (3)$$

allows a much wider input signal swing compared to that of a conventional 1.5b stage implementation shown in Fig. 6a. In this design, the peak to peak differential input signal swing can be as high as 2V with a 1.2V supply voltage. After the subtraction and channel selection, the signal swing is reduced by a factor of 2.5 to 0.8Vppd, as the output swing of this stage is limited by the output swing of the Op-amp which requires larger voltage headroom.

IV. Simulation Results

Traditionally, the dynamic performance of ADCs is characterized by a single tone sine-wave test. But this is not enough in proving the ADC's performance for multi-carrier systems. As it is explained in section II, the statistical properties of multi-carrier signals are far different from that of

a single full scale sine wave. In this paper, a Multi-tone Power Ratio (MTPR) test is adopted to compare the dynamic performance of the proposed ADC with the conventional one. MTPR is an important feature in the evaluation and design of multi-carrier systems [10]. It is the ratio of the power in one subcarrier to the noise power in another selected empty subcarrier, as shown in Fig. 7. A better MTPR performance results in lower bit error rate (BER). The ADCs are simulated with a multi-tone signal composed of 120 tones, each being QAM modulated. As shown in Fig. 8, the peak MTPR of the proposed 11b ADC is 10dB better than that of the conventional 11b ADC and it achieves a similar peak MTPR as that of a conventional 12b ADC.

With a multi-tone input signal, the ratio of the signal power to the total in band noise power (SNDR) is also simulated. Shown in Fig. 9, the SNDR of the 11b ADC with the proposed dual sampling technique is about 5dB better than that without this technique, and achieves a similar peak SNDR of a conventional 12b ADC. From Fig. 9, we observe that the SNDR increases with the increase of signal power when the input signal power is small, since the total noise is dominated by the quantization noise. When the signal increases further, it starts saturating the ADC and clipping noise increases exponentially. As a result, the SNDR drops dramatically. For the ADC with the proposed technique, the samples that are clipped in the main sampling network are replaced by the coarsely quantized samples from the auxiliary sampling network, hence the SNDR keeps increasing until the signal in the auxiliary channel also starts to clip. Results of these simulations are meeting and supporting our analysis in the previous sections.

V. Conclusion

A dual sampling technique for ADCs is proposed for converting multi-carrier signals more efficiently. It enables the ADC to reduce the power consumption and implementation complexity for achieving a required system performance. An 11b switched-capacitor pipeline ADC based on this technique is implemented. Analysis and simulations of the ADC with this technique show a wider input signal range and a substantial improvement in SNDR and MTPR compared to its conventional implemented counterpart for converting multi-carrier signals.

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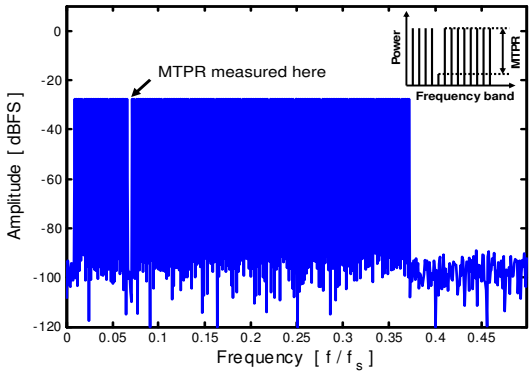

Figure 7. Multi-tone Power Ratio (MTPR) test

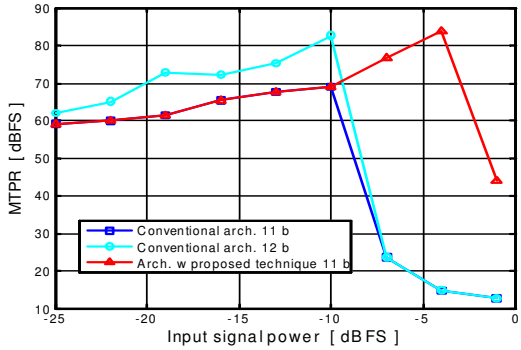

Figure 8. MTPR versus input signal power

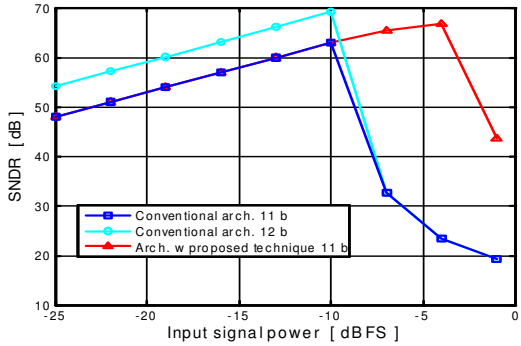

Figure 9. SNDR versus input signal power (with a multi-tone input signal)

References

[1] K. Uyttenhove, M.S.J. Steyaert, "Speed-power-accuracy tradeoff in high-speed CMOS ADCs," Circuits and Systems II, IEEE Transactions on , vol.49, no.4, pp.280-287, Apr 2002

[2] S. Lloyd, "Least squares quantization in PCM," Information Theory, IEEE Transactions on , vol.28, no.2, pp. 129- 137, Mar 1982

[3] J. Max, "Quantizing for minimum distortion," Information Theory, IRE Transactions on , vol.6, no.1, pp.7-12, March 1960

[4] O. Stoeble, V. Dias, and C. Schwoerer, "An 80 MHz 10b pipeline ADC with dynamic range doubling and dynamic reference selection," in ISSCC Dig. Tech. Papers, Feb. 2004, pp. 462–539.

[5] H.C. Choi, J.H. Kim, S.M. Yoo, K.J. Lee, T.H. Oh, M.J. Seo and J.W. Kim, "A 15mW 0.2mm2 10b 50MS/s ADC with Wide Input Range," ISSCC Dig. Tech. Papers, pp. 226-227, Feb., 2006.

[6] H. Van de Vel, B. Buter,H. van der Ploeg, M. Vertregt, G. Geelen, E. Paulus, "A 1.2V 250mW 14b 100MS/s digitally calibrated pipeline ADC in 90nm CMOS," VLSI Circuits, 2008 IEEE Symposium on , vol., no., pp.74-75, 18-20 June 2008

[7] D.J.G. Mestdagh, P.M.P. Spruyt, B. Biran, "Effect of amplitude clipping in DMT-ADSL transceivers," Electronics Letters , vol.29, no.15, pp.1354-1355, 22 July 1993.

[8] S. H. Lewis, H. S. Fetterman, G. F. Gross, R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s Analog-to-Digital Converter," IEEE J. Solid-State Circuits, vol. 27, pp. 351-358, Mar. 1992.

[9] L. Sumanen, M. Waltari, and K.A.I. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," Solid-State Circuits, IEEE Journal of , vol.36, no.7, pp.1048-1055, Jul 2001

[10] F. Maloberti, "Data Converters", Springer-Verlag New York, Inc., Secaucus, NJ, 2007