

Design of a MEMS-based 52 MHz oscillator

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Design of a MEMS-based 52 MHz oscillator

Joep Jacques Marie Bontemps

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Design of a MEMS-based 52 MHz oscillator

PROEFONTWERP

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus, prof.dr.ir. C.J. van Duijn, voor een commissie aangewezen door het College voor Promoties in het openbaar te verdedigen op maandag 21 september 2009 om 16.00 uur

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CHAPTER 1

INTRODUCTION

1.1 MICRO ELECTRO-MECHANICAL SYSTEMS (MEMS)

In the late '50's Jack Kilby and Robert Noyce were both working on the same question: "how to make more of less?" In 1952, Geoffrey Dummer had been the first to conceptualise the integrated circuit. Continued efforts by various people eventually led to the invention of the first working IC in 1958 by Jack Kilby, who worked for Texas Instruments at the time. In 1959, Robert Noyce (Fairchild Semiconductors) independently invented his own working IC combining work of Hoerni and Lehovec. Where Kilby used germanium, Noyce used silicon. Although he was half a year later, Noyce's chip had solved many practical problems that the microchip developed by Kilby had not [1]. The two men could not, however, have foreseen that this marked the start of the semiconductor industry with a global market worth about \$250 billion in 2008 [2]. Over the past fifty years microelectronics has had a large impact in health, communication, entertainment, and most other areas of modern life.

The technological progress in the early years of the semiconductor industry has been described by Moore in 1965. He found that the complexity of integrated circuits, defined as

the number of components per chip, had approximately doubled every year since their introduction [3]. In 1975 he predicted that the rate of increase would slow down in the next years to approximately a doubling every two years [4]. This exponential growth in complexity is called Moore's Law and the trend is observed until today.

The question how to make more of less remains relevant today. It cannot only be achieved through miniaturization (Moore's Law), but also by function integration. Semiconductor industry has always looked for ways to increase functionality of the IC by adding non-integrated components. Micro-Electro-Mechanical Systems (MEMS), also commonly referred to as micromachining in Japan or microsystems in Europe, is an enabling technology that can significantly increase the functionality of an IC.

MEMS is the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through micro-fabrication technology. While the electronics are fabricated using IC-process sequences, the micromechanical components are fabricated using compatible "micromachining" processes, e.g. deposition, lithography and etching. Silicon parts are selectively etched away or new structural layers are added to form the mechanical and electromechanical devices.



FIGURE 1.1 – In (a), a MEMS clamped-clamped beam resonator is depicted [5]. The beam measures 50 μ m across. Figure (b) shows a MEMS ratchet mechanism [6], a mechanical device that controls the rotational motion.

MEMS interface the computing power of the electronic world with the sensor and actuators of the non-electronic world. Microelectronic ICs can be thought of as the "brains" of a system and MEMS augments this decision-making capability with "eyes" and "arms", to

allow microsystems to sense and control the environment. At first, the MEMS field mainly covered electromechanical transducers. The breakthrough of MEMS systems has been triggered by the development of accelerometers for application in airbags in the automobile industry. Today, MEMS applications cover a wider range. A list of examples is given in Table 1.1.

TABLE 1.1 –	Examples	of application	ons in the	wide field	of MEMS	[7].
-------------	----------	----------------	------------	------------	---------	------

Category	Examples	
Inertia sensors	Accelerometer (airbag), gyroscope	
Pressure sensors	Tire pressure, blood pressure, microphone	
Micro fluidics / bioMEMS	Inkjet printer nozzle, micro-bio-analysis systems, DNA chips	
Optical MEMS (MOEMS)	Micro-mirror array for projection, optical fibre switch, adaptive optics	
RF MEMS	Switches, Antenna-filter, high-Q inductor	

The topic of this thesis is silicon MEMS resonators and oscillators. MEMS resonators are mechanical structures that vibrate on-chip. With their high-Q eigenmode they serve as frequency filter in filters or oscillator applications.

1.2 THE TIMING MARKET

1.2.1 Market size and development

In 2008, timing devices constituted a \$4.1 billion market [8]. The predicted annual growth rate is 6-7%. The combination of large size and large growth rate makes it a very attractive market. Currently, 92% of the revenue is accumulated in Asia. The market can be divided into:

- CMOS oscillators
- MEMS
- Crystal oscillators
- Timing IC's (Clock synthesizers, PLLs, Distribution IC's)

The market share (revenues) of each product type is depicted in Fig. 1.2. The 57% market share of the crystal oscillators is larger than the rest of the market combined. The average selling price (ASP) of a timing device is \$0.15. Important to note is that within this market the ASP of timing IC's is \$1.25. Hence, the IC adds considerable value.



FIGURE 1.2 – The worldwide timing devices revenue in 2008 accumulates to \$4.1 billion. The figure [8] shows the market share per product type: 57% is held by crystal oscillators, while timing IC's account for 43%. CMOS oscillators are hardly sold as separate devices.



FIGURE 1.3 – The price of a timing device is determined by its size and performance. Prices erode over time. An increase in performance, i.e. package, power, precision, and phase noise as indicated by the 4 P's, increases the price of a timing device of specific size.

Currently, there are over a hundred significant producers of crystal oscillators. Quartz crystals (resonators) and crystal oscillators are found in most modern electronic equipment. Frequencies for the resonators and oscillators range from kHz to hundreds of MHz.

Crystal oscillators are used as clock, tuning device, timing reference or frequency converter. Typical applications include:

- Computer (41%)
 - PC motherboards, memory modules
- Consumer (28%)
 - Set-top boxes, DVD players and recorders, Video game consoles, digital camera's, watches, AM/FM radio
- Communication (26%)
 - Telecommunication, wireless and broadband, wired communication
- Automotive and Industrial (2% and 3% respectively)

For a crystal oscillator, there is a strong correlation between size and price. Higher prices are paid for smaller oscillators. Furthermore, a higher price can be demanded for an oscillator with superior performance. The performance is described by the four P's of oscillators: Package, Power, Precision (accuracy), and Phase noise. Package stands for the compatibility with the system and not the package size. As an example, a package with solder balls instead of pins can often result in a significant prize premium. For the customer, the package with solder balls reduces assembly time and consequently cost.

1.2.2 Quartz or silicon?

Due to their high Q-factor, mechanical resonators are preferred over electrical resonators in high-precision filters for time-keeping and frequency-reference applications. For decades, crystal oscillators have set the standard in the timing market. Next to the high Q-factor, quartz crystals offer two main advantages. First, quartz is piezoelectric. This effective transduction principle leads to resonators with low signal losses. Second, quartz cut along specific directions shows almost zero temperature drift. This results in highly accurate resonators over a typical temperature range of 100 °C.



FIGURE 1.4 – The main board of a Sony Walkman NW-HD1 showing three discrete timing devices and a mechanical acceleration sensor (photo: Portelligent).



FIGURE 1.5 – Worldwide MEMS resonator market forecast. The figure shows predictions of the average selling price (ASP) and the total sales volume in million units (MU) and million US dollars (MUSD) over the next five years.

Crystal oscillators offer a combination of excellent phase noise performance, low power, and high accuracy unmatched by other timing devices. However, quartz crystals are also bulky and are currently not integrated with IC technology. MEMS resonators have been investigated as a potential alternative to the quartz crystals. Efforts over recent years have shown that MEMS based oscillators are capable of high Q [9], low temperature drift [10,11], excellent phase noise performance with low power consumption [12], and show almost no long-term drift when packaged [13]. Please note that all these achievements have been published after the start of this work in April 2005. MEMS resonators offer exceptional possibilities compared to quartz crystals regarding miniaturization, form factor, price, and system integration. However, so far, MEMS devices have experienced obstacles and limitations in the quest toward being able to replace crystal devices entirely in timing functions. These issues include power efficiency, excessive system noise and jitter (phase noise), and accuracy. In recent years, the MEMS start-ups SiTime, Silicon Clocks, and Discera have started selling commercial MEMS oscillators to customers. All of these companies have developed their own MEMS oscillator concept to tackle the four P's. The coming years will show which of these start-ups has developed the most successful concept. In the mean time, also traditional semiconductor companies like ST or NXP are working on MEMS development. In a market report by Databeans [8] a large growth in the MEMS oscillator market is expected over the next years, as is depicted in Fig. 1.5. The forecasted ASP of MEMS resonators is high, due to the anticipated small size and form factor of the timing device.

1.3 PROJECT DESCRIPTION

1.3.1 NXP Semiconductors

This PhD on design has been performed at NXP Semiconductors. NXP, established in 2006, is a leading semiconductor company. It was founded by Philips, based on their semiconductor division that was created more than 50 years ago. Based in Eindhoven, the company has about 30000 employees working in more than 30 countries and posted sales of \$5.4 billion in 2008 [14]. The company is divided into four business units: Automotive & Identification, Home, Multimarket Semiconductors and NXP Software.

Semiconductors Nijmegen has been founded in 1953. It is the oldest and also the largest manufacturing site of NXP Semiconductors. The most modern facility is the 8-inch wafer foundry. With 12.000 square metres of clean room (equivalent to almost 50 tennis courts), the foundries capacity is of around 450.000 wafers/year [15].



FIGURE 1.6 – A birds view of the NXP Semiconductors manufacturing site in Nijmegen. The new 52 degrees building had not been build at the time this picture was taken.

1.3.2 Project organization

At NXP Research, the MEMSXO project aims to develop MEMS oscillators on 1.5 μ m SOI substrates. The strategic choice for thin SOI substrates has been made for two reasons. First, MEMS processing in thin silicon layers can be done with standard CMOS processing tools. The silicon dioxide layer serves as a sacrificial layer. Second, identical substrates are used for the <u>A</u>dvanced <u>B</u>ipolar <u>CMOS DMOS</u> (ABCD) IC-processes. This class of processes can handle high voltages (ABCD2 up to 120V). The high voltage capability is suitable for the transduction of the mechanical resonator. Both MEMS and IC are processed on an identical substrate, since the aim is to integrate the MEMS structure with the IC-process.

The development of the MEMS oscillator is divided into three subjects:

- MEMS resonator design
- Circuit design
- Processing

Processing of the MEMS resonators is done at NXP Research in Leuven and Eindhoven. This not only involves the processing of the resonator device, but significant effort is also devoted to the development of a thin-film capping layer. The IC Lab in Eindhoven performs circuit design. MEMS resonator design is both done at NXP Research Eindhoven as well as at NXP Nijmegen. This is the main topic of this thesis.

This PhD on design is performed as an integral part of the MEMSXO project. The bulk of the work is carried out at NXP Nijmegen, although significant time has been spent at NXP Research in Eindhoven to collaborate with the project members there. Other important stakeholders are the Eindhoven University of Technology and the PointOne project MEMSLand. MEMSXO is one of the business carriers in MEMSLand, a MEMS initiative financed by the Dutch Ministry of Economic Affairs. Moreover, this ministry supports this work as a C12 cluster project.

1.3.3 Goal and deliverables

The goal of the MEMSXO project is to show the feasibility of high-performance MEMS oscillators in 1.5 μ m SOI. The project addresses specific business cases from business lines in the NXP organization. The requirements of the oscillator will depend on the application in the business case. Most demanding applications are found in wireless communication like GSM or Bluetooth. If the project is able to demonstrate feasibility, the business line can decide to start product development for the specific application. This would mean that the MEMSXO is successful and a technology transfer takes place. The project will then move into a next phase.

This PhD thesis addresses the feasibility of scaling MEMS resonators/oscillators to higher frequencies. The main target frequency for the MEMSXO project is the GSM frequency of 13 MHz. For these platforms, a trend to higher frequencies is observed. Therefore, a 52 MHz platform is anticipated in the future. In this thesis we address the scaling of MEMS resonators to this frequency. We identify the issues concerned with frequency scaling and propose solutions if possible. The deliverables of this thesis on design are:

- 1 A capacitive 52 MHz MEMS resonator on 1.5µm thin SOI.
- 2 A piezoresistive 52 MHz MEMS resonator on 1.5µm thin SOI.
- 3 Demonstrator: a functional, 52 MHZ MEMS-based oscillator on 1.5µm thick SOI.

1.4 CONTENTS OF THESIS

This thesis consists of eight chapters. We have come to the end of Chapter 1, where we have given an introduction into MEMS and defined the goal and deliverables of this thesis. Chapter 2 provides a technical introduction into MEMS resonators. The processing of the MEMS resonators on SOI wafers is discussed first. Next, the transduction principle of both the capacitive and piezoresistive MEMS resonator is explained. The chapter ends with an overview of the MEMS resonator designs, the electrical equivalent models, and the measurement set-up. This chapter provides the framework for the rest of the thesis.

In Chapters 3 to 6 the main results of the thesis are presented. In Chapter 3, frequency scaling of capacitive and piezoresistive MEMS resonators is discussed. MEMS resonators have been designed from 10 to 400 MHz. The results for the two transduction principles are compared. Chapter 4 shows the results obtained with resonator designs compensated for geometric offset. During processing, inaccurate pattern transfer of the resonator layout causes geometric offset in the real resonator. This results in spread of resonance frequency. The frequency of compensated layouts is in first order unaffected by geometric offset and highly accurate resonators can be obtained. This chapter discusses the compensation method and the results from measurements and FEM simulations. Chapter 5 is devoted to temperature drift of MEMS resonators. Since the stiffness of silicon is temperature dependent, the resonance frequency of silicon MEMS resonators notoriously drifts with –30 ppm/K. This chapter presents results obtained with two compensation techniques: oven-control and thermal oxidation. In chapter 6, a 56 MHz piezoresistive MEMS oscillator is demonstrated. This two-chip demonstrator consists of a dogbone MEMS resonator and an IC amplifier designed in the ABCD2 process.

The thesis concludes with an evaluation of the demonstrated project results in Chapter 7. Next to the evaluation, we put the results obtained in perspective. The NXP oscillator concept that has been developed is compared to other oscillator concepts like LC oscillators, quartz oscillators, and other MEMS oscillators. Finally, concluding remarks are given in Chapter 8.

CHAPTER 2

FUNDAMENTALS OF MEMS RESONATORS

2.1 INTRODUCTION

This chapter gives a technical introduction into MEMS resonators. The field of MEMS covers the areas of mechanics, electronics, chemistry, and transport phenomena. This chapter will serve as a framework for the following, more detailed, chapters that will frequently refer back to this chapter.

We first discuss the MEMS resonator process. Next, the mechanical model of the MEMS resonator is derived. Specific attention is paid to the Q-factor. Mechanical resonators are commonly preferred over electrical resonators due to their high-Q. After this section, we step into the electrical domain. We start with the transduction principles followed by the electrical equivalent models of the devices. The electrical model for the both the piezoresistive as well as the capacitive resonator will be discussed. Next, the resonator designs utilized in this thesis are presented. The final section covers the measurement set-up. MEMS resonators are characterized with S-parameters, commonly used in high-frequency measurements. For an extended introduction into MEMS topics, the book by Senturia [16] is suggested.

2.2 MEMS PROCESSING

The MEMS resonators are processed on silicon-on-insulator (SOI) wafers. SOI is convenient to use, since the silicon dioxide layer can be used as a sacrificial layer. SOI wafers consist of three layers, namely.

- The top-layer is the active single-crystal silicon (Si) layer in which devices are made, the SOI layer.
- The second layer is an insulating layer of silicon dioxide (SiO₂), the buried oxide layer.
- These two layers are on top of a thick single-crystal silicon layer, the handle wafer.

The MEMS resonators at NXP are processed on 8-inch wafers, with a SOI layer thickness of $1.5 \,\mu\text{m}$ and a buried oxide layer thickness of $1 \,\mu\text{m}$. The thin SOI layer can be processed with standard CMOS processing tools. A thicker SOI layer would require specialised equipment like a deep-reactive-ion-etcher (DRIE) that significantly enhance process complexity. MEMS resonators in thin SOI allow for batch production in an IC factory.

The process steps are described in Fig. 2.1. A difference is made between open resonators and capped resonators. Open resonators are not enclosed or covered, and are therefore highly susceptible to particles in the surrounding atmosphere. Due to the small volume of the resonators $(10^2-10^5 \ \mu\text{m}^3)$, oxidation of the surface or sticking of particles to the surface can significantly degrade the resonator performance [17]. Moreover, as we will discuss in the next section, the resonators operate in vacuum. This should make the need for a cap clear. The MEMS resonators need a clean, low-pressure environment. A cap that encloses the resonator in a cavity provides this. There are a number of methods to cap a MEMS structure:

- Wafer-to-wafer bonding [18,19].
- Die-to-wafer bonding [20].
- Thin-film package [21].

Of these three methods, the thin-film package is the preferred, but also the most difficult solution. The costs of a thin-film package are low, it has minimal height, and the resonators

are capped early in the process. A successful thin-film package is demonstrated by SiTime [13], where the resonator is covered by a polysilicon cap. At NXP, work is done on a silicon nitride cap. Despite recent success, all results presented in this thesis have been obtained with open MEMS resonators.

To return to the process, the first step is to prepare the lithography masks. The mask drawings are made by the device designer. With the mask pattern, the designer determines the trench pattern that defines the mechanical structure, the aluminium leads and bondpads, the doped and undoped regions of the device, and the areas that need to be covered by the cap. The pattern on mask can be transferred to a resist layer with the help of lithography tools. Selective processing is done on areas that are not covered by resist.

Trenches and holes are etched in the silicon with reactive-ion-etching (RIE). The minimum trench width that can be patterned with the available tools at NXP is 200 nm. Later in this chapter we will see that this minimum trench width is crucial in the transduction principle of the resonator. The maximum trench width is determined by the sacrificial aluminium that defines the cavity. If the trench width is larger than 800 nm, the aluminium fills the trench instead of covering it. Trenches and holes thus have a dimension in the range 200 -800 nm.

The silicon structures are released with a HF vapour etch. The etchant has a high selectivity for silicon dioxide. A vapour etch is used to avoid stiction. This issue is circumvented by using HF vapour, which is capable of high rates. For more detail on MEMS resonator processing, reference is made to internal documentation [22].



FIGURE 2.1 – The resonators are processed on 1.5 μ m SOI wafers. Processing of open MEMS is described in four steps: (a) well implantation (dotted), (b) patterned trench etch to define the mechanical structure and well dope diffusion, (c) contact implantation (hatched) and metal deposition, and (d) sacrificial SiO₂ layer etch. The processing of capped resonators deviates from the open MEMS route after the trench etch. The silicon nitride capping route is described in the following steps: (e) sacrificial SiO₂ layer etch to release the MEMS and sacrificial aluminium deposition for cap, (f) nitride cap deposition (2 times) and plug hole etch, (g) sacrificial aluminium etch, and (h) plug metal deposition and final nitride deposition. This creates a thin-film capped MEMS resonator structure. The deposition pressure of the plug metal determines the lowest achievable pressure inside the cavity.

2.3 MECHANICAL RESONATOR

2.3.1 Lumped-element model

A mechanical resonator can be modelled as a simple mass-spring system (Fig. 2.2). To account for energy loss in the resonator a damper is added to the system. The equation of motion for this system is given in 2.1, where x is the displacement (positive or negative) from the equilibrium position, k is the spring constant, m the lumped mass, and γ the damping coefficient.

$$\sum F_{ext} = m\ddot{x} + \gamma \dot{x} + kx \tag{2.1}$$

We solve this second-order differential equation for the case where the system is subject to a harmonic force. For this, we assume a harmonic solution for the displacement x of the same angular frequency ω as the external force, but not necessarily of the same phase. We therefore introduce a phase difference φ between the actuation force and the displacement [23]. In the solution for the equation of motion we use two system parameters: the eigenfrequency ω_0 and the quality factor Q.

$$\omega_0 = \sqrt{\frac{k}{m}}$$

$$Q = \frac{\sqrt{km}}{\gamma}$$
(2.2)

The eigenfrequency is a natural frequency of the system for which the vibration amplitude shows a large increase. The Q-factor is a measure of the frequency selectivity of the system. We now solve the equation of motion [23] for the harmonic amplitude x_0 and the phase φ .

$$\begin{cases} x_0 = \frac{F_0/m}{\sqrt{(\omega_0^2 - \omega^2)^2 + \omega^2 \omega_0^2/Q^2}} \\ \theta = -\arctan\left(\frac{1}{Q(\omega_0/\omega - \omega/\omega_0)}\right) \end{cases}$$
(2.3)

From Eq. 2.3 we can see that the amplitude has a maximum for $\omega = \omega_0$. Actually, the value is slightly lower than ω_0 , because of the damping. For high Q-factor and thus low damping this difference is negligible.

The amplitude is 90° out of phase with the driving force at resonance. This means that the driving force is exactly in phase with the velocity and thus the damping force. At resonance the spring force and the inertial force cancel each other and the driving force is used to overcome the damping forces on the system. The vibration amplitude increases with a factor Q compared to the static amplitude



FIGURE 2.2 – A simple model of a mechanical resonator consists of three elements: a mass (m), a spring (k) and a damper (γ). Such a mechanical resonator will give a frequency response as depicted in figure E.1. The resonance frequency and the Q-factor of the system can be calculated from the three elements.

2.3.2 Q-factor

The Q-factor has already been introduced in the previous paragraph as a measure of selectivity of the system. It can be calculated from the three mechanical lumped-elements. It can also be derived from the measured resonance peak, where the Q-factor is defined as the ratio of the resonance frequency and the peak width at half maximum. Thus, the sharper the peak, the higher the Q-factor.

$$Q = \frac{f_0}{\Delta f \left(-3dB\right)} \tag{2.4}$$

The resonator can also be seen as an energy storage device. In a classical resonator, energy is constantly transformed from one form into another. In a mechanical resonator (i.e. MEMS resonator) energy is transformed from kinetic energy (movement) into potential energy (spring energy). During transformation energy is lost. The Q-factor relates to the amount of energy loss (damping) in the system. Next to the first definition of selectivity (Eq. 2.4) it can also be defined as:

$$Q = \frac{\text{energy stored in device}}{\text{energy dissipated per cycle}}$$
(2.5)

For every contributing loss mechanism a Q-factor can be determined. The resulting Q-factor of the whole system is the reciprocal sum of all these different Q-factors. This means that the smallest Q-factor is the dominant factor for the overall Q. There are various damping mechanisms that induce energy losses in the system.

- Air damping losses (other surface losses)
- Anchor losses
- Thermo-elastic losses
- Other intrinsic losses (e.g. non-linearity)

2.3.3 FEM simulations

Next to analytical expression, finite element (FEM) simulations are commonly used to extract the resonance frequency of the MEMS device. The eigenfrequency mode is selected that solves the translational equation of motion. If we assume a harmonic solution $u(r,t)=Re(u(r)e^{jwt})$, then this equation becomes [24]:

$$\nabla \cdot (c \nabla u_i) - \rho \omega_i^2 u_i = 0 \tag{2.6}$$

Here c describes the stiffness tensor, ρ the mass density, and u(r,t) the particle displacement field. The structure will have an infinite number of eigenmodes, so the subscript

i points to the ith eigenmode. This equation is solved and from the simulation the eigenmodes and corresponding eigenfrequencies are obtained. Before the simulation can be done, the user needs to set the material properties and boundary conditions.

For the material properties, the density and stiffness of silicon are required. The density is set to 2300 kg/m^3 , a value found in numerous articles on silicon resonators. For the stiffness, the two dimensional stiffness tensor is used, since multi-crystaline silicon is an anisotropic material [25].

$$C = 10^{11} [Pa] \cdot \begin{bmatrix} 1.66 & 0.64 & 0.64 & 0\\ 0.64 & 1.66 & 0.64 & 0\\ 0.64 & 0.64 & 1.66 & 0\\ 0 & 0 & 0 & 0.80 \end{bmatrix}$$
(2.7)

Next to the eigenfrequency, the effective stiffness and mass can also be extracted from the eigenfrequency simulation. For the undamped resonator we know that potential energy is periodically converted into kinetic energy and vice versa. At time t=0, the kinetic energy is zero and all energy is stored as elastic energy.

$$E_{tot} = E_{el,\max} = \frac{1}{2}k_i |x_i|^2 = \left| \int_V W_s dV \right|$$
(2.8)

with W_s the strain energy densitym and V the volume of the device. From this energy relationship we can extract the effective stiffness and the effective mass. First, we need to determine the vibration amplitude x_i . We use a boundary integration in Comsol over the total actuation line. Next we integrate the strain energy over the whole volume to get the total stored strain energy. With the total stored energy and the effective amplitude we can determine the effective stiffness. The effective mass then follows from the resonance frequency and the effective stiffness [26].

$$k_{i} = \frac{2}{\left|x_{i}\right|^{2}} \left| \int_{V} W_{s} dV \right|$$

$$m_{i} = \frac{k_{i}}{4\pi^{2} f_{i}^{2}}$$
(2.9)

2.4 TRANSDUCTION PRINCIPLE

2.4.1 Electrostatic actuation

In this project, we use an electrostatic force F_{el} to actuate the resonator. Electrostatic actuation in combination with capacitive detection is commonly utilized in MEMS resonators, since it can be easily implemented on chip. Piezoelectric actuation is also found often. More exotic materials are needed, however, that increase manufacturing complexity.

To explain how the electrostatic force drives the resonator, an example of a singleclamped beam is given in Fig. 2.3. A superposition of a bias voltage V_{dc} and a signal input voltage v_{ac} are applied on the electrode on the right side of gap g. This induces an electrostatic force on the resonator.

To calculate the electrostatic force, we use a parallel–plate approximation. The parallel plate is formed by the outer end of the resonator beam and the outer end of the electrode that are separated by gap g. For the voltage-controlled moveable-plate capacitor, we take the derivative of the potential energy to calculate the electrostatic force [16,23]. The displacement x of the resonator is defined such that a positive displacement decreases the gap width.

$$F = -\frac{\partial E(V,g)}{\partial g}\Big|_{V} = \frac{\varepsilon_0 A V^2}{2(g-x)^2}$$
(2.10)

Now, the electromechanical coupling coefficient η is introduced. The parameter η describes the coupling between the electrical and the mechanical domain. With η we arrive at the final expression for the electrostatic force. For this, we assume that the displacement *x* is much smaller than the electrode gap width *g*.

$$F = \eta v_{ac}$$

$$\eta \equiv \frac{\partial C}{\partial x} V_{dc} = \frac{\varepsilon_0 A_{el} V_{dc}}{(g-x)^2} \approx \frac{\varepsilon_0 A_{el} V_{dc}}{g^2}$$
(2.11)

The coupling factor η is a key parameter. It determines how effective the ac driving voltage v_{ac} (input signal) is coupled as a force on the mechanical resonator. The coupling can be increased by:

- Increasing the electrode area A_{el}. In the example in Fig. 2.3 this means increasing the thickness of SOI layer or increasing the width of the electrode and the beam.
- Increasing the bias voltage V_{dc} .
- Decreasing the actuation gap g between the resonator and the electrode.

2.4.2 Frequency tuning with bias voltage V_{dc}

The electrostatic force is non-linear, since it depends on the displacement x of the resonator (Eq. 2.11). In the previous paragraph we eliminated the non-linear terms by assuming that $x \ll g$. If we use a Taylor expansion for the term $1/(g-x)^2$ instead and neglect all higher terms of x/g with the same assumption, we find an actuation force that is linearly dependent on displacement [23]. If we use this expression for the force in the equation of motion (2.1), we find an equation for the frequency tuning with the dc bias voltage.

$$\frac{\Delta f}{f_0} \approx \frac{-V_{dc}^2 \varepsilon_0 A_{el}}{2kg^3}$$
(2.12)

Bias tuning of the frequency can be used to trim the frequency after processing. This is a large benefit and can be exploited by designing resonators that have a large tuning range. This can also be a disadvantage, however. If the resonance frequency is highly sensitive to the bias voltage, this will set high demands on bias voltage stability of the product. This is a clear trade-off and the optimal choice will depend on specifications. Bias tuning range can be increased by:

- Increasing the electrode area.
- Decreasing the gap width.
- Decreasing the effective stiffness.
- Increasing the nominal bias voltage (working point).

2.4.3 Capacitive detection

For capacitive resonators, a capacitive current is used to detect the mechanical resonance. Figure 2.4 shows a top view of the 3D resonator in Fig. 2.3. When the bias voltage is applied over the parallel plate capacitor, a charge Q of opposite sign is induced on the two plates. The amount of charge that is induced on the plates depends on the bias voltage, the electrode area and the gap between the two plates. The displacement x has again been defined such that a positive displacement decreases the gap width.

If the two plates are moving towards each other, more charge is induced on the plates and current flows towards the outer end of the beam. If the plates are moving away from each other, less charge is induced on the plates and current flows away from the outer end of the beam. This 'motional' current is thus induced by vibration motion of the mechanical resonator that causes a capacitance change between the two plates.

The detected current is a superposition of the motional current and the electrical current induced by the ac voltage over the static gap capacitance. The motional current is proportional to the velocity of the mechanical resonator, where we neglected the ac voltage assuming that $V_{dc} \gg v_{ac}$. Again, η is the key parameter in the coupling between the mechanical resonator and the electrical output signal.

$$I = \frac{dQ}{dt} = V_{dc} \frac{\partial C}{\partial x} \cdot \frac{\partial x}{\partial t} + C \frac{\partial V}{\partial t} = \eta \frac{\partial x}{\partial t} + C \frac{\partial V_{ac}}{\partial t}$$
(2.13)

2.4.4 Piezoresistive detection

For the piezoresistive resonator, actuation is again done electrostatically. To detect the mechanical resonance, a modulated resistance is used instead of a modulated capacitance, as discussed in the previous paragraph. To describe this readout principle, we stick to our example of the single-clamped beam. We have a look at the top view of this device, which is presented more schematic this time (Fig. 2.5).

The vibration of the resonator induces strain $\varepsilon_L = \Delta L/L$ in the material. This strain induces a proportional change in resistance, as is described by Eq. 2.14. This proportionality is defined in the gauge factor *K*. The gauge factor describes both geometrical induced changes and resisitivity (ρ) induced changes.



FIGURE 2.3 – The 3D structure of the single-clamped beam resonator. The SOI wafer consists of three layers: the active silicon (Si) layer, an insulating silicon dioxide layer (SiO₂), and a thick bulk silicon layer that is only partly shown in the figure. The resonator is actuated with the alternating electrostatic force ΔF_{el} over gap g due to input voltage v_{ac} .



FIGURE 2.4 – Capacitive readout of the single-clamped resonator. The figure shows a top view of Fig. 2.3. The bias voltage induces a charge Q of opposite sign on both sites of the gap. If the resonator vibrates the gap size is changed by the displacement x. This changes the amount of charge on both plates and induces a current in the resonator.



FIGURE 2.5 – Piezoresistive readout of the single-clamped resonator. Again, a top view of the resonator is shown. A slit in the beam forces the current I_d along the length L of the beam. The vibrational motion of the resonator induces strain in the material. This changes the resistance of the current path over the resonator. This modulated resistance is read out with the dc current that induces an ac voltage component over the resonator.

$$\frac{\Delta R}{R} = K \varepsilon_L$$

$$R(\rho, L, A) = \frac{\rho L}{A}$$
(2.14)

For non-piezoresistive materials, the resistivity does not change under strain. The change in resistance is due only to the geometrical effect. For a Poisson ratio of 0.5 this results in a gauge factor of 2. Actual Poisson ratios will be even smaller than 0.5.

For piezoresistive materials, like silicon, gauge factors are two orders of magnitude larger than this. The gauge factor is dominated by the change in resistivity and the geometrical effect can be neglected [27]. This makes piezoresistive readout attractive to use in silicon.

It is straightforward to calculate resistance change for the single-clamped beam in Fig. 2.5. The only assumption that is made is that the slit spans the entire length of the device. The solution shows that the amount of resistance change is proportional to the mechanical vibration amplitude x. Since the resonator describes a harmonic motion, a harmonic resistance modulation is induced.

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} = \frac{K}{L} \int_{0}^{L} \varepsilon dx = \frac{K}{L} x$$
(2.15)

To detect the resistance modulation, a dc current I_d is applied over the resonator. This leads to a modulated voltage v_d superimposed on a dc voltage V_d . The capacitive resonator is a passive device, but the piezoresistive resonator is an active device, since dc power is consumed in the resonator. Higher output voltage can be induced at the expense of higher power consumption.

2.4.5 Frequency tuning with bias current I_d

With the piezoresistive readout there is a second method of frequency tuning. Young's modulus E of silicon, and thus the stiffness of the structure, drifts with temperature at about -60 ppm/°C. If a current is applied through the resonator, dc power is dissipated in the resonator. This power dissipation heats up the resonator shifting the resonance frequency to

lower values. The current I_d can thus be used to tune the resonance frequency. The dominant heat loss mechanism is conduction via the suspension of the structure. The thermal isolation of the suspension therefore determines how effective the frequency can be shifted with I_d . This oven-control principle will be discussed in more detail in chapter 5.



FIGURE 2.6 – The parallel capacitance C_s is added to the electrical equivalent model of the MEMS resonator. Unlike the motional parameters C_s is a real capacitor formed by the gap spacing between the electrodes and the resonator.



FIGURE 2.7 – The figure shows the measured admittance magnitude (Δ) and phase (\Box) of a 52 MHz capacitive MEMS resonator. The admittance has been extracted from calibrated S-parameter measurements. The data is fitted (–) with the electrical equivalent model in Fig. 2.6. A frequency selectivity of 7 dB has been found for this device.

2.5 ELECTRICAL EQUIVALENT MODELS

2.5.1 Capacitive resonators

In the previous section the transduction of the MEMS resonators is discussed. For the capacitive resonator we learned that the force on the resonator is proportional to the input voltage (Eq. 2.11) and the output current is proportional to the velocity of the resonator (Eq. 2.13). In both equations the electromechanical coupling coefficient η describes how effective the electrical and mechanical domain are coupled. Now, we will use the two equations to rewrite the mechanical equation of motion of the mass-spring-damper system (Eq. 2.1).

$$v_{ac} = \frac{m}{\eta^2} \ddot{q} + \frac{\gamma}{\eta^2} \dot{q} + \frac{k}{\eta^2} q \qquad (2.16)$$

This differential equation is identical to the differential equation of an RLC-network. We can therefore model the electrical response of the resonator by an RLC-network. Each mechanical lumped element has a direct equivalent electrical lumped element. The R, L, and C all have a subscript m, since they are called the motional parameters.

$$\begin{cases} R_m = \frac{\gamma}{\eta^2} = \frac{\sqrt{km}}{Q\eta^2} \\ L_m = \frac{m}{\eta^2} \\ C_m = \frac{\eta^2}{k} \end{cases}$$
(2.17)

The RLC-network (Fig. 2.6) models the capacitive current that is induced by the mechanical movement of the resonator. These motional parameters are not real electrical parameters, but electrical equivalent parameters. Off-resonance the MEMS device behaves as a capacitor that is made up by the gap spacing between the resonator and the electrodes. This is a real electrical parameter and it is a signal path, parallel to the RLC-network, from input to output. To calculate the value of C_s , we use the parallel plate approximation.

$$C_s = \frac{\varepsilon_0 A_{el}}{g} \tag{2.18}$$

At series resonance, the effect of L_m and C_m cancel out. The impedance is then determined by the parallel combination of R_m and C_s . This means that with the addition of C_s , the phase at series resonance is no longer zero. Furthermore, the parallel combination of C_s and L_m (and C_m) induces a parallel resonance. At series resonance the impedance is minimum, while at parallel resonance the impedance is maximum. For our MEMS resonators, C_s is three orders of magnitude larger then C_m . This means that the parallel resonance approaches the series resonance.

For a resonator, frequency selectivity is determined by the Q-factor. For our MEMS resonators, however, we have to take the influence of C_s into account. The ratio of R_m and the impedance of C_s determine how high the resonance peak extends over the background signal. We will take this as our definition for frequency selectivity Δ_s . The frequency selectivity of the capacitive resonator is indicated in Fig. 2.7.

$$\Delta_s = \frac{1}{2\pi f_0 C_s R_m} \tag{2.19}$$

2.5.2 Piezoresistive resonator

For the piezoresistive resonator, we can either apply a voltage V_d over the resonator arms or a current I_d through the resonator arms. When we apply a fixed voltage over the resonator, we measure a modulated current. With a fixed current through the resonator, we measure a modulated voltage. The choice is arbitrary and both lead to similar small-signal models [28].

All measurements in this project have been performed with a fixed current through the resonator. In Eq. 2.20, the output voltage v_d is derived. This is a function of the detection current modulation i_d and the voltage gain μ_m of the input voltage v_g .

$$V_{d} = I_{d}R\left(1 + \frac{\Delta R}{R}\right)$$

$$v_{d} = \left(\frac{\partial V_{d}}{\partial I_{d}}\right)_{v_{g}} \cdot i_{d} + \left(\frac{\partial V_{d}}{\partial V_{g}}\right)_{i_{d}} \cdot v_{g} = R_{d}i_{d} + \mu_{m}v_{g}$$
(2.20)

For the piezoresistive resonator, the voltage over the gap V_g is different from the bias voltage applied on the electrodes V_{dc} . The current through the resonator lifts the potential of the resonator. If we assume that the outer end of the resonator (opposite to the electrode) is halfway along the current path, then $V_g=V_{dc}-I_dR_d/2$.

Equation 2.20 incorporates a voltage gain μ_m . For the small signal model of the piezoresistive model we choose to use a transconductive element instead, to follow previous publications on this subject. This model has been developed by Van Beek [29]. Following from Thévenin's theorem and Norton's theorem, the use of a voltage gain or a transconductance is equivalent. We only have to take the 180° phase shift into account [28]. The electrical behaviour of the resonator is identical to a field-effect transistor in the linear region, with frequency selectivity. With the use of the field-effect transistor model, the subscript *g* at the input side now stands for both the electrode gap and the gate of the transistor. Accordingly, subscript *d* at the output side can be read as detection or drain. The transconductance g_m is given by:

$$g_{m} = \frac{g_{m0}}{\left(1 - \frac{\omega^{2}}{\omega_{0}^{2}} + j\frac{\omega}{Q\omega_{0}}\right)}$$
(2.21)
$$g_{m0} = -V_{g}I_{d}\left(\frac{4\varepsilon_{0}}{\pi^{2}}\right)\left(\frac{K}{E}\right)\left(\frac{A_{el}}{L \cdot k_{geom} \cdot g^{2}}\right)\left(\frac{R_{mod}}{R_{tot}}\right)$$

For the piezoresistive resonator, the capacitive signal, explained in paragraph 2.5.1, is superimposed on the piezoresistive readout. In most cases, at resonance, the piezoresistive signal is a few orders of magnitude larger than the capacitive signal. For low currents I_d or high gap voltages V_g , the magnitudes of both signals are comparable. Moreover, the capacitor C_s dominates the response of the piezoresistive resonator off-resonance. Therefore, the capacitive branch (Fig. 2.6) is added to the small signal model of the piezoresistive resonator. The small signal model is depicted in Fig. 2.8. Frequency selectivity Δ_s of the piezoresistive resonator is indicated in Fig. 2.9 and can be calculated with Eq. 2.22.

$$\Delta_s = \frac{g_{m0}Q}{2\pi f_0 C_s} \tag{2.22}$$


FIGURE 2.8 – The complete small signal model for the piezoresistive resonator with the capacitive branch incorporated into the model. This model is for a piezoresistive resonator where a current is applied through the resonator arms.



FIGURE 2.9 – The figure shows the measured admittance magnitude (Δ) and phase (\Box) of a 52 MHz piezoresistive MEMS resonator. The admittance has been extracted from calibrated S-parameter measurements. The data is fitted (–) with the electrical equivalent model in Fig. 2.8. A frequency selectivity of 23 dB has been found for this device.

2.6 **RESONATOR DESIGN**

For the design of the MEMS resonators, a choice for bulk-acoustic-mode resonators over flex-mode resonators has been made. Bulk-acoustic resonators have a higher effective stiffness compared to flex-mode resonators. This leads to some major advantages, especially at higher frequencies like 52 MHz, which is the main target frequency for this project.

- High energy storage. This is important to achieve a high signal-to-noise ratio.
- Higher Q-factor.
- Larger electrode area (size in general).

Although an in-plane flex-mode design is not attractive at 52 MHz, good results have been obtained with an out-of-plane design [30]. This would mean a change in processing, however, which lies beyond the scope of this project.

Round shapes, like rings or discs often found in literature, are also excluded from this project. The argument is that device layouts are made on a grid structure. This makes a curved line an ill-defined shape. It will not follow common design rules in the wafer fab. Moreover, a square shape will offer the same benefits as a disc, and can be made according to design rules.

$$f_{res} = \frac{c_{sound}}{\lambda}$$

$$v_s = \sqrt{\frac{E}{\rho}}$$
(2.23)

The resonance frequency of a bulk-acoustic resonator can be calculated with Eq. 2.23, where c_{sound} is the velocity of the longitudinal sound wave propagating in the material. The wavelength depends on the size of the resonator and the mode number we choose to actuate. In all measurements, the resonator is actuated in its fundamental mode.

For the square plate resonator, the outer ends in both directions are free. This means that in the fundamental breathing mode (Fig. 2.11a), a standing wave of half a wavelength propagates in the material. This is true for both in-plane dimensions, so the displacement pattern of the square plate is the superposition of the two orthogonal longitudinal waves.



FIGURE 2.10 – Schematic top view of the free-free beam, dogbone, and square plate resonator. Geometrical parameters are indicated in the figure.

For the resonance frequency of the plate, not taking holes and corner suspension into account, we find (Fig. 2.10):

$$f_0 = \frac{1}{2L} \sqrt{\frac{E_{2D}}{\rho}} \tag{2.24}$$

Silicon is a anisotropic material, so Young's modulus depends on the crystallographic orientation. For the square plate, we use an effective 2D Young's modulus of 181 GPa [25]. Because of its large stiffness and volume, the square plate is able to store a lot of energy. This means that this design is well suited to meet demanding phase noise specifications [31,32]. The square plate in breathing mode is actuated by electrodes on all four sides. With this large electrode area the motional resistance R_m can be kept low, despite the large stiffness of the structure.

The square plate is also frequently actuated in Lamé-mode (Fig. 2.11b), which is a shear mode. The Lamé-mode is attractive, since the four corners are nodal points of this mode. The structure can thus be suspended at its nodal points, allowing very high Q-factors. The resonance frequency of this mode is not determined by the Young's modulus but by the shear modulus G, which is 160 GPa for silicon.

$$f_0 = \frac{1}{2L} \sqrt{\frac{G}{\rho}} \tag{2.25}$$

For the free-free beam resonator both outer ends are also free. The fundamental mode therefore also consists of half a wavelength (Fig. 2.11c). However, the free-free beam is defined as two parallel resonators connected back-to-back for a balanced operating mode [33]. The bridge in the middle suspends the structure at the nodal point (Fig. 2.10). The resonator thus consists of two beams of length L that both contain a quarter of a wavelength in fundamental mode. Because of the balanced operating mode, the free-free beam design is capable of very high Q-factors. Since the design is small, it is easy to process and cap. The design is oriented along the [100] direction that has a Young's modulus of 131 GPa.

$$f_0 = \frac{1}{4L} \sqrt{\frac{E_{[100]}}{\rho}}$$
(2.26)



a: 52 MHz, breathing mode square plate



b: 41 MHz, Lamé-mode square plate



c: 52 MHz, piezoresistive free-free beam



d: 52 MHz, piezoresistive dogbone

FIGURE 2.11 – FEM simulations show the eigenmode shape of the square plate (2), free-free beam, and dogbone resonators. The colours correspond to total in-plane displacement, where dark red is the maximum displacement and dark blue no displacement. Typical displacements for the MEMS resonators are a few nanometre. In figure (a) and (b) the square plate design is depicted. For the same square size, the extensional or breathing mode is depicted in (a) and the Lamé mode in (b). The plate is perforated with regular spaced square holes to enable the etch of the SiO₂ layer underneath the Si structure. In figures (c) the free-free beam and in (d) the dogbone resonator are depicted. Both designs have a slit to force the current along the length of the structure. This is used for the piezoresistive readout, since for the selected mode shapes most strain is along the length.

The most complex structure is the dogbone resonator (Fig. 2.11d). It is very similar to the free-free beam, but with a lumped mass attached to the outer end [34]. This lumped mass has two benefits; it increases the electrode area and it concentrates the strain in the springs. Because the dogbone has a non-uniform cross section, the fundamental mode consists of two standing waves that connect at the step in cross-section. The resonance frequency can be found with equation 2.25, which has been derived by Van der Avoort [35]. The parameters w and L correspond to the width and length of the spring and b and a to the width and length of the mass.

$$\frac{2w}{b} = \tan(\beta L) \tan(\beta a)$$

$$\beta^{2} = \frac{4\pi^{2} f_{0}^{2} \rho}{E_{[100]}}$$
(2.27)

2.7 MEASUREMENTS

2.7.1 Two-port S-parameter measurements

MEMS resonators, which are the devices-under-test (DUT) in the measurements, are twoport devices. The MEMS resonators are measured with a network analyser, which measures scattering parameters. The name scattering comes from the similarity between the behaviour of light in the field of optics and microwave energy. S-parameters [36,37] provide a way to give a complete description of the electrical behaviour of the DUT. Since electrostatic MEMS resonators are reciprocal devices, S_{12} and S_{21} are equal, thus 3 independent complex numbers can be measured. The main reason to use S-parameters is that they are measured in a matched impedance system (in this case 50 Ω), in contrast to open- and short-circuit-type measurement required for other available network parameters. Measurements that are rather difficult to make at microwave frequencies. Furthermore, when measuring S-parameters with a network analyser, effects of cables, bias tees and the network analyser itself can largely be eliminated.

2.7.2 Measurement setup

A custom-designed setup is used for device characterisation. The MEMS resonators are measured in vacuum, since the resonator movement is severely damped at ambient pressure. For vacuum measurements, a custom-made stainless steel vacuum chamber is used (Fig. 2.12a). Air pressure inside the chamber is reduced by a Pfeiffer turbo molecular drag pumping station with a membrane pre-pump that has a base pressure of $5 \cdot 10^{-5}$ mbar. For resonator measurements, a pressure of 10^{-2} mbar is low enough. At this pressure, air damping is no longer the dominant dissipation mechanism. This pressure is reached in about 5-10 minutes. Electrical feedthroughs on the side of the vacuum chamber can be used to connect signal sources outside the chamber to the probes inside the camber.

A CCD camera on top of a microscope is used to probe the bondpads of the device. Input and output of the devices have a ground-signal-ground bondpad configuration with a 100 μ m pitch. This fits the Süss mircoTec Z-probes used.

The frequency response of the resonator is measured with an Agilent E5062A ENA-L network analyser. Bias voltage and bias current are applied externally, usually with Keithley 2400 SourceMeters. Bias is applied externally, since the network analyser is only capable of bias voltages up to 30V. Bias tees shield the network analyser from the high dc voltages and currents. The PicoSecond 5530A bias tee used is suited for dc voltages up to 200 V. In addition, a 1M Ω resistor is added to prevent high currents in event of a short.

Both isolated and grounded chucks are available for probing. For all measurements in this project an isolated chuck has been used, since a grounded chuck complicates interpretation of the measurements. The grounded chuck becomes part of your DUT and its influence has to be added to the electrical equivalent circuit, which is an unnecessary complication.

Calibration is needed to exclude effects of cables, probes, bias tees and network analyser from the DUT measurements. For this calibration a specific calibration substrate, Picoprobe #CS-5, is used. A full two-port calibration consists of 12 measurements. After calibration the DUT is measured in vacuum. Next, the model parameters are extracted in ICCAP. The measured amplitude and phase of all four S-parameters are fitted with the electrical models in Fig 2.6 and Fig. 2.8.



FIGURE 2.12 – The MEMS resonators are measured in vacuum. In figure (a) the vacuum chamber is depicted with the lens and CCD camera used for probing. In figure (b) a Z-probe can be seen that is used to perform the measurements on wafer.



FIGURE 2.13 – The measurements set-up for measurements on a piezoresistive resonator.

2.7.3 Semi-automatic probe station

For waferspread measurements a semi-automatic probe-station is used. In this case, measurements are done at ambient pressure. One 8-inch wafer consists of \approx 140 identical fields. The Labview controlled waferstation is able to scan a complete wafer and measure an identical resonator design in each field. Measurements are done uncalibrated with an older network analyser, the HP 8753D. It takes about 90 minutes to complete a single scan.

The data is analysed in Matlab. From the uncalibrated data the motional resistance, Q-factor, and resonance frequency can be extracted. Matlab automatically generates 2D waferplots showing the spread of the three extracted parameters over the wafer.

To improve the accuracy of the frequency measurements, the wafer is first heated to 140 °C and fixed at this temperature for an hour. This will remove the thin water film on the resonator surface. After this heat treatment the wafer is cooled down to room temperature and measurements can start. During measurements a flow of dry air is maintained over the wafer, to prevent water molecules to stick on the surface. The resolution is < 500 Hz, which is 10 ppm for a frequency of 52 MHz [38].

CHAPTER 3

FREQUENCY SCALING

3.1 INTRODUCTION

Micromechanical resonators offer capabilities of having multiple frequency standards on a single-chip. This is especially true for lateral resonators, where the resonance frequency is determined by the design on the lithography masks. In this regard, it is an interesting question to see what frequency range is within reach for MEMS resonators.

The frequency range for oscillators ranges from low kHz to several GHz [39]. The lowfrequency oscillators are generally used for real-time clock (RTC) applications, for example the 32.768 kHz RTC found in watches. At the mid-end of the spectrum we find the frequency reference applications, like the 26 MHz found in GSM phones. RF oscillators cover the highfrequency range.

Low-cost ceramic resonators work well in embedded systems in which timing is not critical [40]. They are available at frequencies of 200 kHz to almost 1 GHz. For quartz crystals, higher frequencies are usually obtained at lower cost by using a phase-locked loop (PLL). The PLL consumes power, however, and degrades the phase noise performance of the oscillator.

device #	<i>L</i> [μm]	<i>h</i> [μm]	N _h	<i>L_{el}</i> [μm]	f ₀ [MHz]
1	320	0.5	35	307	13
2	160	0.5	17	147	26
3	80	0.5	9	69.5	52
4	40	0.5	5	32.2	104
5	20	0.5	2	13.3	208
6	10	0.5	-	5.0	416

TABLE 3.1 – The square plate resonator is geometrically scaled six times a factor two. The parameters refer to Fig. 2.10.



104 MHz

208 MHz

416 MHz

FIGURE 3.1 - SEM pictures show the scaling of the square plate resonator. The resonance frequency is inversely proportional to the size of the square plate. The electrodes appear brighter due to charging.

For a MEMS resonator, higher frequencies actually mean a reduction of cost. For a higher frequency, the resonator has to be reduced in size and that means less silicon area is consumed. Silicon area is a cost driver for the chip. Conversely, decreasing frequency means larger resonators. For thin layer structures (e.g. $1.5 \mu m$ SOI), this would mean that robustness is a major issue. For low frequency MEMS resonators, thicker layers are preferred.

In this chapter we will investigate the scaling of MEMS resonators to higher frequencies. We will evaluate whether high-frequency applications are suitable for MEMS resonators. Furthermore, the scaling of the piezoresistive and capacitive concepts will be compared.

3.2 CAPACITIVE RESONATOR

3.2.1 Design of experiment

The square plate design is used to investigate the scaling of the capacitive resonator. The breathing eigenmode of the resonator is depicted in Fig. 2.11a. The square plate is actuated by four electrodes coinciding with the side ends of the plate. To etch the SiO_2 layer underneath the resonator, the plate is perforated with a regular pattern of square etch holes.

The experiment consists of six scaling steps. In each scaling step, the size of the plate and T-shaped suspensions is decreased by a factor two. The electrode length is also decreased, but an exact factor two is not always possible due to design rules and structural restrictions.

The SOI layer thickness (1.5 μ m), gap width (270 nm), hole size (500 nm), and pitch (9 μ m) are kept constant. This means that the number of etch holes N_h^2 scales as well. Table 3.1 and Fig. 3.1 give an overview of the scaling experiment with the square plate resonator. The experimental results presented in the next paragraphs have all been obtained with calibrated S-parameter measurements in vacuum (section 2.7).

3.2.2 Scaling with bias voltage V_{dc}

As has been explained in chapter 2, according to the analytical model, the three motional parameters are expected to scale with bias voltage (Eq. 2.17). Also the resonance frequency, due to the non-linear electrostatic actuation force, should scale with bias voltage (Eq. 2.12).

To test this analytical model empirically, devices are measured at various settings of the bias voltage. The resonators are characterized with calibrated S-parameter measurements in the vacuum set-up (section 2.7).

For the 13 MHz square plate, the results are plotted in Fig. 3.2. The electrical parameters are extracted in IC-CAP [41] where the electrical model (Fig. 2.6) is manually fitted to the measured data. The expected linear dependency is found for all four parameters, which shows that the analytical model accurately describes the bias voltage dependency. A motional resistance of 940 Ω has been measured at 80V bias voltage. This is the lowest motional resistance measured in this project and the only time a motional resistance below 1 k Ω has been measured.



FIGURE 3.2 – The resonance frequency and the three motional parameters all scale with the electrode bias voltage. In figure (a), C_m and f_o^2 are plotted against the bias voltage squared. In figure (b), L_m and R_m are plotted against the inverse of the bias voltage squared. An excellent linear fit is obtained in all four cases.

3.2.3 Mechanical parameter extraction

From the measurements we are able to directly extract the electrical equivalent parameters. With the four slopes obtained from the bias voltage plots, the mechanical parameters can also be extracted. For this, we need some mathematical rework (Eq. 3.1). The only input parameter not measured is the electrode area A_{el} .

The electrode area can be calculated from the layout of the device and the SOI layer thickness of 1.5 μ m. However, using this value for the electrode area does not yield a consistent parameter set compared to the gap width *g* extracted from SEM pictures (270 nm) and *k* and *m* extracted from Comsol simulations. As a pragmatic solution, we introduce the

empirical parameter α and search for an effective electrode area $\alpha \cdot A_{el}$ that will result in a consistent parameter set for g, k, and m (the extracted value for Q does not depend on the electrode area). A consistent parameter set is obtained with $\alpha = 1.4$ for all resonators in the scaling series.

To explain the factor 1.4 increase in effective electrode area, we simulate the effect of stray fields in Comsol [42]. In the analytical model of the MEMS resonator, the parallel plate approximation is used to derive an expression for the electromechanical coupling coefficient η (Eq. 2.11). This does not take the effect of stray fields into account. The simulated capacitance for a gap of 270 nm is a factor 2.4 higher than the capacitance value obtained from the parallel plate approximation. This is clearly higher than the empirically obtained factor $\alpha = 1.4$ increase in electrode area. Currently, we cannot explain the difference between these two values.

The analytical model predicts that the effective stiffness k does not scale with geometry, while the effective mass m should scale quadratically with the area L^2 of the plate. This scaling is confirmed empirically by the experimental results. Measurement and model values differ only by a few percent. Since the etch holes and suspension are not taken into account in the analytical model, a better match cannot be expected.

$$g = \left(\varepsilon_{0}A_{el}4\pi^{2}\right) \times \frac{\partial L_{m}}{\partial(1/V_{dc}^{2})} \times \frac{\partial f_{0}^{2}}{\partial V_{dc}^{2}}$$

$$k = \left(\frac{\varepsilon_{0}^{2}A_{el}^{2}}{g^{4}}\right) \times \frac{\partial V_{dc}^{2}}{\partial C_{m}}$$

$$m = \left(\frac{g^{4}}{\varepsilon_{0}^{2}A_{el}^{2}}\right) \times \frac{\partial L_{m}}{\partial(1/V_{dc}^{2})}$$

$$Q = \left(\frac{\sqrt{kmg^{4}}}{\varepsilon_{0}^{2}A_{el}^{2}}\right) \times \frac{\partial(1/V_{dc}^{2})}{\partial R_{m}}$$
(3.1)

with g the electrode gap width, A_{el} the total electrode area, k the effective stiffness, m the effective mass, and Q the Q-factor of the device as defined in Eq. 2.2 and Eq. 2.4.



FIGURE 3.3 – Model (\blacktriangle) and measured (\square) mechanical and electrical parameters for the square plate resonators of Table 3.1 at V_{dc}=40V. The measured data points are fitted with a linear dependency to evaluate the expected analytical scaling. In (b), we find the empirical relationship Q~ f₀^{-0.75} for the scaling of *Q* with the resonance frequency. In (e), the large increase op R_m at higher frequencies is depicted. In (f), the measured values for C_s deviate strongly from the analytical values for f₀>100 MHz, i.e. L_{el}<40 µm. The simple electrical equivalent model seems to break down at these high frequencies.

3.2.4 Results

In Fig. 3.3, the resonator parameters are plotted. For the square plate resonator, no resonance signal could be found for the 416 MHz designs. The loss of frequency selectivity is most likely the reason that no resonance signal could be found for this design. This is why all graphs in Fig. 3.3 contain only five data points.

For the resonance frequency, the quantitative match between model and measurements is good. The measured resonance frequency is 5% lower as compared to the analytically predicted frequency, which can be explained by the etch holes in the plate [31]. The Q-factor decreases with increasing frequency. The resonator becomes smaller and therefore its energy storage capability is reduced. An unexpected low Q-factor has been found for the 104 MHz design. From measurements we know that the Q-factor of a single resonator design typically shows a spread smaller than 10%, although a few outliers are usually measured. Measurements on four other 104 MHz square plate resonator show that the low value Q=1500 reproduces well with a spread of about 10%. The reason for the low Q of this design is not understood.

The motional electrical parameters also show the expected dependency on geometry. We already confirmed that the mechanical parameters are described well by the model, but the electrical equivalent parameters also depend on the coupling coefficient. For the coupling coefficient, the same empirical parameter in the electrode area is used to account for the effect of stray fields. Again, the results in Fig. 3.3 are obtained for a constant value of 1.4.

The main conclusion on scaling of capacitive resonators is taken from the last two graphs of Fig. 3.3. If we assume that the Q-factor is inversely proportional to frequency, the motional resistance R_m increases quadratically with frequency. In our measurements, R_m increases from 4 to 2000 k Ω (V_{dc}=40V) when the frequency increases from 13 to 208 MHz (Fig. 3.3e). It is very difficult to drive such a high-impedance resonator in an oscillator while maintaining the correct phase change (Barkhausen criteria, chapter 6). Moreover, the impedance of the shunt-capacitance C_s over the gap does not scale with frequency, but remains constant. For the square plate resonator in this experiment, the impedance of C_s is about 100 k Ω . Due to the high value of R_m , the frequency selectivity Δ_s of the resonator is lost. This makes it impossible to meet oscillation conditions.

3.2.5 Dual-gap, coupled designs

For capacitive resonators, scaling to higher frequencies is difficult since frequency selectivity is lost. This is a system level problem. However, solutions can be found in the design of the device. Too improve resonator performance at high frequencies, we should decrease both the motional resistance R_m and the shunt-capacitance C_s . We see that keeping the R_m low when we scale a capacitive resonator to higher frequencies is not straightforward. An interesting option then is to use multiple resonators in parallel, since there is no fundamental limit to the number of resonators that can be coupled together.

The first step is decreasing the shunt-capacitance. With either a dual-gap design or a differential design [43] the shunt-capacitance can largely be eliminated. Since negative voltages used in a differential set-up are difficult to generate on-chip, using a dual-gap design is preferred. With a dual-gap design separate electrodes are used for actuation and detection. The resonator itself is grounded, thus eliminating cross talk over the resonator. This is the main contributor to the shunt-capacitance C_s . For the square plate, this has been done for a Lamé-mode resonator (Fig. 2.11b), but could also be done for a breathing-mode resonator (Fig. 2.11a). The Lamé-mode is attractive to use, since the corners are nodal points of this mode shape. This makes it possible to achieve high Q's [9,43] and decrease the motional resistance. A 52 MHz Lamé-mode design has been processed [44] with a measured Q-factor slightly larger than $6 \cdot 10^4$, which is more than two times higher than the breathing mode resonator of the same frequency. More importantly, the shunt-capacitance has been reduced to only 3 fF. This is an impedance of almost 1 MΩ at this frequency.

The second step is to decrease the motional resistance. This can be achieved by:

1) Increasing the bias voltage V_{dc} over the gap.

Increasing the bias voltage is not attractive, since these high voltages are not directly available on-chip. A charge pump is needed, which consumes power and area (cost). Furthermore, the maximum voltage is limited by the IC process technology.

2) Decreasing the gap width g.

We work with a gap width of 200 nm. For now, this seems to be a practical limit for making highly reproducible gaps.

3) Increasing the electrode area $A_{el.}$

The thin silicon that we use to make our resonators already limits the electrode area. For higher frequencies the size of the device will decrease, further decreasing the electrode area.

- 4) Decreasing the stiffness (and mass such that the resonance frequency remains constant). Since the frequency is determined by the ratio spring constant over mass, the spring constant will certainly not decrease when the device is scaled to a higher frequency. At best, it will remain constant.
- 5) Increasing Q.

As an empirical result, the Q-factor is lower for high-frequency resonators if it is dominated by anchor losses.

None of the five alternatives results in a feasible method to significantly decrease the motional resistance R_m . Therefore, we focus on the coupling of resonators to decrease R_m . To investigate mechanical coupling of resonators, a design of experiment has been performed on coupled square plate resonators (Fig. 3.4). The resonators vibrate in breathing mode. In the first design, the two resonators are actuated and read out in parallel, but not mechanically coupled. In the other designs, the two resonators are mechanically coupled by one beam between the opposite sides of the two resonators. The width of the beam is increased, to test the effect on the Q-factor and resonance frequency. The square plate design is compensated for geometrical offset (Chapter 4), which ensures that the resonance frequency of the two resonators is closely matched.

For the uncoupled design, the two resonators are not forced to vibrate at the same frequency. Therefore, we measure two separate resonance peaks. From this measurement it is clear that we need mechanical coupling to make the two resonators vibrate as a single system. The results of the mechanically coupled resonators are depicted in Table 3.2 and compared to a single resonator of the same design. We can see that a slender beam is enough to couple the resonators effectively. With a slender beam, the Q-factor of the system is as high as the single resonator. We manage to decrease the motional resistance by almost a factor two.

Coupling multiple dual-gap resonators can solve the scaling problem of capacitive resonators. By grounding the resonators the shunt-capacitance C_s can be kept low, while coupling several resonators decreases the motional resistance significantly. This results in high-frequency capacitive resonators with increased frequency selectivity.



FIGURE 3.4 – SEM picture of a coupled square-plate resonator. The electrodes appear brighter due to charging. In the designed experiment, the width of the coupling beam is varied (Table 3.2).

TABLE 3.2 – Results for the measurements on the coupled resonators. The nominal frequency of the square plate design is 51.916 MHz . Electrical parameters have been extracted at Vdc=40V. Resonance frequencies of the single resonator of the same design measured on 140 resonators over a complete wafer lie within a frequency range of \pm -150 ppm of the average frequency (chapter 4).

# resonators	Width coupling beam [µm]	Q	<i>∆f</i> [ppm]	R_m [k Ω]	<i>C</i> s [fF]
1	N.A.	23650	0	44.2	33.5
2	2	24093	45	25.8	59.5
2	4	19999	-7	30.0	59.0
2	8	23785	223	27.5	58.6
2	16	2871	10374	275	58.0

3.3 PIEZORESISTIVE RESONATOR

3.3.1 Design of experiment

In section 3.2 on the square-plate resonator we have shown that the motional resistance of the capacitive resonators increases quadratically with frequency. This makes the concept not well suited for high frequency oscillators. In this section we will investigate the scaling of the piezoresistive resonator.

For the scaling experiment of the piezoresistive resonator we will use a free-free beam design, which is depicted in Fig. 2.10. The free-free beam has a slit of width s to redirect the current along the length L of the resonator. Since the slit does not span the entire length of the resonator, the cross section in the middle of the beam is smaller than the cross-section at the end of the beam. An overview of the experiment is given in Table 3.3 and Fig. 3.5.

We will take this into account when we derive an analytical expression for the resonance frequency of the beam. We assume that the stiffness of the beam is determined by the width *(w-s)* in the middle of the beam, while the effective mass is determined by the width *w* at the end of the beam [45]. The factor *(1-s/w)* is important, since both the resonance frequency and the transconductance g_m scale with this factor. The analytical expression for the resonance frequency is given in Eq. 3.2, with Young's modulus *E* and density ρ .

$$f_0 = \frac{1}{4L} \sqrt{\frac{E}{\rho}} \sqrt{1 - \frac{s}{w}}$$
(3.2)

3.3.2 Results

For the piezoresistive resonator, signal levels are generally larger than for the capacitive resonator. This is certainly true for the thin 1.5 μ m structures that we use, since the resulting small electrode area reduces the electromechanical coupling coefficient η . The higher signal levels make it easier to measure the piezoresistive resonators, especially at high frequencies where the effect of the shunt-capacitance increases. For the free-free beam resonator, all six devices in the scaling series up to a frequency above 400 MHz have been successfully measured. We have shown [46] that even free-free beams with a fundamental mode above 1 GHz can be measured. This is a MEMS resonator record.

device #	<i>L</i> [μm]	<i>w</i> [μm]	<i>s</i> [μm]	1-s/w	f₀ [MHz]
1	136	32	0.8	0.98	14
2	68	16	0.8	0.95	27
3	34	8	0.8	0.90	53
4	17	4	0.4	0.90	105
5	8.5	2	0.2	0.90	211
6	4.25	1	0.2	0.80	397

TABLE 3.3 – The piezoresistive free-free beam resonator is scaled down in six steps, each with a factor two decrease in size. The factor (1-s/w) varies slightly over the series.



FIGURE 3.5 –SEM pictures of the scaling of the free-free beam resonator. The resonance frequency is inversely proportional to the length of the beam. The picture of the 416 MHz design is enlarged. Here, rounding of the corners by the etch process can be observed.

The free-free beam is attractive, since it is easy to process and capable of very high Q's. For the 13 MHz free-free beam, a Q-factor of $171 \cdot 10^3$ has been measured. For all MEMS resonators processed in 1.5 µm SOI at NXP, this is the design with the highest Q.

The frequency of the free-free beam and the transconductance g_{m0} show a good quantitative match between measurements and analytical model (Fig. 3.6b and 3.6c). These results have been obtained by assuming a linear dependence on (1-s/w). To design for a specific frequency with ppm accuracy, however, FEM simulations will be needed. And even FEM simulations have a limited accuracy. Hence, the final solution is to allow for one or two iterations in your design loop. The analytical model, however, gives more insight during device design. Moreover, the measurements show that the model is valid over a large frequency range.

The transconductance g_{m0} is insensitive to geometric scaling, which is shown by the results in Fig. 3.6c. The model predicts that the transconductance is insensitive to SOI layer thickness, but we could not test this empirically. This shows that the piezoresistive concept is very attractive for high frequency resonators in thin layers. The Q-factor does scale with geometry (frequency). This means that the transconductance at resonance $g_{m,max}=g_{m0}\cdot Q$ decreases linearly with frequency. An increased current through the device can compensate these increased losses, at the expense of higher power consumption.

Figure 3.6d shows a large difference between the measured values for shunt-capacitance C_s and the analytically expected values. The measured values are much larger and have only a slight dependence on the electrode width w. This indicates that there is a parasitic capacitance besides the gap capacitance that contributes to C_s . This parasitic capacitance can be due to capacitive coupling via substrate or in-plane due to electrical leads from bondpad to electrodes.

3.3.3 Bondpad capacitance

A final note is made on the bondpad capacitance of the piezoresistive device. The bondpad has a capacitance to ground that loads the transconductance of the piezoresistive resonator (see also paragraph 6.3.3). At low frequencies, the impedance of this bondpad capacitance is high, which means that (loading of) the transconductance is dominated by the piezoresistor. This ideal case leads to a phase shift of 90° at resonance. At higher frequencies,

the bondpad impedance decreases and this shifts the phase of the resonator. For the 400 MHz resonator, the phase shift has decreased to 60°. This parasitic effect is important during oscillator design. The effect can be reduced by decreasing the bondpad capacitance and the impedance of the piezoresistor. Integration of the resonator in the IC process eliminates the need for bondpads between resonator and amplifier altogether. This is a major advantage of our approach, which aims to integrate the MEMS resonator in the ABCD technology.



FIGURE 3.6 – The scaling measurements on the piezoresistive free-free beam resonator at $V_{dc}=20V$ and P=1mW. Measurements (\Box) are compared to results of the analytical model (\blacktriangle). In (b), the Q-factor of the device scales inversely with frequency. In figures (a) and (c), a good quantitative match is found between measurements and model. Measurements confirm that the transconductance g_{m0} is insensitive to geometric scaling. In (d), measured values for the shunt-capacitance C_s are much higher then predicted analytically.

3.4 THE PREFFERED CONCEPT AT HIGH FREQUENCY

In the previous sections we have evaluated the performance of the capacitive square plate and the piezoresistive free-free beam resonators. In the final section of this chapter, we compare the performance of these two readout principles. No resonance signal has been found for the capacitive square plate at 400 MHz. We therefore limit our analysis to the first five scaling steps that span a frequency range from 13 to 210 MHz. In Fig. 3.4, the measured the frequency selectivity Δ_s for the capacitive (Eq. 2.19) and piezoresistive (Eq. 2.22) resonator is depicted.



FIGURE 3.7 – Frequency selectivity of the piezoresistive free-free beam (Δ) and the capacitive square plate resonator (\Box) are compared. Bias voltage V_{dc} is set to 40V for the capacitive resonator and 20V for the piezoresistive resonator. The power consumption of the piezoresistive resonator is 1 mW.

For the capacitive resonator, the ratio of the impedance of the shunt-capacitance C_s and the motional resistance R_m determines the frequency selectivity. The motional resistance is inversely proportional to the Q-factor and the square of the electrode area. The low value at 104 MHz is explained by the low Q-factor of this design (Fig. 3.3b). For the 208 MHz design, the low frequency selectivity is due to the relatively large value of C_s (Fig. 3.3f).

For the piezoresistive resonator, frequency selectivity is determined by the ratio of the impedance of the shunt-capacitance and the transconductance at resonance $g_{m,max}$. The transconductance at resonance is proportional to g_{m0} (Fig. 3.6c) and Q (Fig. 3.6b). The frequency selectivity is lower than expected analytically and decreases faster. This is due to

the high value of the shunt-capacitance C_s that decreases only slightly with frequency (Fig. 3.6d).

When scaling to higher frequencies, the impedance of the resonant branch increases, while the impedance of the parasitic branch decreases. Frequency selectivity thus decreases if we scale to higher frequencies. By increasing the bias conditions of the resonator we can decrease the impedance of the resonant branch and improve selectivity. However, a high bias voltage is impractical on-chip and a high bias current implies high power consumption.

From Fig. 3.7, it becomes clear that the piezoresistive readout is more suitable for high frequency resonators than capacitive readout. At 208 MHz, where both resonators suffer from a high value of C_s , the difference in frequency selectivity is about 20 dB. The piezoresistive readout is insensitive to geometric scaling of the device. The impedance at resonance only increases due to the decrease in Q. The capacitive readout is not only affected by a decrease in Q, but the capacitive current also depends on the electrode area. This electrode area decreases linearly with frequency. The motional resistance is therefore proportional to f_0^2 .

For resonators at high frequencies the piezoresitive concept is preferred. For low power applications, the capacitive concept might still be preferred. Care must be taken to keep the impedance of the piezoresistor low compared to the bondpad impedance that loads the transconductance g_m . This can be done by decreasing the surface area of the bondpad. The capacitance of the bondpad can be calculated analytically with an error margin of 25% [45]. Typical values are 250 fF for a bondpad of 80x80 μ m². Furthermore, keeping C_s low is crucial to maintain sufficient frequency selectivity at high resonance frequencies.

CHAPTER 4

INITIAL FREQUENCY ACCURACY

4.1 INTRODUCTION

For many time-keeping and frequency-reference applications, frequency accuracy is a key specification. The mechanical resonance frequency of the resonating element should therefore be controlled with high precision. In reference, typical quartz crystals exhibit frequency tolerances of +/- 1-50 ppm [40]. For the MEMS resonator to be successful, we feel an accuracy +/- 50 ppm is required for applications such as USB or digital audio players.

The initial frequency accuracy is determined by the material properties and the geometry of the device. The high-level of initial accuracy required can normally not be achieved with batch manufacturing techniques, which result in slight variations of resonator dimensions and, as a result, variation in resonance frequency. This lack of accuracy can be corrected for by a trimming procedure, for instance by laser ablation [47] or by selective deposition [48]. These techniques involve mass tuning of each individual resonator after it has been manufactured. Unfortunately, such a trimming procedure is costly and time consuming. Another approach that has been demonstrated utilizes fractional-N PLLs, notably by SiTime [49], one of the first MEMS oscillator start-ups. The use of a fractional-N PLL is convenient since it can be used to both trim the initial frequency inaccuracy as well as to compensate for

temperature drift of the frequency. However, Fractional-N PLLs consume several tens of mW and degrade the phase noise performance of the oscillator. This trade-off with frequency accuracy might not be beneficial for many applications.

This chapter will demonstrate layouts that are compensated for process induced geometric variations. This means that the resonance frequency is robust against dimensional variations. This type of design allows for the batch production of high precision MEMS resonators without the need for a trimming procedure. A patent application has been submitted [50].

4.2 GEOMETRICAL OFFSET

The resonators are processed in single-crystal silicon. Single-crystal silicon is a wellcontrolled and characterized material. This makes it highly suitable for accurate resonators, since the material properties must be consistent to enable high frequency-accuracy. Furthermore, with its ideal crystalline nature it has the potential for very high Q and minimal aging [51,52].



FIGURE 4.1 – Processing sequence for the fabrication of a MEMS resonator: (a) mask pattern is exposed and developed in photo resist. (b) resist pattern is etched in SOI layer. (c) sacrificial layer is etched to release resonating beam. In (d), we can see a top view of the resonator where the resonator and etch hole dimensions have changed due to the systematic offset δ indicated by the arrows in (b).

A typical processing sequence for the fabrication of a MEMS resonator is shown in Fig. 4.1. Our resonators are surface micromachined into a 1.5 μ m thick SOI layer. This can be done with standard CMOS processing tools, so that these resonators allow for batch production.

For processing, the dimensions of the resonator design are captured in a mask layout of the device. This mask pattern is then etched into the SOI layer. The main cause of resonator dimension inaccuracy is the non-perfect pattern transfer from mask layout to SOI. This is typically called under- or overetch and results in geometric variations. Although these variations may vary over the wafer, they are assumed systematic for one device. The result is a geometric offset in the design dimensions of the resonator.

The geometric offset changes all in-plane dimensions of the resonator slightly. The thickness of the device is unaffected. Figure 4.1 shows an example of a square plate design. A negative offset δ or underetch leads to a decrease in plate size *L*. For simple bulk-acoustic resonators the resonance frequency is proportional to the inverse of the acoustic length *L*. The geometric offset therefore has a direct effect on the resonance frequency. This can be understood from Eq. 4.1, which shows the relative frequency spread with δ for a square plate resonator.

$$\frac{\Delta f}{f_0} = \frac{\frac{1}{L - 2\delta} - \frac{1}{L}}{\frac{1}{L}} \approx \frac{2\delta}{L}$$
(4.1)

The factor two appears, because the plate is etched on both sides. The relative frequency spread is proportional to the ratio of the geometric offset and the plate size. The geometric offset is process dependent and independent of plate size. This means that for higher frequencies and thus smaller plate sizes the relative frequency variation due to geometric offset increases.

For a typical process spread of +/- 20 nm on a plate size of 80 μ m (f₀~52 MHz) the total frequency spread is 1000 ppm. This number can be reduced significantly with the use of compensated designs.

4.3 COMPENSATED DESIGNS

The resonance frequency of a mechanical resonator is determined by its effective stiffness k and mass m. The key in compensated designs, which are insensitive to geometric offset [53], is that the relative change in mass is equal to the relative change in stiffness for an offset.

$$\frac{\partial k/\partial \delta}{k} = \frac{\partial m/\partial \delta}{m}$$
(4.2)

This principle can readily be applied to flex-mode resonators. In two patent applications [54,55] various examples are given of flex-mode designs that are insensitive to geometric offset. We focus on bulk-acoustic-mode resonators instead. This is a different class of resonators, where the resonance frequency is determined by a longitudinal wave propagating through the material. In fundamental mode, a standing wave of a quarter wavelength (fixed-free) or half wavelength (free-free) vibrates in the material. This should make clear that we are dealing with a collective wave in the material with a wavelength of tens or hundreds of microns and not with small lattice vibrations on atomic scale. The resonance frequency of a bulk-acoustic resonator can be calculated with Eq. 4.3, where c_{sound} is the velocity of sound.

$$f_{res} = \frac{c_{sound}}{\lambda} \tag{4.3}$$

To create a design that is insensitive to geometric offset, the relative dependency of the wave velocity and wavelength on the offset should be made equal. This principle can be applied to both one-directional as two-directional bulk-acoustic resonators.

$$\frac{\partial \lambda / \partial \delta}{\lambda} = \frac{\partial c_{sound} / \partial \delta}{c_{sound}}$$
(4.4)

From Eq. 4.1 we have learned that for simple bulk-acoustic resonators, like a plate or a beam, the resonance frequency is proportional to the inverse of the device length. This is,

because the wave velocity is constant, while the wavelength is determined by the length of the resonator. The geometric offset thus directly changes the wavelength of the standing wave in the material. For compensated designs, the wave velocity also needs to be affected by the geometric offset. We use two methods to change the wave velocity in the device:

- Add holes in the material. The wave velocity is reduced by the holes. The larger the holes, the lower the wave velocity.
- Add external springs (suspensions). The external springs increase the effective stiffness and thus increase wave velocity in the material.

A second approach to compensate designs for geometric offset is to ensure that the wavelength of the acoustic wave does not depend on geometric offset. This can be achieved with designs that have a non-uniform cross-section along the length of the device. While the principle also holds for designs with a continuously tapering cross-section, we use designs that have a discontinuity in cross-section. If the structure has a discontinuity in cross-section, the acoustic wave will show a phase jump over this boundary. At resonance, the standing wave in the structure is composed of two standing waves of different wavelengths. The wavelength for such a design is not determined only by the total length of the device, but becomes a function of the length and width of the two parts of different cross-section. For such a design, optimal dimensions can be found for which the effective wavelength is not changed by a geometric offset.

The actual resonator designs are thus more complex than a simple square plate or beam. A FEM model in Comsol Multiphysics has been developed to simulate the effects of geometric offset on the mechanical parameters of the design [56]. The model is written in Comsol Script. The resonator designs include suspension structures to connect the device to its anchors, etch holes to reduce release etch times, step changes in cross-section, and slits to force current to flow along preferred directions. Moreover, the anisotropic Young's modulus of silicon has been incorporated into the model. For a specific offset δ the model recalculates the resonator dimensions and runs the eigenfrequency simulation. The result is the relative frequency spread due to a geometric offset. The user is left to find an optimal set of resonator dimensions that results in resonance frequency compensation.

Compensated layouts for the square plate, dogbone, and free-free beam resonator have been designed. The target frequency for the resonator designs is 52 MHz. In Fig. 4.2 the simulation result for a compensated square plate resonator is depicted. The design is first-

order compensated, leaving a second-order spread profile. Frequency spread over a +/-20 nm offset range is reduced to 40 ppm, which is a factor 25 improvement over the uncompensated design. It is also possible to eliminate second-order frequency variations. Figure 4.2 shows an example for a second-order compensated free-free beam design. The frequency spread over a +/-20 nm offset range is smaller than 1 ppm.



FIGURE 4.2 – Frequency spread as a function of geometrical offset for a compensated 52 MHz square plate resonator. Second-order compensation demonstrated for a 52 MHz free-free beam resonator



FIGURE 4.3 – S-parameter measurement of the compensated square plate design at ambient pressure. In the figure, the magnitude of the S12 parameter is depicted. At ambient pressure, the Q-factor of the device is about 4800, compared to about 25000 in vacuum.

4.4 RESULTS

4.4.1 Experimental set-up

For a compensated square-plate design with square holes and T-shaped corner suspension the simulation results have been presented in Fig. 4.2. An experiment has been set-up around this compensated design. A mask layout of this design has been drawn, together with three other layouts that have been given a geometric offset of -100, -50, and +50 nm respectively. The +100 nm layout could not be drawn, since this would have violated the design rules of the process. The results of the measurements on these devices are presented in this section and compared to measurements on uncompensated designs. The devices are measured with S-parameters, uncalibrated at ambient pressure.

4.4.2 Measurements

Most processed resonators are uncompensated for geometric offset. The uncompensated layouts include various designs, like the free-free beam, dogbone, ring resonator or lever design. Also, the designs span a broad frequency range from 1 MHz to 200 MHz. All these designs, however, show a similar radial pattern of frequency spread over the wafer. An example is given for a 52 MHz free-free beam in Fig. 4.4a.

This radial pattern is expected to be due to process conditions in the etch equipment, which causes geometric offset of the layout. Measurement of the motional resistance of the device can confirm this. The motional resistance is determined by the effective stiffness and mass of the mechanical resonator, the Q-factor, and the electrode gap width. For the effective mass and stiffness, the relative changes over the wafer are at ppm order of magnitude. The Q-factor is measured and approximately constant over the wafer. The spread in R_m is therefore determined by the spread in gap width g ($R_m \sim 1/g^4$). The geometric offset of the layout is proportional to the spread in gap width.

For the spread in R_m a radial wafer pattern is found, identical to the spread in resonance frequency. This is depicted in Fig. 4.4b. This confirms that geometric offset is the dominant source of frequency spread over the wafer. Since the geometric offset has a radial pattern over the wafer, the spread in resonance frequency and R_m also show a radial pattern. With FEM simulations the geometric offset has been estimated to be ± 20 nm.



FIGURE 4.4 – Interpolated wafermap pictures created from the semi-automatic measurements on various resonator designs. Figure (a) shows the relative frequency spread for an uncompensated 52 MHz free-free beam design. In (b) the motional resistance R_m is plotted for the same free-free beam design. Figure (c) shows the relative frequency spread for a compensated 52 MHz square plate. In figure (d), the frequency spread of the free-free beam design in (a) is corrected for the radial dependence. Now this design shows a similar wafer pattern as the compensated design.

Length [µm]	f ₀ [MHz]	Total frequency spread [ppm]
68	26.96	1277
34	52.94	2529
17	105.8	4568
8.5	210.7	7150

TABLE 4.1 – The spread in resonance frequency scales inversely with the length L^{-1} of the free-free beam.

For bulk-acoustic resonators the geometric offset is expected to induce a larger relative frequency spread for smaller resonators. This can be understood from Eq. 4.1, which shows that the relative frequency spread scales inversely with the length of the resonator. Measurements on scaling series of free-free beams confirm this. The results of the scaling experiment are depicted in Table 4.1. For a smaller device, the frequency is higher, and the relative spread in frequency is larger. Thus for small, high-frequency devices compensation for geometric offset is very important.

For compensated designs, the radial wafer pattern is still observed for R_m . However, the frequency spread for the compensated 52 MHz square plate does not show the radial pattern anymore. This is depicted in Fig. 4.4c. The measurements of R_m and f_o show that the radial pattern of geometric offset is still there, but the resonance frequency of the device does not change with this offset. The device is thus compensated. For the compensated square plate design the total frequency spread over the wafer is 446 ppm. Of the 84 measured resonators, 92% has a frequency within +/- 150 ppm of the average frequency.

For an uncompensated design, the radial dependence of the resonance frequency can be eliminated with a regression analysis. The regression analysis is performed for a second-order dependence on the radius of the wafer. When the residuals of the regression analysis are plotted in a wafer plot (Fig. 4.4d), the pattern is similar to that of a compensated design. This has been done for more uncompensated designs with similar result.

In conclusion, the dominant source of frequency spread is geometric offset. This results in a radial pattern for the relative frequency spread. If the spread with geometric offset is eliminated, either by a compensated design or by a regression analysis on an uncompensated design, the radial pattern is not found anymore. The resulting wafer pattern is not random, but still shows systematic variation over the wafer. This indicates other sources of systematic frequency variation in the fabrication process that have not been compensated for.

4.4.3 Comparison with simulation

For the compensated square plate design, the simulation results are verified by comparing the resonance frequency of the nominal device to the resonance frequency of the -100 nm, -50 nm, and +50 nm offset devices. This is done on 69 locations on the wafer. On each location, measurements on the four resonators show that the nominal device is designed around an optimal point. This means that both the devices with a negative offset as the device with a positive offset have a lower resonance frequency than the nominal device. The average result over the 69 locations is plotted in Fig. 4.5 and compared to the FEM simulations.

The measured values show a qualitative match with simulations. This result shows that compensated designs can be obtained from the FEM simulation tool. The measured frequency spread is twice as large as predicted by the FEM model, however. The simulation assumes a constant geometric offset for the device, independent of feature sizes. With SEM, this assumption can be tested for the compensated square plate design. This could explain the larger frequency spread found in measurements.



FIGURE 4.5 – For the compensated square plate design with $f_0=52$ MHz, the nominal device as well as the -100 nm, -50 nm, and +50 nm offset devices are measured on 69 locations on a wafer. The average measured frequencies are plotted (Φ) and compared to FEM simulations (\Box) on the same design.

4.5 **DISCUSSION**

Geometric offset is the main source of initial frequency spread for MEMS resonators. For bulk-acoustic resonators, the frequency spread scales inversely with the length of the device. This means that for small, high frequency devices the frequency spread is large. For a 52 MHz square plate resonator initial frequency spread is about 1000 ppm for a geometric offset of \pm 20 nm.

The initial frequency offset can be corrected for by a trimming procedure, but this is costly and time-consuming. This chapter has shown bulk-acoustic resonator designs that are compensated for geometric offsets. A FEM simulation tool using Comsol Multiphysics and scripting is developed to obtain compensated layouts. The designs are tolerant to process induced geometric offsets.

A compensated 52 MHz square plate design has been processed. Measurements show that the design is indeed successfully compensated for geometric offset. Measurement results show a good qualitative agreement with the simulation results, proving the validity of the FEM model. For the compensated square plate design 92% of the 84 measured resonators on wafer have a frequency within \pm 150 ppm of the average frequency. Moreover, the dominant source of this residual frequency spread is not geometric offset.

The wafermap of the compensated design does not show random variation of the frequency over the wafer. It is clear that other systematic sources of frequency spread remain. The remaining spread pattern could be explained by:

- Underetch variations
- SOI thickness variations
- Variations in residual stress in the SOI layer
- Variation introduced by the measurement set-up

From FEM simulations we have seen that designs are possible that have less than 1 ppm frequency spread over a +/- 50 nm processing window. This low spread will not be found in measurements, however, unless the other systematic sources of frequency spread are identified first. Efforts should focus on explaining the systematic frequency spread found for the compensated designs first, before new designs are processed with even improved compensation. We have already been able to establish that the measurement set-up adds
systematic frequency variation although we have not been able to quantify this yet. Furthermore, the main assumption in the FEM model that the geometric offset is systematic for the whole device should be checked. This is most likely the cause of the quantitative mismatch between simulation and measurements. With a better insight in what geometric variations the process adds to the design the FEM models can be improved. This requires a joint effort from process designers and device designers.

This chapter has shown various concepts that can be used to compensate bulk-acoustic resonators for geometric offsets. How accurate can we finally make these resonators? A lot will depend on the remaining sources of systematic frequency variation that need to be identified. If we know the cause of frequency spread, we can also look for a way to compensate for it. Based on the current results from measurements, a frequency window of \pm 100 ppm is feasible for a 52 MHz bulk-acoustic design. Depending on what other systematic sources of frequency spread are identified, this number could be reduced by a factor 2 to \pm 50 ppm. Anything lower than this will require a trimming procedure. Therefore, it is also worth the effort to consider a cost-effective trimming procedure for MEMS resonators (Chapter 5). This will bring high-accuracy applications such as mobile timing market in range for MEMS.

CHAPTER 5

TEMPERATURE DRIFT COMPENSATION

5.1 TEMPERATURE DRIFT

In chapter 4 we have investigated the initial accuracy of a MEMS resonator. Geometrical offset on the resonator layout from inaccurate processing can easily amount to more than 1000 ppm frequency spread. With compensated designs, this initial frequency spread can de reduced to \pm 150 ppm.

A second contributor to frequency spread is temperature variations. The Young's modulus of silicon is temperature dependent. This means that the stiffness of a silicon resonator drifts with temperature. Since the resonance frequency is proportional to the square root of the ratio of stiffness and mass, the resonance frequency of a silicon resonator also drifts with temperature. Measurements of temperature drift (change of the resonance frequency with respect to temperature) on a piezoresistive dogbone resonator show drift of -32 ppm/°C (Fig. 5.1), which is in agreement with values reported in literature for mono-crystalline silicon [10,57]. For a typical temperature specification range of 100 °C, this results in a frequency spread of about 3000 ppm.

For quartz crystals, cuts along certain crystallographic orientations have almost zero temperature drift. Hence, quartz oscillators can comply with high accuracy specs of a few ppm without the need for any compensation. Adding a temperature-compensation circuit yields a TCXO with accuracy of 1 ppm, and putting the entire oscillator into a temperature-controlled-oven package yields an OCXO with accuracy in the part-per-billion range.

To compete with the specifications of quartz crystal oscillators, we need to significantly reduce the temperature drift of the MEMS resonator. In this chapter we will discuss two options. First, active compensation with an oven-control concept that fixes the temperature of the resonator. Work on this concept has been performed together with master student Di Wu [58] and has resulted in a patent application [59]. Second, passive compensation where the resonator is thermally oxidized [60]. This concept originates from Van Beek [5]. The work presented in this chapter has been carried out together with NXP Research and is documented in a report by Van der Avoort [38].



FIGURE 5.1 –The temperature drift for the piezoresistive dogbone resonator measured for three different samples of the same design (Δ , \Box , and \circ).

5.2 OVEN-CONTROL

5.2.1 Drift in time and self-heating

For piezoresistive devices, the current through the device will induce self-heating. Since the resonance frequency depends on the device temperature, an increase in current through the device will shift the resonance frequency. Also, both the electrical and thermal resistance will increase with device temperature. The self-heating experiment is performed on a freefree beam design (Fig. 5.2). With a length of the resonator arms of 24.7 μ m and a width of 2.5 μ m, a resonance frequency of 74.4 MHz has been found. The thermal resistance of the device can be estimated from the dimensions of the suspension in the centre, which have a length of 0.65 μ m and a width of 1.2 μ m. The samples are wirebonded and mounted in open ceramic packages.

The measurement set-up consists of a vacuum chamber with a heating jacket to change the ambient temperature in the vacuum chamber in which the devices are measured. The ambient temperature inside the chamber is measured with a Pt-1000 sensor connected to a socket close to the device under test. The devices are tested at a vacuum level of 10^{-5} mbar typically. The dc-resistance R_d at room temperature is about 27 k Ω . A Keithley 2400 SourceMeter supplies a dc bias current through the device, while a voltage source supplies up to 20V on the electrodes of the 200 nm electrode gap. The device resonance is measured with an Agilent 4395A network analyser, where the S12-parameter peak gives the value of the resonant frequency. The bias sources are connected to the network analyser with bias tees.

As the resonators are stored in air, a frequency drift is observed (Fig. 5.3a). This is a much smaller drift as compared to the 0.1% range mentioned in [61] for thin resonators, where adsorption or stiffening due to oxidation were mentioned as possible cause. The temperature coefficient of the frequency does not change after this aging. This drift is too small to influence our temperature dependent data.

Two approaches are employed to define an effective device temperature from the experimental data. First, the electrical resistance of the device is used as a temperature sensor at various values for the dc bias current. Second, the resonance frequency of the device is used to define an effective resonator temperature. Also shown (Fig. 5.3b) is the predicted curve of the analytical model, which is based on the power dissipation in the device and the heat conduction via the suspension.

The observation is that the device shows a considerable electrical self-heating [62]. This is mainly due to the low thermal conductivity of the narrow suspension. Secondly, a clear difference between the two effective temperatures is observed. We attribute this difference to the inhomogeneous temperature distribution in the device. The electrical resistance is highest at the ends where the temperature is highest, while the spring constant of the resonator is dominated close to the suspension where the temperature is lower.



FIGURE 5.2 – The self-heating experiment is performed on a 74 MHz free-free beam resonator. This SEM picture shows the dimensions of the device.



FIGURE 5.3 – Figure (a) shows the frequency drift observed at $T_{ambient}=90$ °C during device storage in air. In figure (b), different measures for the effective self-heating of the piezoresistive resonator are depicted; resonance frequency of the device (\Box), analytical model (Δ), and electrical resistance of the device (\circ).

5.2.2 **Proof of principle**

To demonstrate the oven-control principle, the piezoresistive dogbone design (Fig. 2.10 and 2.11) is used. This is the same resonator design that will be used for the MEMS oscillator demo. This is described in chapter 6.

With oven-control, device temperature is controlled over a specific ambient temperature range, typically 100 °C. We use the self-heating of the piezoresistive resonator, as has been described in paragraph 5.1.1. The device temperature has to be maintained at a fixed temperature above the maximum ambient temperature, since self-heating can only be used to increase the device temperature relative to the ambient temperature. As the ambient temperature decreases, the difference between device temperature and ambient temperature increases. An increase in self-heating is required to maintain the stable device temperature. Hence, the highest power dissipation is found at the lowest ambient temperature. In the experiments, the voltage over the resonator is controlled.

Measurements on the dogbone resonator show that the voltage values needed to stabilize the frequency over a 30-100 °C temperature range are realistic. In the first measurement series the resonance frequency is fixed at 56.00 MHz, which corresponds to a device temperature of about 110 °C. In the second series the resonance frequency is fixed at 55.94 MHz, which means a device temperature of about 140 °C. Highest power dissipation is found in the second series at the lowest ambient temperature and is kept below 10 mW (Table 5.1).

Ambient temperature		30 °C			100 °C	
f_0	I_d [mA]	V_d [V]	P _{disp} [mW]	<i>I_d</i> [mA]	V_d [V]	P _{disp} [mW]
55.94	1.68	5.10	8.56	1.05	3.09	3.24
56.00	1.61	4.27	6.88	0.62	1.62	1

TABLE 5.1 – Power consumption of the oven-control frequency stabilization as a function of ambient temperature.

A temperature stabilisation circuit is designed on a test board with discrete components. The circuit is a classic differential amplifier design, which gives a voltage output proportional to the difference of two input voltages. The first input is a fixed reference voltage that can be tuned with a potentiometer. The second input comes from an ambient temperature sensor that



FIGURE 5.4 – This figure shows the flange of the vacuum tube. The vacuum flange has several feedthroughs that connect to two DIL sockets inside the chamber. One socket holds the packaged resonator die and one holds the compensation circuit. External connections can be made on the flange.



FIGURE 5.5 – Temperature dependent frequency of the oven-controlled resonator. The frequency is determined from uncalibrated S-parameter measurements in vacuum. The largest drift is observed for the low voltage compensation (\blacksquare f₀=56 MHz, V_d=4.27V). For the high voltage case (f₀=55.94 MHz, V_d=5.1V) the drift is further reduced. This is measured for two different samples of the same design (\square and Δ) without tuning the bias resistors.

has a voltage output linearly proportional to ambient temperature. The slope can also be adjusted by a potentiometer. The circuit is able to linearly compensate for the changes in ambient temperature by changing the voltage over the resonator.

The measurements are performed in a vacuum chamber (Fig. 5.2). The measurement setup has been described in the previous paragraph. The circuit is able to reduce temperature drift over a 70 °C temperature range from 2100 ppm to 150 ppm, which is a factor 14 improvement. From Fig. 5.5 we can see that the remaining temperature drift has a parabolic profile. For an experienced IC designer it is straightforward to implement a second-order compensation on the circuit. This could further reduce the temperature drift to values well below 100 ppm. If the current through the device is reduced, signal losses in the resonator increase. This can be compensated by a proportional increase in the electrode gap voltage. With this method the temperature drift can be compensated, while keeping the gain of the resonator constant [59].

The temperature of the device depends on the ambient temperature, the amount of dc power dissipation in the device (self-heating), and the thermal insulation of the device. Heat loss is dominated by conduction via the suspension. By increasing the voltage over the device, more power is dissipated, and the device temperature increases due to self-heating. If the voltage over the device is dependent on ambient temperature, a stable device temperature can be maintained.

5.3 THERMAL OXIDATION

5.3.1 Experiments

Where oven-control is an active method of temperature compensation, thermal oxidation is a passive method. A major advantage of this method is that it does not consume power. Power dissipation is an important issue in for instance portable applications.

The Young's modulus of silicon has a negative temperature coefficient, while the Young's modulus of silicon dioxide has a positive temperature coefficient. During global oxidation, an oxide skin is formed on all sides of the structure: top, bottom, and sidewalls.



FIGURE 5.6 – Temperature drift measurements on thermally oxidized resonators. The frequency is determined from uncalibrated S-parameter measurements in air. The four measurement series are made on an identical dogbone resonator design, but each with a different oxide thickness as indicated in the figure.



FIGURE 5.7 – For each of the four measurement series in Fig. 5.4 a temperature coefficient (TC) for the resonator is derived. In this figure, the TC's are plotted against oxide thickness. An oxide thickness just over 300 nm would result in a device with zero temperature drift. The compensation thickness is resonator design dependent, however.



During oxidation, 44 % of the SiO_2 thickness is formed from the initial silicon layer and 56% is growth on top of the initial silicon layer. This is depicted in Fig. 5.8.

FIGURE 5.8 – Cross-section of an oxidized bar of silicon.

With the optimum oxide thickness, a combined structure of two materials is formed with an effective Young's modulus that is constant over temperature. The temperature drift of the MEMS resonator is then reduced to zero. The temperature dependent Young's moduli of silicon and silicon dioxide are given in Eq. 5.1, with a reference temperature of 20 °C.

$$E_{Si} = 131[GPa] \cdot (1 - 60 \cdot 10^{-6} [K^{-1}]\Delta T)$$

$$E_{SiO_{3}} = 73[GPa] \cdot (1 + 196 \cdot 10^{-6} [K^{-1}]\Delta T)$$
(5.1)

Experiments are performed on a dogbone structure (Fig. 2.10). The springs of the dogbone are 20 μ m long and 10 μ m wide, while the lumped mass is 35 μ m in length and 64 μ m in width. The nominal frequency of the design before oxidation is 19 MHz, which is clearly lower than the design used in the oven-control experiments. Various wafers are prepared with different thicknesses of the oxide skin. The devices are measured at atmospheric pressure on a heating chuck. The wafer is heated to temperatures up to 140 °C. By stepping through the temperature range the temperature coefficients (TC's) of the thermally oxidized devices are determined

Measurements show that for a thin oxide skin the TC of the oxidised device is still negative (Fig. 5.6). The negative TC is smaller, however, as compared to the 30 ppm/ °C measured for the unoxidised device. When the oxide thickness is increased the negative TC decreases and finally a positive TC is reached. This shows that the temperature drift can

indeed be eliminated with a combined silicon-silicon dioxide sandwich structure. When we plot the measured TC against oxide thickness a linear increase is found (Fig. 5.7). An optimal oxide thickness of 312 nm is found for this dogbone device.

The optimal oxide thickness can also be calculated analytically. In a simple analytical model we assume that the stiffness of the dogbone resonator is only determined by the two springs. The spring beams are stretched longitudinal. The stiffness of a longitudinal stretched beam is proportional to the Young's modulus and the area of the cross-section. To find the optimal oxide thickness t_{ox} , we need to solve Eq. 5.2, where *E* is the Young's modulus and *A* the cross-section area.

$$\frac{\partial \left(E_{Si}(T)A_{Si}(t_{ox}) + E_{SiO_2}(T)A_{SiO_2}(t_{ox})\right)}{\partial T} = 0$$
(5.2)

The Young's moduli of silicon and silicon dioxide are given by Eq. 5.1, while Fig. 5.8 explains how the total cross-section area of the two materials depends on the oxide layer thickness. Equation 5.2 results in a second-order polynomial for t_{ox} . When we solve for the dimensions of the measured dogbone, namely a spring width of 10 µm and an initial silicon layer thickness of 1.5 µm, the analytical model predicts an optimal oxide thickness of 286 nm. This is 8% lower than the optimal thickness extracted from measurements. Sources of inaccuracy are the material parameters and the simple modeshape that is assumed. With FEM simulations, the complex 2D eigenmode of the dogbone resonator can be taken into account.

The Young's modulus of silicon also has a second-order dependency. Measurements on the four oxidized devices show that the second-order drift is independent of the oxide thickness and accounts for about 100 ppm frequency inaccuracy over 100 °C.

5.3.2 Simulations

A FEM model is developed in Comsol to simulate the effects of global oxidation. This FEM model can be used during device design, since the optimal oxide thickness is device design dependent. Since we simulate the effect of global oxidation, the model is 3D. As before with the simulations for initial accuracy, the model is written in Comsol Script.

The model simulates the effects of the oxide skin on the temperature drift and the nominal frequency of the device. In Fig. 5.9 the results for a 48 MHz dogbone resonator are plotted. During oxidation, a relative spread in oxide thickness of 5% is anticipated. FEM simulations show that the linear temperature will be found between -1.5 and 1.5 ppm/K. This results in a frequency spread of 150 ppm over temperature range. For the nominal frequency, spread is much larger. The 5% inaccuracy during oxidation results in a nominal frequency spread of +/- 3000 ppm. Hence, the reduced temperature drift is offset by an increased nominal frequency inaccuracy.



FIGURE 5.9 – FEM simulation in Comsol showing the effect of 5% inaccuracy in oxidation thickness. The temperature drift (Tdrift, \Box) and the spread in nominal frequency (Δf , Δ) are plotted for three oxide skin thicknesses t_{ox} . The dogbone design has a nominal frequency of 48 MHz.

5.4 REDUCED TEMPERATURE DRIFT

The frequency of the silicon MEMS resonator drifts -30 ppm/°C. Over a temperature range of 100 °C, which is typical for many applications, this leads to 3000 ppm spread in frequency. To reduce the temperature drift we have proposed thermal oxidation of the silicon resonators and an oven-control circuit. In this final section we compare the performance of these two concepts.

	Thermal oxidation	Oven-control
Advantage	Low powerEasy to processLow cost	 Total frequency spread < 100 ppm Easy to implement Trimming of initial +/- 150 ppm frequency spread
Disadvantage	 Residual linear temperature drift: 150 ppm Second-order temperature drift: 100 ppm Initial frequency spread 3000 ppm Optimal oxide thickness design (frequency) dependent 	 High power ≈ 8 mW Cost (IC, trimming) Accurate temperature sensor needed Temporal resolution?

TABLE 5.2 – The advantages and disadvantages of the two methods to reduce temperature drift. Absolute numbers stated in the table are calculated over a 100 $^{\circ}$ C temperature range. For the thermal oxidation we assume that during processing, oxide layer thickness is controlled with 5% inaccuracy.

The preferred solution to reduce temperature drift would be the passive concept of thermal oxidation. This low-cost solution results in an intrinsic compensated structure. The main issue with this concept is that the oxide thickness is controlled only with finite precision. The nominal frequency of the device also depends on the oxide thickness. If we assume a tolerance of 5%, this implies an initial frequency inaccuracy of about 3000 ppm for the oxidized resonator. This is the same order of magnitude as the temperature drift over a 100 °C temperature range for the unoxidized resonator. For a successful application of the thermal oxidation concept we need a resonator design with a much lower sensitivity of the resonance frequency on oxide layer thickness [63]. A second issue is that the optimal oxide thickness is design specific. This means that processing several resonators of different resonance frequency on a single wafer is no longer possible.

The oven-control principle is not design specific, which is an advantage. Temperature drift can largely be eliminated by using a second-order compensation circuit. This solution

will require trimming to account for inaccuracy in resistors and other electrical components. An extra advantage is that this trimming step can also be applied to eliminate a few hundred ppm of the initial frequency inaccuracy of the resonator. The compensation circuit and the trimming step will add to the cost of the product, which is a disadvantage of this method.

The main issue with the oven-control is power consumption. The 8 mW consumed might be too high for many applications. In literature [10], a similar method is found that uses the bias electrode voltage to shift the frequency. This method is low power, but requires a low stiffness device with a large electrode area. This seems not very applicable to our thin SOI, high-frequency devices. Moreover, it results in a higher phase noise that will exclude wireless applications.

To reduce power consumption, thermal insulation of the device should be improved. A second method is to use multiple resonators to span the temperature range. Each resonator has a slightly different frequency and is used in a specific part of the complete temperature range. This reduces the maximum temperature difference between ambient and oven, which lowers the power consumption [64].

This chapter has shown that with both concepts it is possible to reduce temperature drift by more than a factor 10. Together with the geometrically compensated designs from the previous chapter this shows the potential for high-accuracy MEMS based oscillators.

CHAPTER 6

THE PIEZORESITIVE OSCILLATOR DEMONSTRATED

6.1 INTRODUCTION

In chapter 2, the piezoresistive readout has been compared to the more commonly found capacitive readout. For the piezoresistive resonator the resistance modulation due to the mechanical strain in the material is detected. A dc current is applied through the device and the ac resistance modulation induces an ac voltage component over the device. While the capacitive resonator is a passive component, the piezoresistive resonator is an active device, since it needs power input for its operation. With enough power input, the piezoresistive resonator is not the most effective amplifier, using a dedicated amplifier circuit is preferred.

The piezoresistive readout is insensitive to layer thickness or in-plane geometric scaling. This has been discussed in more detail in chapter three. This is a large difference with the capacitive resonator, where signal levels drop significantly if the in-plane dimensions or the layer thickness of the device are reduced. This makes the piezoresonator very attractive for high-frequency oscillators, especially in the thin, 1.5 μ m SOI used for MEMS processing at NXP.

In this chapter, a fully functional, 56 MHz piezoresistive oscillator is presented. Because, as people say: "The proof of the pudding is in the eating". A piezoresistive dogbone resonator is combined with an amplifier designed in the Advanced-Bipolar-CMOS-DMOS-2 (ABCD2 [65]) process by Murroni [66,67]. The choice for ABCD2 is made, since processing is also done on 1.5 μ m thick SOI substrates and the process has high voltage (120V) capability. The main aim of the design is functionality of the 2-die oscillator. Second, we want to assess the feasibility of the piezoresistive concept for low-noise, low-power oscillators

6.2 OSCILLATION CONDITIONS

An oscillator is an electronic circuit that produces a repetitive electronic signal, in this case a harmonic signal. Harmonic oscillators consist of a frequency selective element and a driving amplifier. An output buffer amplifier is added to read out the signal from the oscillator loop.

To sustain oscillation, two loop conditions have to be met. First, the loop gain has to be unity. Second, the loop phase has to be zero. These conditions are known as the Barkhausen criteria and are mathematically stated in Eq. 6.1. The transfer function of the loop depends on frequency. So the Barkhausen criteria have to be met for only one specified frequency $f_{0.}$ Otherwise, the output signal will not be a pure sinusoid.



FIGURE 6.1 – The oscillator is a feedback network of a frequency selective element (resonator) and a driving amplifier.

$$A_{f}(j\omega) = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)} \Longrightarrow \begin{cases} |A(j\omega)\beta(j\omega)| = 1\\ phase(A(j\omega)\beta(j\omega)) = 0 \end{cases}$$
(6.1)

The Barkhausen criteria are sufficient to sustain oscillation. To start-up oscillation, a gain greater than unity is needed. The signal can then build up from the electrical and mechanical noise in the loop. Without something to reduce the gain, the signal will grow indefinitely. The gain is eventually reduced to unity by an amplitude gain control circuit or by the intrinsic oscillator non-linearity. The choice between these two amplitude-limiting systems depends mainly on the required performance.

6.3 PIEZORESISTIVE RESONATOR

6.3.1 Deliverables

The piezoresistive resonator is an active device with voltage gain μ_m . In the ideal case, the transconductance g_m of the piezoresistive resonator is only loaded by the piezoresistor R_d . In that case, the voltage gain is given by:

$$\mu_m = g_m R_d \tag{6.2}$$

In all practical cases, the gain of the resonator will be smaller than one. It is therefore more intuitive to speak about resonator losses instead of resonator gain. For the design of the piezoresistive resonator, the following deliverables are stated:

- $f_0=52$ MHz. This is the required frequency for the demonstrator.
- μ_m as large as possible. The transconductance g_m will be optimised for a choice of R_d.
 Both the optimal choice of R_d and the optimisation of g_m will be discussed in the next sections.

6.3.2 Resonator design

Two piezoresistive resonator designs are used frequently, namely the free-free beam resonator and the dogbone resonator (Fig. 2.10). Both designs are bulk-acoustic-mode resonators and are suited for the high-frequency 52 MHz oscillator. Choice has been made to focus on one design. The dogbone resonator is chosen because:

- It is an original NXP resonator design by Van Beek [34], and is protected by IP.
- For the dogbone design, with FEM simulations we have shown that the design can be made insensitive to geometric offset¹.
- The dogbone is capable of higher g_m than the free-free beam design. This is due to the benefits of the mass head. First, the wide mass head increases the electrode area, which increases the electromechanical coupling. Second, the mass head concentrates the strain in the short springs of the dogbone. This leads to higher strain levels than found in the free-free beam design for the same vibrational amplitude.

6.3.3 The piezoresistor and the bondpad capacitance

For the piezoresistive resonator, the voltage gain is proportional to the current through the piezoresistor. However, the dc power dissipation in the device is proportional to the square of the current through the device. This means that if the power consumption in the device is fixed, more gain can be achieved by increasing the value of the piezoresistor.



FIGURE 6.2 – Electrical small-signal model of the piezoresistive resonator; the transconductance g_m is loaded by the parallel combination of R_d and C_p .

¹The free-free beam design can also be compensated for geometrical offset. This knowledge had not been developed at the moment the choice for the dogbone resonator was made.

$$\begin{cases} \mu_m \sim I_d R_d \\ P_{tot} = I_d^2 R_d \implies \frac{\mu_m^2}{P_{tot}} = R_d \end{cases}$$
(6.3)

in which μ_m is the voltage gain of the resonator. For the actual resonator on-wafer, the output of the resonator is read out via a bondpad. This bondpad and the electrical leads to the bondpad add capacitance to ground. The transconductance is loaded by the parallel combination of the piezoresistor R_d and the bondpad capacitor C_p . This means that the gain of the resonator at fixed power does not increase continuously with R_d . Instead, an optimum value for R_d is found that depends on the bondpad capacitance and the resonance frequency: $R_d=Z(C_p)$.

The bondpad capacitor also shifts the phase of the resonator. For the optimal situation where the piezoresistance is equal to the bondpad impedance the phase at resonance has shifted from 90° to 45°. For the 2-die oscillator demonstrator we have to take into account that the resonator die is wirebonded to the amplifier die. This means that the transconductance is loaded by both the bondpad on the resonator die as well as the bondpad on the amplifier die. (and the bondwire which represents an inductance of about 1 μ H per mm wire length. This is only relevant for RF oscillators.)

6.3.4 Minimising signal losses in the resonator

From the previous paragraphs we have learned that to minimize resonator losses we should optimise the value for the piezoresistance R_d and maximize the transconductance g_m of the resonator. The optimal value for R_d is discussed first.

Finding the optimal value for R_d starts with estimating the value for the bondpad capacitance. From the design rules of the MEMS resonator process [68] the minimum bondpad size is 80 x 80 μ m². This results in a capacitance of 250 fF, if we also add a small capacitance from the active silicon connected to the bondpad. Remember that for the actual 2-die oscillator, the resonator will be loaded by two bondpads. This means that the total bondpad capacitance is estimated to be 500 fF. This results in an impedance of about 6 k Ω at a frequency of 52 MHz.

Hence, the optimal value for R_d that will minimize losses in the resonator is 6 k Ω . The resonator design will have a resistance value of 2 k Ω . This results in an extra voltage loss of 0.6 dB. Main reason for the lower value of R_d is that the phase shift of the resonator needs to

be taken into account. This optimal combination of phase shift and gain depends on the amplifier design. A second reason is that the value of R_d depends on the geometry of the device and the resistivity of the silicon. The choice for the well dopes also depends on other experiments performed within the MEMSXO project.

To maximize the transconductance of the piezoresistive resonator, we take another look at the analytical expression. The transconductance at resonance depends on five factors that can be maximized independently. We will discuss each of the five factors.

$$g_{m}(\omega) = \frac{g_{m0}}{\left(1 - \frac{\omega^{2}}{\omega_{0}^{2}} + j\frac{\omega}{Q\omega_{0}}\right)}$$

$$g_{m0} = -V_{g}I_{d}\left(\frac{4\varepsilon_{0}}{\pi^{2}}\right)\left(\frac{K}{E}\right)\left(\frac{\alpha b}{g^{2}w}\right)\left(\frac{R_{mod}}{R_{tot}}\right)$$
(6.4)

- The bias conditions: The transconductance scales with the bias current I_d through the resonator and the gap voltage V_g . A high bias current is not attractive, since it increases the power consumption of the resonator. A high gap voltage also is not an advantage, since most IC processes have limited high voltage capability. In any case, a charge pump is needed to generate the high bias voltage. This charge pump will consume IC area (cost) and power. For the oscillator demo, both are applied externally.
- <u>The material factor</u>: The ratio of material constants K/E is optimal for a n-type silicon oriented in the [100] crystal orientation. Moreover, this orientation is very convenient, since the axes of the lithography fields on the 8-inch wafer are aligned along this orientation. The gauge factor K=-153 and Young's modulus E=130 GPa for this orientation. The gauge factor depends on temperature and impurity concentration [69].
- <u>Q-factor</u>: The Q-factor should be very high. The balanced operation mode of the dogbone resonator will allow for high Q-factors [33].
- <u>The geometrical factor</u>: The width g of the actuation gap should be as small as possible. This is determined by the process capabilities. DUV tools in ICN8 are able to create measured trench widths as small as 270 nm. The factor *α* accounts for the amount of spring concentration in the resonator springs, as given by:

$$\alpha = \frac{1/L \int_{0}^{L} \varepsilon dx}{1/(L+a) \int_{0}^{L+a} \varepsilon dx}$$
(6.5)

with L the length of the springs, L+a the total length of the device (thus including the lumped mass) and ε the local strain along the length of the device. Together with the ratio b/w, these two factors are determined by the geometrical design of the resonator. The optimal design has a very wide mass head connected to short and slender springs. Bending of the mass head should be avoided, since this will cause strain in the mass head, but not in the springs [70].

• <u>MTTR ratio</u>: The ratio R_{mod}/R_{tot} accounts for the parasitic resistance in the current path through the resonator. Only the resistance of the resonator springs is modulated by the movement of the resonator. Parasitic resistance added by the suspension and anchors add to the total resistance but not to the amount of resistance modulation (Fig. 6.4). This can significantly reduce the relative resistance change. With two well dopes that have a resistivity ratio of 10:1 the relative amount of modulated resistance can be increased. Our results show an improvement by a factor 4.5 as compared to designs with a single well dope [71]. This is depicted in Fig. 6.3.

6.3.5 Results

The measured resonator voltage losses at resonance are 10 dB with a phase shift of 68°, taking the second bondpad on the amplifier die into account. This is measured for an electrode voltage of 20V and a current of 1 mA through the resonator. The power consumption in the resonator at this current is 2 mW.

The resonator and amplifier are processed in parallel. The amplifier has been designed according to predicted resonator values. For the resonator, a phase shift of 70° and losses smaller than 20 dB are specified. Since the values for the piezoresistor R_d and bondpad capacitance C_p are on target the measured phase shift is very close to specification. The losses in the resonator are kept low due to a combination of high Q-factor, low parasitic resistance and high b/w ratio. If the amplifier is able to deliver the +20 dB gain specified, the electrode voltage and power consumption of the resonator might even be reduced.



FIGURE 6.3 – The figure shows the current path through the dogbone resonator. Only the resistance in the resonator springs is modulated. The resistance in the anchors and suspension is parasitic resistance and decreases the relative resistance modulation.



FIGURE 6.4 – The transconductance g_{m0} scales with the product of the bias current and the bias voltage, as can be understood from Eq. 6.4. The graph shows measurement results on three resonators that are of identical geometry, but have different well dopes: single high well-dope resulting in $R_d=7$ k Ω (Δ), single low well-dope resulting in $R_d=700 \Omega$ (•), and the optimised two well-dope design (\Box). An increase of a factor 4.5 in transconductance has been obtained. The transconductance has been derived from calibrated S-parameter measurements in vacuum.

TABLE 6.1 – The table shows the dimensions of the dogbone resonator for the oscillator demo. Furthermore, the mechanical and electrical parameters extracted from measurements are depicted. The resonator has a -10 dB voltage loss at resonance and a phase of 68° . The actual resonator phase from measurements is higher. In this number, the effect of the second bondpad on the amplifier die has already been taken into account.

Parameter	Symbol	Value	Units
Spring length	L	6.0	[µm]
Spring width	W	3.0	[µm]
Mass head length	a	13.4	[µm]
Mass head width	b	20.0	[µm]
Transducer gap	g	0.27	[µm]
Effective mass	m_{eff}	1.66	[ng]
Effective spring constant	k_{eff}	207	[kNm]
Resonance frequency	f_0	56.1	[MHz]
Quality factor	Q	30k	
Electrode bias voltage	V_{g}	20	[V]
Bias current	I_d	1	[mA]
Motional resistance	R_m	516	$[k\Omega]$
Motional inductance	L_m	32.2	[H]
Motional capacitance	C_m	0.25	[aF]
Shunt capacitance	C_s	16.5	$[\mathbf{fF}]$
Piezoresistor	R_d	1.98	$[k\Omega]$
Bondpad capacitance	C_p	192	$[\mathbf{fF}]$
Transconductance	g_{m0}	6.20	[nS]
Transconductance at	~	0.10	[mS]
resonance	gm,max	0.19	
Gain	A_{v}	-10.0	[dB]
Phase	arphi	68	[deg]

The resonance frequency of 56.1 MHz is higher than intended. This is due to an error in the mask layout. Where a width of 2.5 μ m had been intended for the resonator springs, a width of 3 μ m is drawn on the mask layout. The resonance frequency is proportional to the square root of the spring width. The ratio of the two frequencies is f₁/f₂=56.1/52=1.079, while the square root of the ratio of the two spring widths is $\sqrt{(w_1/w_2)} = \sqrt{(3.0/2.5)} = 1.095$. As a result, the higher resonance frequency can be explained by the difference in intended and actual spring width. Since the amplifier characteristics do not change significantly in this frequency range, the design error does not affect the functionality of the oscillator.

6.4 ABCD2 AMPLIFIER

6.4.1 Deliverables

The amplifier compensates for the losses and the phase shift in the resonator, so the Barkhasusen criteria are met. The design of the amplifier has to meet the following deliverables:

- Voltage gain larger than 20 dB.
- Amplifier phase shift $-70^\circ \pm 25^\circ$.
- Power consumption less than 5 mW.
- Amplifier functionality guaranteed over statistical process variations.

Meeting the phase condition is regarded as the highest risk in the oscillator design. Especially since the loop phase of the oscillator cannot be tuned externally. With the high gain of the amplifier, headroom is created regarding the losses in the resonator. This enables the specification for the amplifier phase shift to be relaxed. Time constraints did not permit the design of an amplitude-gain-control circuit.



FIGURE 6.5 – The gain stage includes the amplifier core and the replica bias circuit. The input signal is provided by terminal v_{in} and is decoupled via an input capacitor. The amplifier contains two gain stages and a buffer stage to read out the signal from the oscillator loop.



FIGURE 6.6 – The mask layout of the ABCD2 amplifier chip. Size of the chip is 0.97 x 1.22 mm².

6.4.2 Amplifier design

The amplifier chip has been designed in the ABCD2 process [65] by Murroni [66,67]. The choice for ABCD2 is made, since processing is also done on $1.5 \mu m$ thick SOI substrates and the process has high voltage (120V) capability. High voltage is needed for the electrode bias voltage of the MEMS resonator.

The amplifier design consists of an output buffered, two-stage amplifier that operates at 3V. The two identical gain stages and the output buffer have been entirely designed with lateral npn bipolar transistors. Bipolar transistors have a superior noise performance over MOS devices. Disadvantage is that bipolar transistors in ABCD2 are slow (f_T =200 MHz). As a rule of thumb, the value of f_T should be at least ten times the oscillation frequency. This means that an f_T of 520 MHz would have been required. For the amplifier design in ABCD2, parasitic effects dominate the amplifier response at 52 MHz. This makes it difficult to achieve the desired gain with a simple design.

The core of the gain stage (Fig. 6.5) is a cascaded common-collector common-emitter configuration, also known as a CC-CE cascade. Two stages are needed, since the required gain and phase could not be achieved with a single stage. The gain of the single stages has been improved by replacing all MOS biasing current mirrors by resistors. This decreases the total capacitance to ground, which improves the limited gain-phase performance of the amplifier.

The amplifier circuit is biased with a replica bias technique. The bias is determined by a replica of the amplifier circuit, which is self-biased through a negative feedback loop. The negative feedback guarantees stability of the bias against temperature and process variations.

An on-chip current mirror is designed to supply the bias current to the resonator. If the current would be supplied externally, the drain of the resonator needs to be connected to an external pin. This would load the resonator and cause a significant drop in resonator gain.

6.4.3 Results

The performance of the amplifier IC has been evaluated on five samples. All five samples are functional. The amplifier needs a voltage supply of 3V and consumes 5.1 mW power. It is able to deliver 20 dB gain at a phase shift of -70°. Measured gain and phase of the individual samples are all within a five percent range of the average values stated above. This means that process variations do not significantly change the amplifier performance, which is one of the deliverables. The design has been realised according to specifications. The layout of the amplifier design, which is about 1 mm² in size, is depicted in Fig. 6.6.

6.5 THE FUNCTIONAL OSCILLATOR

The MEMS resonators are open, meaning they are not covered by a cap or a scratch protection layer. Separating single dies of open MEMS structures from a wafer is a challenging task. The standard procedure in IC technology uses a diamond saw to separate the dies. For the MEMS devices, this technique cannot be used. Sawing is a harsh process that introduces a lot of vibration. This might damage the mechanical structures. More importantly, sawing is a wet process, since the saw blade needs to be cooled with water. This would lead to sticking of the open MEMS structures during drying.

The MEMS dies are therefore separated by laser dicing. With standard laser dicing, the laser beam cuts through the silicon. During cutting, debris from the removed material land on the surrounding silicon. This results in very few functional devices after dicing. A second laser-dicing method leads to a much higher yield. The laser beam focuses inside the wafer.

Local heating and subsequent cooling induce small micro-cracks in the amorphized silicon. Since no material is removed, the devices are kept 'debris free'. After laser treatment the wafer is put on foil and stretched, separating the individual dies.

To demonstrate the functionality of the oscillator, the amplifier die and resonator die are placed in a single ceramic DIL24 package. Die-to-die and die-to-pin connections are made by wire bonds. Next, a test board is soldered. The board contains SMA connectors for the bias connections and the signal output from the oscillator buffer. Furthermore, capacitors and resonators are added to decouple all input and output signals. The oscillator samples are measured in a stainless steel vacuum chamber (section 2.7). From the 15 bonded oscillator samples, all have shown good functionality. This supports feasibility of the piezoresistive MEMS oscillator concept.

As has been explained in paragraph 6.3.4, the gain of the resonator is proportional to the product of gap voltage and bias current. Therefore, the two are interchangeable, where an increase in bias current leads to a higher power consumption of the resonator. For the oscillator measurements in vacuum, oscillation is sustained for a gap voltage as low as 7.2V with a bias current of 2 mA. Conversely, the bias current can be reduced to 0.5 mA with a gap voltage of 20V. Typical bias conditions are 12.6V gap voltage and 0.7 mA bias current, which result in a total power consumption for the oscillator of 6.1 mW.

Pressure dependent measurements have also been performed on the oscillator. The pressure inside the vacuum chamber is increased slowly, which increases damping of the resonator movement. This leads to a lower Q-factor and thus higher losses in the resonator. At a certain pressure the gain condition is no longer met and oscillation cannot be sustained. For V_g =30V and I_d=2mA, oscillation can be sustained to a pressure of 440 mbar.

The phase noise performance of the oscillator is measured with an Agilent E5052B Signal Source Analyser. We measure a phase noise of -102 dBc/Hz at 1 kHz offset from carrier and -113 dBc/Hz floor at far from carrier offsets (Fig. 6.8). In order to compare with state-of-the-art performance [8], the measured 1 kHz point needs to be translated from 56 MHz to 13 MHz. If the frequency is divided down, this translates into -115 dBc/Hz at 1 kHz from a 13

MHz carrier. This is higher than required for the most demanding applications mostly found in wireless applications. GSM requires a phase noise specification of -130 dBc/Hz at 1 kHz from a 13 MHz carrier.

The near-carrier spectrum shows a drop of 30 dB/decade. This is a clear indication of 1/f noise intermodulation around the carrier. This degrades the near-carrier noise performance.

Furthermore, the phase noise performance suffers from a low signal level in the oscillator core. By increasing the signal level inside the oscillator core and decreasing the 1/f noise added by the circuit components, phase noise performance of the piezoresistive oscillator can still be improved. With the near-carrier noise performance achieved and the potential for further improvement, the demonstrator shows that a piezoresistive MEMS oscillator is able to achieve demanding phase noise specifications.



FIGURE 6.7 – The demonstrator: in (a) the ABCD amplifier die and the MEMS resonator die are placed in a single ceramic DIL-24 package. The resonator die is larger, since it contains one module with four resonator devices. The wire bonds between the two dies and between the single dies and package can be seen. In (b), the buffered output of the oscillator is presented on a spectrum analyser.



FIGURE 6.8 – The phase noise spectrum of the oscillator measured at bias settings V_g =12.6V and I_d=0.7mA.

Parameter	Symbol	Value	Units
Oscillation frequency	f_{osc}	56.1	[MHz]
Power consumption Amplifier Resonator	P_{tot} P_{amp} P_{res}	6.1 5.1 1.0	[mW]
Operation voltage	V_{DD}	3.0	[V]
Gap voltage	V_g	12.6	[V]
Start-up time	t	1.0	[mS]
Phase noise performance			
10 Hz	I	-48	[dBc/Hz]
1 kHz	L_{f}	-102	[dBc/Hz]
Floor		-113	[dBc/Hz]

TABLE 6.2 – The measured performance of the piezoresistive, MEMS oscillator.

6.6 IMPACT OF THE SUCCESFUL DEMONSTRATOR

With this demonstrator, the main goal of this project has been achieved: a fullyfunctional, piezoresistive MEMS oscillator. With the demonstrator, the project takes a major step towards product development. The oscillator achieves a phase noise of -102 dBc/Hz at 1 kHz offset from carrier with a total power consumption of 6.1 mW. This shows that lownoise, low-power applications are feasible with the piezoresistive concept.

For future oscillator designs, the choice of the IC process needs to be reconsidered. In the current design, the slow speed of the lateral-npn bipolar transistors made it difficult to achieve the required gain-phase performance. As a result, the amplifier design contains a lot of resistors, which increase the power consumption of the amplifier. With a process more suited to the high 56 MHz resonance frequency, the power consumption of the oscillator can be reduced.

For the future resonator design, process spread compensation and temperature drift of the resonator should be considered. The need for a process-compensated design will give trade-offs with the optimisation of the transconductance g_m . For high g_m short and slender springs are beneficial, but this makes the design very susceptible to process-induced geometrical variations.

To reduce temperature drift, the oven-control concept seems to be most feasible at this moment. With the oven-control, the temperature drift over 100 °C can be reduced to values well below 100 ppm. Moreover, the oven-control will require trimming, which can be used to compensate for the residual spread found in the process-compensated designs. An accuracy target of \pm 50 ppm is challenging, but seems to be within reached. Efforts should focus on keeping the power consumption down.

This demonstrator has been a breakthrough in the MEMS oscillator project at NXP, since it is the first time a successful 2-die oscillator has been made. The impact of the demonstrator is two-fold. First, the project gains valuable knowledge from measurements of the oscillator. Analysis of the phase noise of the oscillator has already given valuable insight on the importance of resonator power handling. The insight provided by this demonstrator will help taking steps forward in a next design. Second, this demonstrator is used to create support and business for the project inside the NXP organisation. The demonstrator shows that we have a working concept for low-power, low-noise applications. Again, as people say: "the proof of the pudding is in the eating".

CHAPTER 7

EVALUATION AND PERSPECTIVE

7.1 EVALUATION

7.1.1 Deliverables

This PhD on design has been performed as an integral part of the MEMS oscillator project within NXP Semiconductors. The MEMS resonators are processed on 1.5 μ m thick SOI wafers. The layer thickness has been an important boundary condition for the device design. At the start of the PhD thesis, goal was stated to look at the possibilities to scale MEMS resonator to frequencies above 26 MHz. The main deliverable of the work was a functional 52 MHz MEMS oscillator. Later, as the work evolved, the goal has been extended to look at frequency scaling of MEMS resonators in thin SOI.

Reflecting on the results of the project, we can conclude that the deliverables have been achieved. Resonators have been scaled to frequencies above 400 MHz. The frequency selectivity of the piezoresistive and capacitive resonator have been compared. For the 1.5 μ m thick resonators above 10 MHz, the piezoresistive resonator is preferred over the capacitive resonator (chapter three).

A fully-functional, two-chip MEMS oscillator has been presented in chapter six that combines a 56 MHz piezoresistive MEMS resonator with an ABCD2 amplifier. This demonstrator has a large impact on the MEMS oscillator development at NXP. The results of the demonstrator are used to find new business support and future demonstrators can be developed from the knowledge gained with this demonstrator.

The results of this project go beyond scaling and the development of the demonstrator. We have also been able to address some of the key issues in MEMS oscillator development, like power consumption, phase noise, and frequency accuracy. We would like to restate the most important results that have obtained. Based on these results a MEMS oscillator concept will be presented. We will compare the expected performance of this concept to other MEMS concepts and to substitutes as quartz and LC oscillators.

7.1.2 Results

Scaling to higher frequencies is unattractive with electrostatic actuated and capacitive read out MEMS resonators. To reach higher frequencies, the size of the device has to be scaled down. This means smaller electrode area and, since the electromechanical coupling coefficient η is proportional to the electrode area, the transduction becomes less effective. Therefore, the impedance R_m at resonance scales quadratically with frequency, while the parasitic impedance C_s remains constant. Frequency selectivity Δ_s is lost at high frequencies.

With a piezoresistive resonator, the transduction principle is insensitive to layer thickness or geometric scaling. Selectivity is only lost at higher frequencies due to a drop of the Qfactor. With the patented dogbone design the 56 MHz 2-die oscillator has been made. The dogbone is an optimised structure capable of higher transconductance g_m than for instance the free-free beam resonator. The demonstrator shows that high-frequent oscillators are feasible with the piezoresistive resonator. Functional resonators with frequencies up to 400 MHz have been demonstrated (chapter 3).

With the piezoresistive MEMS oscillator, demanding phase noise specifications often found in wireless applications can also be reached. With the 56 MHz oscillator, we have demonstrated -102 dBc/Hz at 1 kHz offset from carrier. This is equivalent to -115 dBc/Hz at 1 kHz offset from a 13 MHz carrier, which is still 15 dB off from current GSM specifications of -130 dBc/Hz. For the current demonstrator, phase noise can be improved significantly by increasing the signal level inside the oscillator loop. For future piezoresistive MEMS oscillator, a phase noise level below -120 dBc/Hz at 1 kHz offset from a 13 MHz carrier is feasible.

To increase accuracy, the resonator design is compensated for geometrical offset (chapter 4). Temperature drift is reduced with oven-control (chapter 5). Both methods are patented. Geometrical offset is the dominant source of initial frequency spread. For a 52 MHz square plate resonator, initial frequency spread is about +/- 500 ppm for a geometric offset of +/- 20 nm. The initial frequency spread depends on resonator design and frequency. For a 52 MHz square square plate design compensated for geometrical offset, the frequency spread has been reduced to +/- 150 ppm. The source of this spread is no longer geometrical offset, however. If we can find the sources of the residual spread, initial accuracy can be improved still.

One of the important benefits of the oven-control is that it can be used to trim the frequency after processing. Increasing or decreasing the oven temperature a few degrees shifts the resonance frequency. Remember that an increase of 1 °C decreases the frequency by 32 ppm. Since we have not found the sources of the residual spread yet, trimming has to be used to create highly accurate oscillators.

In the oven-control experiments, an accuracy of 150 ppm over 70 °C has been shown, at the expense of 8 mW power dissipation in the device. With a second-order compensation this accuracy can be improved significantly. Frequency accuracy below 50 ppm over a 100 °C temperature range is realistic. With the oven-control concept, it will be crucial to get the power consumption down. Power consumption can be reduced by improving the thermal insulation of the device. Furthermore, an array of devices can be used that each have a slightly different resonant frequency (chapter 5).

7.2 PERSPECTIVE

7.2.1 Integration

SOI wafers are convenient to use in MEMS processing, since the buried-oxide-layer can be used as a sacrificial layer. A strategic choice has been made to process the MEMS resonators on $1.5 \mu m$ thick SOI substrates, the same substrates as used for the ABCD

processes. The advantage of the ABCD processes is their high-voltage capability (ABCD2 up to 120V). High bias voltage is needed in the electrostatic actuation (and capacitive readout) of the MEMS resonators. Processing MEMS on identical substrates as the IC opens the possibility of integrating MEMS devices in the IC process.

Integration of components has a long history in silicon microelectronics. While certainly not straightforward, integration of MEMS components is attractive. Performance-limiting parasites that result mainly from bondpads and bond wires are eliminated by monolithic integration. Signal levels at least two-orders of magnitude smaller can be processed on-chip as compared to off-chip [72, 73]. Moreover, an integrated system can be trimmed on-wafer. This saves time and extra pins that would otherwise be necessary when trimming on package level.

Downside on integration is that the initial development time is longer and requires more investments that will only be retrieved on the long run with high volumes. This makes a multi-die solution attractive, where a modular approach can speed up the development. Moreover, the process of the two dies can be optimised independently.

The decision whether or not to go for integration is not easy, since the arguments can be difficult to quantify. In the long run, we feel that monolithic integration is the preferred solution. A patented process route has been developed for integration of MEMS into the ABCD process [74]. This route is MEMS first without releasing the MEMS and does not add topography to the wafer. This means that CMOS processing can be done without any restrictions. Only after backend processing the structures are released. The MEMS resonators are processed in mono-crystalline silicon. This is a well-characterized material with high reliability and high gauge factor for the piezoresitive readout.

The ABCD3 process would be suited for high-frequency oscillators (Table 7.1). The thin SOI of the ABCD processes matches well with the piezoresistive read out. Low-frequency capacitive resonators for clock applications will probably require a thicker SOI layer.

7.2.2 MEMS oscillator concept

Due to the large parameter space for a MEMS oscillator, it is easy to lose overview. When developing a concept, you are forced to connect the individual physical properties. Working from a concept allows you to gain focus on the key elements. In this paragraph we would like

to present such a concept. The choices are funded on two pillars. First, the concept should be adapted to the specific knowledge and patents developed within the company or otherwise be allowed for use. Second, the concept should be ready for industrialization. Elements with large uncertainty are eliminated.

Parameter	Value	Units
Frequency	10 - 400	[MHz]
Accuracy incl. Temperature drift over 100 °C	+/- 50	[ppm]
Power consumption	< 5	[mW]
Phase noise at 1 kHz offset from 13 MHz carrier	< -120	[dBc/Hz]

TABLE 7.1 – Projected performance of the oven-controlled, piezoresistive MEMS oscillator.

The concept we propose is the result of the work of this thesis and the work of the MEMSXO project team. The concept is based on a piezoresistive dogbone resonator integrated into the ABCD3 process. The dogbone resonator is compensated for geometrical offset. Temperature drift is compensated with an oven-control circuit that needs to incorporate a temperature sensor. This is another reason to integrate, so the temperature sensor can be placed very close to the MEMS resonator. The compensation circuit will control both the current through the resonator and voltage over the electrode gap. The current is controlled to keep the resonator temperature stable, while the gap voltage is used to keep the gain of the resonator constant. A drop in current is compensated by a proportional increase of the gap voltage. The oven-control is used to trim the 100-200 ppm initial frequency spread of the compensated dogbone designs.

Ho et al [10] presented an oscillator where the drift over temperature is compensated by the bias electrode voltage. They designed a low stiffness resonator with a large electrode area that has a resonance frequency strongly dependent on electrode gap voltage. The initial frequency accuracy is achieved with a geometric offset compensated design [54]. This concept is attractive, since tuning with the electrode gap voltage does not consume much power (<1 mW). The concept does not seem suitable for high-frequency oscillators (that require larger stiffness for the resonator) and on top of that requires a very stable bias voltage.
(Stabilization over a 100 °C ambient temperature range with a precision of 30 ppm requires 1% accuracy for the bias voltage.) Most likely, the phase noise performance from the oscillator will suffer from bias voltage instability.

In another approach followed by SiTime, temperature drift and initial frequency inaccuracy is compensated for by a PLL. This solution is easy to implement and enables highly-accurate oscillators with flexible frequency. However, a PLL consumes power and degrades the phase noise performance. From these three concepts, tuning with bias voltage is best for low-power, oven-control is best for phase noise performance, and with a PLL the highest frequency accuracy is achieved.

7.2.3 Competitor benchmark

The concept presented in the previous paragraph will be named the ABCD concept from now. We would like to compare the expected performance of this concept to the performance standard set by a number of competitors on the market. First, these are the quartz crystals that now serve the bulk of the timing market. There are over 100 manufacturers of quartz crystals that operate in the \$4.1 billion timing market. Second, two MEMS start-up companies SiTime and Discera try to gain a small share of the timing market with their own MEMS concept. SiTime has a flexural mode resonator in thick SOI that is etched with patented DRIE technology from Bosch. The MEMS is capped with a thin-film polysilicon layer and wirebonded on top of a CMOS amplifier die. Discera uses traditional semiconductor processes for their MEMS resonators in thin SOI. The MEMS are sealed with a die-to-die cap. Next, the amplifier die and MEMS die are connected with flip-chip technology. Both Discera and SiTime incorporate a PPL in their oscillator design to reach high accuracy levels and offer a wide range of frequencies. Finally, start-up Mobius offers LC oscillators in CMOS technology. In Table 7.2 we compare the projected performance of the ABCD concept with these competitor concepts.

In table 7.2 the performance of a companies concept on each parameter has been reduced to a single number. Most companies offer a wide range of products, however, especially quartz vendors. For quartz oscillator there is an enormous range in package sizes, accuracies, and corresponding cost. The table intends to display how different concepts size up against each other. Quartz oscillators still have superior performance, but are bulky. The two MEMS oscillator start-ups offer smaller packages with much shorter lead times and improved mechanical robustness. They are able to meet high-accuracy specifications over a significant frequency range. However, they still consume significant more power and lack the superior phase noise performance. The LC oscillator can be interesting for applications where phase noise performance is not important. However, power consumption is highest.

The ABCD concept is more promising with respect to power and noise performance. But where the two MEMS start-ups have already started shipping products, product development still has to start for the ABCD concept. The only single chip solution is the LC oscillator of Mobius. By monolithic integration of the MEMS resonator, the ABCD concept can distinguish itself from the two other MEMS oscillator start-ups. Integrated MEMS offer the advantage that it reduces the number of components for clients, which still use quartz crystals.

Parameter	ABCD	SiTime	Discera	Mobius	Quartz
Cost [\$c]	?**	11	17	9	15*
Size [mm]	2.0x1.5x0.8	2.5x2.0x0.85	2.5x2.0x0.85	5x3.2x0.9	7.1x5.1x1.5
Frequency [MHz]	10-400	1-110	1-150	10-100	1-150
Accuracy [ppm]	+/- 50	+/- 50	+/- 50	+/- 100	+/- 20
Power [mW]	5	10	12	76	4
Phase noise [dBc/Hz @ 1 kHz offset]	-110	-70	?	-65	-120

TABLE 7.2 – Various concepts compared on critical performance parameters for a 48 MHz oscillator. The data has been collected on company websites [48, 75-77] and from a market survey [8]. This table has been presented on the MEMSLand consortium meeting in December 2008.

* Average selling price

** Company confidential

7.2.4 Outlook

Significant effort over recent years has been devoted to the design of the resonator and resonator processing. With the FEM and analytical models developed we are able to optimise the transconductance g_m of the dogbone resonator and compensate the design for geometrical offset. We are also able to reliably predict the electrical performance of the device. In this final paragraph we would like to address some of the issues that need to be addressed in the future.

For the resonator, the sources of residual spread should be identified. If we find the cause of this residual spread, a solution could be invented to reduce these effects. This can reduce the level of trimming needed and improve the frequency accuracy of the resonator still. Another focus area is the power handling and corresponding non-linear behaviour of the device. While we have gained knowledge and understanding on this topic [78], it is now necessary to transform this knowledge into design guidelines.

In the area of IC design, a redesign of the current amplifier is needed. This should be done in a faster process, better equipped for a 52 MHz oscillator design. A charge pump and an amplitude-gain-control circuit will have to be added, and the oven-control circuit with second-order compensation has to be designed. All of this has to be achieved with minimum power consumption.

The 56 MHz oscillator demo has shown feasibility of a low-power, low-noise piezoresistive oscillator. The proposed concept can compete with quartz crystals. In a benchmark with MEMS competitors the concept scores well on phase noise, making it most suited for wireless applications.

CHAPTER 8

CONCLUDING REMARKS

The work of this PhD on design has been evaluated in the previous chapter. The main results of the project have been discussed and we have given recommendations for future work. In this final chapter we would like to take an extended view on the design thesis. What broader insight has been gained from this thesis on design? What important trends are seen in the MEMS oscillator field? This is done with a list of concluding remarks.

- In chapter 6 the piezoresistive oscillator is demonstrated. A piezoresistive 56 MHz dogbone resonator has been designed for this purpose. The identical resonator design is used for the next demonstrator in the MEMS oscillator project at NXP. It is accompanied by a redesign of the amplifier IC. This shows the performance standard achieved with this resonator design.
- The largest quartz manufacturer Epson Toyocom has recently presented its first QMEMS [79] oscillator. The clock chip resonator is made by processing quartz wafers using photolithography, etching, metallisation and sacrificial-layer removal the same steps used to make silicon MEMS chips. This clock chip offers significant size reduction, while still offering the high performance standard of quartz. This can be seen

as a defensive action by the quartz manufacturers to vend off entry of the MEMS oscillator start-ups into the timing market. A clock chip made from quartz does not suit monolithic integration with CMOS.

- SiTime has recently presented an ultra-thin MEMS oscillator that measures only 0.25 mm in height. Ultra thin oscillators can be used in for instance smart card applications. This is a very strategic market for MEMS oscillators, since such thin oscillators are still not possible with quartz technology.
- An important device parameter of the MEMS resonator is the Q-factor. Currently, we do not have a design method for high Q. Empirically, we have found that the Q-factor can change considerably from one design to the next, sometimes without apparent reason. Also, drift of Q-factor over time is observed. These issues are known in quartz crystal technology, where the Q-factor (and R_m) is not specified. Since we have been studying open MEMS so far, future will show the stability of the Q-factor for packaged resonators.

Traditionally, NXP has operated in niche markets of the semiconductor industry. With its class of ABCD IC-processes it has become a dominant player in the automotive industry. MEMS offer a new opportunity to enter such a niche market. In this work, a MEMS reference oscillator concept has been presented that is up to standard with competitors' performance in terms of phase noise, power, and accuracy. Product and process development will still require a few years of effort. Main thing to realise is the large difference between MEMS technology and traditional IC technology; like wafer handling, and the assembly and packaging of MEMS dies. These topics have still been too far off from the work in this thesis that has presented the progress made in resonator device design and oscillator concepts. We hope it contributes to the continued efforts by NXP in MEMS development.

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SUMMARY

Mechanical resonators are widely applied in time-keeping and frequency reference applications. Mechanical resonators are preferred over electrical resonators because of their high Q. In the \$4.1 billion (2008) timing market, quartz crystals are still ubiquitous in electronic equipment. Quartz crystals show excellent performance in terms of stability (short-term and long-term), power handling, and temperature drift.

MEMS resonators are investigated as a potential alternative to the bulky quartz crystals, which cannot be integrated with IC technology. MEMS offer advantages in terms of size, cost price, and system integration. Efforts over recent years have shown that MEMS resonators are able to meet the high performance standards set by quartz. Critical success factors are high Q-factor, low temperature drift, low phase noise, and low power. This PhD thesis addresses the feasibility of scaling MEMS resonators/oscillators to frequencies above 10 MHz. The main deliverable is a 52 MHz MEMS-based oscillator.

The MEMS resonators at NXP are processed on 8-inch silicon-on-insulator (SOI) wafers, with a SOI layer thickness of 1.5 μ m and a buried oxide layer thickness of 1 μ m. The strategic choice for thin SOI substrates has been made for two reasons. First, MEMS processing in thin silicon layers can be done with standard CMOS processing tools. The silicon dioxide layer serves as a sacrificial layer. Second, identical substrates are used for the <u>Advanced Bipolar CMOS DMOS (ABCD)</u> IC-processes. This class of processes can handle high voltages (ABCD2 up to 120V). The high voltage capability is suitable for the transduction of the mechanical resonator. Both MEMS and IC are processed on a similar substrate, since the strategic aim is to integrate the MEMS structure with the IC-process in the long run.

Frequency scaling is investigated for both the capacitive and the piezoresistive MEMS resonator. MEMS resonators have been successfully tested from 13 MHz to over 400 MHz. This is achieved by decreasing the size of the resonator with a factor 32. We show that the thin SOI layer and the decreasing size of the resonator increase the effective impedance of the capacitive resonator at higher frequencies. For the piezoresistive resonator, we show that this readout principle is insensitive to geometrical scaling and layer thickness. Therefore, the piezoresistive readout is preferred at high frequencies. The effective impedance can be kept low, at the expense of higher power consumption.

Frequency accuracy can be improved by decreasing the initial frequency spread and the temperature drift of the MEMS resonator. The main source of initial frequency spread is geometrical offset, due to the non-perfect pattern transfer from mask layout to SOI. A FEM tool has been developed in Comsol Multiphysics to obtain compensated layouts. The resonance frequency of these designs is first-order compensated for geometric offset. The FEM tool is used to obtain compensated resonators of various designs. We show empirically that the compensation by design is effective on a 52 MHz square plate design. For the compensated design, frequency spread measurements over a complete wafer show that there are other systematic sources of frequency spread.

The resonance frequency of the silicon MEMS resonator drifts about –30 ppm/K. This is due to the Young's modulus of silicon that depends on temperature. We have investigated two compensation methods. The first is passive compensation by coating the silicon resonator with a silicon dioxide skin. The Young's modulus of silicon dioxide has a positive temperature drift. Measurements on globally oxidized structures show that the right oxide thickness reduces the linear temperature drift of the resonator to zero. A second method uses an oven-control principle. The temperature of the resonator is fixed, independent of the ambient temperature. A demo of this principle has been designed with a piezoresistive resonator in which the dc readout current through the resonator is used to control the temperature of the resonator. With both concepts, more than a factor 10 reduction in temperature drift is achieved.

To demonstrate the feasibility of high-frequency oscillators, a MEMS-based 56 MHz oscillator has been designed for which a piezoresistive dogbone resonator is used. The amplifier has been designed in the ABCD2 IC-process. The MEMS oscillator consumes 6.1 mW and exhibits a phase noise of -102 dBc/Hz at 1 kHz offset from the carrier and a floor of -113 dBc/Hz. This demonstrates feasibility of the piezoresistive MEMS oscillator for low-power, low-noise applications.

Summarizing, this PhD thesis work as part of the MEMSXO project at NXP demonstrates a MEMS oscillator concept based on the piezoresistive resonator in thin SOI. It shows that by compensated designs for geometric offset and oven-control to reduce temperature drift, a frequency accuracy can be achieved that can compete with the performance of crystal oscillators. In a benchmark with MEMS competitors the concept shows the lowest phase noise, making it the most suited concept for wireless applications.

SAMENVATTING

Mechanische resonatoren worden veel gebruikt voor klok functies of als frequentie referentie.Mechanische resonatoren hebben een hoge kwaliteitsfactor en hebben daarom de voorkeur over elektrische resonatoren. In de 'timing' markt met een grootte van \$4.1 miljard (2008) zijn kwarts kristallen nog steeds onmisbaar in elektrische apparatuur. Deze kristallen bieden uitstekende prestaties in tremen van stabiliteit (korte en lange termijn), vermogensgebruik en temperatuur drift.

MEMS resonatoren worden gezien als mogelijk alternatief voor de kwarts kristallen, die als nadeel hun behoorlijke afmetingen hebben en niet in IC technologie geïntegreerd kunnen worden. MEMS heeft als voordelen: grootte, kostprijs en systeem integratie. Voortgang in recente jaren laat zien dat MEMS resonatoren de prestaties van kwarts kunnen evenaren. Kritische factoren voor succes zijn daarbij een hoge kwaliteitsfactor, een lage temperatuur drift, een lage faseruis en laag vermogensgebruik. Dit proefschrift onderzoekt de haalbaarheid van het schalen van MEMS resonatoren/oscillatoren naar frequenties boven de 10 MHz. De belangrijkste mijlpaal is daarbij een 52 MHz MEMS oscillator.

Bij NXP worden de MEMS resonatoren geproduceerd op 200 mm silicium-op-isolator (SOI) wafers, met een SOI laagdikte van 1.5 μ m en een begraven oxide dikte van 1 μ m. De strategische keuze voor dun SOI is gemaakt om twee redenen. Ten eerste kunnen de processen op dun SOI wafers gedaan worden met standaard CMOS productie apparatuur. Ten tweede worden bij NXP identieke wafers gebruikt voor het ABCD IC proces. In deze klasse van processen kunnen hoge voltages gebruikt worden (ABCD2 tot 120V). Dit hoge voltage is nodig voor de elektromechanische transductie van de mechanische resonatoren. De MEMS en het IC worden geproduceerd op identieke wafers, omdat het strategische lange termijn doel is om de MEMS in het IC proces te integreren.

Frequentie schaling is onderzocht voor zowel de capacitieve als de piezoresistieve resonator. MEMS resonatoren zijn succesvol getest in een frequentie bereik van 13 MHz tot boven de 400 MHz. Om de hoge frequentie te bereiken is de grootte van de resonator een factor 32 verkleint ten opzichte van het 13 MHz ontwerp. We tonen aan dat de dunne SOI laag en de steeds kleinere omvang van de resonator de effectieve impedantie van de capacitieve resonator verhoogt op hoge frequentie. Voor de piezoresistieve resonator tonen we dat deze detectie methode ongevoelig is voor laagdikte of geometrische schaling. Daarom

heeft de piezoresistieve resonator op hoge frequentie de voorkeur. De effectieve impedantie kan laag gehouden worden, ten koste van het vermogensgebruik.

Frequentie nauwkeurigheid kan verbeterd worden door de initiële frequentie spreiding en de temperatuur drift van de MEMS resonator te verminderen. De dominante bron van initiële frequentie spreiding is geometrische offset, veroorzaakt door het niet perfect transfereren van het ontwerp op het lithografiemasker naar de SOI laag. Een eindige elementen model is ontwikkeld in Comsol Multiphysics voor het ontwerp van gecompenseerde lay-outs. De resonantie frequentie van deze ontwerpen is eerste orde gecompenseerd voor geometrische offset. We tonen aan de compensatie in het ontwerp effectief is voor een 52 MHz vlakke plaat ontwerp. Voor een gecompenseerd ontwerp, frequentie spreiding metingen over een complete wafer laten zien dat er ook andere systematische oorzaken van frequentie spreiding zijn.

De resonantie frequentie van een silicium MEMS resonator drift met ongeveer -30 ppm/K. wordt veroorzaakt door de temperatuursafhankelijkheid Dit van de elasticiteitsmodulus van silicium. We hebben twee compensatie methodes onderzocht. De eerste methode is een passieve compensatie waarbij de siliciumstructuur gecoat wordt met een huid van silicium dioxide. De elasticiteitsmodulus van silicium dioxide heeft een positieve temperatuur drift. Metingen op globaal geoxideerde structuren laten zien dat met de juiste oxidedikte de lineaire temperatuurdrift tot nul gereduceerd kan worden. De tweede methode maakt gebruik van het ovencontrole principe. De temperatuur van de resonator wordt constant gehouden, onafhankelijk van de omgevingstemperatuur. Een demo van dit principe is ontwikkeld met de piezoresistieve resonator. De gelijkstroom door de resonator, nodig voor de piezoresistieve detectie, wordt gebruikt om de temperatuur van de resonator controleren. Met beide concepten is meer dan een factor 10 reductie in temperatuur drift gerealiseerd.

Om de haalbaarheid van hoog frequente oscillatoren te demonstreren is er een 56 MHz MEMS oscillator ontworpen met een piezoresistief dogbone ontwerp als resonator. De versterker is ontworpen in het ABCD2 IC proces. De oscillator verbruikt 6.1 mW aan vermogen en heeft een faseruis van –102 dBc/Hz op 1 kHz afstand van de draagfrequentie en een faseruis vloer van –113 dBc/Hz. Hiermee wordt de haalbaarheid gedemonstreerd van de piezoresistieve MEMS oscillator voor laag vermogen, lage faseruis applicaties.

Samenvattend, dit proefschrift als onderdeel van het MEMSXO project binnen NXP demonstreert een MEMS oscillator concept gebaseerd op een piezoresistieve resonator in dun SOI. We hebben aangetoond dat met ontwerpen gecompenseerd voor geometrische offset en ovencontrole om temperatuur drift te reduceren, een frequentie nauwkeurigheid behaald kan worden waarmee het concept kan concurreren met kristal oscillatoren. In een vergelijking met MEMS oscillator concurrenten behaalt dit concept de laagste faseruis. Het is daarom het meest geschikte concept voor draadloze communicatie.

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