InP-based membrane photodetectors on Si photonic circuitry

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InP-based Membrane Photodetectors on Si Photonic Circuitry

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PROEFSCHRIFT

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Contents

Chapter 1

Introduction

This chapter introduces the research carried out to develop the indium phosphide (InP) based photodetectors suitable for optical interconnections on silicon (Si) electronic integrated circuits presented in this thesis. The limitations expected with the use of electrical interconnections in future electronic chips are presented and provide the motivation for this work. Several options that are being investigated to face this problem are discussed and compared. Finally, the approach used in the project framework within which the InP-based detectors were developed is described.

1.1   Introduction

In the last two decades optical fibers replaced conventional electrical wires in long-haul communications and are now a core part of the internet. That is mainly because of the high propagation losses that electrical lines suffer at high frequencies, as compared to the excellent performance of optical fibers in the telecom wavelength windows [1]. A migration from electrical to optical interconnections is underway for short-distance communications as well (in the mm range), namely between server backplanes and multirack machines [2]. Recent research studies discuss and demonstrate the advantage of using optics even for on-chip very short interconnections, in the sub-mm range [3]. Nowadays, electronic Integrated Circuits (ICs) make use of electrical wires to distribute the clock and other signals to different functional blocks of the IC and to provide power and ground connections. The electrical wiring system is currently used for both the intra-chip and chip-to-chip interconnections. Nevertheless, future generation Si ICs are expected to suffer a severe bottleneck in the interconnect level, going toward linewidth dimensions and higher bandwidth requirements [4]. In particular, with the technology scaling down and the signal switching frequency increasing, three main issues are predicted to slow down the steady increase in performance for complementary metal-oxide semiconductor (CMOS) ICs: signal propagation delay, power consumption and integration density. To see how the electrical interconnect wiring influences these characteristics, let us analyze what the

wire characteristics are and where the problems occur. Electrical interconnect (EI) wires are normally modeled as *RLC* transmission lines. That is, lines that have:

- Resistance, which is the wire's opposition to the flow of electric current. The resistance (per unit length) depends on the wire's geometry and can be calculated by the material resistivity divided by the conductor's cross-sectional area.

- Capacitance, due to the wire's electrical potential difference relative to the ground and the proximity of adjacent wires. This is changed by adding or removing charge to the wire. The capacitance depends not only on the wire's geometry, but also on the wire's position in the circuit. As a matter of fact, considering the small feature sizes of current electronic ICs, the pitch between the wires is such that side-to-side capacitances are as important as the capacitance relative to the ground.

- Inductance. This wire characteristic is more difficult to identify, both qualitatively and quantitatively. When sending an electrical signal through a wire, a magnetic field is generated by the current flow. When the circuit switches between on and off state, the magnetic flux changes and this induces an electrical field that produces a return current flow. The induced electrical field is proportional to the current variation in time and the constant of proportionality is the inductance. In a complex circuit, the return currents flow in the adjacent wires with the least impedance, but these paths are not fixed, as they depend on the signal frequency. This problem translates into ambiguity in predicting the electromagnetic noise in the IC. The return path uncertainty is tackled by fixing a common reference for the grounding paths, which makes the circuit design more complicated.

With the reduction in feature size, which follows the exponential Moore's law [5], the geometry of the interconnect wires should also scale, and this raises a number of issues. The wire's resistance per unit length quickly increases as the wire's cross-section shrinks, and in most cases this is not compensated by the scaling down of the wire length. This leads to a strong limitation for the bandwidth of the data stream that can be routed through the wire: as the maximum data capacity in an interconnection line is proportional to A/l^2, where l is the length of the interconnect line and A the area of its cross-section, the data flow becomes more and more limited by the interconnection scaling problem [6].

Capacitance and inductance are less sensitive to the scaling problem, though [7]. It is unavoidable, however, that the *RC*-time characteristic of interconnect wires becomes a fundamental limitation for the bandwidth that can be used for the data transport across those wires. The reason the time characteristic is important is that it influences the total circuit delay: when a signal is launched through an interconnect wire, a certain time is needed for the residual currents from that transmission to die away before a second signal can be launched, or otherwise inter-symbol interference (ISI) will occur at the receiver side. As a result, the data transported by the buses that interconnect different parts of a digital computer has to flow at a much lower frequency than the clock frequency. This problem affects in particular the off-chip interconnections, but it is predicted to occur for the shorter on-chip interconnections too in the next few years [6]. Furthermore, capacitance and inductance are responsible for the dynamic

power consumed by the electrical interconnects, which is the power consumed in the CMOS transistors when switching between on-state and off-state. This issue becomes worse with the signal switching frequency scaling up, and therefore it becomes an increasing limitation for the maximum data rate that can be used through the EIs.

Moreover, the circuit complexity and the integration density increase with the technology scaling, which implies that more wires have to be used to interconnect a larger number of devices. This requires a higher wiring density, which can be achieved with device miniaturization, but paying a price in terms of IC performance: miniaturized wires have a higher resistance and therefore dissipate more electrical power. The reduction in wire pitch increases the wire side-to-side capacitance and the electromagnetic (EM) crosstalk.

These issues are currently addressed in a number of ways. Repeaters are used to lower the wire delay and thus increase the bandwidth: this is analyzed in [7], where a comparison between an EI made with an uninterrupted wire and with a wire segmented into several stages each containing a repeating element is made. It is shown that the delay of the uninterrupted wire grows quadratically with the wire length, while by inserting repeaters periodically along the interconnect line, the total wire delay becomes equal to the number of repeated segments multiplied by the single stage delay, and therefore the total delay grows linearly with the interconnect length. Repeaters also make the interconnect wires more robust towards the device size scaling, as the *RC*-time characteristic of repeated wires stays constant. However, the drawback is that repeaters are relatively large and power-hungry components [7, 8].

For these reasons, a radical change in the architecture of the electronic chips started to take place in the recent years to address the problem at the interconnection level. In the next sections, the options that are being employed and investigated are discussed and the topic is then focused on our approach and the devices developed in that context.

1.2   Electrical interconnects: options and state-of-the-art

The interconnection scaling problem described in Section 1.1 can be tackled in a number of ways, at different level of design of a chip, namely at logic gate design level, at hardware design level, at network-on-chip topology and architecture design level. Some examples are:

- Change the network architecture by using multicore processors, thus taking advantage of the parallel communication between processor cores and of the shorter wires to interconnect several functional cores [7, 9–11]. Recently, an 8-core processor realized in 90 nm CMOS technology[1] working at frequencies over 4 GHz was deployed for commercial application [12], and an 80-core processor realized in 65 nm CMOS technology working at frequencies over 5 GHz was demonstrated [13].

- Change the chip architecture by stacking several layers. This leads to a 3D integration scheme, which increases the architecture complexity but keeps the interconnect wires short and therefore keeps low their resistance and their bandwidth limitation [14].

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[1]Half-pitch between two integrated lines

- Change the IC network topology. Analytical models to optimize area and energy efficiency thanks to optimum layout of interconnect wires were studied [15].

- Minimize and miniaturize the interconnections and equalize the transmission channels [16].

- Optimize the hardware design by focusing on critical aspects. In [17], it was demonstrated that more than 50% of the overall dynamic power of CMOS multicore processors is consumed by the interconnect wiring, and that remains an issue for the most recent multiprocessor electronic chips [18, 19]. An interconnect-power saving design driver is therefore necessary for the next generation of CMOS circuits.

- Optimize the design at the logic gate level. Time optimization in logic paths with significant wire delays for the Very Large Scale Integration (VLSI) circuit design translates into significant improvement on the IC performance. In [20], design considerations for minimizing the delay in logic gates interconnected by electrical wires are presented. More specifically, the optimal size, number and location of the gates and of the repeater blocks in the presence of interconnects are studied.

The bottom line is that, even in state-of-the-art multiprocessor computers, the interconnect wires are the main limiting factor for power consumption and communication speed, rather than computation itself [21]. A limit is predicted on a short term, when machines employing terabit per second (Tbit/s) fast communications will be used (e.g. servers and supercomputers) [2].

1.3   Optical interconnects on Si ICs

A promising solution is given by radically changing the means of interconnection into a photonic interconnection layer, suitable for data transport in the optical domain [22, 23]. Clearly, due to the small feature size, the implementation of intra-chip and chip-to-chip interconnections in the optical domain can not rely on optical fibers, but requires the use of photonic integrated circuit (PIC) technology. Changing the means of interconnection into a photonic interconnection layer would provide a number of advantages with respect to the all-electrical solutions, namely:

- Low power consumption, as there would be no need for low impedance terminating lines [24].

- Simpler electronic IC architecture design, thanks to the optical interconnect (OI) immunity to EM noise.

- Opportunity to configure a Wavelength Division Multiplexing (WDM) network-on-chip topology, not possible in the electrical domain. The WDM network is based on the following principle: at the transmitter side, the data from the network users is first converted from electrical to optical. The wavelengths carrying the optical signals are
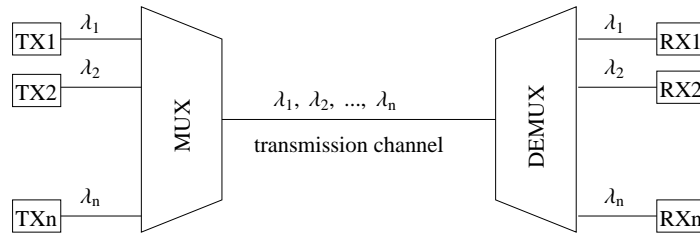
Figure 1.1: WDM network link schematics: the wavelengths $\lambda_1, \lambda_2, ..., \lambda_n$ carrying the optical signals launched by the transmitters TX1, ..., TXn are multiplexed in one channel and transmitted over the network. At the receiver side, a demultiplexer routes the different wavelengths to different channels. For each channel, the detectors RX1, ..., RXn convert the signals from the optical domain back into the electrical domain.

multiplexed in one channel and transmitted over the network. At the receiver side, a demultiplexer routes the different wavelengths to different channels. Finally, for each channel, a photodetector (PD) converts the signal from the optical domain back into the electrical domain (see Fig. 1.1).

- High-speed interconnects, thanks to the high data capacity allowed by the optical communications.

In [25], a prediction of the on-chip EIs performance is made, based on the ITRS road map, and target requirements for the alternative OI scheme are derived in terms of propagation delay, power consumption and bandwidth density, defined as data throughput through a unit cross-section of an interconnect. More specifically, the following considerations are presented in [25]:

- With the technology scaling down, the minimum achievable electrical interconnect delay is an issue. Predictions were made until the CMOS 22 nm technology node[2], at which the interconnect delay per unit length remains fixed at approximately 20 ps/mm, limited by the *RLC* impedances characteristic of the EI. The delay can be optimized by using wider wires, but that reduces the bandwidth density. OIs do not have any associated *RLC* delay and offer therefore a very promising solution to this problem. Fig. 1.2 shows a comparison of the signal propagation delay in EIs and two common OIs, based on silicon and polymer waveguides. Unlike the EI *RLC*-associated delay, the signal propagation delay in OIs is only due to the waveguide intrinsic delay, which is not affected by the CMOS technology scaling. However, the implementation of OIs requires an electrical-to-optical (EO) and an optical-to-electrical (OE) signal conversion at the transmitter and receiver side, respectively, increasing the total delay and power consumption. Because of this reason, the longer the interconnect, the more beneficial the choice of the OI over the EI.

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[2]Half-pitch between two integrated lines
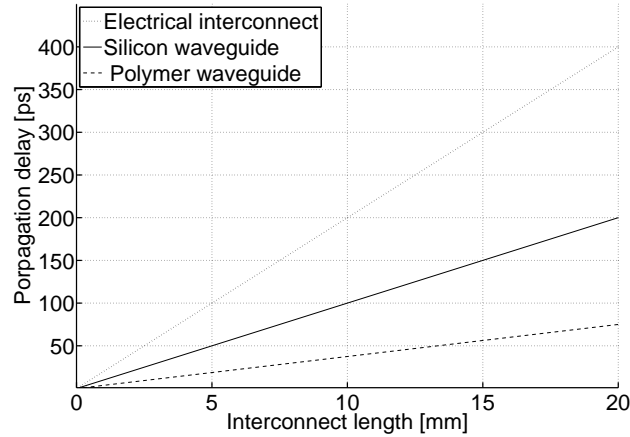
Figure 1.2: Propagation delay of silicon and polymer waveguides as compared to EIs. Both types of optical waveguides have a square cross-section and are assumed to be surrounded by a cladding with an optical refractive index of 1.1 The core of the silicon waveguide is 340 nm wide, with a refractive index of 3.4. The core of the polymer waveguide is 1.36 μm wide, with a refractive index of 1.3. *Source: Haurylau et al., JSTQE, 2006.*

- Even considering delay-optimized EIs with optimal repeater stages, the power consumption of chip-length EIs remains in the order of 1 mW/mm and is expected to increase with higher signal switching frequency, as that increases the dynamic power consumption [26]. This sets a target upper limit for the power consumption in OIs (including EO and OE conversions), in order to be competitive with EIs.

- The bandwidth density that can be reached with EIs can be significantly improved with the use of OIs in WDM on-chip networks. A minimum number of WDM channels is required to exceed the EI bandwidth density. This number of channels is a moving target because the bandwidth density of EIs increases with the technology scaling, as the wire pitch becomes smaller and a higher wire integration density allows for a more powerful parallel communication. Fig. 1.3 shows the number of OI WDM channels required to exceed the EI bandwidth density as a function of the CMOS technology node. For Si photonic OIs, a minimum number of 3 WDM channels is predicted to be necessary to benefit from the OI solution.

Recent studies demonstrate that the delay, power-consumption and density requirements for OIs mentioned above are indeed achievable: in [27], a simulation-based systematic synthesis method for integrated OIs is described. This method was used to extract the performance of mm-long on-chip OIs in terms of interconnect delay, power consumption and integration density in three CMOS technologies, at 65, 45 and 32 nm. In CMOS circuitry, electrical in-
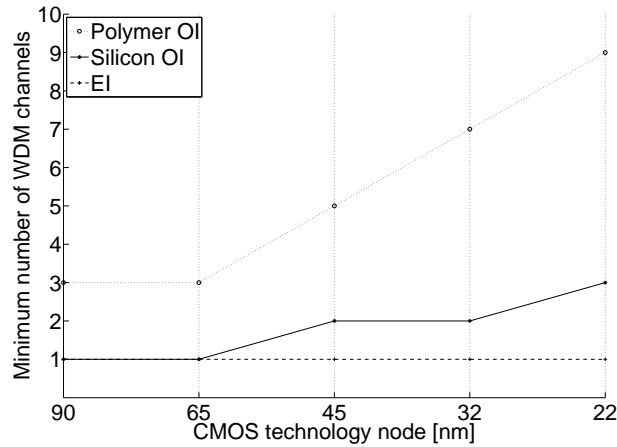
Figure 1.3: Number of OI WDM channels required to exceed the EI bandwidth density as a function of the CMOS technology node. *Source: Haurylau et al., JSTQE, 2006.*

terconnections take a substantial space (CMOS area), at the expense of the device integration density. Therefore, when the interconnections are realized in an optical layer integrated with the CMOS circuitry, the electronic IC density increases. The simulation results in terms of CMOS gate area as a function of the interconnect length are shown in Fig. 1.4. The simulations are made for on-chip OIs, therefore for mm-long interconnects, according to the ITRS projected chip edge length OI of 17.6 mm [4, 25]. As it can be seen in Fig. 1.4, the implementation of OIs in the 65, 45 and 32 nm CMOS circuitry approximately verifies the scaling law for electronic ICs: $A_{32\,nm} = A_{45\,nm} \cdot s = A_{65\,nm} \cdot s^2$, where $s = 0.7$ is the scaling factor between technology nodes. Fig. 1.5 shows the simulation results for the circuit delay when OIs are employed as a function of the interconnect length for the 3 technologies mentioned above. The total circuit delay, which is due to the intrinsic waveguide delay in the OI link and to the delay in the CMOS ICs, decreases with longer interconnects with respect to the intrinsic waveguide delay. This is due to the higher modulation current required in longer OIs to compensate for the higher overall waveguide loss. The higher modulation current drives the source capacitance faster, consuming on the other hand more power. The power analysis results are shown in Fig. 1.6, where the total power is plotted versus the OI length in the three cases of 65, 45 and 32 nm CMOS technology. The total power is the sum of the average static power, which takes into account the power consumed by transmitter, receiver and circuit, and of the dynamic power, which is the power consumed only by the CMOS circuit switching. This analysis shows that the total circuit delay and area and power consumption when on-chip interconnections are implemented in an integrated photonic layer fulfill the requirements set for the future CMOS technology nodes [27].
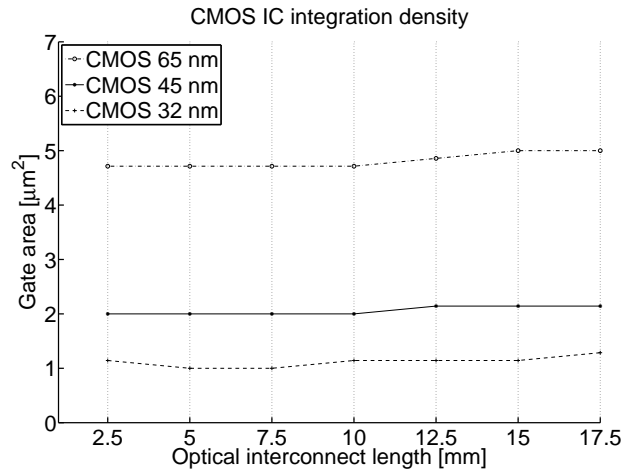
Figure 1.4: Total CMOS gate area (μm^2) for varying OI length and technologies. The implementation of OIs in the 65, 45 and 32 nm CMOS circuitry approximately verifies the scaling law for electronic ICs: $A_{32\,nm} = A_{45\,nm} \cdot s = A_{65\,nm} \cdot s^2$, where $s = 0.7$ is the scaling factor between technology nodes. *Source: O'Connor et al., Transac. on VLSI Systems, 2006.*

1.3.1   Options, challenges and state-of-the-art

The idea of adding a photonic layer on top of the electronic silicon ICs to realize optical interconnections has been investigated by several academic and industrial research groups in the last few years, following the road maps developed for semiconductors [4]. There are several ways to do that, which require different devices and integration schemes, depending on the specific application that needs to be addressed. For example, optical transmitters and receivers in the interconnect layer on top of electronic boards capable of vertically emitting and receiving optical signals are particularly suitable for rack-to-rack interconnections in multirack computer machines and can be used for chip-to-chip on-board interconnections as well. These solutions have been investigated by [28, 29], where Vertical-Cavity Surface-Emitting Laser (VCSEL) sources and substrate illuminated photodetectors fabricated on an interconnect layer on top of an electronic board are employed. A different approach is based on a planar integration scheme, where edge-emitting laser sources and photoreceivers are used. This option is suitable for on-board on-chip and off-chip interconnects and leaves the possibility of integrating more optical devices in the laser-to-detector link path, like modulators, amplifiers, filters, etc. In any case, the main challenges are the integration of the electronic and the photonic components as well as the development of a fabrication process compatible with today's Si IC fabs processing. These two points are essential to consider the optical interconnections in integrated circuits as a real potential alternative to electronics, as they would permit the processing of PIC on a Si wafer scale without requiring substantial changes in current Si IC fabs. The reason why
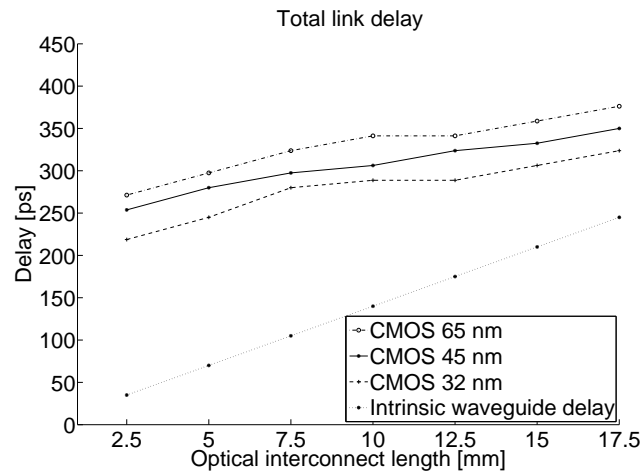
Figure 1.5: Total circuit delay (ps) as a function of OI length for different technologies. The intrinsic delay of a SiO$_2$ waveguide is plotted as a reference. The total circuit delay decreases with longer interconnects with respect to the intrinsic waveguide delay because of the higher modulation current required in longer OIs to compensate for the higher overall waveguide loss. The higher modulation current drives the source capacitance faster, thus decreasing the delay in the electronic gates. *Source: O'Connor et al., Transac. on VLSI Systems, 2006.*

the integration of electronic and photonic devices is so challenging is basically due to the fact that electronic ICs and PICs utilize different materials: while electronic ICs are based on Si, which is a semiconductor with an indirect energy band gap, optical devices are based on compound semiconductors, like InP or GaAs, which have a direct energy band gap. In direct band gap semiconductors, the electron-hole recombination process between conduction and valence energy bands occurs with a much higher probability. As this recombination is the physical mechanism behind light emission, amplification and detection, indirect energy band gap materials such as Si have an intrinsic substantial limitation in terms of type of functionalities they can provide when working at optical frequencies. In the last years, silicon-on-insulator (SOI) photonic technology has made substantial steps forward and the main passive components have been demonstrated, namely waveguides, splitters, interferometers, wavelength filters, gratings [30]. Recently, active components such as photodetectors and modulators in Si and SiGe have been demonstrated too [31–33], but a Si-based light source remains a missing building block in the current Si-photonics scenario. Materials based on direct bandgap semiconductor compounds, like InP, have excellent optical properties for active photonic operations, namely light emission, modulation and photodetection [34–37]. Therefore, the use of such compounds could compensate for the limitations of the SOI technology. However, that raises a different issue: how to integrate devices made out of different materials on the same wafer. Essentially, the problem is that the lattice constant and the thermal expansion coefficient of these
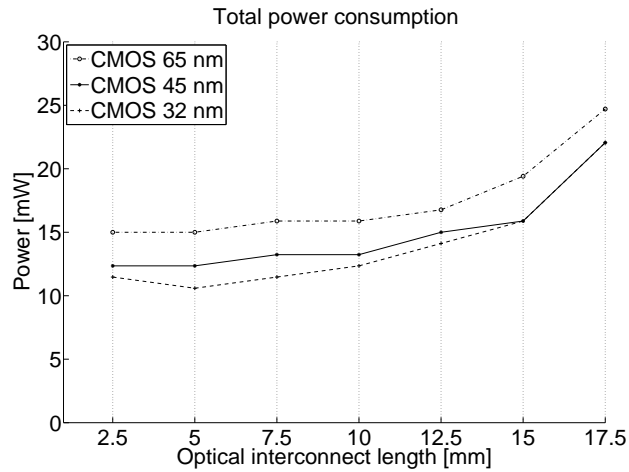
Figure 1.6: Total power (mW) as a function of OI length for different technologies. The total power is the sum of the average static power, which takes into account the power consumed by transmitter, receiver and circuit, and of the dynamic power, which is the power consumed only by the CMOS circuit switching. When OIs are employed, the requirements set for the future CMOS technology nodes in terms of power consumption are fulfilled. *Source: O'Connor et al., Transac. on VLSI Systems, 2006.*

materials are different and that makes it very difficult, and in most cases even impossible, to epitaxially grow optical material layers on a Si substrate. Even when that is possible, the quality of the epitaxially grown layers is poor, due to the high dislocation density caused by the lattice mismatch that affects the material optical properties [38]. Besides these issues related to the epitaxial growth, when III-V compounds such as InP or GaAs are grown on group-IV substrates such as Si a further problem occurs, which has to do with the electronic properties of the materials. The different electron configuration of III-V and group-IV materials leads to a high contact resistance between the epitaxially grown layers, and that compromises the performance of the active photonic devices processed on such layer stack. Moreover, whatever way is used to integrate photonic-based and electronic-based components, an optical device process flow compatible with the fabrication steps of Si electronic circuits has to be developed. Many solutions have been investigated to face these problems: InP nano-wires were successfully grown on a Ge substrate, as demonstrated in [39], and SiGe-based photodetectors and modulators realized by using Ge epitaxial growth lattice-mismatched to Si were recently reported [40–42]. However, the indirect energy band gap of the SiGe compound makes it not suitable for the realization of light emitters and amplifiers. This is, as a matter of fact, the strong argument for introducing direct energy band gap compounds, such as InP. This compound provides excellent light emission, amplification, modulation and detection properties, and therefore has a huge potential as candidate for adding to Si the missing functionalities necessary to the implementation of optical interconnections on Si electronic chips. Due to the

issues mentioned above, related to the growth of III-V compounds on Si, a bonding technology is more suitable for the InP-on-Si heterogeneous integration: the Si and the InP wafers are prepared separately and then bonded together. The bonding approach has the advantage of providing high-index membrane-based devices on a low-index substrate, which is necessary for photonic ultra-compact integrated circuits. Heterogeneous components on a Si/InP platform that make use of the bonding technology were reported by Seassal et al. and Monat et al. [43–45]. Si-based and InP-based devices that exploit the advantages of this technology were more recently reported [46–48]. While several bonding technologies were investigated by [49] to integrate InP-based and Si-based devices, the following main three ones are used:

- Metallic bonding. This technique uses metals for wafer bonding, being the bonding interface Cu-Cu or metal alloys [50, 51]. This has the intrinsic limitation of providing an absorbing bonding layer, which becomes a problem when the optical signal has to be transparently routed between the Si and the bonded InP layer, as a large part of the optical power would be absorbed, and therefore lost, in the metal area used for bonding. On the other hand, this bonding technology is particularly suitable for the hybrid integration of Si and InP chips for which only electrical interconnections are required between the optical and the electronic layers, while the signal processing is done in either one or the other layer. Thanks to that, the bonding alignment does not require a high accuracy (in the order of 10 μm) [52].

- Direct molecular bonding. With this technique, a layer of silicon dioxide (SiO_2) is first deposited on the Si and InP wafers. The two wafer silica surfaces are then flattened by Chemical Mechanical Polishing (CMP) and then fused together. This technique provides an optically transparent bonding layer and is therefore suitable for the heterogeneous integration of Si and InP chips but requires advanced CMP processing to control the bonding layer thickness and roughness [45, 53].

- Benzo-Cyclo-Butene (BCB) bonding. This technique uses an optically transparent polymer layer, which is spin coated onto the substrates and used as a bonding agent. The application of this approach is the same as for the direct molecular wafer bonding approach, but it has the advantage that no CMP processing is required and the tolerance towards the wafer surface roughness is relaxed. However, the bonding layer thickness is difficult to control, as well as the thickness uniformity across the wafer [54].

In the next section, the approach used for the realization of the heterogeneous components presented in this thesis is described.

1.3.2 Our approach

This thesis describes the realization of InP-based photodetectors suitable for use in optical interconnects on Si and of heterogeneously integrated multiwavelength receivers (MWRs) in InP-on-Si technology. This work has been carried out through the European project PICMOS[3]

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[3]Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), http://picmos.intec.ugent.be

and the Smartmix-MEMPHIS[4] project, funded by Dutch Ministry of Economic Affairs. The detectors developed within the PICMOS project framework are realized by using direct molecular bonding. In the project context, two different InP-based dies containing detector and laser layer stacks are bonded on a Si wafer via direct molecular bonding and then processed. The Si wafer contains an SOI waveguide layer, in which optical waveguides are defined to interconnect the active InP-based devices. This led to the demonstration of the world's first optical link integrated on Si utilizing electrically pumped InP-based microdisk lasers, SOI waveguides and InP-based detectors [55–57]. The MWRs developed within the Smartmix-MEMPHIS project framework are built of InP-based detectors BCB-bonded on an SOI wafer in which a Si waveguide layer hosts the receiver passive components, namely waveguide and demultiplexer structures. These receivers are capable to demultiplex and detect a WDM signal carrying data coded in 10 parallel wavelength channels.

In the next section, a brief overview of this thesis is given.

1.4   Thesis overview

This thesis is divided in the following 6 chapters:

- Chapter 1 introduces the work on InP-based detectors presented in this thesis. The bandwidth limitation predicted in the near future for the electrical on-chip and off-chip interconnections in Si electronic ICs is described and provides the motivation for this work. The several options that are being investigated to overcome the interconnection problem are discussed and compared. Finally, the approach used in the project frameworks within which the InP-based detectors described in this thesis were developed is presented.

- Chapter 2 discusses the integrated components designed for the realization of the InP based photodetectors developed in this thesis work. The interconnect waveguides defined on the wafer on top of which the detectors are bonded are presented. The detector structure design is described by focusing first on the design of a detector input InP membrane waveguide, used to couple the light of out the interconnect waveguide layer and bring it towards the PD absorption area, and then on the design of the p-i-n diode heterojunction.

- Chapter 3 addresses the technology developed and used for manufacturing the integrated devices presented in this thesis. The type of integration scheme used to heterogeneously integrate the Si-based and the InP-based components on a single chip is first described. The details of the processing of the SOI circuitry and of the bonding technologies used for the integration of the InP active devices are discussed step by step.

- Chapter 4 focuses on the detector developed in InP-on-Si technology. The PD structure is made of a light absorbing layer stacked on top of an InP layer that is also used for the

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[4]Merging Electronics and Micro & Nano-Photonics in Integrated Systems (MEMPHIS), http://www.smartmix-memphis.nl/

realization of a coupler structure. This coupler is meant to optimize the optical power transfer from the interconnect waveguiding layer to the detector absorption layer, thus improving the device efficiency. In the chapter, the design, fabrication and characterization of a the InP developed coupler structures bonded on a Si wafer are described. After that, detectors bonded on an SOI wafer and on a Si wafer containing CMOS circuitry are described, as well as the integration of lasers and detectors on the same chip for the realization of a point-to-point photonic link on Si.

- Chapter 5 is about the multiwavelength receivers heterogeneously integrated in InP-on-Si technology. First, the MWR device concept is explained. Then, the attention is focused on the single components the MWR is made of: SOI waveguides, demultiplexer and InP-based detectors. The design of each component and the process flow developed for their heterogeneous integration are discussed. Finally, experimental results are presented and an outlook for the future work is given.

- Chapter 6 summarizes the PhD work carried out to develop the detectors realized in InP-on-Si technology described in this thesis. Conclusions are drawn by analyzing the main goals achieved in this research work and the main challenges that are left to be taken up.

Chapter 2

Design of integrated components

This chapter introduces the integrated components designed for the realization of the indium phosphide (InP) based photodetectors (PDs) developed in this thesis work. First, the interconnect waveguides defined on the Si wafer on top of which the detectors are bonded are presented. Then, the detector structure design is described. This description is divided into two parts: the design of the p-i-n diode heterojunction and the design of a detector input InP membrane waveguide, used to couple the light of out the interconnect waveguide layer and bring it towards the PD absorption area.

2.1 Introduction

In the previous chapter, the benefits of optical interconnections on Si for the next generation of electronic integrated circuits (ICs) was discussed, as well as the state-of-the-art options to realize heterogeneously integrated opto-electronic chips. Thanks to its excellent properties at optical frequencies, InP is a very promising compound for the fabrication of active photonic devices on a Si optical interconnection layer, and in this thesis an InP-based photodetector (PD) structure suitable for such purpose is presented. As mentioned in Section 1.3.2, this work has been carried out through the European project PICMOS[1] and the Dutch national Smartmix-MEMPHIS[2] project. The detectors developed in this context are based on an InP layer stack grown on an InP wafer. After growth, this wafer is bonded on a Si wafer via direct molecular bonding or Benzo-Cyclo-Butene (BCB) bonding and then the PDs are processed. The Si wafer is either a silicon-on-insulator (SOI) wafer that contains a Si interconnect waveguide layer on a SiO_2 insulator layer, or a complementary metal-oxide semiconductor (CMOS) wafer on top of which waveguides are patterned in a Si_3N_4 interconnect layer deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD).

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[1]Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), http://picmos.intec.ugent.be

[2]Merging Electronics and Micro & Nano-Photonics in Integrated Systems (MEMPHIS), http://www.smartmix-memphis.nl/

Before going into the details of the heterogeneous chip fabrication, which is the focus of the next chapter, the device concept and design are addressed in this chapter.

2.2   Interconnect waveguides

The interconnect waveguides are realized in Si or Si_3N_4 on top of a SiO_2 insulator layer on a Si or CMOS substrate, respectively, and are meant to interconnect the active photonic devices processed on top of the bonding layer. The choice of these interconnect waveguide materials leads to different integration schemes, with pros and cons:

- Si waveguides are defined on an SOI substrate, where the insulator layer is SiO_2. A further bonding step is then required to integrate the SOI structures with the electronic circuitry in the CMOS wafer. Thanks to the high optical refractive index of Si at optical wavelengths (3.48 at 1550 nm [58]), SOI waveguides have a very high optical field confinement, which allows for extremely compact photonic circuitry. For example, bent waveguides with radii of a few microns can be realized without any additional loss with respect to the straight sections [47].

- Si_3N_4 can be deposited by PECVD on top of an SiO_2 buffer layer flattened by Chemical-Mechanical Polishing (CMP) on a processed CMOS wafer. The Si_3N_4 waveguides can then be processed on wafer scale by means of standard CMOS-compatible lithography and etching processing steps. SiN_x has a much lower optical refractive index than Si: 1.8-2.1 at 1550 nm [58], depending on the PECVD deposition process and SiN_x composition. The Si_3N_4 waveguides used for this thesis work have an optical refractive index of 1.865 at 1550 nm. Si_3N_4 waveguides do not allow for the same high wire integration density that can be achieved with Si waveguides, but they do offer an easier integration with the CMOS ICs.

Alternatively, hydrogenated amorphous silicon (a-Si:H) waveguides can be used. This type of waveguides can also be deposited by PECVD on a Si substrate, thus providing a straightforward integration with the CMOS ICs, as compared to the SOI wires. Disadvantages are a lower light confinement in the waveguide core than for the SOI wires, which translates in a lower wire integration density, and higher propagation loss than the Si_3N_4 wires outside the 1550 nm telecom window [59, 60]. However, a-Si:H waveguides were not used in the context of this thesis and therefore we focus on the Si and Si_3N_4 waveguides used for our on-chip optical interconnects.

A schematic cross-section of the waveguide geometry is shown in Fig. 2.1. The Si and Si_3N_4 waveguides have dimensions of $220 \times 500\,nm^2$ and $400 \times 800\,nm^2$, respectively. The SiO_2 substrate, which is 1-2 μm thick, has a refractive index of 1.45. The top cladding is provided by the bonding layer, for which either SiO_2 or BCB are used. The refractive index of BCB is ~1.54 at 1550 nm and due to the high index contrast with the waveguide core (especially for the Si waveguides), the bonding layer material makes a negligible difference for the optical properties of the interconnect waveguides [61]. Simulations were performed with the Finite Difference (FD) and the Film Mode Matching (FMM) calculation methods implemented
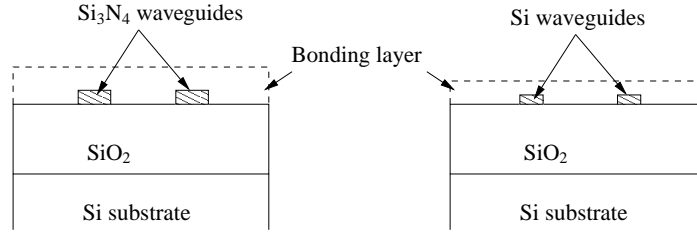
Figure 2.1: Cross-section of the interconnect waveguides defined on top of a SiO_2 insulator layer on a Si wafer. The waveguides are realized in Si (right) or Si_3N_4 (left) with dimensions of $220 \times 500\,nm^2$ and $400 \times 800\,nm^2$, respectively. The bonding layer (dashed line), on top of which the InP detector is processed, is also indicated.

in two different full vectorial mode solvers: OlympIOs, by C2V, and FIMMWAVE, by Photon Design, respectively. With this cross-section geometry, simulation results show that the fundamental mode index is about 2.5 and 1.5 for the Si and Si_3N_4 waveguides, respectively. These optical properties have to be taken into account when designing the heterogeneous photonic devices defined on top of the bonding layer. In the next section, the design of the InP-based photodetector is presented.

2.3 Photodetector structure

The detector structure consists of two parts: an InP membrane input waveguide on top of the bonding layer, meant to provide a good optical coupling from the photonic interconnect waveguide layer underneath up to the PD, and a p-i-n junction, where the optical signal is absorbed and converted into electrical power. Fig. 2.2 shows a drawing of the PD structure bonded on a Si waveguide. The design of these two detector building blocks is described below.

2.3.1 Coupler design

Two different InP coupler structures were investigated, for coupling the optical power out of the Si and the Si_3N_4 interconnect waveguides, respectively.

Before describing the coupler modeling, let us define the symbols and notation that will be used. In general, for an electromagnetic (EM) field propagation in an isotropic medium (in which permittivity and permeability are direction-independent) we can write:

$$\bar{E}(x,y,z,t) = \left[\bar{E}_0(x,y,z) \cdot e^{-j \cdot \left(\beta_x x + \beta_y y + \beta_z z + \phi_1 \right)} + \bar{E}_0^*(x,y,z) \cdot e^{+j \cdot \left(\beta_x x + \beta_y y + \beta_z z + \phi_2 \right)} \right] \cdot e^{j \cdot 2\pi f t}$$

(2.1)

where β_x, β_y, β_z are the field complex propagation constants along the coordinate axis, ϕ_1 and
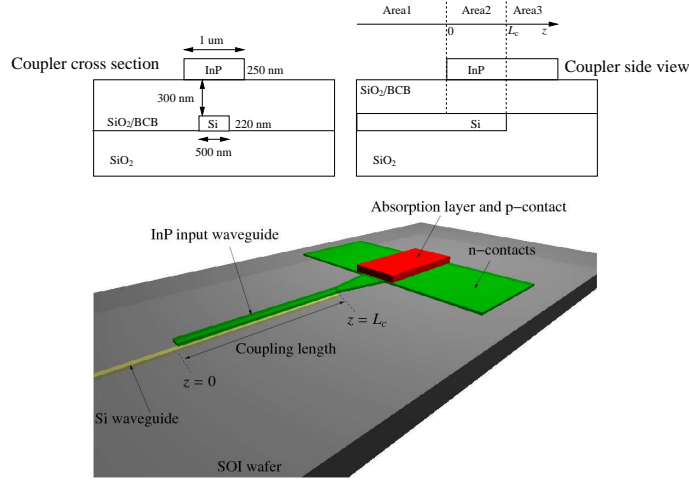
Figure 2.2: Photodetector structure. The coupling from the photonic wiring (Si waveguide) layer to the PD takes place by means of an InP membrane input waveguide. The detector is stacked on top of the membrane waveguide layer and the optical power is detected in the absorption layer. A cross section of the coupler is schematically shown.

ϕ_2 the initial field phase offsets, and

$$\bar{E}_0(x,y,z) = E_x \cdot \hat{x} + E_y \cdot \hat{y} + E_z \cdot \hat{z} \tag{2.2}$$

where E_x, E_y and E_z are the complex field components in the $\hat{x}$, $\hat{y}$, $\hat{z}$ directions. The two terms in Eq. 2.1 correspond to forward and backward propagating modes along the coordinate axis. For our application, we can consider only the forward propagating solutions and set $\phi_1 = 0$. For a waveguide, which is a z-invariant structure if $\hat{z}$ identifies the propagation direction, the field solutions do not change in $\hat{z}$. In this direction, only the field attenuation and phase rotation occur, due to the propagation. Therefore, the field dependence on $\hat{z}$ can be factorized and the following expression for $\bar{E}(x,y,z,t)$ can be written:

$$\bar{E}(x,y,z,t) = \bar{E}_0(x,y) \cdot e^{-j\cdot\beta_z z} \cdot e^{j\cdot 2\pi f t} \tag{2.3}$$

where $\beta_z = \beta - j\alpha$, being β the real propagation constant in the $\hat{z}$ direction and α the field attenuation coefficient. From this point, the field time dependence is omitted, for clarity, and the media are supposed to be lossless and, as a consequence, the modes real. Furthermore, we consider modes that satisfy the field power normalization condition:

$$\left\| \bar{E}(x,y,z,t) \right\|^2 = \int_{-\infty}^{+\infty} \bar{E}_0(x,y) \cdot \bar{E}_0^*(x,y) \cdot dx dy = 1 \tag{2.4}$$

and we define the overlap between two fields $\bar{E}_1$ and $\bar{E}_2$ that satisfy Eq. 2.3 and Eq. 2.4 as

$$a = \frac{\int_{-\infty}^{+\infty} \bar{E}_1 \cdot \bar{E}_2 \cdot dxdy}{\sqrt{\int_{-\infty}^{+\infty} \bar{E}_1 \cdot \bar{E}_1^* \cdot dxdy \cdot \int_{-\infty}^{+\infty} \bar{E}_2 \cdot \bar{E}_2^* \cdot dxdy}} = \int_{-\infty}^{+\infty} \bar{E}_1 \cdot \bar{E}_2 \cdot dxdy \tag{2.5}$$

The Si-to-InP coupler was studied by performing a 3D modal analysis, based on the system modes approach [62]. This is explained in the following, with reference to the annotation used in Fig. 2.2. First, the mode indices of the fundamental mode propagating in the Si and InP single-mode waveguides (Area1 and Area3) and of the even and odd system modes excited in the coupling structure (Area2) are calculated. Let us call them $\bar{E}_{\text{Si}}$, $\bar{E}_{\text{InP}}$, $\bar{E}_{\text{even}}$ and $\bar{E}_{\text{odd}}$, respectively. The fields propagating in the coupler's Si and InP waveguides are:

$$\bar{E}_{\text{Si}}(x,y,z) = \bar{E}_{0_{\text{Si}}}(x,y) \cdot e^{-j \cdot \beta_{\text{Si}} \cdot z} \tag{2.6}$$

$$\bar{E}_{\text{InP}}(x,y,z) = \bar{E}_{0_{\text{InP}}}(x,y) \cdot e^{-j \cdot \beta_{\text{InP}} \cdot z} \tag{2.7}$$

where β_{Si} and β_{InP} are the field propagation constants in the propagation direction $\hat{z}$ and $\bar{E}_{\text{Si}}$ and $\bar{E}_{\text{InP}}$ satisfy Eq. 2.4. Then, the excitation coefficients a_{even} and a_{odd} are calculated by overlapping the Si waveguide fundamental mode and the even and odd system modes. As most of the power is carried by the two supermodes $\bar{E}_{\text{even}}$ and $\bar{E}_{\text{odd}}$, $\bar{E}_{\text{Si}}$ can be expressed with the superposition of $\bar{E}_{\text{even}}$ and $\bar{E}_{\text{odd}}$:

$$\bar{E}_{\text{Si}} = a_{\text{even}} \cdot \bar{E}_{\text{even}} + a_{\text{odd}} \cdot \bar{E}_{\text{odd}} \tag{2.8}$$

As $\bar{E}_{\text{even}}$ and $\bar{E}_{\text{odd}}$ satisfy Eq. 2.4, the excitation coefficients are calculated using Eq. 2.5:

$$\begin{aligned} a_{\text{even}} &= \int_{-\infty}^{+\infty} \bar{E}_{\text{Si}} \cdot \bar{E}_{\text{even}} \cdot dxdy \\ a_{\text{odd}} &= \int_{-\infty}^{+\infty} \bar{E}_{\text{Si}} \cdot \bar{E}_{\text{odd}} \cdot dxdy \end{aligned} \tag{2.9}$$

The guided system modes propagate along the coupling region with different propagation constants β_{even} and β_{odd}. After propagating a distance z from the start of the coupler, the field can be written as:

$$\bar{E}_{\text{c}} = a_{\text{even}} \cdot \bar{E}_{0_{\text{even}}} \cdot e^{-j \cdot \beta_{\text{even}} \cdot z} + a_{\text{odd}} \cdot \bar{E}_{0_{\text{odd}}} \cdot e^{-j \cdot \beta_{\text{odd}} \cdot z} \tag{2.10}$$

Eq. 2.10 represents the field propagating through the coupler structure (with a length of L_{c}). At the interface with the p-i-n junction (interface Area2/Area3), Eq. 2.10 can be written as follows:

$$\bar{E}_{\text{c}}(z = L_{\text{c}}) = e^{-j \cdot \beta_{\text{even}} \cdot L_{\text{c}}} \cdot \left(a_{\text{even}} \cdot \bar{E}_{0_{\text{even}}} + a_{\text{odd}} \cdot \bar{E}_{0_{\text{odd}}} \cdot e^{-j \cdot \Delta\beta \cdot L_{\text{c}}} \right) \tag{2.11}$$

After a distance $z = L_{\text{c}} = \frac{\pi}{\Delta\beta}$, defined as coupling length, the maximum transfer of optical power occurs from the Si to the InP waveguide. The difference $\Delta\beta = \beta_{\text{even}} - \beta_{\text{odd}}$ is responsible for the system dynamics: by varying the waveguide geometry, system modes with different propagation constants are guided and the coupling length changes accordingly. The excitation
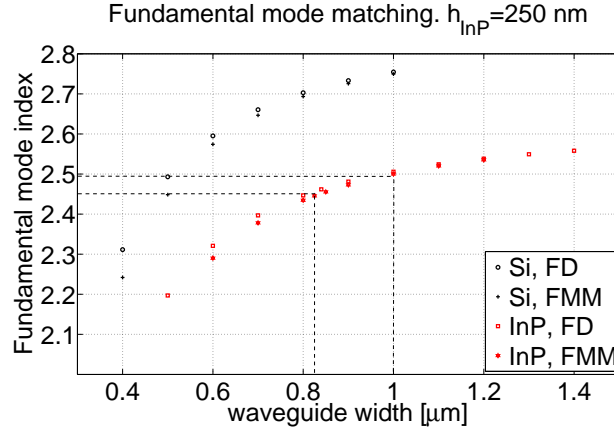
Fundamental mode matching. h_{InP}=250 nm

Figure 2.3: Si and InP waveguide fundamental mode index as a function of the waveguide width calculated with the FD and the FMM methods. For the Si waveguide, the thickness is fixed to 220 nm, while the width is varied. The 500 nm wide Si wires used for this work have a mode index of 2.45-2.5. Fixing the InP waveguide thickness to 250 nm, the predicted optimum width is 0.85 µm (1 µm), calculated with the FMM (FD) method, which is the width at which the mode index matches the index of the Si waveguide fundamental mode, as indicated by the dashed lines.

coefficient γ for the InP waveguide at the interface Area2/Area3 is then calculated by overlapping the fundamental mode guided by the InP waveguide with the field at the section $z = L_c$ (see Fig. 2.2):

$$\gamma = \int_{-\infty}^{+\infty} \bar{E}_c^*(z = L_c) \cdot \bar{E}_{InP} \cdot dxdy \tag{2.12}$$

As a last step, the power coupling efficiency

$$\eta_c = \|\gamma\|^2 \tag{2.13}$$

is calculated. The 2D mode index calculations were done with the FD and the FMM methods, while the field propagation calculations were done with FIMMPROP and through Eq. 2.6-2.13 implemented in Matlab, by MathWorks. Fig 2.3 shows the mode indices for the uncoupled waveguides calculated with the two mode solvers. By properly choosing the InP waveguide dimensions, mode matching can be achieved with the Si waveguide, which is 500 nm wide and 220 nm thick. This is shown in Fig. 2.5, where each point is the result of 2D simulations performed by changing the InP waveguide width along with different thicknesses in order to maximize each time the coupling efficiency. When choosing an InP waveguide thinner than 200 nm, the efficiency quickly drops, while choosing a larger thickness would lead to a narrower waveguide, which is more difficult to manufacture. The InP waveguide thickness was therefore fixed to 250 nm, which leads to a predicted optimum waveguide width of 0.85 µm
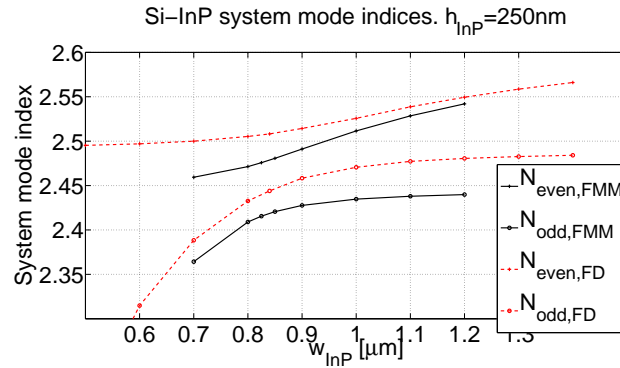
Figure 2.4: Si-InP coupler even and odd fundamental mode indices as a function of the InP waveguide width. The Si waveguide's dimensions are $220 \times 500\,\mathrm{nm}^2$, while the InP waveguide thickness is fixed to 250 nm. When w_{InP} decreases, the even system mode propagates mainly in the Si waveguide and its index approaches the one of the Si waveguide "alone" (as if no InP waveguide was present). In the same time, the odd system mode approaches cut-off. When w_{InP} increases, the even system mode propagates mainly in the InP waveguide and the optical field is less confined in the Si waveguide.
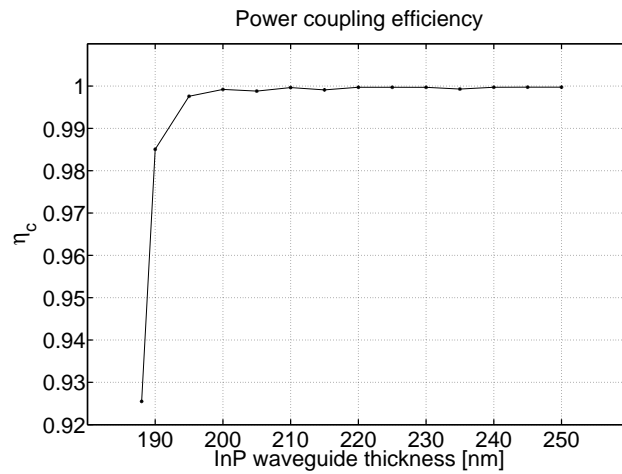

Figure 2.5: Left: Power coupling efficiency as a function of the InP waveguide thickness. In this plot, each point is the result of 2D simulations performed by changing the InP waveguide width along with different thicknesses in order to maximize each time the coupling efficiency.
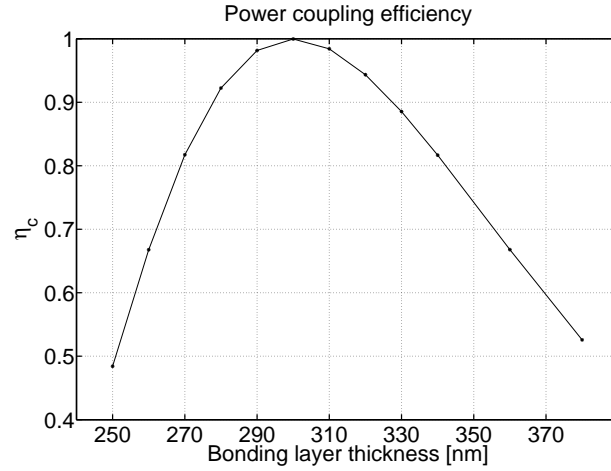
Figure 2.6: Power coupling efficiency as a function of the bonding layer thickness. A coupling efficiency of more than 80% is achieved with a tolerance of ±30 nm for the bonding layer thickness.

(1 μm), calculated with the FMM (FD) method. The coupler fundamental even and odd system modes were then calculated for an InP waveguide thickness of 250 nm. Fig. 2.4 shows the simulation results obtained with the two calculation methods: the strongest coupling occurs at the InP waveguide width at which the even and of the odd system mode indices are closer. In fact, what happens is explained as follows: when w_{InP} decreases, the even system mode propagates mainly in the Si waveguide and its index - and therefore its propagation constant - approaches the one of the Si waveguide "alone" (as if no InP waveguide was present). In the same time, the odd system mode approaches cut-off. When w_{InP} increases, the even system mode propagates mainly in the InP waveguide and the optical field is less confined in the Si waveguide, which translates in a weaker coupling between the waveguides. The optimum coupler width, at which the even and the odd system mode indices are closer, is around 0.85 μm (1 μm) when the FMM (FD) calculation method is used, as can be read from Fig. 2.4. According to the simulations, the predicted coupling length varies between 12 and 14 μm, depending on the calculation method used, and a coupling efficiency of more than 80% is achieved with a tolerance of ±30 nm for the bonding layer thickness (see Fig. 2.6) and a deviation from the optimum simulated geometry of ±10 nm and ±70 nm for the InP waveguide thickness and width, respectively. The simulation results on the power coupling efficiency tolerance towards the waveguide cross-section geometry can be seen in Fig. 2.7 and Fig. 2.8. The tolerances mentioned above for the waveguide cross-section layout are achievable with the current technology limitations. The PD structure shown in Fig. 2.2 allows for the fabrication of laterally tapered membrane waveguides without additional processing steps, which provides an increase of the waveguide alignment tolerance. The finite difference time domain (FDTD) calculation method
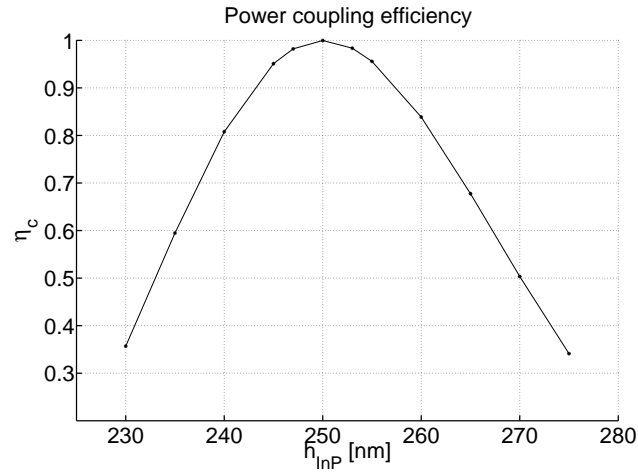
Figure 2.7: Power coupling efficiency as a function of the InP waveguide thickness. A coupling efficiency of more than 80% is achieved with a tolerance of ± 10 nm for the InP waveguide thickness.

Figure 2.8: Power coupling efficiency as a function of the InP waveguide width. The thickness of the membrane waveguide is 250 nm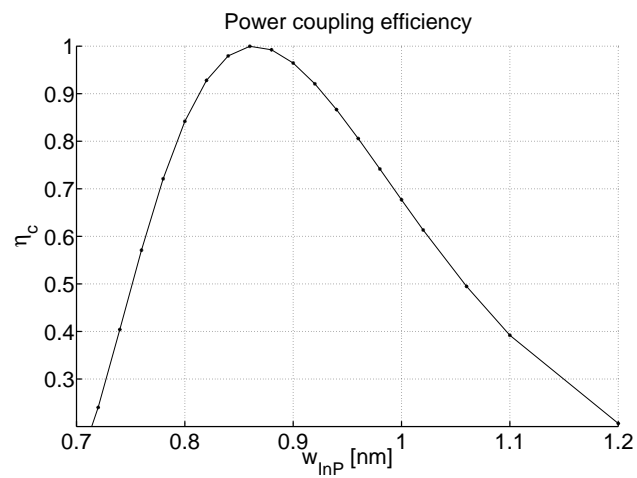. In this configuration, a coupling efficiency of more than 80% is achieved with a tolerance for the InP waveguide width of ± 70 nm.
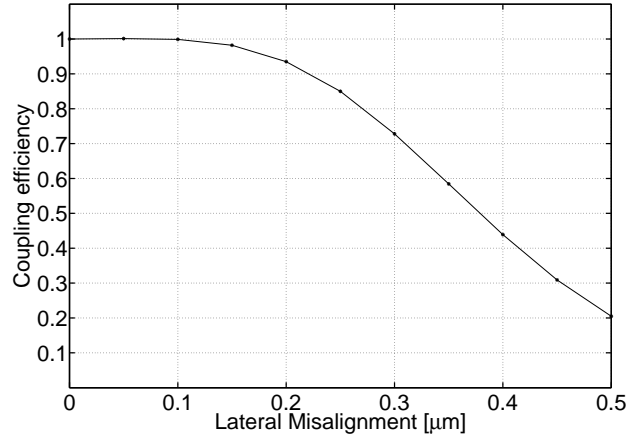
Figure 2.9: Tolerance of the Si-to-InP coupler efficiency as a function of the waveguide-to-waveguide lateral misalignment. The coupling efficiency drops to 50% for a lateral shift of ±370 nm.

implemented in Fullwave, by Rsoft, was used to investigate the Si-to-InP coupler fabrication tolerance with respect to lateral and angular waveguide-to-waveguide misalignment as shown in Fig. 2.9 and Fig. 2.10, respectively. The coupling efficiency drops to 50% (3 dB drop) for a lateral shift of ±370 nm or an angular misalignment of ±1.1°, which is within the limitations of our fabrication technology.

For the coupling between the InP and the Si_3N_4 waveguide, simulation show that the strongest coupling occurs for an InP waveguide width of 340 nm. This raises a fabrication issue: due to this small feature size, it is not possible to define that waveguide structure by means of the 405 nm Ultra-Violet (UV) optical lithography available in the clean room of the COBRA[3] research institute. This issue can be overcome by the use of electron-beam lithography (EBL), but that requires a definitely more complicated and time consuming processing [63, 64]. The reason why the optimum InP waveguide width is so small is due to the high optical refractive index contrast between the two waveguide materials. An option is to taper out the Si_3N_4 waveguide to $2\,\mu m$. This does not solve the lithography issue, as simulations show that the optimum InP waveguide width in this case is 360 nm, but it does relax the fabrication tolerances in terms of waveguide-to-waveguide angular and lateral misalignment. According to 3D BPM simulation results, fabrication tolerances at 3 dB of ±6.8° and ±800 nm for the InP waveguide angular and lateral misalignment, respectively, were calculated. Comparing these results with the simulations for the Si-to-InP coupler, it can be observed that the fabrication tolerances towards angular and lateral waveguide-to-waveguide misalignment are relaxed. However, the Si-to-InP coupling structure is definitely easier to manufacture, thanks

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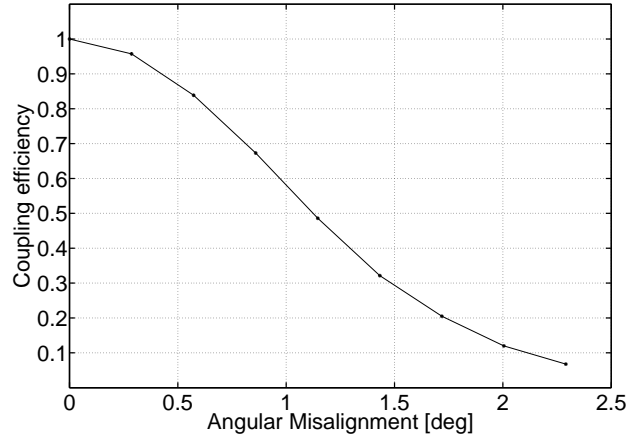[3]COBRA: COmmunication technology; Basic Research and Applications

Figure 2.10: Tolerance of the Si-to-InP coupler efficiency as a function of the waveguide-to-waveguide angular misalignment. The coupling efficiency drops to 50% for an angular misalignment of $\pm 1.1°$.

Material	Thickness	Doping/Function
p–InGaAs	50 nm	1.6E19 p–contact layer
InGaAs	700 nm	n.i.d. absorption layer
n–InP	200 nm	1E18 n–contact layer
n–InP	50 nm	n.i.d.

Figure 2.11: Layer stack used for the fabrication of the photodetectors bonded on Si waveguides, shown upside down as bonded on the Si wafer.

to the lower contrast between the InP and the Si optical refractive indices. For this reason, the InP membrane input waveguide is implemented only in the mask set for the realization of the detectors bonded on Si photonic waveguides. As explained further in the thesis, a different approach is used for the PDs bonded on CMOS wafer, with Si_3N_4 waveguides patterned on top of the electronic circuitry.

2.3.2 Photodiode heterojunction

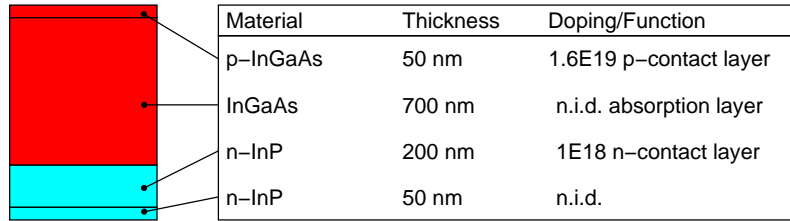The layer stack used for the fabrication of the photodetectors bonded on Si waveguides is shown upside down, as bonded on the Si wafer, in Fig. 2.11. It is built as a 700 nm n.i.d. InGaAs absorption layer sandwiched by a highly p-doped 50 nm thick InGaAs contact layer and a highly n-doped 250 nm thick InP layer, which is also used for realizing the membrane

waveguide. The photodetectors bonded on Si_3N_4 waveguides make use of a very similar layer stack, the only difference being the InP membrane waveguide layer, which is 200 nm thick. The PD mesa footprint is $5 \times 10\,\mu m^2$ and the total thickness of the device is $1\,\mu m$. The choice of this geometry was driven by the need of reaching a good trade-off between the ease of integration with the micro-disk lasers integrated in the same chip for the PICMOS project, as explained further in the thesis, and detector performance, in terms of efficiency and speed [56, 65]. Following, considerations and calculations on the detector speed and efficiency are presented.

Device speed

In a p-i-n photodetector, the speed is generally limited by:

- *RC*-time: characteristic time constant of the photodiode, associated to its electrical *RC* circuit.

- Carrier drift transit time: time needed by the photogenerated carriers to travel across the diode depletion region.

- Carrier diffusion time: time needed by the carriers generated outside the depletion region to diffuse to that region. The diffusion process is slow compared to the carrier drift in the high electrical field region. However, the diffusion time can be neglected for the PD presented in this thesis, as most of the carriers are generated in the depletion region and the doped regions are small compared to the absorption area.

Let us first consider the *RC*-time characteristic. With reference to the detector geometry shown in Fig. 2.12, an equivalent electrical *RC*-circuit can be associated to the structure, being *C* the capacitance across the p-i-n junction and *R* the resistance between the p-metal and the n-metal contacts. The capacitance at the heterojunction is

$$C_j = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{w_{dep}} = 9\,fF$$

where ε_r and w_{dep} are the permittivity and the thickness of the depletion layer and *A* is the mesa surface. The series resistance R_s is given by the sum of a number of factors: the contributions of the resistances at the metal-semiconductor interface, for the p-side and the n-side, are

$$R_{P_{metal}} = \frac{\rho_{c,p}}{A_p} \tag{2.14}$$

and

$$R_{n_{metal}} = \frac{\rho_{c,n}}{A_n} \tag{2.15}$$

where $\rho_{c,p}$ and $\rho_{c,n}$ are the specific contact resistance of the p-metal-semiconductor and n-metal-semiconductor interface, respectively, while A_p and A_n are the p-metallization and n-metallization surface, respectively. The R_s contributions across the heterojunction for the p-side and the n-side are

$$R_{P_{junction}} = \frac{d_p}{q \cdot \mu_h \cdot N_{dp} \cdot w_n \cdot L_{PD}} \tag{2.16}$$

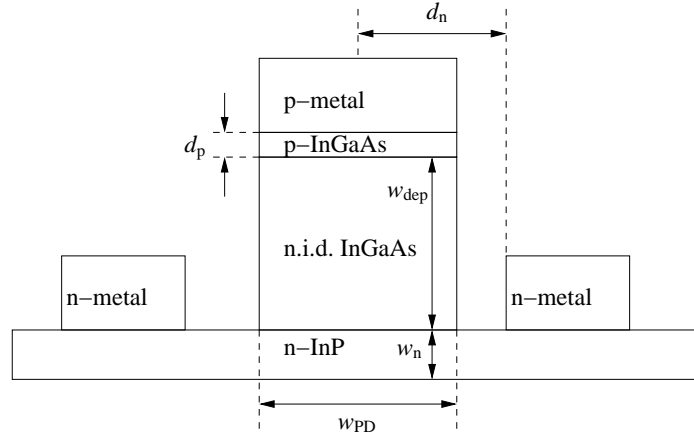**Figure 2.12:** Schematic diagram of the photodetector.

Description	Symbol	Value
mobility of the electrons	μ_n	$10500 \frac{cm^2}{Vs}$
mobility of the holes	μ_h	$420 \frac{cm^2}{Vs}$
specific contact resistance of the n-metal-semiconductor interface	$\rho_{c,n}$	$10^{-6} \frac{\Omega}{cm^2}$
specific contact resistance of the p-metal-semiconductor interface	$\rho_{c,p}$	$10^{-4} \frac{\Omega}{cm^2}$
hole saturation velocity	v_h	$4.8 \cdot 10^6 \frac{cm}{s}$
electron saturation velocity	v_e	$6.5 \cdot 10^6 \frac{cm}{s}$

Table 2.1: Electronic parameters of InGaAs, used as absorption layer in the fabrication of the PD.

and

$$R_{n_{junction}} = \frac{1}{2} \cdot \frac{d_n}{q \cdot \mu_n \cdot N_{dn} \cdot w_n \cdot L_{PD}} \tag{2.17}$$

where d_n (d_p) is the distance from the middle of the detector to the n-contact (p-contact), w_n (w_p) the thickness of the n-doped (p-doped) layer, L_{PD} the length of the detector, q the electron charge, and μ_n (μ_h) the mobility of the electrons (holes). In Eq. 2.17, the factor $\frac{1}{2}$ is due to the use of two n-side contacts. The total series resistance is

$$R_s = R_{p_{metal}} + R_{n_{metal}} + R_{p_{junction}} + R_{n_{junction}}$$

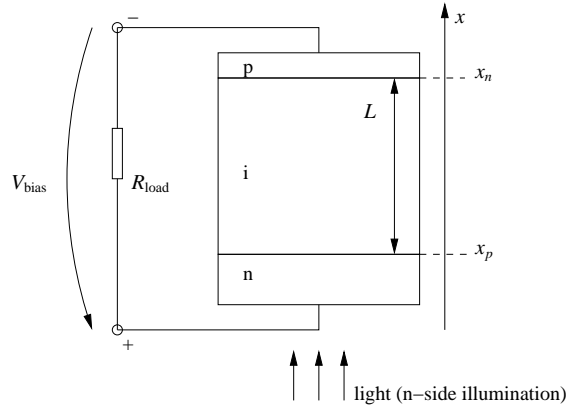Using values reported in Table 2.1, the following values are calculated [66, 67]

Figure 2.13: Schematic diagram of a reversely biased p-i-n junction.

$$
\begin{aligned}
R_{\text{p}_{\text{metal}}} &= 2\,\Omega \\
R_{\text{n}_{\text{metal}}} &= 100\,\Omega \\
R_{\text{p}_{\text{junction}}} &= 1\,\text{m}\Omega \\
R_{\text{n}_{\text{junction}}} &= 5\,\Omega
\end{aligned}
$$

The *RC*-time limited frequency 3-dB cut-off point is defined as

$$
f_{\text{RC}} = \frac{1}{2\pi C_{\text{j}}\left(R_{\text{s}} + R_{\text{load}}\right)} \tag{2.18}
$$

Considering a load resistance of $50\,\Omega$, substitution of the values brings to $f_{\text{RC}} = 110\,\text{GHz}$.

Let us now consider the transit-time limitation. This is analyzed by solving the carrier rate equations for holes and electrons transported in the depletion region of the p-i-n junction and writing the corresponding current density in terms of frequency response. These calculations were outlined by Lucovsky et al. [68] and were used to predict the transit-time limited 3 dB cut-off point of the photodetector frequency response. The following cases were considered for a p-i-n photodiode as schematically sketched in Fig. 2.13:

Uniform illumination In this case, for ease of calculation, it is assumed that the photocarriers are uniformly generated in the diode intrinsic region. The frequency response is plotted in Fig. 2.14 (curve labeled "uniform illumination"), for an absorption layer thickness of 700 nm, while in Fig. 2.15 the 3-dB cut-off point as a function of the absorption layer thickness is plotted. An absorption layer thickness of 700 nm brings to a predicted 3-dB bandwidth of about 35 GHz.

Exponential absorption This case corresponds to a more realistic view, in which the light absorption in the depletion region decays exponentially along *x*. The two cases of illumination from the n-side and from the p-side of the p-i-n junction were analyzed. When
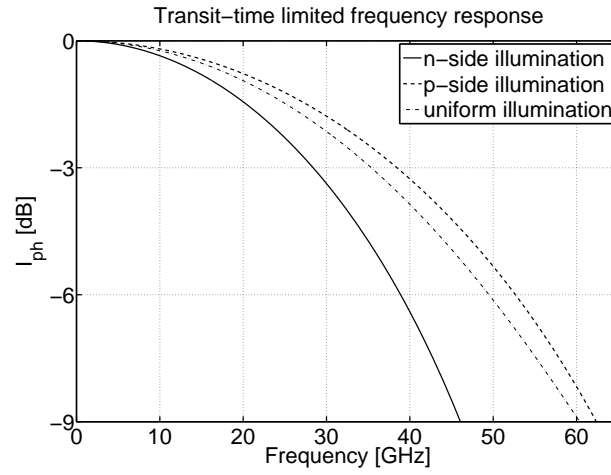
Figure 2.14: Transit time limited frequency response of the p-i-n photodiode calculated as a function of the type of device illumination. The calculations were made for an absorption layer thickness of 700 nm. These curves were generated by using Eq. 37, Eq. 52 and Eq. 56 of Lucovsky et al. [68].

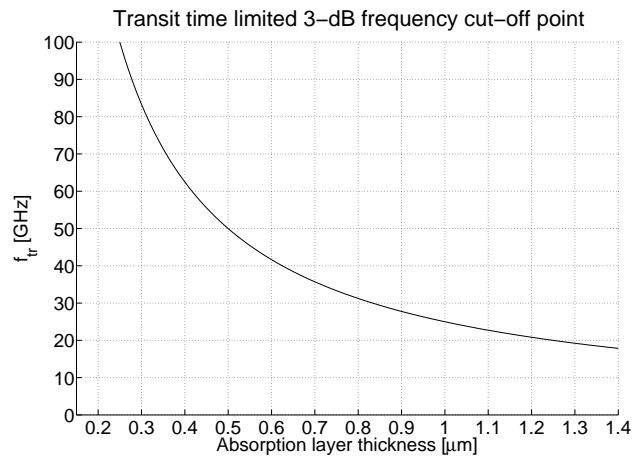**Figure 2.15:** Transit time limited frequency 3-dB cut-off point calculated as a function of the detector absorption layer thickness and under the hypothesis that the absorption layer is uniformly illuminated.

the electron-hole pairs are generated near the n-side, it is the holes that must travel across the depletion region (with velocity v_h) to reach the p-side. Vice versa, when the photocarriers are generated near the p-side, it is the electrons that must travel across the depletion region (with velocity v_e) to reach the n-side. The frequency response for these two cases is plotted in Fig. 2.14.

When reading Fig. 2.14, it clearly appears that a p-side illuminated photodiode is faster as compared to the n-side case. The reason is that electrons and holes have different velocities (v_e and v_h, respectively) in the material; in particular, $v_e > v_h$, as can be read in Table 2.1. That means the time the electrons take to travel to the n-side in a p-side illuminated PD is less then the time the holes take to travel to the p-side in the case of n-side illumination. For the device reported here, the optical signal carried by the photonic wire underneath the bonding layer is first coupled into the n-InP layer through the membrane coupler and then brought towards the absorption region of the detector, as shown in Fig. 2.2. This type of illumination can be considered close to the case of n-side illumination discussed above, according to which a 3-dB cut-off point $f_{tr} = 30$ GHz is expected for the transit-time limited frequency response, as it can be read from Fig. 2.14.

The photodetector 3-dB bandwidth is expressed by

$$\frac{1}{f_{3dB}^2} = \tau_{RC}^2 + \tau_{tr}^2, \tag{2.19}$$

where τ_{RC} and τ_{tr} are the *RC*-time and transit-time constants defined as $\tau_{RC} = f_{RC}^{-1}$ and $\tau_{tr} = f_{tr}^{-1}$, respectively. For the predicted values of $f_{RC} = 110$ GHz and $f_{tr} = 30$ GHz, substitution of the values in Eq. 2.19 leads to $f_{3dB} = 30$ GHz. Eq. 2.19 shows that, with the chosen device geometry, the most limiting factor for the detector speed is the carrier transit time in the diode depletion region.

Device efficiency

Concerning the internal quantum efficiency, first calculations were performed by applying a ray-tracing model, as schematically shown in Fig. 2.16. Assuming that 100% of the optical signal carried by the photonic wire underneath the bonding layer couples into the n-InP membrane layer, the propagation angle θ_0 of the fundamental mode guided by the InP membrane waveguide can be obtained by solving the following equation:

$$N_{0,InP} = \frac{\beta_{0,InP}}{k_0} = n_{InP} \cdot \cos(\theta_0) \tag{2.20}$$

where k_0 is the wave vector and $N_{0,InP} \simeq 2.5$ is the fundamental mode index, which was obtained with 2D mode simulations, as described in Section 2.3.1. The solution of Eq. 2.20 in θ_0 leads $\theta_0 = \simeq 38°$, for transverse electrical (TE) polarization. At the interface with the absorption region, a TE polarized optical signal is transmitted through the InGaAs absorption region with $\theta_t = \simeq 33°$, according to Snell's law [69]. The absorption layer was designed 700 nm thick, as shown in Fig. 2.11, which leads to an effective light path length of AB = 833 nm
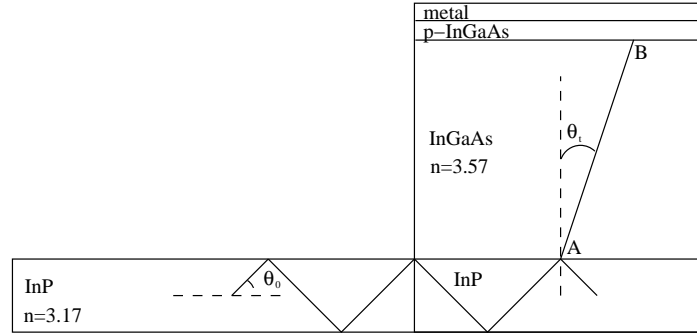
Figure 2.16: Schematic drawing of the detector structure. A ray-tracing model was used to perform the first approximate calculations to investigate the device efficiency.

(see Fig. 2.16). Knowing the InGaAs material absorption constant at $\lambda = 1550$ nm to be $\alpha = 0.7\,\mu\text{m}^{-1}$ [58, 70], the power absorbed in that light path AB can be calculated. If the optical field propagates with an attenuation of $e^{-\alpha \cdot \text{AB}}$, then the power absorbed in the detector InGaAs absorption layer is

$$P_{\text{abs}} = 1 - e^{-2 \cdot \alpha \cdot \text{AB}} \simeq 70\% \tag{2.21}$$

It has to be noticed, however, that these calculations lead to a very rough estimation of the detector quantum efficiency, as the ray-tracing model provides approximate solutions to Maxwell's equations only valid under the hypothesis that the signal's wavelength is much smaller than the space and the objects around which the waves propagate [71]. This is clearly not the case for the detector structure developed in this work, which has an absorption layer thickness of 700 nm, a footprint of few tens of μm^2 and operates at telecom wavelengths. A more accurate investigation of this structure requires wave theory and mode analysis. For that reason, further simulations were performed with the WASMF (Waveguide Analysis with the use of a Scattering Matrix Formalism) 1D mode solver, which performs a 1D slab mode solving of the structure in the vertical direction by using a scattering matrix formalism (SMF) for the field calculation [72], and integral calculations for the field propagation and absorption in the p-i-n photodetector structure. These simulations were performed to estimate the power absorption across the 5 μm wide p-i-n heterojunction, assuming that 100% of the optical signal carried by the photonic wire underneath the bonding layer would couple into the n-InP membrane layer and reach the detector area. Like for the membrane coupler design, 2D mode solver calculations were performed to investigate the optical field guided by the detector input InP membrane waveguide. At the interface with the p-i-n heterojunction, an eigenmode expansion calculation was performed and the absorption of the optical field traveling along the n.i.d. InGaAs layer was calculated. Simulation results show that approximately all the optical power is absorbed within 7 μm, as can be seen in Fig. 2.17 (left). For this reason and including a safe margin, a PD length of 10 μm was chosen. However, part of the power is absorbed in the doped semiconductor layers and in the metal layers. The light absorbed in those regions is lost, as it
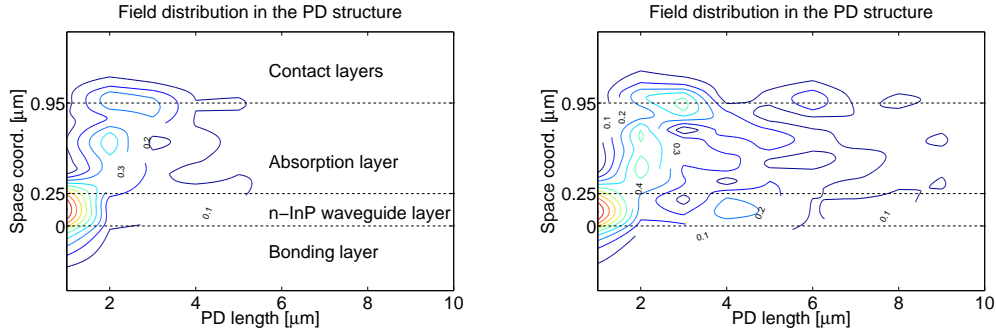
Figure 2.17: Left: The simulated field distribution in the photodetector after the interface between the input waveguide and the p-i-n structure is plotted. Light propagating in the InP waveguide layer is coupled into the absorption layer of the PD. More than 90% of the power is absorbed within 6 μm. Right: The same simulation is repeated, setting the absorption in the p-InGaAs contact layer and in the metal layer to zero.

does not contribute to the generation of the photocurrent. When repeating the simulation after setting to zero the absorption in the doped semiconductor layers and in the metal layers, the field distribution in the PD structure changes: a longer detector is needed to absorb the same amount of power. This can be seen in Fig. 2.17 (right): after 7 μm, ~80% of the optical power is absorbed (as compared to ~100% in the case of Fig. 2.17, left). Because of that, an internal quantum efficiency of ~80% is expected.

The combination of the detector layer stack of Fig. 2.11 and a mesa footprint of $5 \times 10 \, \mu m^2$ is therefore a trade-off between device efficiency and speed. Given the type of detector illumination, the efficiency could be improved by choosing a thicker absorption layer, but this would cause the transit-time to increase and therefore the speed to drop. Vice-versa, thinning down the absorption layer would result in a faster but less efficient photodetector.

2.4   Conclusions

In this chapter, the concept and design of the photodetector developed within this thesis work for use in optical interconnections on Si have been described. The PD structure consists of two parts: an InP membrane input waveguide on top of the bonding layer, meant to provide a good optical coupling from the photonic interconnect waveguide layer underneath up to the PD, and a p-i-n heterojunction, where the optical power is absorbed and converted into an electrical signal.

The membrane coupler was studied with commercially available 2D and 3D mode solvers and with Matlab for the implementation of the equations necessary to apply the coupled mode theory used for the device modeling. Two different InP coupler structures were investigated, for coupling the optical power out of the Si and the Si_3N_4 interconnect waveguides, respectively.

The Si and Si$_3$N$_4$ waveguides have dimensions of $220 \times 500\,\text{nm}^2$ and $400 \times 800\,\text{nm}^2$, respectively, and are defined on a SiO$_2$ buffer layer on top of the Si substrate, while the waveguide top cladding is provided by the bonding layer. The fundamental mode index is about 2.5 and 1.5, respectively, which has to be taken into account when designing the heterogeneous photonic devices defined on top of the bonding layer. For the Si-to-InP coupler, simulations show that the optimum InP waveguide width is around 0.85 µm (1 µm) when the FMM (FD) calculation method is used, while the predicted coupling length varies between 12 and 14 µm, depending on the calculation method used. A coupling efficiency of more than 80% is achieved with a tolerance of ±30 nm for the bonding layer thickness and a deviation of ±70 nm for the InP waveguide width from the optimum simulated geometry, which is achievable with the current technology limitations. The coupling efficiency drops to 50% (3 dB drop) for a waveguide-to-waveguide lateral misalignment of ±370 nm or an angular misalignment of ±1.1°, which is within the limitations of our fabrication technology. For the Si$_3$N$_4$-to-InP coupler, the InP waveguide simulated optimum width is 340 nm, which requires a more complicated and time consuming processing, because of the use of EBL for waveguide definition. The Si-to-InP coupling structure is easier to manufacture, due to the closer optical refractive indices of InP and Si waveguide cores. Therefore, the InP membrane input waveguide is implemented only in the mask set for the realization of the detectors bonded on Si photonic waveguides, while a different approach is used for the PDs bonded on Si$_3$N$_4$ waveguides, as explained further in Section 4.6.

The detector layer stack is built as a 700 nm n.i.d. InGaAs absorption layer sandwiched by a highly p-doped 50 nm thick InGaAs contact layer and a highly n-doped 200/250 nm thick InP layer, for bonding on Si$_3$N$_4$ or Si waveguides, respectively, and the mesa footprint is $5 \times 10\,\text{µm}^2$. This geometry is a trade-off between device efficiency and speed. According to the simulation results, the expected PD internal quantum efficiency is ~80%, limited by the loss of optical power in the metal contact layers and in the metal layer stack, while the expected 3 dB bandwidth is around 30 GHz, limited by the transit-time of the carriers in the diode depletion region.
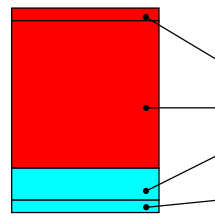
Chapter 3

InP-on-Si Heterogeneous Technology

In this chapter, the fabrication technology used for manufacturing the devices presented in this thesis is described. The integration scheme used to heterogeneously integrate the silicon (Si) based and the indium phosphide (InP) based components on a single chip is first described. Then, the details of the bonding technologies used for the integration of the InP active devices and the Si passive components are discussed, as well as the process flow developed for the InP device fabrication.

3.1   Introduction

The integrated devices presented in this thesis are designed for use in optical interconnections on electronic integrated circuits (ICs). In Chapter 1, the improvements provided by using a photonic interconnection layer on Si ICs with respect to the all-electrical solutions, currently used for on-board and on-chip interconnects, were discussed. In this chapter, the fabrication technology used for the realization of such integrated devices developed in this work is described in detail. The approach used for the fabrication of the integrated components is based on an InP-on-Si heterogeneous technology, in which the Si-based passive circuitry is patterned on an SOI wafer or on a complementary metal-oxide semiconductor (CMOS) wafer, on top of which an InP layer stack is bonded upside down and used for processing the InP-based active components. The following devices and circuits were manufactured within this PhD framework by using such heterogeneous technology approach:

InP-based photodetectors (PDs) bonded on SOI The layer stack used for the fabrication of these photodetectors is shown in Fig. 2.11, while a schematic drawing is shown in Fig. 2.2. The PD structure is grown by Metal-Organic Vapor-Phase Epitaxy (MOVPE) on a 2" InP wafer, which is diced and die-bonded upside down on an SOI wafer via

Material	Thickness	Doping/Function
p–InGaAs	50 nm	1.6E19 p–contact layer
InGaAs	700 nm	n.i.d. absorption layer
n–InP	150 nm	1E18 n–contact layer
n–InP	50 nm	n.i.d.

Figure 3.1: Layer stack of the PD structures bonded on Si_3N_4 waveguides defined on top of a CMOS wafer. The layer stack is shown upside down as it is bonded on the CMOS wafer.

direct molecular bonding. A Si waveguide interconnect layer is patterned on top of the SOI wafer before the bonding: the Si photonic waveguides are defined via 193 nm Deep Ultra-Violet (DUV) lithography on a SiO_2 insulator layer on top of an 8" Si wafer and etched in two steps to realize shallowly and deeply etched passive structures. The PD structure consists of two parts: an InP membrane input waveguide on top of the bonding layer, meant to provide a good optical coupling from the Si waveguide in the photonic interconnect layer underneath the bonding layer to the PD absorption region, and a p-i-n heterojunction, where the optical power is absorbed and converted into an electrical signal.

InP-based PDs bonded on CMOS The detectors designed for this application use the layer stack shown in Fig 3.1, which is grown by MOVPE on a 2" InP wafer. After growth, the InP wafer is bonded upside down on a CMOS wafer via direct molecular bonding. Si_3N_4 interconnect waveguides are processed on a Plasma Enhanced Chemical Vapor Deposition (PECVD) nitride layer deposited on a SiO_2 buffer layer on top of the CMOS wafer before the bonding. Si_3N_4 waveguides do not allow for the same high wire integration density that can be achieved with Si waveguides, but they do offer an easier integration with the CMOS ICs. In this case, the PD structure is built as a p-i-n heterojunction stacked on top of the bonding layer and aligned over the interconnect waveguide underneath. No InP membrane input waveguide is used for this detector structure, as it would require a more complicated and time consuming processing because of the need of electron-beam lithography (EBL) for waveguide definition, as explained in Chapter 2.

Photonic link on SOI A full point-to-point photonic link was realized on an SOI wafer with Si photonic interconnect waveguides defined via 193 nm DUV lithography on a SiO_2 insulator layer on top of the Si substrate and with InP-based micro-disk lasers (MDL) and detectors. The MDL and PD layer stacks are grown by Solid Source MBE and MOVPE, respectively, on 2" InP wafers that are then diced and flip-chip bonded on the 8" SOI wafer via direct molecular bonding. Even though the processing of the bonded InP dies is compatible with wafer scale Si processing, the wafer is sawn in $9 \times 4.5\,mm^2$ small pieces to allow for processing in the COBRA clean room. Within this thesis work,

the PDs were developed and processed in parallel with the MDLs. Despite the detector structure does not change with respect to the one previously described, the integration with the MDL required some key changes in the process flow, which are highlighted in this chapter.

Multiwavelength receivers (MWRs) on SOI Heterogeneously integrated MWRs were realized on an 8" SOI. The MWRs are built of InP-based detectors processed on an InP die BCB-bonded upside down on the SOI wafer. In the Si interconnect waveguide layer patterned via 193 nm DUV lithography on top of the SOI wafer, the receiver passive components are defined, namely waveguide and demultiplexer structures. The PD structures use the layer stack shown in Fig. 2.11 and are aligned over the demultiplexer output waveguides. However, the process flow differs due to the different bonding technology used for the realization of this chip. In this chapter, the main differences are discussed.

In the following sections, the details of the bonding technology and of the InP-based die processing used for the realization of the chips mentioned above are described.

3.2   Bonding technology

The opto-electronic chips presented in the previous section are all based on InP-on-Si technology. In this section, the integration scheme used for the fabrication of the heterogeneously integrated components is described.

The InP-based active components, namely PDs and MDLs, are grown one 2" InP wafers, by MOVPE and MBE, respectively, which are then cleaved in dies of approximately $9 \times 4.5 \, \text{mm}^2$. The unprocessed dies are flip-chip bonded onto the SOI or the CMOS wafer, on which a Si or Si_3N_4 waveguide layer is patterned on top of a 1-2 μm thick SiO_2 buffer layer. These Si or Si_3N_4 waveguides provide the optical interconnections between the active photonic devices. The on-plane die alignment to the interconnect waveguides is not critical, as the InP dies are still unprocessed at bonding time. The die orientation with respect to the major and minor crystal axis of the InP wafer is more important, as it would influence the sidewall profile of the InP-based wet-etched structures. This is not an issue for the MDLs, which are dry-etched, but is relevant for the detector mesas, which are indeed wet-chemically etched. As it can be seen from the PD layer stack of Fig. 2.11 and Fig. 3.1, the detector mesa is built as a 700 nm n.i.d. InGaAs layer. During the wet-etch, which is performed with a $H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 10$ solution, selective to InP [73], the detector mesa sidewalls assume a "V-groove" or a "dovetail" profile depending on the die orientation with respect to the major and minor wafer flat. In particular, "V-groove" and "dovetail" profiles are obtained when the die is aligned along the major and minor flat of the InP-based wafer, respectively. This was verified by experiments performed in the clean room on test samples containing an InP/InGaAs stack on an InP substrate: waveguides aligned to the major and minor wafer flat were patterned by optical lithography and wet-etched with selective solutions. Fig. 3.2 shows Scanning Electronic Microscope (SEM) pictures of the different sidewall profile for waveguides aligned to the two main orientations of the InP crystal. Having a "V-groove" profile of the mesa sidewalls is
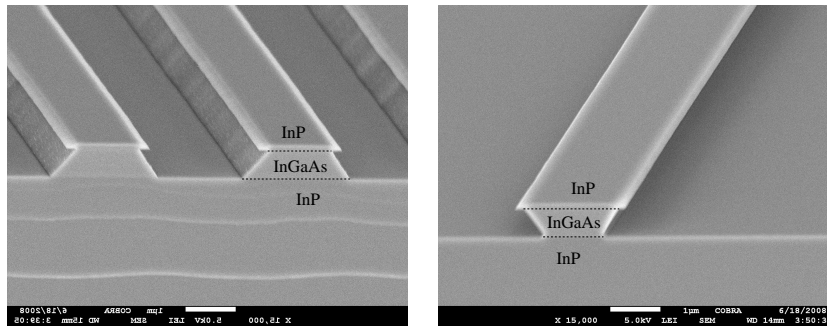
Figure 3.2: SEM pictures of InGaAs structures on an InP substrate wet-etched with diluted H_2SO_4 and by using a 100 nm thick InP layer as a mask. On the left (right) picture, structures are aligned along the major (minor) crystal axis of the InP substrate.
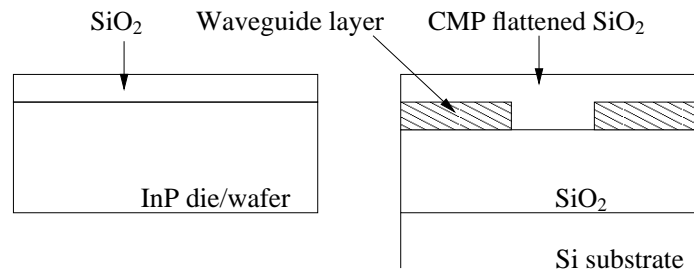

Figure 3.3: Direct molecular bonding. The 2" InP wafers containing the active device layer stacks and the 8" SOI or CMOS wafer that will host the Si or Si_3N_4 interconnect waveguides are grown separately. A layer of SiO_2 is deposited on top of the InP-based unprocessed wafer and on the Si processed wafer. Before the actual bonding process, the SiO_2 on the Si wafer is flattened by CMP.

important for the device metallization step, as it brings to a better quality of the detector top metal contact. When bonding the InP dies upside down, the structure sidewall profiles shown in Fig. 3.2 appear reversed. Clearly, that has to be taken into account, and the InP detectors were intentionally aligned along the InP crystal minor axis in order to eventually obtain a mesa sidewall "V-groove" profile. The direct molecular bonding and the BCB-bonding techniques are used for developing the InP-on-Si devices presented here. In the following, details of such technologies are given:

Molecular Bonding The 2" InP wafers containing the active device layer stacks and the 8" SOI or CMOS wafer that will host the Si or Si_3N_4 interconnect waveguides are grown separately. A layer of SiO_2 is deposited by PECVD on top of the 2" InP wafer and the processed Si wafer (see Fig. 3.3) and thinned down by Chemical Mechanical Polishing (CMP), in order to achieve a bonding layer thickness and roughness suitable for both
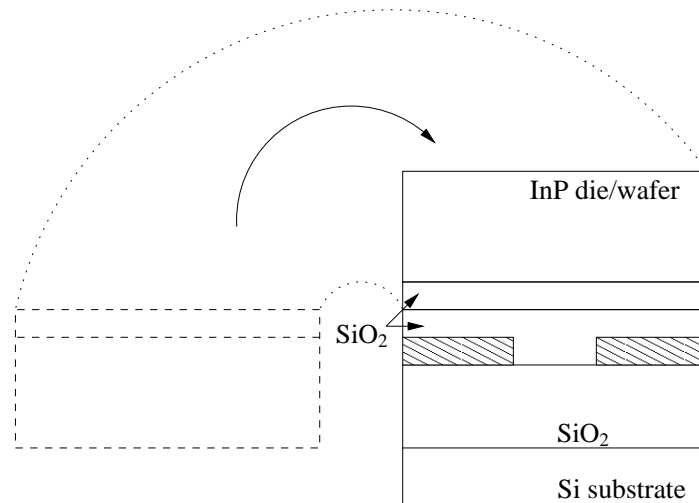
Figure 3.4: The InP layer stack is bonded upside down on the Si wafer, so that the two SiO$_2$ layers are put in contact. In this way, Van Der Waals atomic bonds "glue" the wafers.

bonding feasibility and good optical coupling between the InP waveguide and the Si or Si$_3$N$_4$ wires: the waveguide-to-waveguide vertical spacing is chosen to be 300 nm or 500 nm, respectively. Afterwards, the InP layer stack is bonded upside down on the Si substrate, so that the two SiO$_2$ layers are put in contact (see Fig. 3.4): Van Der Waals atomic forces "glue" the wafers. The SiO$_2$ bonding layer thickness and surface roughness are critical to achieve a good bonding. Requirements in terms of Root Mean Square (RMS) roughness of the wafer surface are below 1 nm. RMS surface roughness measurements were performed by Atomic Force Microscope (AFM) to check the surface quality of the 2" InP wafer with the PD layer stack grown at the COBRA research institute by MOVPE: an RMS surface roughness of about 1.8 nm was measured with an AFM scan over an area of 100 μm^2. After polishing the SiO$_2$ layer deposited on the wafer, the molecular bonding could be performed. For the SOI or CMOS wafer, the flatness, as well as the thickness, is determined by the CMP process quality and control. More details about the molecular bonding technology can be found in [74].

Adhesive Bonding A diluted Benzo-Cyclo-Butene (BCB) polymer layer is used in this case to glue the InP dies to the Si wafer. Given the similar properties of BCB and SiO$_2$ in terms of optical refractive index at telecom wavelengths, the same bonding layer thickness is used. The BCB is first spin coated onto the Si wafer to planarize the surface where the interconnect waveguides are patterned. Then, a baking step at 150°C is performed to remove residual solvent in the polymer and a following partial polymerization is achieved with a short curing step at 250°C, which transforms the BCB into a gel rub-
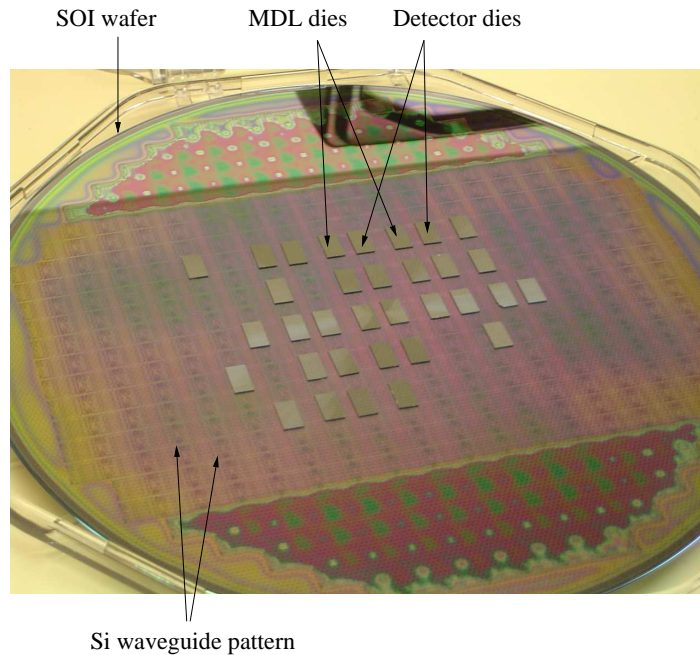
Figure 3.5: InP-based unprocessed dies bonded upside down on an 8" Si wafer, on top of which the Si waveguide layer have been patterned.

ber. At this point, the InP-based dies are flip-chip bonded on the Si substrate in a vacuum environment, to prevent the trapping of air bubbles at the bonding interface. Finally, the BCB is fully polymerized by curing at 250°C for over an hour in a nitrogen environment, to prevent oxidation. This technique provides relaxed tolerance towards wafer surface roughness as compared to molecular bonding. Further details about the BCB bonding technology can be found in [54].

After bonding, the exposed InP substrate is finally thinned down by CMP and wet-chemically removed with an HCl diluted solution. Fig. 3.5 shows InP dies belonging to two different wafers, with laser and detector layer stack, respectively, die-to-wafer bonded upside down on an 8" Si wafer, on top of which a Si waveguide layer has been patterned to interconnect the active photonic devices processed on the dies. An overview of other bonding techniques that were investigated to heterogeneously integrate III-V devices with SOI photonic circuitry can be found in [49].

3.3 InP-based detector processing

3.3.1 Photodetectors onto Si/Si$_3$N$_4$ waveguides on SOI and CMOS wafers

In this section, the processing of the detectors molecular-bonded onto Si waveguides defined on a bare SOI wafer and onto Si$_3$N$_4$ waveguides defined on a CMOS wafer is discussed. The PD structure layer stack used in these samples is shown in Fig. 2.11 and Fig. 3.1. The process flow is shown in Fig. 3.6 and the steps are described as follows:

Detector waveguide layer definition This is the first lithography performed on the unprocessed InP die after the bonding; in particular, the InP waveguide layer of the PD structure is defined in this step (Fig. 3.6, A). The alignment of the InP waveguides to the Si waveguides patterned in the interconnect waveguide layer of the Si wafer is critical, as it influences the coupling efficiency of the PD input InP-membrane coupler structure (see Fig. 2.2). To achieve an accurate alignment of the PD structures on the Si waveguides, the detector InP membrane waveguide layer is patterned by EBL at CEA-LETI, and transferred to a 150 nm thick SiO$_2$ hard mask (see Fig. 3.7). For the PD structures on Si$_3$N$_4$ waveguides, the alignment is done by optical lithography, as the PDs developed for this application do not use any input membrane coupler and no critical structures have to be defined, in terms of feature size, as explained in Section 2.3.1. In this case, the detector pattern is transferred to a 50 nm thick Si$_3$N$_4$ hard mask, previously deposited by PECVD.

Waveguide etching The detector InP waveguide pattern is etched in two steps. In this first step, a partial InP Reactive Ion Etching (InP-RIE) is performed using a CH$_4$: H$_2$ = 20 : 80 standard cubic centimeters per minute (sccm) gas mixture at a plasma RF power of 220 W and a descum of 100 sccm O$_2$ flow every 2 minutes at a power of 200 W to remove the polymer formation on the sample (Fig. 3.6, B). A thin layer of InP (about 100 nm) is intentionally left to protect the SiO$_2$ bonding layer during the top hard mask removal (see Fig. 3.8). This is a very critical step, as it requires an accurate control of the etching process parameters in order to stop the RIE in the n-InP layer. Leaving a thin film of InP is necessary to safely remove the hard mask afterwards, without etching the silica bonding layer underneath. Some dummy etching cycles were performed to obtain the InP and InGaAs etch rate. Around 30 minutes of RIE are necessary to etch the die layers down to the n-InP bottom layer. In our InP-RIE process, the SiO$_2$ is etched with a rate of 2-3 nm/min. Thus, during this processing step, the hard mask is thinned by 60-90 nm. This effect is taken into account for the following steps.

SiO$_2$ hard mask removal The hard mask is removed with a SiN-RIE step (see Fig. 3.9), while keeping the bonding layer protected by photoresist (PR) patterned by optical lithography (Fig. 3.6, C). It is important to optimize this step to minimize the chemical attack to the SiO$_2$ bonding layer areas that are not covered by the resist or the InP-based die (see Fig. 3.10). Dummy samples were used to find out the SiO$_2$ hard mask etch rate in our RIE process, which is optimized for Si$_3$N$_4$ etching. A SiO$_2$ etch rate of ~30 nm/min was derived from measurements performed with a profilometer. Considering that the
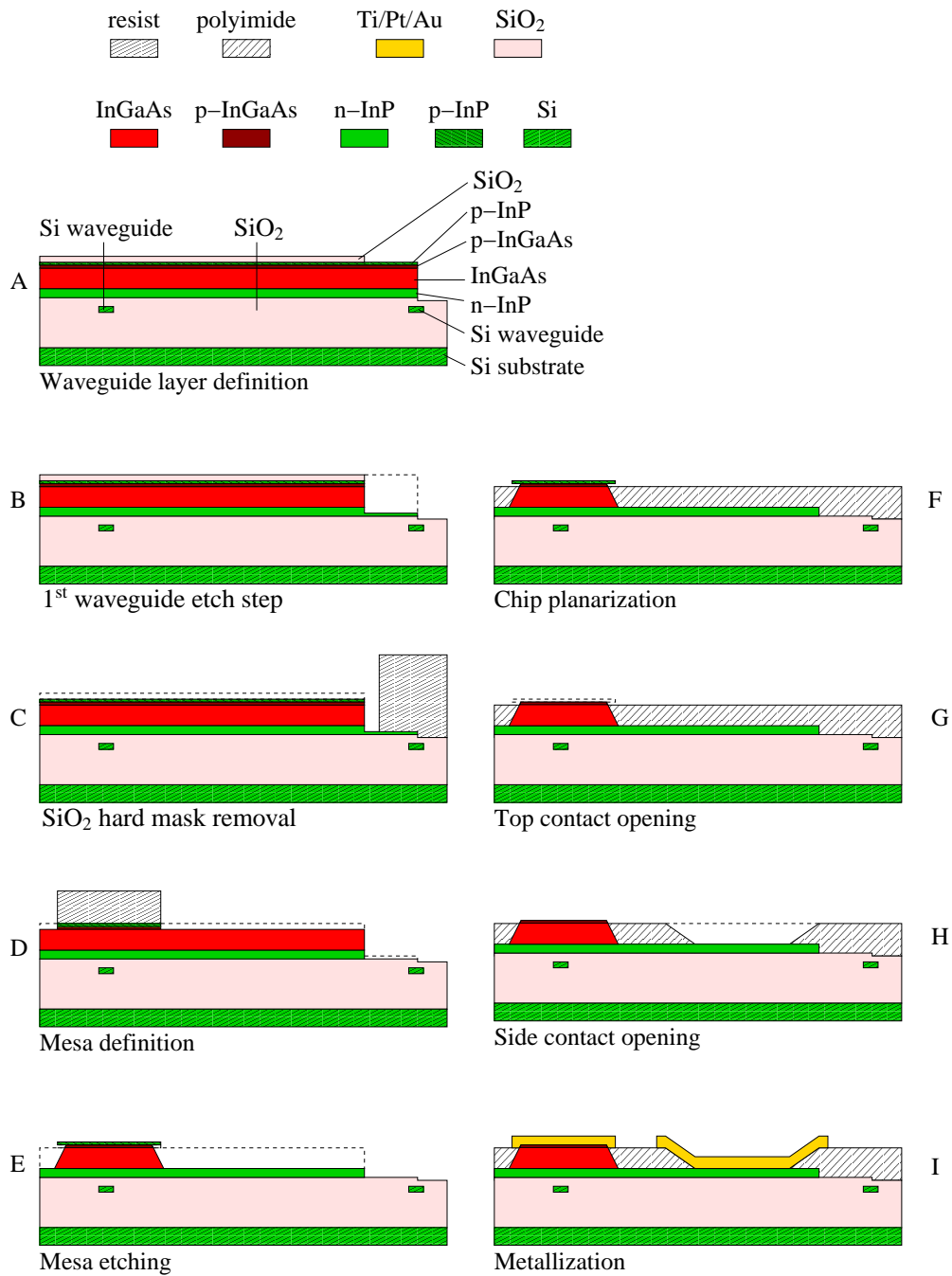
resist   polyimide   Ti/Pt/Au   SiO$_2$

InGaAs   p–InGaAs   n–InP   p–InP   Si

A — Waveguide layer definition

SiO$_2$
p–InP
p–InGaAs
InGaAs
n–InP
Si waveguide
Si substrate

B — 1st waveguide etch step

C — SiO$_2$ hard mask removal

D — Mesa definition

E — Mesa etching

F — Chip planarization

G — Top contact opening

H — Side contact opening

I — Metallization

Figure 3.6: Process flow of InP detectors bonded on SOI.

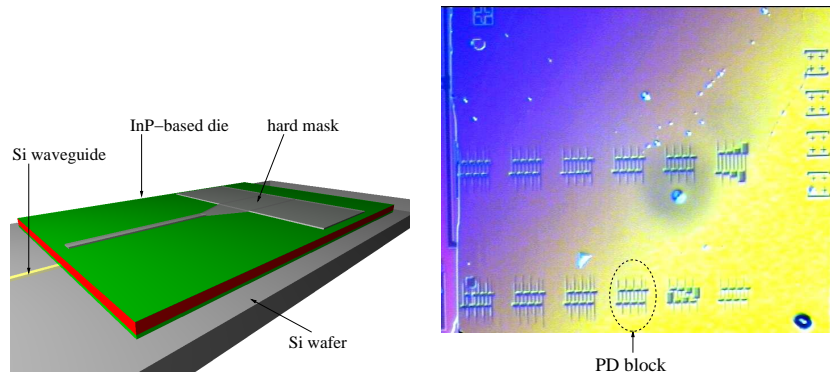Si waveguide   InP–based die   hard mask

Si wafer

PD block

Figure 3.7: Schematic picture of the InP-based die bonded on top of the Si wafer. The PD shape is patterned by the hard mask on top of the layer stack.

Thin InP layer left

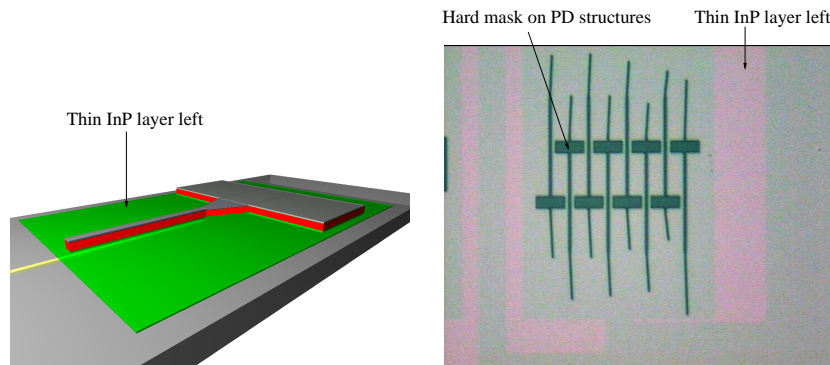Hard mask on PD structures   Thin InP layer left

Figure 3.8: Incomplete RIE of the membrane waveguides.

hard mask becomes thinner during the previous partial InP-RIE step and that an over-etching time is necessary to be sure of completely removing the silica from the top of the PD pattern, the SiO_2 hard mask is removed with a 4.5 min long SiN-RIE process, which employs a $CHF_3 : O_2 = 50 : 5$ sccm gas mixture at a plasma power of 100 W. In Fig. 3.11, photographs taken with optical microscope of detector structures before RIE (with the hard mask on top) and after RIE (with the 20 nm p-InP exposed) can be seen. The color difference visible at the optical microscope, due to the light interference through different materials, is used for evaluating the etch process.

PD mesa definition The PD mesas are defined by 405 nm Ultra-Violet (UV) optical lithography (Fig. 3.6, D). The lithography parameters are optimized for this step, as the detector mesas have to be defined on top of the 800-900 nm high InP epitaxial areas that were masked during the previous waveguide dry-etching. This affects the mesa lithography
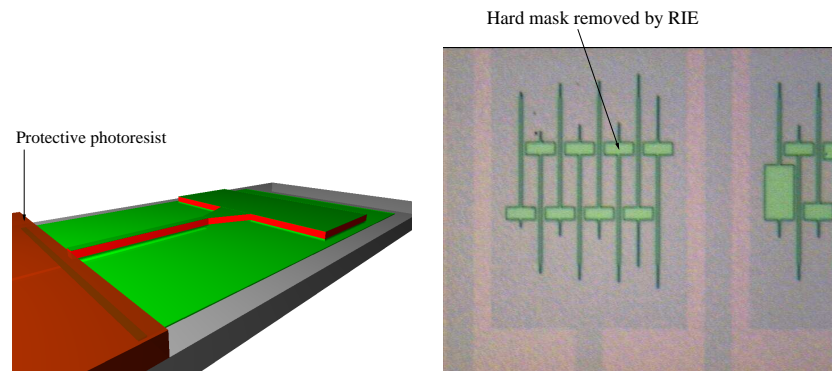
Hard mask removed by RIE

Protective photoresist

Figure 3.9: Dry-etch of the hard mask. Photoresist patterned by optical lithography was used to mask the bonding layer during the RIE process.

Si waveguide bus   Si grating couplers

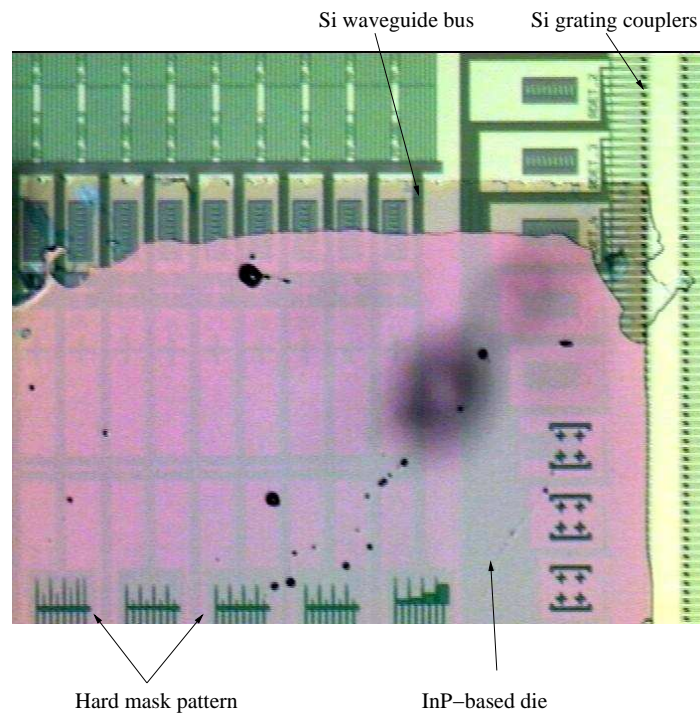Hard mask pattern   InP−based die

Figure 3.10: Picture of the InP die corner bonded on the Si wafer. The hard mask pattern on top of the PD structures is visible at the very bottom of the picture. Some Si waveguides and gratings which are not covered by InP-based epitaxial material are indicated.
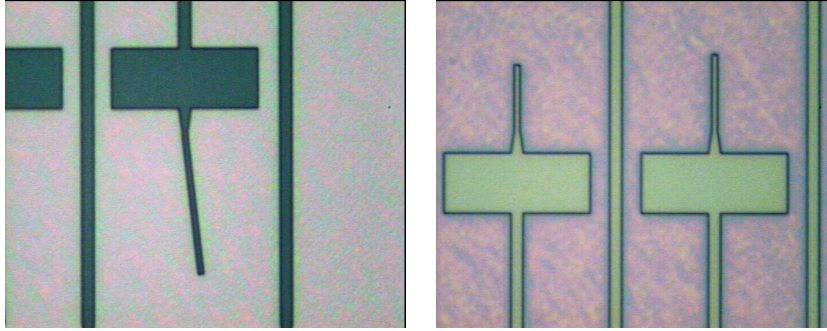
Figure 3.11: Picture of PD structures with slanted input waveguides before RIE (left) and with straight input waveguides after RIE (right).

in the following way. The positive photoresist used for this lithography step (HPR 504) is spun on the sample at 3000 revolutions per minute (rpm) for 30 seconds, which leads to a resist thickness of about 750 nm on a flat substrate. After spinning, the resist on the sample is normally soft-baked at 100°C for 2.5 minutes and the sample exposed to UV light for 4.2 seconds. A following sample post-bake for 1.25 minutes at 115°C and a resist development for 1.25 minutes in the HPR 504 developer (PLSI : $H_2O = 1 : 1$) would normally provide a good definition of the optically patterned structures. However, the spun resist profile follows the substrate surface morphology and a thicker layer of resist accumulates close to the surface steps. In our case, these are the areas of interest, where the PD mesas have to be patterned. To compensate for the thicker HPR 504, a sample overexposure of 6.8 seconds is applied, which results in a good structure definition and a successful resist developing. The HPR 504 is left over and hard-baked to 120°C to protect the mesas during the following RIE step, performed to etch the remaining 100 nm thick InP layer on the die, around the PD structures (see Fig. 3.12).

HPR 504 mask removal The HPR 504 mask is removed with an acetone vapor exposure with the sample upside down to avoid that the PR would fall onto the PD structures, followed by conventional liquid acetone treatment. To remove further residues of HPR 504, oxygen stripping at 300 W for 30 minutes is applied. This causes the oxidation of a few nm of the semiconductor exposed to the oxygen plasma. To remove this thin oxidized layer, a 2 minutes dip in $H_3PO_4 : H_2O = 1 : 10$ solution is used.

Mesa etching After the HPR 504 removal, the exposed 20 nm thick p-InP layer is used to selectively wet-etch the PD mesas with a $H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 10$ solution (see Fig. 3.13 and Fig. 3.6 E). This concentration provides a 900 nm/min InGaAs etch rate, therefore a 1 minute etching is applied to etch the PD mesa.

Planarization and passivation Polyimide (PI) PI 2723 is spun and baked at 300°C several times to planarize the chip surface and provide electrical isolation (Fig. 3.6, F). A Ten-
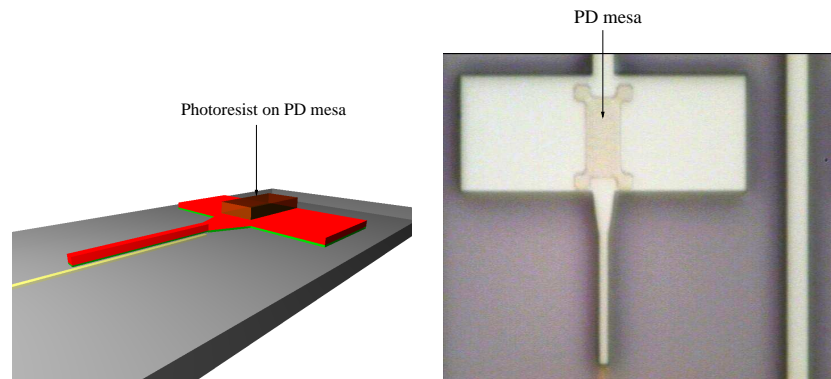
Figure 3.12: Complete RIE. The PD mesas were patterned and masked with photoresist, as indicated in the picture.
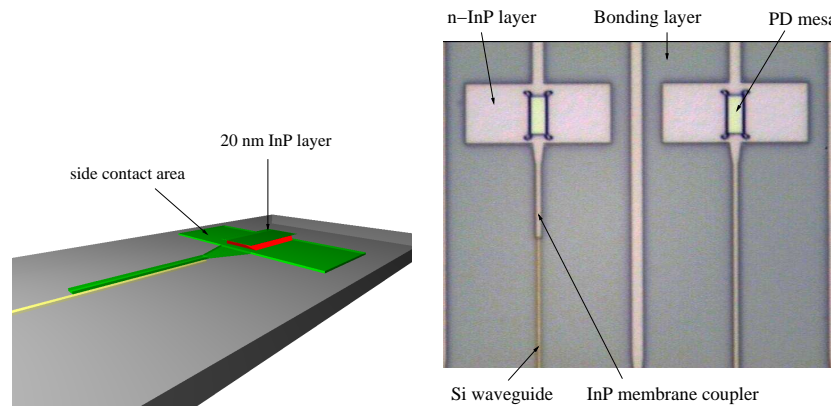

Figure 3.13: Complete RIE. The PD mesas were patterned and masked with photoresist, as indicated in the picture.
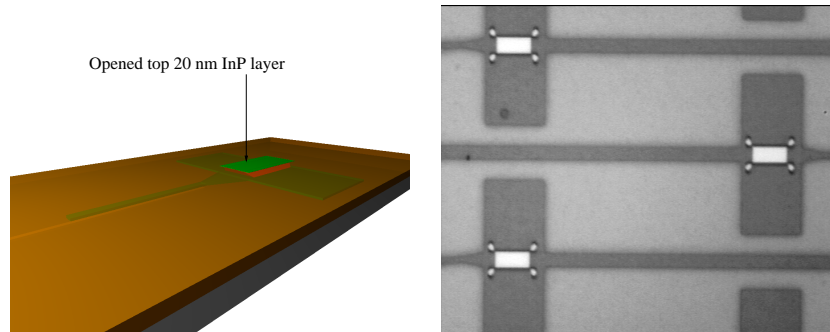
Figure 3.14: Polyimide etch back. The top 20 nm InP layer is open after the dry-etch.
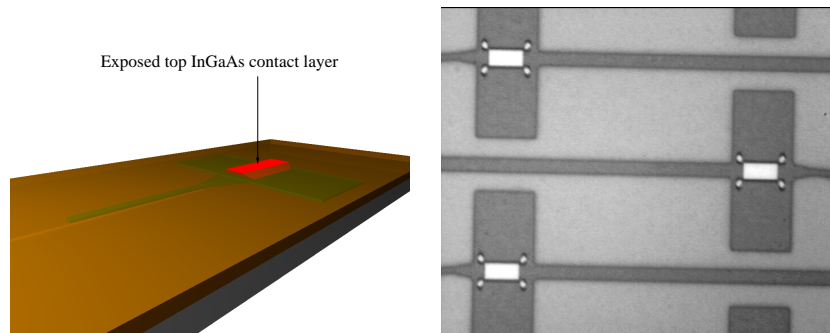

Figure 3.15: Removal of the 20 nm InP layer. The InGaAs top contact layer is exposed after the wet-etch.

cor profilometer is used to monitor the degree of planarization of the chip surface by measuring the PI 2723 step height on the PD mesas, about 1 μm high. After 4-5 PI 2723 layers, typical step height values are 20-30 nm, which provides good conditions to start the polymer etch-back. A barrel etcher is used to isotropically etch back the PI 2723 with the following gas mixture to open the PD mesas (see Fig. 3.14): gas compositions of $CF_4 : O_2 = 45 : 5$ and $CF_4 : O_2 = 35 : 15$ sccm at a plasma power of 300 W are used for faster and slower PI 2723 etching, respectively. This process is done in several etching steps, of 1 or 2 minutes each, to avoid the heating of the sample, that would cause the polymer etch rate to increase and make the whole process difficult to control. The process chamber is equipped with a Faraday cage to prevent damages to the sample surface caused by ion bombardment occurring during the etching process.

Contact opening The top p-contact is opened by selectively removing the 20 nm InP layer used for masking the mesa wet-etch (see Fig. 3.15 and Fig. 3.6, G). An $H_3PO_4 : HCl =$

PI layer   PR mask

Side contact windows

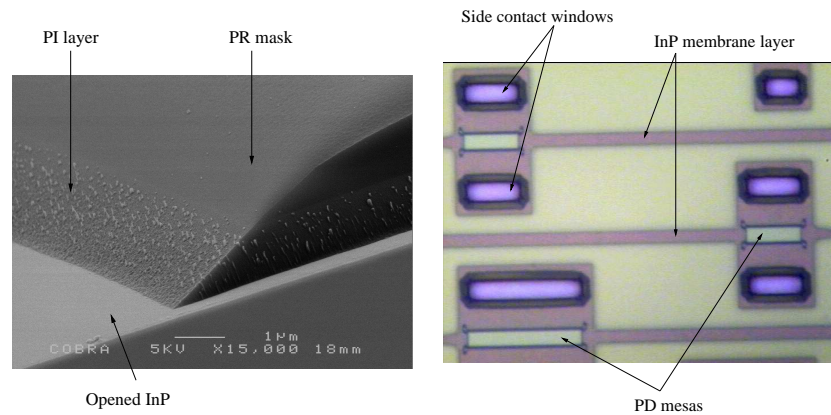InP membrane layer

Opened InP

PD mesas

Figure 3.16: SEM picture (left) and a picture taken with optical microscope (right) of InP side-contact windows. The shape of the sloped sidewalls of the masking PR is transferred to the PI 2723 underneath in the anisotropic etch process.

20 : 1 solution, selective to InGaAs, is used for that purpose. The InP etch rate of this diluted HCl solution is around 90 nm/min, therefore a 30 seconds wet etching is performed to guarantee the InP layer removal. The opening of the side n-contacts is more complicated and is described as follows. Firstly, the contact windows are defined by optical lithography, using a negative photoresist (MaN 440). As the n-InP contact layer is 750 nm lower than PI 2723 surface, sloped polyimide sidewalls are fabricated to avoid any open circuit after the following metal evaporation and lift-off steps. Therefore, the masking photoresist is baked at 120°C for strengthening it and giving its sidewalls a slanted "V-groove" profile, suitable for the purpose just mentioned, and the PI 2723 underneath is then anisotropically etched in a SiN-RIE process with a mix of $O_2 : CHF_3 = 20 : 2$ sccm gas composition at a plasma RF power of 100 W (see Fig. 3.6, H). These process parameters lead to a 230-250 nm/min etch rate for both the MaN 440 and the PI 2723, therefore an accurate control of the MaN thickness and of the PI etching process is necessary. In particular, it is necessary to have the masking PR layer thicker than the PI layer that has to be etched: in our case, the MaN 440 is spun at 2000 rpm for 30", giving a layer thickness in the range of 2.7-3 μm. It is also important to control the whole etching time: that can be estimated based on the measured polymer etch rate, but on the other hand an over-etch is always necessary to guarantee the PI removal. During the over-etching time, the masking MaN is also etched, as well as the exposed semiconductor material (even though with much slower speed). With a thickness of around 2.7-3 μm, the MaN mask is sufficiently thick as to stand even a long (a few minutes) PI over-etch, while the erosion of the exposed InP is negligible, as the etch rate of that material in this anisotropic polymer etching process is around 3 nm/min. Fig. 3.16 shows a SEM picture (left) and a picture taken with optical microscope (right) of InP windows opened with 7 minutes of such etching process. The MaN is then removed by putting
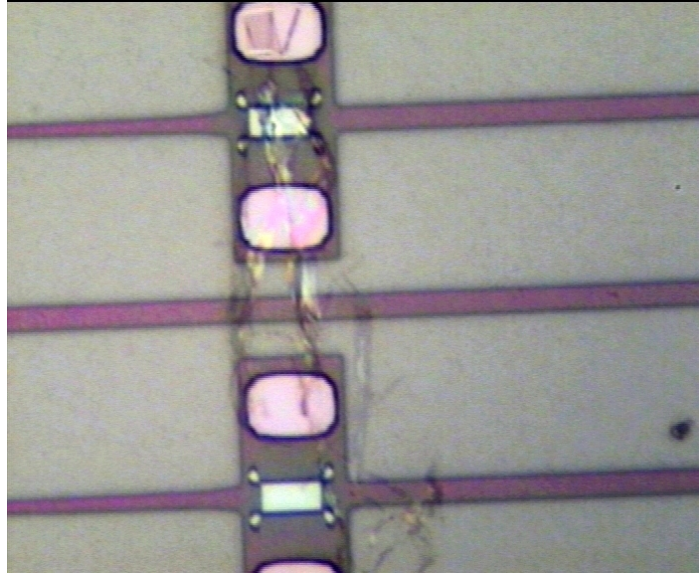
Figure 3.17: Traces of MaN 440 redeposited on the PD structures after acetone treatment with the sample facing upwards. This problem was solved by putting the sample upside down in the acetone vapor bath.

the sample upside down in the acetone vapor for a few hours and acetone liquid for a few minutes. During the acetone treatment, the MaN redeposition onto the PD structures has to be accurately avoided. The redeposited MaN would indeed stick to the sample surface, like shown in Fig. 3.17, and it would be very hard to remove, considering the fact that aggressive oxygen stripping could not be an option as it would remove the polyimide as well. This is avoided by placing the sample upside down in the acetone vapor and liquid bath, as it can be seen in Fig. 3.18. After MaN removal, a Tencor profilometer scan over a PD structure gives the profile shown in Fig. 3.19.

Metallization The metal pattern is defined by optical lithography. The open contact windows are cleaned with a $H_3PO_4 : H_2O = 1 : 10$ solution before the metal deposition. A stack of Ti/Pt/Au, with thickness of 25/75/300 nm is evaporated and patterned by lift-off (see Fig. 3.20 and Fig. 3.6, I). The lift-off step is optimized by investigating the metal lithography parameters. For that lithography, the MaN 440 negative PR is spun at 2000 rpm for 30 seconds and soft-baked at 90°C for 5 minutes. Then, a multiple 4×100 seconds long UV light exposure followed by resist development in pure MaN developer (MaD) for 90 seconds is performed. These process parameters lead to an MaN sidewall profile suitable for the definition of the metal pattern that has to be defined on the chip. From Fig. 3.6 (I), the importance of having a "V-groove" profile of the mesa sidewalls is more clear: the etched-back PI has a good adhesion to the PD mesa. on top of which the metal

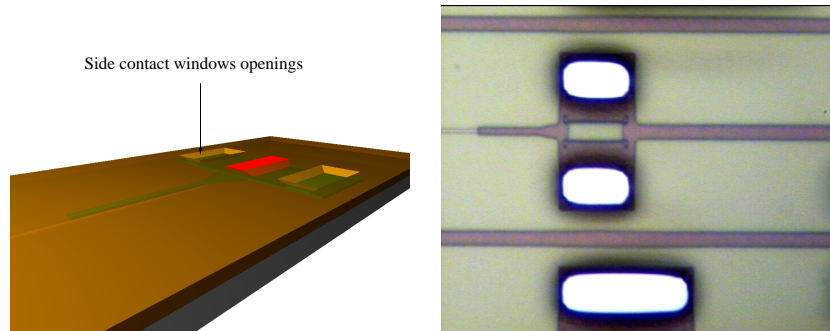**Figure 3.18:** Dry-etch of the polyimide for opening the side contact windows. An anisotropic etch was performed by using the photoresist as a mask to obtain sloped sidewalls.
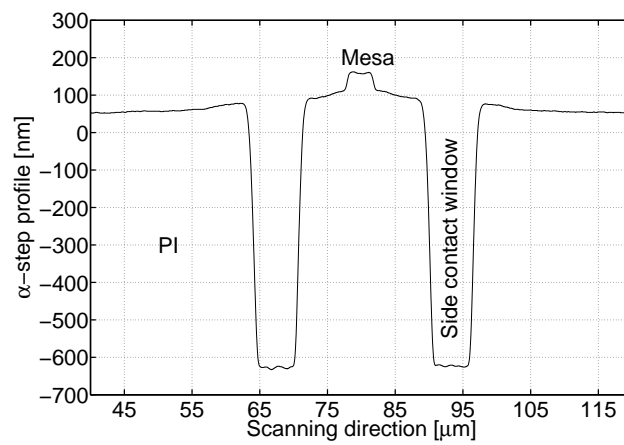

Figure 3.19: Tencor α-step measurement of the chip profile after opening the detector n-contact windows. The measurement scan was performed on a detector structure: the device mesa and side contacts are indicated.
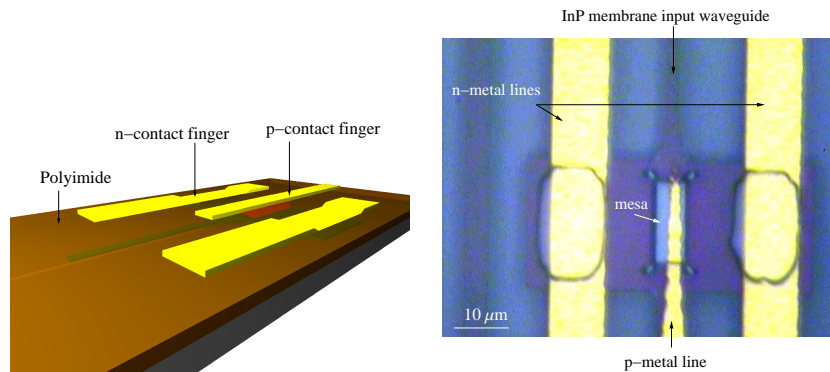
Figure 3.20: Schematic drawing (left) and a picture taken with optical microscope (right) of a metalized photodetector.

is evaporated. Fig. 3.21 shows a picture of the fabricated devices.

3.3.2 Fabrication process for a full optical link on SOI

For manufacturing a full point-to-point photonic link on SOI, the InP-based detectors presented in this thesis are integrated with the microdisk lasers developed by the University of Ghent [75]. The InP dies containing the MDL and PD epitaxial layer stack are molecular-bonded upside down on the SOI wafer on top of which Si photonic interconnect waveguides have been defined, like shown in Fig. 3.5. The Si wafer is sawn in $9 \times 4.5\,\text{mm}^2$ samples, each hosting the PD and the MDL dies. The first die processing steps, namely the InP waveguide etching for both PD and MDL and the detector mesa and the laser microdisk etching, are performed in series. That is, the processing on the PD die is performed by keeping the MDL die covered by protective thick photoresist (AZ 4533) in the COBRA clean room, and vice versa for the laser die processing in the clean room of Ghent University. The chip planarization and passivation are done in parallel for the two dies with BCB, as well as the bottom n-contact window opening. As the microdisk lasers and detectors have different metallization for p-contacts, the top p-contact window opening and metal evaporation steps are done again in series, i.e. on each die while keeping the other protected by thick PR. For the common processing steps, it is important to have a chip surface topology as uniform as possible. This is the reason why PD and MDL structures use a similar layer stack thickness, roughly $1\,\mu\text{m}$ for both sources and receivers. This is a trade off between ease of the fabrication and device performance, as it sets some limits in the device design. For instance, a thicker detector structure would result in a higher device efficiency, as explained in Chapter 2, but would lead to a more irregular chip surface topology, making the chip planarization and passivation steps more complicated. Further details on the joint work on the photonic link on SOI can be found in [76].
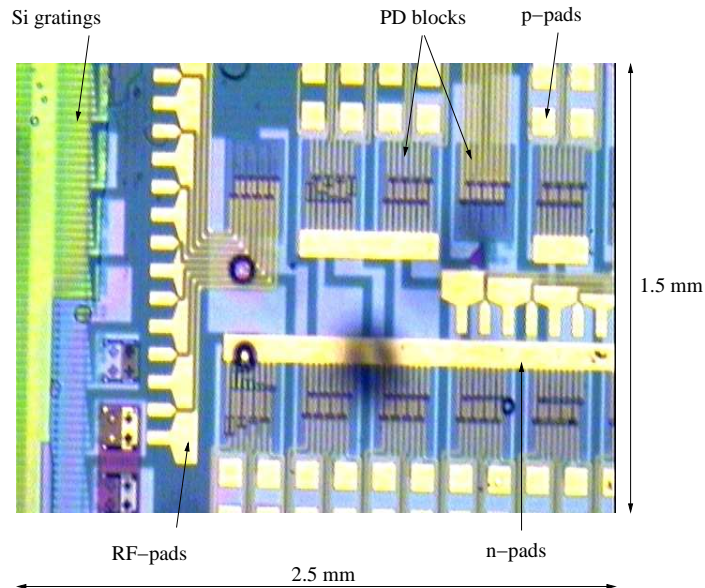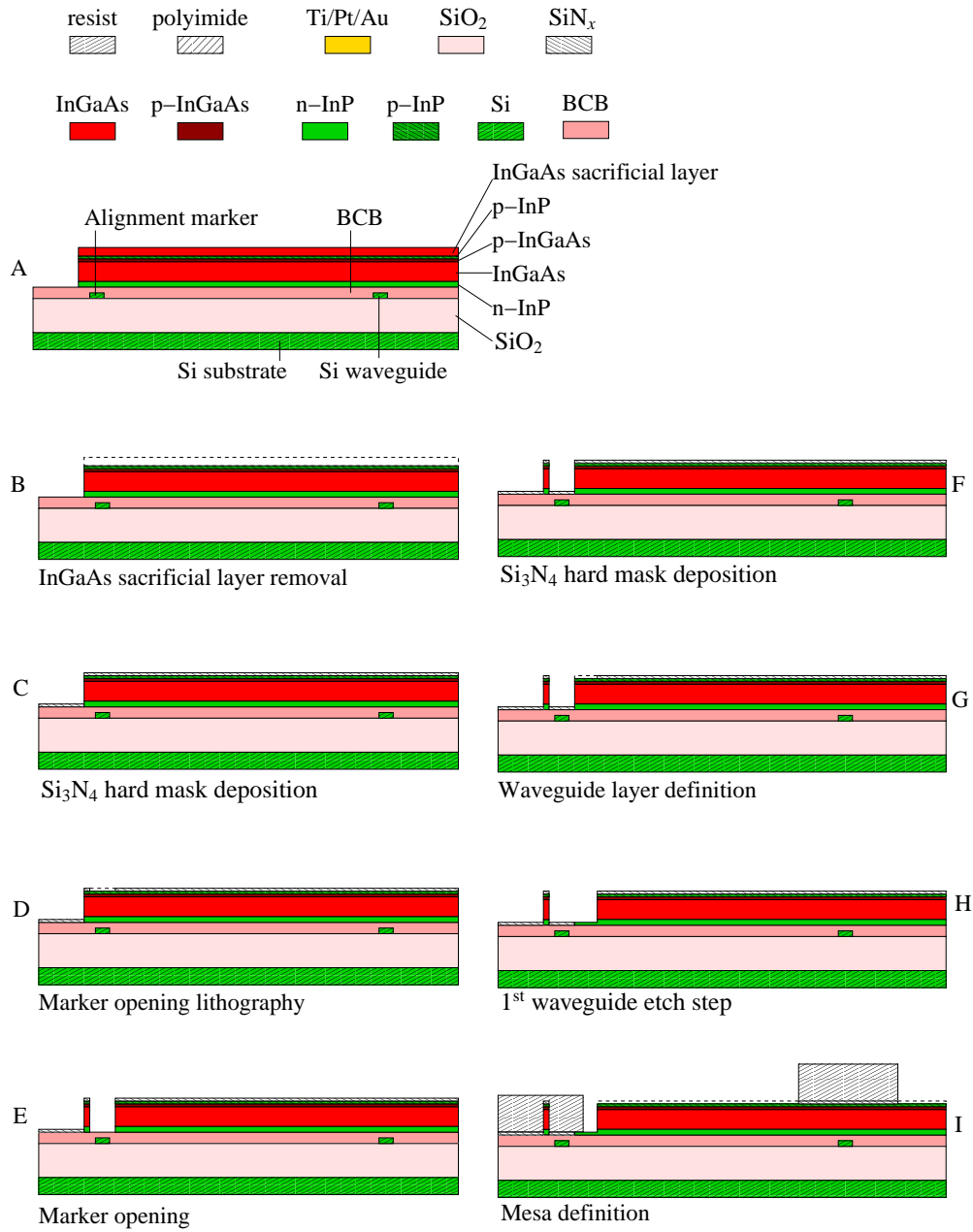
Figure 3.21: Left: picture of the fabricated chip taken with optical microscope. Ten PD blocks (8 devices/block) are shown in this picture. DC and RF p-contact and n-contact pads are also visible, as well as the Si grating couplers (on the very left). Right: Close-up of one PD structure. The metal fingers on top of the central mesa and lateral n-contact windows are visible.

3.3.3   Heterogeneous multiwavelength receivers

In the realization of the heterogeneously integrated MWRs, the InP-based detectors are BCB-bonded on the SOI processed wafer. This requires a few important changes in the detector process flow, which is shown in Fig. 3.22, as compared to the case of SiO_2-bonded PDs. In this section, the changes applied to the detector process flow are described. InP-based dies cleaved out of a 2" wafer containing the detector layer stack are processed on Si samples, where the receiver demultiplexers and access waveguides have been defined. Following successful experiments on optical waveguide alignment, in these samples the PD InP membrane waveguides are defined by 405 nm UV optical lithography, which is cheaper and faster than EBL. The photonic die processing has to be adapted to be able to handle the different bonding layer material. In the following, the processing steps are briefly listed, while the major changes with respect to the processing of PDs molecular bonded on SOI are emphasized:

Sacrificial layer removal The InGaAs sacrificial layer on top of the bonded InP-based stack was left for protection in the dies used for the MWR processing. In this first step, this sacrificial layer is wet-chemically removed with an $H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 10$ solution, selective to InP. This is shown in Fig. 3.22 (A, B).

resist   polyimide   Ti/Pt/Au SiO_2 SiN_x

InGaAs   p–InGaAs   n–InP   p–InP   Si   BCB

A

Alignment marker   BCB   InGaAs sacrificial layer   p–InP   p–InGaAs   InGaAs   n–InP SiO_2

Si substrate   Si waveguide

B   InGaAs sacrificial layer removal

C Si_3N_4 hard mask deposition

D   Marker opening lithography

E   Marker opening

F Si_3N_4 hard mask deposition

G   Waveguide layer definition

H   1st waveguide etch step

I   Mesa definition

resist   polyimide   Ti/Pt/Au   SiO$_2$ SiN$_x$

InGaAs   p–InGaAs   n–InP   p–InP   Si   BCB

J

2nd waveguide etch step

O

Side contact opening

K

Si$_3$N$_4$ hard mask removal

P

Metallization

L

Mesa etching

M

Chip planarization
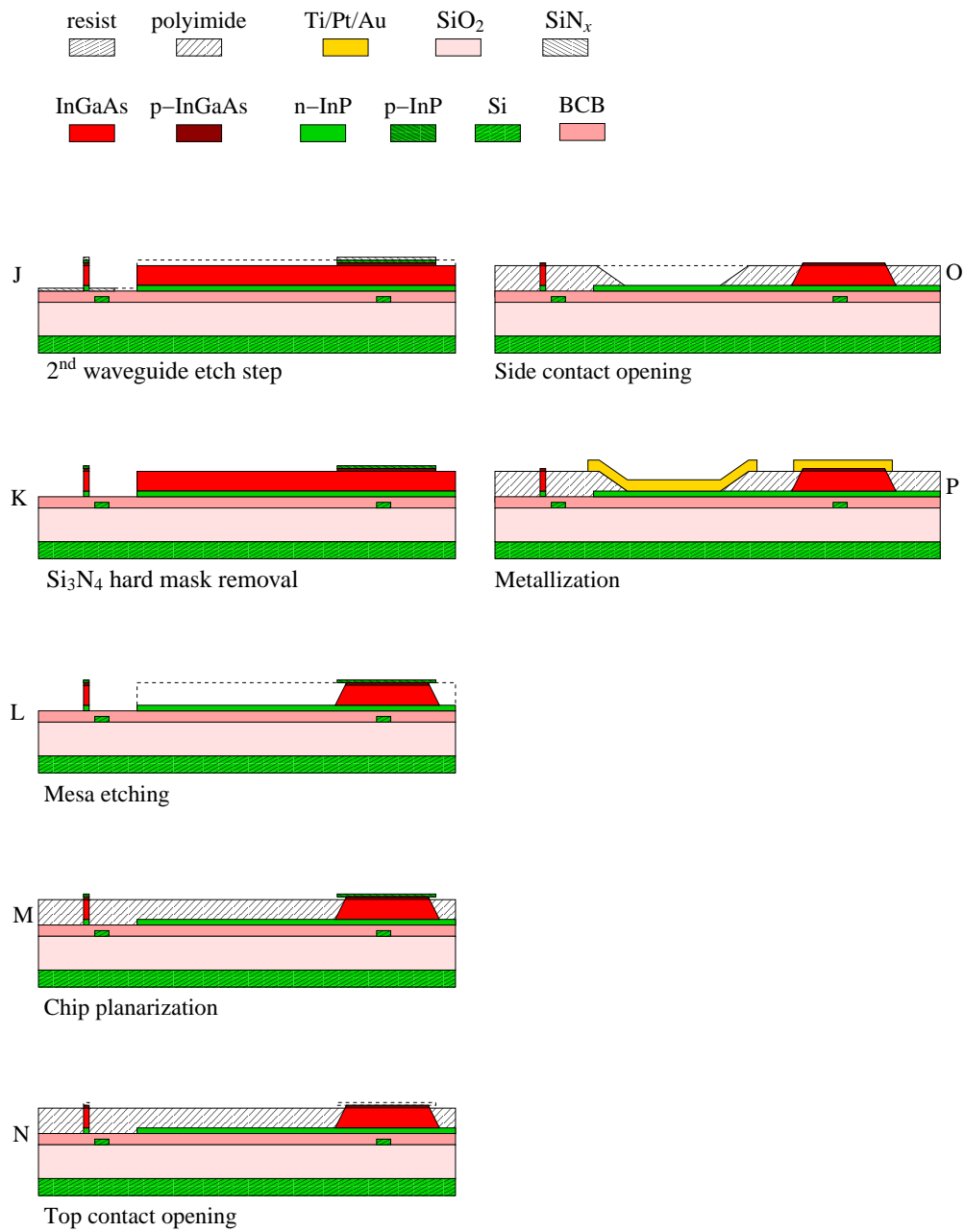
N

Top contact opening

Figure 3.22: Process flow of InP detectors BCB-bonded on SOI.

Marker opening For the MWR processing, 405 nm UV optical lithography is used for the InP waveguide alignment to the processed Si passive circuitry on the SOI substrate. To achieve an accurate alignment, some of the alignment markers in the SOI interconnect waveguide layer need to be used. Such markers are initially not visible, as hidden by the InP die; therefore a first optical lithography step has to be performed to define the etching windows around the markers that need to be opened. This is shown in Fig. 3.22 (C, D). A 50 nm thick layer of Si_3N_4 is first deposited by PECVD and the pattern of the etching windows is transferred to the hard mask by optical lithography and SiN-RIE. The windows are then etched by InP-RIE through the whole InP-based stack, using the patterned Si_3N_4 as a mask, as shown in Fig. 3.22 (E). Despite the presence of oxygen cycles in the InP-RIE, which does attack polymers like BCB, this RIE step is not critical: applying an aggressive over-etch would indeed result in the removal of the BCB on top of the alignment marker structures, which are defined in Si and therefore are selective to the InP-RIE process. This would bring to exposed alignment markers that would be anyway usable for the following critical waveguide alignment.

Detector waveguide layer definition For the waveguide lithography, the hard mask for the previous marker etching is removed with a SiN-RIE and a new layer of Si_3N_4 is deposited by PECVD (Fig. 3.22, F). The BCB etched during the SiN-RIE is not an issue for the chip process, for the same reason explained above. Now, the waveguide structures can accurately be aligned by optical lithography using the previously opened markers (Fig. 3.22, G).

Waveguide etching As for the PDs molecular bonded on SOI, the detector InP waveguide pattern is etched in two steps, in order to protect the bonding layer during the top hard mask removal (Fig. 3.22, H).

SiO_2 hard mask removal The hard mask is removed with a SiN-RIE step, while keeping the PD mesas protected by PR patterned by 405 nm UV optical lithography (Fig. 3.22, I).

PD mesa definition The PR covering the PD mesas is removed by anisotropic dry-etching, using a $O_2 : CHF_3 = 20 : 2$ sccm gas mixture at a plasma RF power of 100 W in our SiN-RIE machine. Oxygen-stripping is avoided for PR removal, as it would isotropically etch the BCB as well, therefore damaging the bonding layer. The exposed Si_3N_4 layer is used to mask the complete InP-RIE (Fig. 3.22, J).

Mesa etching The Si_3N_4 hard mask is removed by SiN-RIE, as shown in Fig. 3.22 (K), and the PD mesas are wet-etched with a $H_2SO_4 : H_2O_2 : H_2O = 1 : 1 : 10$ solution (Fig. 3.22, L).

The chip planarization and passivation with polyimide as well as the contact window definition and metallization steps are shown in Fig. 3.22 (M-P) and do not differ from the process flow followed for the PDs molecular bonded on SOI.

3.4   Conclusions

In this chapter, the fabrication process developed for the realization of the detector and multi-wavelength receiver chips has been described. Such integrated components are based on an InP-on-Si heterogeneous technology, in which the Si-based passive circuitry is patterned on an SOI wafer or on a CMOS wafer, on top of which an InP layer stack is bonded upside down and processed to realize the InP-based active devices. With this approach, a number of chips were successfully fabricated, namely InP-based PDs molecular bonded on SOI and on CMOS wafers on top of which Si and Si_3N_4 interconnect waveguides are defined, InP-based PDs integrated with MDLs molecular bonded on SOI for the realization of a full point-to-point optical link on Si and the on-going work on heterogeneously integrated MWRs, built of InP-based detectors processed on an InP die BCB-bonded upside down on the SOI wafer, on top of which the receiver passive circuitry is defined, i.e. receiver waveguides and demultiplexer. The processing steps performed to manufacture those chips have been presented and discussed in detail in this chapter.

Chapter 4

InP-based Photodetectors on Si

This chapter discusses the realization of the photodetector (PD) structures in InP-on-Si technology: PDs bonded on Si and on Si_3N_4 waveguides via molecular bonding and the realization of a full laser-to-detector optical link on Si.

4.1 Introduction

In the previous chapters, the benefits of optical interconnections (OIs) on electronic integrated circuits (ICs) and the potential of indium phosphide (InP) based active devices, namely sources, modulators, receivers, for that application have been discussed. The design of an InP-membrane based photodetector structure for use in OIs has been presented in Chapter 2 and in the previous chapter the fabrication technology developed to heterogeneously integrate the InP-based detectors with the Si-based circuitry on a silicon-on-insulator (SOI) or on a complementary metal-oxide semiconductor (CMOS) wafer has been described.

This chapter focuses on the chips fabricated with such technology, containing PDs molecular bonded on Si and on Si_3N_4 waveguides on SOI and CMOS wafers, respectively. In particular, the devices fabricated on the following chips are presented in this chapter:

InP-based membrane couplers bonded on SOI This chip contains InP-membrane waveguides processed on an InP-based layer stack flip-chip molecular bonded on an SOI wafer on top of which Si interconnect waveguides are patterned. These structures are part of the PDs developed in this work and are used to enhance the optical coupling from the photonic waveguide underneath the bonding layer to the PD. The purpose of this chip is to obtain experimental feedback on the membrane coupler structure and test its efficiency.

InP-based photodetectors (PDs) bonded on SOI These PD structures are processed in an InP-based epitaxial stack bonded upside down on an SOI wafer containing a Si interconnect waveguide layer on top. The detector structure used for the applications mentioned

above consists of two parts, as shown in Fig. 2.2: an InP membrane input waveguide on top of the bonding layer, meant to provide a good optical coupling from the photonic waveguide layer to the PD, and a p-i-n junction, where the optical power is absorbed and converted into an electrical signal. On the SOI wafer, silicon fiber grating coupler (FGC) structures are also integrated in the photonic waveguide layer, as indicated in Fig. 3.21, in order to allow for on-wafer device characterization.

Photonic link on SOI This chip contains point-to-point laser-to-detector optical links on Si. The active components are based on InP and are realized with the PDs developed in this thesis framework and the microdisk lasers developed by Van Campenhout [75], while the passive components consist of Si photonic waveguides that provide the interconnection between sources and receivers.

InP-based PDs bonded on CMOS These detectors are bonded on Si_3N_4 waveguides defined on top of a CMOS wafer. In this case, the PD structure is built as a p-i-n heterojunction aligned over the interconnect waveguide underneath the bonding layer, without any input membrane coupler, which requires a more complicated processing due to the choice of Si_3N_4 as interconnect waveguide core material, as explained in Chapter 2. For this chip, the PD characterization is performed by using a fiber-to-waveguide butt-coupling approach.

In the next sections, the design, fabrication and characterization of the Si and Si_3N_4 passive components, the membrane InP couplers and the PD structures implemented in the chips mentioned above are described.

4.2   Si and Si_3N_4 components

The passive circuitry patterned in the interconnection layer of the chips used for the fabrication of the photodetectors implements basic functions. It consists of Si or Si_3N_4 waveguide structures meant to carry the optical signal from a laser source (integrated on the same chip or external) to the PD structure, as described in detail in Section 2.2. To test the detectors, an external laser source is used. The fiber-to-chip light coupling is realized in two different ways, when working with Si_3N_4 waveguides on CMOS and with Si waveguides in SOI. In the first case, the optical power is launched into the chip through an optical lensed fiber focussed to the waveguide. In the second case, Si fiber grating couplers integrated on the chip are employed to allow for on-wafer characterization of the detectors, without the need of any additional processing step to create chip facets for fiber-to-waveguide edge coupling. The FGC structures are defined by 193 nm Deep Ultra-Violet (DUV) lithography and are shallowly etched in the Si waveguide layer. The grating element width and pitch are 325 nm and 615 nm, respectively, while the number of elements is 25. With this geometry, the grating footprint is about $12 \times 15\,\mu m^2$. Fig. 4.1 shows SEM pictures of a few fabricated Si gratings and waveguides. An extensive description of the FGC design, fabrication and characterization can be found in [77].
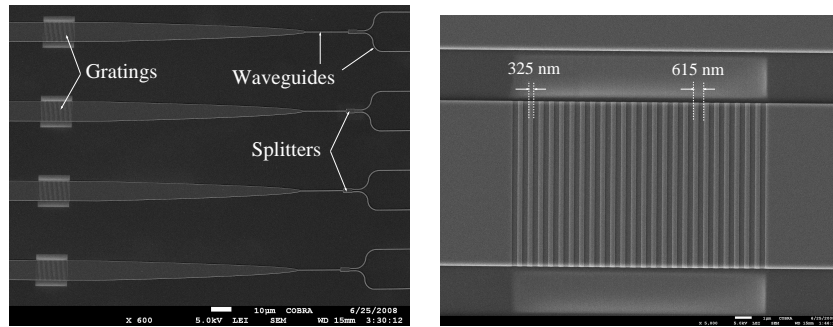
Figure 4.1: Left: SEM pictures of Si waveguide structures and gratings patterned in the Si photonic interconnection layer. Right: Zoom on a grating, shallowly etched in the Si waveguide layer.

4.3 Membrane InP couplers

In this section, the mask design, fabrication and characterization of the full-passive chip containing the InP-membrane couplers bonded on Si waveguides are described. The InP structures are processed on an InP-based layer stack molecular bonded on an SOI wafer on top of which the Si photonic waveguides are patterned. These couplers are part of the PD structure developed in this work, as shown in Fig. 2.2, and are used to enhance the optical coupling from the photonic waveguide underneath the bonding layer to the PD. For the ease of the processing, the InP membrane input waveguides are implemented only in the mask set for the realization of the detectors bonded on Si photonic waveguides on SOI and not of the PDs bonded on Si_3N_4 waveguides on CMOS, as discussed in Chapter 2.

4.3.1 Coupler realization

Commercially available 2D and 3D mode solvers and Matlab are used for the membrane coupler modeling, which is described in detail in Section 2.3.1. In this section, the mask design and the processing for the realization of the all-passive chip containing Si-to-InP membrane coupler structures are discussed.

Mask design

The InP passive couplers are processed on an InP-based layer stack bonded on an SOI wafer on which the Si photonic wiring layer has been previously defined. The layout of the manufactured Si-to-InP coupler structures is schematically drawn in Fig. 4.2, while Fig. 4.3 shows a close-up of the layout of the structures as implemented in the mask set: the optical input signal is split into two branches by means of a multi-mode interference (MMI) 3 dB splitter, in which the two output branches are 20 μm spaced to allow for transmission measurements through the two arms with microscope objectives for light coupling. The test arm is interrupted and the
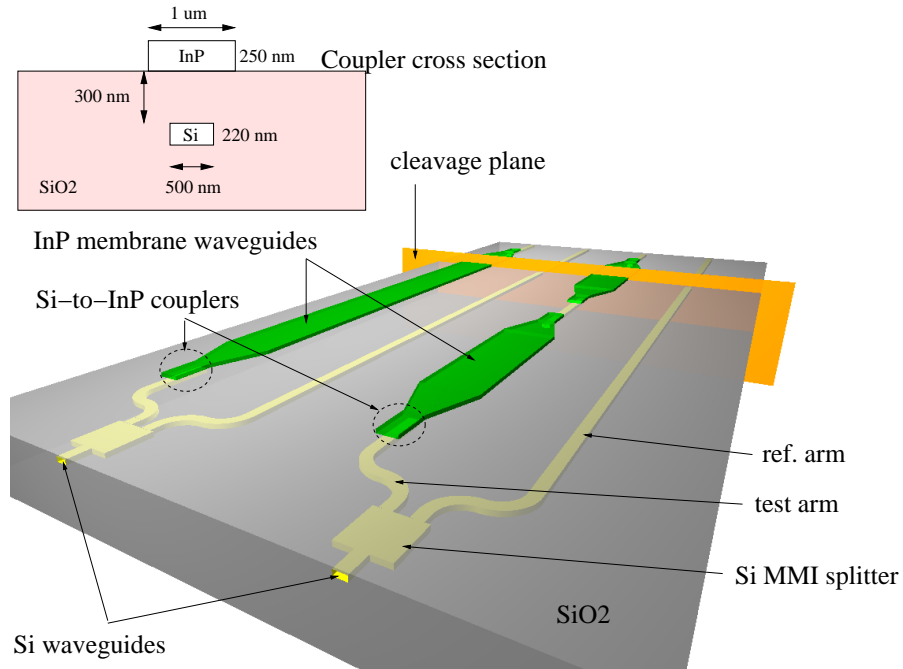
1 um

InP 250 nm Coupler cross section

300 nm

Si 220 nm

SiO2 500 nm

cleavage plane

InP membrane waveguides

Si−to−InP couplers

ref. arm

test arm

Si MMI splitter

SiO2

Si waveguides

Figure 4.2: The passive chip was cleaved after a short distance from the beginning of the membrane couplers. The left structure has one Si-to-InP straight coupler in the test arm and the InP membrane waveguide is 140 μm long. The right structure has three Si-to-InP straight couplers and the InP membrane waveguide is 80 μm long.
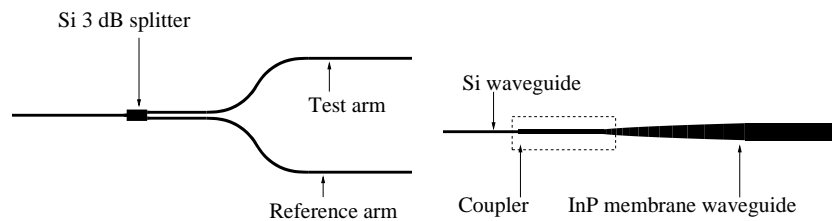
Si 3 dB splitter

Test arm

Reference arm

Si waveguide

Coupler   InP membrane waveguide

Figure 4.3: Close-up on components as drawn in the mask: on the left, a 3 dB MMI structure that splits the incoming optical signal into the top test arm and the lower reference arm is indicated. On the right, the Si-to-InP coupling section is shown.

Layer	Target thickness	Measured thickness	Deviation
InP membrane layer	250 nm	232 ± 5 nm	$-7 \pm 2\%$
SiO$_2$ bonding layer	300 nm	295 ± 3 nm	$-2 \pm 1\%$

Table 4.1: Layer thicknesses measured with the Tencor alpha-step profilometer.

InP structures are fabricated over the gaps (see Fig. 4.2): the coupling to and from the optical wiring layer is measured and compared to the reference signal propagating in the lower branch. The following types of couplers are implemented in the mask:

Straight couplers These structures are built as InP waveguides aligned over the Si waveguides with an overlapping region as long as the predicted optimum coupling length. Variations in key parameters, namely the coupler width, length and lateral offset, are implemented to compensate possible misalignments during the device pattern definition.

Tapered couplers These structures are built as InP waveguides, laterally tapered in order to increase the lateral alignment tolerance. The taper angle, and hence the taper length, varies for different structures, thus varying the actual coupling region length.

Slanted couplers These structures are straight InP waveguides that lay over the Si waveguides and are tilted by a small angle (a few degrees). By varying that angle, the effective coupling region surface varies. Slanted waveguides with a different tilt are therefore implemented in the mask. The advantage of these structures is that they are basically insensitive to the lateral waveguide misalignment, even though they require a longer overlap region, which leads to larger device dimensions.

Moreover, test structures are implemented in the mask design to test waveguide losses. Those structures are curved InP waveguides, with varying bending radius, coupled to the Si waveguides by means of the couping structures listed above.

Device fabrication

The InP couplers are processed on a 2" InP wafer grown with the detector layer stack shown in Fig. 2.11 bonded on the SOI wafer containing the Si waveguide pattern. After bonding, the InP substrate and the InGaAs etch-stop layer are removed by a combination of CMP and wet-etching steps. The bonded wafer is finally diced in six pieces of $1.8 \times 2.7 \, cm^2$ to allow for processing in the COBRA clean room. Dry-etching and selective wet-etching processing steps and a Tencor profilometer were used to measure the wafer layer thicknesses. The results are shown in Table 4.1. The InP membrane layer thickness was found to be off-spec by $-7 \pm 2\%$, which leads to an expected coupling efficiency of $45 \pm 20\%$, as it can be read from Fig. 2.7. The SiO$_2$ bonding layer thickness was measured to be 295 ± 3 nm, but simulations show that this deviation from the 300 nm spec value has a negligible impact on the coupling efficiency (see Fig. 2.6).
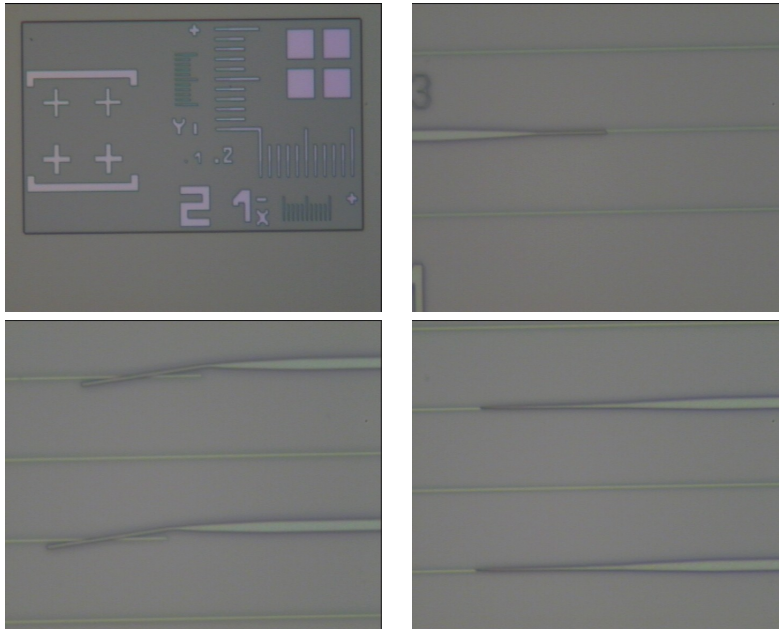
Figure 4.4: Photograph of fabricated straight (top right), slanted (bottom left) and laterally tapered (bottom right) membrane couplers taken with optical microscope. The Si waveguides underneath the bonding layer are also visible. The top right picture shows alignment markers opened with RIE in the Si waveguide layer.

A mask set consisting of 2 masks is used to fabricate the devices. The first mask is used to define etching-windows around the alignment markers in the Si layer, underneath the InP-based bonded wafer. The mask alignment is performed by using markers that are outside the bonded area, which are visible through the 300 nm silica bonding layer. An InP-RIE step follows, to etch those windows through the detector layer stack and open the alignment markers, used in the further lithography steps. The second mask is then used to define the coupler pattern on top of the interconnect layer. Considering that the waveguide alignment is performed by 405 nm UV optical lithography, this is the most critical step due to the small waveguide dimensions and the height difference between the waveguide layers. After waveguide lithography, the couplers are fabricated by using a combination of wet and dry etching processing steps. In particular, InP-RIE is used to etch the waveguides through the InP-based layer stack, while selective HCl-based and H_2SO_4-based wet-etch solutions are used to remove sacrificial layers. The samples are finally sawn to create input and output facets for fiber-coupling to the waveguides. Fig. 4.4 shows photographs taken with an optical microscope of the alignment markers opened with the first RIE step (top left) and of the fabricated Si-to-InP straight (top right), slanted (bottom left) and laterally tapered (bottom right) membrane couplers. After the coupling section, the InP waveguide is tapered out to 3 μm to reduce the propagation losses.
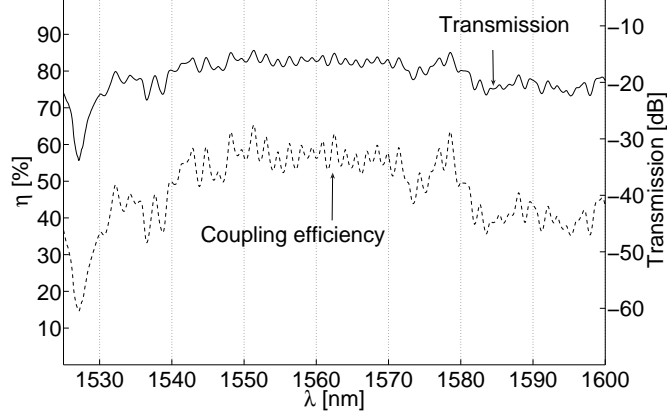
Figure 4.5: Experimental results for the Si-to-InP couplers. The transmission curve represents the measured data, while the coupling efficiency was calculated by using Eq. 4.1.

4.3.2 Measurement results

The characterization of the Si-to-InP couplers is performed by focusing a Transverse Electric (TE) polarized optical signal in the Si waveguide with a microscope objective. The 2 mm long chip contains structures with one coupler and a 1.4 mm long InP waveguide and structures with three couplers and two membrane straight waveguide sections with a total length of 0.8 mm (see "cleavage plane" indicated in Fig. 4.2). The output power P_{test} collected from the InP waveguide in the test arm is normalized to the power P_{arm} measured out of the reference arm: the transmission parameter can be expressed by

$$\frac{P_{\text{test}}}{P_{\text{arm}}} [\text{dB}] = \eta \cdot N - \alpha \cdot L \tag{4.1}$$

where η is the membrane coupler efficiency in dB, N is the number of Si/InP couplers of the measured structure, α is the waveguide propagation loss in dB per unit length and L is the waveguide length. To estimate the efficiency of the membrane couplers, devices with a total InP waveguide length of 1.4 and 0.8 mm were measured and Eq. 4.1 was used for extracting the results, shown in Fig. 4.5. Considering a measurement error margin of ± 0.5 dB over the whole spectrum, which accounts for the objective-waveguide alignment for input and output light-coupling and reflections at the objective-facet interface, a coupling efficiency of $50 \pm 6\%$ is achieved for TE-polarized light in the wavelength range between 1540 and 1570 nm [78]. Residual ripples are due to Fabry-Pérot reflections in the measurement set-up. Taking into account the growth of the thinner InP membrane layer, as mentioned in Section 4.3.1, the device performance is in good agreement with the simulations. The measured InP membrane waveguide propagation loss is very high, over 100 dB/cm in the monitored wavelength range,

as shown in Fig. 4.5. That made the characterization of other types of coupling structures (i.e. slanted couplers and intentionally misaligned couplers) not feasible.

4.4 Photodetectors

4.4.1 Device design

The detector layer stack is grown as a 700 nm n.i.d. InGaAs absorption layer sandwiched by a highly p-doped 50 nm thick InGaAs contact layer and a highly n-doped 200/250 nm thick InP layer, for bonding on Si_3N_4 or Si waveguides, respectively, and the mesa footprint is $5 \times 10 \, \mu m^2$. As explained in Section 2.3, this geometry is a trade-off between device efficiency and speed. According to the simulation results, the expected PD internal quantum efficiency is ~80%, limited by the loss of optical power in the metal layers, while the expected 3 dB bandwidth is around 30 GHz, limited by the transit-time of the carriers in the diode depletion region.

4.4.2 Fabrication

The InP-based detectors are processed on a 2" wafer grown with the PD layer stack shown in Fig. 2.11. The wafer is diced in $9 \times 4.5 \, mm^2$ pieces, which are then molecular-bonded upside down on an SOI wafer, in which the Si waveguide pattern has been defined. After bonding, the InP die substrate and the InGaAs etch-stop layer were removed by a combination of Chemical-Mechanical Polishing (CMP), HCl-based and H_2SO_4-based solutions, respectively. Afterwards, the SOI wafer was sawn into samples, each hosting a photonic die, which were processed as described in Section 3.3. Fig. 3.21 shows an optical microscope picture of the fabricated chip. As can be observed in the close-up shown in Fig. 3.20 (right), the signal metal-finger does not completely cover the PD mesa as in the glass metal-mask. This is due to the lithography step performed to define the metallization pattern: the tip of the metal fingers is more exposed to the radiation of the optical mask aligner Ultra-Violet (UV) lamp, as compared to the rest of the metal finger structures. That results in an over-exposure of the negative photoresist used for that lithography in the area of the metal finger tip. Measurement results show that the partial coverage of the detector mesa was not catastrophic for the devices, as described in the next section. However, the problem was faced for the following chip run by changing the metallization pattern design and the corresponding lithography recipe, as described in Section 4.4.4.

4.4.3 Static measurements

The detector electrical characterization is performed by using a Keithley 2400 source-meter unit to bias the device and read out the dark current. Measurement results are shown in Fig. 4.6, which shows the diode I-V characteristic in reverse and forward bias working regimes. Values around 1.6 nA were registered at -4 V.
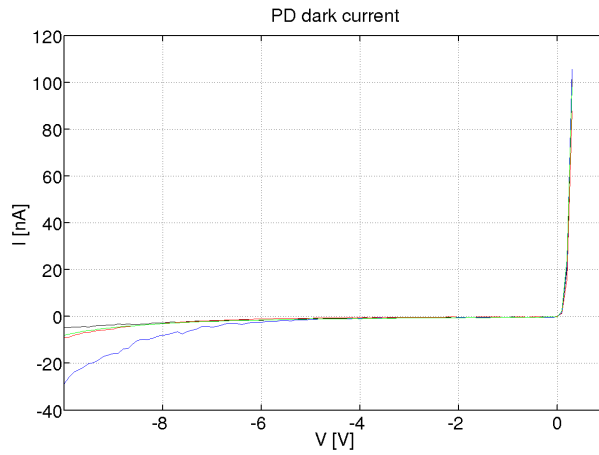
Figure 4.6: Diode I-V characteristic in reverse and forward bias working regimes measured in the darkness. Dark current values around 1.6 nA were registered at -4 V.
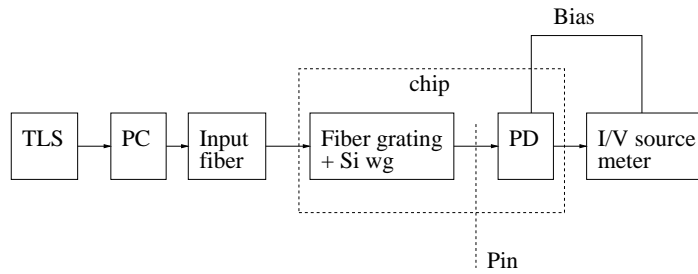

Figure 4.7: PD measurement setup. The optical signal generated by the tunable laser (TLS) is filtered by the polarization controller (PC). TE-polarized light is launched into the input optical fiber aligned over the Si grating couplers. Thus, the optical signal is coupled into the Si waveguide (Si wg) and illuminates the PD structure with an optical power P_{in}. The rightmost block is a Keithley unit used for biasing the diodes and reading the generated photocurrent.
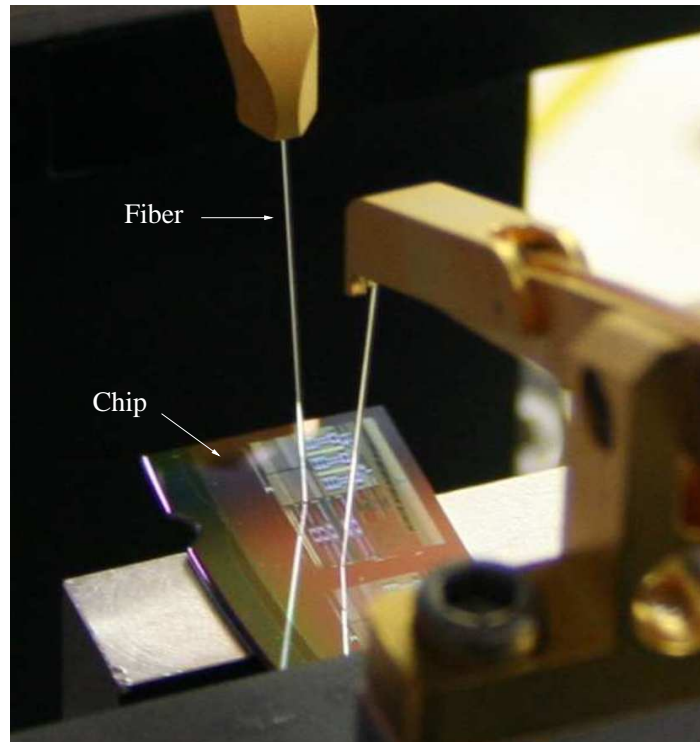
Figure 4.8: Close-up of the measurement setup. The chip lies on a vacuum chuck. Two
tilted optical SMFs aligned over the Si gratings are shown in the picture. The tilt angle is
about 10°. The fiber-grating alignment is done with the help of a microscope placed under
an angle of about 30°. Probing needles are not shown in this photograph, for clarity.

As shown schematically in Fig. 4.7, the optical direct current (DC) characterization is
performed by using an external HP8168A tunable laser source (TLS) and a Keithley source-
meter unit to read out the PD generated photocurrent. A polarization controller (PC) is used
to filter the optical signal at the output of the TLS. Thus, TE-polarized light is launched into
the single mode fiber (SMF) aligned over the Si grating couplers, as shown in Fig. 4.8. The
optical signal is coupled into the Si waveguides and guided towards the detectors. The detector
generated photocurrent as a function of the applied bias voltage was measured for the following
TLS output powers: 0 mW, 0.2 mW and 0.4 mW. To evaluate the detector efficiency, the
following factors are considered. Firstly, the fiber connections from the TLS to the PC and
to the coupling input fiber causes a loss of 0.7 dB. Secondly, the Si gratings fabricated on
this wafer have an optimum coupling efficiency at $\lambda = 1575$ nm of about 20%. Lastly, Si
waveguide measured losses are 4-5 dB/cm, for TE-polarized light [59]. That leads to a loss
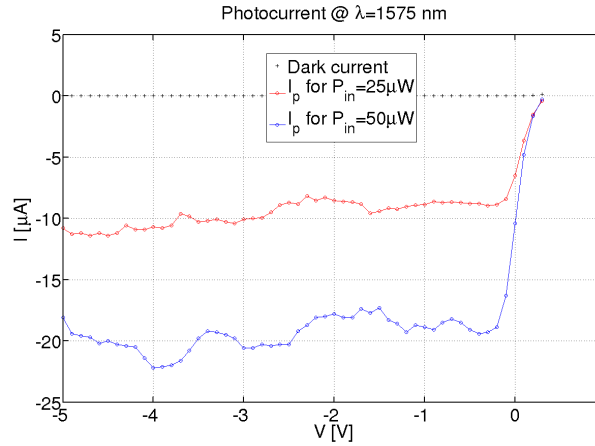of 1.3 dB along the full Si waveguide length (~3.2 mm), from the grating coupler to the PD

Figure 4.9: Measured photocurrent for 0 µW, 25 µW and 50 µW optical input power as a function of the detector applied bias voltage.

input. Taking those loss sources into account, the detector optical input powers corresponding to the TLS intensities mentioned above are $P_{in} = 0$ µW, $P_{in} = 25$ µW and $P_{in} = 50$ µW. The responsivity of the PD structure is thus calculated to be $R = 0.45$ A/W at $\lambda = 1575$ nm, which is a conservative value, as the grating's maximum coupling efficiency is assumed. The quantum efficiency, defined as the ratio between the number of electron-hole pairs generated and the number of incoming photons, can be written as a function of the responsivity in the following way:

$$\eta = \frac{I_p/q}{P_0/h\nu} = R \cdot \frac{h\nu}{q}$$

where I_p is the detector generated photocurrent, P_0 the optical input power, q the electron charge and $h\nu$ the photon energy. Therefore, the measured responsivity $R = 0.45$ A/W corresponds to a quantum efficiency $\eta = 35\%$, which includes the efficiency of the InP membrane coupler and the internal quantum efficiency of the pin-detector itself. Measurement results are shown in Fig. 4.9, which also demonstrates the linear behavior of the PD response to the incoming input power.

4.4.4 Dynamic measurements

The RC characteristic at radio frequency (RF) of the detector electrical equivalent circuit was investigated by measuring the output port reflection parameter with an Agilent HP8703A 20 GHz Lightwave Component Analyzer (LCA), using the set-up shown in Fig. 4.10. A 50 GHz RF probe and a 65 GHz bias-T was used to perform the RF measurements throughout the LCA and provide at the same time a DC reversed bias to the devices by means of a Keithley source/voltage-meter. Measurement results are shown in Fig. 4.11 (right), where the
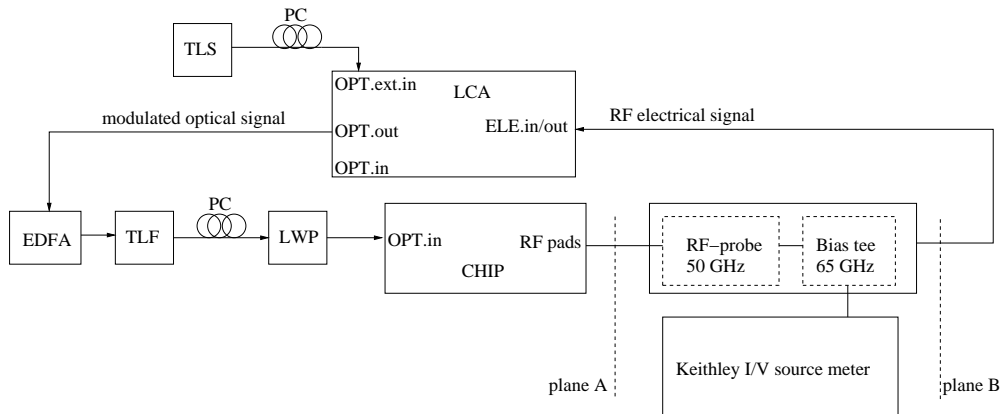
Figure 4.10: Schematics of the set-up for measurements of RF transmission/reflection *S* parameters performed with the LCA. The port labeled "ELE.in/out" is also used to launch an electrical RF signal towards the device and register the reflection parameter S_{22} to investigate the detector RC characteristic at RF frequencies.
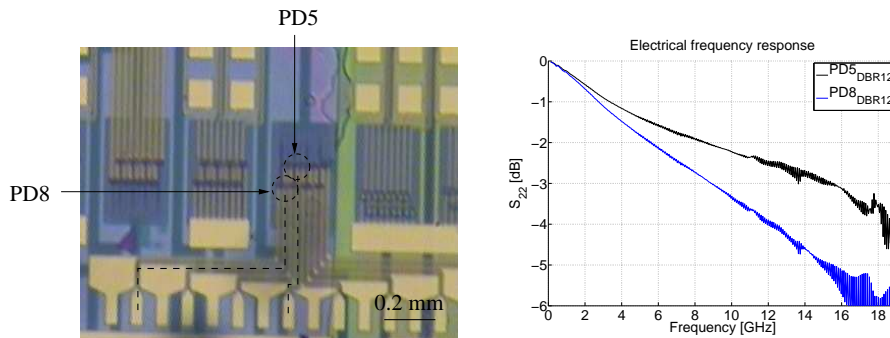

Figure 4.11: Detector electrical RF frequency response: S_{22} output port reflection parameter. Left: Picture of a "block" of photodetectors contacted with RF pads on chip. PDs in the central part of the block are connected via the shortest transmission line to the pads (PD5), while outer devices make use of a longer transmission line (PD8). The metal path through the transmission lines for the central the outer devices is indicated with dashed lines. Right: The upper bold line corresponds to PD5, with the shortest RF coplanar metal line: the 3-dB cut-off point is at 15 GHz. The lower line corresponds to PD8, with the longest RF coplanar metal line: the 3-dB cut-off point is at 9 GHz.

typical electrical frequency response curves of the fabricated detectors are traced. The two curves correspond to devices with the shortest (around 0.9 mm long) and the longest (around 1.4 mm long) metal transmission lines used for connecting the PD contacts to the RF probing pads, as shown in Fig. 4.11 (left). The influence of the metal transmission line on the device RF performance is obvious, when comparing the two curves. The transmission line is designed as a Ground-Signal-Ground (GSG) coplanar waveguide (CPW), impedance-matched to 50 Ω in order to minimize power reflection in the RF measurement path. As indicated in Fig. 4.10, this path goes from the device through the integrated transmission line and external RF probe, bias-T and RF cable to the LCA electrical RF port, which are components all matched to 50 Ω. However, the chip metal layer is defined on top of the etched-back polyimide (PI) PI 2723, as explained in Section 4.4.2, which is approximately 700 nm thick. According to simulations, the microwave field propagating through the transmission line extends for a few microns in the substrate and is partially absorbed in the Si waveguide and substrate layers. These simulations were performed with MOLCAR[1], which is a 2D mode solver developed by [79, 80] that uses the method of lines (MOL) to calculate the electromagnetic field guided by the structure at microwave frequencies. The MOL is a semi-analytic method, which analyzes the 2D input structure in two different ways along the vertical and the horizontal directions. In the direction perpendicular to the layer stack, a full analytical solution is computed for the Maxwell differential equations. In the horizontal direction, a numerical solution is calculated, based on a FD method [79, 80].

To improve the detector RF performance, a different metallization scheme is implemented in the following chip run, as described below.

Improved RF metallization

In order to optimize the detector RF metallization, further MOLCAR simulations were performed to investigate the benefits that an electro-plated RF metal pattern would provide. By electro-plating the metal pattern on the chip, the metal thickness would increase to about 1.5 μm, providing less resistance and more confinement for the electrical signal in the transmission line, which translates into lower losses at RF frequencies. Clearly, a drawback of this option is given by the extra processing steps required for plating. To figure out whether those extra processing steps would be worthwhile, simulations were performed to investigate the RF electrical signal propagation through the CPW transmission line as a function of the CPW geometry. Fig. 4.12 shows the structure analyzed with MOLCAR. The metal layer consists of three parts: a 350 nm thick layer, evaporated and patterned by lift-off, 400 nm of evaporated seed layer, and the top plated layer, whose thickness is used as a variable parameter in the simulations. Thus, the microwave complex effective index of the RF electrical field propagating in the CPW structure was computed and Fig. 4.13 and Fig. 4.14 show the simulation results. The first calculation point is for a metal thickness of 350 nm, corresponding to the thickness of the metal evaporated and patterned by lift-off. The other calculation points simulate the plated CPW and start from 750 nm, as the 400 nm thick seed layer has to be taken into account. Normally, the total thickness of the plated metal is around 1.5 μm and that is

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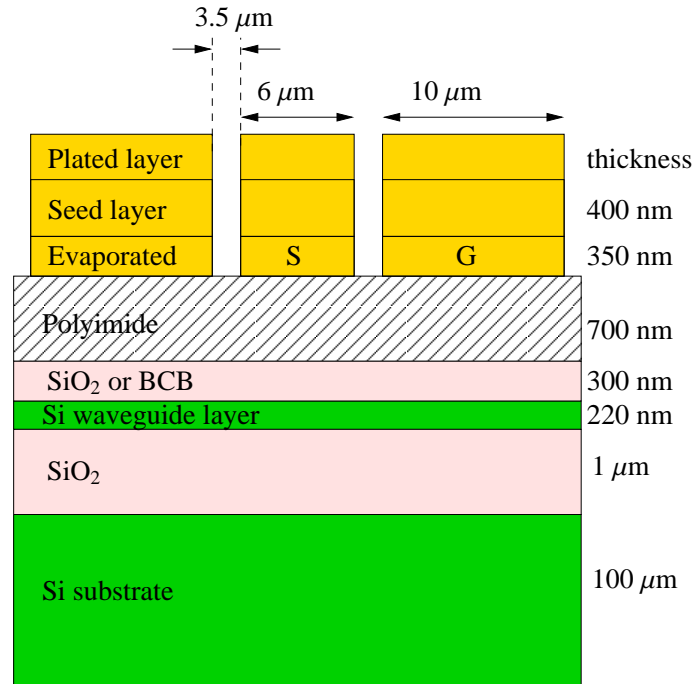[1]MOLCAR : Method of Lines Complex Arithmetic Routine

Figure 4.12: Schematic of the structure simulated with the MOL. The indentation in the metal layer was intentionally designed to simulate the real shape that the CPW cross-section would have, if plated.

the reason why the simulations were performed in a 0-2 μm window. The simulation results in Fig. 4.13 and Fig. 4.14 show the dependence of the real part of the microwave effective index and of the RF loss on both the operating frequency and the metal layer thickness. The loss dependence on the operating frequency is due to the skin-effect resistance R_{AC} and the finite conductivity of the metal. The skin-effect is the tendency of an alternate current (AC) to distribute next to the conductor surface rather than in the conductor core and the associated skin-depth is the depth the AC-current lines penetrate in the substrate. The skin-depth is proportional to $1/\sqrt{f}$, where f is the operating frequency, and that causes R_{AC} to increase as fast as $\sqrt{f}$ [81]. Therefore, the higher the operating frequency, the higher the microwave loss. When the frequency increases, the skin-effect pushes the mode to be more confined around the conductor area, which has a lower real refractive index as compared to the dielectric in the substrate, and the real part of the microwave effective mode index decreases accordingly, as shown in Fig. 4.13. These results are in good agreement with the slow-wave behavior of the microwave field propagating in the CPW, as reported in [82, 83]. This behavior is due to the electrical and magnetic field confinement in the Metal-Insulator-Semiconductor (MIS) CPW, determined by the structure capacitance and inductance, respectively [84, 85]. This reflects
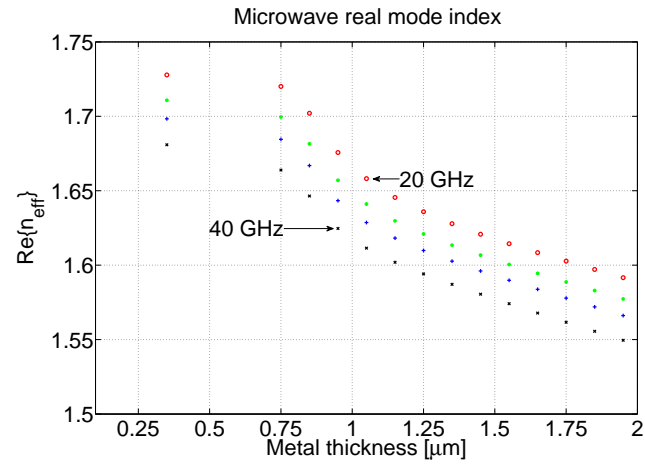
Figure 4.13: Real part of the microwave effective mode index as a function of metal thickness and operating frequency.
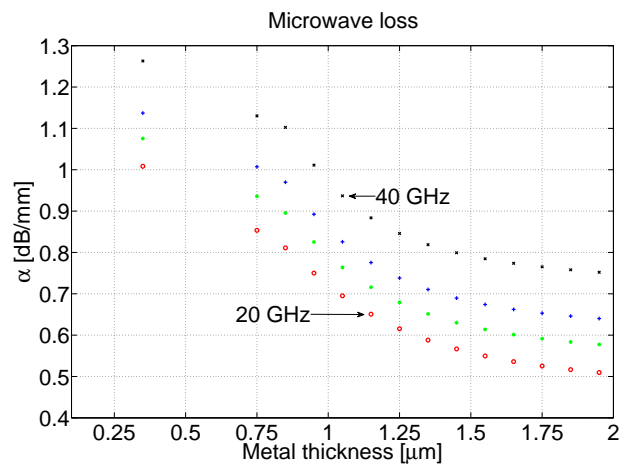

Figure 4.14: Loss in dB/mm as a function of metal thickness and operating frequency, determined by the imaginary part of the microwave effective mode index.

Common ground pad

Si gratings   RF signal pads   GSG pads   Metal fingers
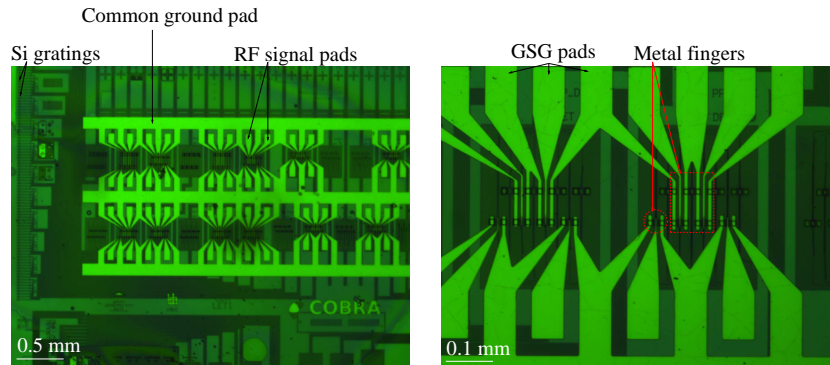
Figure 4.15: Left: Picture of photodetectors processed with the improved RF pattern metal-mask. Right: A close-up on two detector groups. Half of the PDs are connected to the RF pads by means of short tapered structures. The remaining half makes use of a very short transmission line.

in reducing the mode propagation velocity to a value smaller than the one determined by the medium permeability and permittivity, characteristic of a transverse electromagnetic (TEM) wave. Fig. 4.13 and Fig. 4.14 also show the dependence on the metal layer thickness: losses decrease when a thicker metal layer is used, as the electrical signal is in that case more confined in the conductor area, hence suffering less resistance. However, the predicted improvement in terms of loss at RF frequencies provided by the electro-plating option is relatively small: for a transmission line of 1-1.5 mm, which was the case for the photodetector chip previously mentioned, the RF electrical signal propagation loss would be reduced by less than 1 dB, as can be read from Fig. 4.14. That made this option a less promising solution.

An alternative to the electro-plating is the implementation of a simpler RF metal pattern, which avoids the use of any transmission line and which was indeed designed and used for the following chip run. Fig. 4.15 shows pictures of the devices fabricated with the new RF metallization pattern. As can be seen in Fig. 4.15 (right) , half of the PDs are connected to the RF pads by means of 100 μm long tapered structures, avoiding the use of any transmission line. The remaining half makes use of an additional very short transmission line (around 70-80 μm long), much shorter than that used in the previous design and without any 90° bent sections (see Fig. 4.11, left). Furthermore, further improvements were implemented to face the poor definition of the p-metal finger, as explained in Section 4.4.2: firstly, in the new layout the metal fingers extend for 10 μm beyond the detector mesa and side-contact edges, as shown in Fig. 4.16. This way, the structure edges, which always affect the lithography process, fall outside the device area and the metallization on the PD remains better defined. Secondly, key parameters of the metal-lithography processing step were optimized, namely: the resist spinning speed was increased to 4000 rpm to obtain a thinner resist layer, the chip soft-bake temperature was increased to 95°C and the exposure was changed into a single 150 seconds exposure. These changes were made based on previous experiments done in our group
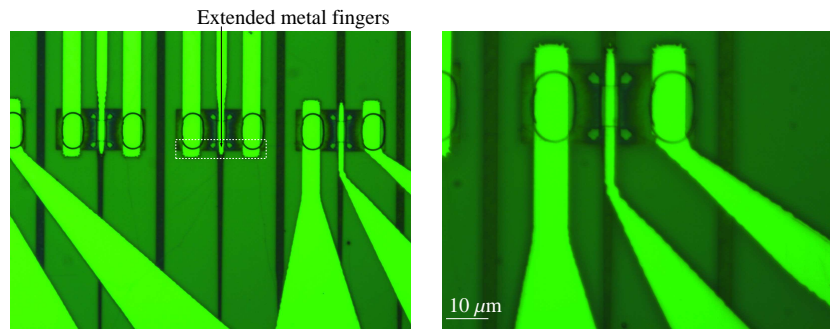
Extended metal fingers

Figure 4.16: Left: Picture of photodetectors processed with the improved RF pattern metal-mask. The metal fingers extend for 10 μm beyond the mesa and side-contact edges to improve the accuracy of the pattern definition during the metal-lithography step. Right: A close-up on a device, showing the result of the metal evaporation and lift-off after using the improved RF metal-mask.
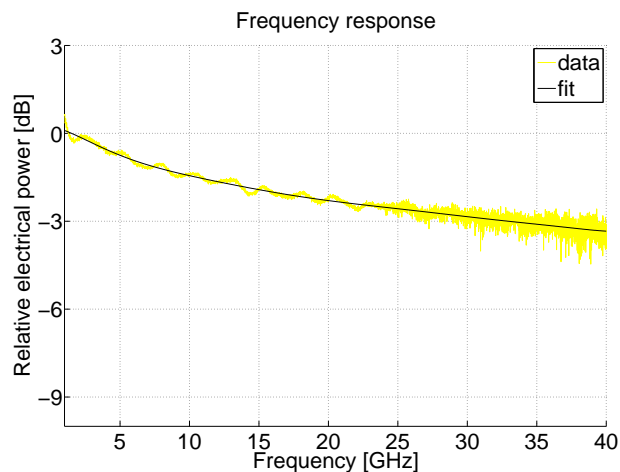

Figure 4.17: Detector RF frequency response: transmission parameter S_{21}.

to optimize the resist profile and pattern resolution for different structures and feature sizes. Fig. 4.16 (right) shows a close-up of a photodetector processed with the new metallization scheme: a better mesa coverage and a higher structure resolution can clearly be noticed, as compared to the results in the previous chip run (see Fig. 3.20, right). The disadvantage of this improved RF pattern with respect to the electro-plating option is that a lower device integration density can be achieved, due to the space taken by the RF pads.

Optical-to-Electrical (OE) dynamic measurements of the new PDs are performed using the
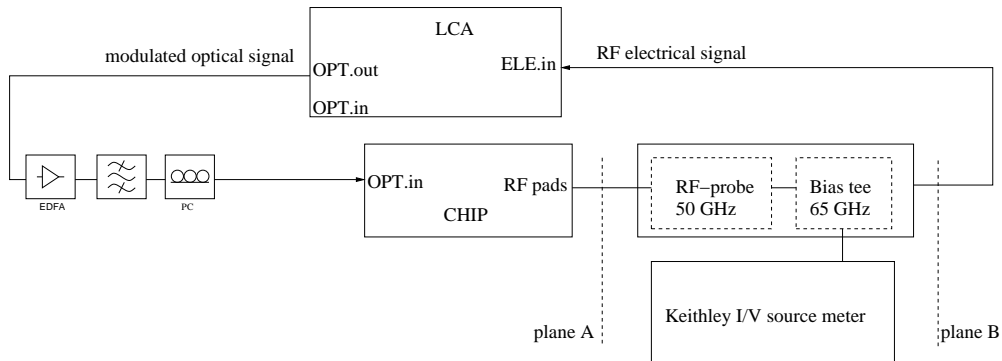
Figure 4.18: Schematics of the set-up used for the dynamic measurements of the detectors with the improved RF metal pattern.

set-up shown in Fig. 4.18 in the range of 100 MHz to 40 GHz with an Agilent HPN4373B 67 GHz LCA, used for small signal modulation of the input optical power from the 1550 nm laser source integrated in the LCA optical module and for reading out the RF photogenerated electrical signal. Results are presented in Fig. 4.17: a 3 dB cut-off frequency response of about 33 GHz was measured, which quite well matches the expectations, as described in Section 2.3.2.

4.5   Integrated optical link

4.5.1   Link design

A full optical link on an SOI chip was realized within the PICMOS project framework. In that context, the optical link consists of a heterogeneously integrated InP-based microdisk laser (MDL) and a microdetector. The electrically driven InP-based MDL is coupled evanescently into the Si waveguide in the interconnection layer. The optical power is carried by the Si waveguide ($500 \times 220\,\text{nm}^2$ in cross section) over the link and is coupled into a PD structure by means of an InP membrane coupler: the mask layout and a schematic drawing of the MDL-to-PD point-to-point link are shown in Fig. 4.19. The MDL is realized with an InAsP multi-quantum well active layer in the n.i.d. InGaAsP core, which is sandwiched between an n-type contact layer and a tunnel-junction-based p-type contact [86]. The PD structure is built as an n.i.d. InGaAs absorption layer sandwiched between a highly p-doped InGaAs contact layer and a highly n-doped InP layer, which is also used for realizing a membrane waveguide acting as a coupling structure. The microdisk and the detector mesa footprints are $50\,\mu\text{m}^2$ [76].
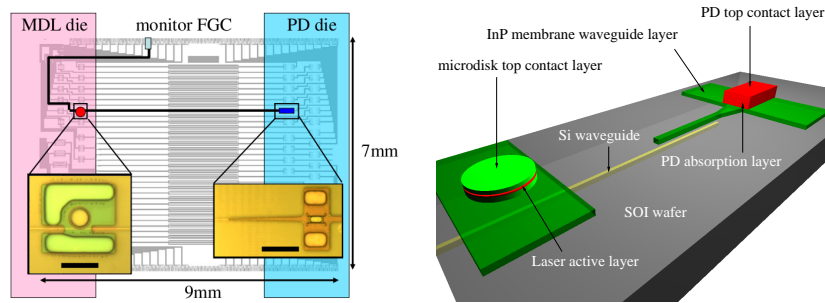
Figure 4.19: Mask layout (left) and schematic diagram (right) of a photonic link on an SOI substrate: the electrically pumped MDL launches an optical signal into the Si wave guide. Light is collected by the detector structure.

4.5.2 Fabrication

Two InP-based 2" wafers with the MDL and the PD layer stack were grown with Solid Source MBE and MOVPE, respectively, and diced in $9 \times 4.5\,mm^2$ pieces. The dies were then molecular-bonded upside down on an SOI wafer (see Section 3.2), in which the Si waveguide pattern had been defined. FGCs [77] were etched into the Si photonic waveguide layer to allow monitoring the laser output power. After bonding, the InP die substrate and the etch-stop layers were removed by a combination of CMP, HCl-based and H_2SO_4-based wet-etching, respectively, and laser and PD pattern were defined by e-beam lithography and transferred to a 150 nm SiO_2 hard mask. Afterwards, the SOI wafer was sawn into samples, each containing the MDL and the PD photonic dies, which were processed as described in Section 3.3.2. Fig. 4.19 (left) shows the mask layout and a picture of the fabricated devices in the inset, taken with an optical microscope before the chip metallization.

4.5.3 Link measurements

The static performance of the integrated optical link was tested at room temperature by applying a variable current to the MDL and detecting the corresponding PD current. In the fabricated chip, not all the lasers and detectors worked and only a few MDL-to-PD links could be measured. A working combination was found for a microdisk laser with a diameter of $7.5\,\mu m$ and a detector of $30 \times 5\,\mu m^2$. The length of the link was 7 mm. A pulsed current drive signal with a duty cycle of 8% (80 ns pulses, 1 µs period) was applied to the MDL in order to avoid excessive self heating of the laser [76]. The optical power launched into the SOI waveguide was monitored through the FGC at the end of the SOI wire opposite to the one terminated by the detector (Fig. 4.19, left). The detector was kept unbiased at 0 V throughout the experiment, as the detectors on this particular sample suffered from relatively large dark currents (several µA) at elevated reverse bias level, most probably due to unexpected erosion of the top p-contact layer, occurred during the mesa wet-etching step (see Fig. 4.20). The measured data for the
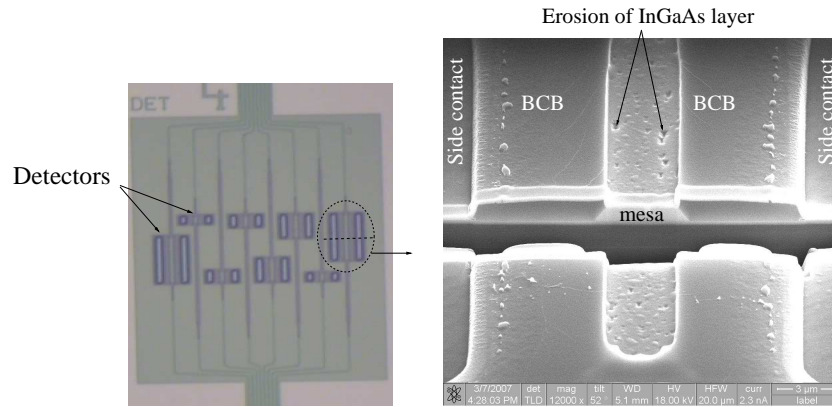
Figure 4.20: Optical microscope picture (left) of detector structures after the mesa wet-etching processing step. A 30 μm long detector structure was investigated by FIB (right): the erosion of the mesa due to unexpected wet-etch of the top InGaAs p-contact layer is indicated.
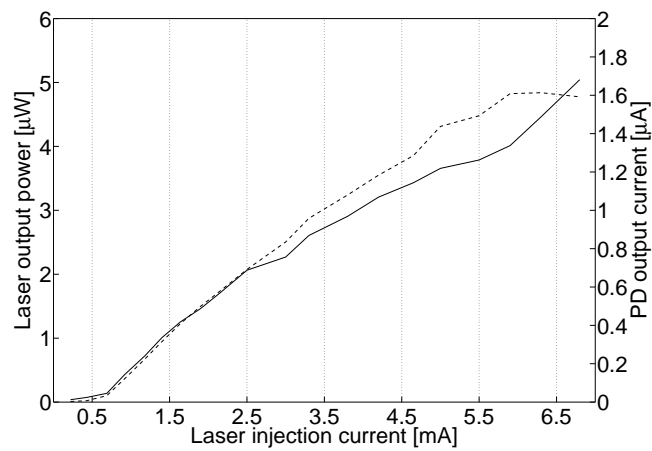

Figure 4.21: Laser-to-PD integrated link measured in laser pulse-regime. A pulsed current drive signal with a duty cycle of 8% was applied to the laser. The laser output power (dashed line) and detector photocurrent (solid line) as a function of the laser pump current are plotted after correction for the duty cycle.

pulsed experiment can be found in Fig. 4.21, showing the laser power in the SOI waveguide and the detector current as function of the laser current, after correction for the 8% duty cycle used in the laser driver. The threshold of the laser is reached at a laser current of 700 µA. The laser slope efficiency is estimated to be 1.8 µW/mA, accounting for a grating coupler efficiency of 25%. The measured detector current is almost linear with the output power of the MDL. The detector responsivity was estimated to be 0.33 ± 0.04 A/W, under the assumption that the MDL emits equal amounts of power in both directions of the SOI waveguide and that the propagation loss for both on-chip light paths is equal. At the maximum laser current of 6.8 mA, the recorded detector current was as high as 1.75 µA.

The link developed within this work is the first laser-to-detector optical interconnection demonstrated on Si [76]. Its performance is still modest because of the low link efficiency and low power emitted by the source, which limit the maximum data rate and make it difficult to drive the CMOS circuitry. We expect that significant improvement is possible.

4.6 Photodetectors on CMOS

The detectors designed for wafer bonding on a CMOS wafer use the layer stack shown in Fig 3.1. The 400 nm thick Si_3N_4 interconnect waveguides are patterned on top of the last electronic IC metallization layer in the CMOS wafer. The Si_3N_4 waveguide layout is analogous to the Si waveguide layout used for realizing the membrane coupler chip, schematically shown in Fig. 4.2. The input optical signal is split into two branches by a 3 dB Si_3N_4 MMI splitter. Fig. 4.22 shows some relevant parts of the mask layout and a close-up on a detector structure, respectively. The PDs are aligned over the lower output arms of the Si_3N_4 MMI splitters, while the upper arms are used as a reference for the measurements. For manufacturing this chip, a 2" InP wafer with the layer stack shown in Fig 3.1 was grown and molecular-bonded upside down on an 8" CMOS wafer, which was sawn in $3 \times 3\,cm^2$ dies afterwards to allow for processing in the COBRA clean room. After the device processing, which is described in Section 3.3, the chip was sawn to allow for light edge-coupling to the Si_3N_4 waveguides. Fig. 4.23 shows optical microscope pictures of the fabricated chip.

4.6.1 Measurements

The detector DC characterization is performed by using an external HP8168A TLS and a Keithley 2400 source-meter unit to reversely bias the device and read out the generated photocurrent, with a set-up analogues to that as schematically shown in Fig. 4.7. Dark current values around -2 nA were registered at -4 V. The optical signal is edge-coupled into the Si_3N_4 waveguide and guided towards the detectors. The detector generated photocurrent as a function of the applied bias voltage was measured for TLS output powers of -2 and -3 dBm. The measurement results are shown in Fig. 4.24. To evaluate the detector efficiency, the following factors are considered. Firstly, the fiber connections from the TLS to the PC and to the coupling input fiber causes a loss of 0.7 dB. Secondly, an additional 3 dB loss caused by the integrated Si_3N_4 MMI splitter has to be taken into account (see Fig. 4.23, right). The insertion loss of
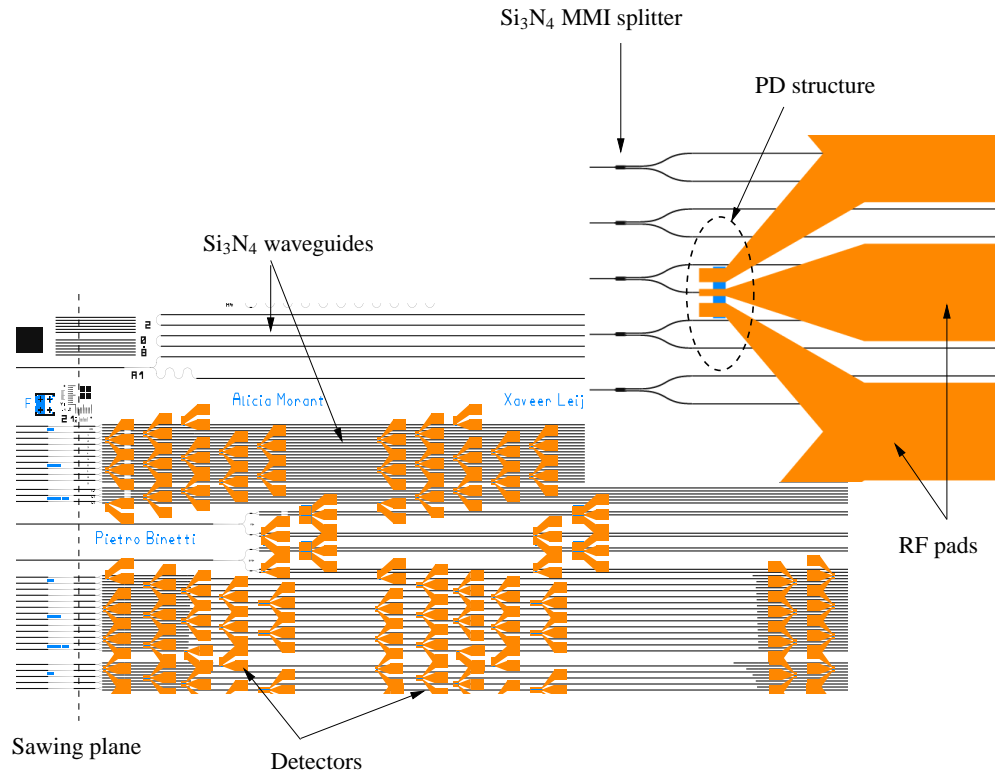
Figure 4.22: Mask layout. The PDs are aligned over the lower output arms of the Si_3N_4 MMI splitters, while the upper arms are used as a reference for the measurements. On the left, the position of the sawing plane is indicated. On the right, a close-up on a photodetector aligned on a Si_3N_4 waveguide is shown.

the MMI splitter is neglected, as it is within the 0.1 dB accuracy of the measurements performed. Thirdly, the Si_3N_4 waveguide propagation loss was measured to be around 6 dB/cm at $\lambda = 1550$ nm, as reported in [59]. That causes an additional 0.5 dB loss in the 1 mm long path to the detector. Lastly, a 3±0.5 dB loss is estimated for the fiber-to-chip edge-coupling, determined by the fiber-waveguide mode matching and the Fresnel reflections at the chip facet, which are estimated to be around 10%. The responsivity of the PD structure is thus calculated to be $R = 0.68 \pm 0.1$ A/W at $\lambda = 1550$ nm, which corresponds to a quantum efficiency $\eta = 55 \pm 8\%$.

OE dynamic measurements of the PDs are performed using the set-up shown in Fig. 4.25 in the range of 100 MHz to 40 GHz with an Agilent HPN4373B 67 GHz LCA, used for small signal modulation of the input optical power from the 1550 nm laser source integrated in the LCA optical module and for reading out the RF photogenerated electrical signal. Results are
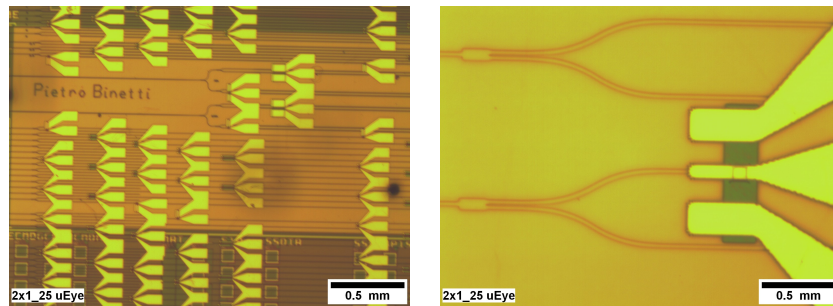
Figure 4.23: Left: picture of the fabricated PDs on a CMOS sample. Right: Close-up on a PD structure. The input Si_3N_4 waveguide is coupled to a 50/50 MMI waveguide, which splits the optical signal into a reference arm and a test arm, on top of which the detector is aligned.
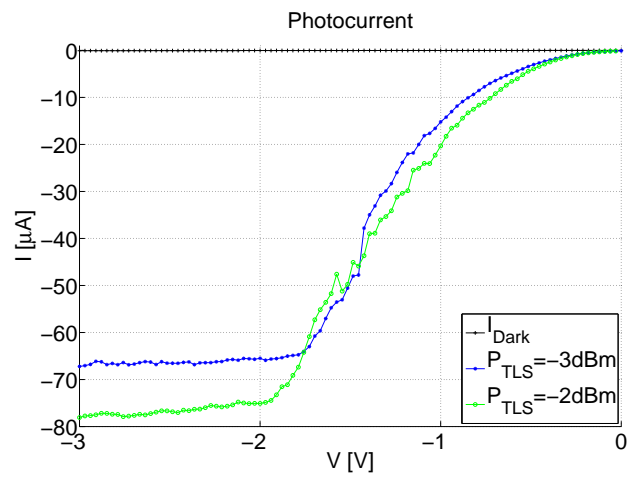

Figure 4.24: Dark current and photocurrent measured for -2 and -3 dBm optical input power as a function of the detector applied bias voltage.
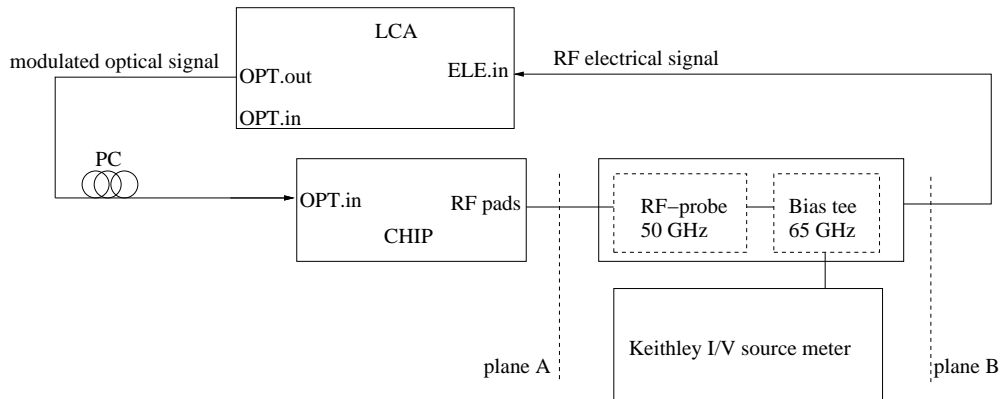
Figure 4.25: Schematics of the set-up for RF measurements of the *S* parameters performed with the 67 GHz LCA.
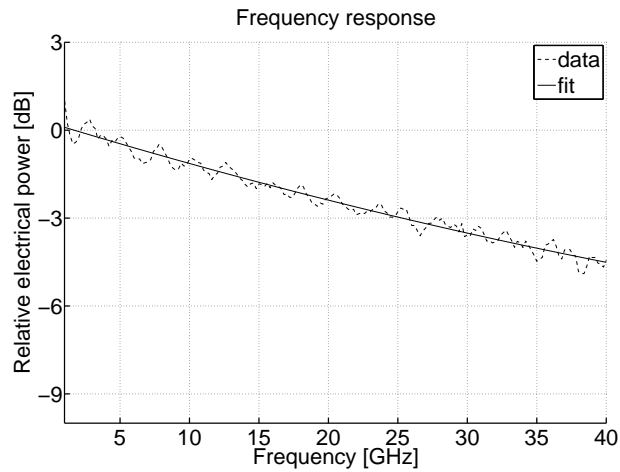
Figure 4.26: Detector RF frequency response: transmission parameter S_{21}.

presented in Fig. 4.26, which shows an OE 3 dB cut-off frequency response at 25 GHz.

4.7 Conclusions

In this chapter, an InGaAs/InP photodetector structure suitable for optical interconnections on Si has been presented. The PD mesa footprint is $5 \times 10\,\mu m^2$ and an InP membrane input waveguide is used to couple the optical signal out of the interconnect layer. A number of chips

were fabricated and have been discussed in this chapter.

An all-passive chip with InP membrane coupler structures was manufactured and characterized. The purpose of this chip was to obtain experimental feedback on the membrane input coupler that is used in the PD structure. Propagation losses in the InP-membrane waveguides of ~100 dB/cm were registered in the $\lambda = 1550$-1600 nm wavelength range, which gives an additional ~0.15 dB loss for the membrane coupler. A coupling efficiency exceeding 50% was measured for the Si-to-InP coupler structure, caused by the growth of a thinner InP membrane waveguide layer.

Photodetectors coupled to Si waveguides were developed on an SOI wafer and were characterized. DC measurements recorded a detector responsivity $R = 0.45$ A/W, which corresponds to a quantum efficiency $\eta = 35\%$. This efficiency includes the InP membrane input coupler efficiency and the internal quantum efficiency of the p-i-n detector itself. The speed of these detectors was limited to 15 GHz, mainly due to the metal transmission line integrated on the chip. This limitation was removed in a next chip run, where an improved RF metallization scheme was used and the metallization lithography was optimized. Dynamic measurements of the improved PDs recorded a 3 dB cut-off frequency response of about 33 GHz, limited by the carrier transit-time in the depletion region.

Photodetectors bonded on Si_3N_4 interconnect waveguides defined on top of a CMOS wafer were also manufactured. Si_3N_4 waveguides do not allow for the same high wire integration density that can be achieved with SOI technology, but they do offer an easier integration with the CMOS ICs: the waveguides are defined on a Si_3N_4 layer deposited by PECVD on a SiO_2 buffer layer on top of the CMOS circuitry, without the need of additional bonding steps. The DC and RF measurements of these detectors recorded a responsivity $R = 0.7$ A/W, which corresponds to a quantum efficiency $\eta = 55\%$, and a bandwidth of 25 GHz. In this case, the detectors do not make use of any membrane coupler structure to couple the light out of the Si_3N_4 layer. However, due to the smaller light confinement in the Si_3N_4 waveguide core, the responsivity is higher as compared to the PDs on SOI waveguides.

In the framework of the EU PICMOS project, the first integrated laser-to-detector point-to-point optical link on an SOI wafer was reported. Si photonic waveguides were used to interconnect InP-based microdisk lasers and detectors, which were processed on InP-based dies molecular-bonded on the SOI wafer. The measured PD current is almost linear with the output power of the MDL and the PD responsivity was estimated to be 0.33 A/W.

Chapter 5

Heterogeneous MWRs

This chapter discusses the design, fabrication and characterization of the heterogeneous multi-wavelength receivers (MWRs) realized in InP-on-Si technology. First, the MWR device concept is explained. Then, the attention is focused on the components the MWR is made of: silicon-on-insulator waveguides, demultiplexer and InP-based detectors. The design of each component and the process flow developed for their heterogeneous integration are discussed. Finally, experimental results are presented and an outlook for the future work is given.

5.1   Introduction

The multiwavelength receiver is an essential component for a wavelength division multiplexing (WDM) network. Its basic concept is schematically shown in Fig. 5.1: the input multiwave-length signal carrying *n* wavelengths is first demultiplexed into *n* channels, each carrying one
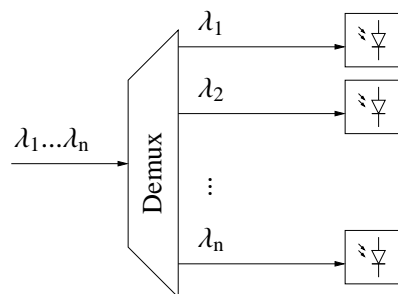

Figure 5.1: Schematic diagram of a multiwavelength receiver device. A broadband signal is demultiplexed into several channels, each carrying one wavelength. The optical power carried by each wavelength is absorbed by a photodetector, which converts the optical signal into an electrical signal.
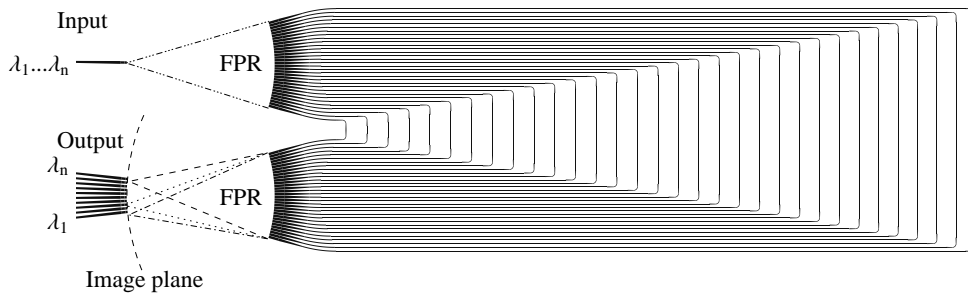
Figure 5.2: Annotated layout of the arrayed waveguide grating.

wavelength. The optical power carried by each wavelength is then absorbed by a photodetector, which converts the optical signal into an electrical signal.

The integrated MWR developed in this work, and within the framework of the Smartmix-MEMPHIS[1] project, is realized in a heterogeneous InP-on-Si technology, in which the receiver passive components, namely waveguides and demultiplexer structure, are realized in silicon-on-insulator (SOI), and the photodetectors are based on InP. This device is suitable for use in applications such as on-chip and off-chip optical interconnections and it benefits from the advantages of the employed heterogeneous integration: the SOI technology offers good waveguiding properties and very high integration density thanks to the high light confinement in the SOI waveguide structure core [30], while the InP-based detectors are more efficient and faster as compared to Si PDs. The receiver demultiplexer is implemented as an arrayed waveguide grating (AWG) defined in the waveguide layer of an SOI wafer, while radio frequency (RF) InP-based photodetectors (PDs) are bonded on the SOI wafer for the optical-to-electrical (OE) conversion of the demultiplexed output signals. The AWG device is extensively described in [87, 88], however, for convenience we briefly summarize its principle here, referring to Fig. 5.2. The light carried by an input waveguide (e.g. a WDM signal) is no longer laterally confined after entering the free propagation region (FPR). The diffracted light is collected by the waveguide array, and propagates through the AWG arms. In the output FPR, the fields guided by the array arms diverge because the light is not laterally confined, and therefore they interfere. The AWG adjacent arms are designed with a length difference equal to an integer multiple of the central wavelength. For this wavelength, the fields that propagated through the array arms arrive at the output aperture with equal phase and constructively interfere in the output FPR. Thus, an image of the input field is reproduced at the center of the image plane. For other wavelengths, the path length difference between the adjacent array arms causes a phase difference between the fields that arrive at the output aperture. Therefore, the recombined field has a tilted phase front and is focused to a different point on the image plane. By placing output waveguides centered to the spots where the fields are focused on the image plane, the optical

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[1]Merging Electronics and Micro & Nano-Photonics in Integrated Systems (MEMPHIS), http://www.smartmix-memphis.nl/
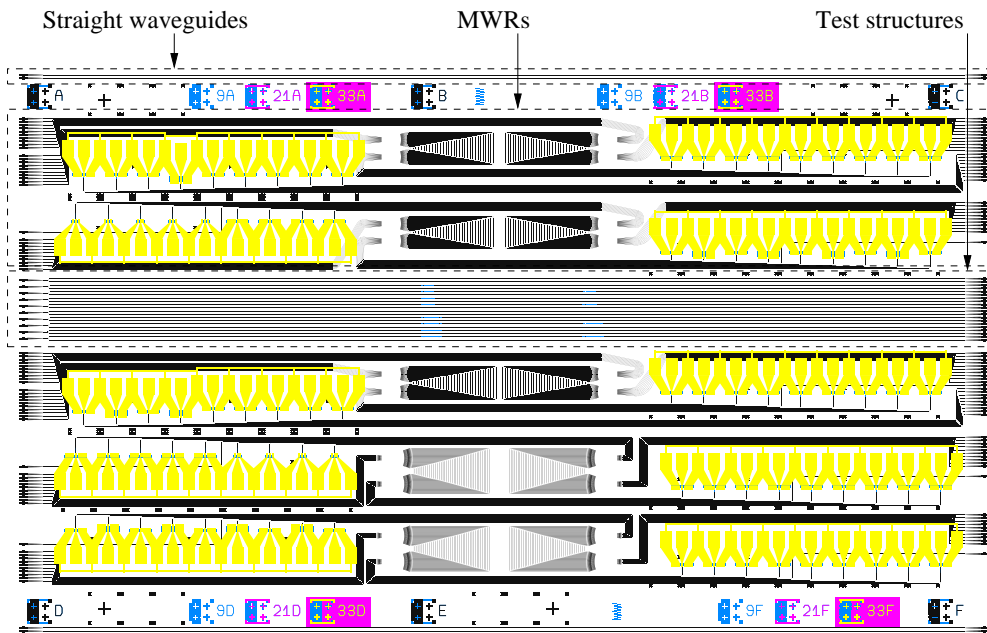
Figure 5.3: Mask layout of the MWR chip.

power carried by the input wavelengths is coupled into different output channels. A fiber grating coupler (FGC) integrated on the chip is used to couple the optical power generated from an external source for characterizing the MWR.

The design, fabrication and characterization of the receiver are described in this chapter.

5.2 Integrated components

In this section, an in-depth description of the structures designed for the realization of the MWR chip is given. As it can be seen in the mask layout, shown in Fig. 5.3, the components that are integrated on the chip are the following:

FGCs As no light sources are integrated on the chip, an off-chip generated optical input signal has to be used to characterize the MWRs. Integrated grating structures defined in the SOI waveguide layer are used to couple the external optical input signal to the waveguides on the chip.

Waveguide structures SOI waveguides are used to interconnect the several components integrated on the chip.

AWGs These devices are defined in the SOI waveguide layer and implement the demultiplexing function of the receiver.

PDs InP-based photodetectors are used to absorb the optical power carried by the output channels of the AWGs and convert it into an electrical signal.

5.2.1   Fiber grating couplers

The Si fiber grating couplers developed by the University of Ghent [77] are used to couple the optical power from/to an external single-mode fiber (SMF) to/from an SOI waveguide on-chip, thus allowing for on-wafer measurements, as explained in Section 4.2. The FGCs are defined by optical lithography and are shallowly etched in the Si waveguide layer. They are designed with an element width and pitch of 325 nm and 615 nm, respectively, while the number of elements is 25. With this geometry, the grating footprint is about $12 \times 15 \, \mu m^2$ and an angle of about 8°-10° with respect to the vertical needs to be used to prevent a 3 dB loss and optimize the fiber-to-waveguide coupling efficiency. The minimum vertical pitch between adjacent FGCs is $20 \, \mu m$, which allows for a high integration density and low optical crosstalk at the same time.

   The use of these gratings permits the characterization of the MWR passive SOI components before the integration of the InP-based detectors because there is no need for sawing the sample, which is one of the main advantages of the heterogeneous integration scheme. In this way, transmission measurements of SOI test structures and AWGs can be performed and the experimental results can be used as a reference for the characterization of more complex components which include the InP-based devices. Fig. 4.1 shows scanning electronic microscope (SEM) pictures of some fabricated Si gratings.

5.2.2   Interconnect waveguides

Si waveguides are used to interconnect the MWR components integrated on the chip. The external optical input signal is collected by a FGC and coupled to an SOI waveguide by means of a $100 \, \mu m$ long tapered waveguide. Fig. 4.1 (left) shows an SEM picture of these tapered structures. The SOI waveguide carries the optical power towards the input FPR of the receiver demultiplexer. After the propagation through the AWG arms, the optical power is collected by SOI waveguides placed at the fan-out section of the AWG and then guided towards the detectors. These single-mode interconnect waveguides have a cross-section of $500 \times 220 \, nm^2$ and are realized in SOI technology, which allows for high integration density thanks to the high refractive index contrast between the waveguide core and cladding materials.

5.2.3   Multi-mode interference splitter

Test structures are implemented in the mask set to characterize the passive interconnect waveguides and the InP-membrane couplers. These test structures are built as an FGC coupled to an input Si waveguide that enters a 1×2 MMI coupler, acting as a 3 dB splitter. The MMI lower output connects to a reference waveguide that ends at the edge of the Si cell and can be used for
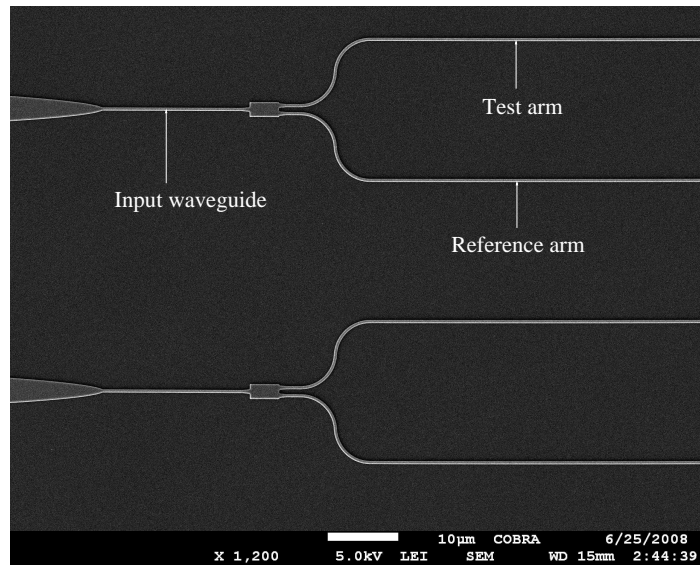
Figure 5.4: SEM picture of two fabricated MMI structures.

the characterization of the SOI waveguide, while the upper test arm is used to characterize the test InP-membrane couplers. The Si test arm is divided into two sections, separated by a gap: the InP membrane couplers are defined over that gap during the processing of the bonded InP die, analogously to the passive coupler structures described in Section 4.3. Both the reference arm and the second part of the test branch are terminated with an FGC, for characterization. Those InP membrane couplers play a critical role in the MWR structure, as they couple the optical power carried by the AWG output waveguides towards the photodiode absorption layer. Fig. 5.4 shows an SEM picture of two fabricated MMI structures, while a close-up on an MMI waveguide is captured in Fig. 5.5. Simulations were performed with Agilent's Advanced Design System (ADS), in which we implemented an optical circuit simulator [89], to design the 1×2 MMI coupler with a splitting ratio of 50/50. As can be seen in Fig. 5.6 and Fig. 5.7, the optimum MMI waveguide length and width were found to be $4.28\,\mu\text{m}$ and $2.2\,\mu\text{m}$, respectively, while the optimum offset of the output waveguides from the center of the MMI structure was found to be 565 nm, as can be read in Fig. 5.8. Moreover, to avoid reflections at the input and output sections of the splitter, the MMI access waveguides are adiabatically tapered out to 700 nm by means of a $1\,\mu\text{m}$ long taper, as indicated in Fig. 5.5.

5.2.4   Arrayed waveguide gratings

Ten AWGs are designed in the mask set for the realization of the MWR chip, as shown in Fig. 5.3. They are designed as 10 channel AWGs with a channel spacing of 1.6 nm (200 GHz in frequency) and a period, or free spectral range (FSR) of 16 nm, corresponding to ten times

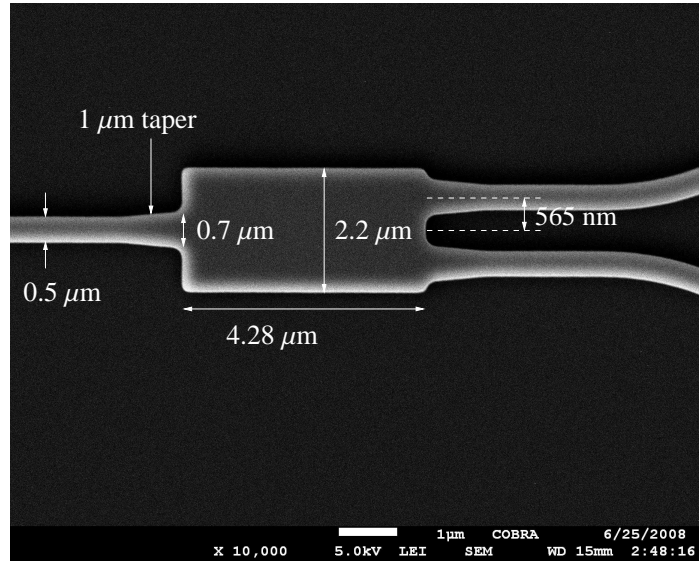**Figure 5.5:** SEM picture of a 1×2 MMI waveguide with access waveguides. The key device dimensions are indicated in the picture.
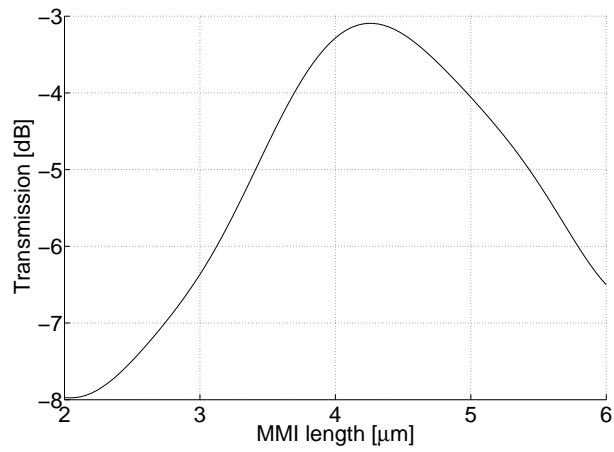

Figure 5.6: ADS transmission simulations of a 1×2 MMI waveguide as a function of the MMI waveguide length.
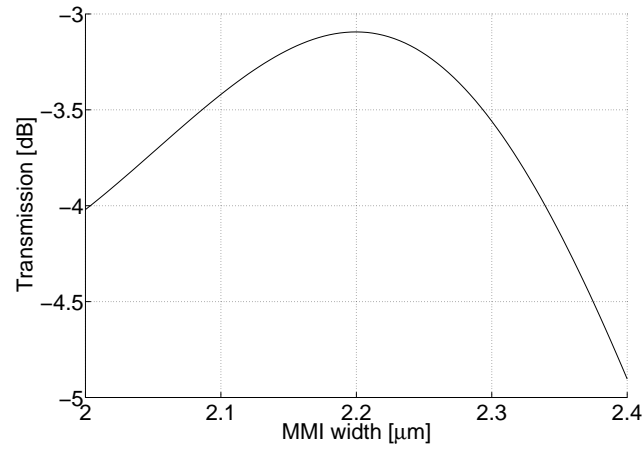
Figure 5.7: ADS transmission simulations of a 1×2 MMI waveguide as a function of the MMI waveguide width.
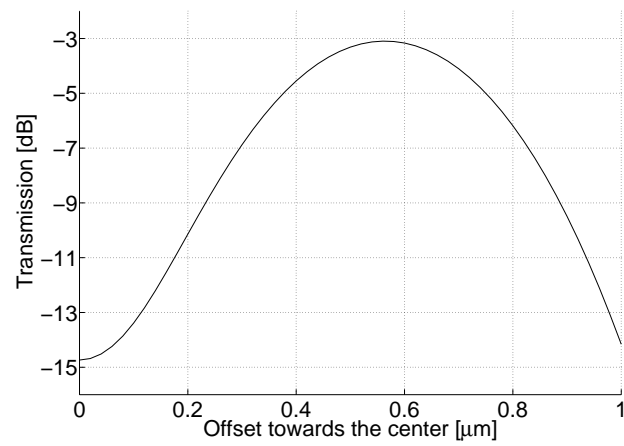

Figure 5.8: ADS transmission simulations of a 1×2 MMI waveguide as a function of the lateral offset applied to the output waveguides with respect to the center of the MMI structure.
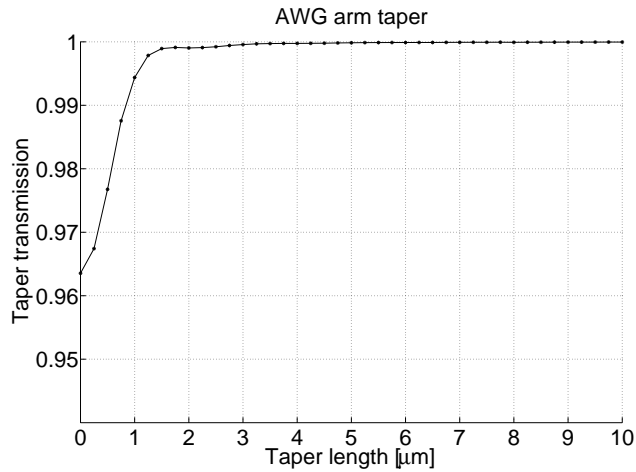
Figure 5.9: BPM simulations of the taper transmission in the AWG straight arm sections as a function of the taper length.

the channel spacing. For each AWG, nine of the ten output waveguides are connected to the integrated InP-based PDs, while the remaining waveguide is terminated with an FGC, enabling the characterization of the demultiplexer without using a PD. The AWGs are designed with a very compact orthogonal geometry, thanks to the high light confinement of the SOI waveguides. The waveguide grating arms are 800 nm wide in the straight sections and are tapered down to 500 nm in the curved sections, where the waveguides are monomode. To avoid any mode conversion, a 5 μm long linear adiabatic taper is used. This tapered waveguide structure was simulated with the beam propagation method (BPM) implemented in OlympIOs, by C2V. BPM simulation results are shown in Fig. 5.9, where the taper transmission is plotted as a function of the taper length. The 5 μm long linear taper implemented in the mask design guarantees the monomode condition for the field propagating through each AWG arm. The 90° bends of the orthogonal AWGs are designed with a bending radius of 3 μm, which provides negligible additional loss with respect to a straight waveguide [47]. The same minimum bending radius is used for the waveguides outside the AWGs. A lateral offset can be applied at the straight/curved waveguide junction to optimize the signal transmission. This can be done by maximizing the overlap of the optical power of the modes guided by the two waveguide sections [90]. Simulations were performed with ADS to investigate the optimum offset as a function of the bending radius for a $500 \times 220 \, \text{nm}^2$ SOI waveguide. The simulation results are shown in Fig. 5.10: even for very sharp bending radii (few micrometers), the calculated optimum offset is very small (few nanometers). Following up these results and considering the fact that a 5 nm grid was used to write the mask set for the fabrication of the SOI circuitry, no offset was applied at the straight/curved waveguide junctions. Fig. 5.11 (left) shows an SEM photograph of a Si curved waveguide.
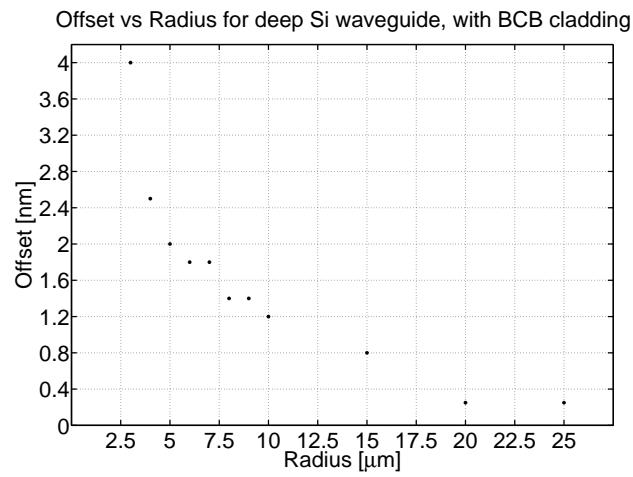
Figure 5.10: Calculated optimum lateral offset to be applied at a straight-curve waveguide junction as a function of the waveguide bending radius.
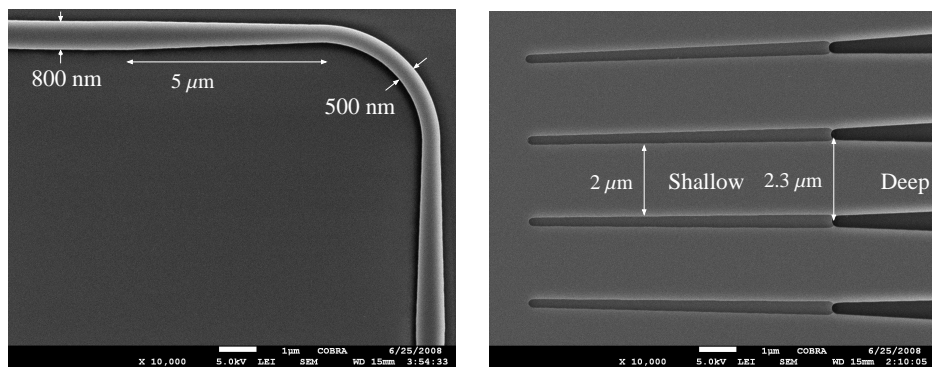

Figure 5.11: Left: SEM photographs of a curved waveguide of a fabricated AWG arm section. Right: SEM photograph of a shallow-to-deep transition in a fabricated AWG.
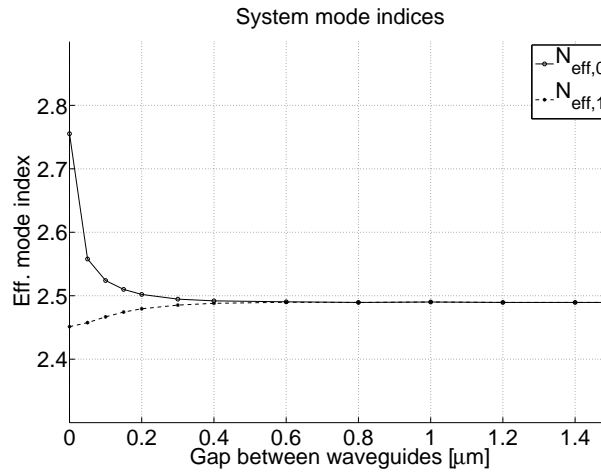
Figure 5.12: Maximum optical coupling between two adjacent SOI waveguides calculated as a function of the center-to-center waveguide spacing and waveguide width.

The AWG adjacent arms are designed to minimize the size of the integrated devices, aiming at high integration density, and at the same time to provide sufficient optical isolation between the SOI arms. This was investigated through simulations performed with an FD calculation method implemented in the 2D mode solver OlympIOs, by C2V. The simulation results are shown in Fig. 5.12: the system mode effective indices of two adjacent SOI waveguides are plotted as a function of the spacing between them. When the gap increases, the effective index of the even and of the odd system modes are the same, which clearly indicates that the waveguides are not coupled. A safe minimum gap of $1.5\,\mu m$ is used in the mask design.

For reducing the losses, the AWG FPR access waveguides are shallowly etched and a transition structure is designed to optimize the power transmission at the shallow-deep waveguide junctions. This structure is schematically shown in Fig. 5.13: the $2\,\mu m$ wide shallowly etched FPR access waveguide is butt-coupled to a $2.3\,\mu m$ wide deeply etched waveguide at the shallow-deep junction. This is done to match the profile of the fundamental modes of the two waveguides, thus maximizing the power coupling efficiency between the two waveguide sections. This was investigated by means of the 2D full vectorial mode solver FIMMWAVE, by Photon Design, and the BPM method implemented in OlympIOs, by C2V. The simulation results are shown in Fig. 5.14, where the power coupling efficiency between the shallow and the deep waveguide sections is plotted as a function of the offset parameter, as indicated in Fig. 5.13. According to the simulation results, the optimum deeply etched waveguide width at the shallow-to-deep junction is $2.3\,\mu m$. After the shallow-to-deep transition, the deep $2.3\,\mu m$ wide waveguide is tapered down to the 500 nm standard single-mode waveguide width by means of a linear taper. BPM simulations of the taper structure show that a $40\,\mu m$ long taper adiabatically couples the power into the 500 nm wide waveguide, as can be seen in Fig. 5.15.
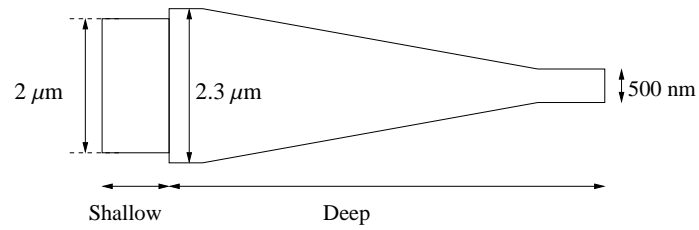
Figure 5.13: Shallow-to-deep waveguide transition. The 2 μm wide shallowly etched wave-guide is butt-coupled to 2.3 μm wide deeply etched waveguide to maximize the efficiency of the power coupling between the two waveguide sections. After the shallow-to-deep junction, the deep 2.3 μm wide waveguide is tapered down to the 500 nm standard single-mode waveguide width by means of an adiabatic 40 μm long linear taper.
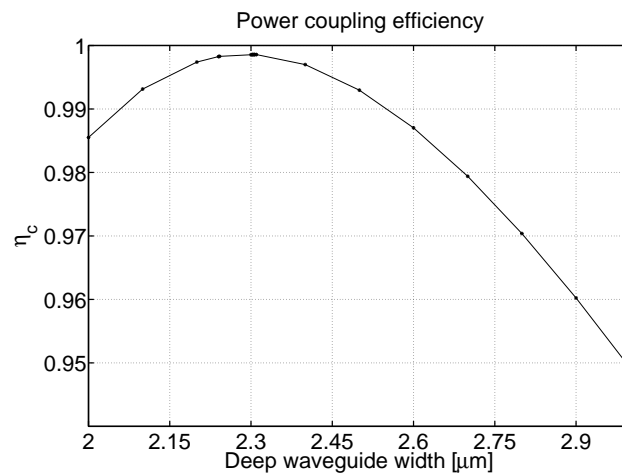
Figure 5.14: Efficiency of the power coupling between the shallow and the deep waveguide sections plotted as a function of the deep waveguide width.

Figure 5.15: BPM simulations of the taper structure used after the shallow-to-deep wave-guide transition in order to adiabatically couple the optical signal to the standard single-mode 500 nm wide SOI waveguide.

An SEM photograph of a shallow-to-deep transition is shown in Fig. 5.11 (right).

With the design figures mentioned above, the size of the 10 channel AWG device is about $700 \times 200 \, \mu\text{m}^2$.

5.2.5   Photodetectors

The InP-based PDs aligned over the output waveguides of the receiver demultiplexer are realized on the same basis of the detector s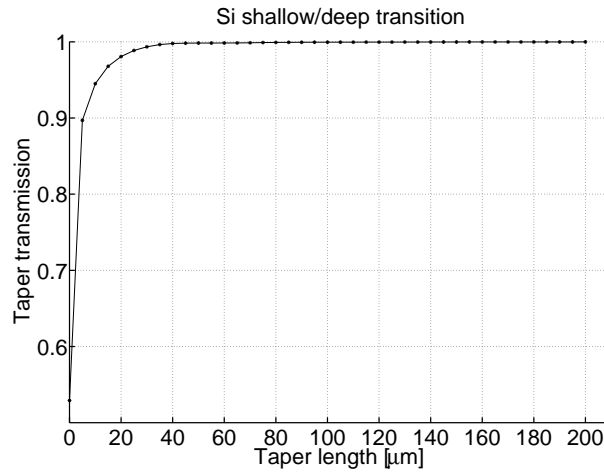tructure presented in Section 4.4: they consist of an InP membrane input waveguide on top of the bonding layer, meant to enhance the optical coupling from the photonic waveguide layer to the absorbing part, a p-i-n junction where the optical power is absorbed and converted into an electrical signal. Additional improvements were investigated to relax the fabrication tolerance of the InP-membrane detector input waveguide as compared to the Si-to-InP coupler implemented in the PD structure of Section 4.4. In this section, the PD implemented in the MWR chip with the improved design of the input membrane coupler structure is presented.

The layer stack used for the detector fabrication is shown upside down, as bonded on the Si wafer, in Fig. 5.16. It is built as a 700 nm n.i.d. InGaAs absorption layer sandwiched by a highly p-doped 50 nm thick InGaAs contact layer and a highly n-doped 220 nm thick InP layer. The n-doped InP membrane layer is also used for realizing the input membrane coupler. With respect to the PD structure described in Chapter 4, the InP coupler waveguide width is broadened to 1550 nm and the layer thickness reduced to 220 nm, while the Si waveguide underneath the membrane InP coupler is broadened to 550 nm. These changes in the coupler geometry lead to an expected considerable improvement in terms of tolerance towards fabri-
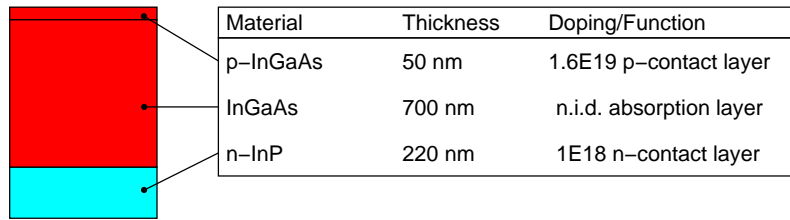
Material	Thickness	Doping/Function
p–InGaAs	50 nm	1.6E19 p–contact layer
InGaAs	700 nm	n.i.d. absorption layer
n–InP	220 nm	1E18 n–contact layer

Figure 5.16: Layer stack used for the fabrication of the photodetectors, shown upside down as it was bonded on the Si wafer.
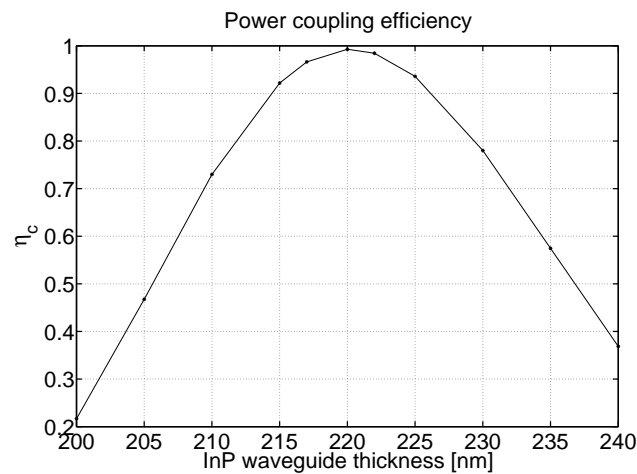
Figure 5.17: Coupler efficiency as a function of the InP membrane layer thickness. The InP and the Si waveguide widths are fixed to 1550 and 550 nm, respectively. In this configuration, a coupling efficiency of more than 80% is achieved with a tolerance of ± 10 nm for the InP waveguide thickness.

cation errors. The new geometry was studied with FIMMWAVE, by Photon Design, and with the BPM method implemented in OlympIOs, by C2V. The simulation results are shown in Fig. 5.17 and Fig. 5.18: the curves plotted in these figures represent the tolerance of the coupler efficiency as a function of the InP membrane layer thickness and width, respectively. The substantial improvement is in the tolerance against the InP-membrane waveguide width: the coupler efficiency drops to 80% for a change of ± 250 nm in the waveguide width, as compared to a tolerance of ± 70 nm obtained for the coupler geometry described in Section 2.3.1. There are two reasons why this is an important improvement, which have to do with the 405 nm Ultra-Violet (UV) optical lithography used to define the InP-membrane waveguide:

- A relaxation in the tolerance towards the InP waveguide width translates into a relaxation
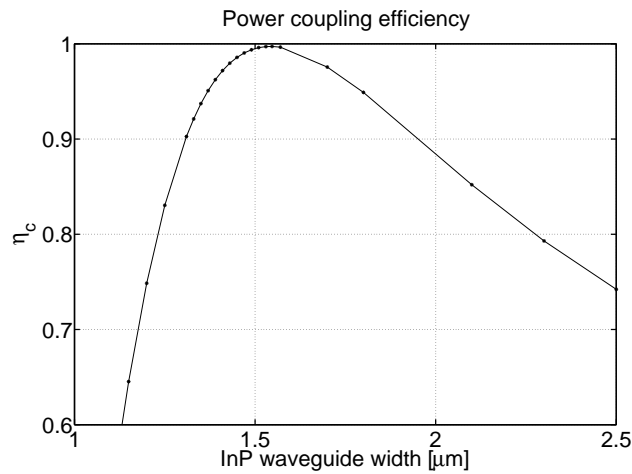
Figure 5.18: Coupler efficiency as a function of the InP membrane waveguide width. The InP membrane layer thickness and the Si waveguide width are fixed to 220 and 550 nm, respectively. The efficiency drops to 80% for an InP waveguide width deviation of ± 250 nm.

towards the UV lithography exposure time/intensity. That means the exposure can be optimized without catastrophic consequences on the coupler efficiency.

- Due to the optical refractive index difference between InP and Si, broadening the Si waveguide from 500 to 550 nm implies broadening the InP waveguide from about 1000 to 1550 nm. As a consequence, the waveguide-to-waveguide alignment performed at the mask aligner is easier and simulations show that the tolerance against lateral misalignment is substantially relaxed (see Fig. 5.19).

According to the simulation results, the fabrication tolerances towards the InP-membrane layer and bonding layer thickness do not change in this new coupler configuration: a coupler efficiency of more than 80% is achieved with a deviation of ± 10 nm for the InP membrane layer thickness and ± 30 nm for the BCB bonding layer thickness. To broaden the Si waveguide from 500 to 550 nm, a $1\,\mu$m long tapered waveguide is used. According to BPM simulations, this compact structure is sufficient to avoid any mode conversion. Fig. 5.20 shows the fundamental mode power overlap from the 500 to the 550 nm wide section of the tapered structure as a function of the taper length.

5.3 Chip realization and characterization

The integration of the MWR chip components is based on the heterogeneous integration approach described in Chapter 3. The Si structures are implemented in a mask set for processing on an 8" SOI wafer; Fig. 5.21 shows a picture of half of this wafer. After processing, the wafer

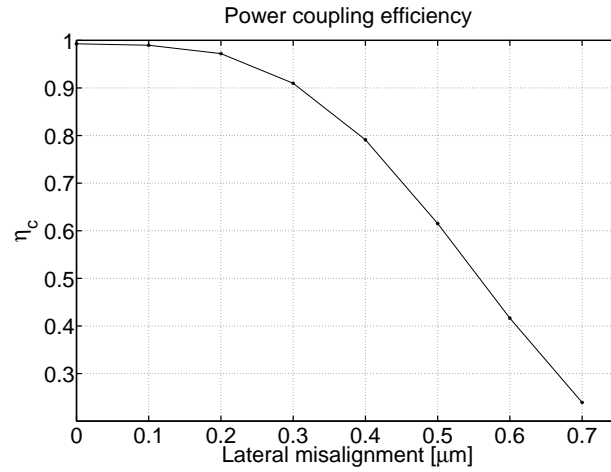**Figure 5.19:** Coupling efficiency tolerance with respect to lateral waveguide misalignment. The efficiency drops to 80% for a misalignment of 400 nm. In these simulations, the width of the Si and the InP waveguides were 550 and 1550 nm, respectively.
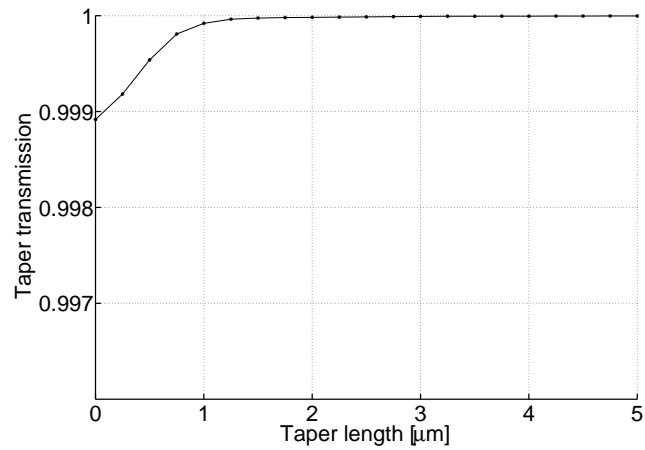

Figure 5.20: Taper transmission for the fundamental mode as a function of the taper length. The Si waveguide structure is tapered from 500 to 550 nm.
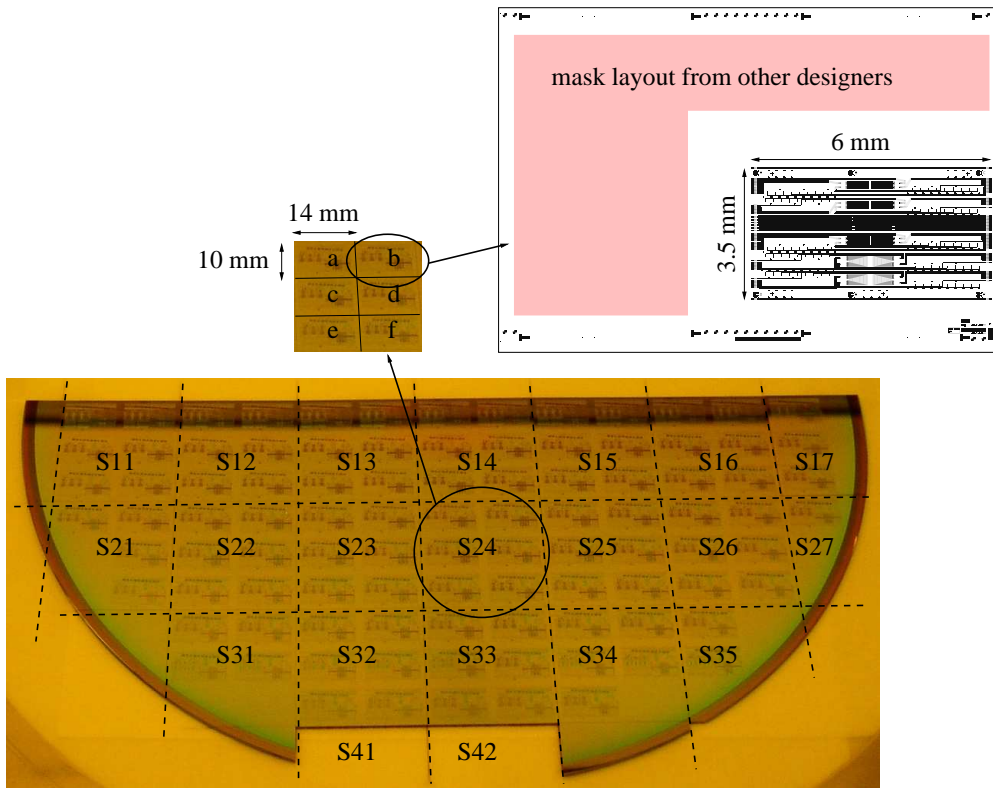
Figure 5.21: Picture of the half 8" Si wafer containing the MWR passive SOI circuitry. Af-
ter processing, the wafer is sawn in square samples: the sawing lines are indicated (dashed
lines). Each sample contains six identical cells, labeled "a, b, ..., f", and the mask layout of
one cell is shown on the top right.

is sawn in square samples of about $2 \times 2\,cm^2$, as indicated in Fig. 5.21. Each Si sample con-
tains six identical $6 \times 12\,mm^2$ cells (labeled "a, b, ..., f" in Fig. 5.21), which include the pattern
of Fig. 5.3. For each sample, only the most central cell is used for the bonding, as shown in
Fig. 5.22. That makes not only the bonding step easier, but also the sample easier to handle
during the InP-based layer stack processing. Furthermore, it guarantees more uniformity of
the polymers spun during the InP die processing. The size and the position of the InP die are
chosen in order to cover the Si cell and with sufficient margin from the markers in the Si layer
located at the edge of the cell, as indicated in Fig. 5.23. This is crucial for the processing: the
InP die needs to cover the whole $3.5 \times 6\,mm^2$ Si cell (indicate in Fig. 5.23), as the detectors
are defined over the same area (see Fig. 5.3). For the feasibility and the ease of the bonding
step, the photonic die size has to be larger than the Si cell. On the other hand, it is important
to keep the InP die size relatively small, in order to leave visible the alignment markers in the

Figure 5.22: Location of the InP-dies on the SOI wafer. For each Si sample, only the most central of the 6 cells is used for the bonding.

Si layer that are placed at the edge of the Si cell, as indicated in Fig. 5.23, as they have to be used for the processing of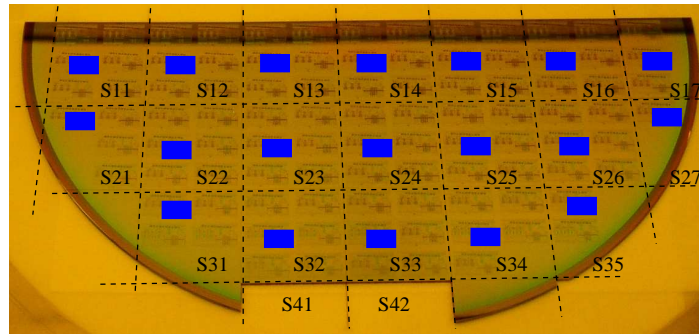 the InP-based layer stack. More specifically, they are used during the first optical lithography to open the Si markers hidden by the InP die. Subsequently, the opened markers are used to accurately perform the mask alignment in the rest of the optical lithography steps.

The details of the MWR chip processing are described in Section 3.3.3. The InP-based die processing is currently under way and therefore only the passive components of the MWR chip have been measured. Below, the measurement techniques and experimental results of these components are presented.

5.3.1 Si passive components

The Si components were measured before the InP die-to-wafer bonding, taking advantage of the heterogeneous integration approach chosen for the chip realization. Fig. 5.24 shows the measurement set-up assembled for the characterization of the Si passive components of the MWR. A broadband light-emitting diode (LED) and a polarization controller (PC) are used to launch transverse electric (TE) polarized light into the cleaved single-mode fiber (SMF) that illuminates a FGC integrated on the chip. The signal propagates through the passive device under test (DUT) and the output signal is coupled via a FGC into an external cleaved SMF connected to either a power-meter or an Optical Spectrum Analyzer (OSA), to measure the optical power transmission and spectrum, respectively.

From previous transmission measurements of SOI waveguides realized in the same technology, the propagation loss is known to be 4-5 dB/cm at 1550 nm [59], while the FGC coupling efficiency was measured to be around 20% at 1550 nm in the MWR chip. The FGC wavelength response can be seen in Fig. 5.25, where the spectrum of straight waveguide coupled to FGCs is plotted (solid line) after correcting for the spectrum of the broadband LED source (dashed line) used in the measurement set-up. This measurement is used for normalizing the transmission plots of the other integrated SOI components.

External markers

mask layout from other designers

8 mm

6 mm

3.5 mm

5 mm

0.5 mm

External markers
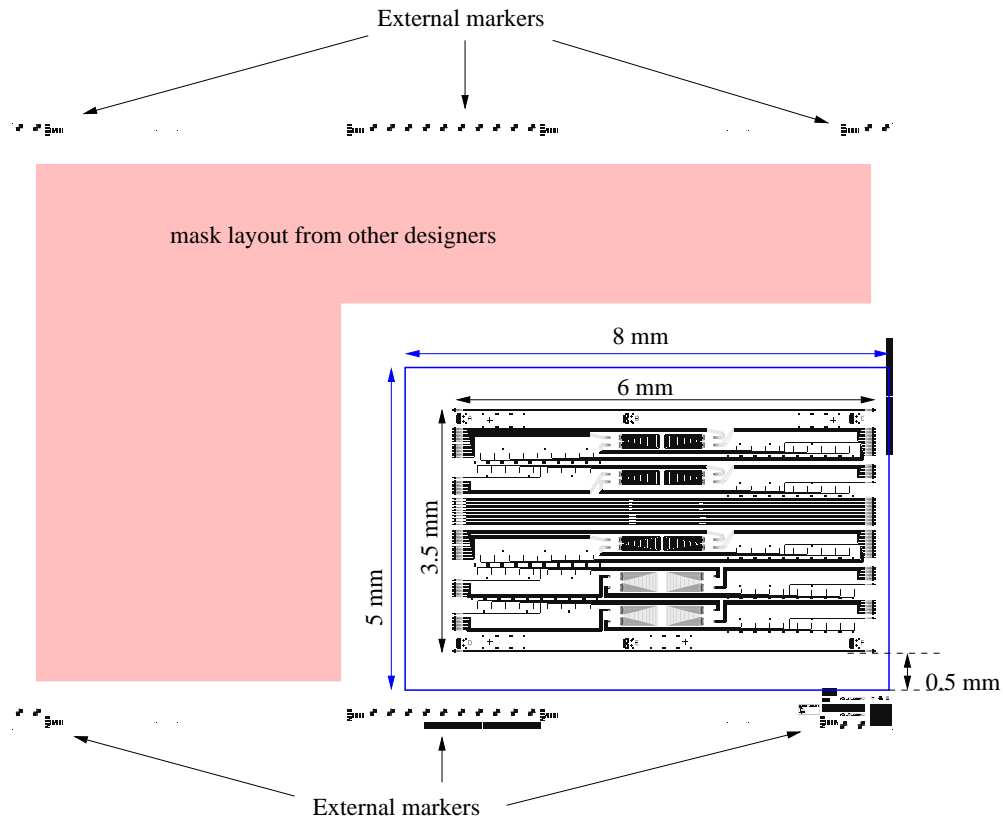
Figure 5.23: InP-die size and position with respect to the Si cell. The $5 \times 8\,\mathrm{mm}^2$ contour line indicates the InP-die. The Si markers at the edge of the Si cell, which are used to the mask alignment in the photonic die lithography steps, are also indicated.

Chip

OSA

DUT

Source   PC   FGC   FGC

Power meter
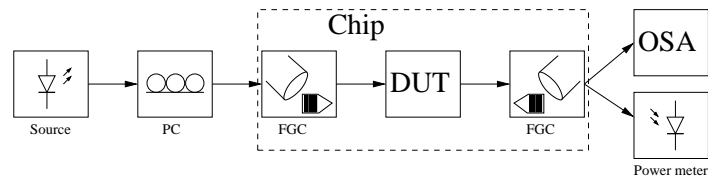
Figure 5.24: Schematic diagram of the set-up used for the measurements of the MWR passive components. A broadband LED and a PC are used to illuminate an FGC integrated on the chip. Thus, the TE-polarized optical signal is coupled into the Si waveguiding layer and propagates through the passive DUT. The output signal is collected by another FGC on the chip and coupled to an SMF connected to a power-meter or to an OSA.
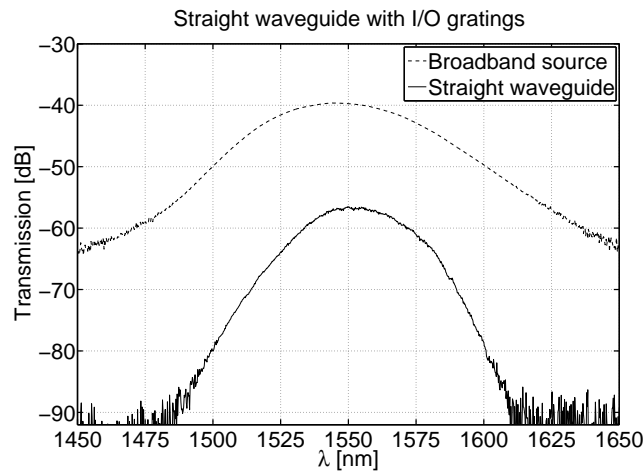
Figure 5.25: Spectrum of a straight waveguide coupled to FGCs (solid line) corrected for the spectrum of the broadband LED source (dashed line) used in the measurement set-up.

Si AWGs

The measurement set-up of Fig. 5.25 is also used for the characterization of the AWGs. The device characterization is performed using only TE-polarized light, as the transverse magnetic (TM) light polarization is filtered by the FGC [77]. As described in Section 5.2.4, the 10 channel MWRs have ten FGC-coupled SOI access waveguides connected to the demux input FPR and ten output waveguides. Nine of the output waveguides end on the SOI chip and are used to route the AWG output signal towards the InP-based photodetectors, while one output waveguide is coupled to an FGC to measure the AWG transmission. The ten FGCs coupled to the input SOI waveguides have a vertical pitch of 20 µm, which causes an optical crosstalk of about −28 dBm, measured between adjacent waveguides and caused by the coupling in the FGCs. Even though this crosstalk level is low, it would compromise the accuracy of the transmission measurements. Therefore, these waveguides are used as output waveguides for the transmission measurements, while the single FGC-coupled MWR output channel is used as an input waveguide (see Fig. 5.26. This is possible thanks to the AWG reciprocity property. Fig. 5.27 and Fig. 5.28 show the spectra recorded for the 10 channel AWG, relative to the transmission through a straight waveguide. A channel spacing of 1.6 nm and an FSR of 16 nm are observed, which perfectly match the device design. The insertion loss, channel crosstalk and non-uniformity are measured to be 3 ± 1 dB, 11 ± 1 dB and 2.5 ± 0.5 dB, respectively, where the spread depends on the device measured and on the reproducibility of the fiber-to-waveguide alignment in the measurement set-up.
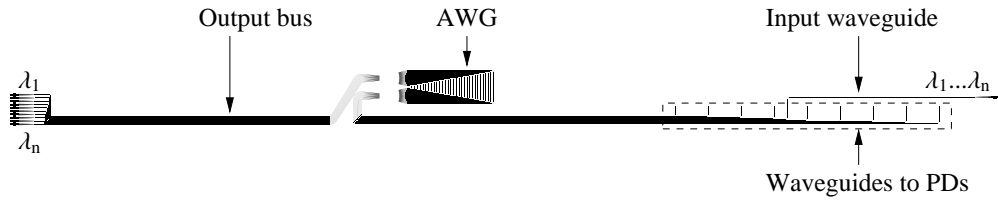
Figure 5.26: The AWG transmission measurements are performed by using the only FGC-coupled MWR output SOI waveguide as the input channel (on the right side of the figure). The demultiplexed broadband signal is collected by the ten FGC-coupled MWR input waveguides (on the left side of the figure).
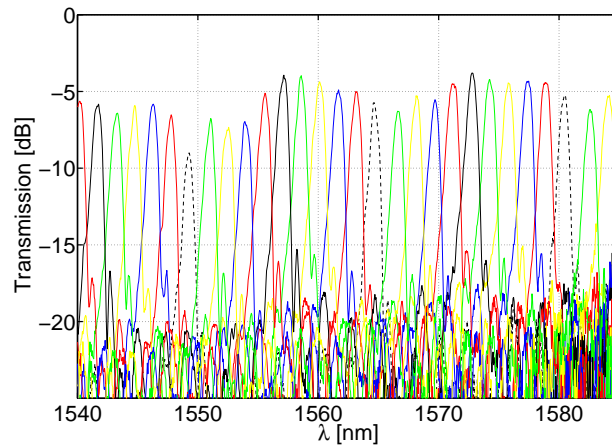
Figure 5.27: AWG recorded spectrum.

5.4 Conclusions

In this chapter, the heterogeneously integrated MWR in InP-on-Si technology has been presented. The device consists of SOI-based passive components, namely waveguides and a demultiplexer structure, and RF InP-based photodetectors. The heterogeneous integration approach used for manufacturing the MWR chip makes the device suitable for use in optical interconnections on Si and benefits from the advantages the SOI and InP technology for the passive and active components, respectively. The SOI technology offers good waveguiding properties and very high integration density thanks to the high light confinement in the SOI waveguide structure core, while the InP-based detectors are more efficient and faster as compared to Si PDs. The receiver demux was implemented as a $700 \times 200\,\mu m^2$ compact AWG. This AWG is a 10 channel demultiplexer, with a channel spacing and FSR of 1.6 and 16 nm,
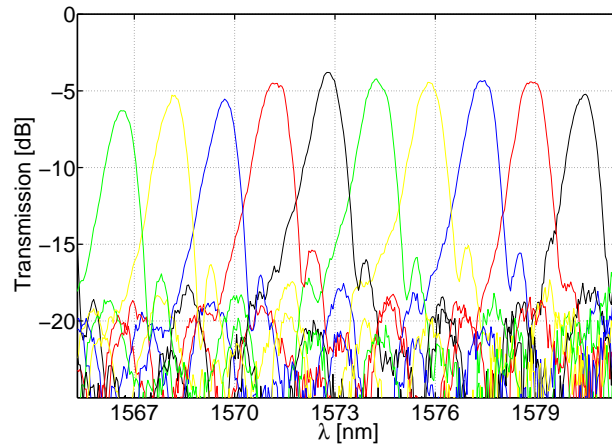
Figure 5.28: AWG recorded spectrum: zoom on one period.

respectively. The ten AWG input waveguides are provided with FGCs, for fiber-to-waveguide light coupling. Nine of the ten output waveguides are connected to integrated InP-based PDs, while the remaining output waveguide is terminated with an FGC and is used for the passive characterization of the demultiplexer. The InP-based p-i-n detector structure is built as a 700 nm n.i.d. InGaAs absorption layer sandwiched by a highly p-doped 50 nm thick InGaAs contact layer and a highly n-doped 220 nm thick InP layer, which is also used for realizing a membrane waveguide aligned over each AWG output SOI waveguide. This membrane waveguide is meant to enhance the detector efficiency by coupling the optical power out of the Si waveguide and bringing it towards the detector absorption region. The InP-based die processing is currently under way and therefore only the passive components of the MWR chip were measured. The Si components were measured before the bonding of the InP-based PDs. The AWG channel spacing and FSR were verified by the recorded device spectra, while the average insertion loss, channel crosstalk and non-uniformity were deduced from the transmission measurements to be 3 dB, 11 dB and 2.5 dB, respectively.

Chapter 6

Conclusions and recommendations

In this chapter the main conclusions of this PhD work are drawn and recommendations for improvement are given.

6.1 Conclusions

With the technology scaling down and the signal switching frequency increasing, three main issues are predicted for the complementary metal-oxide semiconductor (CMOS) integrated circuits (ICs): signal propagation delay, power consumption and integration density. In this thesis, it has been shown how electrical interconnects (EIs) strongly limit these characteristics and the promising solution given by replacing EIs with optical interconnects (OIs) has been discussed. Due to the small feature size, the implementation of intra-chip and chip-to-chip OIs can not rely on optical fibers, but requires the use of photonic integrated circuit (PIC) technology.

Within this work, an InGaAs/InP photodetector (PD) structure for use in OIs on CMOS circuitry was designed, manufactured and characterized. A fabrication technology compatible with Si wafer scale processing was developed, assuring compatibility with future electronic ICs. The technology is based on a heterogeneous integration scheme, in which the PD is manufactured on an InP-based layer stack bonded on a Si wafer, on top of which a Si or a Si_3N_4 interconnect waveguide layer has been defined. The PD structure consists of two parts: an InP membrane input waveguide on top of the bonding layer, meant to efficiently couple the optical signal out of the photonic interconnect waveguide, and the detecting part, a p-i-n heterojunction where the optical signal is detected and converted into an electrical signal. The PD structure was engineered to meet a trade-off between device responsivity and speed. Experimental results for the PDs on SOI waveguides recorded a responsivity of 0.45 A/W and an optical-to-electrical (OE) 3 dB cut-off bandwidth of 33 GHz, limited by the carrier transit-time in the detector depletion region. The characterization of the photodetectors on Si_3N_4 waveguides on CMOS showed a responsivity of 0.7 A/W and an OE 3 dB cut-off frequency

response of 25 GHz.

A heterogeneously integrated 10 channel multiwavelength receiver (MWR) in the InP-on-Si technology was also developed. The device consists of SOI-based passive components, namely waveguides and a demultiplexer structure, and InP-based photodetectors bonded on the processed SOI substrate. The receiver demultiplexer was implemented as a compact arrayed waveguide grating (AWG) defined in the Si waveguide layer, while the InP-based PD structures were integrated to detect the demultiplexed optical signals.

6.2   Recommendations

The detector presented in this thesis was designed to meet a trade-off between device responsivity and speed. A first consideration is that, depending on the needs, either characteristic can be improved at the expense of the other by changing the PD geometry. For instance, thinning down the absorption layer leads to a faster, but less efficient, detector. The trade-off between device responsivity and speed could also be overcome by using a lateral p-i-n detector geometry. Ge-based p-i-n detectors on SOI based on this lateral geometry have been recently reported [91–94]. The advantage of this configuration is that the efficiency is decoupled from the active region thickness and therefore efficiency and speed can be simultaneously optimized. On the other hand, the processing required for this geometry is more complicated as compared to the vertically grown p-i-n structure used here.

The PD employs an input InP-membrane waveguide to increase the device efficiency. Experimental results showed that the InP-membrane coupler had an efficiency of about 50%, caused by the growth of a thinner InP waveguide layer. By optimizing the coupler design, the fabrication tolerances can be relaxed and the efficiency improved. In this work, we already started exploring this option by implementing an improved coupler design in the PD structure employed in the MWR chip. The investigation of couplers based on different coupling mechanisms could also bring to a more tolerant structure: possible structures such as a 45° waveguide mirror or a waveguide grating implemented in the interconnect waveguide layer have been studied [95, 96], even though they require extra processing steps as compared to the membrane coupler we presented.

At a fabrication level, the metallization lithography step could be improved. In the fabricated PDs, the metallization on the top p-contact has a relatively poor coverage of the p-contact window. This increases the carrier drift-time in the n-doped and p-doped regions, thus limiting the bandwidth. This was not a problem for the PD structure developed in this work, as the carrier transit-time in the depletion region provided the dominant bandwidth limitation. However, it could be an issue for detectors that use a very thin active region to boost the speed. The PD metallization can be improved by both optimizing the lithography process parameters (soft-bake, exposure time and post-bake) and correcting the metal pattern geometry in the mask layout.

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Nomenclature

ADS	Advanced Design System
AFM	Atomic Force Microscope
AWG	Arrayed Waveguide Grating
BCB	Benzo-Cyclo-Butene
BPM	Beam Propagation Model
CMOS	COmplementary Metal-Oxide Semiconductor
CMP	Chemical-Mechanical Polishing
COBRA	COmmunication technologies; Basic Research and Applications
CPW	CoPlanar Waveguide
DC	Direct Current
DUT	Device Under Test
DUV	Deep Ultra-Violet
EBL	Electron-Beam Lithoghraphy
EI	Eptical Interconnect
EM	Electromagnetic
EO	Electrical-to-Optical
FD	Finite Difference
FDTD	Finite Difference Time Domain
FGC	Fiber Grating Coupler
FIB	Focused Ion Beam

FMM   Film Mode Matching

FPR   Free Propagation Region

FSR   Free Spectral Range

GSG   Ground-Signal-Ground

ICs   Integrated Circuits

ISI   Inter-Symbol Interference

LCA   Lightwave Component Analyzer

LED   Light-Emitting Diode

MBE   Molecular Beam Epitaxy

MDL   Micro-Disk Laser

MEMPHIS Merging Electronics and Micro & Nano-Photonics in Integrated Systems

MIS   Metal-Insulator-Semiconductor

MMI   Multi-Mode Interference

MOL   Method Of Lines

MOLCAR Method of Lines Complex Arithmetic Routine

MOVPE Metal-Organic Vapor-Phase Epitaxy

MWR   Multi-Wavelength Receiver

n.i.d.   Non Intentionally Doped

OE   Optical-to-Electrical

OI   Optical Interconnect

OSA   Optical Spectrum Analyzer

PC   Polarization Controller

PECVD Plasma Enhanced Chemical Vapor Deposition

PI   Polyimide

PIC   Photonic Integrated Circuit

PICMOS Photonic Interconnect Layer on CMOS

PR   Photoresist

RF   Radio Frequency

RIE   Reactive Ion Etching

RMS   Root Mean Square

rpm   revolutions per minute

sccm   standard cubic centimeters per minute

SEM   Scanning Electron Microscope

SMF   Scattering Matrix Formalism

SMF   Single Mode Fiber

Tbit/s Tera-bit per second

TE   Transverse Electric

TEM   Transverse Electromagnetic

TLS   Tunable Laser Source

TM   Transverse Magnetic

UV   Ultra-Violet

VCSEL   Vertical-Cavity Surface-Emitting Laser

VLSI   Very Large Scale Integration

WASMF   Waveguide Analysis with the use of a Scattering Matrix Formalism

WDM   Wavelength Division Multiplexing

Summary

InP-based Membrane Photodetectors on Si Photonic Circuitry

The work presented in this thesis is about indium phosphide (InP) based photodetectors for use in optical interconnections on silicon (Si) integrated circuits (ICs). The motivation for this work comes from the bottleneck expected at the interconnect level for future generation electronic ICs: with the technology scaling down and the signal switching frequency increasing, three main issues are predicted for the complementary metal-oxide semiconductor (CMOS) ICs, namely signal propagation delay, power consumption and integration density. Electrical interconnects (EIs) strongly limit these characteristics and a promising solution is given by replacing EIs with optical interconnects (OIs). The implementation of intra-chip and chip-to-chip OIs requires the use of photonic integrated circuit (PIC) technology. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry provides bandwidth increase, immunity to electromagnetic (EM) noise and reduction in power consumption. This solution was investigated within this work, which focuses on the detector part. InP-based membrane photodetectors were realized on InP dies bonded on Si and CMOS wafers, on top of which passive Si and Si_3N_4 photonic circuitry had been defined. This approach combines the advantages of high quality Si-based passive circuits with the excellent properties of InP-based components for light generation and detection. The technology used for the InP device fabrication is compatible with wafer scale processing steps, assuring compatibility towards future generation electronic ICs. The major results of this work are summarized as follows: InP membrane couplers and detectors were successfully fabricated on Si and Si_3N_4 photonic circuits. Experimental results show working active and passive devices, namely: passive Si photonic components (waveguides, MMIs, (de)-multiplexers), InP membrane couplers, InP-based detectors and heterogeneously integrated multiwavelength receivers. A working laser-to-detector integrated optical link on Si was successfully demonstrated. This work was carried out with the support of the European project IST-PICMOS and of the Dutch Ministry of Economic Affairs through the Smartmix Memphis project.

Pietro Binetti

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Thank you all,

Pietro

Curriculum Vitæ

Pietro Binetti was born in Bologna, Italy, in 1979. He received his M.Sc. degree in electrical engineering from the University of Bologna, Italy, in 2004. His M.Sc. thesis project was carried out at the COBRA research institute, Eindhoven University of Technology, The Netherlands, on the characterization of photonic integrated circuits. In 2004, he started working in the same institute as a Ph.D. student on InP-based photodetectors for use in optical interconnections on Si.

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