# Design and debugging of multi-step analog to digital converters 

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## DESIGN AND DEBUGGING OF MULTI-STEP ANALOG TO DIGITAL CONVERTERS

Amir Zjajo

The work described in this thesis has been carried out at the Philips Research Laboratories and Corporate Research of NXP Semiconductors, both in Eindhoven, The Netherlands, as part of the Philips Research and NXP Semiconductors Research Program

Front cover: A/D converter described in this thesis

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# DESIGN AND DEBUGGING OF MULTI-STEP ANALOG TO DIGITAL CONVERTERS 

## PROEFSCHRIFT

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door

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prof.dr. J. Pineda de Gyvez

70 my father

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## LIST OF ABBREVATIONS

| A/D | Analog to Digital |
| :--- | :--- |
| ADC | Analog to Digital Converter |
| ADSL | Asynchronous DSL |
| ATE | Automatic Test Equipment |
| ATPG | Automatic Test Pattern Generator |
| BIST | Built-In Self-Test |
| CAD | Computer Aided Design |
| CDMA | Code Division Multiple Access |
| CMFB | Common-Mode Feedback |
| CMOS | Complementary MOS |
| CMRR | Common-Mode Rejection Ratio |
| CPU | Central Processing Unit |
| D/A | Digital to Analog |
| DAC | Digital to Analog Converter |
| DAE | Differential Algebraic Equations |
| DEM | Dynamic Element Matching |
| DFT | Discrete Fourier Transform |
| DfT | Design for Testability |
| DIBL | Drain-Induced Barrier Lowering |
| DLPM | Die-Level Process Monitor |
| DMT | Discrete Multi Tone |
| DNL | Differential Non-Linearity |
| DR | Dynamic Range |
| DSL | Digital Subscriber Line |
| DSP | Digital Signal Processor |
| DTFT | Discrete Time Fourier Transform |
| DUT | Device under Test |
| EM | Expectation-Maximization |
| ENOB | Effective Number of Bits |
| ERBW | Effective Resolution Bandwidth |
| ESSCIRC | European Solid-State Circuit Conference |
| FFT | Fast Fourier Transform |
| FoM | Figure of Merit |
| FPGA | Field Programmable Gate Array |
| GBW | Gain-Bandwidth Product System for Mobile Communication |
| GSM |  |
|  |  |
|  |  |


| IC | Integrated Circuit |
| :---: | :---: |
| IF | Intermediate Frequency |
| INL | Integral Non-Linearity |
| IP | Intellectual Property |
| ISDN | Integrated Services Digital Network |
| ISSCC | International Solid-State Circuit Conference |
| ITDFT | Inverse Time Discrete Fourier Transform |
| KCL | Kirchhoff Current Law |
| LMS | Least Mean Square |
| LSB | Least Significant Bit |
| ML | Maximum Likelihood |
| MNA | Modified Nodal Analysis |
| MOS | Metal Oxide Semiconductor |
| MOSFET | Metal Oxide Semiconductor Field Emitter Transistor |
| MSE | Mean Square Error |
| MSB | Most Significant Bit |
| NMOS | Negative doped MOS |
| OFDM | Orthogonal Frequency Division Multiplex |
| OTA | Operational Transconductance Amplifier |
| PCB | Printed Circuit Board |
| PCM | Process Control Monitoring |
| PDF | Probability Density Function |
| PGA | Programmable Gain Amplifier |
| PLL | Phase Locked Loop |
| PMOS | Positive doped MOS |
| PSK | Phase Shift Keying |
| PSRR | Power Supply Rejection Ratio |
| PTAT | Proportional to Absolute Temperature |
| RF | Radio Frequency |
| RSD | Redundant Sign Digit |
| S/H | Sample and Hold |
| SDM | Steepest Descent Method |
| SC | Switched Capacitor |
| SEIR | Stimulus Error Identification and Removal |
| SFDR | Spurious Free Dynamic Range |
| SINAD | Signal to Noise and Distortion |
| SNR | Signal to Noise Ratio |
| SNDR | Signal to Noise plus Distortion Ratio |
| SoC | System on Chip |
| SR | Slew Rate |
| SVM | Support Vector Machine |
| THD | Total Harmonic Distortion |
| UMTS | Universal Mobile Telecommunication System |
| VGA | Variable Gain Amplifier |
| VLSI | Very Large-Scale Integrated Circuit |
| WCDMA | Wideband Code Division Multiple Access |
| WLAN | Wireless Local Area Network |
| xDSL | HDSL, ADSL, VDSL, ... |

## LIST OF SYMBOLS

| $a$ | Elements of the incidence matrix $A$ |
| :--- | :--- |
| $A^{\prime}$ | Amplitude, area, amplifier voltage gain, incidence matrix |
| $A_{f}$ | Voltage gain of feedback amplifier |
| $A_{0}$ | Open loop $d c$ gain |
| $b$ | Number of circuit branches |
| $B_{i}$ | Number of output codes |
| $B$ | Bit, effective stage resolution |
| $B_{n}$ | Noise bandwidth |
| $c_{i}$ | class to which the data $x_{i}$ from the input vector belongs |
| $c_{x y}$ | Process correction factors depending upon the process maturity |
| $c_{b(i)}$ | Highest achieved normalized fault coverage |
| $C^{*}$ | Neyman-Pearson Critical region |
| $C$ | Capacitance, covariance matrix |
| $C_{C}$ | Compensation capacitance, cumulative coverage |
| $C_{e f f}$ | Effective capacitance |
| $C_{F}$ | Feedback capacitance |
| $C_{G}$ | Gate capacitance, input capacitance of the operational amplifier |
| $C_{G S}$ | Gate-Source capacitance |
| $C_{H}$ | Hold capacitance |
| $C_{i n}$ | Input capacitance |
| $C_{L}$ | Load capacitance |
| $C_{o u t}$ | Parasitic output capacitance |
| $C_{o x}$ | Gate-oxide capacitance |
| $C_{p a r}$ | Parasitic capacitance |
| $C_{t o t}$ | Total load capacitance |
| $C_{Q}$ | Function of the deterministic initial solution |
| $C_{\Xi \Xi}$ | Autocorrelation matrix |
| $C_{S S}$ | Symmetrical covariance matrix |
| $C_{H}$ | Cumulative histogram |
| $d_{i}$ | Location of transistor $i$ on the die with respect to a point of origin |
| $D_{i}$ | Multiplier of reference voltage |
| $D_{o u t}$ | Digital output |
| $D_{T}$ | Total number of devices |
| $e$ | Noise, error, scaling parameter of transistor current |
| $e_{q}$ | Quantization error |
|  |  |


| $e^{2}$ | Noise power |
| :---: | :---: |
| $E_{\text {conv }}$ | Energy per conversion step |
| $f_{\text {clle }}$ | Clock frequency |
| $f_{\text {in }}$ | Input frequency |
| $f_{p, n}\left(d_{i}\right)$ | Eigenfunctions of the covariance matrix |
| $f_{s}$ | Sampling frequency |
| $f_{\text {sig }}$ | Signal frequency |
| $f_{\text {fpur }}$ | Frequency of spurious tone |
| $f_{T}$ | Transit frequency |
| $F_{F}$ | Folding factor |
| $F_{Q}$ | Function of the deterministic initial solution |
| $g$ | Conductance |
| $G_{i}$ | Interstage gain |
| $G_{k}$ | Fourier series coefficient of gain mismatch |
| $G_{m}$ | Transconductance |
| i | Index, circuit node, transistor on the die |
| I | Current |
| $I_{\text {amp }}$ | Total amplifier current consumption |
| $I_{D}$ | Drain current |
| $I_{D D}$ | Power supply current |
| $I_{r e f}$ | Reference current |
| $j$ | Index, circuit branch |
| $J_{0}$ | Jacobian of the initial data $\chi_{0}$ evaluated at $p_{i}$ |
| k | Boltzmann's coefficient, error correction coefficient, index |
| K | Amplifier current gain, gain error correction coefficient |
| 10 | Likelihood function |
| L | Channel length |
| $L_{R}$ | Length of the measurement record |
| $L\left(\theta \mid T_{X}\right)$ | Log-likehood of parameter $\theta$ with respect to input set $T_{X}$ |
| $m$ | Number of different stage resolutions, index |
| M | Number of terms |
| $n$ | Index, number of circuit nodes, number of faults in a list |
| N | Number of bits, number of parallel channels, noise power |
| $N_{\text {aperture }}$ | Aperture jitter limited resolution |
| $P$ | Power |
| $p$ | Process parameter |
| $p\left(d_{i}, \theta\right)$ | Stochastic process corresponding to process parameter $p$ |
| $p_{X \mid \Theta}(x \mid \theta)$ | Gaussian mixture model |
| $p^{*}$ | Process parameter deviations from their corresponding nominal values |
| $p_{1}$ | Dominant pole of amplifier |
| $p_{2}$ | Non-dominant pole of amplifier |
| 9 | Channel charge, circuit nodes, index |
| Q | Quality factor |
| $Q_{i}$ | Number of quantization steps, cumulative probability |
| $Q(x)$ | Normal accumulation probability function |
| $Q\left(\theta \mid \theta^{(t)}\right)$ | Auxiliary function in EM algorithm |
| $r$ | Resolution, resistance, circuit nodes |
| R | Resistance |


| $r_{\text {ds }}$ | Output resistance of a transistor |
| :---: | :---: |
| $\mathrm{R}_{\text {eff }}$ | Effective thermal resistance |
| $\mathrm{R}_{\text {on }}$ | Switch on-resistance |
| $r_{\text {out }}$ | Amplifier output resistance |
| $\mathrm{R}_{\text {ref }}$ | Reference value (current or voltage) |
| $s$ | Scaling parameter of transistor size, observed converter stage |
| $t$ | Time |
| T | Absolute temperature, sampling period, transpose, test, test stimuli |
| $t_{0 x}$ | Oxide thickness |
| ts | Sampling time |
| $v_{f}$ | Fractional part of the analog input signal |
| $U B_{i}$ | Upperbound of the ith level |
| $V$ | Voltage |
| $V_{D D}$ | Positive supply voltage |
| $V_{D S}$ | Drain-source voltage |
| $V_{\text {DS,SAT }}$ | Drain-source saturation voltage |
| $V_{\text {FS }}$ | Full-scale voltage |
| $V_{G S}$ | Gate-source voltage |
| $V_{b e}$ | Base-emitter voltage |
| $V_{\text {in }}$ | Input voltage |
| $V_{[k]}$ | Fourier series coefficient of offset mismatch |
| $V_{L S B}$ | Voltage corresponding to the least significant bit |
| $V_{\text {margin }}$ | Safety margin of drain-source saturation voltage |
| $V_{\text {off }}$ | Offset voltage |
| $V_{\text {ped }}$ | Pedestal voltage |
| $V_{\text {res }}$ | Residue voltage |
| $V_{T}$ | Threshold voltage |
| w | Normal vector perpendicular to the hyperplane, weight |
| $w_{i}$ | Cost of applying test stimuli performing test number $i$ |
| W | Channel width, parameter vector, loss function |
| $W^{*}, L^{*}$ | Geometrical deformation due to manufacturing variations |
| $x_{i}$ | Vectors of observations |
| $x(t)$ | Analog input signal |
| $X$ | Input |
| $y_{0}$ | Arbitrary initial state of the circuit |
| $y[k]$ | Output digital signal |
| Y | Output, yield |
| 20 | Nominal voltages and currents |
| $2(1-\alpha)$ | (1- $\alpha$ )-quantile of the standard normal distribution $Z$ |
| $r[k]$ | Reconstructed output signal |
| $\alpha$ | Neyman-Pearson significance level, weight vector of the training set |
| $\beta$ | Feedback factor, transistor current gain |
| $\gamma$ | Noise excess factor, measurement correction factor, reference errors |
| $\delta$ | Relative mismatch |
| $\delta_{\text {ramp }}$ | Slop of the ramp signal for given full-scale-range $V_{\text {FS }}$ |
| $\varepsilon$ | Error |
| $\zeta$ | Samples per code, forgetting factor |


| $\eta$ | Distance based weight term, stage gain errors |
| :---: | :---: |
| $\theta$ | Die, unknown parameter vector |
| $\vartheta_{p, n}$ | Eigenvalues of the covariance matrix |
| $\kappa$ | Converter transition code |
| $\lambda$ | Threshold of significance level $\alpha$, decision stage offset error |
| $\lambda_{\kappa}$ | Central value of the transition band |
| $\mu$ | Carrier mobility, mean value, iteration step size |
| $v$ | Fitting parameter estimated from the extracted data |
| $\xi_{i}$ | measure the degree of misclassification of the data $x_{i}$ |
| $\xi_{n}(\theta)$ | Vector of zero-mean uncorrelated Gaussian random variables |
| $\rho$ | Correlation parameter reflecting the spatial scale of clustering |
| $\varsigma_{p}$ | Random vector accounting for device tolerances |
| $\sigma$ | Standard deviation |
| $\sigma_{a}$ | Gain mismatch standard deviation |
| $\sigma_{b}$ | Bandwidth mismatch standard deviation |
| $\sigma_{d}$ | Offset mismatch standard deviation |
| $\sigma_{r}$ | Time mismatch standard deviation |
| $\tau$ | Time constant |
| $\phi$ | Flux stored in inductors |
| $\varphi$ | Clock phase |
| $\chi$ | Circuit dependent proportionality factor |
| $\omega_{S}$ | Dominant pole frequency, angular sampling frequency |
| $\omega_{G B W}$ | Angular gain-bandwidth frequency |
| $\Gamma_{r, f}[$. | Probability function |
| $\Delta$ | Relative deviation |
| $\Delta_{b i}$ | Bandwidth error parameter in $i$ th channel |
| $\Delta_{g i}$ | Gain error parameter in $i$ th channel |
| $\Delta_{o i}$ | Offset error parameter in $i$ th channel |
| $\Delta_{t i}$ | Time error parameter in $i$ th channel |
| $\Lambda$ | Linearity of the ramp |
| $\Xi$ | Quasi-static fault model |
| $\Xi_{r}$ | Boundaries of quasi-static node voltage |
| $\Omega$ | Sample space of the test statistics |

## CHAPTER 1.

## INTRODUCTION

### 1.1. A/D Conversion Systems

Analog-to-digital (A/D) conversion and digital-to-analog (D/A) conversion lie at the heart of most modern signal processing systems where digital circuitry performs the bulk of the complex signal manipulation. As digital signal processing (DSP) integrated circuits become increasingly sophisticated and attain higher operating speeds more processing functions are performed in the digital domain. Driven by the enhanced capability of DSP circuits, $\mathrm{A} / \mathrm{D}$ converters (ADCs) must operate at ever-increasing frequencies while maintaining accuracy previously obtainable at only moderate speeds. This trend has several motivations and poses important consequences for analog circuit design. The motivations for processing most signals digitally are manifold: digital circuits are much less expensive to design, test, and manufacture than their analog counterparts; many signal processing operations are more easily performed digitally; digital implementations offer flexibility through programmability; and digital circuitry exhibits superior dynamic range, thereby better preserving signal fidelity. As a consequence of the aforementioned advantages accrued by DSP, fewer and fewer operations benefit from analog solutions. Since A/D conversion generally requires more power and circuit complexity than D/A conversion to achieve a given speed and resolution, ADCs frequently limit performance in signal processing systems. This fact underscores the second consequence of enhanced DSP performance on the role of analog circuit design. That is, since A/D conversion limits overall system performance, development of improved A/D conversion algorithms and circuitry represents an extremely important area of research for the foreseeable future.

Propelling the great venture and unprecedented success of digital techniques, the CMOS technology has emerged and dominated the mainstream silicon IC industry in the last few decades. As the lithography technology improved, the MOS device dimensions have reduced its minimum feature size over the last forty years and greatly impacted the performance of digital integrated circuits. During the course of pursuing a higher level of system integration and lower cost, the economics has driven technology to seek solutions to integrate analog and digital functionalities on a single die using the same or compatible fabrication processes. With the inexorable scaling of the MOS transistors, the raw device speed takes great leaps over time, measured by the exponential increase of the transit frequency $f_{T}$ - the frequency where a transistor still yields a current gain of unity. The advancement of technology culminated in a dramatic performance improvement of CMOS analog circuits, opening an avenue to achieve system integration using a pure CMOS technology. Process enhancements, such as the triple-well option, even helped to
reduce the noise crosstalk problem - one of the major practical limitations of sharing the substrate of precision analog circuits with noisy digital logic gates. As CMOS integrated circuits are moving into unprecedented operating frequencies and accomplishing unprecedented integration levels (Figure 1-1), potential problems associated with device scaling - the short-channel effects - are also looming large as technology strides into the deep-submicron regime. Besides that it is costly to add sophisticated process options to control these side effects, the compact device modeling of short-channel transistors has become a major challenge for device physicists. In addition, the loss of certain device characteristics, such as the square-law $I-V$ relationship, adversely affects the portability of the circuits designed in an older generation of technology. Smaller transistors also exhibit relatively larger statistical variations of many device parameters (i.e., doping density, oxide thickness, threshold voltage etc.). The resultant large spread of the device characteristics also causes severe yield problems for both analog and digital circuits.


Figure 1-1: a) Left, first working integrated circuit, 1958, (Copyrighto Texas Instruments: source-www.ti.compublic domain), b) Middle, revolutionary Intel Pentium processor fabricated in $0.8 \mu \mathrm{~m}$ technology containing 3.1 million transistors, 1993, c) Right, Intel's 45-nanometer test chip containing over a billion transistors, 2008 (Copyright ${ }^{\circ}$ Intel Corporation: source-www.intel.com-public domain)

The analog-to-digital interface circuit in highly integrated CMOS wireless transceivers exhibits keen sensitivity to technology scaling. The trend toward more digital signalprocessing for multi-standard agility in receiver designs has recently created a great demand for low-power, low-voltage analog-to-digital converters (ADCs) that can be realized in a mainstream deep-submicron CMOS technology. Intended for embedded applications, the specifications of such converters emphasize high dynamic range and low spurious spectral performance. In a CMOS radio SoC, regardless of whether frequency translation is accomplished with a single conversion, e.g., the direct-conversion and lowIF architecture, or a wideband-IF double conversion and low-IF architecture, or a wide-band-IF double conversion, the lack of high-Q on-chip IF channel-select filters inevitably leads to a large dynamic range imposed on the baseband circuits in the presence of in-band blockers (strong adjacent channel interference signals). For example, the worstcase blocking specifications of some wireless standards, such as GSM, dictate a conversion linearity of twelve bits or more to avoid losing a weak received signal due to distortion artifacts. Recent works also underline the trend toward the IF digitizing architecture to enhance programmability and to achieve a more digital receiver. However, advancing the digitizing interface toward the antenna exacerbates the existing dynamic range problem, as it also requires a high oversampling ratio. To achieve high linearity, high dynamic range, and high sampling speed simultaneously under low supply voltages in deepsubmicron CMOS technology with low power consumption has thus far been conceived of as extremely challenging.

A typical analog-to-digital and digital-to-analog interface in a digital system is depicted in Figure 1-2. The majority of signals encountered in nature are continuous in both time and amplitude. The analog-to-digital converter (ADC) converts analog signals to discrete time digitally coded form for digital processing and transmission. Usually analog-to-digital conversion includes two major processes: sampling and quantization, as shown in the sub-blocks in the figure. The bandwidth of the analog input signal is limited to the Nyquist frequency by means of an anti-alias filter. This band-limited signal is then fed to the sample-and-hold stage that performs the first step towards a digital signal. The input signal that has been continuous in time is converted to a discrete-time signal. The amplitude, however, remains continuous after the sample-and-hold stage. The quantization of the amplitude is performed by the $\mathrm{A} / \mathrm{D}$ converter. While during the conversion of a continuous-time signal to a discrete-time signal no information is lost if the signal is band-limited to the Nyquist frequency, the amplitude quantization that maps a continuous signal to a finite number of discrete values inevitably causes a decrease of information such that a complete reconstruction of the signal is not possible any more. The A/D converter thus limits the accuracy and the dynamic range of the entire system; the design of the converter must therefore be carried out with special care.


Figure 1-2: A typical digital system with analog input and output quantities

The output of the A/D converter consists of digital data that represents the analog input signal apart from the limitations mentioned above. A digital system processes this data. This system can be as simple as a single digital filter, but can also be as complex as e.g., a digital telephone system. In either case the resulting output is also digital data that has to be converted back to the analog domain, which is performed by the digital-to-analog (D/A) converter, whose output is an analog, but still discrete-time signal. A reconstruction filter finally creates the continuous-time output signal. Although the entire system seems to be very complex, it has a number of advantages over purely analog signal processing. The most obvious advantage is the flexibility of the system. As mentioned above, the digital signal processing block can perform any function, from very simple to very complex. Many tasks that are complicated to achieve in the analog domain, such as storing large amounts of data, are comparatively easy in the digital domain. Moreover, the entire system can be made programmable or even adaptive to the current situation. In an analog signal processing system, the addition of functionality often degrades the signal. Any filtering stage, e.g., that is added to the signal path also adds noise to the signal and thus reduces the dynamic range. In a digital system, however, the losses are small once the analog signal is converted to the digital domain, no matter how complex the operations are that are performed with the digital data.

A/D converters are widely used in numerous applications (Table I). Recently, the applications for A/D converters have expanded widely as many electronic systems that used to be entirely analog have been implemented using digital electronics. Examples of such applications include digital telephone transmission, cordless phones, transportation, and medical imaging. Consumer products, such as high-fidelity audio and image processing, require very high resolution, while advanced radar systems and satellite communications
with ultra-wide-bandwidth require very high sampling rates (above 1 GHz ). Advanced radar, surveillance, and intelligence systems, which demand even higher frequency and wider bandwidth, would benefit significantly from high resolution A/D converters having broad bandwidths.

| Medical imaging | Antenna Array Position | Portable instrumentation (battery) |
| :--- | :--- | :--- |
| Positron Emission Tomography | IF sampling | Handheld oscilloscope |
| MRI receivers | CDMA2k, WCDMA, TD-SCDMA. | Digital oscilloscope |
| Nondestructive ultrasound | IS95, CDMA-One, IMT2000 | Spectrum analyzers |
| Ultrasound | BS Infrastructure | Communications instrumentation |
| Ultrasound beam forming system | AMPS, IS136, (W)-CDMA, GSM | Instrumentation |
| X-ray imaging | Direct Conversion | Radar, Infrared Imaging |
| Medical scan converters | Digital Receiver Single Channel | Radar, Sonar and Satellite Subsystems |
| Optical networking | Communication Subsystem | Power-sensitive military applications |
| Broadband access | Wideband Carrier Frequency System | Astronomy |
| Broadband LAN | Point to Point Radio | Flat panel displays |
| Communications (modems) | GPS Anti-jamming Receiver | Projection systems |
| Powerline networking | MMDS base station | CCD imaging |
| Home phone networking | Wireless Local Loop (WLL) | Set-Top Boxes |
| Wireless Local Loop, Fixed Access | I \& Q Communications | Vsat terminal / receiver |
| WLAN | DSP front-end | Multimedia |
| VDSL, XDSL \& HPNA | Tape drives | Film Scanners |
| Power amplifier linearization | Phased Array Receivers | Data Acquisition |
| Broadband wireless | Secure Communications | Bill Validation |
| Quadrature radio receivers | Digital Receivers | Motor Control |
| Cable Reverse Path | Antenna array processing | Industrial Process Control |
| Communications receivers | Antenna array processing | Optical Sensor |
| Diversity radio receivers | Digital Receivers | Cable Head-End Systems |
| Viterbi decoders | Video Imaging | Test \& measurement equipment |

TABLE I - A/D CONVERTER's FULL APPLICATION SCOPE

### 1.2. Remarks on Curent Design and Debugging Practice

Reduction of the power dissipation associated with high speed sampling and quantization is a major problem in many applications, including portable video devices such as camcorders, cellular phones, personal communication devices such as wireless LAN transceivers, in the read channels of magnetic storage devices using digital data detection, and many others. With the rapid growth of internet and information-on-demand, handheld wireless terminals are becoming increasingly popular. With limited energy in a reasonable size battery this level of power consumption may not be suitable and further power reduction is essential for power-optimized A/D interfaces. The trend of increasing integration level for integrated circuits has forced the A/D converter interface to reside on the same silicon in complex mixed-signal ICs containing mostly digital blocks for DSP and control. The use of the same supply voltage for both analog and digital circuits can give advantages in reducing the overall system cost by eliminating the need of generating multiple supply voltages with $d c-d c$ converters. However, specifications of the converters in various applications, such as communication applications emphasize high dynamic range and low spurious spectral performance. It is nontrivial to achieve this level of linearity in a monolithic environment where post-fabrication component trimming or calibration is cumbersome to implement for certain applications or/and for cost and manufacturability reasons. Another hurdle to achieve full system integration stems from the power efficiency of the A/D interface circuits supplied by a low voltage dictated by the gate-oxide reliability of the deeply scaled digital CMOS devices.

Similarly, the integrated circuits (ICs) manufacturing process in itself is neither deterministic nor fully controllable. Microscopic particles present in the manufacturing environment and slight variations in the parameters of manufacturing steps can all lead to the geometrical and electrical properties of an IC to deviate from those generated at the end of the design process. Those defects can cause various types of malfunctioning, depending on the IC topology and the nature of the defect. Silicon wafers produced in a semiconductor fabrication facility routinely go through electrical and optical measurements to determine how well the electrical parameters fit within the allowed limits. These measurements are augmented with process control monitoring (PCM) data. The information obtained is than used in the Fab to decide if some wafer process layers need to be reworked and if the devices should be tested by a special characterization at the back end of the line to make certain that their electrical operating values meet the a priori specifications, e.g. temperature range, durability, speed, etc.

Various models have been constructed for estimating the device yield of a wafer - usually based on the die size, process linewidth, and particle accumulation. The yield is determined by the outcome of the wafer probing (electrical testing), carried out before wafer dicing. The functional testing of mixed-signal devices is very thorough, and much information can be acquired about circuit failure blocks and mechanisms based on these test results. The simplest form of yield information is the aggregate pass/fail statistics of the device, where the yield is usually expressed as a percentage of good dice per all dice on the wafer to make process and product comparisons easier. In principle, yield loss can be caused by several factors, e.g. wafer defects and contamination, IC manufacturing process defects and contamination, process variations, packaging problems, and design errors or inconsiderate design implementations or methods. Constant testing in various stages is of utmost importance for minimizing costs and improving quality.

Early discovering the presence of a defect chip is therefore most desirable as the cost of detecting a bad component in a manufactured part increases tenfold at each level of assembly. In the semiconductor industry, although the cost to fabricate a transistor has fallen dramatically, at the same time, the cost of testing each transistor has remained relatively stable. As a result, it is expected that testing a transistor in the near future (around 2012) will cost the same amount of money as manufacturing it. In general, for a fault-free die, the IC test cost is given by the costs of running the tester per unit time multiplied by the total test time per IC. However, for a given industrial test facility, consisting of ATE and prober or handler, and a given test yield, the test cost parameters are the test time of a fault-free product and the average test time of a faulty product. For the average cost of testing a die, the parameters test yield and average test time of a faulty die must also be taken into account. The test time of a fault-free die is the total time the complete test program takes to measure and process measurement data. The fact that the test time of a faulty die plays also a role implies that the tests should be ordered according to their success in detecting defects.

It should also be noted that wafer loading or package handling times are also important parameters for test time. In the situations where the handling times are comparable with the test time, decreasing the test length will obviously not be sufficient. In these cases alternative solutions such as multisite testing have to be applied, in order to make use of (a part of) the handling time to test another IC. The remaining factor, the test yield, depends on the process yield and the presence of test and measurement errors.

It becomes clear from the discussion of cost and quality issues of an IC that having tests with high fault coverage can improve both the quality and the cost figures. With the increasing demand for low defect levels, it is imperative that the effects of all possible process parameter variations be modeled and tested for. These defects are highly dependent on the type of process, and their effect on the overall circuit behavior depends on the design's process tolerance. The list of possible faults for an integrated circuit is in fact infinite, but by considering only the most likely faults, a finite set can be created. To develop realistic fault model various types of failures, their causes and effects should be considered. Parametric variations (measured in terms of their standard deviation $\sigma$ ) arise due to statistical fluctuations in process parameters such as oxide thickness, doping, line width, and mask misalignment. The effect varies from complete malfunction of the circuit (catastrophic), to marginally out-of-specification performance of some circuit parameters (e.g. gain, linearity), to performance that may even lie within given specifications but poses a reliability risk. Typically, process monitor circuits on each wafer are tested to ensure that all key process parameters are well within specifications so that the as yet untested chips on the wafer can be assumed to be free of excessive process variation. Nevertheless, process variations local to a chip (or to a circuit within a chip) might be out of specification.

| Defect (cause) | Fault (effect) |  |  |
| :---: | :---: | :---: | :---: |
|  | Within specification limits | Parametric fail | Catastrophic fail |
| Process parameters within specification limits | Defect-free and fault-free | Specific design can not account for all possible parameter combinations for all possible conditions | Oversight in design, example: insufficient phase margin for combination of process parameters |
| Process parameter out of specification limits | Reliability risk, example: intermetal dielectric that is too thin | Classic parametric faults and soft faults | Example: a low $V_{T}$ causing a transistor to not turn off |
| Shorts and Opens | Occur due to unspecified performances, example: a short circuit that causes excessive current while circuit remains within specification | Marginally fail a specification, example: a short circuit in flash A/D converter resistor chain causing a few incorrect output codes | Classic catastrophic and hard faults |

TABLE II - CATEGORIES OF DEFECTS AND FAULTS
Table II shows all-comprising list of defects and faults. The rows correspond to the manufacturing process defect that caused the fault, ranging from global process variation to local variation and shorts and opens. The columns correspond to the impact of the defect on the performance of the circuit under test, ranging from parametric failure to catastrophic failure. The most likely parametric faults that are also difficult to test are of most significance. A test set is having $100 \%$ fault coverage if a circuit, which passes the test, meets all performance specifications at all operating conditions. Defects, which cause no specification failure, but may reduce reliability can be distinguished in three failure regimes: early, where the products show a high, but decreasing failure rate as a function of time until the failure rate stabilizes, random failure period and wear-out period, where the failure rate increases again when end-of-life of the products is reached. The nature of the failures in the three periods is generally very different. The majority of the failures in the early failure period are caused by manufacturing defects like near opens and shorts in metal lines, weak spots in isolating dielectrics or poorly bonded bondwires in the package. In the random failure period many different rootcauses occur but failures related to specific events like lightning, load dump spikes occurring during disconnection of car batteries or other overstress situations are most notable. Failures in the wear-out period are related to intrinsic properties of the materials and devices used in the product in combination with the product use conditions like temperature, voltage and currents
including their time dependence. Examples of wear-out failure mechanisms are electromigration, (gate) oxide breakdown, hot carrier degradation and mobile ion contamination. Reliability engineering, which deals with on one hand systematically reducing the infant mortality and random failures and on the other hand keeping the wear-out phase beyond practical duration is beyond the scope of this thesis and it will not be further discussed.

Another test-related factor that contributes indirectly to the cost of an IC is the area contribution of the built-in self-test (BIST) and design for testability (DfT) circuitry. In fact, adding BIST and DfT in an efficient way can help decrease the test development and debugging costs, thereby compensating for at least a part of the additional area cost. Finally, on-line debugging of tests has also often been pointed out as a cost factor, because of the high costs of operating the expensive ATE. Some ATE manufacturers supply debugging software for off-line debugging, but the debugging of the device under test (DUT) is still performed for a large part on-line. Standardization in terms of tester and interface board models have not been achieved yet for mixed-signal circuits.

Historically, digital and analog testing have developed at very different paces, causing analog test methodology to be in a far earlier stage today than its digital counterpart. Computer aided design (CAD) tools for automatic test generation and test circuitry insertion are available already since two decades for digital circuits. The main reason for this is the ease of formulating the test generation as a mathematical problem due to the discrete signal and time values. The distinction between what does and what does not work is evident for digital circuitry. For analog designs, the definition of fault-free and faulty circuits is much more a matter of specification thresholds and sensitivity of application than a sharp distinction as in the case of digital circuits. In analog signal processing circuits there are not only two choices of signal values to choose from, but in principle an infinite number of signal values are possible. Similarly, the time variation properties of analog signals bring an extra dimension to the problem. Additionally, the propagation of fault effects to the output is not possible in the digital sense, since the fault effect propagates in all directions and the calculation of this propagation pattern becomes therefore much more complex than in the digital case. The information that a fault is present at a certain node does not readily comprise the signal value information for that node, making time consuming calculations of signal values necessary. Nonlinearity, loading between circuit blocks, presence of energy-storing components and parasitics further complicate these calculations.

### 1.3. Motivation

With the fast advancement of CMOS fabrication technology, more and more signalprocessing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. This has recently generated a great demand for low-power, low-voltage A/D converters that can be realized in a mainstream deep-submicron CMOS technology. However, the discrepancies between lithography wavelengths and circuit feature sizes are increasing. Lower power supply voltages significantly reduce noise margins and increase variations in process, device and design parameters. Consequently, it is steadily more difficult to control the fabrication process precisely enough to maintain uniformity. The inherent randomness of materials
used in fabrication at nanoscopic scales means that performance will be increasingly variable, not only from die-to-die but also within each individual die. Parametric variability will be compounded by degradation in nanoscale integrated circuits resulting in instability of parameters over time, eventually leading to the development of faults. Process variation cannot be solved by improving manufacturing tolerances; variability must be reduced by new device technology or managed by design in order for scaling to continue. Similarly, within-die performance variation also imposes new challenges for test methods.

In an attempt to address these issues, this thesis specifically focus on: $i$ improving the power efficiency for the high-resolution, high-speed, and low spurious spectral A/D conversion performance by exploring the potential of low-voltage analog design and calibration techniques, respectively, and ii) development of circuit techniques and algorithms to enhance testing and debugging potential to detect errors dynamically, to isolate and confine faults, and to recover errors continuously. This will become increasingly important as devices experience parametric degradation over time, requiring run-time reconfiguration.

### 1.4. Organization of the Thesis

Chapter 2 of this thesis reviews high-speed, high resolution A/D converter architectures and discusses the design challenges for analog circuits and the design choices for converter's common building blocks in a deep-submicron CMOS technology. On the basis of this assessment, a multi-step A/D converter is selected to explore the prominent issue of power efficiency under low supply voltages. Chapter 2 further describes the multi-step A/D converter architecture in more detail. Key design techniques for each stage are highlighted and the details of the circuit implementation are presented. In particular, error sources are identified and circuit techniques to lessen their impact are proposed. The chapter ends with a summary of the prototype experimental results. Chapter 3 focuses on novel computer-aided and design-for-test circuit technique to augment the analysis of random process variations on the converter's performance. The chapter further presents a continuous-time on-chip waveform generator and a method for the built-in characterization of the converter parameters. Development of circuit techniques and algorithms to enhance debugging prospectives are presented in Chapter 4. Initially, an approach to monitor die-level process variations to allow the estimation of selected performance figures and in certain cases guide the test is introduced. The chapter further continues with discussions on how to guide the test with the information obtained through monitoring process variations and how to estimate the selected performance figures. The chapter closes with for diagnostic analysis of static errors based on the steepest-descent method. In this approach, the most common errors are identified and modeled before the model is applied to estimate adaptive filtering algorithm look-up table for error estimation and fault isolation. Additionally, diagnostic analysis of the bandwidth mismatch of the time-interleaved systems is introduced. Finally, foreground calibration is discussed and experimental results given. In Chapter 5 the main conclusions are summarized and recommendations for further research are presented.

## CHAPTER 2.

## DESIGN OF MULTI-STEP ANALOG TO DIGITAL CONVERTERS

In highly integrated telecommunication systems, moving analog-to-digital converters capable of IF sampling towards the high frequency front-end maximize economic-value exploiting system complexity and full integration. The goal of the A/D converter is to minimize analog filtering and to replace it with better controllable digital functions. System-on-chip, SoC, realizations require an $\mathrm{A} / \mathrm{D}$ converter embedded in a large digital IC. To achieve the lowest cost, the system-on-chip has to be implemented in state-of-the-art CMOS technologies and must be area and power efficient and avoid the need for trimming to achieve the required accuracy. The rapidly decreasing feature size and power supply voltage of deep-submicron CMOS technology increases the pressure on converter requirements. As the supply voltage is scaled down, the voltage available to represent the signal is reduced. To maintain the same dynamic range on a lower supply voltage, the thermal noise of the circuit must also be proportionally reduced. In analog circuits, decreasing the voltage supply consequently reduces the output swing, which reduces the SNR. This results in an increase of power consumption, which is determined by the SNR at a given frequency. Although several architectures can be embedded in SoC realizations, some of the drawbacks such as large amount of silicon and power of flash A/D converters, the matching of the inputs of several tens of folding amplifiers in the folding A/D converters and the larger latency for certain digital feedback loops in pipelined A/D converters, limits the choice to sub-ranging or two-step/multi-step architecture.

### 2.1. High-Speed High-Resolution A/D Converter Architectural Choices

Since the existence of digital signal processing, A/D converters have been playing a very important role to interface analog and digital worlds. They perform the digitalization of analog signals at a fixed time period, which is generally specified by the application. The A/D conversion process involves sampling the applied analog input signal and quantizing it to its digital representation by comparing it to reference voltages before further signal processing in subsequent digital systems. Depending on how these functions are combined, different A/D converter architectures can be implemented with different requirements on each function. To implement power-optimized $\mathrm{A} / \mathrm{D}$ converter functions, it is important to understand the performance limitations of each function before discussing system issues. In this section, the concept of the basic A/D conversion process and the fundamental limitation to the power dissipation of each key building block are presented.

### 2.1.1. Multi-Step A/D Converters

Parallel (Flash) A/D conversion is by far the fastest and conceptually simplest conversion process [1-20], where an analog input is applied to one side of a comparator circuit and the other side is connected to the proper level of reference from zero to full scale. The threshold levels are usually generated by resistively dividing one or more references into a series of equally spaced voltages, which are applied to one input of each comparator. For $n$-bit resolution, $2^{n}-1$ comparators simultaneously evaluate the analog input and generate the digital output as a thermometer code. Since flash converter needs only one clock cycle per conversion, it is often the fastest converter. On the other hand, the resolution of flash ADCs is limited by circuit complexity, high power dissipation, and comparator and reference mismatch. Its complexity grows exponentially as the resolution bit increases. Consequently, the power dissipation and the chip area increase exponentially with the resolution. The compo-nent-matching requirements also double for every additional bit, which limits the useful resolution of a flash converter to eight to ten bits. The impact of various detrimental effects on flash A/D converter design will be discussed further in section 2.5.1.

To reduce hardware complexity, power dissipation and die area, and to increase the resolution but to maintain high conversion rates, flash converters can be extended to a two-step/multi-step [22-39] or sub-ranging architecture [40-53] (also called series-parallel converter). Conceptually, these types of converters need $m \times 2^{n}$ instead of $2^{n \times n}$ comparators for a full flash implementation assuming $n_{1}, n_{2}, \ldots, n_{m}$ are all equal to $n$. However, the conversion in sub-range, two-step/multi-step ADC does not occur instantaneously like a flash ADC, and the input has to be held constant until the sub-quantizer finishes its conversion. Therefore, a sample-and-hold circuit is required to improve performance. The conversion process is split into two steps as shown in Figure 2-1. The first A/D sub-converter performs a coarse conversion of the input signal. A $\mathrm{D} / \mathrm{A}$ converter is used to convert the digital output of the $\mathrm{A} / \mathrm{D}$ sub-converter back into the analog domain. The output of the $\mathrm{D} / \mathrm{A}$ converter is then subtracted from the analog input. The resulting signal, called the residue, is amplified and fed into a second $A / D$ sub-converter which takes over the fine conversion to full resolution of the converter. The amplification between the two stages is not strictly necessary but is carried out nevertheless in most of the cases. With the help of this amplifying stage, the second $A / D$ sub-converter can work with the same signal levels as the first one, and therefore has the same accuracy requirements. At the end of the conversion the digital outputs of both A/D sub-converters are summed up.


Figure 2-1: Two-step $A / D$ converter

By using concurrent processing, the throughput of this architecture can sustain the same rate as a flash A/D converter. However, the converted outputs have a latency of two clock cycles due to the extra stage to reduce the number of precision comparators. If the system can tolerate the latency of the converted signal, a two-step converter is a lower power, smaller area alternative.

### 2.1.2. Pipeline A/D Converters

The two-step architecture is equipped with a sample-and-hold $(\mathrm{S} / \mathrm{H})$ circuit in front of the converter (Figure 2-1). This additional circuit is necessary because the input signal has to be kept constant until the entire conversion (coarse and fine) is completed. By adding a second S/H circuit between the two converter stages, the conversion speed of the two-step A/D converter can be significantly increased (Figure 2-2). In a first clock cycle the input sample-and-hold circuit samples the analog input signal and holds the value until the first stage has finished its operation and the outputs of the subtraction circuit and the amplifier have settled. In the next clock cycle, the $\mathrm{S} / \mathrm{H}$ circuit between the two stages holds the value of the amplified residue. Therefore, the second stage is able to operate on that residue independently of the first stage, which in turn can convert a new, more recent sample. The maximum sampling frequency of the pipelined two-step converter is determined by the settling time of the first stage only due to the independent operation of the two stages. To generate the digital output for one sample, the output of the first stage has to be delayed by one clock cycle by means of a shift register (SR) (Figure 2-2). Although the sampling speed is increased by the pipelined operation, the delay between the sampling of the analog input and the output of the corresponding digital value is still two clock cycles. For most applications, however, latency does not play any role, only conversion speed is important. In all signal processing and telecommunications applications, the main delay is caused by digital signal processing, so a latency of even more than two clock cycles is not critical.


Figure 2-2: Two-Step converter with an additional sample-and-hold circuit and a shift register (SR) to line up the stage output in time

The architecture as described above is not limited to two stages. Because the inter-stage sample-and-hold circuit decouples the individual stages, there is no difference in conversion speed whether one single stage or an arbitrary number of stages follow the first one. This leads to the general pipelined A/D converter architecture, as depicted in Figure 2-3 [54-89]. Each stage consists of an $\mathrm{S} / \mathrm{H}$, an N -bit flash A/D converter, a reconstruction $\mathrm{D} / \mathrm{A}$ converter, a subtracter, and a residue amplifier. The conversion mechanism is similar to that of sub-ranging conversion in each stage. Now the amplified residue is sampled by the next $\mathrm{S} / \mathrm{H}$, instead of being fed to the following stage.

All the $n$-bit digital outputs emerging from the quantizer are combined as a final code by using the proper number of delay registers, combination logic and digital error correction logic. Although this operation produces a latency corresponding to the sub-conversion stage before generating a valid output code, the conversion rate is determined by each stage's conversion time, which is dependant on the reconstruction $\mathrm{D} / \mathrm{A}$ converter and residue amplifier settling time. The multi-stage pipeline structure combines the advantages of high throughput by flash converters with the low complexity, power dissipation, and input capacitance of sub-ranging/multi-step converters.


Figure 2-3: Multi-stage pipeline A/D converter architecture
The advantage of the pipelined A/D converter architecture over the two-step converter is the freedom in the choice of number of bits per stage. In principle, any number of bits per stage is possible, down to one single bit. It is even possible to implement a non-integer number of bits such as 1.5 bit per stage by omitting the top comparator of the flash A/D subconverter used in the individual stages [59]. It is not necessary, although common, that the number of bits per stage is identical throughout the pipeline, but can be chosen individually for each stage [65-69]. The only real disadvantage of the pipelined architecture is the increased latency. For an A/D converter with $m$ stages, the latency is $m$ clock cycles. For architectures with a small number of bits per stage, the latency can thus be ten to fourteen clock cycles or even more.

### 2.1.3. Parallel Pipelined A/D Converters

The throughput rate can be increased further by using a parallel architecture [90-106] in a time-interleaved manner as shown in Figure 2-4. The first converter channel processes the first input sample, the second converter channel the next one and so on until, after the last converter channel has processed its respective sample, the first converter has its turn again (see Section 2.4.2 for extensive discussion on timing-related issues in time-interleaved systems). The individual $\mathrm{A} / \mathrm{D}$ converters therefore operate on a much lower sampling rate than the entire converter, with the reduction in conversion speed for each individual converter equal to the number of A/D converters in parallel. The only building block that sees the full input signal bandwidth of the composite converter is the sample-and-hold circuit of each A/D converter. Theoretically, the conversion rate can be increased by the number of parallel paths, at the cost of a linear increase in power consumption and large silicon area requirement. A second problem associated with parallel A/D converters is path mismatch. During operation, the input signal has to pass different paths from the input to the digital output. If all A/D converters in parallel are identical, these paths are also identical.


Figure 2-4: Parallel pipeline $A / D$ converter architecture

However, if offset, gain, bandwidth or time mismatch occur between the individual converters, the path for the input signal changes each time it is switched from one converter to another. This behavior gives rise to fixed-pattern noise at the output of the composite A/D converter which can be detected as spurious harmonics in the frequency domain [90]. How these errors are seen in the spectrum of the sampled signal will be discussed in conjunction with the time-interleaved $\mathrm{S} / \mathrm{H}$ in Section 2.4.2. The parallel architecture is advantageous when high sampling rates are necessary which are difficult to achieve with single A/D converter. Although the architecture is straightforward, parallel A/D converters usually are not the best compromise when it comes to increasing the conversion rate of medium speed converters. For the A/D converter family described in this thesis, it has therefore been decided in favor of two-step/multi-step converter to obtain higher speed.

### 2.2. Multi-Step A/D Converter Architecture

Demanding requirements are placed on high-performance analog-to-digital converters and analog components in most digital receivers. In cellular base station digital receivers for example, sufficient dynamic range is needed to handle high-level interferers (or blockers) while properly demodulating the lower level desired signal. A cellular base station consists of many different hardware modules including one that performs the receiver and transmitter functionality. Today, analog technology is being replaced by CDMA and WCDMA worldwide and Europe adapted GSM over a decade ago.

To verify the effective resolution bandwidth versus power efficiency of a multi-step architecture, a GSM base-station application (Table I) has been targeted as an appropriate vehicle for a prototype described in this Chapter. Various CDMA and GSM designs exist today and methods to reduce cost and power are continuously being sought by base transceiver station manufacturers. Optimizing single-carrier solutions or developing multi-carrier receivers can accomplish this. For the sub-sampling receiver architecture, which is commonly used in base transceiver station equipment, stringent noise and distortion requirements are placed on the A/D converter. In receiver applications, the lower level desired signal is digitized alone or in the presence of an unwanted signal(s) that can be significantly larger in amplitude. To properly design the receiver, the A/D converter effective noise figure must be determined under these two signal extremes. The converter noise figure is determined by comparing its total noise power to the thermal noise floor. For small analog input signals, the thermal plus quantization noise power dominate the A/D converter noise floor, which is used to approximate the $A / D$ converter effective noise figure. In practice, once the $A / D$ converter effective noise figure is known in the small signal condition and the cascaded noise figure of the analog circuitry (RF and IF) is determined, the minimum power gain ahead of the $\mathrm{A} / \mathrm{D}$ converter is selected to meet the required receiver noise figure.

| Technology | Digital CMOS |
| :---: | :---: |
| Resolution | 12 bit |
| Supply voltage | Single supply |
| Sample rate | $>50 \mathrm{Msample} / \mathrm{s}$ |
| Effective bandwidth | 25 MHz |
| SNR | $>66 \mathrm{~dB}$ |
| SFDR | $>75 \mathrm{~dB}$ |
| THD | $>70 \mathrm{~dB}$ |
| Power dissipation | $<150 \mathrm{~mW}$ |
| Area | $<1 \mathrm{~mm}^{2}$ |

TABLE I - REQUIREMENTS FOR IF CONVERSION

The amount of power gain places an upper limit on the highest interference level the receiver can tolerate before the A/D converter overloads. The sub-sampling architecture can be used with a single down conversion architecture if sufficient SNR and SFDR performance can be obtained from the converter at higher IF frequencies. Distortion causes inter-modulation of large unwanted signals, the resulting products of which can fall in the wanted channel band. A/D converter with the 12 -bit accuracy is sufficient together with the amount of channel filtering and the gain of the automatic gain control, which is included to relax dynamic range requirements of the A/D converter. To be able to deal with the complete GSM band, the sample rate of the A/D converter has to be $50-60 \mathrm{MSample} / \mathrm{s}$ with an effective resolution bandwidth of 25 MHz . The SINAD of the GSM signal is only 9 dB but in order to handle the large neighboring channels the SNR of the converter needs to be 66 dB . The spurious tones generated by large interfering unwanted channels can disturb the reception of a small wanted channel. The SFDR must therefore be below 75 dB . The target power dissipation is chosen as 150 mW .

A detailed block diagram of the two-step A/D converter is shown in Figure 2-5. Because the five-eight partitioning (the A/D converter utilizing five-bit coarse and eight-bit fine quantizer) offers a lower transistor count for the required accuracy, this topology was selected over the six-seven approach. The differential input signal is sampled with three timeinterleaved sample-and-hold circuits. Noise generated and sampled in the S/H deteriorates the analog input signal which has to be quantized by the A/D converter. This generated and sampled noise has to be sufficiently low to meet SNR requirements. The resulting analog
signal is processed into the five-bit coarse A/D converter, which compares the differential input signal with a resistor reference ladder. Because of their simple structure and high-speed capability, flash architectures are natural choices for coarse A/D converter. To perform a proper total conversion the coarse A/D converter has to have accuracy such that the resulting residue signal is always in the range of the fine A/D converter. If offset voltage is the main inaccuracy, then input device area needs to be increased in inverse proportion to the required precision, increasing power of the fine comparators in a square fashion. Alternatively, some offset cancellation techniques can be used (with some timing and speed impact), increasing power only by the extra circuitry needed to do the cancellation. The acquired signal from this quantization is stored in a latch and is also applied to a switch unit. The switching-matrix voltage reference will add power similar to that required by the reference ladder for a full flash converter. The power of the resistor ladders in the switching-matrix should also follow the same characteristics as will be shown in the coarse section. This switch unit selects, according to the coarse quantization, four reference signals, from the same resistor reference ladder used for the coarse quantization. These selected reference signals are combined with the held input signals from $\mathrm{S} / \mathrm{H}$ in two residue amplifiers. Reducing the offsets of these amplifiers is necessary since residue signals have to be accurate at the overall A/D converter accuracy. After amplification, the residue signals are placed into the fine resistor ladder using fine buffers. The eight bits of the fine ADC can be generated with sufficient accuracy without using compensation by using a folding and interpolating A/D converter.


Figure 2-5: Prototype two-step/multi-step $A / D$ converter
If there is an error in the coarse $A / D$ converter, missing codes can occur, which can be caused by insufficient settling in the coarse A/D converter or by mismatch in the coarse comparators. Therefore over-range of one bit is applied in the fine A/D converter. The S/H circuit must exhibit linearity consistent with twelve-bit operation. For a twelve-bit linear reconstruction $\mathrm{D} / \mathrm{A}$ converter (consisting of resistor reference ladder and switch matrix), the coarse A/D converter needs only to be five-bits linear since errors in its quantization levels generate over or under-range values in the residue signal that are eventually digitized by the fine A/D converter. However, before the inputs of the residue amplifier are subtracted, they must retain twelve-bit linearity, a very important constraint when one input must be converted from voltage to current before subtraction from the other. The overall linearity of the residue amplifier and fine A/D converter must exhibit linearity consistent with eight bits.

### 2.3. Error Sources in Multi-Step A/D Converter

The overall A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers. Although a multi-step A/D converter makes use of considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. The conversion process therefore is susceptible to analog circuit and device impairments. Besides timing errors, the primary error sources present in a multi-step A/D converter are offset, gain and linearity errors of each stage. Offset and gain errors are combined result of two physical effects: noise, which includes charge injection noise in analog switches, thermal, shot and flicker noise, and noise coupled from digital circuitry (via crosstalk or substrate) and on-chip process parameter variation, e.g. device mismatch. The offset errors include offset caused by either component mismatch, self heating effects, comparator hysteresis or noise. The gain error group includes all the errors in the amplifying circuit, including technology variations and finite gain and offset of the operational amplifier. The use of redundancy and digital correction has emerged as an effective means of coping with the some of these errors, namely those originating from high offsets of amplifiers and comparators [59]. Since nonlinearity and gain errors in the coarse A/D converter provoke over-range problems and code level shifting, the approaches to apply digital correction are based on either increasing the input range of the next stage and using extra comparators or using the partial codes in the next stages to correct the code of the present stage. With digital correction, the effects of offset, gain and coarse A/D converter nonlinearity are reduced or eliminated; therefore, the $\mathrm{D} / \mathrm{A}$ converter nonlinearity and residue amplifier gain and offset errors limit the performance of multi-step converters.

The effect of introducing redundancy on the coarse A/D converter offset is studied by examining plots of the ideal residue versus the input in Figure 2-6a), residue versus input with coarse A/D converter offset in Figure 2-6b) and residue versus input with coarse A/D converter offset error when over-range is applied in Figure 2-6cc. In Figure 2-6a), both, the coarse $\mathrm{A} / \mathrm{D}$ converter and the $\mathrm{D} / \mathrm{A}$ converter are assumed to be ideal. When the input is between the decision levels determined by the coarse A/D converter, the coarse ADC and DAC outputs are constant; therefore, the residue rises with the input. When the input crosses a decision level, the coarse A/D converter and the D/A converter outputs increase by 1 LSB at a two-bit level, so the residue decreases by a digital value of conversion range of fine ADC. When the coarse $\mathrm{A} / \mathrm{D}$ converter has some nonlinearity, with the $\mathrm{D} / \mathrm{A}$ converter still ideal, as shown in Figure 2-6b) for a similar example, two of the coarse ADC decision levels are shifted, one by $-1 \frac{1}{2} \operatorname{LSB}(n+1$ error) and the other by $+2 \mathrm{LSB}(n+2$ error). When the input crosses a shifted decision level the residue decreases by digital value of conversion range of fine A/D converter. If the conversion range of the second stage is increased to handle the larger residues, they can be encoded and the errors corrected (Figure 2-6c) [55,59]. The effect of an offset error in a comparator on a stage transfer function is shown in Figure 2-6d). The dotted line represents an ideal transfer function, and the solid line shows a transfer function with an offset voltage in a comparator.

The references of the $\mathrm{D} / \mathrm{A}$ converter and the subtraction of the input signal and the $\mathrm{D} / \mathrm{A}$ converter output determine the achievable accuracy of the total A/D converter. Nonuniform spacing of the $\mathrm{D} / \mathrm{A}$ converter reference levels also contributes to the nonlinearity of the analog to digital converter. Similarly, the residue signal is incorrect exactly by the amount of the $\mathrm{D} / \mathrm{A}$ converter nonlinearity. In this design, matching of the reference ladder resistors in a $\mathrm{D} / \mathrm{A}$ converter is adequate for twelve-bit level [107], while several techniques for reduc-
ing comparator offsets, such as auto-zeroing [48], averaging [50] or capacitive interpolation [62] can be employed. Alternatively, the offsets and input capacitance can be reduced by means of distributed pre-amplification combined with averaging [108], and possibly also with interpolation [109]. An offset on the residue amplifier gives a $d c$ shift of the fine A/D converter reference with respect to the coarse A/D converter and D/A converter range. The offset error in the residue amplifier does not affect linearity if calibration is used as shown in Section 2.6.2.


Figure 2-6: a) Ideal residue versus input, b) Residue versus input with coarse $A / D$ converter offset, c) Residue versus input with coarse $A / D$ converter offset errors when over-range is applied, d) Effect of comparator offset, e) Finite do gain effect on transfer function, and f) Finite gain-bandwidtth effect on transfer function

In a multi-step analog to digital converter, errors in per stage gain (Figure 2-6e) cause a nonlinearity in the input to output transfer characteristic. If a gain error in the residue amplifier occurs, the total range of the residue signal (signal as a result of the subtraction of the input signal and the $\mathrm{D} / \mathrm{A}$ converter signal) will be adjusted causing an error in the analog input to the next stage. As a consequence the residue signal will not fit in the fine A/D converter range. The techniques, such as dual-residue signal processing [61], spread the errors of the residue amplifiers over the whole fine range, which results in an improved linearity. An error in the range of the fine $\mathrm{A} / \mathrm{D}$ converter results in an error similar to a residue amplifier gain error. As a consequence, the gain of the residue amplifier should therefore be lined up with the fine $\mathrm{A} / \mathrm{D}$ converter range.

The linearity of the fine A/D converter determines the overall achievable linearity of the A/D converter. However, since the residue amplifier provides gain, the linearity requirements are reduced by this gain factor. Influence of the finite gain-bandwidth product (Figure $2-6 f f$ of each stage on total A/D converter resolution will be further argued in following sections.

Note that the sample-and-hold errors are not discussed in this section since the requirements of this block in the multi-step architecture are not different from the requirements in other architectures.

### 2.4. Time-Interleaved Front-End Sample-and-Hold Circuit

The front-end sample-and-hold $(\mathrm{S} / \mathrm{H})$ plays a crucial role in the performance of multi-step A/D converters. Without an $\mathrm{S} / \mathrm{H}$, the maximum allowable frequency of the input signal would be substantially lower than its theoretical Nyquist requirement $\left(f_{i n}<f_{s} / 2\right)$ and limited to $f_{i n}<\left(3 f_{s}\right) /\left(\pi 2^{N}\right)$, where $N$ is resolution in bits and $f_{s}$ is sampling frequency. However, linearity and dynamic range of the $\mathrm{S} / \mathrm{H}$ directly affect those of the overall system, while the speedprecision trade-offs limit the conversion rate. This trade-off is further discussed in this section.

### 2.4.1. Time-Interleaved Architecture

The sampling rate of a system can be increased by a using time-interleaved technique [90106], where a higher sampling rate is obtained by running the system in parallel as illustrated in Figure 2-7a), although at different clock phases. The total three-time S/H consists of three units. Since the clock signals are one high out of three, each sample-and-hold unit is sampling during one clock period and holding during the other two enabling three actions (sampling, coarse and fine decision) to proceed at the same time on different analog samples as shown in Figure 2-7b). In this design, only one clock cycle of the master clock for sampling is used implying that the total capacitance as seen from the input is reduced since now only one instead of three hold capacitors $C_{H}$ is connected to the input simultaneously. If $\mathrm{S} / \mathrm{H} 1$ is tracking the analog input signal $n, S / H 3$ performs the coarse quantization of the previous sample $n-1$ while $S / H 2$ completes the fine quantization of two samples earlier $n-2$ and so on. In sample mode, the output switches are open and the load capacitance of the opamp is small. Hence, the opamp bandwidth is high and output can now follow the input. During operation, the input signal has to pass different paths from the input to the digital output. However, if offset, gain, bandwidth or time mismatch occur between the individual units, the path for the input signal changes each time it is switched from one unit to another, which gives rise to fixed-pattern noise at the output of the sample-and-hold circuit. Extensive discussion on the effects of these errors and remedies are given in the next section.


Figure 2-7: a) Total sample-and-hold circuit consisting of three time-interleaved sample-and-bold units at the moment when S/H1 is sampling and S/H2 and S/H3 are holding, b) Timing diagram of interleaved principle, signals out 13 are internal signals of clock generator

Failure to settle accurately, which is caused by an inadequate hold time, results in errors that degrade the performance of the A/D converter. If the settling is linear, the error is proportional to the input, and the result is a fixed gain error. If the settling is nonlinear, the effect is a signal dependent error [110]. Choosing the amplifier bandwidth too high increases the amplifier's wide-band noise and additionally demands unnecessarily low on-resistance of the switches and thus large transistor dimensions which in turn increases charge injection. The output voltage has to fulfill two settling requirements. By the time the converter makes its decision, the output signal of the sample-and-hold circuit must have settled to five and eight bit accuracy, respectively. The settling to the full twelve bit accuracy can take place simultaneously with the settling of the D/A converter and is only necessary at the input of the residue amplifier.

The type and the dimensions of the switches not only determine the charge injection that can cause non-linearity and offset, but also the bandwidth and the stability of the sample-andhold circuit are affected. The effective capacitance $C_{f f f}$ which can be derived from the hold capacitance $C_{H}$, the input capacitance $C_{G}$ of the operational amplifier and the parasitic capacitance $C_{p a r}$ together with the switch on-resistance, forms a pole in addition to the dominant pole of the operational amplifier. The optimum speed is achieved if both poles are real and identical, e.g., $\omega_{s}=4 \omega_{G B W}$ [111], where $\omega_{s}$ denotes the pole caused by the switch and $\omega_{G B W}$ is the gain-bandwidth product of the amplifier. The necessary on-resistance of the feedback switches can thus be found as $r_{o n}=1 /\left(4 \omega_{G B W} C_{e f f}\right)$. At the sampling phase, the sampling behavior depends on the unit gain bandwidth and phase margin of the circuit. On the other hand, at the hold phase, the settling behavior mostly depends on the closed-loop time constant of the amplifier only. Because the feedback factor is smaller than one, the phase margin is not an issue at the hold phase. If $\left(V_{G S}-V_{\mathrm{T}}\right)$ is fixed to meet an output swing requirement and $g_{m}$ (proportional to $C_{a x}(W / L)$ is fixed to meet a speed requirement, $C_{G}$ will be proportional to $L$. Then, scaling of $L$ with advanced CMOS technologies will reduce $C_{G}$. However, the noise mostly originate from the sampling capacitor given its weak dependence on $C_{G}$ and further reduction on the capacitor value is not expected even with scaled technologies as a result. As shown in Figure 2-8a), the optimum time constant remains constant regardless of the S/H circuit size (or $I_{D}$ ) because $C_{L}$ scales together with $C_{H}$ and the parasitic capacitance $C_{p}$. So, if speed is the only constraint, the power dissipation can be reduced by scaling down the capacitor size until the speed is limited by other practical considerations, such as layout, matching, etc.


Figure 2-8: a) Closed loop normalized time constant versus bold capacitance $C_{H}$ for different biasing conditions; case for $L=0.18 \mu \mathrm{~m}, C_{H}=3 C_{L}, C_{L}=C_{p}$, b) Optimum gate capacitance $C_{G, \text { opt versus hold capacitance } C_{H} \text { for different loading }}$ and parasitic conditions

The time constant is normalized to the $\tau_{t}\left(=1 / f_{t, \text { intrinisid }}\right)$ of the device which is approximately $\left(C_{G} / g_{n}\right)$. The parasitic-loading effects worsen as the conversion rate increases. In a high-speed converter, the parasitic capacitance can be comparable to the total sampling capacitance. At each point on the curve, there are two possible bias conditions, and only the curve with a positive slope will be considered here on since it is the low power solution.

Noise is an important constraint in high resolution front-end S/H circuits, thus, an appropriate hold capacitor size must be first chosen in order to reduce its $k T / C$ noise level down below a given noise requirement. The choice of the hold capacitor value is a trade-off between noise requirements on the one hand and speed and power consumption on the other hand. The sampling action adds $k T / C$ noise to the system which can only be reduced by increasing the hold capacitance $C_{H}$. A large capacitance, on the other hand, increases the load of the operational amplifier and thus decreases the unity-gain bandwidth for a given power consumption. The selected value of the hold capacitor therefore is always a compromise. Next, the op amp size and its bias current can be determined for a given speed requirement and minimum power dissipation using $\tau$-vs.- $C_{H}$ curves as in Figure 2-8a). Notice that for low frequency operation (where $\tau / \tau_{t}$ is large) the $C_{G}$ that achieves the minimum power dissipation for given settling time and noise requirements usually does not correspond to the minimum time constant point. This is because fixing the $C_{H} / C_{G}$ ratio of the circuit to the minimum time constant point requires larger $C_{G}$ resulting in power increase and excessive bandwidth.


Figure 2-9: a) Maximum acbievable SNR for different sampling capacitor values and resolutions, b) SNR versus power dissipation

Near the speed limit of the given technology (where the ratio $\tau / \tau_{\mathrm{t}}$ is small), however, the difference in power between the minimum power point and the minimum time constant point becomes smaller as the stringent settling time requirement forces the $C_{H} / C_{G}$ ratio to be at its optimum value to achieve the maximum bandwidth. The $C_{H} / C_{G}$ (Figure 2-8b) ratio can be expressed as $C_{G, \phi t}=\chi_{2} C_{H}$, where $\chi_{2}$ is a circuit-dependent proportionality factor. For a given speed requirement and signal swing, a two times reduction in noise voltage (in $\sigma$ ) requires a four times increase in the sampling capacitance value and the op amp size. Conversely, a two times increase in the supply voltage and the signal swing results in a four times smaller $\mathrm{S} / \mathrm{H}$ circuit, and therefore, a two times smaller op amp power dissipation. This means that the S/H circuit power quadruples for every additional bit resolved for a given speed requirement and supply voltage as illustrated in Figure 2-9. Notice that for a small sampling capacitor values, thermal noise limits the SNR, while for a large sampling capacitor, the SNR is limited by the quantization noise and the curve flattens out.

### 2.4.2. Matching of Sample-and-Hold Units

The uniformity of the sample-and-hold units is affected by two principal sources of error (Figure 2-10): inaccuracies in the fabrication process [112-114] and control signal feed-through. Although the sample-and-hold units are designed to be nominally identical, the degree of component matching is limited by imperfections in the fabrication process. Capacitor matching is determined by variations in the area of the capacitor plates and the thickness of the dielectric. The matching of transistor characteristics on a chip is determined by the matching of threshold voltages, mobilities, oxide and gate-overlap capacitances, and the widths and lengths of the transistor gates.


Figure 2-10: Sources of errors in the three times interleaved sample-and-hold
In general, the effect of the non-uniformity of the sampling units coherent to a timeinterleaved system can be divided into static (offset) and dynamic (time, gain, and bandwidth) mismatch errors [115-118]. Static mismatch causes fixed pattern noise in the sample-andhold. It arises from op-amp offset mismatches and charge injection mismatches across the sample and hold units. For a $d c$ input, each sample and hold unit may produce a different output and the period of this error signal is $N / f_{s}$ as illustrated in Figure 2-11a) and Figure 2-13a). Since the offset voltage under consideration is that of a CMOS source-coupled differential amplifier, it is a function of the threshold voltage $V_{\mathrm{T}}$, aspect ratio $W / L$ and $g_{m} / I_{b i a s}$. Of these three terms, the process determines the first two, while the third is proportional to the square root of the bias current. Under fast turn-off conditions the variation in channel charge dominates the charge injection mismatch $\Delta q$ [113] and can be modeled as part of the mismatch of two geometric parameters, the channel width and length. The difference in channel area, $\delta(W L)$, of two mismatched transistors is $\delta(W L)=(W+\delta W)(L+\delta L)-W L$, where $\delta W$ and $\delta L$ are the variations in channel width and length. The voltage error due to non-uniform charge injection, $\delta V_{\text {pead }}$ is thus proportional to the channel width and length of the sampling transistor, which implies that the size of the error voltage and the input time constant are related. The switches with smaller $W / L$ ratio yield smaller pedestal mismatches but limit the signal bandwidth of the sampling unit. Charge injection is deposited on the hold capacitor $C_{H}$, introducing an error in the voltage stored on the capacitor, which appears as a distortion at the output with period of $N / f_{s}$. Another potential source of non-uniformity of the pedestal voltages resulting from charge injection mismatch is the variation in sampling capacitance. However, typically, this error is small compared to the error from the mismatch of the sampling switches and can therefore be neglected.

Offset mismatch will distort the signal every time a sample is taken with a different offset other than the one used to take the previous sample. Offset mismatch can be measured by sending signals with the same number of periods to all interleaved channels and studying the difference in average values. Once the offset is measured, it can be compensated for and thus the offset errors corrected. As shown in Appendix $A$, assuming that $d_{n}, n=0,1,2, \ldots, N-1$ are independent and identically distributed random variables with zero mean and standard deviation $\sigma_{d \phi}$ the power density of a spurious signal due to the offset, can be expressed as
$P_{d}^{\text {spur }}(k)=\frac{1}{N^{2}}\left|\sum_{n=0}^{N-1} d_{n} \cdot e^{-j k n(2 \pi / N)}\right|^{2}=\frac{1}{N^{2}} \sigma_{d}^{2}$

The offset mismatch in time-interleaved systems can be cancelled with analog techniques or digitally. One limitation of the digital method $[91,97]$ from the system point of view is the fact that the static offset has to be measured before the calibration.


Figure 2-11: $N=3, f_{s}=100 \mathrm{MS} / \mathrm{s}$, a) Simulated offset mismatch at $\sigma_{d}=1.5 \times 10^{-4}$ and $\sigma_{r}=4.5 \times 10^{-4}$, b) Simulated time mismatch at $\sigma_{r}=1 \times 10^{-4}$ and $\sigma_{r}=1 \times 10^{-3}$


Figure 2-12: $N=3$, $f_{s}=100 \mathrm{MS} / \mathrm{s}$, a) Simulated gain mismatch at $\sigma_{a}=5 \times 10^{-5}$ and $\sigma_{a}=7.9 \times 10^{-4}$, b) Simulated bandwidth mismatch at $\sigma_{d}=2.8 \times 10^{-2}$ and $\sigma_{r}=2.8 \times 10^{-3}$

Alternatively, chopping of the channel input signals, controlled with a pseudo-random signal, together with de-chopping of the channel $\mathrm{A} / \mathrm{D}$ converter outputs, can be employed [98]. One analog offset cancellation technique employs an auxiliary input stage to store a representation of the operational amplifier offset and the charge injection offset on capacitors [119].

In this implementation the resulting $d c$ offset is mainly cancelled with design percussions, such as differential signal path, bottom plate sampling, small feedback switches, opamp high common-mode rejection ratio and by using the closed loop sampling architecture, such that consequent offset mismatch is sufficiently low for the required resolution.

The uniformity of the sampling unit transfer characteristics is also affected by feed-through of control signals via the substrate and parasitic inter-layer capacitances. In addition, perturbations (e.g. ringing) on common power, ground, signal, or signal-return lines, induced by control signals, can be the cause of $\mathrm{S} / \mathrm{H}$ unit performance mismatch. Therefore, the layout of the circuit is carefully designed and extensively shielded so as to minimize coupling through parasitic inter-layer capacitances and through the substrate.

In the front-end sample and hold, where the clock is used to sample a continuous time signal, any deviation of the sampling moment from its ideal value results in an error voltage in the sampled signal equal to the signal change between these two moments. Thus, the sampling clock has to be regarded as a sensitive analog signal and treated accordingly. Beside the random variations in the phase (mainly due to device noise and random noise coupled from the power supply and substrate and the signals present on the chip or the circuit board that can couple to the clock), time-interleaved front-end S/H suffer also from frequency-dependent sample time deviations (systematic error, clock skew), which originates mainly due to device mismatch and asymmetric layout of the clock generator and clock lines. The error signal caused by clock skew is the largest at the zero-crossings with a period of $N / f s$ and is modulated by the input frequency $f_{\text {in }}$ as illustrated in Figure 2-11b) and Figure 2-13b). As shown in Appendix $A$, assuming that $r_{n}, n=0,1,2, \ldots, N-1$ are independent and identically distributed random variables with zero mean and standard deviation $\sigma_{n}$, power density of a spurious due to the time mismatch can be expressed as

$$
\begin{equation*}
P_{r}^{\text {spur }}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1}\left(1-j r_{n} \omega_{i n} T\right) \cdot e^{-j k n(2 \pi / N)}\right|^{2}=\frac{A^{2} \omega_{i n}^{2} T^{2}}{2 N^{2}} \sigma_{r}^{2} \tag{2-2}
\end{equation*}
$$

where $A$ is the amplitude of the input sinusoid. The clock skew between sampling clocks of distributed $\mathrm{S} / \mathrm{H}$ circuits can be calibrated by measuring its value and controlling tunable delays of a DLL [120]. However, in general, calibration of the skew between S/H circuits has two significant drawbacks. First, measurement of the skew is complex and second, tuning of the delays requires high accuracy from the calibration hardware and algorithm. Alternatively, timing alignment within the required accuracy can be obtained by using a master clock [111] to synchronize the different sampling instants and careful design by matching the channels clock and input signals lines [121]. In this design, a similar approach is followed: besides extensive shielding of the clock lines, differences in line lengths, in passive interconnect parameters, (such as line resistivity and capacitance and line dimensions and via/contact resistance) and in delays of any active buffers within the clock distribution network are kept to the minimum.

Similarly to clock skew, if the gains of each $\mathrm{S} / \mathrm{H}$ unit are different, the basic error occurs with a period of $N / f s$ but the magnitude of the error is modulated by the input frequency $f_{i r}$. In both cases (clock skew and gain mismatch), noise spectrum peaks at $f s / N \pm f_{i \text { in }}$ (Figure 2-12a and Figure 2-14a). Assuming that $a_{n}, n=0,1,2, \ldots, N-1$ are independent and identically distributed random variables with zero mean and standard deviation $\sigma_{\omega}$, power density of a spurious due to the gain mismatch can be expressed as (Appendix A)
$P_{a}^{s p u r}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1} a_{n} \cdot e^{-j k n(2 \pi / N)}\right|^{2}=\frac{A^{2}}{2 N^{2}} \sigma_{a}^{2}$

Gain and timing offset mismatch will have a similar effect on the signal. By pure observation, it is not possible to distinguish whether the signal is distorted by gain or timing errors. One possible method to analyze the underlying behavior is to vary the input frequency; e.g. gain errors will not vary with input frequency, however, timing errors will increase linearly as the sampling frequency increases. Gain and timing offset errors also introduce errors at every sampling point.


Figure 2-13: SFDR versus a) offset mismatch ranging from $\sigma_{d}=1.5 \times 10^{-4}$ and $\sigma_{d}=4.5 \times 10^{-4}$ for different $N$, b) $f_{\text {in }} / f_{s}$ ratio for different time mismatch ranging from $\sigma_{r}=1 \times 10^{-3}$ and $\sigma_{r}=1 \times 10^{-4}$


Figure 2-14: SFDR versus a) gain mismatch ranging from $\sigma_{a}=5 \times 10^{-5}$ and $\sigma_{a}=7.9 \times 10^{-4}$ for different N , b) different bandwidth mismatch ranging from $\sigma_{b}=2.8 \times 10^{-2}$ and $\sigma_{b}=2.8 \times 10^{-3}$

As opposed to the offset error, however, the magnitudes of these errors depend on the phase of the sampled signal. Gain errors, for example, are small if the signal is sampled near its zero-crossing and large if it is sampled near its peaks. The gain mismatch can be calibrated digitally by measuring the reference levels and storing them in a memory. The ideal output code can be recovered using these measured reference levels [63]. However, by dimensioning the open loop $d$ c-gain of the operational amplifiers large enough, the effect of their mismatch is suppressed below the quantization noise level. With careful sizing and layout, capacitor matching sufficient for twelve-bit level, depending on the process, is achieved.

The random variation in the $\mathrm{S} / \mathrm{H}$ unit's internal capacitance $C_{G}$, transconductance $g_{m}$, switch on-resistance $R_{o n,}$ hold capacitance $C_{H}$ as well as the input capacitance and kickback noise of the subsequent stages, as seen from one $\mathrm{S} / \mathrm{H}$ unit, degrade the output settling behavior and the circuit's gain-bandwidth product differently. This error occurs with a period of $N / f s$, but the magnitude of the error, which is frequency and amplitude dependant, is modulated by the input frequency $f_{i n}$ with noise spectrum spurious at $f s / N \pm f_{i n}$ (Figure 2-12b and Figure 2-14b). Assuming that $b_{n}, n=0,1,2, \ldots, N-1$ are independent and identically distributed random variables with zero mean and standard deviation $\sigma_{b}$, power density of a spurious due to bandwidth mismatch in one-pole system can be expressed as (Appendix $A$ )

$$
\begin{equation*}
P_{b}^{\text {spur }}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1} b_{n} e^{-j k n(2 \pi / N)}\right|=\frac{A^{2} f_{i n}^{2}}{2 N^{2} f_{1}^{2}} \sigma_{b}^{2} \tag{2-4}
\end{equation*}
$$

By severely increasing the bandwidth, the impact of the bandwidth mismatch at the signal frequency becomes lower. For this reason, the bandwidth of each sample-and-hold unit has been chosen larger than what is required when just looking at signal attenuation.

### 2.4.3. Circuit Design

### 2.4.3.1. Folded-Cascode with Gain-Boosting Auxilarry Amplifier

The maximum speed and, to a large extent, the power consumption of $\mathrm{S} / \mathrm{H}$ is determined by the operational amplifier. In general, the amplifier's open loop dc gain limits the settling accuracy of the amplifier output, while the bandwidth and slew rate of the amplifier determine the maximal clock frequency. The operational amplifiers in the $\mathrm{S} / \mathrm{H}$ circuit have some unique requirements; the most important is the input impedance, which must be purely capacitive so as to guarantee the conservation of charge. Consequently, the operational amplifier input has to be either in the common source or the source follower configuration. Another characteristic feature of the $\mathrm{S} / \mathrm{H}$ circuit is the load at the amplifier output, which is typically purely capacitive and as a result, the amplifier output impedance must be high. The benefit of driving solely capacitive loads is that no output voltage buffers are required. In addition, if all the amplifier internal nodes have low impedance, and only the output node has high impedance, the speed of the amplifier can be maximized. Unfortunately, an output stage with very high output impedance cannot usually provide high signal swing.

The ultimate settling accuracy is limited by the finite amplifier $d c$ gain. What the exact settling error is depends not only on the gain but also on the feedback factor in the circuit utilizing the amplifier. A very widely-used method to improve the $d c$ gain is based on local negative feedback [56,122-124]. In addition to this cascode regulation other techniques for increasing the $d c$ gain have been proposed as well. Gain boosting with positive feedback has been investigated, [125-126]. In [127], dynamic biasing, where the op amp current is decreased toward the end of the settling phase, is used to increase the $d c$ gain. It exploits the fact that current reduction lowers the transistor $g_{D S,}$, which increases the $d c$ gain. By regulating the gate voltages of the cascode transistors [128] by adding an extra gain stage, the $d c$ gain of the amplifier can be increased by several orders of magnitude.

Besides the amplifier bandwidth, the settling time is limited by the fact that the amplifier can supply only a finite current to the load capacitor. Consequently, the output can not change faster than the slew rate. When designing an amplifier, the load capacitor is known and the required slew rate $S R=k \cdot V_{\text {max }} / T_{S}$ can be calculated from the largest voltage step $V_{\text {max }}$ and the clock period $T_{S}$. A commonly used rule of thumb suggests that one third of the settling time should be reserved for slewing, resulting in $k$ of six. The required slewing current is $I_{S R}$ $=\left(k \cdot V_{\max } C_{I}\right) / T_{s}$. It is linearly dependent on the clock frequency, while the current needed to obtain the amplifier bandwidth has a quadratic dependence.


Figure 2-15: Folded-casode amplifier with gain-boosting auxiliary amplifier
In order to use the amplifier in a closed loop configuration, its frequency response should be close to the single pole response. Thus, the phase margin at the unity gain frequency has an effect on the settling time as well, and the choice between an $n$-channel device and $p$-channel device input pair is made on the basis of this requirement. The $p$-channel device input architecture (Figure 2-15) offers lower gain-bandwidth product $\left(g_{m 1} / C_{L}\right)$ due to the low $p$-channel device transconductance, but the highest non-dominant pole $\left(g_{m s} / C_{t}\right)$ associated with the $n$ channel device cascode devices at the folding node (source of transistor $T_{5}$ ). On the other hand, utilizing a $n$-channel device input pair gives higher gain-bandwidth product, but the non-dominant pole is lower. Feed-forward capacitors can be used to bypass the cascode transistors at high frequencies to improve the phase margin [129-131]. In principle, the technique produces a zero, which is used to cancel the pole associated with the cascode node. It is, however, not possible to place this zero exactly on top of the pole. Thus, there is a sufficiently closely spaced pole-zero pair, a doublet, which is known to introduce a slowly settling component in the step response [132]. It is possible to employ an $n$-channel device and a $p$ channel device input pair in parallel, which increases the slew rate by $1 / 3$ (with the same total current consumption). However, at the same time that will increase the input capacitance and thermal noise and lower the non-dominant pole.

In fully differential amplifiers the common mode voltage level is not automatically determined. To set it to the wanted level, the input stage has been provided with common-mode circuit, consisting of two extra transistors $T_{11}$ and $T_{12}$ in a common-source connection, whose gates are connected to a desired common-mode reference $V_{c m}$ at the input, and their drains connected to the ground [128]. If a positive $d c$ feedback between the output and input exists, the $V_{c m}$ level at the output is regulated so that the $V_{c m}$ level at the input is equal to $V_{c m}$ at the gates of $T_{11}$ and $T_{12}$. If the $V_{c m}$ level at the input rises, the common-mode current in $T_{1}$ and $T_{2}$
is lowered and taken away by $T_{11}$ and $T_{12}$ to ground. The result is that the common-mode current in $T_{5}$ and $T_{6}$ increases pulling the $V_{c m}$ level at the output back down. The advantage of this solution is that the common-mode range at the output is not restricted by a regulation circuit and can approach a rail-to-rail behavior very closely.

The transistors of the output stage have three constrains: the sum of the saturation voltage for the transistors in one of the output branches must fit into the voltage headroom, resulting as the difference between the voltage supply and the desired output voltage swing. Second, the transconductance of the cascading transistors $T_{5,6}$ must be high enough, in order to boost the output resistance of the cascode, allowing a high enough $d c$ gain. Finally the saturation voltage of the active loads $T_{3,4}$ and $T_{9,10}$ must be maximized, in order to reduce the extra noise contribution of the output stage. These considerations underline a tradeoff between fitting the saturation voltage into the voltage headroom and minimizing the noise contribution. A good compromise is to make the cascading transistors larger than the active loads: in such a way the transconductance of the cascading transistors is maximized, boosting the dc gain, while their saturation voltage is reduced, allowing for a larger saturation voltage for the active loads, without exceeding the voltage headroom.

The op amp unity gain frequency $\omega_{1}$ (Figure 2-16a) can be made larger increasing $g_{m m}$ by means of making the transistors bigger; however this does not necessarily imply a faster op amp. The parasitic capacitance $C_{G}$ is also increased, therefore the feedback factor $\beta=C_{H} /\left(C_{H}+C_{p}+C_{G}\right)$ becomes smaller and the dominant pole $\omega_{p}=\beta \omega_{1}$ is pushed towards lower frequencies. Therefore, a trade off between the increase of $g_{m 1}$ and $C_{G}$ exists. This suggests that an optimum size for the input pair exists, which maximizes the transconductance of the op amp by avoiding to make the input capacitance dominant on the feedback factor (Section 2.4.1).


Figure 2-16: a) Open-loop frequency response of implemented folded-cascode amplifier with auxiliary gain-boosting amplifier, b) Noise contribution of the individual transistors

The total noise contribution of all the devices in the amplifier is usually combined as a single voltage source at the amplifier input. Assuming the noise sources to be uncorrelated, the total noise is obtained as a root of the sum of the squares of the individual input-referred noise sources. The noise contribution of the devices in the amplifier's first stage is the most significant (Figure 2-16b), and usually the noise of the other stages can be neglected, since it is attenuated by the preceding voltage gain. The input-referred noise of the amplifier input pair is reduced by increasing the transconductance, increasing the current, or increasing the aspect ratio of the devices.

The effect of the last method, however, is partially canceled by the increase in the noise excess factor. When referred to the amplifier input, the noise voltages of the transistors used as current sources (or mirrors) in the first stages are multiplied by the transconductance of the device itself and divided by the transconductance of the input transistor, which again suggests that maximizing input pair transconductance minimizes noise. It can be further reduced by decreasing the transconductances of the current sources. Since the current is usually set by other requirements, the only possibility is to decrease the aspect ratio of the device. This leads to an increase in the gate overdrive voltage, which, as a positive side effect, also decreases $\gamma$. It should be noticed that the overdrive voltage is equal to $V_{D S, S A T}$. Consequently, obtaining low noise with low supply voltage is difficult, especially with single stage amplifiers, where the output signal swing does not permit large $V_{D S, S A T}$. Increasing $L$ to avoid short channel effects is also possible, but with a constant aspect ratio it increases the parasitic capacitances, reducing the amplifier bandwidth. Cascode transistors do not make a significant contribution to noise, because their noise voltage is transformed into current through the high output impedance of the underlying current source.

### 2.4.3.2. Bootsrap Circuit

In standard CMOS technologies, the threshold voltage of MOS transistors does not scale with the supply voltage and it becomes a significant problem when MOS transistors are used as switches at low voltages. When the signal amplitudes are large, accuracy and signal bandwidth are limited by distortion, which originates from the fact that switch on-resistance are not constant but vary as functions of drain and source voltages. The on-resistance is expressed as $\mathrm{R}_{o n}=L /\left(\mu C_{a x} W\left(V_{G S}-V_{T}\right)\right.$ ), if $V_{D S}$ is small. In the equation two different signaldependent terms can be identified. The first and dominant one is the gate-source voltage $V_{G S}$. The second is the threshold voltage $V_{T}$ dependency on the source-bulk. Although large transistor switches can be used for the worst case $V_{T}$ design, the switch parasitic capacitance can significantly overload the output of the circuit. Therefore, increasing $V_{G S}-V_{T}$ is desirable to implement low on-resistance switch without adding too much parasitic capacitance.


Figure 2-17: Bootstrap circuit to boost the clock voltage

Several methods allow increase of this gate voltage drive. One method is to reduce $V_{T}$ by including an extra low-threshold transistor in the process, although it will add to process complexity. Another method is to increase $V_{G S}$ by using one large supply created from chip supply to drive all switches on the chip, but potential problems including possible cross-talk to some sensitive nodes through the shared supply and difficulty in estimating the total charge drain to drive all switches renders this method absolvent.

Another viable solution to avoid major source of non-linearity is to make the switch gatesource voltage constant, by making the gate voltage track the source voltage with an offset $\Delta V_{\text {offin }}$ which is, at its maximum, equal to the supply voltage. This technique, which is implemented in this design, is called bootstrapping [67]. In this case, the bootstrap circuit shown in Figure 2-17 drives each switch that uses the same clock to avoid the problem of crosstalk through the clock line. A $\Delta V_{\text {offin }}$ can be generated with a switched capacitor, which is pre-charged in every clock cycle. During the clock phase when the transistor is nonconductive the switched capacitor is pre-charged to $\Delta V_{\text {offitin }}$.To turn the switch on, the capacitor is switched between the input voltage and the transistor gate.

The capacitor values are chosen as small as possible for area considerations but large enough to sufficiently charge the load to the desired voltage levels. The device sizes are chosen to create sufficiently fast rise and fall times at the load. The load consists of the gate capacitance of the switching device $T_{10}$ and any parasitic capacitance due to inter-connect between the bootstrap circuit and the switching device. Therefore, it is desirable in the layout to minimize the distance between the bootstrap circuit and the switch or to insert shielding protection. The output waveforms of the bootstrap circuit are shown in Figure 2-18a).


Figure 2-18: a) Bootstrap circuit output, b) Sample-and-Hold output
When the switch $T_{10}$ is on, its gate voltage $V_{G}$ is greater than the analog input signal $V_{i n}$ by a fixed difference of $\Delta V_{\text {offin }}=V_{D D}$. Although the absolute voltage applied to the gate may exceed for a positive input signal, none of the terminal-to-terminal device voltages exceeds $V_{D D}$. A single-phase clock $c l k$ turns the switch $T_{10}$ on and off. During the off phase, clk is low discharging the gate of the switch to ground through devices $T_{11}$ and $T_{12}$. At the same time, $V_{D D}$ is applied by $T_{3}$ and $T_{7}$ across as capacitor connected transistor $T_{16}$, which act as the battery across the gate and source during the on phase. $T_{8}$ and $T_{9}$ isolate the switch from the capacitance while it is charging.

When clkn goes high, $T_{6}$ pulls down the gate of $T_{8}$, allowing charge from the battery capacitor to flow onto gate of $T_{10}$. This turns on both $T_{9}$ and $T_{10} . T_{9}$, enables gate of $T_{10}$ to track the input voltage applied at the source of $T_{10}$ shifted by $V_{D D}$, keeping the gate-source voltage constant regardless of the input signal. For completeness of this section, the output waveforms of the total sample-and-hold circuit are shown in Figure 2-18b).

### 2.5. Multi-Step A/D Converter Stage Design

### 2.5.1. Coarse Quantization

To maximize the settling time of the sub-D/A converter output, i.e. to achieve a high conversion speed, the coarse $A / D$ converter should be able to provide its output to the sub$\mathrm{D} / \mathrm{A}$ converter as soon as possible after the $\mathrm{S} / \mathrm{H}$ circuit samples the input and enters the hold mode. Therefore, almost without exception, the coarse A/D converter of multi-step A/D converter is of parallel, flash type [1-20] as it provides the highest throughput rate. As mentioned in Section 2.1, in the flash architecture the analog signal is simultaneously compared to every threshold voltage of the A/D converter by a bank of comparator circuits. The threshold levels are usually generated by resistively dividing one or more references into a series of equally spaced voltages, which are applied to one input of each comparator. All of the drawbacks of flash converters stem from the exponential dependence of comparator count on resolution. The large number of comparators required, $2^{N}-1$, where $N$ is the resolution of the A/D converter causes various detrimental effects: large die size which implies high cost, large device count leading to low yield, complicated clock and single distribution with significant capacitive loading, large input capacitance requiring high power dissipation in the $\mathrm{S} / \mathrm{H}$ driving the coarse $\mathrm{A} / \mathrm{D}$ converter and degrading dynamic linearity, high power supply noise due to large digital switching current and significant errors in threshold voltages caused by comparator input bias current flowing through the resistive reference ladder. These factors make implementation of flash converters above eight bits very difficult, especially if low power dissipation is required.


Figure 2-19: a) Interpolation principle, b) Interpolation in coarse $A / D$ converter implementation
The accuracy requirement for the coarse $\mathrm{A} / \mathrm{D}$ converter is equal to its effective stage resolution if the over-range is applied. The performance of a low-resolution flash A/D converter is in turn limited primarily by the accuracy of the comparators and secondarily by the accuracy of the reference. To ease the problem of the large input capacitance, the difference between the analog input and each reference voltage can be quantized at the output of each preamplifier, which is possible because of preamplifier finite gain (non-zero linear input range). This
indicates that interpolating between the outputs of preamplifiers can increase the equivalent resolution of a flash stage [134]. The interpolation technique of Figure 2-19 substantially reduces the input capacitance (from $2^{\mathrm{N}}-1$ to $2^{\mathrm{N} \text {-Nintetopolation }}$ ), power dissipation and area of flash converters, while preserving the one-step nature of the architecture, since all of the signals arrive at the input of the latches simultaneously and hence can be captured on one clock edge.


Figure 2-20: a) Left, total capacitance $C_{\text {tot }}=\left(2^{\mathrm{N}}-1\right)^{*} C_{\text {in, diff }}$ in a flash converter as a function of intrinsic preamplifier capacitance for different converter resolutions, b) Right, total capacitance $C_{\text {tot }}=\left(2^{\text {N-Nintepolating })} * C_{\text {in, diff }}\right.$ in a interpolating converter as a function of intrinsic preamplifier capacitance for different converter resolutions

Interpolation can generally be viewed as analog to digital conversion in terms of zerocrossing points rather than direct amplitude quantization; in essence, interpolation adds zero crossings to the set of input/output characteristics of a flash stage. The interpolation principle makes use of the fact that the preamplifiers are non-ideal. Instead of switching from low to high instantaneously when the input voltage exceeds the reference voltage, they follow the input signal over a limited range in a more or less linear way. Since the information contained in the preamplifiers output signals is not affected as long as the position of the zero crossing of the output signal remains unchanged, the accuracy of the converter is not affected. By scaling the amplifiers in the analog preprocessing chain from front to back also the overall power consumption can be optimized under the given gain/bandwidth constraints.


Figure 2-21: a) Left, total power consumed in a flash converter according $P_{t o t}=C_{\text {bot }} V_{D D^{2}} f s$ at $f s=60 \mathrm{MS} / \mathrm{s}$ as a function of intrinsic preamplifier capacitance for different converter resolutions, b) Right, total pover consumed in a interpolating converter according $P_{t o t}=C_{t o t} V_{D D^{2}} f_{s}$ at $f_{s}=60 \mathrm{MS} / \mathrm{s}$ as a function of intrinsic preamplifier capacitance for different converter resolutions

The gain in the pre-amplifiers reduces power consumption as well as the required accuracy of the comparators. By their parallel nature, the power dissipated by a flash converter increases by the number of quantization levels desired. So to a first order, power increases exponentially as a power of two for every additional bit of resolution (Figure 2-21). The relationship between power dissipation and sampling rate depends upon the process used and the method used to vary the circuit speed. The power of a circuit is a function of the fixed extrinsic capacitance (any capacitance that does not scale with transistor width, internally or off-chip) $C_{f x a d}$ and the maximum sample frequency $f_{S_{\text {maxx }}}$, which is some factor (4 to 50 ) lower than the device $f_{T}$ (Figure 2-21). When $f_{S}$ is much lower than $f_{S(\text { maxx })}$, the power is directly proportional to $f_{s}$. This occurs when the intrinsic capacitance $C_{\text {saled }}$, which scales with transistor $W$, is much smaller than $C_{f \text { xxed }}$. When $C_{\text {salede }}$ is much larger than $C_{f \text { xxed }}$ the asymptotic behavior takes over as $f_{s}$ approaches $f_{S(\text { max })}$. In this regime, power increase results in a diminishing increase in $f_{s}$ and is inefficient from a power utilization standpoint. The transition or break-even point between these two regimes occurs when $C_{\text {saled }}$ equals $C_{f x x e d}$. In a power-speed efficiency sense, this is the optimum power point, $P_{\text {opr }}$. The minimal power consumption is limited by the matching quality of the technology for a given speed and accuracy.

The accuracy requirements of the five bits coarse A/D converter is limited to only six bits because the fine $A / D$ converter is able to correct errors up to half a sub-range. In the implementation of the overall A/D converter the differential outputs from $\mathrm{S} / \mathrm{H}$ are compared with a static reference ladder to obtain the coarse quantization. To be able to compare two signals with a static reference a comparator is necessary, which should not have the trip point at the zero crossing but at a certain reference voltage. Therefore pre-amplifiers are used with four inputs: two inputs are connected to the $\mathrm{S} / \mathrm{H}$ analog outputs and two inputs are connected to the reference ladder. By using different references for each pre-amp all zerocrossings are generated. The maximum non-linearity errors occur at the differential amplifiers whose reference voltage is furthest from the input voltage and the non-linearity errors of the preamplifiers, which have the reference voltage closest to the input voltage and are responsible for A/D conversion, are minimized.


Figure 2-22: Transistor level implementation of coarse $A / D$ converter preamplifiers: a) first stage, b) second stage and c) bias circuit

Behind this first pre-amplifier stage, interpolation is applied and by combination of the output signals from adjacent pre-amplifiers the additional zero-crossings are generated. Interpolation lends itself to implementation in sub-micron technologies since the preamplifiers do not need to have an accurate gain, high linearity or large output swings and can be made simple to maximize the speed (Figure 2-22). Interpolation is applied again (Figure 2-24a) and these amplifiers drive thirty-three comparators. Each of the comparators compares the difference of the $\mathrm{S} / \mathrm{H}$ outputs voltages with the difference of the reference voltages prior to digital code encoding. Since this conversion technique needs only static $d c$ reference, it is
therefore naturally free from the $R C$ delay. The most important comparator specifications are offset, gain, speed, power consumption and immunity to noise and mismatch just as for op amps. As very small transistors are preferred to minimize power and area, comparators are inevitably sensitive to larger offsets. To lessen the impact of the offset voltage of comparators on the linearity of A/D converter, several schemes, such as inserting a preamplifier [1], auto-zero scheme [2] or digital background calibration [18], have been developed. In the proposed fully differential comparator shown in Figure 2-23, the consequent low offset is achieved and therefore no offset compensation is required as a result of four measures. The input signal is relatively large due to signal amplification in the preamplifier circuits. The large transresistance of the current-to-voltage conversion causes a large LSB voltage at the input of the voltage decision circuit. The two-phase clocking scheme [135] reduces the number of devices that contribute to the offset, and finally the choice of appropriate $g_{m}$-ratios further reduces the input-referred offset. As a result of the absence of offset compensation, the clock frequency is high.


Figure 2-23: a) Schematic of the proposed comparator, b) Comparator biasing circuit

The current-input latch which results from combining the input current-to-voltage conversion and the subsequent voltage decision circuit is characterized by high speed and low offset. The speed is achieved by clamping the input voltage swing in the current-to-voltage conversion circuit and by optimizing the design of the regenerative circuit. When clk is high, the output of the decision circuit is dependent on the input signals. The regenerative action of the clock combined with the preamplifier causes an imbalance in the decision circuit, forcing the outputs into a state determined by $V_{(9)}$ and $V_{(q \mathrm{~N})}$.


Figure 2-24: a) Left, some interpolated signals of the preamplifiers first and seoond stage, b) Right, the comparator switcbing

When clk is low, the cross-coupled inverters are isolated from the decision circuit; the comparator stops comparing and remembers the status of the inputs at the instant $c / k$ is switched low. Current flows through the closed resetting switches $T_{7,8}$, which force the previous two logic state voltages to be equalized. After the input stage settles on its decision, a voltage proportional to the input voltage difference is established between nodes $q$ and $q_{N}$ in the end (Figure 2-24b). This voltage will act as the initial imbalance for the following decision interval. The operation speed of the latch is determined by the regeneration time constant $\tau=C_{\text {tot }}\left(\left(g_{m n}+g_{m p}\right)\right.$ where $g_{m n}$ is transconductance of $T_{5,6}, g_{m p}$ of $T_{11,12}$ and $C_{\text {tot }}$ total capacitance at $q$ and $q_{\mathrm{N}}$. The lengths of switches $T_{7,8}$ should be small as possible because it adds parasitic junction capacitances and can introduce undesirable gain $\left(q / q_{N}\right)$. However, its width should be large enough to reset node $q$ and $q_{N}$ at the end of the reset phase to prevent hysteresis. As diode connected transistors $T_{9,10}$ limit the decision circuit result. During the decision-making they are switched off. At the output of the comparator, two inverters $T_{23,25}$ and $T_{24,26}$ are placed to buffer this information and produce a digital signal.

### 2.5.2. Fine Quantization

The coarse quantizer digitizes the input signal with low resolution, and applies the resultant digital value to a reconstruction $\mathrm{D} / \mathrm{A}$ converter. The analog output of the $\mathrm{D} / \mathrm{A}$ converter is then subtracted from the held output of $\mathrm{S} / \mathrm{H}$ to form a residue signals. The four residue signals are connected to four fine buffers, which apply the signals to both the top and bottom of two moving ladders in the fine $A / D$ converter. Although the full-parallel system (flash) implementation for the eight-bit fine A/D converter would provide a one-step operation, large number of comparators required, renders this architecture obsolete. On the other hand, folding and interpolation technique have been shown to be an effective mean of digitization of high bandwidth signals at intermediate resolution [136-137].

From a power perspective, the preamplifier stages in the folding block consume more power than a comparator at a given speed for two reasons; the output node capacitance of the folding block is about $n / 2$ times larger due to the $n$ preamp stages in a $n$ times folder and the bandwidth of the folding block needs to be about $n / 2$ times higher than a comparator from the $n / 2$ times input signal frequency multiplication by the folding action. From the prior description of the folding converter, an $m+l$ bit converter with $m$ most significant bits and $l$ least significant bits, requires $2^{\prime \prime}-1$ MSB comparators, $2^{\prime \prime \prime}$ times folding per block and $2^{\prime}-1$ folding blocks and LSB comparators. It is clear from Figure 2-25 that the folding converter consumes more power and is slower than a regular flash converter. To improve the performance of the folding converter, interpolation is used to generate half or more of the folded waveforms. Since only the zero-crossing point is important, the interpolated waveform could replace the folding block waveform, allowing its removal. Although in this case only one block is eliminated, in the case of eight-times folding, three of seven blocks could be removed using interpolation, thus approaching a saving of half the power and area as the number of folds increases, yielding a more favorable power performance than for a flash converter. For this reason, most folding converter use the modified architecture for lowdistortion coupled with interpolation to reduce the power and area.

A folding and interpolating $\mathrm{A} / \mathrm{D}$ converter determines the digital output code transitions based on the zero-crossing locations. Therefore, in order to increase the A/D converters resolution, more zero-crossings have to be created across the input range. One way to
achieve this is by increasing the number of folding amplifiers at the input. Yet, this approach will increase more parallelism, with associated power and speed penalty. The folding amplifiers also have high sensitivity to transistors matching which in turn can affect the A/D converter's performance. An alternative method to increase the number of zero-crossings is by increasing the interpolation factor. However, this approach has several drawbacks. First, more fine comparators are required at the output, which results in increased power consumption, larger area and possibly degraded speed performance. Second, as presented in [138], the signals generated by interpolation have an amplitude mismatch from the original folding signals. The folding signal obtained by interpolation only provides good approximation of the ideal folding signal around the zero-crossing. The interpolated signal itself has a different amplitude and slope. In particular, the mismatch in amplitude leads to displacement in zerocrossings when the interpolation factor is more than two. Another possible solution to circumvent the problem is to increase the number of foldings in each folding signal before interpolation.


Figure 2-25: a) Left, total capacitance $C_{\text {tot }}$ in a folding and interpolating converter as a function of intrinsic preamplifier capacitance for different converter resolutions, b) Right, total power consumed in a folding and interpolating converter according $P_{\text {tot }}=C_{\text {tot }} V_{D D^{2}} f s$ at $f s=60 M S / s$ as a function of intrinsic preamplifier capacitance for different converter resolutions and folding factors

However, inserting too many differential pairs in one folding amplifier reduces the gain of the folding amplifier. This is because an increase in the number of foldings per folding signal reduces the voltage difference between two consecutive differential pairs in the folding amplifier. The $g_{m}$ curves of the differential pairs starts overlapping; thus, deteriorating the gain of the folding amplifier. Given the limitations described in this section, the focus on improving the folding and interpolating architecture is placed on increasing the number of foldings per signal. Although, cascaded folding and interpolating architecture [108,138], alleviates the problem of overlapping $g_{m}$ curves, since folding is conducted at a lower frequency in each stage, its inherited speed-precision-area-time to market trade-off did not warrant the choice, bearing in mind fine $\mathrm{A} / \mathrm{D}$ converter design specifications.

The architecture overview of the proposed fine A/D converter is shown in Figure 2-26. Since error correction is employed in the fine A/D converter as explained in Section 2.3, additional required ranges have to be created from the residues, which are the input signals for the fine converter. By making use of dual-residue technique as will be shown in next section, fine A/D converter will not have fixed reference voltages; zero-crossings for the fine conversion are generated by interpolation with two resistor ladders.

To reduce power dissipation and capacitive loading, two stages of the interpolation preamplifiers (consisting of nine preamplifiers in the first and seventeen preamplifiers in the second stage, similar to coarse quantizer interpolation preamplifiers described in previous section) are placed in front of folding preamplifiers. At the output of the first stage preamplifiers, additional, interpolated, zero-crossings are generated between the differential output voltages of two adjacent preamplifiers as illustrated in Figure 2-27a). This second interpolation stage is controlled by dir signal, which change from high to low depending of the direction of the ladder current. The first folding stage consists of thirty-three folding amplifiers. These amplifiers generate a bell shaped signal (Figure 2-27b), which are interpolated to produce additional folds as shown in Figure 2-28.


Figure 2-26: Conceptual schematic of the proposed folding and interpolating fine $A / D$ converter, MSB generation not shown

Transistor level implementation of the first and second preamplifier stage, folding amplifier differential pair and bias circuit is shown in Figure 2-29. To illustrate the implemented folding principle into more detail, consider typical and implemented folder principle shown in Figure $2-30$. In a typical folder implementation, the inputs of the differential pairs are connected to the converter input voltage and reference voltages generated by a resistor ladder. Crossconnecting the output of every other differential pair produces the periodic transfer characteristic for this folder. The current output of the folder is converted into a voltage through the load resistors. The transfer characteristic realized in this way resembles the ideal one, but its peaks are flattened, which would result in excessive distortion in the response of the overall A/D converter if the full output range of the folder were to be resolved. This rounding problem is solved by offset parallel folding, where zero-crossing detection replaces precise level quantization. Parallel use of folding blocks increases the resolution of the A/D converter without increasing the folding rate of the system. All folding blocks have exactly the same analog behavior, although they use slightly shifted reference voltages. As the number of folds available increases, the number of levels that need to be resolved at each fold decreases proportionately for a given overall resolution. Although, employing straightforward parallel folding would lead to large number of folders to obtain sufficient resolution, which in itself would lead to large input capacitance, the interpolation technique renders this limitation to acceptable levels.

Ideally the folding amplifier should have piecewise linear transfer characteristics, but due to the mismatch between different differential pairs in the folding amplifier, the slopes of each linear segment may be different. However, mismatch between different circuit elements cause an unwanted drift in output zero-crossing and appears as if it is the offset of the differential pair. Errors such as the difference between current of the constant current sources, the deviation of the tail current from their ideal values, offsets of differential pairs, the nonlinear distribution of the reference voltages, and the mismatch between output loads contribute to the equivalent input offset of each folding cell. Nevertheless, due to the gain in the preamplifiers, offset in the differential pairs of the folding amplifier have only limited impact. Transistors with smaller dimensions can be employed limiting total capacitance at the output nodes of the folding block, and hence ensuring a large bandwidth in the folding preprocessing.


Figure 2-27: a) Left, interpolation of the first, second and third preamplifiers stages, b) Right, forming of bell-shaped folding signals in folding encoder

Additionally, the gain in the preamplifiers enables large $V_{D S A T}$ for folders, which in turn enables folding under low supply voltages. As a consequence, folder requires only differential pairs, which offers simple, fast and low supply voltage compatible solution (Figure 2-29). The folder input-output characteristic implies that the bandwidth of the signal at the output of the folder will be larger than that at the input. Second, the slew rate of the folding amplifier and interpolators also should be large enough to prevent the signal skew. Both large bandwidth and slew rate demand large bias current. Band-limiting affects the output of the folder in three ways [139]: $i$ ) it attenuates the waveform; $i$ it it introduces group delay; and $i i i)$ it alters the relative position of the zero-crossings. In an actual implementation, simple amplification is used to compensate for the attenuation without affecting the position of the zerocrossings, while the group delay is simply an overall delay in the folder output that does not influence the linearity of the converter. However, the remaining displacements of the zerocrossings, correspond to variations in the thresholds used to sample the input signal and, thus, introduce nonlinearity into the conversion process. The narrower the bandwidth of the filter at the output of the folder, the more severe the displacements, and thus the distortion of the signal, become. If the bandwidth of folding amplifier (or other analog preprocess blocks) is not large enough, the high frequency internal signal will cause the degradation of the dynamic performance. The capacitance loading the output nodes of the folder consists of the input capacitance of the following stage and the parasitic capacitances at the drains of the differential pair transistors. The latter can be quite significant [140-142]. The terminating resistors and the capacitances at the output of a folder form a bandwidth-limiting network that filters the output waveform. To combat analog bandwidth limitations a transresistance amplifier is employed [140]. The input and output impedance of the transresistance stage are
both $1 / g_{m}$ and are made low, and thus, the analog bandwidth is increased by a factor $g_{m} R$. An additional advantage is its low output impedance, which facilitates driving the next stage.


Figure 2-28: a) Left, Bell-shaped signals at the input of the folding encoder, b) Right, signal interpolation

The low-ohmic outputs outp and outn of the folding amplifier are connected to the resistive interpolation ladder. Resistive [136], current [142] or active [143] interpolation can be used to produce additional folds. In current mode interpolation the interpolating currents are split with cascode current mirrors into various fractions proportional to the current mirror size and are summed to form the fine current divisions [144]. However, the current offsets from the interpolating devices (i.e., the current mirrors) cause error in the interpolated zero crossing points. A large channel length is favorable because it yields a larger effective gate voltage, which makes the threshold offset less significant referred to the signal input. In comparison with voltage mode interpolation, current mode interpolation circuits' delay variation is much smaller. In active interpolation [143] differential pairs of folding amplifiers from Figure 2-30 are replaced by four transistor structure implementing interpolating differential pair. The drain and source connection of two extra transistors are connected to drain and sources of the original differential pair. In the output current, which is a function of both input signals, a zero crossing is realized in between the zero crossings of the two input signals.


Figure 2-29: Transistor level implementation of fine $A / D$ converter amplifiers: a) first interpolation stage, b) second interpolation stage preamplifier, c) folding amplifier differential pair and d) bias circuit

Resistive interpolation, on the other hand, offers simplicity of realization and is more power efficient solution in comparison with current interpolation. In the resistive interpolation, the linear portion of two interpolating folding waveforms must extend to the zero crossing point of each other to avoid error in the interpolated folding waveforms. The interpolatable region is half of the linear region of folding waveforms. To improve linearity in the resistive interpolation, several techniques based on resistive mesh network [138,145] and averaging [108-109]
are available. However, a common problem in such architectures is the need for over-range comparators to maintain linearity at the edges of the conversion range. A circuit technique in [146] allows reduction of the number of over-range comparators, although the technique relies on matching the termination resistor with the output resistance of the over-range blocks. Nevertheless, a special case of interpolation is two-times interpolation, where nonlinearity does not affect the accuracy of the interpolated zero crossing point, so long the interpolating folding waveforms possess symmetry and are identical in shape and is therefore utilized in this design. Additionally, in comparison to higher interpolation factor, two-times interpolation reduce the delay difference, which is caused by different impedances looking back into the interpolator from the input terminals of each comparator and similarly, relaxes the bandwidth limitation. With two-times interpolation thirty-two complementary signals from source follower are converted to sixty-four zero crossings that could drive sixty-four differential comparators corresponding to the six least significant bits. To distinguish eight possible input voltages that correspond to the same folding signal output, over-range signals are applied to additional four comparators to generate two most significant bits. Comparators of both stages are similar to the one described in Section 2.5.1 (Figure 2-31).


Figure 2-30: a) Typical and b) Implemented folder with second stage preamplifier

The low output impedance of the source follower circuit can drive the resistors directly. The $d c$ voltage drop produced by the source follower bias current across each ladder defines half of the differential full-scale range; therefore, the quantizer input range is controlled by varying the ladder bias current. Each tap on both ladders must follow the full excursion of the input signal; however, the lower taps settle prohibitively slowly due to the distributed RC delay of the comparators loading the ladders. However, signal interpolation reduces this capacitive loading on the ladder.


Figure 2-31: a) Schematic of the implemented comparator, b) Comparator biasing circuit

### 2.6. Inter-Stage Design and Calibration

### 2.6.1. Sub-D/A Converter Design

After the coarse decision is completed and a thermometer code is generated, a combination of exor gates compares every two adjacent bits of the thermometer code. The results then turn on corresponding switch in the switching matrix, which selects certain sub-range sub from the static resistor reference ladder. Suppose sub(n) is selected as shown in Figure 2-32a). By switching the proper switches four references closest to the differential input signal are selected. These references are combined together with the differential input signal to generate two differential pairs of residue signals according to: res $A=\operatorname{inp}-$ ref $A ;$ nres $A=$ inn-nref $A$; nres $B=$ inp-refB; res $B=$ inn-nrefB. Both pairs of residue signals are connected to both the top and bottom of two resistor ladders as shown in previous section. The signal changes from $\operatorname{sub}(n)$ into $\operatorname{sub}(n+1)$. One pair of reference signals ( $r e f B$ en $n r e f B$ ) remains connected by the switches, while the other pair (ref $A$ en $n r e f A)$ changes taps. As seen in Figure 2-32b), insufficient settling in the coarse $\mathrm{A} / \mathrm{D}$ converter or mismatch in the coarse comparators is translated into a quantization error and appears as a shift in the location of the quantization step causing missing codes. As mentioned in Section 2.3, use of over-range and digital correction has emerged as an effective means of coping with these errors [59,147-148]. To generate this over-range, the fine $\mathrm{A} / \mathrm{D}$ converter does not use the same references as employed by the coarse decision; it connects to reference taps shifted half a sub-range as shown in Figure 2-32c).


Figure 2-32: a) Switching of reference signals and generation of residue signals, b) Signal switching with coarse ADC error, without over-range, c) Signal switching with over-range and residue signals with over-range

The pairs of residue signals are generated in a similar way as described above. The residue signal has an in-range part as well as an under- and over-range part. When the coarse A/D converter makes an error, there are still fine comparators outside the sub-range to quantize this level. Reconstruction of the out-of-range levels is performed by adding up the properly delayed stage outputs with one-bit overlap: the MSB of fine stage is added to the $L S B$ of the coarse stage. The $L S B$ of the coarse stage is not corrected, which suggests that the coarse stage must be a full flash without over-range. The excess in hardware caused by the overrange correction is very small. In a fine stage, the number of comparators is increased, but in the sub-D/A converter, only a few extra switches are required. However, as the comparator specifications are simultaneously relaxed significantly, the effects on area and power minimi-
zation are positive. For the reconstruction in the digital domain, only a small adder is required. It is noticeable, that the $\mathrm{S} / \mathrm{H}$ operation, sub $\mathrm{D} / \mathrm{A}$ conversion and subtraction of the residue have to fulfill an accuracy requirement equal to the total resolution of the multi-step A/D converter. Thus, the resolution of a multi-step A/D converter is limited by the accuracy of the sub-D/A converter, i.e. settling and component matching.

In a standard CMOS process a medium resolution sub-D/A conversion can be performed on several ways such as based on binary weighted current sources [149] or by using current division in R-2R ladder with MOS switches [150]. The resistor-ladder architecture is by far the simplest $\mathrm{D} / \mathrm{A}$ converter implementation. Additionally, they are inherently monotonic as long as the switching elements are designed correctly and the DNL is relatively low compared to other architectures. The resistor-ladder $\mathrm{D} / \mathrm{A}$ converter is essentially a string of identical resistors in series, with the top resistor tied to power supply and the bottom resistor tied to ground (Figure 2-33). The nodes in between each resistor have different voltages depending on their proximity to power supply and by using thermometer or binary decoding on the digital signal one specific node can be selected as the correct analog voltage. The number of resistor elements determines the resolution of the resistor-ladder $\mathrm{D} / \mathrm{A}$ converter; an $n$-bit $\mathrm{D} / \mathrm{A}$ converter requires a ladder with $2^{n}$ resistors.


Figure 2-33: Resistor string $D / A$ converter
In high-speed operation, parasitic capacitors at a tap point create the voltage glitch. This transient has to settle out to the given accuracy within a given period of time, and the worst case settling occurs at the middle tap where the equivalent $R$-value is one half of the total resistance plus the switch on-resistance. This transient causes the signal dependent settling of the $\mathrm{D} / \mathrm{A}$ converter and can translate into harmonic distortion. Therefore, the R -value is designed small enough so that the worst case transient settles within twelve bit accuracy. A limit on $R$-value is set, however, by mismatches of individual resistors, which determine the overall accuracy of the generated reference voltages. It can be shown [151] assuming that the resistor values are normally distributed with mean $R$ and standard deviation $\sigma_{R}$ that the maximum mismatch $\sigma_{R} / R$ allowed for five-bit resolution and twelve-bit precision is $\leq 0.1$ percent.

### 2.6.2. Residue Amplifier

### 2.6.2.1 Offset Calibration

To build multi-step A/D converter with a large tolerance to component non-idealities (comparator offsets, etc.) redundancy is introduced by making the sum of the individual stage resolutions greater than the total resolution. The conversion accuracy thus solely relies on the precision of the residue signals; the conversion speed, on the other hand, is largely determined by the settling speed of the residue amplifier. When the redundancy is eliminated by a digital-correction algorithm, it can be used to eliminate the effects of inter-stage offset on the overall linearity [152]. However, a gain error in the residue amplifier is still critical [153]. The accumulative inter-stage gain relaxes the impact of circuit non-idealities, such as noise, nonlinearity, and offset, of later stages on the overall conversion accuracy. Consider a classical single-residue processing in multi-step A/D converter illustrated in Figure 2-34a). A gain error in the residue amplifier scales the total range of residue signal and causes an error in the analog input to the next stage when applied to any nonzero residue, resulting in residue signal not fitting in the fine $\mathrm{A} / \mathrm{D}$ converter range. If the error in the analog input to the fine ADC stage is more than one part in $2^{r}$ (where $r$ is the resolution remaining after the residue amplifier gain error), it will result in a conversion error, which can lead to non-monotonicity or missing codes [153], that is not removed by digital correction. If the references for fine converter experience the same gain as the residue signal this conversion error can be reduced [64], although it will still limit the achievable accuracy to around ten bits.


Figure 2-34: a) Single-residue and b) Dual-residue signal processing
To overcome this limitation dual-residue processing [61] as illustrated in Figure 2-34b) have been employed. According to coarse quantization decision, a first and a second residue amplifier pass the difference between the analog signal and the closest and the second closest quantization level, respectively. By passing both residues to subsequent stages, information is propagated about the exact size of the quantization step, because the sum of the two residues is equal to the difference between the two quantization levels. The absolute gain of the two residue amplifiers is therefore not important, providing that both residue amplifiers match and have sufficient signal amplitude to overcome finite comparator resolution. By making use of dual-residue technique, fine $\mathrm{A} / \mathrm{D}$ converter does not have fixed reference voltages. Conceptually, dual-residue system can be considered like two amplifiers generating zero-crossing at the edges of the sub-range. Baring that in mind, the additional required zero-crossing for
the comparators can be generated by resistive interpolation. Thus, to summarize, the dominant error contributing components in the signal path before gain is applied are the $\mathrm{S} / \mathrm{H}$, the reference ladder, the switches in the switch unit and the offset on the residue amplifiers. Sufficient power is spent to meet the noise and linearity requirements of the $\mathrm{S} / \mathrm{H}$ and matching of the reference ladder resistors is adequate for twelve-bit level. Since switches in switch matrix are simple CMOS switches designed to have low enough on-resistance to provide sufficient bandwidth for twelve bit settling of the reference signals on the residue amplifiers, the offset on the residue amplifiers remains as the only accuracy-limiting component. Therefore, to maintain speed in the residue amplifiers while accomplishing twelve bit linearity requirement, offset calibration is applied.

A wide variety of calibration techniques to minimize or correct the steps causing discontinuities in the A/D converter's stage transfer functions have been proposed [29,95-96,154-163]. The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. Analog calibration methods include in this context the techniques in which adjusting or compensation of component values is performed with analog circuitry, while the calculation and storing of the correction coefficient can be digital. When no idle time exists in the system to update the coefficients, the calibration measurements must run in the background without interrupting the normal operation. Typically, the background calibration techniques [34,95-96,160-163] are developed from the same algorithms as the foreground methods by adding hardware or software to perform the calibration coefficient measurements transparent to the normal operation. Mixed-signal chopping and calibration technique [34] applied to the residue amplifiers is one such technique, where the digital processing capability of the CMOS technology is used to extract the offset from the A/D converter output.


Figure 2-35: Transfer curve of ADC with residue amplifier offset

Because of the way of switching in dual-residue signal processing, offset on both amplifiers will have the effect on the transfer curve as shown in Figure 2-35, which gives a deterministic repeated pattern in the INL curve of the A/D converter. Thus, the offsets can be measured in the digital domain by observing at the regular digital signal at the output of the ADC. Since offset is determined randomly, it can have any value. However, contributions to overall offset can be partitioned into two components: a common $\left(V_{\text {commonen }}=\left(V_{\text {offitat }}+V_{\text {officte }}\right) / 2\right)$, which is an equal value for both amplifiers, and a differential component $\left(V_{d i f f}=\left(V_{\text {offiet }}-V_{\text {offecte }}\right) / 2\right)$, which is also equal but has the opposite sign. A common offset component reduce the over-range capability in the fine A/D converter, which results in a smaller allowable offset in the coarse

A/D converter. The differential offset component, however, directly reduces the nonlinearity of the two-step A/D converter. The total compensation loop is shown in Figure 2-36. To extract both common and differential offset components and to distinguish the offset of the residue amplifiers from the $d c$ value of the input signal of the A/D converter the chopping method [98] is applied. In general, dynamic offset-cancellation techniques can be subdivided into autozeroing and chopping techniques [164]. The fundamental difference between them is the offset handling. While the autozero principle first measures the offset and subtracts it in a next phase, chopping modulates the offset to higher frequencies. Many derivatives of these two basic offset-cancellation techniques can be found, like correlated doublesampling [164], chopper-stabilization, self-calibrating opamps or the two or three-signal approach [165] as examples of autozeroing techniques and synchronous detection, chopper amplifier, chopper-stabilization and dynamic element matching (DEM) as illustration of chopping techniques. The main characteristic of the autozero technique and its derivatives is that the offset cancellation is done in two phases. A sampling phase when the offset is measured and sampled on and an amplification phase when the sampled offset is subtracted from the input signal and amplified. However, as a consequence of the sampling action, highfrequency components are folded back to the lower-frequencies and as a result the thermal noise floor is increased by the ratio of the unity-gain bandwidth of the amplifier and the autozeroing frequency [164]. In the chopper technique the input signal is modulated to the chopping frequency, amplified and modulated back to the lower frequency. The offset is modulated only once and appears at the chopping frequency and its odd harmonics. These frequency components are then removed by a low-pass filter. In contrast to the increased white noise component of autozero amplifiers, the low-frequency noise of chopper amplifiers is almost equal to the wideband thermal noise, assuming that the chopping frequency is higher than the $1 / f$ noise corner frequency. The lower noise of the chopper technique is the main reason to use this technique for calibration of the residue amplifier.


Figure 2-36: Compensation loop
After amplification by the residue amplifiers, the signal is quantized in the fine $\mathrm{A} / \mathrm{D}$ converter. In the digital domain the data is chopped back to retrieve the original input signal, which is applied to a common and a differential offset extractor. Although, the common and differential offset component require different processing in the digital domain, both can be detected by integrating the signal at the output of the A/D converter, where the sign of both common and differential offset are extracted [34]. After a certain integration period the content of the integrator is positive if the common offset component shown in Figure 2-37a) is positive and visa versa. A differential offset component detection require additional processing, since the areas of the error curve illustrated in Figure 2-37b) will compensate each other
after integration. The necessary additional processing firstly rectifies the error areas, Figure $2-37 c$ ), before integrating the signal. The resulting sign is used to change the values of the up and down counter. The output of the counter is fed to the offset compensation D/A converter located inside the residue amplifiers, which compensates in the analog domain for the offset present in the residue amplifier. Figure 2-37d) and Figure 2-37e) illustrate how the offset is removed after a few integration cycles. The calibration does not change the values on the compensation $\mathrm{D} / \mathrm{A}$ converter when the content of the integrator is smaller then a threshold value.


Figure 2-37: a) Common offset, b) Differential offset, c) Differential offset with sub-range dependent processing, d) Integrator signal and e) Residue amplifier error

The different effects of the common and the differential offset extractors can be seen at the adders. A change caused by the common offset extractor gives both $\mathrm{D} / \mathrm{A}$ converter values a step of the same sign, while a change caused by the differential offset extractor gives a step of the opposite sign. These $\mathrm{D} / \mathrm{A}$ converters close the compensation loop, thereby removing the offset in the residue amplifiers.

### 2.6.2.2 Circuit Design

The residue amplifier two differential pairs act as sub-tractors (Figure 2-38) [163], since the circuit performs the subtraction of the input signal with the selected references from the reference ladder. The differences between the analog inputs and their respective references are subtracted in the current domain. The circuit gain of the residue amplifier reduces the accuracy (noise and matching) requirements of all circuits after this amplifier with the gain factor. The residue amplifiers provide a gain of eight before the residue signals are applied to the eight bit fine A/D converter. To reduce the dependence of the circuit gain upon the input level, which usually translates into making the gain relatively independent of the biasing currents, source degeneration of the differential input pair is applied through linear polyresistor.


Figure 2-38: Residue amplifier and part of offset compensation circuit

In this case, the circuit gain is determined by the ratio of the degeneration resistors $R_{D E G}$ and the output resistors $R_{\text {OUT }}$, and thus, the gain matching between both residue amplifiers will be predominantly determined by poly-resistor matching. The effect of the finite output impedances will lead to modulation of the total bias current and therefore affect the gain accuracy and linearity. However, since the matching of poly-resistors is sufficient, it will not limit the performance of the complete A/D converter. Additionally, as shown in previous section, the absolute gain requirement of the residue amplifiers is not essential as long as the gain values of both amplifiers have the same gain value. A current source (transistors $T_{11,12}$ ) is added to the two output resistors to generate a convenient common-mode signal. The accuracy of this common-mode output signal level will be determined by the process spread of the output resistors and the accuracy of the biasing current.


Figure 2-39: Residue amplifier biasing and common-mode feedback circuit using source followers
The biasing and common-mode feedback circuit is shown in Figure 2-39. Note that $\mathrm{R}_{1}$ and $\mathrm{R}_{2}$ have to be sufficiently large to ensure proper conditions for source followers $T_{25}$ and $T_{29}$ when a large differential swing appears at the output. The input-referred offset of the residue amplifier, which determines the accuracy of the total A/D converter, arises from mismatch between the input transistors, mismatch between current sources and poly-resistor matching. The digital offset extraction block determines the digital code, which is a measure for the offset of the amplifier, applied to the current-steering compensation D/A converter (Figure 240). The reference source is simply replicated in each branch of the D/A converter and each branch current is switched on or off based on the input code. For the binary version, the reference current is multiplied by a power of two, creating larger currents to represent higher magnitude digital signals. The compensation $\mathrm{D} / \mathrm{A}$ converter drive a current via folding nodes and further via a low ohmic cascode node to the output resistors of the amplifier to remove the offset. A nine-bit resolution has been found to be sufficient resolution of the offset compensation. Since this D/A converter only has to provide a current to compensate for the offset error its linearity is not an issue.


Figure 2-40: Offset compensation current-steering $D / A$ converter

From the residue signals, which are the input signals for the fine converter, zero-crossings for the fine conversion are generated by interpolation with two resistor ladders as shown in Section 2.5.2. The residue signals are set on these resistor ladders with buffers as illustrated in Figure 2-26.


Figure 2-41: a) Fine buffer schematic, b) Fine buffer biasing circuit

Transistor level implementation of fine buffers is shown in Figure 2-41. It consists of first folded cascode stage $\left(T_{0}-T_{7}\right)$ and source follower output stage $\left(T_{9}-T_{10}\right)$. The source follower is implemented in $p$-channel MOS in order to eliminate the non-linearity due to the body effect. Sufficient phase margin can be obtained by making the non-dominant pole $p_{2} \approx g_{n 5} / C_{G S 5}$ as large as possible. This can be achieved by increasing the transconductance of the cascode device $T_{5}$ by either increasing the width of the device or the current flowing through it. Increasing the width also increases $C_{8,5}$. Increasing the biasing current increases the power consumption. Furthermore, care have to be taken as to large increase in the bias current can cause the transistor acting as current source $T_{3}$ to move out of the strong inversion region of operation. The dominant pole is decreased by inserting the $C_{T 8}$ to improve stability of the circuit.


Figure 2-42: a) Biasing circuit of the additional current source, b) Additional current source
The direction of the current flowing in the fine ladders is determined by the selected subrange and by the chop state. Two buffers therefore have to sink the ladder current, and two buffers have to source the ladder current, depending on the sub-range and chop state. The current is reversed in a sub-range transition or a chop state change, which can cause a jump in the output signal of the buffers due to the large change in current. To restrict this effect, two current sources (Figure 2-26 and Figure 2-42) have been added at the top and bottom of both ladders to sink or source the ladder current. Now the buffers only have to deliver the error current, which is much less than the $d c$ current through the ladders.

### 2.7. Experimental Results

The prototype of the proposed two-step/multi-step A/D converter illustrated in Figure 2-43 and described in this chapter was fabricated in a five-metal layers $0.18-\mu \mathrm{m}$ CMOS process. The chip has three independent power supplies and grounds: two for analog and digital blocks and one for the output drivers. The supply voltages are provided by HP3631A and the reference current sources are generated by Keithley 224. Potentiometers are used to adjust the reference voltages and the common mode voltage. The clock reference for signal generation, $\mathrm{A} / \mathrm{D}$ converter clock generation and data capturing are generated by the Agilent 81134A. A single frequency, sinusoidal input signal is generated by an arbitrary waveform generator (Tektronix AWG2021) and applied at the first to a narrow, band-pass filter to remove any harmonic distortion and extraneous noise, and then to the test board. The signal is connected via $50 \Omega$ coaxial cables to minimize external interference. On the test circuit board, the single-ended signal is converted to a balanced, differential signal using a transformer. The common-mode voltage of the test signal going into the A/D converter is set through matching resistors connected to a voltage reference. The digital output of the proposed A/D converter is buffered with an output buffer to the drive large parasitic capacitance of the lines on the board and probes from the logic analyzer. The digital outputs are captured by the logic analyzer (Agilent 1682AD). A clock signal is also provided to the logic analyzer to synchronize with the A/D converter. All the equipment is set by a LabView program, which also does the signal analysis.


Figure 2-43: Prototype two-step/multi-step $A / D$ converter with mixed-chopping calibration algorithm
The A/D converter itself must deal with issues such: routing of critical paths, power and ground isolation, noise coupling from the digital sections to the analog sections, shielding of clock lines, etc. In order to reduce wiring capacitance in the input path, front-end sample and hold input is routed as symmetrical and short as possible. Power and ground lines with maximal allowed width are overall routed to reduce the voltage drop. Since the analog sections are susceptible to noise coupling from the digital sections, they are constantly kept separated. Critical clock lines have been provided with shielding. In mixed-signal chips, it is often unclear what the best strategy is for minimizing the impact of noise coupling from the digital circuitry to the sensitive analog circuitry via the common substrate. The most effective way to reduce substrate noise is to create a low-impedance path from the $p+$ substrate to
ground (or the lowest potential in the chip). Typically, however, the backside of the die is oxidized by exposure to air, which increases its resistance. Thus even if the die is conductively attached to a package with a grounded cavity, the resistance to the substrate is high. If cost permits, the backside of the die can be back-lapped (ground down), gold-coated, and conductively attached to package. In this prototype, the following approach was taken: separate supply rails were used for the digital and analog signals, which were named $V_{D D D}, V_{S S D}$, $V_{D D A}$, and $V_{S S A}$ respectively. Since an $n$-well process was used, the digital and analog $p$ channel transistors were naturally isolated by separate wells. The $n$-channel transistors, however, interact via the common, high-resistance $p+$ substrate. The $p+$ substrate has the advantage that it makes it difficult to create latch-up, which is critical for digital circuits and creating a high resistance path for the coupling of undesired signals. Because noise travels almost exclusively in the $p+$ region, traditional isolation using grounded $n$-well guard rings to collect noise is not effective [166]. For the analog $n$-channel transistors, it is important that the source-to-body voltage is constant. Otherwise, if these voltages move relative to each other, the drain current is modulated through the body effect. Therefore, it is important to locally have a low-resistance path from body to source. In the layout, a $p+$ substrate ring was placed around each $n$-channel analog transistor.


Figure 2-44: Chip micrograph

This ring was then contacted to $V_{S S \mathcal{A}}$, which is the same potential as the source for commonsource devices. This helps keep the potential of the source and the body the same. For cascode $n$-channel devices, this arrangement helps reduce fluctuations on the body terminal, but it cannot guarantee that the source and body will move together (since the source is not at ground potential). For cascode devices, however, the relationship between drain current and $V_{S B}$ is much weaker due to source degeneration. Enough of these $V_{S S A}$ substrate contacts are used to make the source-to-body path low resistance. $V_{D D A}$ and $V_{D D D}$ were generated by separate but equal voltage regulators to allow the supply currents to be measured independently. All analog paths were differential to increase the rejection of common mode noise, such as substrate noise and supply voltage fluctuations. To reduce switching noise on power supply lines on-chip decoupling capacitors are employed. Decoupling capacitors act like local power supplies during the switching instant. Thus, most of the current can be drawn from decoupling capacitors instead of directly from the power supplies, which would signal a reduction in the current from an off-chip supply flowing through the parasitic impedance of a package and reduction of the switching noise associated with the current.

A chip microphotograph of the $\mathrm{A} / \mathrm{D}$ converter is shown in Figure 2-44. The sample-and-hold circuit with hold capacitance is clearly visible in left part, coarse part with switching matrix is situated right of $\mathrm{S} / \mathrm{H}$ circuit, while fine part, residue amplifiers, choppers, biasing, calibration and the rest of the circuits are placed further up right. Digital parts are situated on the top right side of layout. Routing of the digital signals such as clocks and data outputs is placed between digital parts. Digital outputs leave the chip from the lower and the right sides of the chip. Using this total arrangement there is a minimum of analog and digital signal lines crossings. The sample and hold input is the most critical node of the realized integrated circuit. Therefore, a great deal of care was taken to shield this node from sources of interference. The total sample-and-hold consists of three identical interleaved sample-and-hold units. S/H units, input signals, critical clock lines and output signal lines have been all provided with shielding and routed as short and symmetrical as possible. In the coarse $A / D$ converter the nine preamplifiers of the first stage must align with seventeen preamplifiers of the second stage and thirty-three coarse comparators implying that a high aspect ratio is necessary for the preamplifier and comparator layout. The switch unit is placed near the reference ladder to reduce the resistor-ladder $\mathrm{D} / \mathrm{A}$ converter settling time. Although the resistor ladder is placed at some distance from the comparators, this is bearable, since the comparators should have only six bits precision. Selected reference signals from the switch unit are routed as short as possible, since the delay due to the wiring capacitance increases the residue amplifier settling time. The delay due to the wiring capacitance causes residue amplifier to momentarily develop its output in the wrong direction until the correct selection switch closes. After the correct switch is selected, the output starts to converge in the correct direction.

| Technology | Digital CMOS $0.18 \mu \mathrm{~m}$ |
| :---: | :---: |
| Resolution | 12 bit |
| Supply voltage | 1.8 Volt |
| Sample rate | $>60 \mathrm{MSample} / \mathrm{s}$ |
| Effective bandwidth | 30 MHz |
| DNL | $\pm 0.9 \mathrm{LSB}$ |
| INL | $\pm 1.5 \mathrm{LSB}$ |
| SNR | 66.3 dB |
| SFDR | 78.4 dB |
| THD | 73.1 dB |
| SNDR | 65.1 dB |
| Power dissipation | 100 mW |
| Area | $0.67 \mathrm{~mm}^{2}$ |

TABLE II - MEASURED PERFORMANCE OF A 12-bIT PROTOTYPE

Therefore, the wiring capacitance increases the residue amplifier settling time due to the wires. If reference ladder is placed nearer, the reference signals for the comparators could be easily corrupted due to the coupling of the large digital signals traveling nearby. The three stages of the preamplifiers and folding encoder are laid out in a linear array, similar to the coarse $A / D$ converter preamplifiers, and connected to the comparator array by abutment. The comparator array must align with preamplifiers, implying that high aspect ratio is necessary for the comparator layout. Locating these arrays close to each other greatly reduces wiring capacitance providing maximum speed. To keep the comparator array small and the wires short, data is driven out of the array immediately after amplification to full swing. Clocks are distributed from right to left, to partially cancel the sample time variation with reference level that increases from left to right. The comparators with complementary clocks are interleaved, sharing the same input, reference and supply wires so that charge kickback and supply noise are cancelled to first order. The die area is 0.9 mm by 0.75 mm excluding the bond pads. The complete A/D converter core draws 53 mA from a 1.8 V voltage supply, excluding output buffers, resulting in a less then 100 mW power consumption, of which 6.6
mW is drawn by the digital core for sample frequencies up to $80 \mathrm{MS} / \mathrm{s}$. Measurements across 25 samples show $\pm 0.2$ ENOB variations. A code density test [35] was conducted to obtain static linearity of the proposed A/D converter. The measured DNL and INL are shown in Figure 2-45. From the figures, the maximum value of DNL and INL are 0.9 LSB and 1.5 LSB at twelve bit level, respectively.


Figure 2-45: a) Measured DNL, b) Measured INL
The dynamic performance of the proposed A/D converter is measured by analyzing a Fast Fourier Transform (FFT) of the digital output codes for a single input signal. Figure 2-46a) illustrates the spectrum of the output codes of the A/D converter with an input frequency at 21 MHz sampled at 60 MHz . The largest spike, other than the fundamental input signal, is the spurious harmonic which appears at $f_{s} / 3 \pm f_{\text {in }}$ and is about 78 dB below the fundamental signal. The SNR, SFDR and THD as a function of input frequency are shown in Figure 2-46b). All measurements were performed with a $1.8-\mathrm{V}$ supply at room temperature $\left(25{ }^{\circ} \mathrm{C}\right)$. The measured results are summarized in Table II. The degradation with a higher input signal is mainly due to the parasitic capacitance, clock non-idealities and substrate switching noise. Parasitic capacitance decreases the feedback factor resulting in an increased settling time constant. Clock skew, which is the difference between the real arrival time of a clock edge and its ideal arrival time of a clock edge, can also be caused by parasitic capacitance of a clock interconnection wire. The non-idealities of clock such as clock jitter, non-overlapping period time, finite rising and fall time, unsymmetrical duty cycle are another reason for this degradation.


Figure 2-46: a) Measured frequency spectrum at $60 \mathrm{MS} / \mathrm{s}$ with an input frequency at 21 MH \% b) Measured SNR , THD, SFDR as a function of input frequency

The three latter errors reduce the time allocated for the setting time. These errors either increase the noise floor or cause distortion in the digital output spectrum resulting in decreased SNR and SNDR. As an input frequency and resolution increase, the requirement for clock jitter [167] is getting more stringent. In other words, a clock jitter error will degrade the SNR even more as an input frequency approaches Nyquist input frequency. A locked histogram test revealed a $3.2-\mathrm{ps}$ rms jitter in the system including the clock generator, the synthesizer, the A/D comparator chip and the board, which translates to a $64-\mathrm{dB}$ SNR at 30 MHz approximately. This confirms the observation that the performance of this converter is limited by the clock jitter at high input frequencies.

### 2.8. A/D Converters Realization Comparison

In this section, a number of recently published high resolution analog to digital converters are compared. Tables III through VI show the FoM of the realized A/D converters from 1998 until 2008 distributed over the categories: flash, two-step/multi-step/subranging, pipeline and parallel pipeline. Normalizing the dissipated power $P$ to the effective resolution ENOB and to the effective resolution bandwidth ERBW , the Figure of Merit, FoM $=P /\left(2^{E N O B} \times 2\right.$ $E R B W)$ ) [168], is a measure for the required power per achieved resolution per conversion. Today, the state-of-the-art FoM for Nyquist A/D converters is around $1 \mathrm{pJ} /$ conversion, which means that $1 p J$ per conversion cycle is required to convert an analog signal to a single bit.

From Table III it can be seen that the flash architecture is (barely or) not used at all for accuracies above six bits due to the large intrinsic capacitance required. The most prominent drawback of flash $\mathrm{A} / \mathrm{D}$ converter is the fact that the number of comparators grows exponentially with the number of bits. Increasing the quantity of the comparators also increases the area of the circuit, as well as the power consumption. Other issues limiting the resolution and speed include nonlinear input capacitance, location-dependent reference node time constants, incoherent timing of comparators laid out over a large area, and comparator offsets. To lessen the impact of mismatch in the resistor reference ladder and the unequal input offset voltage of the comparators on the linearity of ADC, several schemes, such as inserting a preamplifier [1] in front of the latch, adding a chopper amplifier [2] and auto-zero scheme to sample an offset in the capacitor in front of the latch or digital background calibration [18] have been developed. Alternatively, the offsets and input capacitance can be reduced by means of distributed pre-amplification combined with averaging [109] and possibly also with interpolation [169]. As thin oxide improves the matching property of transistors, smaller devices can be used in newer technology generations to achieve the same matching accuracy; this fact has been exploited by many recent works of flash-type converters to improve the energy efficiency of the conversion.

The realized FoM of the two-step/multi-step or subranging architectures is relatively constant for different values of the ENOB. In Table IV it was shown that the FoM of a two-step/multistep or subranging converter increases less rapidly than the noise-limited architectures such as multi-stage pipeline. Although the number of comparators is greatly reduced from the flash architecture, path matching is a problem and in some cases the input bandwidth is limited to relatively low frequency compared to the conversion rate [23-24,26]. Fine comparators accuracy requirements can be relaxed by including an inter-stage gain amplifier to amplify the signal for the fine comparator bank [22,25]. While both, $\mathrm{D} / \mathrm{A}$ converter and input of the residue amplifier require full resolution requirement, the coarse $\mathrm{A} / \mathrm{D}$ converter section
requirement can be relaxed with the digital error correction. If one stage subtracts a smaller reference than it nominally should due to the comparator offset, the subsequent stages compensate for this by subtracting larger references. This widely-employed error correction method is referred to as redundant signed digit (RSD) correction, which was firstly developed for algorithmic ADCs in [147-148] and later utilized in pipelined ADC [59]. Other related methods have also been used [54].

| Ref | $N$ | $E N O B$ | $f_{s}[M S / s]$ | $E R B W[M H z]$ | $P[m W]$ | $F o M / p]]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $[8]$ | 6 | 5.8 | 500 | 160 | 225 | 12.6 |
| $[9]$ | 6 | 5.2 | 500 | 250 | 330 | 17.3 |
| $[11]$ | 6 | 5.2 | 1300 | 750 | 545 | 11.4 |
| $[13]$ | 6 | 5.2 | 22 | 11 | 0.48 | 0.6 |
| $[14]$ | 6 | 5.3 | 1300 | 600 | 600 | 12.7 |
| $[15]$ | 6 | 5.4 | 2000 | 1000 | 310 | 3.5 |
| $[16]$ | 6 | 5.7 | 1200 | 600 | 135 | 2.2 |
| $[17]$ | 6 | 5.2 | 4000 | 1000 | 990 | 13.5 |
| $[19]$ | 5 | 4.7 | 1000 | 200 | 46 | 1.8 |
| $[20]$ | 5 | 4.0 | 5000 | 2500 | 102 | 1.3 |

TABLE III - TABLE OF REALIZED FLASH A/D CONVERTERS

The redundancy allows for quantization errors as far as the residue stays in the input range of the next stage. The errors can be static or dynamic; it is only essential that the bits going to the correction logic circuitry match those which are $\mathrm{D} / \mathrm{A}$ converted and used in residue formation. The same correction method can easily be expanded to larger resolution stages as well. As a minimum, one extra quantization level is required [170], but for maximum error tolerance the nominal number of comparators has to be doubled. The level of error tolerance on the coarse $\mathrm{A} / \mathrm{D}$ converter section depends on how much digital error correction range the fine A/D converter section can provide. The correction range varies from $\pm 3$ LSB's in [24] to a much larger value in $[22,25]$ with an $\mathrm{S} / \mathrm{H}$ inter-stage amplifier.

If over/under-range protection is used, the offset requirements for the coarse converter can be greatly relaxed; but the fine one shares similar matching concerns as the flash architecture. Interpolation can be applied as well to reduce the number of preamps and their sizes. A balanced design can often achieve energy efficiency per conversion close to that of the pipeline converters. Since the two-step/multi-step architecture is matching limited, calibration can be applied to reduce the intrinsic capacitance. Two approaches can be taken to calibrate out the errors: mixed signal or fully digital. In mixed signal calibration, the erroneous component values are measured from the digital output and adjusted closer to their nominal ones [34]. The correction is applied to the analog signal path and thus requires extra analog circuitry.

| Ref | $N$ | $E N O B$ | $f_{s}[M S / s]$ | $E R B W[M H z]$ | $P[m W]$ | $F o M[p J]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 30 | 10 | 9.1 | 25 | 12.5 | 195 | 14.2 |
| 31 | 14 | 12 | 100 | 50 | 1250 | 3.1 |
| 32 | 12 | 10.3 | 50 | 25 | 850 | 13.5 |
| 33 | 13 | 11.1 | 40 | 15 | 800 | 12.1 |
| 34 | 12 | 10.3 | 54 | 4 | 295 | 29.2 |
| 35 | 10 | 9.1 | 160 | 10 | 190 | 17.3 |
| Ch $2[37]$ | $\mathbf{1 2}$ | $\mathbf{1 0 . 5}$ | $\mathbf{6 0}$ | $\mathbf{3 0}$ | $\mathbf{1 0 0}$ | 1.1 |
| 38 | 15 | 10.8 | 20 | 2 | 140 | 19.7 |
| 50 | 12 | 10.1 | 40 | 20 | 30 | 0.7 |

TABLE IV - TABLE OF REALIZED TWO-STEP/MULTI-STEP/SUBRANGING A/D CONVERTERS

In the fully digital approach the component values are not adjusted [171]; however, the accuracy of this method depends on the accuracy of the measurement. In the sub-ranging converter the absence of a residue amplifier places stringent offset and noise requirements on the second quantizer, which can be overcome at modest power dissipation through the use of auto-zeroing [48], averaging [50] or background offset calibration [49]. The utilization of time-interleaved second quantizers increases the effective sampling rate [46].

The FoM of the pipeline converter increases as a function of the realized ENOB (Table V). The architecture has evolved by making use of the strengths of the switched capacitor technique, which provides very accurate and linear analog amplification and summation operations in the discrete time domain. When the input is a rapidly-changing signal, the relative timing of the first stage $\mathrm{S} / \mathrm{H}$ circuit and the sub-ADC is critical and often relaxed with a front-end $\mathrm{S} / \mathrm{H}$ circuit. Consecutive stages operate in opposite clock phases and as a result one sample traverses two stages in one clock cycle. So, the latency in clock cycles is typically half the number of stages plus one, which is required for digital error correction. For feedback purposes, where low latency is essential, a coarse result can be taken after the first couple of stages. The different bits of a sample become ready at different times. Thus, digital delay lines are needed for aligning the bits.

| Ref | $N$ | $E N O B$ | $f_{S}[M S / s]$ | $E R B W[M H z]$ | $P[m W]$ | $F o M[p J]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 66 | 12 | 11.1 | 20 | 10 | 250 | 5.7 |
| 66 | 14 | 12 | 20 | 10 | 720 | 8.8 |
| 72 | 14 | 12.5 | 2.5 | 1.2 | 145 | 5.0 |
| 73 | 12 | 10.5 | 100 | 50 | 390 | 2.2 |
| 74 | 10 | 9.3 | 80 | 40 | 69 | 1.4 |
| 75 | 12 | 10.4 | 110 | 10 | 97 | 3.6 |
| 76 | 10 | 9.4 | 100 | 50 | 67 | 1.0 |
| 78 | 10 | 8.6 | 200 | 90 | 55 | 0.8 |
| 80 | 14 | 13.1 | 125 | 60 | 1850 | 1.7 |
| 84 | 11 | 10.5 | 45 | 5 | 81 | 5.6 |

TABLE V - TABLE OF REALIZED PIPELINED A/D CONVERTERS

Several techniques for achieving resolutions higher than what is permitted by matching have been developed; the reference feedforward technique [55] and commutated feedback capacitor switching [56] improve the differential non-linearity, but do not affect the integral nonlinearity. In 1 -bit/stage architecture the capacitive error averaging technique, which has previously been used in algorithmic ADCs [171] can be used [66]. With it, a virtually capacitor ratio-independent gain-of-two stage can be realized. The technique, however, requires two opamps per stage (a modification proposed in [70]) and needs at least one extra clock phase. Pipeline architecture has been found very suitable for calibration [57,62]. The number of components to be calibrated is sufficiently small, since only the errors in the first few stages are significant as a result of the fact that, when referred to the input, the errors in the latter stages are attenuated by the preceding gain. Furthermore, no extra A/D converter is necessarily required for measuring the calibration coefficients, since the back-end stages can be used for measuring the stages in front of them.

Similar to a subranging converter, over/under-range protection is necessary in a pipeline A/D converter. Since the comparator offset specs are substantially relaxed due to a low stage resolution and over/under-range protection, comparator design in pipeline A/D converters is far simpler than that of the flash ones, and usually does not impose limitation on the overall conversion speed or precision. It is how fast and how accurate the residue signals can be
produced and sampled that determines the performance of a pipeline converter, especially for the first stage that demands the highest precision. Negative feedback is conventionally employed to stabilize the voltage gain and to broaden the amplifier bandwidth. It is expected that with technology advancement, the accompanying short-channel effects will pose serious challenges to realizing high open-loop gain, low noise, and low power consumption simultaneously at significantly reduced supply voltages. The tradeoff between speed, dynamic range, and precision will eventually place a fundamental limit on the resolution of pipeline converters attainable in ultra-deep-submicron CMOS technologies.

The realized FoM of the parallel pipeline architectures is severely limited by the required power (Table $V I)$. Up to a certain resolution, component matching is satisfactory enough and the errors originating from channel mismatch can be kept to a tolerable level with careful design. High-resolution time-interleaved A/D converters, however, without exception, use different techniques to suppress errors. The offset can be rather easily calibrated using a mixed signal [172] or all-digital circuitry [91]. Calibrating the gain mismatch is also possible, but requires more complex circuitry than offset calibration [95-96]. The timing skew may originate from the circuit generating the clock signals for different channels or it may be due to different propagation delays to the sampling circuits. Skew can be most easily avoided by using a full-speed front-end sample-and-hold circuit [154]. The A/D converter channels resample the output of the $\mathrm{S} / \mathrm{H}$ when it is in a steady state, and so the timing of the channels is not critical. However, the $\mathrm{S} / \mathrm{H}$ circuit has to be very fast, since it operates at full speed.

| Ref | $N$ | ENOB | $f_{s}[M S / s]$ | ERBW $[M H \approx]$ | $P[m W]$ | FoM $[$ p $]]$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 94 | 8 | 7.6 | 75 | 35 | 75 | 5.5 |
| 95 | 10 | 9.4 | 40 | 20 | 650 | 24.1 |
| 96 | 10 | 9.5 | 40 | 10 | 565 | 39.0 |
| 98 | 10 | 9.4 | 120 | 20 | 234 | 8.7 |
| 100 | 10 | 9.7 | 120 | 2 | 75 | 22.5 |
| 102 | 10 | 9.4 | 200 | 60 | 104 | 1.3 |
| 103 | 8 | 7.8 | 150 | 75 | 71 | 2.1 |
| 104 | 11 | 9.4 | 800 | 400 | 350 | 0.65 |
| 105 | 15 | 12.3 | 125 | 60 | 909 | 1.5 |

TABLE VI - TABLE OF REALIZED PARALLEL-PIPELINED A/D CONVERTERS

### 2.9. Conclusion

Practical realizations from Section 2.8 (Figure 2-47) show the trend that to a first order, converter power is directly proportional to sampling rate $f_{s}$ when $f_{s}$ is much lower than the device technology transition frequency $f_{T}$. However, power dissipation required becomes nonlinear as the speed capabilities of a process technology are pushed to the limit. In the case of constant current-density designs, there is an optimum power point when total intrinsic capacitance equals total extrinsic capacitance, beyond which power increases yield diminishing returns in speed improvements.

Power dependence on converter resolution is not as straight-forward as its dependence on $f_{S}$ because converter architecture also varies with resolution. Flash converters dominate at the high-speed low-resolution end of the spectrum while pipelined converters are usually employed at the low-speed high-resolution end typically from eight to twelve bits without calibration and up to fifteen bits with calibration. The inter-stage gain makes it possible to scale the components along the pipeline, which leads to low power consumption. Resolutions up
to fifteen bits can be covered with two-step/multi-step/subranging converters or with an architecture which is a combination of these. Pipeline and two-step/multi-step converters tend to be the most efficient at achieving a given resolution and sampling rate specification. Its power proficiency for high resolution is demonstrated with prototype [37] in this Chapter.


Figure 2-47: a) Energy versus $S N D R$ for $A / D$ converters shown in Table III-VI, b) Effective resolution bandwidth versus SNDR for $A / D$ converters shown in Table III-VI

The explosive growth of portable multimedia devices has generated great demand for low power A/D converters. With an increasing trend to a system-on-chip, an A/D converter has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other digital circuits. Fundamental limitations to the power dissipation of key functions for high speed A/D converters, such as sampling, quantization and reference generation in each case are dictated by accuracy consideration. The power proficiency for high resolution of multi-step converter by combining parallelism and calibration and exploiting low-voltage circuit techniques is demonstrated with a $1.8 \mathrm{~V}, 12$-bit, $80 \mathrm{MS} / \mathrm{s}, 100 \mathrm{~mW}$ analog to-digital converter fabricated in five-metal layers $0.18-\mu \mathrm{m}$ CMOS process. As shown in Figure 2-48, comparison of the figure of merit of all A/D converters (flash, folding and interpolating, multi-step, pipelined, parallel pipelined, successive approximation and sigma-delta) published at ISSCC and ESSIRC in the last ten years shows that this prototype ranks among the best reported.


Figure 2-48: a) Energy versus SNDR for A/D converters published at ISSCC and ESSIRC in the last ten years, b) Effective resolution bandwidth versus SNDR for $A / D$ converters publisbed at ISSCC and ESSIRC in the last ten years

## CHAPTER 3.

## MULTI-STEP ANALOG TO DIGITAL CONVERTER TESTING

Complex System-on-Chip, SoC, realizations require an A/D converter embedded in a large digital IC to be testable. Since these converters are embedded in the SoC, it is difficult to access all of their ports and as such existing test practices are not always applicable, or need to be revised. This implies also that test times need to be reduced to acceptable limits within the digital-testing time domain; it also implies the incorporation of Design-for-Testability (DfT), Built-in-Self-Test (BIST) and silicon debug techniques. In an attempt to address these issues, this chapter focuses on a novel computer-aided, DfT and BIST techniques to augment analysis of converter's performance.

### 3.1. Analog ATPG for Quasi-Static Structural Test

For SoCs, many of the tests exercised at final test are being migrated to wafer test, partly because of the need to deliver known good dies before packaging, and partly because of the need to lower analog test costs. A typical test flow allocates test times to wafer test and final test. More traditionally, a wafer test consists primarily of $d c$ tests with current/voltage checks per pin under most operating conditions and with the test limits properly adjusted and in some cases some low-frequency tests to ensure functionality. A wafer test is geared to check open/short circuits, $d c$ biases, charge-pump currents, and logic leakage among other parameters. A final test consists of checking device functionality by exercising tests to cover important circuit parameters. However, with the advent of new packaging techniques and pressure on test costs, traditional functional tests at package level are being pushed backwards to wafer level. Under this new scenario, wafer testing is performed to determine the true performance of the die independent of the packaging.

Structural, fault-orientated testing [174-179] is a convenient mean to avoid functional testing at wafer-level test. These low-frequency test techniques depart from the traditional role of current/voltage $d c$ checks and are rather applicable for substituting or complementing functional tests. Fault-oriented test involves the use of a fault model to describe the behavior of a real defect, or set of defects. The fault model is then used to establish the faulty behavior of the circuit so that new tests can be derived or the effectiveness of existing tests investigated. The fault model cannot only describe the fault effect clearly and offer clues to derive the test stimuli, but also makes it feasible to modify input stimuli and estimate fault coverage. This approach is well established for digital circuits for which there are numerous test pattern generators and fault simulators based on a zero/one decision, as is the case of the single-stuck-at fault model. However, due to the continuous nature of analog circuits, the distinction between the fault-free circuit and the faulty circuit is not as clear as in the digital case.

The statistical variations of the process parameters and component tolerances make that tolerance windows on the measurements have to be used to make a decision during fault detection. In addition, derivation of an acceptable tolerance window is aggravated with the presence of the overlap regions in the measurement values of the fault-free and faulty circuits, resulting in ambiguity regions for fault detection.

Several studies [180-185] have revealed that faults which shift the operating point of a transis-tor-level analog circuit can be detected by inexpensive $d c$ testing or power supply current monitoring. A model in [180] tests analog circuits by measuring the $d c$ voltage at different nodes. The relationship between the parameters, such as voltage and current, at component interconnections represents their behavior. This model deduces the values of parameters within the circuit by propagating the effect of the measurement through this model. In [181] a $d c$ test selection procedure was presented where the detection criteria included the effect of parameter tolerance with a linear approximation around the nominal values. In [182], to include the effect of parameter tolerance during testing, the test generation problem is formulated as a min-max optimization problem and solved iteratively as successive linear programming problems. An approach for the fault detection based on Bayes decision rule for $d c$ testing is presented in [183] by combining the a priori information and the information from testing. Principle component analysis is applied for the calculation of the discrimination function in the case of the measurements being dependent. However, the tests are obtained using simulation of a number of circuits and recording the percentage of good and faulty devices misclassified. The parametric fault simulation and test vector generation in [184] utilizes the process information and the sensitivity of the circuit principal components in order to generate statistical models of the fault-free and faulty circuit. The Bayes risk is computed for all stimuli and for each fault in the fault list. The stimuli for which the Bayes risk is minimal, is taken as the test vector for the fault under consideration. In [185], the measurement events are classified according to the regions that data fall into and the statistical profiles of the measurable parameters for each parametric fault are obtained. By iteratively conducting the tests and applying the Bayesian analysis, the occurrence probability of each fault is found.

The Neyman-Person statistical detector [186], which is a special case of the Bayes test, provides a workable solution when the a priori probabilities may be unknown, or the Bayes risk may be difficult to evaluate or set objectively. The study in this section [187] utilizes those findings. In this approach altering the circuit's biasing conditions generate various functional faults encountered in analog circuits. As seen from experimental results [188] acting on the circuit in such way a satisfactory level of correlation between structural and functional testing can be accomplished. After parameter extraction, sets of bounds of signal values that can occur for fault-free circuits and circuits with specific faults, respectively, are generated and the deviations of the circuit's quasi-static node voltages are calculated through the accessed variations of the extracted process parameters. With Karhunen-Loève expansion method, hereby proposed [189], the parameters of the devices are modeled as stochastic processes over the spatial domain of a die, thus making parameters of any two devices on the die, two different correlated random variables. Additionally, a fault model is verified according to performance specifications if one accounts for possible process parameter spread in a computation of a tolerance range. The variation in absolute value of process parameters is considered, as well as the differences between related elements, i.e. matching.

### 3.1.1. Test Strategy Definition

In this approach the circuit under test is excited with a quasi-static stimulus to sample the response at specified times to detect the presence of a fault. The waveform is systematically formed from piecewise-linear ramp segments that excite the circuit's power supply, biasing, reference and inputs, which forces the majority of the transistors in the circuit to operate in all the regions of operation, and hence, provide bias currents rich in information. To apply the power-supply-current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques, since the method requires more than a simple coarse observation of abnormal currents at the power supply network. Analog faulty behaviours are not so pronounced as those in the digital case, and due to the resolution limitations of the power-supply-current observation technique, the device under test has to be subjected to a design for testability methodology which consists of partitioning the circuit to reach better current observability. The method measures current signatures, not single values. Many faults have unique or near-unique signatures, easing the diagnosis process. Indeed it is independent of the linearity or nonlinearity of the systems, circuit or component.


Figure 3-1: ATPG - proposed top-level flow diagram

The proposed top-level test generation flow diagram is shown in Figure 3-1. Firstly a tolerance window is derived according to test stimuli and test program. The circuit is simulated without any faults and the results of this test are saved in a database. The next step is to sequentially inject the selected faults into the circuit and simulate according to the same test stimuli and test program as used to derive the tolerance window. All simulation results are saved in the database, from where the fault coverage can be calculated in conformance with the tolerance window and discrimination analysis. To derive necessary stimuli, the test stimuli optimization is performed on the results available in the database.

### 3.1.2. Linear Fault Model based on Quasi-Static Nodal Voltage Approach

### 3.1.2.1 General Network Analysis

Modern integrated circuits are often distinguished by a very high complexity and a very high packing density. The numerical simulation of such circuits requires modeling techniques that allow an automatic generation of network equations. Furthermore, the number of independent network variables describing the network should be as small as possible. Circuit models have to meet two contradicting demands: they have to describe the physical behavior of a circuit as correct as possible while being simple enough to keep computing time reasonably small. The level of the models ranges from simple algebraic equations, over ordinary and partial differential equations to Boltzmann and Schrodinger equations depending on the effects to be described. Due to the high number of network elements (up to millions of elements) belonging to one circuit one is restricted to relatively simple models. In order to describe the physics as good as possible, so called compact models represent the first choice in network simulation. Complex elements such as transistors are modeled by small circuits containing basic network elements described by algebraic and ordinary differential equations only. The development of such replacement circuits forms its own research field and leads nowadays to transistor models with more than five hundred parameters.

A well established approach to meet both demands to a certain extent is the description of the network by a graph with branches and nodes. Branch currents, branch voltages and node potentials are introduced as variables. The node potentials are defined as voltages with respect to one reference node, usually the ground node. The physical behavior of each network element is modeled by a relation between its branch currents $j$ and its branch voltages $v$. In order to complete the network model, the topology of the elements has to be taken into account. Assuming the electrical connections between the circuit elements to be ideally conducting and the nodes to be ideal and concentrated, the topology can be described by Kirchhoff's laws (the sum of all branch currents entering a node equals zero and the sum of all branch voltages in a loop equals zero). One elegant way to describe the network topology is by the (reduced) incidence matrix $\mathbf{A}=\left(a_{i j}\right)$ that express the relation between all nodes (except the ground node) and all branches of the network. It is defined as: $a_{i j}=1$ if the branch $j$ leaves the node $i, a_{i j}=-1$ if the branch $j$ enters the node $i$, and $a_{i j}=0$ otherwise. Let a connected network with $n$ nodes and $b$ branches be given. If $\mathfrak{j}=\left(j_{1}, j_{2}, \ldots, j_{b}\right)^{T}$ is the vector of all branch currents of the circuit, then Kirchhoff's current law (KCL) implies

$$
\begin{equation*}
\mathbf{A} \cdot \mathbf{j}=0 \tag{3-1}
\end{equation*}
$$

The incidence matrix allows, additionally, a simple description of the relation between node potentials and branch voltages of the network. If $\mathbf{v}=\left(v_{1}, v_{2}, \ldots, v_{b}\right)^{T}$ is the vector of all branch voltages and $\mathbf{e}=\left(e_{1}, e_{2}, \ldots, e_{n-1}\right)^{T}$ denotes the vector of all node potentials, then the relation

$$
\begin{equation*}
\mathbf{v}=\mathbf{A}^{T} \mathbf{e} \tag{3-2}
\end{equation*}
$$

is satisfied. Each individual equation of (3-2) corresponds to one branch voltage. Writing characteristic equations of all network elements as

$$
\begin{equation*}
f\left(\frac{d q_{C}(v, t)}{d t}, \frac{d \phi_{L}(j, t)}{d t}, \mathbf{v}, \mathbf{j}, t\right)=0 \tag{3-3}
\end{equation*}
$$

This notation assumes that the terminal equations for capacitors and inductors are defined in terms of charges and fluxes, where $q(t)$ is the charge stored in the capacitors and $\phi(t)$ the flux stored in the inductors. The system (3-1)-(3-3) is a differential algebraic system, e.g. a coupled system of differential and algebraic equations in the network variables $j, v$ and $e$. The dimension of this system equals $2 b+n-1$. The approach leading to this system is called sparse tableau analysis. The modified nodal analysis (MNA) requires a much smaller number of unknowns. In this case, one replaces the branch currents of all current defining elements in (3-1) by their characteristic equations, and all branch voltages by node voltages using (3-2). The resulting systems represent differential-algebraic equations (DAEs). General differential-algebraic equations have been widely investigated [190-193]. The results cover, among other things, unique solvability, feasibility of numerical methods as well as stability properties. However, most of the results suppose a certain structure (e.g. Hessenberg form), high smoothness and depend mainly on the index of the differential-algebraic equation. Recently, the special structure and the index of the network equations have been investigated [194] and a more general study of different circuit configurations was presented [195]. It clarifies that the index may become arbitrarily high and may also depend on parameters. In [196], electrical networks result in a differential algebraic system with an index not higher than two. In essence, the network branches are a numbered in such a way that the incidence matrix forms a block matrix with blocks describing the different types of network elements. The blocks are then given as $\mathbf{A}=\left[\mathbf{A}_{R}, \mathbf{A}_{O} \mathbf{A}_{J}, \mathbf{A}_{V}, \mathbf{A}_{J}\right]$ where the index stands for resistive, capacitive, inductive, voltage source and current source branches, respectively. Replacing the branch currents of all current defining elements in (4-1) by their characteristic equations, and all branch voltages by node voltages using (4-2), the following system can be obtained

$$
\begin{align*}
& \mathbf{A}_{C} \frac{d q_{C}\left(\mathbf{A}_{C}^{T} \mathbf{e}, t\right)}{d t}+\mathbf{A}_{R} g\left(\mathbf{A}_{R}^{T} \mathbf{e}, t\right)+\mathbf{A}_{L} \mathbf{j}_{L}+\mathbf{A}_{V} \mathbf{j}_{V}=-\mathbf{A}_{I} \mathbf{i}_{s}(t) \\
& \frac{d \phi_{L}\left(\mathbf{j}_{L}, t\right)}{d t}-\mathbf{A}_{L}^{T} \mathbf{e}=0  \tag{3-4}\\
& \mathbf{A}_{V}^{T} \mathbf{e}=\mathbf{v}_{s}(\mathrm{t})
\end{align*}
$$

with the unknowns $\mathbf{e}(t), \mathbf{j}_{L}(t)$ and $\mathbf{j}_{V}(t)$. The network equations in (3-4) describe linear electric network including capacitors, inductors, resistors, independent voltage and current sources, representing the KCL for each node and the element characteristics of inductors and voltage sources. Denoting the number of nodes by $n$, the number of inductive branches by $n_{L}$ and the number of voltage source branches by $n_{V}$, the dimension of the system is now $n-1+n_{L}+n_{V}$. In the charge oriented MNA approach, additionally charges $q$ and fluxes $\phi$ as unknown variables are introduced. This implies the equivalent system
$\mathbf{A}_{C} \frac{d q}{d t}+\mathbf{A}_{R} g\left(\mathbf{A}_{R}^{T} \mathbf{e}, t\right)+\mathbf{A}_{L} \mathbf{j}_{L}+\mathbf{A}_{V} \mathbf{j}_{V}=-\mathbf{A}_{I} \mathbf{i}_{s}(t)$
$\frac{d \phi}{d t}-\mathbf{A}_{L}^{T} \mathbf{e}=0$
$\mathbf{A}_{V}^{T} \mathbf{e}=\mathbf{v}_{s}(\mathrm{t})$
$\mathrm{q}=q_{C}\left(\mathbf{A}_{c}^{T} \mathbf{e}, t\right)$
$\phi=\phi_{L}\left(j_{L}, t\right)$

In general, the charge oriented system (3-5) is, for several reasons, the main approach used in circuit simulators [195] as replacement circuit models for semiconductor elements. The simple form of the equations $q=q_{C}\left(\mathbf{A}_{C}{ }^{T} \mathbf{e}, t\right)$ and $\phi=\phi_{L}\left(j_{\nu}, t\right)$ involves only function evaluations for the determination of $q$ and $\phi$. Consequently, from the computational point of view, the dimension of the charge oriented system equals the dimension of the classical system. To expand the network equation in (4-4) to include the semiconductor devices, the currents of the semiconductor device have to be added to the KCL equation
$\mathbf{A}_{C} \frac{d q_{C}\left(\mathbf{A}_{\mathbf{c}}^{T} \mathbf{e}, t\right)}{d t}+\mathbf{A}_{R} g\left(\mathbf{A}_{R}^{T} \mathbf{e}, t\right)+\mathbf{A}_{L} \mathbf{j}_{L}+\mathbf{A}_{V} \mathbf{j}_{V}+\mathbf{A}_{S} \mathbf{j}_{s}+\mathbf{A}_{I} \mathbf{j}_{s}=0$
$\frac{d \phi_{L}\left(\mathbf{j}_{L}, t\right)}{d t}-\mathbf{A}_{L}^{T} \mathbf{e}=0$
$\mathbf{A}_{V}^{T} \mathbf{e}-\mathbf{v}_{s}=0$
$\mathbf{A}_{s}$ has the same form as the other incidence matrices $\left[\mathbf{A}_{O} \mathbf{A}_{R}, \mathbf{A}_{V}, \mathbf{A}_{V}, \mathbf{A}_{I}\right]$. The entries of the matrix $\mathbf{A}_{s}$ are defined as $a_{i k}=1$ if the current $j_{s k}$ enters node $i, a_{i k}=-1$ if the reference terminal is connected to node $i$, or $a_{i k}=0$ otherwise all for $i=1, \ldots, n-1$ and $k=1, \ldots, b_{s}-1 . n$ is the number of nodes of the network and $b_{s}$ is the number of terminals of the semiconductor. A procedure such as [196], allows decomposing the circuit's unknowns (node voltages, currents through branches) into a differential component $\mathbf{y}$ for time dependent solutions and an algebraic component $\mathbf{z}$ for quasi-static analysis. The nominal voltages and currents $\mathbf{z}_{0}$ are obtained by [197]
$\mathbf{z}_{0}=-\mathbf{B}^{-1}\left(\mathbf{C}_{Q} \mathbf{y}_{0}-\mathbf{F}_{Q}\left(\mathbf{i}_{(0)}, \mathbf{v}_{(0)}\right)\right)$
where $\mathbf{B}, \mathbf{C}_{Q}$ and $\mathbf{F}_{Q}$ are functions of the deterministic initial solution related to linear and non-linear couplings among the circuit's devices, $\mathbf{y}_{0}$ is an arbitrary initial state of the circuit and $\mathbf{i} \in \mathfrak{I}^{\boldsymbol{l}^{(t)}}$ and $\mathbf{v} \in \mathfrak{I}^{\boldsymbol{n}^{(V)}}$ are the independent current and voltage sources, respectively. It is assumed that for each process parameter $p$, e.g. threshold voltage, transconductance etc., there is only one solution of $\mathbf{z}_{0}$.

| $W / L=10 / 0.18$ |  |  |  | $W / L=10 / 0.18$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $p$ | $\mu$ | $\sigma$ | $p$ | $\mu$ | $\sigma$ |  |
| $V_{T 0, N}$ | 516.92 | 10.44 | $V_{T 0, P}$ | 481.148 | 10.103 | mV |
| $K_{0, N}$ | 422.53 | 10.34 | $K_{0, P}$ | 518.538 | 13.109 | $\mathrm{mV}^{1 / 2}$ |
| $K_{N}$ | 446.967 | 8.461 | $K_{P}$ | 451.971 | 17.434 | $\mathrm{mV}^{1 / 2}$ |
| $\beta_{N}$ | 26.334 | 1.290 | $\beta_{P}$ | 6.775 | 0.261 | $\mathrm{mA} / \mathrm{V}^{2}$ |
| $W_{e f f ; N}$ | 10.034 | 0.010 | $W_{\text {eff, } P}$ | 10.034 | 0.010 | Mm |
| $L_{e f f i, N}$ | 0.108 | 0.005 | $L_{\text {eff } f}$ | 0.143 | 0.005 | Mm |
| $I_{\text {DS, }, \text { lin }}{ }^{\text {a }}$ | 1.354 | 0.018 | $I_{\text {DS }, ~ / i i n ~}{ }^{\text {c }}$ | 0.402 | 0.018 | mA |
| $I_{\text {S }, \text {,sat }}{ }^{\text {b }}$ | 6.035 | 0.226 | $I_{D S, \text {,sat }}{ }^{\text {d }}$ | 2.914 | 0.226 | mA |

TABLE VII - MOST KEY PARAMETERS IN 0.18 CMOS TECHNOLOGY AT $\mathrm{V}_{\mathrm{BS}}=0 \mathrm{~V}$
a. $\mathrm{I}_{\mathrm{DS}, \text { lin }}$ at $\mathrm{V}_{\mathrm{GS}}=1.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=0.1 \mathrm{~V} \quad$ c. $\mathrm{I}_{\mathrm{DS}, \text { lin }}$ at $\mathrm{V}_{\mathrm{GS}}=-1.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=-0.1 \mathrm{~V}$
b. $\mathrm{I}_{\mathrm{DS}, \text { sat }}$ at $\mathrm{V}_{\mathrm{GS}}=1.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=1.8 \mathrm{~V} \quad$ d. $\mathrm{I}_{\mathrm{DS}, \text { sat }}$ at $\mathrm{V}_{\mathrm{GS}}=-1.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{DS}}=-1.8 \mathrm{~V}$

However, due to process variations, the manufactured values of process parameters will differ; hence, the manufactured values of the parameters $p_{i} \in\left\{p_{1}, \ldots, p_{m}\right\}$ for transistor $i$ are modeled as a random variable
$p_{i}=\mu_{p, i}+\sigma_{p}\left(d_{i}\right) \cdot p\left(d_{i}, \theta\right)$
where $\mu_{p, i}$ and $\sigma_{p}\left(d_{i}\right)$ are the mean value and standard deviation of the parameter $p_{i}$, respectively, $p\left(d_{j} \theta\right)$ is the stochastic process corresponding to parameter $p, d_{i}$ denotes the location of transistor $i$ on the die with respect to a point origin and $\theta$ is the die on which the transistor lies. This reference point can be located, say in the lower left corner of the die, or in the center, etc. As way of example, Table VII shows some typical transistor parameters $p$ with their mean and spread values.

### 3.1.2.2 Spatial Correlation Model

The availability of large data sets of process parameters obtained through parameter extraction allows the study and modeling of the variation and correlation between process parameters, which is of crucial importance to obtain realistic values of the modeled circuit unknowns. As an illustration Figure 3-2a) shows the parameter statistics of a batch with three different threshold-adjust implantations (identical for both $n$ - and $p$-channels). Typical procedures determine parameters sequentially and neglect the interactions between them and, as a result, the fit of the model to measured data may be less than optimum. In addition, the parameters are obtained as they relate to a specific device and, consequently, they correspond to different device sizes. The extraction procedures are also generally specialized to a particular model, and considerable work is required to change or improve these models. For complicated IC models, parameter extraction can be formulated as an optimization problem. The use of direct parameter extraction techniques [198] instead of optimization allows end-of-line compact model parameter determination. The model equations are split up into functionally independent parts, and all parameters are solved using straightforward algebra without iterative procedures or least squares fitting. With the constant downscaling of supply voltage the moderate inversion region becomes more and more important, and an accurate description of this region is thus essential.


Figure 3-2: a) p-channel threshold voltage, $V_{T O, P,}$ versus n-channel threshold voltage, $V_{T O, N ;}$ measured on two bundred transistor pairs from the same batch; b) Body-effect factor, $K_{0, N}$, versus threshold voltage, $V_{T o, N ;}$ for two bundred $n$ channel transistors from a batch with three different implantations to adjust the threshold voltage; b) Behavior of modeled covariance functions using $M=5$ for a/ $\rho=[1, \ldots, 10]$

The threshold-voltage-based models, such as BSIM and MOS 9, make use of approximate expressions of the drain-source channel current $I_{D S}$ in the weak inversion region (i.e., subthreshold) and in the strong-inversion region (i.e., well above threshold). These approximate equations are tied together using a mathematical smoothing function, resulting in neither a physical nor an accurate description of $I_{D S}$ in the moderate inversion region (i.e., around
threshold). The major advantages of surface potential [199] (defined as the electrostatic potential at the gate oxide/substrate interface with respect to the neutral bulk) over threshold voltage based models is that surface potential model does not rely on the regional approach and $I-V$ and $C-V$ characteristics in all operation regions are expressed/evaluated using a set of unified formulas. In the surface-potential-based model, the channel current $I_{D S}$ is split up in a drift ( $I_{\text {difif }}$ ) and a diffusion $\left(I_{\text {diff }}\right)$ component, which are a function of the gate bias $V_{G B}$ and the surface potential at the source $\left(v_{s 0}\right)$ and the drain $\left(v_{s I}\right)$ side. In this way $I_{D S}$ can be accurately described using one equation for all operating regions (i.e., weak, moderate and stronginversion). The numerical progress has also removed a major concern in surface potential modeling: the solution of surface potential either in a closed form (with limited accuracy) exists or as with our use of the second-order Newton iterative method to improve the computational efficiency in MOS model 11 [200].

A random process can be represented as a series expansion of some uncorrelated random variables involving a complete set of deterministic functions with corresponding random coefficients. This method provides a second-moment characterization in terms of random variables and deterministic functions. There are several such series that are widely in use. A commonly used series involves spectral expansion [201], in which the random coefficients are uncorrelated only if the random process is assumed stationary and the length of the random process is infinite or periodic [202]. The use of Karhunen-Loève expansion [189] has generated interest because of its bi-orthogonal property, that is, both the deterministic basis functions and the corresponding random coefficients are orthogonal [203], e.g. the orthogonal deterministic basis function and its magnitude are, respectively, the eigenfunction and eigenvalue of the covariance function. Simulation using Karhunen-Loève expansion can be made efficient if an analytical pre-processing step of the eigen-solution is available, whereby the computational effort is drastically reduced while safeguarding accuracy [202-203]. Assuming that $p_{i}$ is a zero-mean Gaussian process and using the Karhunen-Loève expansion, $p_{i}$ can be written in truncated form (for practical implementation) by a finite number of terms $M$ as
$p_{i}=\mu_{p, i}+\sigma_{p}\left(d_{i}\right) \cdot \sum_{n=1}^{M} \sqrt{\vartheta_{p, n}} \xi_{p, n}(\theta) f_{p, n}\left(d_{i}\right)$
where $\left\{\xi_{n}(\theta)\right\}$ is a vector of zero-mean uncorrelated Gaussian random variables and $f_{p, n}\left(d_{V}\right)$ and $\vartheta_{p, n}$ are the eigenfunctions and the eigenvalues of the covariance matrix $C_{p}\left(d_{p}, d_{2}\right)$ of $p\left(d_{v} \theta\right)$. Without loss of generality, consider for instance two transistors with given threshold voltages. In this approach, their threshold voltages are modeled as stochastic processes over the spatial domain of a die, thus making the parameters of any two transistors on the die, two differently correlated random variables. The variables can be generated by available established subroutines and then multiplied by the eigenfunctions and eigenvalues derived from eigen-decomposition of the target covariance model. The value of $M$ is governed by the accuracy of the eigen-pairs in representing the covariance function rather than the number of random variables. Unlike previous approaches, which model the covariance of process parameters due to the random effect as a piecewise linear model [204] or through modified Bessel functions of the second kind [205], here the covariance is represented as (Figure 3-2b) as a linearly decreasing exponential function

$$
\begin{equation*}
C_{p}\left(d_{1}, d_{2}\right)=\left(1+\zeta_{d_{x, y}}\right) \cdot \gamma \cdot\left(e^{-c_{x}\left|d_{x 1}-d_{x 2}\right| c_{y}\left|d_{y_{1}}-d_{y y}\right| / \rho}\right) \tag{3-10}
\end{equation*}
$$

where $\varsigma$ is a distance based weight term, $\gamma$ is the measurement correction factor for the two transistors located at Euclidian coordinates $\left(x_{1} y_{1}\right)$ and $\left(x_{22} y_{2}\right)$, respectively, $c_{x}$ and $c_{y}$ are process correction factors depending upon the process maturity. For instance, in Figure 3-2b) $c_{x, y}=$ 0.001 relates to a very mature process, while $c_{x, y}=1$ indicates that this is a process in a ramp up phase. In ( $3-10) \rho$ is the correlation parameter reflecting the spatial scale of clustering defined in $[-a, a]$, which regulates the decaying rate of the correlation function with respect to distance $\left(d_{l}, d_{2}\right)$. Physically, lower $a / \rho$ implies a highly correlated process and hence, a smaller number of random variables are needed to represent the random process and correspondingly, a smaller number of terms in the Karhunen-Loève expansion. This means that for $c_{x, y}=0.001$ and $a / \rho=1$ the number of, transistors that need to be sampled to assess, say a process parameter such as threshold voltage is much less than the number that would be required for $c_{x, y}=1$ and $a / \rho=10$ because of the high nonlinearity shown in the correlation function.


Figure 3-3: a) Top, systematic effect analysis for $68.3 \%(\sigma)$, $95.4 \%$ ( $2 \sigma$ ), $99 \%$, $99.3 \%$, $99.5 \%$ and $99.7 \%$ ( $3 \sigma$ ) yield expectations; Bottom, measured and modeled random effect; b) The spatial correlation dependence of Figure 3-2

To maintain a fixed difference between the theoretical value and the truncated form, $M$ has to be increased when $a$ increases at constant $b$. In other words, for a given $M$, the accuracy decreases as $a / b$ increases. Eigenvalues $\vartheta_{p, n}$ and eigenfunctions $f_{p, n}(\tau)$ are the solution of the homogeneous Fredholm integral equation of the second kind indexed on a bounded domain $D$. To find the numerical solution of Fredholm integral, each eigenfunction is approximated by a linear combination of a linearly decreasing exponential function. Resulting approximation error is than minimized by the Galerkin method.

One example of spatial correlation dependence and model fitting on the available measurement data of Figure 3-2a) through Karhunen-Loève expansion is given in Figure 3-3. The sampling window radius versus on-chip variability as a result of the spatial filtering analysis is shown in Figure 3-3a), where a single variability function, which is tuned for a specific yield expectation, is derived through combination of the distributions of each wafer. The sampling window radius corresponds to the worst-case distance between the reference point and any other cell within the window area. To analyze random process variation, dominant systematic effects from the measurement data are removed by variability decomposition method [206]. For comparison purposes, a grid-based spatial-correlation model (Figure 3-3b) is intuitively simple and easy to use, yet, its limitations due to the inherent accuracy-versus-efficiency necessitate a more flexible approach, especially at short to mid range distances [205].

### 3.1.2.3 Fault Model Definition

From a statistical modeling perspective, global variations affect all transistors in a given circuit equally. Thus, systematic parametric variations can be represented by a deviation in the parameter mean of every transistor in the circuit, which can be seen as a defect. A defect model is now introduced, $\eta_{p}=f($.$) , accounting for voltage and current shifts due to random$ manufacturing variations in transistor dimensions and process parameters defined as,
$\eta_{p}=f\left(\nu, W^{*}, L^{*}, p^{*}\right)$
where $\eta_{p}=f($.$) is the function of changes in node voltages and branch currents, v$ defines a fitting parameter estimated from the extracted data, $W^{*}$ and $L^{*}$ represent the geometrical deformation due to manufacturing variations, and $p^{*}$ models electrical parameter deviations from their corresponding nominal values, as defined in (3-9), e.g. altered transconductance, threshold voltage, etc. This defect model is used to generate a corresponding circuit fault model by including the term $\eta_{p}$ of (3-11) into (3-7), written in matrix form as

$$
\begin{equation*}
\boldsymbol{\Xi}=\mathbf{z}_{0} \times \boldsymbol{\eta}_{p} \tag{3-12}
\end{equation*}
$$

where $\mathbf{z}_{0}$ is a matrix of the nominal data and $\boldsymbol{\eta}_{\phi}$ a random vector accounting for device tolerances. Basically, the fault model of (3-12) shifts the $d c$ nodal voltages ( $d c$ branch currents) out of their ideal state based on the random and systematic variations of the process technology. While the functional behavior of a circuit in the frequency domain may not be linear, or even in the $d c$ domain as a result of a nonlinear function between output and input signals, as long as the biasing and input conditions of the circuit under test remain quasi-static, the faulty nodal voltage (branch current) of (3-12) follows a Gaussian distribution as posed in (3-9). An obvious limitation of the fault model of (3-12) is that it cannot capture a faulty transient behavior of the circuit under test.

In general, a circuit design is optimized for parametric yield so that the majority of manufactured circuits meet the performance specifications. The computational cost and complexity of yield estimation, coupled with the iterative nature of the design process, make yield maximization computationally prohibitive. As a result, circuit designs are verified using models corresponding to a set of worst-case conditions of the process parameters. Worst-case analysis refers to the process of determining the values of the process parameters in these worstcase conditions and the corresponding worst-case circuit performance values. Worst-case analysis is very efficient in terms of designer effort, and thus has become the most widely practiced technique for statistical analysis and verification. Algorithms previously proposed for worst-case tolerance analysis fall into four major categories: corner technique, interval analysis, sensitivity-based vertex analysis and Monte Carlo simulation. The most common approach is the corners technique. In this approach, each process parameter value that leads to the worst performance is chosen independently. This method ignores the correlations among the processes parameters, and the simultaneous setting of each process parameter to its extreme value result in simulation at the tails of the joint probability density of the process parameters. Thus, the worst-case performance values obtained are extremely pessimistic. Interval analysis is computationally efficient but leads to overestimated results, i.e., the calculated response space enclose the actual response space, due to the intractable interval expansion caused by dependency among interval operands. Interval splitting techniques have been
adopted to reduce the interval expansion, but at the expense of computational complexity. Traditional vertex analysis assumes that the worst case parameter sets are located at the vertices of parameter space, thus the response space can be calculated by taking the union of circuit simulation results at all possible vertices of parameter space. Given a circuit with $M$ uncertain parameters, this will result in a $2^{M}$ simulation problem. To further reduce the simulation complexity, sensitivity information computed at the nominal parameter condition is used to find the vertices that correspond to the worst cases of circuit response. The Monte Carlo algorithm takes random combinations of values chosen from within the range of each process parameter and repeatedly performs circuit simulations. The result is an ensemble of responses from which the statistical characteristics are estimated.


Figure 3-4: Monte Carlo versus equation (3-14) for the folded node voltage and supply current $I_{D D}$ as function of the input voltage

Unfortunately, if the number of iterations for the simulation is not very large, the Monte Carlo simulation always underestimates the tolerance window. Accurately determining the bounds on the response requires a large number of simulations, so Monte Carlo method becomes very CPU-time consuming if the chip becomes large. From the test point of view, generally, the fault-free circuit and faulty circuit have different tolerance windows meaning that for the fault-free circuit and each faulty circuit, the corresponding tolerance window should be generated. The total number of tolerance-windows is therefore $(n+1)$ if the number of faults in the fault list is $n$.


Figure 3-5: Monte Carlo versus equation (3-14) for the folded node voltage and supply current $I_{D D}$ as function of the supply voltage

In our case, based on the central limit theorem, to completely characterize Gaussian data in (3-12) probabilistically, firstly the means and correlations have to be found by calculating the first and second-order moments through expectation. Even if the random variable is not strictly Gaussian, a second-order probabilistic characterization yields sufficient information for most practical problems. To make the problem manageable, the system in (3-12) is linearized by a truncated Taylor approximation assuming that the magnitude of the random defect $\eta_{p}$ is sufficiently small to consider the equation as linear in the range of variability of $\eta_{p}$, or that the non-linearity of the electrical fault $\Xi$ in the case of quasi-static $d c$ biasing are so smooth that they might be considered as linear even for a wide range of $\eta_{p}$.


Figure 3-6: Maximum and minimum difference in percentage [\%] between Monte Carlo and (3-14) for the node voltage and supply current $I_{D D}$ as function of the input voltage. $\Xi_{, m a x}, \Xi_{, \text {minn }}, I_{D D \max }$ and $I_{D D \min }$ denote the tails of the probability function.

Next, the autocorrelation function of each nodal voltage (branch current) for each of the process parameters has to be calculated. This is necessary to estimate a tolerance window required to make a decision whether the circuit is faulty or not. The autocorrelation of $\boldsymbol{\Xi}$ for a quasi-static time period is then calculated as
$\mathbf{C}_{\bar{\Xi} \Xi}=\mathbf{J}_{0} \mathbf{C}_{\eta \eta} \mathbf{J}_{0}^{T}$
where $\mathbf{J}_{0}$ is the Jacobian of the initial data $\mathbf{z}_{0}$ evaluated at $p_{i}$ and $\mathbf{C}_{m j}$ is the symmetrical covariance matrix whose diagonal and off-diagonal elements contain the parameter variances and covariances as defined in (3-10), respectively. Following (3-13), the boundaries of quasi-static node voltage $\Xi_{r}$ with mean value $\mu_{\Xi_{r}}$ are expressed with

$$
\begin{equation*}
\left[\boldsymbol{\Xi}_{r, \text { min }}, \boldsymbol{\Xi}_{r, \text { max }}\right]=\boldsymbol{\mu}_{\Xi_{r}} \pm \sum_{k} \sum_{m}\left\{\left|\mathbf{C}_{\Xi_{r}, \Xi_{r}}\right|^{\max }\right\} \tag{3-14}
\end{equation*}
$$

for any $p_{i} \in\left\{p_{p}, \ldots, p_{m}\right\}$ of $i \in\left\{i_{p}, \ldots, i_{k}\right\}$ transistors connected to node $r \in\left\{r_{1}, \ldots, r_{q}\right\}$. Per definition, setting the quasi-static node voltage $\Xi_{\text {, }}$ outside the allowed boundaries in (3-14) designates the faulty behavior. To obtain a closed form of moment equations, Gaussian closure approximations are introduced to truncate the infinite hierarchy. In this scheme higher order moments are expressed in terms of the first and second order moments as if the components of $\boldsymbol{\Xi}$ are Gaussian processes. The method is fast, and comparable to regular nominal circuit simulation. Suppose that there are $m$-trial Monte Carlo simulation for $n$ faults, the proposed
method (using statistical data of the process parameters variations) gains a theoretical speedup of $m \times n$ over the Monte Carlo method. The precision of the method is illustrated on the quiescent current and node voltage of folded-cascode amplifier with gain boosting auxiliary amplifier shown in Figure 2-15. Equation (3-14) versus Monte Carlo analysis (it can be shown that 1500 iterations are necessary to accurately represent performance function) as a function of the input and supply voltage is illustrated in Figure 3-4 and Figure 3-5. The difference between the two methods is shown in Figure 3-6 and Figure 3-7.


Figure 3-7: Maximum and minimum difference in percentage [\%] between Monte Carlo and this approach for the node voltage and supply current $I_{D D}$ as function of the supply voltage. $\Xi_{, \text {max }}, \Xi_{, \text {min }}, I_{D D \max }$ and $I_{D D \min }$ denote the tails of the probability function.

### 3.1.3. Decision Criteria and Test-Stimuli Optimization

### 3.1.3.1 Neyman-Pearson Decision Criteria

As each branch current is a Gaussian random variable in linear combination of parameter variations, the power supply current due to the voltage deviation at the node $r$, denoted as $I_{D D n}{ }^{\prime \prime}(n$ samples) is, therefore, also a Gaussian distributed random variable, and its derivatives to all process parameters $\partial I_{D D n}{ }^{r} / \partial p_{i}$ can easily be found from its linear expression of parameters. To avoid notation cluttering, $I_{D D n}$ denotation is further used. Derivation of an acceptable tolerance window for $I_{D D n}$ is aggravated due to the overlapped regions in the measured values of the error-free and faulty circuits, resulting in ambiguity regions for fault detection. To counter this uncertainty, the Neyman-Pearson test [207], which is based on the critical region $C^{*} \subseteq \Omega$, where $\Omega$ is the sample space of the test statistics, offer the largest power of all tests with significance level $\alpha$ (the probability that the fault-free circuit is rejected when it is faultfree)
$C^{*}=\left\{\left(I_{D D_{1}}, \ldots, I_{D D_{n}}\right): l\left(I_{D D_{1}}, \ldots, I_{D D_{n}} \mid G, F\right) \leq \lambda\right\}$
where $I_{D D}$ is an observation sample, $l()$ is a likelihood function, and $G$ and $F$ denote the errorfree and faulty responses, respectively. Since both $\alpha$ and $\beta$ (the probability that faulty circuit is accepted when it is faulty) represent probabilities of events from the same decision problem, they are not independent of each other or of the sample size. Of course, it would be desirable to have a decision process such that both $\alpha$ and $\beta$ are small. However, in general, a
decrease in one type of error leads to an increase in the other type for a fixed sample size. The only way to simultaneously reduce both types of errors is to increase the sample size, which proves to be time-consuming process. The Neyman-Pearson test is a special case of the Bayes test, which provides a workable solution when the a priori probabilities may be unknown or the Bayes average costs of making a decision may be difficult to evaluate or set objectively. As the density functions of the $I_{D D n}$ under fault-free and faulty condition $f\left(I_{D D n} \mid G\right)$ and $f\left(I_{D D_{n}} \mid F\right)$, respectively, are often termed likelihood functions, the likelihood ratio is defined as
$l\left(\left(I_{D D \mid}, \ldots, I_{D D_{n}}\right)\right)=\frac{f_{I D_{n}}\left(\left(I_{D D,}, \ldots, I_{D D_{n}}\right) \mid G\right)}{\left.f_{I D D_{n}}\left(I_{D D 1}, \ldots, I_{D D_{n}}\right) \mid F\right)}$

For the threshold $\lambda$ to be of significance level $\alpha$

$$
\begin{gather*}
P=\left\{\left(I_{D D}, \ldots, I_{D D_{n}}\right) \in C^{*} \mid P(G)\right\}=\alpha \\
P\left(\bar{I}_{D D} \geq \lambda \mid I_{D D} \sim N\left(\mu, \sigma^{2} / n\right)\right)=P\left(Z \geq \frac{\lambda-\mu_{G}}{\sigma_{G} / \sqrt{n}}\right)=\alpha \tag{3-17}
\end{gather*}
$$

where $\mu_{G}$ and $\sigma_{G}$ are mean and variance of the error-free response. $P\left(Z<z_{\left.\Omega_{1}-\alpha\right)}\right)=1-\alpha$, and $z_{\left.\tau_{1}-\alpha\right)}$ is the (1- $\alpha)$-quantile of $Z$, the standard normal distribution. Recall that if $I_{D D} \sim N\left(\mu, \sigma^{2}\right)$, then $Z=\left(I_{D D}-\mu / \sigma\right) \sim N(0,1)$. In the present case, the sample mean of $I_{D D} \sim N\left(\mu, \sigma^{2} / n\right)$, since the variable $I_{D D}$ is assumed to have a normal distribution. From previous equation follows that the test $T$ rejects for
$T=\frac{\bar{I}_{D D}-\mu_{G}}{\sigma_{G} / \sqrt{n}} \geq z_{(1-\alpha)}$

To incorporate the Neyman-Pearson lemma, the first step is to choose and fix the significance level of the test $\alpha$ and establish the critical region of the test corresponding to $\alpha$. This region depends both on the distribution of the test statistic $T$ and on whether the alternative hypothesis is one- or two- sided. After data collection/observation from the measurements, the following step is to calculate the value of $T$ (called $t^{*}$ ) from the data sample. This result is compared with the distribution of $T$ in order to see whether or not it falls in the critical (rejection) region. At the end, decision is made to accept or reject the data sample.

| Algorithm |
| :--- |
| Initialization |
| - Define probabilities $\mathrm{P}(\mathrm{G})$ and $\mathrm{P}(\mathrm{F})$ of each observation sample |
| - Assign significance level $\alpha$ |
| Data collection |
| - Collect $I_{D D n}$ sampling points instants for each calculation |
| Main body |
| 1. Calculate the critical region $C^{*}$ according to (4-15) |
| 2. Define decision threshold $\lambda^{*}=\mu_{G}+z_{(I-\alpha)} \sigma / \sqrt{n}$ |
| 3. Calculate the $(1-\alpha)$-quantile of the standard normal distribution $z_{(I-\alpha)}$ |
| 4. Calculate the value of $T$ from the data sample according to $(4-18)$ |
| 5. If $T \geq z_{(I-\alpha)}$ reject otherwise accept the observation sample |

### 3.1.3.2 Test Stimuli Optimization

All simulation results are stored within a block in the database. This makes it possible to fillin the database in an incremental way by first investigating results of a certain simulation, and later on adding the results of a different simulation, possibly containing a different set of faults and/or tests. The database-block is viewed as a matrix where a column contains the entire test results for a single fault and a row contains the results for a single test. In this way, every matrix entry is the test result for a test-fault combination.

To derive necessary stimuli's for the test pattern generation, the test stimuli optimization on the results available in the database is necessary. Several possible ways exist to optimize test stimuli: A brute force method would be to first gather fault coverage data for each of the circuit specifications. This data can then be used to find the best order of the test stimuli's, by trying all possible permutations of the test stimuli set. If the circuit has $n$ specifications, $n$ ! permutations would have to be tried, for example for 20 specifications $2.4 \times 10^{18}$ permutations are needed, which is clearly not computationally feasible. The approach in [208] is more advanced. Here Dijkstra's Algorithm is applied to select and order analog specification tests. The computational complexity of the algorithm is $n \times 2^{n}$, so for $n=20,1 \times 10^{6}$ probabilities need to be computed. This is a great improvement over the brute force method, but it is still too large. The disadvantage of Dijkstra's algorithm is that it does not take into account fault coverage, which appears to be critical for test ordering. In general it is best to perform the test stimuli's with high fault coverage's first, provided that they are not too expensive.

The algorithm in [181] and partially implemented here are based on these observations. First test stimuli's that have very low fault coverage's are eliminated from the test stimuli set, and then the remaining test stimuli's are ordered. Two approaches to test stimuli ordering are considered: in the first stage, the test stimuli are ordered so that the test stimuli detecting the most faulty parameters that are detected by no other test stimuli is performed first, and the least important test stimuli is performed last (the test stimuli are ordered in descending order of unique coverage values). In the second stage the more costly test stimuli are moved downwards and are therefore used on a smaller number of circuits thus reducing the total test stimuli cost. Going from top to bottom, test stimuli, which do not increase the cumulative coverage, are moved to the bottom of the list.

Because some test stimuli are eliminated from the test stimuli set before the test stimuli's are ordered, both algorithms are heuristic, and both can handle circuits with many more specifications at much less computation cost. The computational complexity of the algorithm is $n^{2}$, so for $n=20,400$ probabilities need to be computed. Because of the heuristic approach, the algorithm does not necessarily produce the real optimum value, but usually a value close to the optimum value. In order to find optimum test stimuli set, the algorithm tries various permutations of the test stimuli set. The more costly test stimuli are considered first, and the less costly test stimuli are considered last. Suppose a costly test stimulus is in the $i^{\text {th }}$ position. The algorithm considers moving it to each position $j$ with $j>i$. When the $i^{\text {th }}$ test stimulus is moved to the $j_{\text {th }}$ position, the test stimuli currently in the $i+1$ st to $j^{\text {th }}$ positions are moved forward one step. When a permutation is made, all of the test stimuli's yields, $Y_{j}$, change. The yield $Y_{i}$ of test $T_{i}$ is defined to be the fraction of devices passing test $T_{i}$, given all previous test stimuli's in the sequence. This means that the yield of test stimuli depends on its place in a test sequence. The optimal test sequence is the test sequence for which the test stimuli cost is
a minimum. The average test stimuli cost is
$T_{c}=w_{1}+w_{2} \frac{\left(D_{T}-N_{1}\right)}{D_{T}}+w_{3} \frac{\left(D_{T}-N_{1}\right)}{D_{T}} \frac{\left(D_{T}-N_{1}-N_{2}\right)}{\left(D_{T}-N_{1}\right)}+\ldots=\sum_{i=1}^{n} w_{i} \prod_{j=1}^{i-1} Y_{j}$
where $w_{i}$ is cost of applying test stimuli performing test number $i, N_{i}$ is defined to be the number of faults detected uniquely by test stimuli $T_{i}$ and not by any of the previous test stimuli's and $D_{T}$ is the total number of devices.

```
Optimization Algorithm
Initialization
    - Initialize the input test stimuli set T, w
    - Initialize the number of test stimuli's m
    Main body
    - Compute the average test stimuli cost T
    - Compute the test stimuli cumulative coverage C}\mp@subsup{C}{c}{
- Find min argument of wi,i\inT
j=i+l
while j\leqm
    { Compute (3-22) and (3-23)
        if (3-23) < (3-22)
            { Compute \mp@subsup{T}{c}{}\mp@subsup{}{}{`}}\mathrm{ (the new average test stimuli cost) using (3-19)
                If }\mp@subsup{T}{c}{}\mp@subsup{}{}{`}<\mp@subsup{T}{c}{
                    move the ith}\mathrm{ test stimuli to the jith}\mathrm{ position
                    move the i+\mp@subsup{l}{}{\mathrm{ st }}\mathrm{ to j}\mp@subsup{j}{}{\mathrm{ th }}\mathrm{ test stimuli's up one position and update }\mp@subsup{T}{c}{}
            }
        Compute C}\mp@subsup{C}{c}{}\mp@subsup{}{}{`}\mathrm{ (the new average test stimuli cost) using (3-24)
        If C}\mp@subsup{C}{c}{`}<\mp@subsup{C}{c}{}\mathrm{ ,
            { move the ith test stimuli to the jth}\mathrm{ position
                move the i+ l 't to j}\mp@subsup{}{}{\mathrm{ th }}\mathrm{ test stimuli's up one position and update }\mp@subsup{C}{c}{
            }
        j=j+1
    }
- Stop when the optimum test stimuli set T is found
```

The algorithm avoids the calculation of all the new test stimuli's yields, $Y$, for each possible permutation, and instead it first estimates if the change is likely to improve average test stimuli cost. If the $i^{\text {th }}$ test is moved to the $j^{t / h}$ position then only the test yields of the $i^{\text {th }}$ to $j^{\text {th }}$ tests can change. In particular, the only change in previous equation is

$$
\begin{equation*}
\sum_{k=1}^{j} w_{k} \prod_{l=i}^{k-1} Y_{l} \tag{3-20}
\end{equation*}
$$

Defining $x$ as

$$
\begin{equation*}
x=\sum_{k=1+1}^{j} w_{k} \prod_{l=i+1}^{k-1} Y_{l} \tag{3-21}
\end{equation*}
$$

Then before a permutation, (3-20) is equal to

$$
\begin{equation*}
w_{i}+Y_{i} x \tag{3-22}
\end{equation*}
$$

If $Y_{i}$ does not change significantly, after a permutation, (3-20) can be approximated by

$$
\begin{equation*}
x+w_{i} \prod_{l=i+1}^{j} Y_{l} \tag{3-23}
\end{equation*}
$$

So if (3-23) is smaller than (3-22), the permutation is likely to reduce test stimuli cost, and the true $Y_{i}$ are computed. If test stimuli cost decreases, the move is accepted. The algorithm continues by trying more permutations until the shortest tests have been tried. The cumulative coverage of test stimuli is the number of faults detected by the test stimuli or a previous test stimuli divided by the total number of faults.
$C_{c}=\frac{1}{N} \sum_{i-1}^{n} c_{h}(i)$
where $c_{b}(i)$ is the highest achieved normalized fault coverage and $N$ is the total number of faults.

Following the steps described in this Section, the total time required for fault injection $t_{\text {injection }}$ fault simulation $t_{\text {simplation }}$ discrimination analysis $t_{\text {discrimination }}$ and test stimuli optimization $t_{\text {optimization }}$ can be expressed as

```
\(t_{\text {injection }}=N_{\text {nodes }} \cdot t_{\text {swap }}\)
\(t_{\text {simulation }}=N_{\text {bias }} \cdot N_{\text {supply }} \cdot N_{\text {input }} \cdot N_{\text {reference }} \cdot t_{\text {circuit }}+t_{\text {tolerance }}\)
\(t_{\text {discrimination }}=N_{\text {faults }} \cdot t_{\text {analysis }}\)
\(t_{\text {optimization }}=N_{\text {permutation }} \cdot N_{\text {faults }}\)
```

 the circuit netlist, derive the boundaries of circuit response and perform the NeymanPearson test, respectively. $N_{\text {nodes }}$ denote the number of the nodes in the circuit, $N_{\text {biass }}, N_{\text {suppb }}$, $N_{\text {ipput }}$ and $N_{\text {refernere }}$ designate the number of bias, supply, input and reference nodes where a quasi-static stimulus is applied, respectively, $N_{\text {faults }}$ indicate the number of the faults and $N_{\text {permurn }}$ tation designate the number of permutations of the test stimuli set.

### 3.2. Design for Testability Concept

Modern Systems-on-Chip (SoC) integrate digital, analog and mixed-mode modules, e.g. mixed-signal, or RF analog and digital, etc., on the same chip. This level of integration is further complicated by the use of third-party cores obtained from virtual library descriptions of the final IC block. Furthermore, the variety and number of cores and their nature type, e.g. analog, complicate the testing phase of individual blocks, of combinations of blocks and ultimately of the whole system. The problem in the analog domain is that it is much more difficult to scan signals over long distances in a chip and across its boundary to the outside world, since rapid signal degradation is very likely to occur. The IEEE 1149.4 [209] is a standard mixed-signal test bus that can be used at the device, sub-assembly, and system levels. It aims at improving the controllability and observability of mixed-signal designs and at supporting mixed-signal built-in test structures in order to reduce test development time and costs, and to improve test quality.

There are various known approaches for designing for testability of analog circuits. The most common approach is to partition a system into sub-blocks to have access to internal nodes such that each isolated sub-block receives the proper stimuli for testing [210]. DfT in [211] is oriented at testing sub-blocks of a filter such that each stage is tested by increasing the bandwidth of the other stages. This is done by adjusting the switching scheme in the case of switched-capacitor filters, or by bypassing the filter capacitors using additional MOS transistor switches. The problem with the latter approach is that MOS transistors are in the direct signal path of the filter degrading the performance. A switched op amp structure can overcome this limitation [212]. In essence, this switched op amp has basically two operational modes, test and normal, depending upon a digital control signal. The op amp is used at the interface between any two sub-blocks. An enhanced approach similar to [212] that makes use of an op amp with duplicated input stages is given in [213-214]. In this approach every op amp in the initial filter design is replaced by the DfT op amp. In [215] a DfT scheme suitable to detect parametric faults in switched-capacitor circuits based on a circuit that can compute all the capacitor ratios that determine the transfer function of the filter is shown. Other DfT schemes include A/D converters with self-correction capability [216].

Unlike previous approaches that test the analog circuit for functionality, analog structural testing [217-218] consists of exciting the circuit under test with a $d c$ or low-frequency stimulus to sample the response at specified times to detect the presence of a fault. The $d c$ transient waveform can be formed from piecewise-linear segments that excite the circuit's power supply, biasing, and/or inputs. To facilitate this kind of testing, it is preferable to observe the current (or voltage) signatures of individual cores instead of observing the current (or voltage) signature of the whole analog SoC. Therefore, proposed DfT method works like a power-scan chain aimed at turning on/off analog cores in an individual manner, at providing observability means at the core's power and output terminals, and at exciting the core under test [219]. Existent DfT techniques do not turn individual blocks on and off, but merely disconnect the observed block from the signal path; neither are they suitable for $d_{c}$ transient testing such as $V_{D D}$ ramping [220].

The supply-current monitoring technique has, so far, found no practical widespread application in analog circuits. This is mainly because analog faulty behaviours are not so pronounced as those in the digital case; special test vectors often have to be applied to increase fault coverage, in a special test mode. To apply the power-supply-current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques. This is because of two factors: $i$ ) the method requires more than a simple observation of abnormal currents; ii) unlike digital circuits, bias currents always exist between the power supplies in analog circuits and in most cases abnormal currents cannot be defined.

For analog circuits and systems, fault diagnosis techniques are more complex when compared to their counterparts in digital circuits for various reasons: i) the requirement of measurements of current and voltage signals at the internal nodes; ii) diagnosis errors caused by softfaults, which are due to the tolerance of the components.

An advanced methodology for testing analog circuits that overcomes the majority of the obstacles encountered with the supply-current-monitoring technique was proposed in [220]. To obtain signatures rich in information for efficient testing, the transistors in the circuit are forced to operate in all possible regions of operation by applying a ramp signal to the supply terminals instead of the conventional constant $d c$ signal or ground voltage. The power-
supply-ramping technique can potentially detect and diagnose catastrophic [217] as well as parametric faults [218]. The application of a ramp signal to the power supply voltage nodes instead of the conventional step (or $d c$ voltage) can force the majority of the transistors in the circuit to operate in all the regions of operation, and hence, provide bias currents rich in information. The method measures current signatures, not single values. Many faults have unique or near-unique signatures, easing the diagnosis process. Indeed it is independent of the linearity or nonlinearity of the systems, circuit or component.

### 3.2.1. Power-Scan Chain DfT

Conventional DfT methods can provide test access points to each input and output node in the signal path. The CMOS switch matrix is capable of three modes. First, it can pass the signal from one block to the next for normal operation. Second, it can disconnect the output from one block and connect the input of the following block to the analog test input bus. The tester can then inject a test signal into the input of the circuit under test. Finally, the switch matrix allows observation of the output of the circuit under test through the analog test output bus. However, when using CMOS switches in the signal path of sensitive analog circuits, some possible problems may occur such as crosstalk, capacitive loading, and increased noise and distortion.


Figure 3-8: Power-Scan Chain Analog DfT
An objective of the proposed power scan-chain DfT [219] illustrated in Figure 3-8 is to avoid (minimize) the number of switches in the signal path as well as to provide means to support current-based testing techniques. The main feature of the DfT is to selectively turn individual cores on and off such that the core(s) $d c, a c$, and/or transient characteristics can be tested in isolation or together with other cores of an analog SoC. Conceptual overview of power-scan chain implemented in the two-step A/D converter is shown in Figure 3-9. There are several ways of turning on/off analog cores. Preferred choice is by placing switches in the biasing network of the analog core, as this does not interfere with signals in the signal path. Another option is to place switches in the power path. However, these switches introduce a voltage drop that can have an impact on the core's performance. Additionally, the latter switches may be bulky. The DfT network shown in Figure 3-8 has been designed to operate in all possible regions of operation by using a ramp signal at the supply instead of the conventional constant
$d c$ signal or ground voltage. The DfT consists of an Analog Test Input Bus to provide input stimuli to the core under test, an Analog Test Output Bus to read out stimuli response, a Digital CS and OS Interface to read out digitized current signatures (CS) and digitized output response stimuli (OS), an Analog Supply Network to read out currents in the power line and two Shift-register controllers to turn on/off individual cores and to select/deselect input/out test busses, respectively.


Figure 3-9: Conceptual overview of power-scan chain DfT implemented in the two-step ADC.

### 3.2.1.1 Analog Supply Network and Biasing Control

Only one sensor is inserted in the $V_{D D}$ path of analog supply network, which is essentially an amp meter to measure the current flowing through the power supply terminal. An important property of any current sensor is to provide accurate measurements of extremely small current readings in the environment where the current changes are very fast and usually masked with high transients.


Figure 3-10: Part of the switching matrix used to turn on and off the core's biasing circuits

Conversely, under the condition that the ratio of the supply current to the background current is not sufficient to differentiate between a fault-free and a faulty circuit, the main limitation would be off-chip sensing. However, with development of built-in current monitor onchip, these constraints have been largely overcome [221-222]. To facilitate supply current readings of the individual cores ( $I_{D D B, g} I_{D D 1}, I_{D D 2}, \ldots, I_{D D \|}$ ), the biasing network of the cores
under consideration are turned on/off in an individual manner. The supply currents of the individual cores are found from the difference between the supply currents found for the different codes, clocked in from left to right out of the bias shift register. The supply current readings are performed at the core's nominal operating conditions. The needed test time depends on the complexity of the analog blocks. ATPG results provide the optimum choice of the applied ramp and of the sequence of switching on/off individual analog core leading to the minimum test time under the restriction of a certain minimum allowed fault coverage.


Figure 3-11: Part of the switching matrix control circuitry
To increase readability and avoid the rounding effects of the low-level power supply current, the quiescent power supply current is sensed across a sensing element and further amplified in a voltage amplifier with automatic-gain-control features to deal with wide dynamic ranges. After amplification and digitalization, all individual supply current readings are stored in a memory unit. The $\varphi$ operator allows any type of mathematical operation, such as addition, multiplication, convolutions, etc., for any combination of individual current signatures. Postprocessing of the current signature is done by any post-processing means, such as for in-
stance integration or FFT. Besides observing the analog waveform of the power supply current signature this approach allows observing its digitized version as well. Figure 3-8 shows a flash $N$-bit digitizer, with $N \geq 1$, whose $V_{T H}$ references originate from the Analog Test Input bus, although, any $N$-bit digitizer architecture can be implemented. The Digital-Decoder clock signal is related to the system. The biasing network consists of a bandgap circuit providing an $I_{r f}$ current, and of a current mirror with multiple legs, each feeding an analog core. The (bias) shift register controller is a digital circuit with $V_{D D}($ logical 1$)$ and $V_{S S}(l o g i c a l ~ 0)$ voltage levels. For the $n$-channel-based biasing network of this example, a bit value 1 in any position of the shift register turns on any of the switches $D_{1}, D_{21} \ldots D_{2 \mathrm{~N}} \ldots D_{\mathrm{NN}}$. Note that when node $D_{1}$ is switched on or when the bandgap is powered down by the global powerdown signal $\left(G P_{t}\right)$, $I_{r f}$ will no longer flow and all bias currents will become zero irrespective of the $D_{21} \ldots D_{2 N} \ldots D_{N N}$ signals. When node $D_{1}$ is switched on all bias currents will become zero irrespective of the $D_{27} \ldots D_{2 N} \ldots D_{N N}$ signals, however, $I_{r f}$ will still flow. Switches $D_{21} \ldots D_{2 N} \ldots D_{N N}$ are used to turn off the core-under-test or to adjust the corresponding current biasing. One can regard switch $D_{k 1}$, where $k=2 \ldots N$, as the master switch that enables the nominal biasing current to the core under normal operation. The remaining switches are used in test mode to allow the biasing current to be modified for testing purposes. In Figure $3-8$, it is assumed that switches in the biasing network are composed of $n$-channel transistors. However, actual implementation comprises both $n$-channel and $p$-channel transistors as shown in Figure 3-10. Part of the switching matrix control circuitry is shown in Figure 3-11.

The IC may consume a certain amount of current even if all blocks are off due to the leakage current of the digital circuitry used in mixed-signal circuits. It is important to note that by placing the switches at the ground nodes of the core's biasing circuit and not at the ground nodes of the analog core itself, an impact on the core's bias point due to voltage drop caused by switch on-resistance is limited. To ensure that individual core is totally off, e.g. that it does not have floating nodes, a local power-down signal, $P_{d}$, is made available. The local powerdown signal is active, when switches $D_{21} \ldots D_{2 N}$ connected to the biasing network of the core $1, D_{31} \ldots D_{3 \mathrm{~N}}$ for core $2, D_{\mathrm{N} 1} \ldots D_{\mathrm{NN}}$ for core N , are disconnected. The implementation for these settings is a logical nor port. Switches $D_{T 1} \ldots D_{T N}$ are used to test the biasing network itself. They connect the bias nodes to the Analog Output Test bus. The core's biasing network is tested by turning on one core at a time and reading out the corresponding biasing voltage levels. Sensing of the bias network can be easily adjusted to detect the biasing current as well. As a final test provision is made to test the bandgap power-supply current.

### 3.2.1.2 Analog Test Input and Output Bus

The scheme provides an Analog Test Input Bus to control (excite) the cores that are enabled. When using CMOS switches in the signal path of sensitive analog circuits, some possible problems may occur, such as cross-talk and increased noise, distortion and capacitive loading. In this approach two switches are implemented instead of, conventionally used, four. Observe that there are no switches in the signal path from core to core, and that the Analog test bus is shunted with the signal path. This is possible when assuming that the core prior to the core under test is turned off through the I/O register-controlled switch and the local power-down signal. The Analog Test Output Bus provides observability of the core-undertest; associated with this bus is the Digital Output Interface, which digitizes the analog signal. The Analog Test Input bus can offer the input signal to the system, and the system output signal can be digitized and offered to the Digital Output Interface as well, to allow voltage read outs in Power-Scan chain mode in the whole system.

### 3.2.1.3 Power Scan-Chain Interface

The serial shift register provides the control of the various analog switches for bias-current control and connections to the analog test bus. In this implementation this register is a user register controlled by an IEEE Std 1149.1 TAP controller [223]. The analog test bus interface is provided by the IEEE 1149.4 analog test bus extension to 1149.1. Using an 1149.1 TAP allows access to the serial register, while the device is in functional mode. Other serial access interfaces, such as $\mathrm{I}^{2} \mathrm{C}$ or a 3 -wire bus can also be used to control the serial shift register, although they do not allow accessing the register in functional mode. The fact that one can gain access to the shift registers while the device is in functional mode opens unique opportunities for on-chip silicon debugging. For instance, it is possible to debug certain circuit specifications by properly tuning the biasing network of a core in operating mode, e.g., the gain of an amplifier, or the bandwidth of an active filter could be debugged by changing their biasing conditions. Similarly, a core can be isolated and its specification debugged with external input stimuli through the analog test input bus and by adjusting its biasing network. For instance, one can debug the bandwidth and insertion loss of a filter to known input signals, or debug the LSB sections of a data converter. Yet another example is to bypass a core in normal operating mode and to provide its neighboring cores with known input signals, or to analyze a core's output signal through the analog test output bus.


Figure 3-12: DfT with integrated current sensors

### 3.2.1.4 DfT with Integrated Current Sensors

The current sensors can also be placed between the $V_{D D}$ pad and the core's $V_{D D}$ terminal, as illustrated in Figure 3-12. Although at the cost of the increased complexity, placing the sensors in individual power supply lines will enable parallel current-sensing operation, which as a consequence, results in significantly reduced test times. Compared to the Figure 3-8, the DfT now incorporates an Analog Power Output Bus to read out currents in the power line. The biasing network, Analog Test Input Bus, Analog Test Output Bus, Digital CS and OS Interface and two Shift-register controllers are similar. Note that band-gap sensor alterations can
be made, so that the band-gap voltage can be measured and read out on the analog or digital power output bus. In tested systems with limited chip package pin-count, multiple individual blocks can be powered through one chip package pin. In those cases, on-chip current sensors provide additional observability. The supply currents of the individual cores can be found by turning on the biasing network of the cores under consideration. All supply current readings are performed at the core's nominal operating conditions. The outputs of the sensors are chained into an amplifier, with automatic-gain-control features to deal with wide dynamic ranges. The amplifier and post-processing units are part of the Automatic Test Equipment (ATE). The measured current(s) of the core(s)-under-test are used for testing purposes. Similar to the Figure 3-8, the $\varphi$ operator allows any type of mathematical function on the current signatures of any two consecutively enabled cores. Post-processing of the current signatures can be done by any post-processing means, such as for instance integration or FFT.

### 3.2.2. Application Example

The test generation methodology given in Section 3.1 can be employed for both fault detection (to determine whether the circuit is good or bad) and fault isolation (to identify the faulty sub-circuit). As mentioned before, the input to the test generator consists of the circuit description, test stimuli and test program giving the output consisting of test nodes, fault coverage and optimum test stimuli's that are sufficient to detect (or isolate) the failure modes (faults) in the circuit under test. To overcome system-test limitations of the structural cur-rent-based testing, the device-under-test is partitioned into smaller blocks with only limited additional hardware by means of the power-scan DfT technique.

The results shown in the next paragraphs were obtained with limited area overhead (approximately $5 \%$ ), primarily from additional biasing transistors and routing, and at negligible extra power consumption since these bias transistors are not used in normal functional node. Performance loss is insignificant as no switches are placed in the signal path. The total test time required at wafer-level manufacturing test based on current-signature analysis is in three $\sim$ four milliseconds range per input stimuli. As the results indicate, most quasi-static failures in various blocks of the multi-step A/D converter from Chapter 2, depending on the degree of partitioning, are detectable through quasi-static structural test. For the entire A/D converter eleven input stimuli are required, which results in a total test time for the quasistatic test of at most 45 milliseconds. This pales in comparison to around one second needed to perform histogram-based static or approximately one second for FFT-based dynamic A/D converter test offering more then twenty fold reduction in test time. Note that time required to perform these functional tests depends on the speed of the converter and available post-processing power.

### 3.2.2.1 Quasi-Static Structural Test of Fine A/D Converter

Since the linearity of the fine A/D converter determines the overall achievable linearity of the overall converter, let's firstly examine the fine A/D converter into more details. As elaborately examined in Section 2.5 .2 using folding and interpolation technique in the fine $A / D$ converter (Figure 3-13), the number of the required comparators is significantly reduced, however, at the cost of the reduced bandwidth by the number of folds. The nonlinear distribution
of the reference voltages and resistor and preamplifier matching limits the linearity in fine A/D converter, since mismatch effects put a lower boundary on the smallest signal that can be processed in a system. As a result, their influence is most important at the first stage, where the signal levels are small. The offset voltage is major limiting factor of the comparator accuracy as well. If the gain mismatch of preamplifiers is present in the circuit, zero crossing of interpolated signal will be altered. Non-linearity of preamplifiers prevents perfectly linear interpolation as well by shifting the ideal zero crossings, while comparators non-linearity of comparators lead to the wrong comparator decision. Additionally, the error due to the tailcurrent mismatch of folding preamplifiers appears as if it is the offset of the differential pair. Since the zero crossing error due to the tail current mismatch is additive, the number of tail current that need to be matched is the same as the folding degree. As a result, it is beneficial to have a low folding degree since the error due to the tail current mismatch also decreases as the folding degree decreases. Each zero-crossing of the output is ideally determined only by one folding amplifier.


Figure 3-13: Power Scan Chain DfT employed in the Fine $A / D$ converter

Detecting the faults in the first stage is essential since offset of the first stage preamplifiers determine the total referred input offset, providing that the gain of the preamplifiers is high enough. For illustration, two faults as defined by (3-12) are inserted (Figure 3-14), at the output $\Xi_{r 1}$ and at the input biasing node $\Xi_{r 2}$ of first stage amplifier. This fault injection sets the node voltage outside the permitted node variation range characterized by (3-14) as illustrated in Figure 3-15a) and leads to easily spotted integral nonlinearity (INL) errors as shown in Figure 3-15b).

Next, the influence of the modeled fault at the power supply current $I_{D D}$ is examined. As shown in Figure 3-16a), inserting the fault at the observed nodes and simulating at nominal input values will lead to a deviation in the supply current, although, as seen for the fault at the negative output node $\Xi_{r 1}$ a large ambiguity region within error-free $P(G)$ and faulty $P(F)$ circuit probabilities make any decision subject to an error. However, by concurrently applying a linear combination of the inputs stimuli (the input signal, the biasing, reference and the
power supply voltage) one can find the operating region where uncertainty due to the ambiguity regions for both modeled faults is reduced (Figure 3-16b), and, thus, the corresponding probability of accepting the faulty circuit as a error-free is decreased. Next, the significance level of the test $\alpha$ is set and based on the distribution of the test statistics (3-18) the NeymanPearson critical (rejection) region $C^{*}$ is formulated.


Figure 3-14: Schematic of the fine $A / D$ converter. Two observed nodes, at the input and output of the first stage preamplifier are shown

Continuing with the example illustrated in Figure 3-16b), where $P(G): I_{D D n} \sim N(1.946 m A$, $0.23 \mathrm{~mA})$ and $P(F): I_{D D n} \sim N(2.16 \mathrm{~mA}, 0.25 \mathrm{~mA})$ for the fault at node $\Xi_{r}$, the critical region $C^{*}$ for the test to be of significance level $\alpha=0.1$
$\alpha=P\left(Z \geq \frac{\lambda-\mu_{G}}{\sigma_{G} / \sqrt{n}}\right)=1-\Phi\left(\frac{\lambda-\mu_{G}}{\sigma_{G} / \sqrt{n}}\right)=0.1$



Figure 3-15: a) Fault insertion and their relation towards tolerance window defined in (3-14), b) Integral Nonlinearity when faults are inserted in the first stage preamplifier.

Hence, from standard normal tables,
$\Phi\left(\frac{\lambda-\mu_{G}}{\sigma_{G} / \sqrt{n}}\right)=0.9 \Rightarrow \frac{\lambda-\mu_{G}}{\sigma_{G} / \sqrt{n}}=1.282$
leading to the critical region of

$$
\begin{equation*}
C^{*}=\left\{\left(I_{D D 1 \ldots} I_{D D n}\right): \bar{I}_{D D} \geq \mu_{G}+1.282 \frac{\sigma_{G}}{\sqrt{n}}=2.01 \mathrm{~mA}\right\} \tag{3-28}
\end{equation*}
$$

where $\mu_{G}$ and $\sigma_{G}$ are mean and variance of error-free power supply current. Thus, the circuit will be specified as a faulty if its power supply current value $I_{D D n}$ is higher or equal to the threshold $\lambda$.


Figure 3-16: a) Preamplifier $I_{D D}$ bistogram plot at nominal input values for the error-free and for top) fault at node $\boldsymbol{\Xi}_{r 2}$ and bottom) $\Xi_{r 1}$, b) Preamplifier $I_{D D}$ bistogram plot after ATPG optimization for the error-free and for top) fault at node $\boldsymbol{\Xi}_{r 2}$ and bottom) $\boldsymbol{\Xi}_{r 1}$.


Figure 3-17: a) Difference in percentage [\%] between Monte Carlo analysis and limits given by equation (3-14) for the supply current $I_{D D}$ of the error-free and faulty circuit as function of the supply voltage $V_{D D} . I_{D D, \text { max }}$ and $I_{D D, \text { min }}$ denote the tails of the probability function; b) Influence of the inserting of the fault at $\boldsymbol{\Xi}_{r 1}$ on transfer function

A comparable discrimination analysis is performed for all circuit's power supply current values generated as a consequence of inserting the faults at all nodes in the circuit in the entire range specified in the test program. The probabilities $P(G)$ and $P(F)$ as specified in (314) match the spread of more than 1500 Monte Carlo iterations within $1 \%$, while allowing multiple order of magnitude CPU time savings. Figure 3-17a) displays the accuracy of using (314) for a power supply sweep. Influence of the inserting of the fault $\boldsymbol{\Xi}_{r 1}$ on transfer function is illustrated in Figure 3-17b).

In the entire fine $\mathrm{A} / \mathrm{D}$ converter a total of 2198 faults, corresponding to a similar number of nodes, are injected in the fault-free circuit netlist, and simulated according to the test stimuli and the specified test program. The results of the test generator offer an indication for the required circuit partitioning through power-scan DfT, within the framework of circuit performance, area and testability. The tests are performed hierarchically and influenced by circuit architectural aspects, such as feedback among sub-blocks. At the first instance, the supply current of the entire fine A/D converter is found. Next, starting from the comparators and finishing at the first preamplifiers stage, one by one stage is switched off and the supply current is measured.

|  | Nr of | Fault coverage [\%] |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | faults | $\alpha=0.05$ | $\alpha=0.1$ | $\alpha=0.2$ |
| 1 st $^{\text {st }}$ Stage Amplifiers | 45 | 81.5 | 100 | 100 |
| 2 $^{\text {nd }}$ Stage Amplifiers | 119 | 56.3 | 68.9 | 70.6 |
| 1 $^{\text {st }}$ and 2nd Stage Amplifiers | 164 | 67.8 | 78.8 | 84.9 |
| Folding Stage Amplifiers | 102 | 76.5 | 82.4 | 84.3 |
| Total without Folding Encoder | 266 | 68.4 | 78.2 | 93.5 |
| Folding Encoder | 96 | 66.7 | 85.4 | 85.4 |
| Total without DfT | 362 | 68.3 | 79.9 | 81.1 |
| Total with DfT (43 transistors) | 362 | 100 | 100 | 100 |
| Comparators Block | 1836 | 70.4 | 80.1 | 93.2 |
| Total Fine ADC | 2198 | 69.9 | 80.1 | 91.3 |
| TiBLE VII |  |  |  |  |

TABLE VII -FINE A/D CONVERTER TEST RESULTS

Implementing the DfT in such a way ensures that the reference voltages for the preamplifiers inputs of all stages are still provided. The supply currents of the individual cores can be found from the difference between the supply currents found for the different codes, clocked in from left to right out of the bias shift register. Notice that the use of DfT, as shown in Table VII, increases the fault coverage of the preamplifier stages and folding encoder to $100 \%$. The undetected faults in the inactive parts of the comparator's decision stage and storage latch, expose the limitations of the quasi-static approach, due to the dynamic nature of the response. After test stimuli optimization, only three test stimuli (Table VIII) are needed to achieve designated fault coverage from a given input stimuli ramps.

| $\mathrm{V}_{\text {DD }}$ <br> $[1.8-0.0,0.1]$ | $\mathrm{V}_{\text {RESA }}$ <br> $[1.2-1.8,0.1]$ | $\mathrm{V}_{\text {NRESA }}$ <br> $[1.2-0.6,0.1]$ | $\mathrm{V}_{\text {RESB }}$ <br> $[1.8-1.2,0.1]$ | $\mathrm{V}_{\text {NRESB }}$ <br> $[0.6-1.2,0.1]$ | Fault <br> Coverage |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $[0.8]$ | $[1.3]$ | $[1.0]$ | $[1.5]$ | $[0.8]$ | $61.3 \%$ |
| $[0.0]$ | $[1.8]$ | $[0.6]$ | $[1.4]$ | $[1.0]$ | $67.2 \%$ |
| $[0.0]$ | $[1.4]$ | $[1.1]$ | $[1.6]$ | $[0.7]$ | $69.9 \%$ |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $[0.0]$ | $[1.6]$ | $[0.9]$ | $[1.6]$ | $[0.6]$ | $69.9 \%$ |

TABLE VIII - OPTIMUM TEST STIMULI SET FOR FINE A/D CONVERTER

### 3.2.2.2 Quasi-Static Structural Test of S/H, Coarse ADC, Sub DAC and Residue Amplifier

The rest of the observed A/D converter has been evaluated following the similar principles. To enable fault detection based on differences of the power-supply current and prevent fault masking due to the feedback and common-mode regulation the sample-and-hold units are monitored in open-loop. The voltage deviation of the biasing transistors translates to voltage deviation of all biasing levels, which in itself leads to, easily detectable, variations of the power supply current. The faults on the output switches are relatively easy to detect since they have direct impact on the power supply current. A total of 244 faults are injected in the fault-free circuit netlist and simulated according to test stimuli and the test program. The
low-frequency test stimuli offered are ramp for bias current and power-supply voltage and triangle for differential input voltage. The results with the DfT in place are shown in Table IX.

|  | Nr of <br> faults | Fault coverage [\%] |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | 74 | 94.6 | 97.3 | 100 |
| S/H 1 | 74 | 98.6 | 100 | 100 |
| S/H 2 | 74 | 93.2 | 95.9 | 100 |
| S/H 3 | 10 | 100 | 100 | 100 |
| Bias Circuit | 12 | 91.7 | 100 | 100 |
| Output Switches | 244 | 95.5 | 97.9 | 100 |
| Total |  |  |  |  |

TABLE IX - S/H TEST RESULTS
The total fault coverage for the whole sample-and-hold circuit reaches 95.5, 97.9 and $100 \%$ for the probability $\alpha=0.05,0.1,0.2$, respectively, that the fault-free circuit is rejected as a faulty. After test stimuli optimization, five test stimuli are needed to achieve $95.5 \%$ fault coverage from the given input stimuli's ramps (Table X).

| $\begin{gathered} \hline \hline \mathrm{V}_{\mathrm{DD}} \\ {[0.0-1.8,0.1]} \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{V}_{\mathrm{IN}} \\ {[-0.5-0.5,0.1]} \end{gathered}$ | $\begin{gathered} \hline \hline \mathrm{V}_{\text {BIAS }} \\ {[0.4-0.6,0.1]} \end{gathered}$ | $\begin{gathered} \hline \mathrm{C}_{\mathrm{LK} 1} \\ {[0.0-1.8,0.1]} \\ \hline \end{gathered}$ | $\begin{gathered} \hline \hline \mathrm{C}_{\mathrm{LK} 2} \\ {[0.0-1.8,0.1]} \\ \hline \end{gathered}$ | $\begin{gathered} \hline \hline \mathrm{C}_{\mathrm{LK} 2} \\ {[0.0-1.8,0.1]} \\ \hline \end{gathered}$ | Fault Coverage |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| [0.5] | [0.2] | [0.4] | [1.8] | [1.8] | [0.0] | 60.7 \% |
| [1.0] | [0.1] | [0.4] | [1.8] | [0.0] | [1.8] | 78.3 \% |
| [1.0] | [-0.4] | [0.5] | [1.8] | [1.8] | [0.0] | 87.3 \% |
| [0.5] | [0.5] | [0.5] | [0.0] | [1.8] | [1.8] | 90.6\% |
| [0.7] | [0.4] | [0.4] | [1.8] | [1.8] | [0.0] | 95.5 \% |
| $\ldots$ $[0.5]$ | [0. $[-0.2]$ | $\ldots$ $[0.4]$ | [1.8] | $\ldots$ $[0.0]$ | [1.8] | 95.5 \% |

TABLE X - Optimum TEST STIMULI SET FOR S/H
The offered stimuli for coarse A/D converter quasi-static test are adapted ramp-down and ramp-up for the power-supply and input voltage. The fault coverage of $69.5,79.0$ and $88.3 \%$ for the probability $\alpha=0.05,0.1,0.2$, respectively, is accomplished with only two optimized test stimuli for the 996 injected faults in the five-bit coarse A/D converter as shown in Table XI.

|  | Nr of | Fault coverage [\%] |  |  |
| :--- | :---: | :---: | :---: | :---: |
|  | faults | $\alpha=0.05$ | $\alpha=0.1$ | $\alpha=0.2$ |
| Preamplifier 1st stage Block | 54 | 25.9 | 57.4 | 81.5 |
| Preamplifier 2nd stage Block | 51 | 100 | 100 | 100 |
| Total without DfT | 105 | 61.9 | 78.1 | 90.5 |
| Total with DfT (21 transistors) | 105 | 100 | 100 | 100 |
| Comparators Block | 891 | 70.3 | 79.1 | 89.5 |
| Total Coarse ADC | 996 | 69.5 | 79.0 | 88.3 |

TABLE XI - COARSE A/D CONVERTER TEST RESULTS
Once again the faults responsible for the fast dynamic behavior of the comparators were not entirely captured by quasi-static approach. After test stimuli optimization, only two test stimuli's (Table XII) are needed to achieve the previously indicated fault coverage.

| $\mathrm{V}_{\text {DD }}$ | $\mathrm{V}_{\text {INP }}$ | $\mathrm{V}_{\text {INN }}$ | Fault |
| :---: | :---: | :---: | :---: |
| $[1.8-0.0,0.1]$ | $[0.4-0.9,0.1]$ | $[0.9-0.4,0.1]$ | Coverage |
| $[0.1]$ | $[0.8]$ | $[0.5]$ | $32.1 \%$ |
| $[0.2]$ | $[0.5]$ | $[0.8]$ | $69.5 \%$ |
| $\ldots$ | $\ldots$ | $\ldots$ | $\ldots$ |
| $[1.4]$ | $[0.7]$ | $[0.5]$ | $69.5 \%$ |

TABLE XII - OPTIMUM TEST STIMULI SET FOR COARSE A/D CONVERTER

Adapted ramp-down and ramp-up at the top and bottom of the reference ladder and adapted ramp-down (digital code from $2^{\mathrm{N}}-1$ to 0 ) and ramp-up (digital code from 0 to $2^{\mathrm{N}}-1$ ) at the input of the $\mathrm{D} / \mathrm{A}$ converter have been offered and the current through the resistor ladder was measured. When inserting the two modeled parametric faults (resistor in the reference ladder and transistor switch) $\mathrm{D} /$ A converter differential outputs will be shifted by the $\Delta V$, as illustrated in Figure 3-18. The fault in the resistor will shift entire output signal by the $\Delta V$, due to the shifting of the all reference voltages, while the fault at the switch will shift the output value only for the code corresponding to the digital value of that signal. The fault coverage obtained (less then $3 \%$ ) shows that the resistor-based D/A converter is not suitable for current signature-based testing without additional, application specific, adjustments.


Figure 3-18: a) $D / A$ converter differential outputs, b) Influence of the resistors and switches parametric faults on the $D / A$ converter outputs

Inserting the couple of the parametric faults at the input and output of the residue amplifier shifts selected range by the $\Delta V$ as illustrated in Figure 3-19. Fault coverage of the residue amplifier reaches $100 \%$ with the adapted ramp-down and ramp-up for the power-supply and input voltage.


Figure 3-19: a) Fault-free output of the residue amplifier, b) Output of the residue amplifier in the presence of the parametric fault at the input

### 3.3. BIST using a Highly Linear On-Chip Waveform Generator

The constant evolution of the integration capability in CMOS technologies is making possible the development of complex mixed-signal SoC (System on Chip). However, this increasing complexity has the associated issue of more complex and hence more expensive test, which is identified in the SIA Roadmap for Semiconductors as one of the key problems for present and future mixed-signal SoCs. In addition, the diversity of analog circuit designs, the multitude of their performance parameters and their limited observability, make analog and mixed-signal circuit BIST (Built-In Self-Test) a very challenging problem compared to pure digital circuit BIST. Performing the built-in characterization of all the possible parameters would completely avoid the need of external testing, but the required design time and silicon area overhead would often make that option unaffordable. Nevertheless, a reduction of the testing time, through the built-in aided test of a sub-set of the performance parameters of a mixed-signal IC, can positively influence the final cost of the chip. On-chip evaluation and generation of periodic signals are of undoubted interest from this point of view. Conventional sine-wave signal generation methods rely on an analog oscillator consisting of a filtering section and a non-linear feedback mechanism [224], by adapting digital techniques, which facilitates a digital interface for control and programming tasks [225-228] or by employing the programmable integrator followed by filtering segment [229-230]. In an analog oscillator based techniques a non-linear feedback mechanism forces the oscillation while the filtering section removes the unwanted harmonics. However, the quality of the generated signal depends on the linearity and selectivity of the filter and the shape of the nonlinear function (smooth functions are needed for low distortion), which requires a lot of area and power. In digital techniques, by exploiting the noise shaping characteristics of $\Sigma \Delta$ encoding schemes use of the $\mathrm{D} / \mathrm{A}$ converter is avoided [225-228]. In essence, a one-bit stream $\Sigma \Delta$ encoded version of an $N$-bit digital signal is generated and the shape of a filter is matched with the noise shaping characteristics of the encoded bit stream. Although, these schemes are valid for single and multi-tone signals they require large bit-stream lengths and a highly selective filter to remove the noise. In addition, these approaches are frequency limited due to the need of very high over-sampling ratios. On the other hand, the programmable integrator such as the one proposed in this section [231] allows continuous-time periodic analog signal generation and in essence, fulfils the function of the $\mathrm{D} / \mathrm{A}$ converter. The method has the attributes of digital programming and control capability, robustness and reduced area overhead, which make it suitable for BIST applications. The prototype based on continuous-time transcon-ductor-capacitor-transconductor ( $G_{m}$-C-OTA) technique and fabricated in 65 nm CMOS technology is the only one reported with the possibilities to characterize and test (frequency domain specifications, linearity, etc.) high-speed, high resolution (up to 12 bit) A/D converters.

In the continuous-time transconductor-capacitor $\left(G_{m}-C\right.$ ) technique the bandwidth is only limited by the internal poles of the transconductor, which can approach that of the transistor $f_{T}$ [232]. Additionally, the bandwidth can be maximized using transconductors without internal poles [233]. However, parasitic wiring capacitances, the output capacitance of the transconductor and the input capacitances of the following transconductors augment the integrating capacitors and thus shift the integrator time-constant from the desired value. The continuous tuning of transconductors is performed at the expense of large signal handling capability [234]. The correct control signal, a current or voltage, can be derived using the masterslave tuning scheme [232].

In a $G_{m}$ C-OTA integrator, the output of the transconductor is buffered with a Miller integrator [232], thereby reducing the sensitivity to parasitic capacitances. The latter amplifier can be a simple, wide-band OTA, like a common-source stage or differential pair, as it does not drive resistive loads. The $d c$ gain of the structure is the sum of the $d c$ gains of the two amplifiers meaning that cascoding in the OTA is not required to achieve a sufficient $d c$ gain [235]. The $G_{m}$-C-OTA filters have low complexity and are power- and area efficient. As the transconductor limits the linearity of a $G_{m-}-$-OTA integrator distortion level is comparable to that of $G_{m}-C$ structures using equivalent transconductors. The $G_{m-} C$ topology suffers from low $d c$ gain and, more importantly, high sensitivity to parasitic capacitance at the output node. However, since the $G_{m}$-C-OTA structure does not suffer from the aforementioned problems as the transconductor does not have to swing a large voltage range; it can tolerate larger and more nonlinear parasitic capacitance and it can be less sensitive to noise, $G_{m}-C$-OTA structure is chosen for continuous-time implementation. Furthermore, either a low- or high-outputimpedance Miller integrator can be employed as it only needs to drive capacitive loads. In this implementation, high-output-impedance OTA is employed as it tends to have higher unitygain frequencies, be simpler and have less power dissipation.

To realize the proposed analog signal generation in $G_{m}$-C-OTA technique illustrated in Figure 3-20, multiple transconductors are connected in parallel to sum all the output currents. Scaling the input transconductance by a factor $K$ introduces only a gain factor in the overall transfer function. The transconductor is based on a linearized voltage follower driving a resistor. The transconductance stems primarily from the resistor and the linearity is therefore limited only by the material of the resistor and the amount of loop gain linearizing the voltage follower. The OTA used in the integrator shown in Figure $3-20$ is a simple $n$-channel differential pair with an active load. Applying a capacitive feedback around it leads to a parasitic right half-plane zero in the closed-loop transfer function, causing a serious degradation in the phase response of the integrator near its unity-gain frequency. An ideal unity-gain buffer, inserted in the feedback path eliminates this right half-plane zero. However, the buffer, implemented here as a simple source-follower, has a finite output impedance. This creates a high-frequency left half plane zero which causes an unwanted phase-lead error. To create a parasitic phase-lag that nominally cancels the phase lead created by the source follower and provide additional gain a variable-gain voltage amplifier is connected in cascade. The gain of this amplifier can be varied by shunting the feedback resistor with a MOSFET in triode region $\left(T_{1-4}\right)$. Changing the gate voltage of this MOSFET varies the filter unity-gain frequency.


Figure 3-20: $G_{m}$-C-OTA integrator and biquad filter realization

The operating principle of the $G_{m}$ stage can be explained from Figure 3-21. A differential input voltage causes a current to flow through the resistor $R_{D E G}$ to the source node of $T_{1}$. The feedback loop formed by the transimpedance stage $T_{3}$ and $T_{13}$, and transconductance stage $T_{11}$ and $T_{15}$, forces all of this current to flow to the other input, thus making the drain current and $V_{G S}$-voltage of $T_{1}$ constant and thereby linearizing the voltage follower $T_{1}$. The linear voltage follower gives a linear relationship between the input voltage and the current through the resistor $R_{D E G}$ supplied by the output transconductance stage. Since the sum of the currents from the two outputs of the transconductance stage is constant it follows that the current from the other output is also a linear function of the input voltage, and that this current may be used as an output of the whole transconductor -structure. The transimpedance stage is a single transistor $T_{13}$ in common-gate configuration. This stage provides a low impedance input for the voltage follower $T_{1}$ and a suitable bias level for the transconductance stage $T_{11}$ extending the swing capability of the input. Similarly, it increases gain in the feedback loop reducing the gain error and linearizes the voltage follower. However, source degeneration lowers the value of the effective transconductance and, in this way, the dc gain of the integrator. To solve this, the output impedance is increased by using nonminimal transistor lengths in the output branches. The capacitors $C_{1}$ and $C_{2}$ stabilize the feedback loops of $G_{m}$. To avoid significant reductions in the signal handling capability of $G_{m}$ stage, the input-referred $d c$ offset voltage has to be canceled in the input stage of $G_{m}$ stage. This has been implemented with a $p$-channel differential pair $T_{18-19}$. The output signals from this differential pair are connected to the drains of the input devices of $G_{m}$ so as to be able to control the gate-source voltages of the input devices and thus the input-referred $d c$ offset voltage of $G_{m}$. The $d c$ offsets are canceled with an off-chip control signal $V_{\text {officer }}$


Figure 3-21: Transconductor $G_{m}$ realization
The voltage amplifiers were implemented as gain-boosted folded cascode amplifiers as shown in Figure 3-22. A $n$-channel input pair $T_{1-2}$ is placed in parallel with a $p$-channel input pair $T_{34}$ to process signals from rail to rail. To make the transconductance as a function of the commonmode input voltage constant a simple feed-forward method is applying current switches $T_{5.8}$ [237]. The current switches are divided into two transistors of which the drains are connected to the drains of the corresponding input-stage transistors. By adding the currents to the outputs of the input-stage transistors the output current of the input stage does not change as a function of the common-mode input voltage. Since relatively small current-switch transistors can be used, their noise contribution to the noise of the amplifier can be made relatively small. With a common-mode feedback circuit comprising of $T_{23.35}$ [238], where the resistor/capacitor network in balanced resistor/capacitor differential-difference amplifier com-mon-mode feedback structure is replaced by a transistor network consisting of $T_{23,28}$, the output common mode level can be sensed without changing the impedance at the system output.

The signal path from the opamp output to the gate of $T_{32}$ is built exclusively by sourcefollower stages, so the gate voltage $V_{G(T 32)}$ is a monotonically increasing function of the output common-mode level. Similarly, since $T_{23-28}$ are complementary types of transistors, the output common-mode level is guaranteed to be detected in full-swing range without pulling any transistors of $T_{31-35}$ away from the saturation region. Additionally, since all nodes in the network $T_{23.28}$ are low impedance nodes, no additional stability problems will occur.


Figure 3-22: Voltage amplifier schematic
To keep the filter bandwidth relatively constant with temperature and process variations, tuning of the characteristic frequency and a quality factor $Q$ of the filter is required. One advantage of the $G_{m}$-C-OTA filter is that passive components like the resistor and inductor can be realized with OTA and capacitor. The resistor is realized by connecting negative input of OTA to positive output and the function of inductor can be realized at certain frequency by using two OTAs and a capacitor. However, linearity of the resistors and the inductors is highly dependent on the performance of OTA. If the OTA has finite bandwidth characteristics, the gain and phase of the filter will deviate from its ideal frequency response. The specific nature of the deviation will be a function of the OTA's open-loop characteristic and the filter's desired response. However, in comparison to the active RC realization where full opamp is employed, due the simplicity of the OTA, active $G_{m}-C-O T A$ filters can be pushed to higher frequencies before OTA gain-bandwidth product impacts the filter's response. Although the absolute value of capacitors and transconductances are quite variable; capacitors vary due oxide thickness variations and etching inaccuracies ( $\sim 15 \%$ ) and transconductances due to mobility, oxide thickness, current, device geometry variations (could vary by more than $40 \%$ with process, temperature and supply voltage variations), their ratios can be very accurate and stable over time and temperature if special attention to layout (e.g. interleaving, use of dummy devices, common-centroid geometries...) is provided, e.g. capacitor ratio matching with $<0.05 \%$, and $G_{m}$ ratio matching $<0.5 \%$, providing well-preserved relative amplitude and phase versus frequency characteristics with the need to tune only continuoustime filter critical parameters.

There are many different tuning systems such as adaptive tuning circuit, direct tuning strategy, master-slave tuning circuit, etc. In PLL tuning, the output of the VCO or master filter is compared with the reference signal through a phase detector. If there is any difference between reference signal and the output, a certain level of voltage, which is proportional to phase difference between reference signal and VCO or master filter output, is produced and the voltage is filtered through low-pass filter to eliminate high frequency component. Then only $d c$ control voltage is applied to both master and main filter to correct the frequency difference. For $Q$ factor control, amplitude detector or peak detector is often used to com-
pare the magnitude at the certain frequency. Like frequency tuning, the peak of the master filter is compared with the reference signal at the certain frequency. Then peak difference is usually amplified and low pass filtered to apply $Q$ factor control voltage to the main filter. However, to utilize such a tuning, it is assumed that the filter's bandpass gain at center frequency is equal (or proportional) to the quality factor $Q$. Nevertheless, in the presence of dominant parasitics this relation may not hold, especially at high $-Q$ values. Also, nonlinearities of the filter affect the gain versus $Q$ relationship, which may result in further $Q$-tuning errors. Here, the technique applied utilizes the phase response of a second-order block rather than the magnitude. In this case, $Q$-tuning, as well as center frequency tuning, is independent of the filter gain. By fitting the output phase at two reference frequencies to the known values, which can be calculated from the desired response, both center frequency and $Q$ are tuned accurately. Utilizing a digital technique, only one tuning loop is allowed to operate at a given time, which improves the stability of the tuning circuit and eliminates the need for slow loops.

Figure 3-23 shows the complete tuning system. The PLL realized is a standard implementation. The low-frequency clock signal Clke determines the tuning cycles in which the filter's frequency is switched between referenced frequencies. The signals $V_{\text {bigb } b}$ and $V_{\text {low }}$ are delayed clocks, whereas $V_{\text {up }}$ and $V_{\text {domn }}$ are the control voltages. The filter is calibrated when the Tune signal is high. Normal operation of the filter (i.e., processing the signal) is resumed when the Tune signal is set to low, where the tuning voltages $V_{u p}$ and $V_{\text {domp }}$ are hold at their proper values. Since the two reference frequencies cannot be applied simultaneously, the frequency of the filter changes periodically between referenced frequencies. When one reference frequency is applied to the filter, the low-pass output is compared with $V_{\text {lon }}$.


Figure 3-23: Tuning circuitry for the Gm-C-OTA realization

The low-pass output is connected to the clock input of the flip-flop whereas the reference is applied to the D input. Assuming that transition occurs at the rising edge of the clock, the flip-flop stores high output level if the low-pass delay is more than $V_{\text {lonn }}$, otherwise the output is zero. In the next phase, when the filter input is at different reference frequency, delay of the low-pass output is compared with $V_{\text {big }, \text {. }}$ The first set of D flip-flops compares the low-
pass phase with the appropriate references and the output is stored in the following D flipflops at the end of each cycle. The counters are updated by the Clk signal and are enabled only when the Tune signal is high. Note that $V_{u p}$ and $V_{\text {domn }}$ do not change simultaneously (in the same tuning cycle), which ensures the stability of the tuning loops. Similarly, DACs operate at very low frequency and can be avoided in case of a digitally tunable filter [236]. The simulation results shown in Figure 3-24, illustrate the feasibility of the proposed continu-ous-time realizations. The signal generator has been laid out through a two-level matching process. In lower level, the internal transistors of every transconductor have been laid out following a common centroid technique. Similarly, in the higher level, every $G_{m}$ cell has been arranged in a common centroid structure. A similar rule has been applied for capacitors, which have been laid out in an array of unit capacitors with common centroid geometry. The filter outputs were buffered using a simple source follower before connecting them to the pads. The implemented double feedback structure yields an overall improvement on the filter linearity performance. With the opposite phase of the distortion amount introduced by the transcoductors in the feedback path, smaller loop (with $G_{m_{2}}$ ) partially attenuates nonlinearity deriving from transconductor $G_{m 3}$, whereas larger loop (with $G_{m \neq}$ ) attenuates that deriving from the input transconductor $G_{m 1}$. The transconductor $G_{m 2}$ introduces some partial positive feedback (acts as a negative resistor) so that the quality factor can be made as high as desired, only limited by parasitics and stability issues. The filter cut-off frequency is controlled through $G_{m 3}$ and $G_{m 4}$, the Q -factor is controlled through a $G_{m 2}$, and the gain can be set with $G_{m}$. This property of varying the gain while maintaining constant the frequency and quality factor could be profited to embed variable gain in order to optimize the dynamic range between sections of high order filters. Table XIII gives a comparison between the presented generator and other reported approaches. It demonstrates that the proposed sine-wave signal generation based on the $G_{m i} C$-OTA technique with the measured performance of 74 dB at 81 MHz while occupying only $0.11 \mathrm{~mm}^{2}$ is currently the best reported and the only one available for testing of high-speed, high-resolution (up to 12 bit ) A/D converters.


Figure 3-24: a) Open-loop gain of the voltage amplifier, two different gain settings, b) Spectral purity of the generated signal

|  | Continuous-Time Oscillator [224] | Analog $\Sigma \Delta$ Oscillator [228] | ROM-based Generator [226] | Variable Gainbased [229] | This Section [231] |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Technology | $0.8 \mu \mathrm{~m}$ CMOS | $\text { FPGA }+6^{\text {th }} \text { order }$ <br> filter | $0.8 \mu \mathrm{~m}$ BiCMOS | $0.35 \mu \mathrm{~m}$ CMOS | $0.065 \mu \mathrm{~m}$ CMOS |
| Area | $0.63 \mathrm{~mm}^{2}$ | ----- | $\begin{aligned} & 0.83 \mathrm{~mm}^{2}+4^{\text {th }} \\ & \text { order filter } \end{aligned}$ | $0.1 \mathrm{~mm}^{2}$ | $0.1 \mathrm{~mm}^{2}$ |
| THD | 44dB@ 25MHz | 84dB @ 5kHz | not reported | 67dB@ 41MHz | 71 dB @ 81MHz |
| SFDR | 49dB@ 25MHz | 86dB@ 5kHz | 65dB @ 10MHz | 67dB@41MHz | 74 dB @ 81MHz |

TABLE XIII - COMPARISON WITH DIFFERENT APPROACHES

### 3.4. Conclusion

The increasing costs associated with testing and debugging of complex mixed-signal electronic systems has motivated various research efforts to explore efficient testing methodologies. Structural, fault-model based testing has been recognized as a promising alternative or addition to expensive specification testing. The presented inexpensive structural methodology [187] intends to facilitate test pattern generation at wafer level test, thereby providing a quantitative estimate of the effectiveness and completeness of the testing process. In the fault-based, structural testing, the fault model cannot only describe the fault effect more clearly and offer clues to derive the test stimuli, but also makes it more feasible to modify the input stimuli and to estimate its fault coverage. This approach is well established for digital circuits for which there are numerous test pattern generators and fault simulators based on a pass/fail decision, as is the case of the single-stuck-at fault models. Recent studies have revealed, however, that faults which shift the operating point of a transistor level analog circuit can be detected by inexpensive quasi-static testing or power supply current monitoring. With that in mind, the proposed fault model utilizes the sensitivity of the circuit's quasistatic node voltages to process variations and consequently the current deviance so as to differentiate the faulty behavior. With the Karhunen-Loève expansion method, the parameters of the transistors are modeled as stochastic processes over the spatial domain of a die, thus making parameters of any two devices on the die, two different correlated random variables.

In fault-based approaches to analog testing the response from the device under test during manufacture is compared with the pre-compiled fault responses and a decision of rejection of the device is based on this comparison. It has been recognized that failures in analog circuits may assume a continuum of values, and a band-fault approach has been proposed for linear analog circuits where the signature for each fault assumed the form of a band and the decision of pass/fail made on the basis of comparison of bands. Since normally the fault list is quite large in analog fault simulation, it is very important to generate the tolerance window fast and efficiently. Therefore, the bounds on the circuit response are calculated by performing a mathematical evaluation of the performance function attributes against physical tolerance limits defined by device mismatch yielding the significant CPU-time savings.

The Bayes risk is computed for all stimuli and for each fault in the fault list. The stimuli for which the Bayes risk is minimal, is taken as the test vector for the fault under consideration. The proposed Neyman-Person statistical detector [207], which is a special case of the Bayes test, provides a workable solution when the a priori probabilities are unknown, or the Bayes risk is difficult to evaluate or set objectively. The tests are generated and evaluated taking into account the potential fault masking effects of process spread on the faulty circuit responses. The test generator technique also allows the test procedure to test only for the most likely group of faults induced by a manufacturing process.

To overcome system-test limitations of the structural current-based testing, the device-undertest is partitioned into smaller blocks with only limited additional hardware by means of the power-scan DfT technique. The variety and number of cores in modern Systems-on-Chip ( SoC ) and their nature type, e.g. analog, complicate the testing phase of individual blocks, of combinations of blocks and ultimately of the whole system. The problem in the analog domain is that it is much more difficult to scan signals over long distances in a chip and across
its boundary to the outside world, since rapid signal degradation is very likely to occur. The proposed DfT [219] intends to facilitate structural, signature-based testing, by providing the means to observe the current (or voltage) signatures of individual cores (or parts of) instead of observing the current (or voltage) signature of the whole analog SoC. Additionally, as in case of multi-step A/D converters, such a DfT lessen the impact of overlap between the conversion ranges implemented to obtain high linearity, which can either mask faults or give an incorrect fault interpretation.

As the results of test pattern generator indicate, most quasi-static failures in various blocks of the twelve-bit two-step/multi-step A/D converter, depending on the degree of partitioning, are detectable through power-supply current structural test offering more then twenty fold reduction in test time in comparison to more traditional, functional histogram-based static or FFT-based dynamic ADC test. Only limitations of the quasi-static approach are due to the dynamic nature of the response such as faults in the inactive parts of the comparator's decision stage and storage latch. Furthermore, the fault coverage obtained shows that the resis-tor-based D/A converter is not suitable for current signature-based testing without additional, application specific, adjustments.

Besides DfT, BIST approaches are similarly an efficient way to help decrease the test development and debugging costs. The analog circuits are usually tested using functional approaches, often requiring a large data volume processing, high accuracy and high speed ATEs. In addition, these analog cores are normally very sensitive to noise and loading effects, which limit the external monitoring and make their test a difficult task. BIST schemes consist on moving part of the required test resources (test stimuli generation, response evaluation, test control circuitry, etc) from the ATE to the chip. However, the diversity of analog circuit designs, the multitude of their performance parameters and their limited observability, make analog and mixed-signal circuit BIST a very challenging problem compared to pure digital circuit BIST. Performing the built-in characterization of all the possible parameters would completely avoid the need of external testing, but the required design time and silicon area overhead would often make that option unaffordable. Nevertheless, a reduction of the testing time, through the built-in aided test of a sub-set of the performance parameters of a mixed-signal IC, can positively influence the final cost of the chip. On-chip evaluation and generation of periodic signals are of undoubted interest from this point of view as most of the analog systems can be characterized and tested (frequency domain specifications, linearity, etc.) using this kind of stimuli. The method for sine-wave signal generation proposed in this thesis [231] relay on the programmable integrator, which allows continuous-time periodic analog signal generation. The method has the attributes of digital programming and control capability, robustness and reduced area overhead, which make it suitable for BIST applications. The prototype fabricated in 65 nm CMOS technology with the measured performance of 74 dB at 81 MHz while occupying only $0.11 \mathrm{~mm}^{2}$ is currently the best reported and the only one available for testing of high-speed, high-resolution (up to 12 bit) A/D converters.

## CHAPTER 4.

## MULTI-STEP ANALOG TO <br> DIGITAL CONVERTER DEBUGGING

CMOS technologies move steadily towards finer geometries, which provide higher digital capacity, lower dynamic power consumption and smaller area resulting in integration of whole systems, or large parts of systems, on the same chip. However, due to technology scaling, ICs are becoming more susceptible to variations in process parameters and noise effects like power supply noise, cross-talk reduced supply voltage and threshold voltage operation. Likewise, imperfection at the manufacturing stage, with a raw factory yield between $50-95 \%$, depending on the maturity of the process technology, silicon area, and extending the use of 193 nm lithography for sub- 65 nm CMOS technology, where Resolution Enhancement Techniques are no longer sufficient for accurate device definition and significantly impact circuit performance. With increased system complexity and reduced access to internal nodes, the task of accurately testing these devices is becoming a major bottleneck. The large number of parameters required to fully specify the performance of mixed-signal circuits and the presence of both analog and digital signals in these circuits makes the testing expensive and a time consuming task. Particularly for nanometer CMOS ICs, the large number of metal layers with increasing metal densities, prevents easy physical probing of the signals for debug purposes. Since parameter variations depend on unforeseen operational conditions, chips may fail despite they pass standard test procedures. Several circuit techniques and algorithms are introduced in this Chapter to enhance debugging development. Additionally, discussions on how to guide the test with the information obtained through monitoring process variations, how to estimate the selected performance figures, and how to supplement converter calibration are presented.

### 4.1. Concept of Sensor Networks

Traditional test methods for analog circuits rely on specification testing, in which some or all response parameters are checked for conformity to the design specifications. However, specification testing is time consuming and hence, also expensive. Although several attempts [240-248] have been made to alleviate the increase of test difficulties of A/D converter' testing and debugging, none of these methods provides the possibilities for early identification of excessive process parameter variations. In [240], DSP techniques for data analysis are utilized. However, the technique requires intensive computation and on-chip availability of both, $\mathrm{A} / \mathrm{D}$ and $\mathrm{D} / \mathrm{A}$ converters. In [241], processing core circuits are incorporated into a VXI bus-based system, which performs both static and dynamic tests. A similar system with external instruments is developed in [243]. A large amount of sampled data must be collected to support both methods. The approach in [244] relies on analog circuitry and reference voltages for measurements and allows testing of only $\mathrm{D} / \mathrm{A}$ converter-based $\mathrm{A} / \mathrm{D}$ converters. In the oscillation-test method in [245], the impact of the control logic delay and the imperfect analog BIST circuitry on the test accuracy is not assessed. In [246], the linearity of the A/D
converters is tested by monitoring the LSB externally. In [247] an efficient polynomial-fitting algorithm for $\mathrm{D} / \mathrm{A}$ converter and $\mathrm{A} / \mathrm{D}$ converter BIST is proposed. The drawback is again the need of both, on-chip A/D converter and D/A converter. The viability of a histogrambased BIST approach in case of a sine-wave input test signal is investigated in [248]. Applying the sequential decomposition to the test procedure, although reducing the additional circuitry, implies that a high number of input test patterns are required to complete the test.

Functional faults in each of the analog component in the multi-step A/D converters affects the transfer function differently [249] and analyzing this property forms the basis of the approach described in this chapter [250]. To enhance observation of important design and technology parameters, such as temperature, threshold voltage, etc., and to provide valuable information, which can be used to guide the test and to allow the estimation of selected performance figures, dedicated sensors are embedded within the functional cores. Additionally, by monitoring on-chip process deviations the proposed method facilitates fast identification of excessive process parameter variations and provides a reliable and complementary method to quickly discard faulty circuits in wafer and final tests without testing the complete device. Such a test method reduces the cost associated to production tests, since this early detection of the faulty circuits avoids running an important fraction of traditional tests. Detecting faulty devices at wafer level has the additional advantage that packaging costs (which commonly represent $25 \%$ of the total system cost) can be avoided. Economic considerations are only one of the advantages of providing die-level process variation observability. Other advantages include increased fault coverage and improved process control, diagnostic capabilities, reduced IC performance characterization time-cycle, simplified test program development and easier system-level diagnostics.

### 4.1.1. Observation Strategy

From a circuit design perspective parametric process variations can be divided into inter-die and intra-die variations. Inter-die variations such as the process temperature, equipments properties, wafer polishing, wafer placement, etc. affect all transistors in a given circuit equally. For the purposes of circuit design, it is usually assumed that each component or contribution in inter-die variation is due to different physical and independent sources; therefore, the varying component can be represented by a deviation in the parameter mean of the circuit. Intra-die variations are deviations occurring within a die. These variations may have a variety of sources that depend on the physics of the manufacturing steps (optical proximity effect, dopant fluctuation, line edge roughness, etc.) and the effect of these non-idealities (noise, mismatch) may limit the minimal signal that can be processed and the accuracy of the circuit behavior. For linear systems, the non-linearities of the devices generate distortion components of the signals limiting the maximal signal that can be processed correctly. Although, certain circuit techniques such as using a small modulation index for the bias current to reduce the effect of distortion non-idealities, or using large device sizes to lower mismatch, and utilizing low-impedance levels to limit thermal noise signals, they have, however, important consequences on the power consumption and operation speed of the system.

In general, the design margins for mixed signal designs depend significantly on process parameters and their distributions across the wafer, within a wafer lot and between wafer lots, which is especially relevant for mismatch. Measurement of these fluctuations is paramount for stable control of transistor properties and statistical monitoring. The evaluation of these
effects enables the efficient development of test patterns and test and debugging methods, as well as ensures good yields. IC manufacturing facilities try to realize constant quality by applying various methods to analyze and control their process. Some of the quality control tools include, e.g. histograms, check sheets, pareto charts, cause and effect diagrams, defect concentration diagrams, scatter diagrams, control charts, time series models and statistical quality control tools, e.g. process capability indices, and time series. Process control monitoring (PCM) data (electrical parameters, e.g. MOS transistor threshold voltage, gate width, capacitor Q-value, contact chain resistance, thin-film resistor properties, etz. measured from all the test dice on each wafer) is required to be able to utilize these quality control tools. Making decisions about if the product or process is acceptable, is by no means an easy task, e.g. if the process/product is in control and acceptable, or in control but unacceptable, or out of control but acceptable.


Figure 4-1: Observation strategy

Masks for wafers are generally designed so that a wafer after being fully processed through the IC manufacturing process will contain several test dice. The area consumed by a test die is usually quite large, i.e. sometimes comparable to several ordinary production dice. Measuring the electrical properties from the test dice gives an estimate of the quality of the lot processing, and device requirement to fulfill a priori specifications e.g. temperature range, speed. Finally the IC devices are tested for functionality at the block level in the wafer probing stage, and the yield of each wafer is appended to the data. The tester creates suitable test patterns and connects signal generators online. It digitizes the measurement signals and finally determines, according to the test limits, if the device performs acceptably or not. Then, the wafer is diced, and the working dice are assembled into packages. The components are then retested, usually in elevated temperature to make sure they are within specification.


Figure 4-2: Concept illustrated on multi-step $A / D$ converter

Silicon wafers produced in a semiconductor fabrication facility routinely go through electrical and optical measurements to determine how well the electrical parameters fit within the allowed limits. The yield is determined by the outcome of the wafer probing (electrical testing), carried out before dicing. The simplest form of yield information is the aggregate pass/fail statistics of the device, where the yield is usually expressed as a percentage of good dice per all dice on the wafer. In principle, yield loss can be caused by several factors, e.g. wafer defects and contamination, IC manufacturing process defects and contamination, process variations, packaging problems, and design errors or inconsiderate design implementations or methods. Constant testing in various stages is of utmost importance for minimizing costs and improving quality. Figure 4-1 depicts the proposed observation strategy block diagram for dice wafer probing. A family of built-in process variation sensing circuits is placed (at least) at each corner of the device-under-test as it maximizes the sensing capability of process variations due to process gradients or are embedded in the device-under-test itself. Depending on the size of the DUT, additional sensors can be placed in and around the DUT to form the additional statistical mass. Figure 4-2 depicts the test strategy block diagram applied to a two-step / multi-step A/D converter. Note that around each sub-block a sensining circuitry is placed.

### 4.1.2. Integrated Sensor

The complete test scheme including the die-level process monitor circuit, detector, reference ladder and the switch matrix to select the reference levels for a decision window, the interface to the external world, control blocks to sequence events during test, the scan chain to transport the pass/fail decisions, and the external tester is illustrated in Figure 4-3. The analog decision is converted into pass/fail (digital) signals through the data decision circuit. The interface circuitry, allows the external controllability of the test, and also feeds out the decision of the detector to a scan chain. The test control block (TCB) selects through a test multiplexer (TMX) the individual die-level process monitor circuit measurement. Select, reference and calibration signals are offered to the detector through this interface circuitry. Digital control logic can be inserted on the chip or done externally.


Figure 4-3: Test scheme block diagram

The die-level process monitor (DLPM) circuits can be extracted from selected structures in the device-under-test. This selection, although easily generalized, relies on the knowledge and analysis of the device-under-test itself, so the resulting DLPM circuits and reference voltages are related to the device-under-test specifications and performance figures under study. Alternatively, die-level process monitor circuits can be designed as an array of transistor pairs as well, each of the different size, where one pair of the $n$-channel and $p$-channel transistors is selected through the internal decoding/selection circuitry. Loading for each transistor pair can be extracted from the device-under-test or set independently. The data detector compares the output of the die level process monitor against a comparison reference window, whose voltage values (corresponding to the required LSB values) are selected from the reference ladder or set externally. The reference voltages defining the decision windows are related to the device-under-test specifications and performance figures under study. By sweeping the reference voltage until a change in the decision occurs, it is possible to detect the tolerance of the die-level process monitor circuit under test, which in turn is a mirror of the actual circuit component in the device-under-test. This information can be used to assess whether the whole device-under-test is likely to be faulty, or to adjust the test limits in the ATE to test the device-under-test.

Die-level process monitor circuit testing is based on a pass/fail condition of a window rather than on a single threshold. In contrast to single threshold decisions, testing against a decision window requires differential measurements. Due to the differential nature of the measurements, two runs with interchanged detector references are needed in each test to ensure a proper pass/fail decision. This double-measurement protocol allows the definition of a pass/fail window, instead of a single pass/fail level. Since the result of each run is a digital one-bit signal, the computation of the test result can be done either on-chip adding some simple logic to the detector, or off-chip using resources located in the tester itself. Two runs $m_{t 1}$ and $m_{t 2}$ are needed with interchanged data decision circuit references, consisting of two thresholds $m_{t, 2 l}$ and $m_{t, 2 r}$ If a test is successful, the measurement point plus uncertainty due to noise, $m_{t, 2}+\zeta$, will lie within the range given by ( $m_{t, 2 b} m_{t, 22}$ ), where $\varsigma$ is the uncertainty due to noise. As a result, the following inequalities hold,

$$
\begin{gather*}
m_{t 1,2 l} \leq m_{t 1,2}+\varsigma \leq m_{t 1,2 r}  \tag{4-1}\\
m_{t 1,2 l}-\max (\varsigma) \leq m_{t 1,2} \leq m_{t 1,2 r}-\min (\varsigma)
\end{gather*}
$$

Assuming noise $\varsigma$ falls in the range of $(-\Delta, \Delta), m_{t, 2}$ satisfies the following inequality detection thresholds in the presence of measurement noise is

$$
\begin{equation*}
m_{t 1,2 l}-\Delta \leq m_{t 1,2} \leq m_{t 1,2 r}+\Delta \tag{4-2}
\end{equation*}
$$

The reference voltages defining the decision windows are related to the device-under-test specifications and performance figures under study. By sweeping the reference voltage until a change in the decision occurs, information about the process variations can be extracted. The performance of the detector in terms of resolution and robustness against process variations is a major concern for the intended application. The robustness against process variations is provided by an auto-zeroing scheme. If a better resolution is required, the efficiency of this auto-zeroing can be improved, at the expense of area overhead, by increasing the value of the input capacitors and/or the preamplifier gain. However, the auto-zeroing scheme does not assure the functionality of the comparator. For instance, a stuck-at fault affecting the output memory element will not be corrected and it will result in a faulty detector. For this reason, a
previous test stage to test the detector functionality has to be added to the test protocol. Figure 4-4 illustrates the timing diagram of the required control signals (external and on-chip generated ones). When the Enable signal is high, the system enters the test mode. In the test mode, two main phases can be distinguished according to the state of signal $\phi$. If $\phi$ is high, the inputs of the detector are shorted to the analog ground to perform a test of the detector itself, e.g. the circuit is in the auto-zeroing mode, whereas if $\phi$ is low the particular die-level process monitor circuit is connected to the detector and tested. Each of these phases takes four master clock periods, two with the reference signal set to the upper limit of the comparison window and the other two with the reference set to the lower limit. During the detector auto-test, the change of the reference should cause the output to change state, since the input is set to zero.


Figure 4-4: Clocking scheme
The detection of this change is a quick and easy proof of the functionality of the detector. During the die-level process monitor circuit test, the output of the DLPM is sequentially compared with the references to determine whether the measurement is inside the expected window or not. In both cases, a simple shift register triggered by the signal labeled Read acquires the detector output. The rising edges of the Read signal are located at the hold state of the detector. The test output will be a four-bit signal, labeled $a_{0} a_{1} a_{2} a_{3}$, which codifies the four different states. The overall result of the test is given by $T=\left(a_{0} \oplus a_{1}\right) \&\left(a_{2} \oplus a_{3}\right)$. This test result can be computed either on-chip in a DSP unit, as depicted in Figure 4-3, or off-chip. Once the result is available (either the test result itself or the four-bit number $a_{0} a_{1} a_{2} a_{3}$ without processing) it can be fed to a scan chain scheme for its later extraction.


Figure 4-5: a) Test result as a function of flip-flops outputs, b) Comparator switching

Notice that the control signals related to the scan chain are not shown in the timing diagram. In addition, it is important to remark that the system features an additional test mode to test all the flip-flops used in the test scheme (not represented in the figure for simplicity). When this test mode is activated, the flip-flops are isolated from the rest of the circuitry and connected together as a shift register. Additional input/output tests for this purpose are also available. Different simulations have been carried out as illustrated in Figure $4-5$ to verify the functionality. A 'pass' die-level process monitor circuit test event denotes the measurement inside the comparison window, while a 'fail' DLPM test event is obtained with a slightly narrower comparison window. At the end of the evaluation time the test output is a go/nogo digital signal, which combines the result of the detector test and the die-level process monitor circuit test. Note that the implementation of the clock generation circuitry needs a control signal to set the initial conditions in the D-flip-flops to a known value. This signal can be externally or internally generated, for instance it can be triggered by the rising edge of the enable signal. All the flip-flops used are scannable and there is a flip-flop test enable signal for that purpose. For a proper definition of the comparison window, the digital correction and the offset cancellation implemented in the actual design have to be taken into account. Detailed description on how to define the comparison window is explained in following section.

### 4.1.3. Decision Window and Application Limits

In multi-step A/D converters, high linearity is obtained by extensive use of correction and calibration procedures. Providing structural DfT and BIST capabilities to this kind of A/D converters is difficult since the effects of the correction mechanism must be taken into account. Overlap between the conversion ranges of two stages has to be considered, otherwise, there may exist conflicting operational situations that can either mask faults or give an incorrect fault interpretation. Although a multi-step A/D converter makes use of considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. The conversion process therefore is susceptible to analog circuit and device impairments. The primary error sources present in each stage in a multi-step $A / D$ converter are systematic decision stage offset errors $\lambda$, stage gain errors $\eta$, and errors in the internal reference voltages $\gamma$. The offset errors include offset caused by component mismatch, self-heating effects, comparator hysteresis or noise. The gain error group includes all the errors in the amplifying circuit, including technology variations and finite gain and offset of the operational amplifier. The reference voltage errors are caused by resistor ladder variations and noise, as well as to errors in the switch matrix, which are mainly due to charge injection in the transmission gate. The input-referred error $e_{i n}$ that is equivalent to the contributions of all the individual error sources can be expressed as
$e_{i n}=e_{1}+\sum_{i=1}^{k-1} \frac{e_{i+1}}{G^{i}} \quad$ with $\quad e_{i} \leq \frac{V_{F S}}{2^{N+1}} G^{i-1}$
which is the limit of the $A / D$ converter error arising from each error source to less than $1 / 2$ LSB , where $k$ is the number of the stages $i, V_{F S}$ is full scale input signal and $G$ is the gain of the stage. The decision stage offset moves the $\mathrm{A} / \mathrm{D}$ converter decision levels. If the correction range is not exceeded by the combination of all errors that shift the first-stage $A / D$ converter decision levels, the effect of the first-stage $A / D$ converter decision stage offset is eliminated by the digital correction, leaving the input-referred offset as the only effect of a sub-range offset. An offset on the residue amplifier gives a $d c$ shift of the next-stage $\mathrm{A} / \mathrm{D}$
converter reference with respect to the preceding stage A/D converter and sub-D/A converter range. The effect of coarse A/D converter offset is studied by examining plots of the ideal residue versus the input illustrated in Figure 4-6a); note that the fault provokes over-range and level shifting errors. Processing these data with the rest of the A/D converter, including the correction logic is shown in Figure 4-6b). Digital correction does not mask all errors, and hence the circuit is faulty: on the other hand, since the window comparator threshold has been exceeded the fault is also a detected fault.


Figure 4-6: a) Coarse ADC transfer characteristics in the presence of offset error, b) Faulty digitally corrected $A D C$ transfer characteristic
$\mathrm{D} / \mathrm{A}$ converter offset can be replaced by an input-referred stage offset and an offset in series with the coarse A/D converter as shown in Figure 4-7. The non-compensated remaining offset at the input of each A/D converter comparator due to the decision stage offset is given by $V_{o f \mid N C}^{D}=V_{o f f}^{D} / G^{i-1}$, where $V_{o f f \mid N C}{ }^{D}$ is the input referred non-compensated offset, $V_{o f f}^{D}$ is the decision stage offset, and $G^{i-1}$ is the gain of the preceding stage. Imposing a $\pm 1 / 2 \mathrm{LSB}$ maximum deviation leads to the definition of the comparison window:
$\Delta V=G^{i} V_{\text {off }}^{C} \Rightarrow-\frac{V_{F S}}{2^{N+1}} G^{i} G^{i-1} \leq \Delta V \leq \frac{V_{F S}}{2^{N+1}} G^{i} G^{i-1}$
where $G^{i}$ is the gain of the die-level process monitor circuit.


Figure 4-7: a) Block diagram of a first stage $A / D$ converter with offset error in $D / A$ converter, b) Equivalent diagram with rearranged offet errors

The gain requirements are straightforward. An error in per stage gain causes non-linearity in the transfer characteristic from input to output of the multi-step A/D converter. A gain error in the residue amplifier scales the total range of residue signal and causes an error in the analog input to the next stage when applied to any nonzero residue, which will result in residue signal not fitting in the fine $\mathrm{A} / \mathrm{D}$ converter range. If the error in the analog input to the next stage is more than one part in $2^{r}$ (where $r$ is the resolution remaining after the interstage gain error), it will result in a conversion error that is not removed by digital correction. Moreover, if the inter-stage gain is smaller than the ideal value, a fixed number of missing codes at every MSB transition can occur [55] (i.e., constant DNL errors or constant jumps in INL at every transition of the bits resolved by the first stage). Dual-residue signal processing [61] spreads the errors of the residue amplifiers over the whole fine range, which results in an improved linearity. An equivalent block diagram in which the $\mathrm{D} / \mathrm{A}$ converter gain error $\Delta_{i}$ has been replaced by three gain errors: one in series with the stage input, one in series with the coarse A/D converter, and one in series with the stage output is illustrated in Figure 4-8. If the correction range is not exceeded by the combination of all errors that shift the coarse A/D converter decision levels, the effect of the gain error in series with the coarse A/D converter is eliminated by the digital correction. The two remaining gain errors contribute inter-stage gain errors, which have the same effect on $\mathrm{A} / \mathrm{D}$ converter linearity as the residue amplifier gain errors.


Figure 4-8: a) Block diagram of a first stage of examined $A / D$ converter with gain error in $D A C$, b) Equivalent diagram with rearranged gain errors

An error in the range of the fine $A / D$ converter results in an error similar to a residue amplifier gain error. The gain of the sub-tractor and amplifier should therefore be lined with the fine $\mathrm{A} / \mathrm{D}$ converter range. To limit resulting nonlinearity to $\pm 1 / 2 \mathrm{LSB},\left|G \sigma_{i} V_{r s}\right| \leq$ $G X\left(V_{F S} / 2^{N+1}\right)$. The error in the residue amplifier is proportional to $G \times V_{n o s}$ thus, the effect of the gain error is largest when $G \times V_{r s}$ is maximum. The references of the $\mathrm{D} / \mathrm{A}$ converter and the subtraction of the input signal and the $\mathrm{D} / \mathrm{A}$ converter output determine the achievable accuracy of the total $\mathrm{A} / \mathrm{D}$ converter. The residue signal $V_{n s}$ is incorrect exactly by the amount of the $\mathrm{D} / \mathrm{A}$ converter nonlinearity
$V_{\text {res }}=G V_{\text {in }}-D A C_{\text {out }}-\delta_{l}$
where $D A C_{\text {out }}$ is the ideal output of the $\mathrm{D} / \mathrm{A}$ converter, $G$ is the gain and $\boldsymbol{\delta}_{t}$ is $\mathrm{D} / \mathrm{A}$ converter nonlinearity error. D/A converter errors result in each linear segment of the residue transfer curve being shifted up or down by different static random values. Hence, D/A converter
errors result in non-constant missing codes at every MSB transition. To limit resulting D/A converter nonlinearity to less than $1 / 2 \mathrm{LSB},\left|\delta_{l}\right|_{\text {minin }} \leq V_{F S} / 2^{\mathrm{N}+1}$. The comparison window for internal reference voltages deviations is, thus, given by:
$\left.\begin{array}{l}\Delta V_{\operatorname{lmax}}=V_{F S} \frac{\Delta R}{\sum_{j=1}^{N} R_{j}} \\ \Delta V=I_{r e f} \Delta R\end{array}\right\} \Rightarrow-\frac{I_{r e f} \sum_{j=1}^{N} R_{j}}{2^{N+1}} \leq \Delta V \leq \frac{I_{r e f} \sum_{j=1}^{N} R_{j}}{2^{N+1}}$
where $I_{r f}$ is the reference current in the resistor ladder die-level process monitor circuit, $V_{F S}$ is the full scale of the converter, $R_{j}$ is the value of each resistor in the resistor ladder, and $N$ is the total number of resistor in the ladder.

### 4.1.4. Die-Level Process Monitors Circuit Design

To illustrate the concept, consider only a simple four bit flash stage as shown in Figure 4-9, consisting of a reference ladder and sixteen comparators. From the previous analysis it can be concluded that the gain, decision and reference ladder are crucial to the proper converter performance. To mimic the device-under-test behavior, the gain-based and decision stagebased die-level process monitor are extracted (replicated) from the device-under-test as illustrated Figure 4-10 and Figure 4-11, where the stage gain-based and the decision stage-based die-level process monitor matches the actual flash converter comparator.

The type of latch employed is determined by the resolution of the stage. For a low-resolution quantization per stage, a dynamic latch is more customary since it dissipates less power than the static latch. While the latch circuits regenerate the difference signals, the large voltage variations on regeneration nodes will introduce the instantaneous large currents. Through the parasitic gate-source and gate-drain capacitances of the transistors, the instantaneous currents are coupled to the inputs of the comparators, making the disturbances unacceptable. In flash A/D converters where a large number of comparators are switched on or off at the same time, the summation of variations came from regeneration nodes may become unexpectedly large and directly results in false quantization code output [251]. It is for this reason that the static latch is preferable for higher-resolution implementations. The key requirement which determines the power dissipation during the comparison process is the accuracy, i.e. how accurately the comparator can make a decision in a given time period. As typical crosscoupled latch comparators exhibit a large offset voltage, several pre-amplifiers are placed before the regenerative latch to amplify the signal for accurate comparison. The power dissipation in the regenerative latch is relatively small compared to the preamp power, as only dynamic power is dissipated in the regenerative latch and low offset pre-amp stages usually require $d c$ bias currents. Therefore, the power dissipation is directly related to how many preamp stages are required, and the number of stages is determined by the required amplification factor before a reliable comparison can be made by the regenerative comparator. If high gain is required from a single stage preamp, the large value of the load resistor must be used, which in turn slows down the amplification process with an increased RC-constant at the output. In situations like this, the gain is distributed among several cascaded low gain stages to speed up the process. During this process care must also be taken to design a low noise pre-amp stage since its own circuit noise is amplified through its gain. For instance, if the input signal is held constant close to the comparator threshold, the thermal noise from both circuits and input sampling switches is also amplified through the preamp gain. The
preamp stage is usually implemented with a source-coupled pair, and its power-to-thermalnoise relationship is similar to that of the $\mathrm{S} / \mathrm{H}$ circuit case where the key block is the high gain op amp, except that the preamp is usually in the open-loop configuration. Also, $1 / f$ noise must be considered since it appears like a slowly varying offset of the comparator for high speed operation. Periodic offset cancellation at a rate much higher than the $1 / f$ noise corner frequency, usually every clock period, can reduce this effect. The analysis for noise is omitted here since it is relatively straightforward compared to that of the amplifier in the feedback as in $\mathrm{S} / \mathrm{H}$ circuits.


Figure 4-9: Flash $A / D$ converter with built-in sensors

Another major factor which affects the accuracy of the comparator is the offset voltage caused by the mismatches from process variations. This includes charge injection mismatches from input switches, threshold and transistor-dimensions mismatches between cross-coupled devices. To lessen the impact of mismatch, several schemes, such as inserting a preamplifier [1] in front of the latch, adding a chopper amplifier [2] and auto-zero scheme to sample an offset in the capacitor in front of the latch or digital background calibration [18] have been developed. In the auto-zero scheme, during the offset sampling period, the output of the first stage caused by its offset voltage is sampled on the sampling capacitor of the second stage. In the next clock phase, when the actual comparison is to be made, the stored voltage on the second stage sampling capacitor effectively cancels out the offset of the first amplifier, and a very accurate comparison can be made. For this cancellation technique, notice that the gain of the first stage must be chosen relatively low so that the output voltage due to its offset does not rail out of the range (or supply). One observation is that the offset voltage of the dynamic comparator circuit cannot be cancelled by this technique because the positive feedback amplifies even a small offset voltage to the supply rails and therefore no information on the offset voltage can be obtained at the output of the comparator. As a result, this technique
requires a preamp with a $d c$ bias current and therefore static power to reduce offset voltage. If an input signal is sampled on a capacitor before comparison, the capacitance value must be carefully chosen to reduce various non-idealities in addition to the $k T / C$ noise. In some multi-step A/D converters realizations, the comparator often has its own input sampling capacitor to eliminate the dedicated input $\mathrm{S} / \mathrm{H}$ circuit [62].

Figure 4-10 shows a sensor together with an auto-zeroing scheme to cancel a possible sensor offset. The switched-capacitor comparator operates on a two phase non-overlapping clock. The differencing network samples $V_{r g}$ during phase $c / k$ onto capacitor $C$, while the input is shorted giving differential zero. During phase clen, the input signal $V_{\text {in }}$ is applied at the inputs of both capacitors, causing an input differential voltage to appear at the input of the comparator preamp. At the end of clkn the regenerative flip-flop is latched to make the comparison and produce digital levels at the output. The charge injection from $T_{8}$ will cause an offset voltage $\Delta V=\Delta Q /\left(C+C_{p}\right)$. Requirement on the input bandwidth sets the magnitude of $\Delta V$, and the higher the sampling bandwidth is, larger the $\Delta V$. Circuit technique employed to limit charge injection include bottom plate sampling, use of dummy switch or reducing the gate channel length (Section 2.4). Another important consideration for choosing $C$ is the signal attenuation due to $C_{p}$. At the input of the amplifier, the input capacitance of the amplifier and the parasitic capacitance from the switch attenuate the input signal by $C /\left(C+C_{p}\right)$ and effectively reduces the amplification. Based on matching and common-mode charge injection errors, $C$ was chosen to be near minimum size, approximately $5 f F$.


Figure 4-10: Data decision with offset calibration: a) Preamplifier and offset calibration circuit and b) data decision stages

The comparison references needed to define the sensor decision windows are controlled through the $d c$ signals labeled refp and refn in the figure. The die-level process monitor measurements are directly related to asymmetries between the branches composing the circuit, giving an estimation of the offset when both DLPM inputs are grounded or set at predefined common-mode voltage. As shown in Figure 4-11a), the gain-based monitor consists of the circuitry replicated from the observed A/D converter gain stage, which consists of a differential input pair (transistors $T_{1}$ and $T_{2}$ ) with active loading $\left(T_{3}\right.$ and $\left.T_{4}\right)$ and some additional gain (transistors $T_{5}$ and $T_{6}$ ) to increase the monitor's resolution and transistors $T_{7}$ and $T_{8}$ to connect to read lines (lines leading to a programmable data decision circuit). The different device arrangements in the matrix include device orientation and the nested device environment. The matrix is placed several times on the chip to obtain information from different chip locations and distance behavior. Similarly, as shown in Figure 4-11b), in the decision stage monitor circuit the latch (transistors $T_{12}$ to $T_{17}$ ) has been broken to allow a dc current flow through the device needed for the intended set of measurements. In addition to these two,
internal reference voltages monitoring circuits as shown in Figure 4-12 sense the mismatch between two of the unit resistors used in the actual resistor ladder design. The current that flows through the resistors (whose values are extracted from the ladder itself) is fixed using a current mirror. Since the current is fixed, the voltage drop between the nodes labeled $V_{1}$ and $V_{2}$ is a measurement of the mismatch between the resistors. The feedback amplifier is realized by the common-source amplifier consisting of $T_{5}$ and its current source $I_{5}$. The amplifier keeps the drain-source voltage across $T_{3}$ as stable as possible, irrespective of the output voltage. The addition of this amplifier ideal increases the output impedance by a factor equal to one plus the loop gain over that which would occur for a classical cascode current mirror. Assuming the output impedance of current source $I_{5}$ is roughly equal to $r_{d s 5}$ the loop gain can be approximated by $\left(g_{m s} r_{d 5 s}\right) / 2$. The circuit consisting of $T_{7}, T_{9}, T_{11}, I_{1}$ and $I_{2}$ operates almost identically to a diode-connected transistor; however it is employed instead to guarantee that all transistor bias voltages are accurately matched to those of the output circuitry consisting of $T_{1}, T_{3}, T_{5}$ and $I_{5}$. As a consequence $I_{\mathrm{R} 1}$ will very accurately match $I_{1}$ [252].


Figure 4-11: Die-level process monitors, a) Stage gain-based and b) Decision stage-based

As transistors $T_{3}$ and $T_{9}$ are biased to have drain-source voltages ( $\left.V_{D S 3}=V_{D S 9}=V_{4 f 5}+V_{T}\right)$ larger than the minimum required, $V_{e f f 3}$, this can pose a limitation in very low power supply technologies. An alternative realization [253], illustrated in Figure 4-12b) combines the wideswing current mirror with the enhanced output-impedance circuit. Here, diode-connected transistors used as level shifters have been added in front of the common-source enhancement amplifier. At the output side, the level shifter is the diode-connected transistor $T_{7}$, biased with current $I_{2}$. The circuitry at the input acts as diode-connected transistor while ensuring that all bias voltages are matched to the output circuitry to the $I_{\mathrm{R} 1}$ accurately matches $I_{1}$. In the case in which $I_{7}=I_{1} / 7$ all transistors are biased with nearly the same current density, except $T_{7}$ and $T_{g}$. As a result, all transistors have the same effective gate-source voltages, except for $T_{7}$ and $T_{9}$, which have twice effective gate-source voltage as they are biased the four times the current density. Thus, the gate voltage of $T_{9}$ equals $V_{G 9}=2 V_{e f f}+V_{T}$ and the drain-source voltage $T_{3}$ is given by $V_{D S 3}=V_{G 9}-V_{G S 12}=V_{e f f}$. Therefore, $T_{3}$ is biased on the edge of the triode region. Although the power dissipation of the circuit is almost doubled over that of a classical cascode current mirror, by biasing the enhancement circuitry at lower densities, albeit at the expense of speed, e.g. additional poles introduced by the enhancement circuitry are at lower frequencies, sufficient power dissipation savings can be made.

Thus, three generalized strategies can be extracted from the presented die-level process monitor circuits: gain stage-, decision stage- and resistor ladder-DLPMs. Gain stages, such as the residue amplifiers in the A/D converter, can be tested using the same strategy developed for testing the preamplifier in the A/D converter. The proposed methodology can be di-
rectly translated to any gain stage, allowing the detection of mismatch issues through the measurement of output offset. Decision stages in the A/D converter can be tested via adapting the proposed decision stage die-level process monitor strategy to each particular design. This strategy is based on breaking the regeneration feedback in the latch, and then sensing process mismatches through the measurement of output offset.


Figure 4-12: Internal reference voltages-based DLPM with, a) Enhanced output impedance current mirror b) Modified wide-swing current mirror with enhanced output impedance

Internal reference voltages can be tested by adapting the same scheme proposed for the resistor ladder DLPM, which gives a measurement of resistor mismatch through the measurement of a voltage drop. To increase the monitor resolution, some additional gain can be inserted into the DLPMs between the input differential pair and the loading. By sweeping the reference voltage until a change in the decision occurs, information about the process variation can be extracted as shown in Figure 4-13a).


Figure 4-13: a) Sweeping the reference voltages to extract the DLPMs offset voltage values, illustrated on the decision DLPM, b) Testing the device-under-test by setting the discrimination window to $1 / 2 L S B$ level and sweeping the process parameters values

Similarly, by setting the discrimination window to $1 / 2$ LSB level, variations due to the mismatch can be detected (Figure 4-13b). A discrimination window for various die-level process monitors has been defined according the rules of the multi-step A/D converter error model from Section 4.1.3. By extracting the die-level process monitor circuit from the device-under-test itself, the monitoring circuit accomplishes some desirable properties: $i$ ) it is designed to maximize the sensitivity of the circuit to the target parameter to be measured, $i i$ it matches the physical layout of the extracted device under test, and iii) it is small and stand alone, and consumes no power while in off state.

### 4.1.5. Temperature Sensor

To convert temperature to a digital value, both a well-defined temperature-dependent signal and a temperature-independent reference signal are required. Both can be derived utilizing exponential characteristics of bipolar devices for both negative- and positive temperature coefficient quantities in the form of the thermal voltage and the silicon bandgap voltage. For constant collector current, base-emitter voltage has negative temperature dependence around room temperature. This negative temperature dependence is cancelled by a proportional-toabsolute temperature (PTAT) dependence of the amplified difference of two base-emitter junctions biased at fixed but at unequal current densities resulting in the relation directly proportional to the absolute temperature. This proportionality is quite accurate and holds even when the collector currents are temperature dependent, as long as their ratio remains fixed. In a $n$-well CMOS process, both lateral $n p n$ and $p n p$ transistors and vertical or substrate $p n p$ transistors are used for this purpose. As the lateral transistors have low current gains and their exponential current voltage characteristic is limited to a narrow range of currents, the substrate transistors are preferred. In the vertical bipolar transistors, a $p^{+}$region inside an $n$ well serves as the emitter and the $n$-well itself as the base of the bipolar transistors. The $p$ type substrate acts as the collector and as a consequence, all their collectors are connected together, implying that they can not be employed in a circuit unless the collector is connected to the ground. These transistors have reasonable current gains and high output resistance, but their main limitation is the series base resistance, which can be high due to the large lateral dimensions between the base contact and the effective emitter region. To minimize errors due to this base resistance, the maximum collector currents through the transistors are constrained to be less than 0.1 mA .


Figure 4-14: a) Typical implementation of bandgap reference circuit, b) Temperature sensor - conceptual view
The slope of the base-emitter voltage depends on process parameters and the absolute value of the collector current. Its extrapolated value at 0 K , however, is insensitive to process spread and current level. The base-emitter voltage is also sensitive to stress. Fortunately, substrate $p m p$ transistors are much less stress-sensitive than other bipolar transistors [254]. In contrast with the base-emitter voltage $V_{b o} \Delta V_{b c}$ is independent of process parameters and the absolute value of the collector currents. Often a multiplicative factor is included in the equation for $\Delta V_{b e}$ to model the influence of the reverse Early effect and other nonidealities [255]. If $V_{b c}$ and $\Delta V_{b c}$ are generated using transistors biased at approximately the same current density, an equal multiplicative factor will appear in the base-emitter voltage. $\Delta V_{b e}$ is insensitive to stress [256]. Its temperature coefficient is, however, typically an order of magnitude smaller than that of (depending on the collector current ratio).

The nominally zero temperature coefficient is usually exploited in a temperature-independent reference generation circuits such as bandgap-reference illustrated in Figure 4-14a). In general, accurate measure of the on-chip temperature is acquired or through generated proportional-to-absolute temperature current or the generated proportional-to-absolute temperature voltage. In the previous case, the reference voltage is converted into current by utilizing an opamp and a resistor. The absolute accuracy of the output current will depend on both the absolute accuracies of the voltage reference and of the resistor. Most of the uncertainty will depend on this resistor and its temperature coefficient. In a bandgap voltage reference, an amplified version of $\Delta V_{b e}$ is added to $V_{b e}$ to yield a temperature-independent reference voltage $V_{r g}$. The negative voltage-temperature gradient of the base-emitter junction of the transistor $Q_{1}$ is compensated by a proportional-to-absolute temperature voltage across the resistor $R_{l}$, thereby creating an almost constant reference voltage $V_{r f}$ [257]. The amplifier $A$ senses voltages at its inputs, driving the top terminals of $R_{1}$ and $R_{2}\left(R_{1}=R_{2}\right)$ such that these voltages settle to approximately equal voltages. The reference voltage is obtained at the output of the amplifier (rather than at its input). Due to the asymmetries, the inaccuracy of the circuit is mainly determined by the offset of the opamp, which directly adds to $\Delta V_{b c}$. To lower the effect of offset, the opamp incorporates large devices. Similarly, the collector currents of bipolar transistors $Q_{1}$ and $Q_{2}$ are rationed by a pre-defined factor, e.g. transistors are multiple parallel connections of unit devices.

The conceptual view of the temperature sensor is illustrated in Figure 4-14b). The left half of this circuit is the temperature sense-circuit, which is similar to a conventional bandgap reference circuit. The right part, comprising a voltage comparator, creates the output signal of the temperature switch. To enable a certain temperature detection, two signals are required, both with a well defined but different temperature dependence; an increasing proportional-toabsolute temperature voltage across the resistor network $N_{T} R$ and decreasing voltage at the comparator positive input generates temperature decisions. As the bias currents of the bipolar transistors are in fact proportional to absolute temperature, proportional-to-absolute temperature current $I_{D 3}$ can be generated by a topology comprising bipolar transistors $Q_{1}$ and $Q_{2}$, resistor $R$, an amplifier and CMOS transistors $T_{1}-T_{3}$.

The temperature sensor as shown in Figure 4-15 is based on a modified temperature sensor [258]. The amplifier consists of a non-cascoded OTA with positive feedback to increase the loop-gain. The amplifier output voltage is relatively independent of the supply voltage so long as its open-loop gain is sufficiently high. If input voltages are equal to zero, the input differential pair of the amplifier may turn off. To prevent this, a start-up circuit consisting of transistors $T_{5}-T_{6}$ is added, which drives the circuit out of the degenerate bias point when the supply is tuned on. The diode-connected device $T_{5}$ provides a current path from the supply through $T_{6}$ to ground upon start-up. The scan chain delivers a four-bit value for the setting of the resistor value $N_{T} R$. The input of the comparator consists of a differential sourcecoupled stage, followed by two amplifying stages and one digital inverter.

To provide stable bandgap reference voltage < 1V as illustrated in Figure 4-16a), zerotemperature coefficient voltage $\approx 1.2 \mathrm{~V}$ is firstly converted into current through transistor $T_{22}$ and then summed up to lower reference voltage through $R_{2}$ and $N_{R} R$. The opamp has sufficient gain to equalize its input voltages. Since these nodes are the same, the currents from these nodes to ground must be the same as well. The current through $R_{1}$ is therefore propor-tional-to-absolute temperature. This current is also flowing through the output transistor $T_{22}$. The curvature of $V_{b e}$ will also be present in the reference voltage. For a current, which is
independent of temperature, the curvature correction is in the same order of magnitude of mismatch. By allowing a proportional-to-absolute temperature current to have a small positive temperature coefficient, the second-order component of the curvature is eliminated. Such a temperature-dependent reference voltage cancels the second-order nonlinearity originating from $V_{b c}$. For this purpose, a transistor $Q_{3}$ is added. In essence, a term based on the ratio of the resistors $N_{R} R$ and $R_{2}$ is generated which subtracts the $V_{b e}$ of a junction with a constant current for the $V_{b e}$ of a junction with the proportional-to-absolute temperature current. To accurately define this ratio, all resistors are constructed of identical unit resistors. The voltage across $R_{2}$ is curvature-compensated by adjusting the base-emitter voltage $V_{b e}$ of a substrate $p n p$ transistor with adjustable resistors $N_{R} R$. The proportional-to-absolute temperature voltage across this resistor compensates for the proportional-to-absolute temperaturetype spread on $V_{b e}$ of a transistor $Q_{3}$.


Figure 4-15: Temperature sensor - schematic view

In the test silicon, four bits for a sixteen selection levels are chosen for the temperature settings, resulting in a temperature range from $0-150^{\circ} \mathrm{C}$ with a resolution of $9^{\circ} \mathrm{C}$ as illustrated in Figure 4-16b). If a higher accuracy is required, a selection D/A converter with higher resolution is necessary. For the robustness, the circuit is completely balanced and matched both in the layout and in the bias conditions of devices, cancelling all disturbances and non-idealities to the first order.


Figure 4-16: a) Bandgap reference voltage; nominal, fast-fast and slow-slow process corners, b) Sixteen selection levels in the temperature sensor

### 4.2. Estimation of Die-Level Process Variations

### 4.2.1. Expectation-Maximization (EM) Algorithm

In general, a circuit design is optimized for parametric yield so that the majority of manufactured circuits meet the performance specifications. The complexity of yield estimation, coupled with the iterative nature of the design process, makes yield maximization computationally prohibitive. As a result, circuit designs are verified using models corresponding to a set of worst-case conditions of the process parameters. Worst-case analysis is very efficient in terms of designer effort, and thus has become the most widely practiced technique for statistical verification. However, the worst-case performance values obtained are extremely pessimistic and as a result lead to unnecessary large and power hungry designs in order to reach the desired specifications. Thus, it would be advantageous to choose a more relaxed design condition. Statistical data extracted through the sensor measurements allow not only possibilities to enhance observation of important design and technology parameters, but to characterize current process variability conditions (process corners) of certain parameters of interest, enabling optimized design environment as well. As the number of on-chip sensors is finite due to area limitations, additional informations are obtained through statistical techniques. Although, in statistics several methods, such as listwise [259] and pairwise [260] deletion and structural equation modelling [261] would provide estimates of the selected performance figures from the incomplete data, imputation method (e.g. substitution of some plausible value for a missing datapoint) and its special case, multiple imputations based on expectation-maximization (EM) algorithm [262-263] offers maximum likelihood estimates. The work in this section [264] utilizes therefore the EM method and adjusted support vector machine (SVM) classifier [265-266] as a very efficient method for test guidance based on the information obtained through monitoring process variations, since it simultaneously minimizes the empirical classification error and maximizes the geometric margin. Given the observation vector of the sensor's observations $x_{i} \in X$, the estimation of an unknown parameter vector $\theta \in \Theta$ designating true values of die-level process parameter variation would be an easy task if the missing data vector $y_{i} \in Y$, assumed to be realizations of the random variables which are independent and identically distributed according to the probability $p_{X Y \mid} \Theta(x, y \mid \theta)$, were also available. The maximum likelihood (ML) estimation involves estimation of $\theta$ for which the observed data is the most likely, e.g. marginal probability $p_{X \mid \Theta}(x \mid \theta)$ is a maximum. The parameters $\theta$ involve parameters $\left(\mu_{y}, \Sigma_{y j}\right), y \in Y$ of Gaussian components and the values of the discrete distribution $p_{Y \mid \Theta}(y \mid \theta), y \in Y$. The $p_{X \mid \Theta}(x \mid \theta)$ is the Gaussian mixture model given by the weighted sum of the Gaussian distributions. The logarithm of the probability $p\left(T_{X} \mid \theta\right)$ is referred to as the $\log$-likehood $L\left(\theta \mid T_{X}\right)$ of $\theta$ with respect to $T_{X}$. The input set $T_{X}$ is given by $T_{X}=\left\{\left(x_{i}, \ldots, x_{X}\right)\right\}$, which contains only vectors of sensors's observations $x_{i}$ The log-likelihood can be factorized as
$L\left(\theta \mid T_{X}\right)=\log p\left(T_{X} \mid \theta\right)=\sum_{i=1}^{l} \sum_{y \in Y} p_{X \mid \ominus \theta}\left(x_{i} \mid y_{i}, \theta\right) p_{Y \mid \Theta}\left(y_{i} \mid \theta\right)$
The problem of maximum likelihood estimation from the set of sensor's observations $T_{X}$ can be defined as

$$
\begin{equation*}
\theta^{*}=\max _{\theta \in \Theta} L\left(\theta \mid T_{X}\right)=\max _{\theta \in \Theta} \sum_{i=1}^{1} \sum_{y \in Y} p_{X| | \Theta}\left(x_{i} \mid y_{i}, \theta\right) p_{Y \mid \Theta}\left(y_{i} \mid \theta\right) \tag{4-8}
\end{equation*}
$$

Obtaining optimum estimates through the ML method involves two steps: computing the likelihood function and maximization over the set of all admissible sequences. To evaluate the contribution of the random parameter $\theta$, analysis of the likelihood function requires computing an expectation over the joint statistics of the random parameter vector, a task that is analytically intractable. Even if the likelihood function can be obtained analytically off line, it is invariably a nonlinear function of $\theta$, which makes the maximization step (which must be performed in real time) computationally infeasible. In such cases, the expectationmaximization algorithm [262-263,267-270] may provide a solution, albeit iterative, to the ML estimation problem. Instead of using the traditional incomplete-data density in the estimation process, the EM algorithm uses the properties of the complete-data density. In doing so, it can often make the estimation problem more tractable and also yield good estimates of the parameters for small sample sizes [267]. Thus, with regard to implementation, the EM algorithm holds a significant advantage over traditional steepest-descent methods acting on the incomplete-data likelihood equation. Moreover, the EM algorithm provides the values of the log-likelihood function corresponding to the maximum likelihood estimates based uniquely on the observed data. The EM algorithm builds a sequence of parameter estimates $\theta^{(0)}, \theta^{(1)}, \ldots, \theta^{(t)}$, such that the log-likelihood $L\left(\theta^{(t)} \mid T_{X}\right)$ monotonically increases, i.e., $L\left(\theta^{(0)} \mid T_{X}\right)<L\left(\theta^{(1)} \mid T_{X}\right)<\ldots<L\left(\theta^{(\theta)} \mid T_{X}\right)$ until a stationary point $L\left(\theta^{(1-1)} \mid T_{X}\right)=L\left(\theta^{(\theta)} \mid T_{X}\right)$ is achieved. In each iteration, two steps, called E-step and M-step, are involved. In the E-step, the EM algorithm forms the auxiliary function $Q\left(\theta \mid \theta^{(t)}\right.$, which determines the expectation of log-likelihood of the complete data based on the incomplete data and the current parameter

$$
\begin{equation*}
Q\left(\theta \mid \theta^{(t)}\right)=E(\log p(X, Y \mid \theta) \mid X, \theta(t)) \tag{4-9}
\end{equation*}
$$

In the M-step, the algorithm determines a new parameter maximizing $Q$

$$
\begin{equation*}
\theta^{(t+1)}=\max _{\theta} Q\left(\theta \mid \theta^{(t)}\right) \tag{4-10}
\end{equation*}
$$

At each step of the EM iteration, the likelihood function can be shown to be non-decreasing [270]; if it is also bounded (which is mostly the case in practice), then the algorithm converges. In [262] is proved that an iterative maximization of $Q\left(\theta \mid \theta^{(t)}\right)$ will lead to a maximum likelihood estimation of $\theta$. For a broad class of probability density functions, including Gaussian mixture densities, at each iteration the new parameter estimate $\theta$ can be explicitly solved as the stationary point corresponding to the unique maximum of $Q\left(\theta \mid \theta^{(t)}\right)$ [267]. As in direct maximum likelihood estimation, the EM algorithm only leads to locally optimal estimates of model parameters, with each resulting estimate depending upon the initial parameters chosen to start the iterative estimation.

## EM Algorithm

## Initialization

- Initialize the data set $T x=\left\{\left(x_{l}, \ldots, x_{l}\right)\right\}$
- Initialize the parameter $\theta^{(0)}$

Data collection

- Collect $N$ samples from the DLPMs

Update parameter estimate

1. Calculate $Q\left(\theta \mid \theta^{(t)}\right)=E\left(\log p(X, Y \mid \theta) \mid X, \theta^{(t)}\right) \quad$ - E step (4-9)
2. Re-estimate $\theta$ by maximizing the $\theta$-function $\theta^{(t+1)}=\max _{\theta} Q\left(\theta \mid \theta^{(t)}\right)$, estimate mean and variance $\quad-\mathrm{M}$ step (4-10)
3. Increase the iteration index, $t$
4. Stop when a stationary point $L\left(\theta^{(t-1)} \mid T_{X}\right)=L\left(\theta^{(t)} \mid T_{X}\right)$ is found

### 4.2.2. Support Vector Machine Limits Estimator

When an optimum estimate of the parameter distribution is obtained as described in Section 4.2.1, the next step is to update the test limit values utilizing the adjusted support vector machine classifier. Assuming that the input vectors (e.g. values defining test limits) belong to a priori (nominal values) and a posteriori (values estimated with EM algorithm) classes, the goal is to set test limits, which reflect observed on-chip variation. Each new measurement is viewed as an $r$-dimensional vector (a list of $r$ numbers) and the SVM classifier maps (separates) the input vectors into $r-1$-dimensional hyperplane in space $Z$ where a linear decision surface is constructed through non-linear mapping. Although several classifiers are available, such as quadratic, boosting, neural networks, Bayesian networks, adjusted support vector machine (SVM) classifier is especially resourceful, since it simultaneously minimize the empirical classification error and maximize the geometric margin.

Let $D=\left\{\left(x_{i}, c_{i}\right) \mid x_{i} \in R^{r}, c_{i} \in\{-1,1\}\right\}^{n}{ }_{i=1}$ be the input vectors belonging to a priori and a posteriori classes. Similarly, let

$$
\begin{equation*}
w \cdot x+b=0 \tag{4-11}
\end{equation*}
$$

be the optimal hyperplane in feature space. The vector $w$ is a normal vector perpendicular to the hyperplane. The parameter $b /||w||$ determines offset of the hyperplane from the origin along the normal vector $w$. To maximize the margin, $w$ and $b$ are chosen as such that they minimize nearest integer $||w||$ subject to the optimization problem described by

$$
\begin{equation*}
c_{i}\left(w \cdot x_{i}+b\right) \geq 1 \tag{4-12}
\end{equation*}
$$

for all $1 \leq i \leq n$. The optimization problem is difficult to solve because it depends on $\|w\|$, which involves a square root. If the input vectors belonging to a priori and a posteriori classes cannot be separated by a hyperplane, the margin between patterns of the two classes becomes arbitrary small, resulting in the value of the functional vector of parameters turning arbitrary large. To solve the posed optimization problem, it is proposed in this section to utilize standard quadratic programming optimization [265]. The equation is altered by substituting $\|w\|$ with $1 / 2| | w| |^{2}$ without changing the solution (the minimum of the original and the modified equation have the same $w$ and $b$ ). The input vectors belonging to a priori and a posteriori classes are divided into a number of sub-sets. The quadratic programming problem is solved incrementally, covering all the sub-sets of classes constructing the optimal separating hyperplane for the full data set. Note that during this process the value of the functional vector of parameters is monotonically increasing, since more and more training vectors are considered in the optimization leading to a smaller and smaller separation between the two classes. Writing the classification rule in its unconstrained dual form reveals that the maximum margin hyperplane and therefore the classification task is now only a function of the support vectors, e.g. the training data that lie on the margin

$$
\begin{equation*}
\max \sum_{i=1}^{n} \alpha_{i}-\frac{1}{2} \sum_{i, j} \alpha_{i} \alpha_{j} c_{i} c_{j} x_{i}^{T} x_{j} \tag{4-1-1}
\end{equation*}
$$

subject to $\alpha_{i} \geq 0$ and $\sum_{i=1}^{n} \alpha_{i} c_{i}=0$,
$w=\sum_{i} \alpha_{i} c_{i} x_{i}$
where the $\alpha$ terms constitute the weight vector in terms of the training set. Additionally, to allow for mislabelled examples a modified maximum margin technique [265] is employed. If there exists no hyperplane that can divide the a priori and a posteriori classes, the modified maximum margin technique finds a hyperplane that separates the training set with a minimal number of errors. The method introduces non-negative variables, $\xi_{;}$, which measure the degree of misclassification of the data $x_{i}$
$c_{i}\left(w \cdot x_{i}+b\right) \geq 1-\xi_{i}$
for all $1 \leq i \leq n$. The objective function is then increased by a function which penalizes non-zero $\xi_{;}$, and the optimization becomes a trade off between a large margin, and a small error penalty. For the linear penalty function, the optimization problem now transforms to

$$
\begin{equation*}
\min \frac{1}{2}\|w\|^{2}+C \sum_{i} \xi_{i}^{\sigma} \tag{4-16}
\end{equation*}
$$

such that (4-12) holds for all $1 \leq i \leq n$. For sufficiently large constant $C$ and sufficiently small $\sigma$, the vector $w$ and constant $b$ that minimize the functional (4-16) under constraints in (4-12), determine the hyperplane that minimizes the number of errors on the training set and separate the rest of the elements with maximal margin. This constraint in (4-12) along with the objective of minimizing $\|w\|$ can be solved using Lagrange multipliers. The key advantage of a linear penalty function is that the variables $\xi_{i}$ vanish from the dual problem, with the constant $C$ appearing only as an additional constraint on the Lagrange multipliers. Similarly, non-linear penalty functions can be employed, particularly to reduce the effect of outliers on the classifier; however, the problem can become non-convex and thus, finding a global solution can become considerably more difficult task.

In general, the discriminant function of an arbitrary classifier does not have a meaning of probability e.g. support vector machine classifier. However, the probabilistic output of the classifier can help in post-processing, for instance in combining more classifiers together. Fitting a sigmoid function to the classifier output is a one way to solve this problem. Let $T_{X Y}$ $=\left\{\left(x_{1}, y_{1}\right), \ldots,\left(x_{b} y_{i}\right)\right\}$ is the training set composed of the vectors $x_{i} \in X$ and the corresponding $y_{i} \in Y$. It is assumed that the training set $T_{X Y}$ to be identically and independently distributed from underlying distribution. Let $f: X \subseteq \mathrm{R}^{n} \rightarrow \mathrm{R}$ be a discriminant function trained from the data $T_{X Y}$. The parameters $\theta$ of a posteriori distribution $p_{Y| |^{\Theta} \Theta}(y \mid f(x), \theta)$ of $y$ given the value of the discriminant function $f(x)$ are estimated by the maximum-likelihood method
$\theta=\max _{\theta^{\prime}} \sum_{i=1}^{l} \log p_{Y \mid F \Theta}\left(y_{i}\left|f\left(x_{i}\right)\right| \theta^{\prime}\right)$
where the distribution $p_{Y \mid F^{\Theta}}(y \mid f(x), \theta)$ is modeled by a sigmoid function determined by parameters $\theta$.

### 4.3. Debugging of Multi-Step A/D Converter Stages

### 4.3.1. Quality Criterion

Before proceeding with debugging of an A/D converter stages, firstly a measure of error, e.g. an estimator of the loss function, is introduced. In other words, a mechanism is necessary to distinguish, whether the A/D converter performance is acceptable or not. A quality criterion is generally speaking a function that given the input and output to a system calculates the deviation inflicted by the system. The quality criterion usually adopted for an estimator of the loss function is the mean-squared error (MSE) criterion, mainly because it represents the energy in the error signal, is easy to differentiate and provides the possibilities to assign the weights.

Besides timing errors, the primary error sources present in a multi-step A/D converter are systematic decision stage offset errors $\lambda$, stage gain errors $\eta$, and errors in the internal reference voltages $\gamma$. To find a parameter vector $W^{T}=[\eta, \gamma, \lambda]$ that gives the best-fit line, the leastsquares method attempts to locate a function which closely approximate the transition points by minimizing the sum of the squares of the ordinate differences (called residuals) between points generated by the function and the corresponding points in the data. Suppose that $D_{\text {out }, i}$ represents the output code which results from an input voltage of $V_{i}, f\left(V_{i}\right)=a V_{i}+b$. If the sum of the squares of the residuals, $\Gamma_{\text {MSE }}(W)$
$\Gamma_{\text {MSE }}(W)=\sum_{i=0}^{2^{n}-1}\left(D_{\text {out }, i}-f\left(V_{i}, W\right)\right)^{2}$
is minimized, then the function $f\left(V_{i}\right)$ has the property that $f\left(V_{i}\right) \approx D_{\text {out }, i} f\left(V_{i}\right)$ is the best-fit line, whose slope is given by $a$, and the point which the line intercepts the y -axis in given by the $b$. The design of A/D converter incorporates both defining the quantization regions $f\left(V_{i}\right)$ and assigning suitable values to represent each level with the reconstruction points. In most cases the $D_{\text {out }, i}$ is a function of the input $f\left(V_{i}\right)$, so that the expected value is taken with respect to $f\left(V_{j}\right)$ only. Optimal reconstruction points for minimizing the mean-square error have been derived in [271]. The estimation values dependent not only on the characteristics of the A/D converter under test, but also on the test signal itself (through the PDF of the signal). It is therefore of vital importance that the estimation routine is carefully designed as it can yield an estimation system that is heavily biased towards a specific signal, since the estimation values were trained using that signal type. On the other hand, if prior knowledge says that the A/D converter will be used to convert signals of a specific class, it is straightforward to evaluate the system using the same class of signals. Using estimation signals with a uniform PDF can be considered to lead to unbiased calibration results. In this case, both meansquared and midpoint strategy, coincide. Although, there are many specific measures for describing the performance of an $\mathrm{A} / \mathrm{D}$ converter - signal-to-noise-and-distortion ratio, spurious-free dynamic range, effective number of bits, total harmonic distortion, ... to mention a few, which assess the precision and quality of A/D converters, most of the specialized measures result in fairly complicated expressions that do not provide results of practical use. Exceptions are signal-to-noise-and-distortion ratio and effective number of bits which are both closely related to the mean-squared error criterion; therefore, most results expressed as mean-squared error can be transferred to results on signal-to-noise-and-distortion ratio and effective number of bits as shown in Appendix B.

### 4.3.2. Estimation Method

Even though extensive research [274-277] has been done to estimate the various errors in different A/D converter architectures, the use of DfT and dedicated sensors for the analysis of multi-step ADCs to update parameter estimates has been negligible. The influence of the architecture on analog-to-digital converter modeling is investigated in [274], and in [275] with use of some additional sensor circuitry, pipeline A/D converter are evaluated in terms of their response to substrate noises globally existing in a chip. In [276], the differential nonlinearity test data is employed for fault location and identification of the analog components in the flash converter and in [277] is shown how a given calibration data set may be used to extract estimates of specific error performance. Functional fault in each of the analog component in the multi-step ADC affects the transfer function differently [249] and analyzing this property form the basis of approach described in this section [278]. The A/D converter is here seen as a static function that maps the analog input signal to a digital output signal. The static parameters are determined by the analog errors in various A/D converter components and therefore, a major challenge in $\mathrm{A} / \mathrm{D}$ converter test and debugging is to estimate the contribution of those individual errors to the overall $\mathrm{A} / \mathrm{D}$ converter linearity parameters. The A/D converter characteristics may also change when it is used, e.g., due to temperature change. This means that the A/D converter has to be reevaluated at regular intervals through temperature sensors to examine its performance. Each stage of the A/D converter under test is evaluated experimentally, i.e., a signal is fed to the input of each stage of the A/D converter and the transfer characteristics of each stage of the A/D converter are determined from the outcome. Most of the evaluation methods require that a reference signal is available in the digital domain, this being the signal that the actual stage output of the A/D converter is compared with. This reference signal is in the ideal case a perfect, infinite resolution, sampled version of the signal applied to the A/D converter under test. In a practical situation, the reference signal must be estimated in some way. This can be accomplished by incorporating auxiliary devices such as a reference $A / D$ converter, sampling the same signal as the $A / D$ converter under test [279], or a D/A converter feeding a digitally generated signal to the A/D converter under test [273,280]. Another alternative is to estimate the reference signal by applying signal processing methods to the output of the $A / D$ converter under test. Special case of this exists; in [281], sinewave reference signals in conjunction with optimal filtering techniques extract an estimate of the reference signal. Some of the methods do not rely on any digital reference signal. In [279], a method is proposed that estimates the integral nonlinearity (INL) from the output code histogram. In [281], a hybrid system utilizing the minimum mean-squared approach followed by a lowpass filter is proposed. The filtering is possible since the system is aimed at over-sampling applications, so that the signal of interest only can reside in the lower part of the spectrum. The method is aided with the sinewave histogram method and Bayesian estimation.

The overall examined multi-step A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers. In $m+n$ multi-step A/D converter the $m$ most significant bits are found from the first resistance ladder and the $n$ least significant bits are generated from the second resistance ladder. Usually, the full range of the second resistance ladder is longer than one step in the first ladder, as explained in Section 2.3. With this over-range compensation in the second ladder, the static errors can be corrected since the signal still lies in the range of the second ladder. This means that the output of the ADC is redundant and it is not possible, from the digital output, to find the values from each subranging step without employing dedicated DfT.

Since the separate cores of A/D converter have to be verified, it is necessary to fix the circuit during testing in such a way that all cores are tested for their full input range. In the analog part, there are seven scan chains of which three need special attention. To set the inputs of the separate cores at the wanted values, a scan-chain in the switch-ladder circuit is proposed [282]. So, for mid-range A/D converter measurements, it is necessary to fix the coarse A/D converter values since they determine mid-range $\mathrm{A} / \mathrm{D}$ converter references, and for evaluation of the fine A/D converter both coarse and mid A/D converters decisions have to be predetermined. The response of the individual cores is then routed to the test bus. The subD/A converter settings are controlled by serial shift of data through a scan chain that connects all sub-D/A converter registers in serial as shown in Figure 4-17. In order to create extra margin in the timing, signals are shifted half a period, which translates as running on a negative clock in application mode. To avoid the problems, which can arise by integrating this chain in a much longer chain in the larger system, the polarity of the clock control signal cleswld can be switched at will. This is implemented through the bold_clk_fine signal, which is in fact a clk_fine_off signal (results in a ' 0 ' signal) as shown in Figure 4-17b). Note that cleswld cannot be set off in the clock block. In the clock gates is an override by the scan-enable signal present, making it possible to shift new values in or through the chain, without the need for reprogramming the test control block even if the fix signal has been set accidentally. The needed inversion for application mode is done locally in the switch ladder logic followed by a local clock-tree, needed for the 128 flip-flops and one anti-skew element. It is possible to freeze the contents of the sub-D/A converter registers in normal mode and shift out the data via the scan chain to capture the current sub-D/A converter settings. A test control bit is required per sub-D/A converter to adjust (increase) the reference current to obtain an optimal fit of the sub-D/A converter output range to the A/D converter input range.

The references of the sub-D/A converter and the subtraction of the input signal and the subD/A converter output determine the achievable accuracy of the total A/D converter. The residue signal $V_{r s}$ is incorrect exactly by the amount of the sub-D/A converter nonlinearity caused by errors in the internal reference voltages $\gamma$

$$
\begin{equation*}
V_{r e s}=\eta V_{i n}-(s-1) \gamma V_{\text {ref }}-\lambda V_{\text {offset }} \tag{4-19}
\end{equation*}
$$

where $s$ is the observed stage. To obtain a digital representation of (4-19) each term is divided with $V_{r g}$

$$
\begin{equation*}
D_{\text {out }}=\eta D_{\text {in }}-(s-1) \gamma-\lambda D_{\text {os }} \tag{4-20}
\end{equation*}
$$

where $D_{o u t t}=V_{r e s} / V_{r p} D_{i n}=V_{i n} / V_{r p p}$ and $D_{o s}=V_{\text {ofiste }} / V_{r p}$. By denoting the $k^{t h t}$ stage ( $k=1, \ldots, 3$ for the observed converter) input voltage as $D_{i, k}=V_{i n, k} / V_{r e}$, the $k_{k}^{t, h}$ stage output voltage as $D_{\text {out }}=V_{r s, k} / V_{r e p}$ and the $k_{k}^{t h}$ stage decision $D_{k}$, a recursive relationship when (4-20) is applied to each stage in sequence becomes

$$
\begin{align*}
& D_{\text {out }}=D_{\text {out }, 3}=\left\{[\ldots] \eta_{2}-\left(D_{2}-1\right) \gamma_{2}-\lambda_{2} D_{\text {os }, 2}\right\} \eta_{3} \\
&-\left(D_{3}-1\right) \gamma_{3}-\lambda_{3} D_{o s, 3}=  \tag{4-21}\\
&= D_{\text {in }, N} \eta_{N} \ldots \eta_{1}-\left(D_{3}-1\right) \gamma_{3}-\lambda_{3} D_{\text {os }, 3}
\end{align*}
$$

Such a model is useful to economically generate an adaptive filtering algorithm look-up table for error estimation and fault isolation. Although in estimation theory several methods are available to estimate the desired response $D_{\text {out }}(t)$, the steepest-descent method (SDM) algo-
rithm [283] offers the smallest number of operations per iteration, gives unbiased estimates and require less memory than comparable algorithms based on Hessian matrix, such as for instance the Gauss-Newton, Levenberg-Marquardt and BFS methods.


Figure 4-17: a) Clock shell, b) Control logic for the switch ladder
By feeding the different input values $D_{i n}$ to each stage at iteration time $t$, as shown in Figure 4-18, the unknown filter outputs the desired response $D_{\text {out }}(t)$
$D_{\text {out }}(t)=D_{\text {in }}(t) \times W$
where weights $W^{T}=[\eta, \gamma, \lambda]$ are used to describe the behavior of the filter. Statistical data extracted through the die-level process monitor measurements and on-chip temperature information and their maximum-likelihood calculated through EM algorithm provide the esti-
mates $\left(W^{\prime}\right)^{T}=\left[\eta^{\prime}, \gamma^{\prime}, \lambda^{\prime}\right]$ with an initial value. By forcing the input signals to the predefined values in each stage, the input to a filter is controlled and residue voltages are obtained. The desired output is digitized; $D_{\text {out }}$ is collected from the back-end A/D converter and subtracted from the corresponding nominal value. This desired response is then supplied to filter for processing. Essentially, based on the predefined inputs and current error estimates $W^{T}=[\eta, \gamma, \lambda]$, the steepest-descent algorithm involves creation of an estimation error, $e$, by comparing the estimated output $D_{\text {out }}^{\prime}(t)$ to a desired response $D_{\text {out }}(t)$ and the automatic adjustment of the input weights $\left(W^{\prime}\right)^{T}=\left[\eta^{\prime}, \gamma^{\prime}, \lambda^{\prime}\right]$ in accordance with the estimation error $e$

$$
\begin{equation*}
W^{\prime}(t+1)=W^{\prime}(t)-\mu \times D_{\text {in }}(t) \times e(t) \tag{4-23}
\end{equation*}
$$

where the scaling factor used to update $W^{\prime}(t+1)$ is the step-size parameter, denoted by $\mu$.


Figure 4-18: Estimation method
$D_{\text {ourt }}(t)$ and $D_{i n}(t)$ are matrices with $2^{n-1}$ rows and three columns, where $n$ is the resolution of the stage. The step size, $\mu$, decrease in each iteration until the input weights decrease, i.e., until $W^{\prime}(t+1)<W^{\prime}(t)$. The estimation error, $e$, is the difference between the desired response and the actual steepest-descent filter output
$e(t)=D_{\text {out }}^{\prime}(t)-D_{\text {out }}(t)$
and based on the current estimate of the weight vector, $W^{\prime}, D^{\prime}(t)$ is
$D_{\text {out }}^{\prime}(t)=D_{\text {in }}(t) \times W^{\prime}(t)$

At each iteration, the algorithm requires knowledge of the most recent values, $D_{\text {in }}(t), D_{\text {out }}(t)$ and $W^{\prime}(t)$. During the course of adaptation, the algorithm recurs numerous times to effectively average the estimate and finally find the best estimate of weight $W$. The temporarily residue voltage in input $D_{i n}$ need to be updated after each iteration time to improve the accuracy, which can be done by using the current error estimate $W^{\prime}$ '.

It is important to note that because of the imbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another and that these fluctuations in the die temperature influence the device characteristics thereby altering the performance of integrated circuits. Furthermore, the increase in the doping concentration and the enhanced electric fields with technology scaling tend to affect the rate of change of the device parameter variations when the temperature fluctuates. The device parameters that are affected by temperature fluctuations are the carrier mobility, the saturation velocity, the parasitic drain/source resistance, and the threshold voltage. The absolute values of threshold voltage, carrier mobility, and the saturation velocity degrade as the temperature is increased. The degradation in carrier mobility tends to lower the drain current produced by a MOSFET. Although both saturation velocity and mobility have a negative temperature dependence, saturation velocity displays a relatively weaker dependence since electric field at which the carrier drift velocity saturates increases with the temperature. Additionally, as the transistor currents become higher while the supply voltages shrink, the drain/source series resistance becomes increasingly effective on the $I-V$ characteristics of devices in scaled CMOS technologies. The drain/source resistance increases approximately linearly with the temperature. The increase in the drain/source resistance with temperature reduces the drain current. Threshold voltage degradation with temperature, however, tends to enhance the drain current because of the increase in gate overdrive. The effective variation of transistor current is determined by the variation of the dominant device parameter when the temperature fluctuates. On average the variation of the threshold voltage due to the temperature change is between $-4 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ and $-2 \mathrm{mV} /{ }^{\circ} \mathrm{C}$ depending on doping level. For a change of $10^{\circ} \mathrm{C}$ this results in significant variation from the 500 mV design parameter commonly used for the 90 nm technology node. In the implemented system, the temperature sensors register any on-chip temperature changes, and the estimation algorithm update the $W^{\prime}$ with a forgetting factor, $\zeta$ [284]. The estimate at time $t+1$ is

$$
\begin{gather*}
W^{\prime}(t+1)=\zeta W^{\prime}(t)+(1-\zeta) W^{0}(t+1)  \tag{4-26}\\
0<\zeta \leq 1
\end{gather*}
$$

where $W^{0}(t+1)$ is an estimate prior to the registered temperature change.

```
Algorithm
Initialization
- Initialize the input vector \(D_{\text {in }}(0)\)
- Force the inputs and collect the desired output \(D_{\text {out }}(0)\)
- Measure and set the initial value of the weights \(W^{\prime}(0)\)
- Initialize the steepest descent update step \(\mu=1\)
- Initialize the forgetting factor \(\zeta\)
Data collection
- Collect \(N\) samples from the DLPM and temperature sensors
- Collect \(N\) samples from the AD converter
Update parameter estimate
    1. Update the input vector \(D_{i n}(t+1)\) based on current available \(W(t)\)
    2. Calculate the error estimate \(W^{\prime}(t)\)
    3. Generate the output estimate \(D^{\prime}{ }_{\text {out }}(t)=D_{\text {in }}(t) \times W^{\prime}(t)\)
    4. Calculate the estimation error \(e(t)=D_{\text {out }}^{\prime}(t)-D_{\text {out }}(t)\)
    5. Calculate the error estimate \(W^{\prime}(t+1)=W^{\prime}(t)-\mu \times D_{i n}(t) \times e(t)\)
    6. If \(W^{\prime}(t+1)>W^{\prime}(t)\) decrease step size \(\mu\) and repeat step 5
    7. Increase the iteration index, \(t\) and repeat steps 1-6 for best estimate
    8. Denote the final value of \(W^{\prime}\) by \(W_{l}\) '
    9. If temperature changes update \(W^{\prime}\) with new estimate \(W_{i}\) '
```


### 4.4. Debugging of Time-Interleaved Systems

System-on-chip (SoC) realizations require an A/D converter to be embedded on a large digital IC. To achieve the lowest cost, the system-on-chip has to be implemented in state-of-the-art CMOS technologies and must be area and power efficient and avoid the need for trimming to achieve the required accuracy. The rapidly decreasing feature size and power supply voltage of deep-submicron CMOS technology increases the pressure on converter requirements. The multi-step A/D converter architecture as shown in Chapter 3, allows the design of a high-speed, power efficient converter with less latency and less digital logic then a pipelined A/D converter. In such a system, the differential input signal is sampled with a time-interleaved sample-and-hold $(\mathrm{S} / \mathrm{H})$ circuit. In a time interleaved system, the sampling process is divided between $N \mathrm{~S} / \mathrm{H}$ units, which should be identical. The input signal is connected to all the units and the $N$ different $\mathrm{S} / \mathrm{H}$ units sequentially sample the input signal. This means that each unit has the time $N T_{s}$ to complete a sampling process, while the overall sampling interval is $T_{s}$. The output signals from the $\mathrm{S} / \mathrm{H}$ units are further quantized in the conversion stages before they are multiplexed together to form one output digital signal, which has a sampling interval of $T_{s}$. To achieve the sequential sampling, the clock signal is delayed with $i T_{s}$ to the $i^{\text {th }} \mathrm{S} / \mathrm{H}$ unit. However, the sample-and-hold circuit must still be fast enough to track the high frequency input signal. This is one limit to the number of S/H units that can be used in the time interleaved system. As extensively elaborated in Section 2.4.2, although time-interleaved principle provides high-speed and low power solution, its implementation, due to the manufacturing process, introduces several static and dynamic mismatch errors between interleaved units (offset, gain, bandwidth and time [115-118]), which limit the system performance. Offset mismatch causes fixed pattern noise in the sample-and-hold. It arises from op-amp offset mismatches and charge injection mismatches across the sample and hold units and results in constant amplitude offset in each $\mathrm{S} / \mathrm{H}$ unit. For a $d c$ input, each sample and hold unit may produce a different output and the period of this error signal is $N / f_{s}$. Due to the time mismatch caused by clock skew, clock jitter, phase noise or clock cross-coupling with input signal, delay times of the clock between the different S/H units are not equal. As a result the input signal will be periodically but non-uniformly sampled. The time mismatch errors cause frequency dependant noise in the system, which is the largest at the zero-crossings with a period of $N / f_{s}$ and is modulated by the input frequency $f_{\text {itr }}$ Similarly, if the gains of each $\mathrm{S} / \mathrm{H}$ unit are different, the basic error occurs with a period of $N / f s$ but the magnitude of the error is modulated by the input frequency $f_{i n}$. In both cases, noise spectrum peaks at $f_{s} / N \pm f_{i \text { i. }}$. The random variation in $\mathrm{S} / \mathrm{H}$ unit's internal capacitance, transconductance, hold capacitance as well as input capacitance and kickback noise of the subsequent stages, as seen from one $\mathrm{S} / \mathrm{H}$ unit, degrade output settling behavior and circuit gain-bandwidth product differently. This error occurs with a period of $N / f s$, but the magnitude of the error, which is frequency and amplitude dependant, is modulated by the input frequency $f_{i n}$ with noise spectrum spurious at $f_{s} / N \pm f_{i n}$.

Various methods for estimating static and dynamic mismatch effects in time-interleaved systems have been proposed [95-96,287-291]. In [287], the knowledge of multitone signals in DSL modems is used to estimate offset and time errors. In [95-96,288], a pseudo random signal is employed for background calibration of offset and gain errors. Distortion in time interleaved systems, with an algorithm for estimation and interpolation of the time errors with a sinusoidal input signal is discussed in [115,117]. In [288], an efficient interpolation algorithm is presented to estimate time error with a ramp input signal. In [289], a blind time error estimation method and in [290] blind equalization of the time, gain, and offset
mismatch errors was presented, assuming only that the input signal is band limited to the Nyquist frequency. In this thesis [291], blind estimation method for a rather new problem, bandwidth mismatch in an interleaved sampling system is proposed and the explicit formulas for its effects are derived.

Following notation in [290], the nominal sampling interval, without time errors, is denoted $T_{s}$. The sampling frequency is denoted $f_{s}=1 / T_{s}$ and the angular sampling frequency, $\omega_{s}=2 \pi f s . N$ denotes the number of $\mathrm{S} / \mathrm{H}$ units in the time interleaved array, which means that the sampling interval for each $\mathrm{S} / \mathrm{H}$ unit is $N T_{s}$. The time, offset, bandwidth and gain errors are denoted $\Delta^{0}{ }_{t 0} \Delta^{0}{ }_{o p} \Delta^{0}{ }_{b,}$ and $\Delta^{0}{ }_{g,}, i=0, \ldots, N-1$ respectively. The vector notation $\Delta^{0}=\left[\Delta^{0}{ }_{t 0} \ldots \Delta^{0}{ }_{t N-1}\right]$ is used to denote all the time errors. The offset, bandwidth and gain errors are denoted similarly. It is assumed that there are no other errors in the S/H units except the four types of mismatch errors. Similarly, $x(t)$ is the analog input signal and $y_{i}[k]$ are the output subsequences from the $\mathrm{NS} / \mathrm{H}$ units, sampled with time errors
$y_{i}[k]=\left(1+\Delta_{g_{i}}^{0}\right)\left(1+\Delta_{b_{i}}^{0}\right) x\left((k N+i) T_{s}+\Delta_{t_{i}}^{0}\right)+\Delta_{o_{i}}^{0}$

Uniform sampling of $x(t)$ at the Nyquist rate results in samples $x(t=n T)$ that contain all the information about $x(t)$. If the input signal is band limited to the Nyquist frequency and the error parameters are known, the input signal can be perfectly reconstructed from the irregular samples [292]. The amplitude offset errors are removed by subtracting the offset error parameters from the respective subsequences. Similarly, the gain errors can be removed, after the offset errors are removed, by dividing the subsequences by the respective $\mathrm{S} / \mathrm{H}$ gain. At the end the bandwidth errors are removed. Reconstructured output signal \% can be then expressed as

$$
\begin{align*}
& z_{i}^{\left(\Delta_{o_{i}}^{0}\right)}[k]=y_{i}[k]-\Delta_{o_{i}}^{0}=\left(1+\Delta_{g i}^{0}\right)\left(1+\Delta_{b_{i}}^{0}\right) x\left((k N+i) T_{s}+\Delta_{t_{i}}^{0}\right) \\
& \left.z_{i}^{\left(\Delta_{i}^{0} \Delta_{i} \Delta_{g_{i}}^{0}\right)}{ }^{\prime}{ }^{0}\right]=z_{i}^{\left(\Delta_{i}^{0}\right)}[k] /\left(1+\Delta_{s_{i}}^{0}\right)=\left(1+\Delta_{b_{i}}^{0}\right) x\left((k N+i) T_{s}+\Delta_{t_{i}}^{0}\right)  \tag{4-28}\\
& z_{i}^{\left(\Delta_{o_{i}}^{0}, \Delta_{g_{i}}^{0} \Delta_{i_{i}}^{0}\right)}[k]=z_{i}^{\left(\Delta_{o_{i}}^{0}, \Delta_{i_{i}}^{0}\right)}[k] /\left(1+\Delta_{b_{i}}^{0}\right)=x\left((k N+i) T_{s}+\Delta_{i,}^{0}\right)
\end{align*}
$$

In [293] a minimal sampling rate for an arbitrary sampling method that allows perfect reconstruction is developed. In [294] it was shown that only special cases of bandpass signals can be perfectly reconstructed from their uniform samples at the minimal rate of $2 \times$ Bandwidth [samples/sec], while in [295] a reconstruction scheme that recovers any bandpass signal exactly is provided. In [296] and [297] a blind multi-coset sampling strategy that is called universal in [297] is suggested. Multi-coset sampling is a selection of certain samples from uniform sampling. The uniform grid is divided into blocks of $L$ consecutive samples. A constant set $C$ of length $p$ describes the indices of $p$ samples that are kept in each block while the rest are zeroed out. The set $C=\left\{c_{i}\right\}_{i=1}$ is referred to as the sampling pattern where $0 \leq c_{1}<c_{2}<\ldots<c_{p} \leq L-1$. Define the $i^{\text {th }}$ sampling sequence for $1 \leq i \leq p$ as

$$
x_{c i}[n]=\left\{\begin{array}{cl}
x\left(t=n T_{s}\right) & n=m L+c_{i}  \tag{4-29}\\
0 & \text { otherwise }
\end{array}\right.
$$

The sampling stage is implemented by $p$ uniform sampling sequences with period $1 /\left(L T T_{s}\right.$, where the $t^{t^{t h}}$ sampling sequence is shifted by $c_{i} T_{s}$ from the origin. Therefore, a multi-coset
system is uniquely characterized by the parameters $L, p$ and the sampling pattern $C$. Direct calculations show that [297]

$$
\begin{align*}
& Z_{c}^{\left(\Delta_{b}^{0}\right)}\left(e^{j 2 \pi T T_{s}}\right)=\frac{1}{L T} \sum_{r=0}^{L-1}\left(e^{j 2 \pi c_{i} r L}\right) X\left(f+\frac{r}{L T}\right)  \tag{4-30}\\
& \forall f \in F_{0}=\left(0, \frac{1}{L T}\right), 1 \leq i \leq p
\end{align*}
$$

where $Z_{i}\left(e^{j 2 \pi f T}\right)$ is the discrete-time Fourier transform (DTFT) of $x_{i[ }[n]$ band-limited to $F$. For our purposes it is convenient to express previous equation in a matrix form as

$$
\begin{equation*}
y(f)=A x(f), \quad \forall f \in F_{0} \tag{4-31}
\end{equation*}
$$

where $y(f)$ is a vector of length $p$ whose $i^{\text {th }}$ element is $Z_{i d}\left(e^{2 \pi \pi T}\right)$, and the vector $x(f)$ contains $L$ unknowns for each $f$

$$
\begin{equation*}
x_{i}(f)=X\left(f+\frac{i}{L T}\right), \quad 0 \leq i \leq L-1, \quad f \in F_{0} \tag{4-32}
\end{equation*}
$$

The matrix $A$ depends on the parameters $L, p$ and the set $C$ but not on $x(t)$ and is defined by

$$
\begin{equation*}
A_{i k}=\frac{1}{L T_{s}} e^{j 2 \pi c_{i} k / L} \tag{4-33}
\end{equation*}
$$

With the inverse time discrete Fourier transform (ITDFT) the time error reconstructed signal can be derived

$$
\begin{equation*}
z_{c}^{\left(\Delta_{t}^{0}\right)}[k]=\operatorname{ITDFT}\left(Z^{\left(\Delta_{t}^{0}\right)}\left(e^{j 2 \pi f T_{s}}\right)\right) \tag{4-34}
\end{equation*}
$$

The quality criterion commonly adopted for an estimator of the loss function is the meansquared error criterion, mainly because it represents the energy in the error signal, is easy to differentiate and provides the possibilities to assign the weights (Section 4.3.1)

$$
\begin{equation*}
W_{t}^{(M)}\left(\Delta_{t}\right)=\sum_{i=1}^{L-1 i-1} \sum_{j=0}\left(\frac{1}{L} \sum_{k=1}^{M}\left(z_{i}^{\left(\Delta_{i}\right)}[k]\right)^{2}-\left(z_{j}^{\left(\Delta_{j}\right)}[k]\right)^{2}\right)^{2} \tag{4-35}
\end{equation*}
$$

Similarly, to estimate the offset errors, it is assumed that the mean value of the output from each $\mathrm{S} / \mathrm{H}$ unit corresponds to the respective offset errors. Additionally, it is assumed that there are no other errors in the $\mathrm{S} / \mathrm{H}$ units except the offset errors. To estimate the gain errors, it is assumed that the gain errors are only errors present in the circuit.

The measure of the gain error is the variance of the output from each $\mathrm{S} / \mathrm{H}$ unit corresponding to the respective gain of the $\mathrm{S} / \mathrm{H}$ unit. Equally, to estimate the bandwidth errors, it is assumed that the bandwidth errors are only errors present in the circuit. The measure of the bandwidth error is the variance of the gain-bandwidth product from each S/H unit corresponding to the respective gain-bandwidth product of the $\mathrm{S} / \mathrm{H}$ unit. Note that $\Delta_{b i}$ is a function of the input frequency as well as the bandwidth. Also, remark that phase variation due to the bandwidth mismatch is a nonlinear function of the input frequency while the phase
mismatch due to the timing skew is its linear function. The offset, gain and bandwidth loss function can be then defined as

$$
\begin{align*}
& W_{o}^{(M)}\left(\Delta_{o}\right)=\sum_{i=1}^{L-1} \sum_{j=0}^{i-1}\left(\frac{1}{L} \sum_{k=1}^{M}\left(z_{i}^{\left(\Delta_{o_{i}}\right)}[k]\right)^{2}-\left(z_{j}^{\left(\Delta_{o}\right)}[k]\right)^{2}\right)^{2} \\
& W_{g}^{(M)}\left(\Delta_{g}\right)=\sum_{i=1}^{L-1-1-1} \sum_{j=0}\left(\frac{1}{L} \sum_{k=1}^{M}\left(z_{i}^{\left(\Delta_{\left.g_{i}\right)}\right)}[k]\right)^{2}-\left(z_{j}^{\left(\Delta_{g_{j}}\right)}[k]\right)^{2}\right)^{2}  \tag{4-36}\\
& W_{b}^{(M)}\left(\Delta_{b}\right)=\sum_{i=1}^{L-1} \sum_{j=0}^{i-1}\left(\frac{1}{M} \sum_{k=1}^{M}\left(z_{i}^{\left(\Delta_{i}\right)}[k]\right)^{2}-\left(z_{j}^{\left(\Delta_{j}\right)}{ }^{2}[k]\right)^{2}\right)^{2}
\end{align*}
$$

The minimizing arguments of the loss functions give the mismatch error estimates. However, the mismatch errors may change slowly with for instance temperature and aging, so the parameter estimates have to be adaptively updated with new data. Since the minimizing argument cannot be calculated analytically, a numerical minimization algorithm instead is employed.

Although in estimation theory several methods are available to estimate the desired response, a gradient search method [283] offers the smallest number of operations per iteration and does not require correlation function calculation. Essentially, the algorithm involves creation of an estimation error by comparing the estimated output to a desired response and the automatic adjustment of the input weights in accordance with the estimation error
$\Delta^{(i+1)}=\Delta^{(i)}-\mu \nabla W\left(\Delta^{(i)}\right)$
where the scaling factor used to update $\Delta^{(i+1)}$ is the step-size parameter, denoted by $\mu$. The step size, $\mu$, decrease in each iteration until the input weights decrease, i.e., until $\Delta^{(i+1)}<\Delta^{(i)}$. If condition on-chip change, e.g. temperature, the estimation algorithm update the $\Delta^{(i+1)}$ with a forgetting factor, $\zeta$ [284]. The new estimate is given as

$$
\begin{gather*}
\Delta^{(i+1)}=\zeta \Delta^{(i)}+(1-\zeta) \Delta_{F}^{(i+1)}  \tag{4-38}\\
0<\zeta \leq 1
\end{gather*}
$$

where $\Delta_{F}^{(i+1)}$ is an estimate prior to the registered temperature change.

| Algorithm |
| :--- |
| Initialization |
| - Choose a batch size, $M$, for each iteration |
| - Initialize the steepest descent update $\mu=1$ |
| - Initialize the parameter estimates $\Delta_{o i}{ }^{(0)}=0, \Delta_{g i}^{(o)}=0, \Delta_{b i}{ }^{(0)}=0, \Delta_{t i}^{(0)}=0, i=0, \ldots, N-1$ |
| - Initialize the forgetting factor $\zeta$ |
| Data collection |
| - Collect $M$ samples from DUT |
| Update parameter estimate |
| 1. Calculate the reconstructed signal according to $(4-28)$ and $(4-34)$ |
| 2. Calculate the gradients of the loss function $r W_{o}\left(\Delta_{o}\right), r W_{g}\left(\Delta_{g}\right), r W_{b}\left(\Delta_{b}\right), r W_{t}\left(\Delta_{t}\right)$ |
| 3. Update the parameter estimate $\Delta^{(i+1)}=\Delta^{(i)}-\mu \times r W\left(\Delta^{(i)}\right)$ |
| 4. If $\Delta^{(i+1)}>\Delta^{(i)}$ decrease step size $\mu$ and repeat step 3 |
| 5. Increase the iteration index, $i$, and repeat steps 1-4 for best estimate |
| 6. Denote the final value of $\Delta^{(i+1)}$ by $\Delta_{F}^{(i+1)}$ |
| 7. If condition change update $\Delta_{F}^{(i+1)}$ with new estimate $\Delta_{F}{ }^{(i+1)}$ |

### 4.5. Foreground Calibration

As elaborated in Chapter 2, a practical converter is likely to exhibit deviations from the ideal operation of sample, hold and quantization. Debugging techniques, such as those described in the previous sections, evaluate if the true output from the converter is within the tolerable deviation of the ideal output. The information obtained in this manner can than be re-used to supplement the circuit calibration. Since the use of digital enhancing techniques reduces the need for expensive technologies with special fabrication steps, a side advantage is that the cost of parts is reduced while maintaining good yield, reliability and long-term stability. Indeed, the extra cost of digital processing is normally affordable as the use of submicron mixed signal technologies allows for efficient usage of silicon area even for relatively complex algorithms.

A wide variety of calibration techniques to minimize or correct the steps causing discontinuities in the A/D converter's stage transfer functions has been proposed [29,95-96,154-163]. The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. Analog calibration methods include in this context the techniques in which adjusting or compensation of component values is performed with analog circuitry, while the calculation and storing of the correction coefficient can be digital. However, digital methods have gained much more popularity, mainly because of the increased computational capacity, their good and well predefined accuracy, and flexibility.

Besides the classification of the calibration methods to error-averaging, analog, and digital, the calibration techniques can be divided into foreground and background methods, depending on whether the normal operation is interrupted or not. As illustrated in Figure 4-19a), foreground calibration requires the operation of an $A / D$ converter to be interrupted so that a known input sequence can be applied to the $\mathrm{A} / \mathrm{D}$ converter, where by comparing the output of the $A / D$ converter to the expected $A / D$ converter output under ideal conditions the impact of missing codes can be quantified and corrected. The ideal A/D converter, drawn with dashed lines in Figure 4-19a) is not physically implemented (e.g. instead, in practice, a look-up table based methods are implemented); digital output is already known since calibration input is known. In foreground schemes calibration can be achieved within a small number of clock cycles as the error signal is highly correlated with the error sources causing the missing codes. However, the A/D converter has to be taken offline every time calibration is performed, which in some applications may not be possible.

On the other hand, background calibration shown in Figure 4-19b), such as [34] highlighted in Section 2.6.2 continuously measures and removes missing codes. Similar to foreground calibration, the ideal A/D converter in the background calibration technique is not physically implemented; the digital output is already known since pseudo-noise sequence is known. Typically, the background calibration techniques are developed from the same algorithms as the foreground methods by adding hardware or software to perform the calibration coefficient measurements transparent to the normal operation, although, a number of algorithms are originally intended for background operation. In a statistical scheme the input of the stage under calibration is effectively modulated by a known pseudo-random sequence, where by correlating the digital output of the A/D converter with the known pseudo-random sequence the impact of missing codes can be determined. In essence, the input signal is multiplied with a pseudo binary random sequence of +1 and -1 before $A / D$ conversion. The digital output
signal is then multiplied with the same sequence, to reconstruct the signal. To avoid significantly altering the A/D converter output spectrum the pseudo-noise sequence is typically made very long to avoid correlations with the analog input, as well as small in amplitude so that the injected pseudo-random sequence which appears as an additional white noise source at the output only consumes a small portion of the dynamic range.


Figure 4-19: Principle of a) foreground calibration and b) background calibration
In general, the maximum sample rate and attainable resolution are equal for foreground and background calibration techniques, while the latter approach ends up with more complex realizations requiring redundant hardware or excessive digital signal processing. With background calibration schemes however, since the adjustment of the compensation values is with $\pm 1$ at a time, a large number of clock cycles are required before the end value is reached. In A/D converters which use background-statistical techniques long calibration times can lead to excessive test times, limiting IC production throughput and thus reducing revenue. For example, with 4 million calibration cycles, even with a reasonably high sampling rate of $40 \mathrm{MS} / \mathrm{s}, 100 \mathrm{~ms}$ would be required at minimum to test the A/D converter. For higher resolution and/or lower speed $\mathrm{A} / \mathrm{D}$ converters the test time can be much higher [298].

Unlike in the analog calibration technique where components are measured and then corrected until they match, in the foreground digital calibration technique component ratios are measured, quantized by following stages of the A/D converter and then stored digitally. The results of the measurements are later used with the digital output of the analog to digital converter to generate a corrected digital output with improved linearity. This technique has the disadvantage that it requires the use of digital adders not required by the analog technique. However, the technique greatly relaxes the design requirements for some of the analog components and results in a design that is very reliable and robust. In each stage of the multistep, the comparators divide the range of possible signal values into a set of smaller ranges or bins. Associated with each bin is a digital code and D/A converter weight. Each stage of the A/D converter assigns the signal to a certain bin and generates a residue signal. When the conversion is complete, the signal has a bin assignment for each stage of the A/D converter. Thus, the signal is assigned a digital code and weight by each stage of the A/D converter. To reconstruct a linear digital representation of the input signal, the weights are all summed.

When the linear reconstruction of the inputs is done, the results for both signals should match each other. If $w$ is used to denote the weights from the $i$ stage of interest and $D$ is used to denote the code resulting from the rest of the A/D converter, then code $=w_{i}+D_{i}$ and co$d e_{i+1}=w_{i+1}+D_{i+1}$. For codes to match, $w_{i+1}-w_{i}=D_{i}-D_{i+1}=G\left(V_{\mathrm{R} i}-V_{\mathrm{R} i+1}\right) \cdot D_{i}-D_{i+1}$ is the height of the discontinuity. Thus, the height of the discontinuity is the difference in the weights corresponding to the bins on either side of the discontinuity. Therefore, the weights are assigned by measuring each of the discontinuities: assume that a signal $V_{i}$ close to the threshold for the discontinuity is applied to the input of the stage of interest. Two measurements are then made: in the first case, the $\mathrm{D} / \mathrm{A}$ converter level immediately below the comparator threshold is subtracted from the input signal. The resulting residue for this case is then amplified and quantized by the rest of the multi-step $\mathrm{A} / \mathrm{D}$ converter obtaining the digitized output $D_{i}$. Next, the input signal is kept the same and the $\mathrm{D} / \mathrm{A}$ converter level immediately above the comparator threshold is subtracted from the input signal. The residue for this case is also amplified and quantized by the rest of the multi-step A/D converter. For this case, the residue output $D_{i+1}$ is obtained. $D_{i}-D_{i+1}$ is then computed to obtain the result for the weight difference. This measurement is done at each threshold.

A digitally calibrated multi-step A/D converter operation is similar to the operation of an uncalibrated converter with the following exception. Instead of incorporating the A/D converter output bits from each stage directly into the digital output word, the bits from each stage are instead used as the address to a lookup table. A decoder translates the address into a signal that selects the appropriate $\mathrm{D} / \mathrm{A}$ converter weight from the lookup table. This $\mathrm{D} / \mathrm{A}$ converter weight is then added to the digital result from the previous stage. In the last stage, the final digital output word is the sum of each of the selected DAC weights, one from each stage of the converter. Recall that residue signal $V_{i+1}$ of $i+1$ stage can be described by
$V_{i+1}=\eta_{i} V_{i}+\left(1-D_{i}\right) \cdot \gamma_{i} V_{\text {ref }}+\lambda_{i}$
where $D_{i}$ is the output from the sub-A/D converter of the stage. Dividing both sides with $V_{r p}$ the stage $i$ input signal $V_{i}$ can be found as

$$
\begin{equation*}
V_{i} / V_{\text {ref }}=1 / \eta_{i}\left(V_{i+1} / V_{\text {ref }}-\left(1-D_{i}\right) \cdot \gamma_{i}-\lambda_{i} / V_{\text {ref }}\right) \tag{4-40}
\end{equation*}
$$

This equation forms the basis of the proposed calibration algorithm [299-300]. Stage gain error $\eta_{i}$, internal reference voltage error $\gamma_{i}$ and systematic offset error $\lambda$ are estimated by using the algorithm described in Section 4.3. In order to recover the correct value of $V_{\rho} V_{i+1} / V_{r g}$ have to be recovered first. A digital code $D_{\text {out }}$ is obtained by normalizing the analog input voltage $V_{i n}$ to reference voltage $V_{r p}$

If the ( $\mathrm{N}-\mathrm{\imath}$ ) bits back-end $\mathrm{A} / \mathrm{D}$ converter is an ideal $\mathrm{A} / \mathrm{D}$ converter, the digital output $D_{\text {BE }}$ of input voltage $V_{i+1}$ written in offset code format can be expressed as
$D_{B E}=b_{1} b_{2} \ldots b_{N}=b_{1} 2^{N-1}+b_{1} 2^{N-2}+\ldots+b_{N-1} 2+b_{N}$

Multiplying the offset-coding $D_{B E}$ by $V_{L S B}$ and removing the offset, the approximate value of $V_{i+1}$ is then calculated as

$$
\begin{equation*}
V_{i n} / V_{r e f} \approx\left(D_{B E}-2^{N-i-1}\right) / 2^{N-i-1}=b_{i+1}+b_{i+2} 2^{-1}+\ldots+b_{N-1} 2^{-(N-i-2)}+b_{N} 2^{-(N-i-1)}-1+1 / 2^{N} \tag{4-42}
\end{equation*}
$$

Assuming the error parameters for each stage which will be calibrated are known from the algorithm described in Section 4.3, the procedure to calibrate the entire multi-step A/D converter can be described as:
i) firstly, calibration is started from stage $i$ to find the residue voltage $V_{i+1}$ from back-end A/D converter output $D_{B E}$, ii) next, the stage input $V_{i}$ based on the algorithm output $V_{i+1}$ is recovered and $i i i$ ) at the end, first two steps to calibrate stage $i-1$ are repeated until the first stage is reached. $V_{1}$ is the calibrated value of input signal $V_{i n}$. The digital output is obtained by quantizing $V_{1}$ to $N$ bits.

The accuracy of the calibration is dependent on the accuracy of the A/D converter used to perform the calibration. Differential non-linearity in the A/D converter used to measure the weights corrupts the measurement; the new $A / D$ converter that includes the measured stage will have DNL at the comparator thresholds, which can be a limiting factor if the multi-step A/D converter is employed to calibrate itself. Fortunately, the DNL caused by the A/D converter during this measurement is scaled down since the measurement occurs on the amplified residue. Therefore, if the DNL of the A/D converter without the calibrated stage is $x$, the DNL of the A/D converter with the calibrated stage is $x / G$ where $G$ is the gain of the residue amplifier. Thus, it is possible to calibrate a multi-step A/D converter starting from the back-end A/D converter output and working forward towards the front-end. Similarly, some accumulation of errors does occur during the calibration process. However, this accumulation of errors are kept to a minimum by designing the multi-step A/D converter in such a way that small variations in the input signal only affect the code produced by the end stages.

The design allows the inclusion of the calibration logic on the same chip as the A/D converter or its realization with an FPGA, which is combined with the A/D converter chip on the circuit board level. The calibration state machine controls the reference voltage switching in the $\mathrm{D} / \mathrm{A}$ converters of the first two stages during the calibration hold phases. The input signals for the calculation and coding logic are the RSD-corrected digital words from the converter chip, the raw bits of the first and the second stage, the state-indicating bits, and an external reset signal. The calibration coefficients per stage are calculated as an average of four measurements and stored in a memory. During normal operation calibration coding is simply the addition of two coefficients, which are selected according to the raw bits of the two first stages, to each uncalibrated A/D converter output word.

### 4.6. Experimental Results

The validity of the various concepts described in this Chapter is evaluated on the proposed three-step/multi-step A/D converter (Figure 4-20) with dedicated embedded sensors fabricated in standard single poly, six metal $0.09-\mu \mathrm{m}$ CMOS. The converter input signal is sampled by a three-time interleaved sample-and-hold, eliminating the need for re-sampling of the signal after each quantization stage. The $\mathrm{S} / \mathrm{H}$ splits and buffers the analog delay line sampled signal that is then fed to three A/D converters, namely, the coarse (four bits), the mid (four bits) and the fine (six bits). The quantization result of the coarse A/D converter is used to select the references for the mid quantization in the next clock phase. The selected references are combined with the held input signal in two dual-residue amplifiers, which are offset calibrated. The mid A/D converter quantizes the output signals of these mid-residue amplifiers. The outputs from both coarse and mid A/D converters are combined in order to select proper references for the fine quantization. These references are combined with the sampled input signal in two, also offset calibrated, dual-residue amplifiers. The amplified residue signals are applied to a fine A/D converter.


Figure 4-20: Prototype three-step/multi-step $A / D$ converter

The prototype was fabricated in standard single poly, six metal $0.09-\mu \mathrm{m}$ CMOS with the core area of $0.6 \mathrm{~mm}^{2}$ excluding bond pads. The A/D converter operates at 1.2 V supply voltage and dissipates 85 mW (without output buffers). As the CMOS technology scales to a smaller feature size, it is apparent that digital circuits will benefit from it in speed, power and area. These benefits cannot be applied to analog circuits directly simply because the figures of merit in analog circuits extend beyond speed, power and area. The digital scaling yields a combination of area reduction, bandwidth increase and reduction in power dissipation although at the cost of lower SNR and worse linearity. The focus of the scaling for the analog circuits can be shifted from the standard digital scaling to the performance increase analog scaling. In [301] is shown that the analog scaling can achieve the increase of the circuit bandwidth and the dynamic range at a fixed frequency, although under assumption that analog circuits occupy small part of a system on chip and therefore can be penalized by the increase of area and power. The techniques which contribute to the goals of the scaling can be categorized into two sections. On architectural level, the choice of per-stage resolution, coding and digital correction relaxes the requirements on some active circuit blocks which are conventionally known as power demanding blocks. On a circuit level, taking advantage of digital
correction, dynamic comparators are used to eliminate static power consumption. A high speed, low voltage opamp with a pre-amplifier and cascode transconductance stage is employed to achieve fast settling and high $d c$ gain. Lastly, the clock boosting circuit is utilized to reduce the on-resistance due to low supply voltage. The digital section in this converter design includes the clock generators, digital decoders and digital correction circuit.

The effect of technology scaling on source/drain parasitic capacitance is not obvious because it depends on doping density, junction depth, source/drain area scaling, etc. If it is assumed that parasitics are only affected by the scaled feature size, the ratio of the source/drain parasitic capacitance is roughly equal to the technology scaling constant $s$. Other sources of parasitics capacitance, such as wiring, overlapping, also change with technology. Although the line width of a metal line may decrease with technology, the coupling between two adjacent metal lines tends to increase because the minimum separation between metal lines is decreased. Other minor factors, such as metal resistance requirement, may determine the width for a long metal wire which will also affect the parasitic capacitance. In general, because the overall die size is about $(1 / s)^{2}$ smaller, it can be assumed that the parasitic (if dominated by wiring and overlapping) is roughly $(1 / s)^{2}$ as well. If all of the dimensions and voltages (and currents) are scaled following the suggestions from the analog scaling scenario, the transconductance increase by the factor $1 / s^{3}$. The output impedance in saturation scales with $s^{3}$ so the intrinsic gain, $g_{m} r_{o}$ remains constant. With analog scaling, the maximum allowable voltage swings decrease by a factor $s$, lowering the dynamic range of the circuit. In order to restore the dynamic range, the transconductance of the transistors must increase by a factor $1 / \mathrm{s}^{3}$ because thermal noise voltages and currents scale with $V_{g_{m}}$. Since voltage scaling requires that $V_{G S}-V_{T}$ decrease by a factor of $1 / \mathrm{s}$, drain current $I_{D}$ must increase by the same factor, increasing the power dissipation with $1 / s$. Similarly, if $C_{o x}$ is scaled up by $1 / s$ and $L$ and $\left(V_{G S}-V_{T}\right)$ are scaled down by $s$, then $W$ must increase by $1 / s^{2}$.

For the twelve bit resolution, the hold capacitors in the sample-and-hold circuit is determined by the noise limitation, therefore, the required capacitor size is the same in both technologies. In reality, since $C_{H}$ is kept the same for noise reasons, $f_{T}$ is higher in the scaled technology for a particular bias condition and a fixed $g_{m}$. This translates to an increase of speed with the same power dissipation. Furthermore, $v_{D S A T}$ can also be lowered in the scaled technology to increase $g_{m}$. Also the parasitic capacitances for both the opamp input and source/drain output capacitances are smaller in the scaled technology than the $0.18-\mu \mathrm{m}$ design improving the feedback factor as well as the settling time. If the $C_{L}$ is determined by the parasitic capacitance, it is decreased by about a factor of $s$ when the technology is scaled due to the reduced gate and source/drain capacitances. This means $g_{m}$ can be scaled by a factor of $s$ as well. If $v_{D S A T}$ is kept constant, the current required can be reduced by roughly a factor of $s$, which translates to a power saving of $1 / \mathrm{s}$.

In Figure 4-21 a micrograph of the test-chip is presented. Dedicated embedded sensors and the complete DfT occupy less than $10 \%$ of the overall area. Extra digital circuitry is added on the left, along with some dummy metal lines for process yield purposes. Additionally, the testchip contains a temperature sensor (located between the coarse A/D converter and the fine residue amplifiers) and matrix of differential transistor pairs and ladder resistors divided into specific groups, which are placed in and around the partitioned multi-step A/D converter.

To allow characterization of current process variability conditions of certain parameters of interest, enabling the optimized design environment, each group of monitors target a specific error source as shown in Section 4.1.4. Repetitive single die-level process monitor measurements are performed to minimize noise errors. Each die-level process monitor consists of multiple differential transistor pairs (with sources and drains connected in parallel within one path), which are spaced at different mutual distances to examine the effect of spatial dependence on offset. All sources are connected to a common point. All transistors in the same monitor have their gates connected to a common point. Special attention is paid in the layout to obtain a very low resistance in the gate path to eliminate systematic errors during the measurements; very wide source metal connections are used.


Figure 4-21: Chip micrograph
The clock lines are routed in the center of the active area where the appropriate phases are tapped off at the location of each stage in the circuit. Digital correction is at the lower right corner of the active area; and twelve bit output is produced at the pads on the bottom. Extra digital circuitry is added on the right, along with some dummy metal lines for process yield purposes. Similar to the converter described in Chapter 2, the differential circuit topology is used throughout the design and multiple substrate taps are placed close to the noise sensitive circuits to avoid the noise injection. For analog blocks, substrate taps are placed close to the $n$-channel transistors and connected to an analog ground nearby (for common-source configuration, substrate taps are connected to the source). For digital blocks, substrate taps are placed close to $n$-channel transistors and connected to a separate substrate pin to a dedicated output pad. This pad is then joined with ground on the evaluation board. An added advantage for placing substrate taps close or next to transistors is to minimize the body effect variation. For common-source devices, no body effect is found since the source and body are connected. For cascode devices, although the source potential may vary with respect to the body potential, the effect of $V_{T}$ on the drain current is greatly reduced due to the source degeneration. No additional substrate taps are placed to avoid that they act as noise receptors to couple extra noise into the circuit. Separate $V_{D D}$ and ground pins are used for each functional block not only to minimize the noise coupling between different circuit blocks, but also to reduce the overall impedance to ground. Multiple $V_{D D}$ and ground pins are used throughout the chip. The digital $V_{D D}$ and ground pins are separated from the analog ones. Within the analog section, $V_{D D}$ and ground pins for different functional blocks are also separated to have more flexibility during the experiment. Each supply pin is connected to a Hewlett-Packard HP3631A voltage regulator and is also bypassed to ground with a $10 \mu \mathrm{~F}$ Tantalum capacitor and a $0.1 \mu \mathrm{~F}$ Ceramic chip capacitor.

The reference current sources are generated by Keitbley 224 external current source. For the experiment, the sinusoidal input signal is generated by an arbitrary waveform generator (Tektronix AWG2021). This signal comes on-board through a SMA connector and is applied to a transformer (Mini-Circuit PSCJ-2-1) which converts the single-ended signal to a balanced, differential signal. The outputs of the transformer are $d c$ level-shifted to a common-mode input voltage and terminated with two $50 \Omega$ matching resistors. The common-mode voltage of the test signal going into the $\mathrm{A} / \mathrm{D}$ converter is set through matching resistors connected to a voltage reference and is nominally set at 0.6 V . The digital output of the $\mathrm{A} / \mathrm{D}$ converter is buffered with an output buffer to the drive large parasitic capacitance of the lines on the board and probes from the logic analyzer. The digital outputs are captured by the logic analyzer (Agilent 1682AD). A clock signal is also provided to the logic analyzer to synchronize with the A/D converter. All the equipment is set by a LabView program and signal analysis is performed with MatLab.

### 4.6.1. Application of Results for A/D Test Window Generation/Update

By sweeping the reference voltage until a change in the decision occurs, information about the process variation effects is extracted. A discrimination window for various die-level process monitors is defined according to the rules of the multi-step A/D converter error model described in Section 4.1.3. The drain voltage of the different transistors in each dielevel process monitor are accessed sequentially though a switch matrix which connects the drain of the transistor pairs under test to the voltage meter; the drains of the other transistors are left open. The switch matrix connects the gate of the transistor pairs under test to the gate voltage source and connects the gates of the other rows to ground. The analysis of critical dimensions shows a dependence of the poly-line width on the orientation. This cause performance differences between transistors with different orientations. For transistor pairs no systematic deviations are observed between different gate orientations. All transistors are biased in strong inversion by using gate voltages larger than $V_{T}$. Since the different transistors are measured sequentially the $d c$ repeatability of the $d c$ gate voltage source must be larger than the smallest gate-voltage offset to be measured. The repeatability of the source in measurement set-up was better than six digits, which is more than sufficient. The offset is estimated from the sample obtained by combining the results of the devices at minimum distance over all test-chips. The same statistical techniques are used as for the distance dependence.

In the coarse A/D converter illustrated in application example, some DNL errors are present as shown in Figure 4-22a). Figure 4-22b) and Figure 4-23 illustrate histogram estimated from one hundred and forty samples extracted from a similar number of differential transistor pairs and ladder resistor measurements in the test matrix. As the number of on-chip die-level process monitors is finite due to area limitations, additional information is obtained through statistical techniques. The estimation of the parameters based on the EM-algorithm is illustrated in Figure 4-24, corresponding to the maximum likelihood estimates based uniquely on the observed data. The EM algorithm allows obtaining the maximum likelihood estimates of the unknown parameters by a computational procedure which iterates, until convergence, between two steps. As the main statistical concern is parameter estimation and in most cases this is best achieved by the use of maximum likelihood theory, the EM algorithm substitutes the missing data in the log likelihood function, not in the incomplete data set; the missing values are substituted by the conditional expectations of their functions, as they appear in the log-likelihood function. To make the problem manageable, the model for the process parameter variation in this realization is assumed to follow Gaussian distribution. With that
assumption, then the modeled values corresponds to the expected values of the sufficient statistics for the unknown parameters. For such densities, it can be said that the incompletedata set is the set of observations, whereas each element of the complete-data set can be defined to be a two-component vector consisting of an observation and an indicator specifying which component of the mixture occurred during that observation. The mixtures of Gaussians are initialized by applying the EM equations to the observed mixtures of two univariate Gaussian components based on die-level process monitors and coarse A/D converter DNL measurements. The plot of the log-likelihood function $L\left(\theta^{(t)} \mid T_{X Y}\right)$ with respect to the number of iterations is visualized in Figure 4-25a). Each iteration is guaranteed to increase the likelihood, and finally the algorithm converges to a local maximum of the likelihood function in twelve iterations.

The mean $\mu$ and the variance $\sigma$ of decision stage offset errors $\lambda$, stage gain errors $\eta$, and errors in the internal reference voltages $\gamma$ is estimated. The convergence properties of the EM algorithm are discussed in detail in [263]. Recall that $\theta^{(t+1)}$ is the estimate for $\theta$ which maximizes the difference $\Delta\left(\theta \mid \theta^{(t)}\right)$. Starting with the current estimate for $\theta$, that is $\theta^{(t)}, \Delta\left(\theta \mid \theta^{(t)}\right)=0$. Since $\theta^{(t+1)}$ is chosen to maximize $\Delta\left(\theta \mid \theta^{(t)}\right), \Delta\left(\theta^{(t+1)} \mid \theta^{(t)} \geq \Delta\left(\theta^{(t)} \mid \theta^{(t)}\right)=0\right.$, so for each iteration the likelihood $L(\theta)$ is nondecreasing.


Figure 4-22: a) Coarse $A / D$ converter bistogram estimated from measured bundred samples, b) gain-based DLPM bistogram estimated from measured one bundred and forty samples


Figure 4-23: DLPM bistogram estimated from measured one bundred and forty samples of a) decision stage-based DLPM and b) reference-based DLPM

When the algorithm reaches a fixed point for some $\theta^{(t)}$ the value $\theta^{(t)}$ maximizes $Q(\theta)$. Since $L$ and $Q$ are equal at $\theta^{(t)}$ if $L$ and $Q$ are differentiable at $\theta^{(t)}$, then $\theta^{(t)}$ must be a stationary point of $L$. The stationary point needs not, however, be a local maximum. In [263] it is shown that it is possible for the algorithm to converge to local minima.

When a measured parameter distribution is derived, the next step is to update the high and low limit values by adjusting the support vector machine (SVM) classifier (Figure 4-25b) in the corresponding functional test specs of the device under test. This process related information allows design re-centering based upon the most failing die-level process monitors (test event, which is obtained with a slightly narrower comparison window), e.g. on the fly test limit setting. Through standard quadratic programming optimization, the input vectors belonging to a priori and a posteriori classes are divided into a number of sub-sets. The quadratic programming problem is solved incrementally, covering all the sub-sets of classes constructing the optimal separating hyperplane for the full data set. Note that during this process the value of the functional vector of parameters is monotonically increasing, since more and more training vectors are considered in the optimization leading to a smaller and smaller separation between the two classes. As illustrated in Figure 4-25b), the high limit value can be updated in the corresponding functional test specs of the device under test with 0.35 LSB , which will lead to the increased yield.


Figure 4-24: a) Estimating mean $\mu$ values of $\lambda, \eta, \gamma$ with respect to the number of iterations of the EM, b) Estimating variance $\sigma$ values of $\lambda, \eta, \gamma$ with respect to the number of iterations of the EM


Figure 4-25: a) Log-likelihood with respect to the number of iterations of the EM, b) Fitting a posteriori probability to the SVM output based on multiple runs of DLPM and DUT measurements

### 4.6.2. Application of Results for A/D Converter Debugging and Calibration

The key to the debugging of the multi-step $\mathrm{A} / \mathrm{D}$ converter is to select and separate the information on the faults from the transfer function. For at-speed testing and debugging of the analog performance of the $\mathrm{A} / \mathrm{D}$ converter it is not only imperative to have all twelve digital outputs and the two out of range signals available at the device pins, but to be able to perform debugging of each stage the output signals of the coarse, mid and fine A/D converters need to be observable too. Debugging of each stage is performed sequentially starting from the first stage. Each stage is tested separately - at a lower speed - enabling the use of standard industrial analog waveform generators. To allow coherent testing, the clock signal of the A/D converter has to be fully controllable by the tester at all times. Adding all these requests together leads to an output test bus that needs to be fourteen bits wide. The connections of the test bus are not only restricted to the test of the analog part. For digital testing the test bus is also used to carry digital data from scan chains. The test-shell contains all functional control logic, the digital test-bus, a test control block (TCB) and a CTAG isolation chain for digital input/output to and from other IP/cores. Further, logic necessary for creating certain control signals for the analog circuit parts, and for the scan-chains a bypass mechanism, controlled by the test control block, is available as well.

In the coarse $\mathrm{A} / \mathrm{D}$ converter, faults in the analog components internal to the converter cause deviation, from ideal, of the transfer function of the coarse A/D converter by changing the step sizes in the transfer function. The fault cases which include resistor value, comparator's offset and comparator's bias current out of specification fault result in different patterns. The number of peaks and the location of the peak data identify the type of fault and the location of the fault. Since there is no feedback from mid and fine A/D converters to the coarse result value, it is not necessary to set these two A/D converters at the fixed value to test coarse $\mathrm{A} / \mathrm{D}$ converter. Calibration $\mathrm{D} / \mathrm{A}$ converter settings do not show in coarse $\mathrm{A} / \mathrm{D}$ converter results; the calibration system however should remain operative. Random calibration cycles are not allowed to prevent interference with test results. The response of the mid A/D converter cannot directly be tested using the normal A/D converter output data due to an overlap in the A/D converter ranges. Nevertheless, by setting the coarse exor output signals using the scan chain through this block, known values are assigned to the mid switch. The residue signals are now used to verify the mid A/D converter separately by observing the mid A/D converter output bits via the test bus.

Faults in mid A/D converter affect the step sizes in the transfer function of the $m$ mid bits, and repeat themselves in all coarse $c$ bits. For the mid A/D converter test the chopper signals required for calibration need to be operative. After completing the mid A/D converter test, the chopper signal have to be verified by setting the chopper input to the two predefined conditions and analyze the mid A/D converter data to verify offsets. Since calibration D/A converter settings do show in mid A/D converter results, the $\mathrm{D} / \mathrm{A}$ converter is set to a known value to prevent interference with mid ADC test results.

Similarly to the mid A/D converter, the fine A/D converter cannot be monitored directly due to the overlap in the A/D converter ranges. Through the available scan chains in the coarse exor and the switch-ladder, control signals are applied to the both mid and fine switch. The predefined input signals are extracted when the A/D converter works in a normal application mode with a normal input signal. At a certain moment the scan chains are set to a hold mode to acquire the requested value. Now, the residue signals derived through the predefined input signals evaluate the fine A/D converter performance. For the fine A/D converter test
the chopper signals need to be active. To verify offsets, a similar procedure as in the mid A/D converter is followed. The calibration $\mathrm{D} / \mathrm{A}$ converter settings have to be known and set to a known value to prevent interference with test results. The digital control block for all three tests operates normally; provides clock pulses, chopper signals and sets the calibration $\mathrm{D} / \mathrm{A}$ converters in a known condition.

To evaluate the proposed algorithms in Section 4.3 and 4.4 consider the test results shown in Table XIV and XV. For each of the three-steps of the A/D converter in Table XIV, different $\lambda, \eta$, and $\gamma$ are generated randomly, so that the relative errors are uniformly distributed in the interval $[-0.1,0.1]$. At first, $\mu$ was set to $1 / 4$ to speed up the algorithm, and then $\mu$ equal to $1 / 64$ after 1000 iteration times to improve the accuracy. Steady state is attained within $\sim 10^{4}$ clock cycles or effectively 0.22 ms (with $\mu=1 / 64$ ).

In Table XV spurious-free dynamic range is employed as a performance matrix. The circuit under test is the three time-interleaved $\mathrm{S} / \mathrm{H}$ before prototyping. Validations have been performed for the entire $\mathrm{S} / \mathrm{H}$ usable signal bandwidth and most probable limitation mechanisms, the time $\sigma_{t}$, offset $\sigma_{\theta}$, bandwidth $\sigma_{b}$, and gain $\sigma_{g}$ variations. The two input frequencies are shown; for both of them, three values for any of the observed error mechanisms are chosen for the evaluation.

The advantage of the proposed method is that it gives unbiased estimates, so that the estimation accuracy can be made arbitrarily good by increasing the amount of estimation data. Although the accuracy increase quite slowly with the amount of data, observed A/D converter, however, use very high sample rates (above $50 \mathrm{MS} / \mathrm{s}$ ) so some million samples are collected in less than second ensuring the very fast converter evaluation.

|  | Actual value | Estimated value |
| :---: | :---: | :---: |
| $\gamma_{1}$ | 0.0229362 | 0.0259427 |
| $\eta_{1}$ | 0.0121342 | 0.0116849 |
| $\lambda_{1}$ | 0.0017936 | 0.0011347 |
| $\gamma_{2}$ | 0.0328464 | 0.0342953 |
| $\eta_{2}$ | 0.0154584 | 0.0142748 |
| $\lambda_{2}$ | 0.0054635 | 0.0052347 |
| $\gamma_{3}$ | 0.0417635 | 0.0424573 |
| $\eta_{3}$ | 0.0173216 | 0.0165324 |
| $\lambda_{3}$ | 0.0093764 | 0.0104636 |


| $f_{\text {in }}[M H z]$ | 21 |  |  | 43 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\sigma_{0}$ [\%] | 0.015 | 0.046 | 0.156 | 0.015 | 0.046 | 0.156 |
| Cal. [dB] | 76.77 | 67.23 | 56.78 | 76.77 | 67.23 | 56.78 |
| Est. [dB] | 77.50 | 67.96 | 57.50 | 77.50 | 67.96 | 57.50 |
| $\sigma_{g}[\%]$ | 0.01 | 0.05 | 0.10 | 0.01 | 0.05 | 0.10 |
| Cal. [dB] | 89.54 | 75.56 | 69.54 | 89.54 | 75.56 | 69.54 |
| Est. [dB] | 89.55 | 75.59 | 69.58 | 89.55 | 75.59 | 69.58 |
| $\sigma_{b}[\%]$ | 0.286 | 1.42 | 2.86 | 0.286 | 1.42 | 2.86 |
| Cal. [dB] | 84.06 | 70.14 | 64.06 | 78.62 | 64.70 | 58.62 |
| Est. [dB] | 83.60 | 70.14 | 64.29 | 78.59 | 64.85 | 58.96 |
| $\sigma_{t}[\%]$ | 0.01 | 0.05 | 0.10 | 0.01 | 0.05 | 0.10 |
| Cal. [dB] | 87.46 | 73.42 | 67.41 | 81.11 | 67.13 | 61.11 |
| Est. [dB] | 86.39 | 73.23 | 67.33 | 80.09 | 66.99 | 61.02 |

TABLE XV - EXAMPLE OF THE CALCULATED AND ESTIMATED VALUES

The most significant A/D converter output bits have a strong correlation to the analog input signal, which is utilized to investigate the signal feedthrough from the output to the input by adding the possibility of scrambling the outgoing digital words with a pseudo-random bitstream. The scrambling is realized by putting XOR gates before each output buffer and applying the random bit to their other input. For unscrambling, the random bits are taken out through an extra package pin.

The calibration technique was verified in all stages with full scale inputs. If the analog input to the calibrated A/D converter is such that the code transition is $i$, then the code transition of the ideal A/D converter is either $i$ or $i+1$. The offset between the digital outputs of these two converters for the range of analog inputs is denoted $\Delta_{i 1}$ and $\Delta_{i 2}$, respectively. If a calibrated $\mathrm{A} / \mathrm{D}$ converter has no errors in the internal reference voltages $\gamma$, and the stage gain errors $\eta$, the difference between the calibrated and the ideal A/D converter outputs is constant regardless of the analog input, thus $\Delta_{i 1}=\Delta_{i 2}$. If errors in the internal reference voltages $\gamma$ and stage gain errors $\eta$ are included, the calibrated A/D converter incurs unique missing codes. The difference between $\Delta_{i 1}$ and $\Delta_{i 2}$ precisely gives the error due to missing codes that occurs when the ideal A/D converter changes from $i$ to $i+1$. In a similar manner the unique error due to missing codes at all other transitions can be measured for the calibrated A/D converter.


Figure 4-26: a) Mean-square error for two thousand samples. The quality criterion adopted for an estimator is the mean-squared error criterion, mainly because it represents the energy in the error signal, is easy to differentiate and provides the possibilities to assign the weights, b) Mean-square error for two million samples

With errors from the missing codes at each measured transition, the calibrated $\mathrm{A} / \mathrm{D}$ converter stage is corrected by shifting the converter's digital output as a function of the transition points such that the overall transfer function of the calibrated A/D converter is free from missing codes. As long as the input is sufficiently rapid to generate a sufficient number of estimates of $\Delta_{i 1}, \Delta_{i 2}$, for all $i$, there is no constraint on the shape of the input signal to the A/D converter.


Figure 4-27: DNL curve a) before calibration, b) after calibration

Constant offset between calibrated and ideal A/D converter appears as a common-mode shift in both $\Delta_{i 1}$ and $\Delta_{i 2}$. Since the number of missing codes at each code transition is measured by subtracting $\Delta_{i 2}$ from $\Delta_{i 1}$, the common mode is eliminated and thus input-referred offsets of calibrated A/D converter have no impact in the calibration scheme (under the practical assumption that the offsets are not large enough to saturate the output of the converter stages). To account for an overall internal reference voltages $\gamma$, stage gain errors $\eta$ and systematic offset $\lambda$, the algorithm provides the estimates with the final values $\left(W^{\prime}\right)^{T}=\left[\gamma^{\prime}, \eta^{\prime}, \lambda^{\prime}\right]$. As ideal A/D converter offers an ideal reference for calibrated A/D converter, the error signal used for the algorithm adaptation (which is formed by the difference of the two A/D converter outputs) is highly correlated with the error between them, thus steady state convergence of occurs within a relatively short time interval.


Figure 4-28: INL curve a) before calibration and b) INL curve after calibration

In Figure 4-26 the correction parameters are shown. The largest correction values significantly decrease with the amount of samples. Calibration results of the mid A/D converter are shown in Figure 4-27 and Figure 4-28. The most of the errors that change quickly between adjacent levels are eliminated; some of the slow varying errors are however still left. This is caused by errors in the estimation of the amplitude distribution; slow variations in the errors cannot be distinguished from variations in the true amplitude distribution since only smoothness is assumed. For a sinusoidal signal the amplitude distribution looks like a bathtub. Because of the bathtub shape with high peaks near the edges the histogram is very sensitive to amplitude changes in the input signal. The estimation is the most accurate for the middle codes. The errors near the edges of the excitation are, however, not completely eliminated due to the amplitude distribution, which has an abrupt change near the edges. Since only the static errors are handled in the algorithm, the errors can be assumed to approximately have a repetitive structure. This can be used to estimate the errors by extrapolation near the edges where the excitation is too low even to estimate the mismatch errors. However, the quality improvement is limited by the extrapolation that does not give perfect result, since the errors are not exactly periodical.

The peak improvement is about $\pm 0.2$ LSB for DNL measurement and $\pm 2.9$ LSB for INL. It is noted that the residual INL errors after calibration shown in Figure 4-28 are due primarily to distortion from the fine A/D converter, as well as distortion from the front-end sample and hold, which sets the best achievable linearity for A/D converter.

### 4.7. Conclusion

The design margins for mixed signal designs depend significantly on process parameters and their distributions across the wafer, within a wafer lot and between wafer lots, which is especially relevant for mismatch. Measurement of these fluctuations is paramount for stable control of transistor properties and statistical monitoring and the evaluation of these effects enables the efficient development of the test patterns and test and debugging methods, as well as ensures good yields. With the use of dedicated sensors [250], which exploit knowledge of the circuit structure and the specific defect mechanisms, the method described in this thesis facilitates early and fast identification of excessive process parameter variation effects at the cost of at maximum $10 \%$ area overhead. The sensors allow the readout of local (within the core) performance parameters as well as the global distribution of these parameters. The flexibility of the concept allows the system to be easily extended with a variety of other performance sensors. The feasibility of the method for on-line and off-line debugging has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal $0.09-\mu \mathrm{m}$ CMOS and evaluated on 12 -bit multi-step A/D converter.

As the number of on-chip sensors is finite due to area limitations, additional informations are obtained through statistical techniques. Instead of using the traditional incomplete-data density in the estimation process, the implemented maximum-likelihood algorithm [264] uses the properties of the complete-data density. In doing so, it can often make the estimation problem more tractable and also yield good estimates of the parameters for small sample sizes.

To allow the test guidance with the information obtained through monitoring process variations several classifiers are considered, such as quadratic, boosting, neural networks, or Bayesian networks. However, implemented adjusted support vector machine classifier [264] is chosen, since it simultaneously minimize the empirical classification error and maximize the geometric margin.

The proposed debugging method [278] is applied after the converter stages and operates on the digital signal provided from the output. Additionally, the method for debugging and analysis of bandwidth mismatch in time-interleaved systems is introduced [291]. The quality criterion adopted for an estimator of the loss function is the mean-squared error criterion, mainly because it represents the energy in the error signal, is easy to differentiate and provides the possibilities to assign the weights. Additionally, employed adaptive filtering algorithm for error estimation offers the small number of operations per iteration and does not require correlation function calculation nor matrix inversions. To control the input to a filter, DfT is necessary, which allows forcing the input signal to the predefined values in each stage. The implemented design-for-test approach [282] permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range allowing full observability and controllability of the device under test. Adding testing capability does not degrade the converter performance and has low impact on area and power consumption. Moreover, the debugging approach is extended to allow foreground calibration of the multi-step A/D converter [300].

## CHAPTER 5.

## CONCLUSIONS AND RECOMMENDATIONS

### 5.1. Summary of Results

With the fast advancement of CMOS fabrication technology, more and more signalprocessing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. The trend of increasing integration level for integrated circuits has forced the A/D converter interface to reside on the same silicon in complex mixed-signal ICs containing mostly digital blocks for DSP and control. However, specifications of the converters in various applications emphasize high dynamic range and low spurious spectral performance. It is nontrivial to achieve this level of linearity in a monolithic environment where post-fabrication component trimming or calibration is cumbersome to implement for certain applications or/and for cost and manufacturability reasons. Additionally, as CMOS integrated circuits are accomplishing unprecedented integration levels, potential problems associated with device scaling - the short-channel effects - are also looming large as technology strides into the deep-submicron regime. The A/D conversion process involves sampling the applied analog input signal and quantizing it to its digital representation by comparing it to reference voltages before further signal processing in subsequent digital systems. Depending on how these functions are combined, different A/D converter architectures can be implemented with different requirements on each function. As discussed in Chapter 2, practical realizations show the trend that to a first order, converter power is directly proportional to sampling rate. However, power dissipation required becomes nonlinear as the speed capabilities of a process technology are pushed to the limit. Pipeline and two-step/multi-step converters tend to be the most efficient at achieving a given resolution and sampling rate specification.

This thesis is in a sense distinctive work as it covers the whole spectrum of design, test, debugging and calibration of multi-step A/D converters; it incorporates development of circuit techniques and algorithms to enhance the resolution and attainable sample rate of an A/D converter and to enhance testing and debugging potential to detect errors dynamically, to isolate and confine faults, and to recover and compensate for the errors continuously.

As presented in Chapter 2, the power proficiency for high resolution of multi-step converter by combining parallelism and calibration and exploiting low-voltage circuit techniques is demonstrated with a $1.8 \mathrm{~V}, 12$-bit, $80 \mathrm{MS} / \mathrm{s}, 100 \mathrm{~mW}$ analog to-digital converter fabricated in five-metal layers $0.18-\mu \mathrm{m}$ CMOS process [37]. Lower power supply voltages significantly reduce noise margins and increase variations in process, device and design parameters. Consequently, it is steadily more difficult to control the fabrication process precisely enough to maintain uniformity. Microscopic particles present in the manufacturing environment and slight variations in the parameters of manufacturing steps can all lead to the geometrical and
electrical properties of an IC to deviate from those generated at the end of the design process. Those defects can cause various types of malfunctioning, depending on the IC topology and the nature of the defect. To relief the burden placed on IC design and manufacturing originated with ever-increasing costs associated with testing and debugging of complex mixed-signal electronic systems, several circuit techniques and algorithms are developed and incorporated in proposed ATPG [187], DfT [219] and BIST [231] methodologies described in Chapter 3.

Process variation cannot be solved by improving manufacturing tolerances; variability must be reduced by new device technology or managed by design in order for scaling to continue. Similarly, within-die performance variation also imposes new challenges for test methods. This subject is treated in detail in Chapter 3 and 4 . With the use of dedicated sensors, which exploit knowledge of the circuit structure and the specific defect mechanisms, the method described in this thesis [250] facilitates early and fast identification of excessive process parameter variation effects. The implemented expectation-maximization algorithm [264] makes the estimation problem more tractable and also yields good estimates of the parameters for small sample sizes. To allow the test guidance with the information obtained through monitoring process variations implemented adjusted support vector machine classifier [264] simultaneously minimize the empirical classification error and maximize the geometric margin.

On a positive note, the use of digital enhancing calibration techniques reduces the need for expensive technologies with special fabrication steps. Indeed, the extra cost of digital processing is normally affordable as the use of submicron mixed signal technologies allows for efficient usage of silicon area even for relatively complex algorithms. Employed adaptive filtering algorithm for error estimation of static [278] and bandwidth [291] errors offers the small number of operations per iteration and does not require correlation function calculation nor matrix inversions. The implemented design-for-test approach [282] permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range allowing full observability and controllability of the device under test. The presented foreground calibration algorithm [300] works with every signal applied to the A/D converter. The feasibility of the method for on-line and off-line debugging and calibration has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal $0.09-\mu \mathrm{m}$ CMOS process.

### 5.2. Original Contribution of This Thesis

The original contributions of this thesis include:

- Analysis of technology limitations on the A/D converters power efficiency.
- Development and analysis of time-interleaved signal processing technique for application in multi-step A/D converters.
- Development and analysis of folding and interpolation signal processing technique for application in multi-step A/D converters.
- Development of an architecture, as well as design and characterization of a 12 -bit multi-step A/D converter using time-interleaved signal processing together with the background calibration technique.
- Development of the test pattern generator for wafer level test to provide a quantitative estimate of the effectiveness and completeness of the testing process.
- Development as well as design and characterization of a design-for-test technique for full observability and controllability without degrading the converter performance and with low impact on area and power consumption.
- Development as well as design and characterization of on-chip sine-wave signal generation for evaluation of $A / D$ converters without large area overhead and with high-level of robustness and digital control capability.
- Development as well as design and characterization of a sensor network to allow early and fast identification of excessive process parameter variation effects.
- Development of algorithms to estimate process parameter variations for small sample sizes and to allow the test guidance while simultaneously minimizing the empirical classification error.
- Development of a fast and adaptive filtering algorithm for error estimation in each stage of multi-step converter.
- Development of a fast and adaptive filtering algorithm for bandwidth error estimation in time-interleaved systems.
- Development and analysis of a foreground calibration technique to calibrate the errors in each stage, without requiring dedicated test signal or part of the conversion time.


### 5.3. Recommendations and Future Research

Even though the resolution of all today's A/D converter architectures is finally limited by jitter in the sampling clock, in low voltage multi-step A/D converters, the practical limitation for the conversion rate and resolution are imposed by full-resolution requirement on the time-interleaved front-end sample-and-hold stage, sub-D/A converter and residue signal. As a result, the design of fast and accurate multi-step A/D converters will become increasingly complex with the technology scaling. On the other hand, technology scaling allows an extensive use of digital signal processing to correct and compensate for the imperfections of the analog circuitry. Whether the evolution of the multi-stage architecture has reached saturation level, or will continue to be one of the dominant architectures of wide-band A/D converters, depends on the balance between these pros and contras of the development of the IC processes.

Similarly, continuous research efforts are made to explore various methods to reduce production test time. Beside the methods based on monitoring on-chip process parameter variation, one effective approach is by increasing the parallel efficiency of testing multiple devices-under-test on one tester e.g. the multi-site testing. Nevertheless, for an A/D converter test, the increasing number of devices-under-test in parallel usually requires more high-quality analog signal sources weakening the gains acquired with multi-site testing. If both converter types are present on the same chip, DAC-ADC loopback combination allows an all-digital test configuration and avoids the need for expensive external analog instrumentation. However, loopback method, suffers from fault masking caused by the uncorrelated interaction between non-functionally related components in loopback mode. In particular, unlike dynamic parameter testing where noise and distortion parameters are additive, static parameters such as INL and DNL tend to cancel, making standard test approaches such as a histogrambased method impractical. Similar to reconstruction and compensation technique, the stimulus error identification and removal (SEIR) algorithm implemented in loopback configuration can estimate linearity of both converters simultaneously without fault masking problems. In an ideal $\mathrm{A} / \mathrm{D}$ converter, the code widths in the code density histogram are equal. Thus, the code density histogram in ideal case is similar to the probability density function (PDF) of the input signal. If the $\mathrm{D} / \mathrm{A}$ converter input is uniformly distributed over all the codes, the $\mathrm{D} / \mathrm{A}$ converter output is uniformly distributed as well; thus, the A/D converter code density histograms can be exploited to calculate ideal histogram. As the last step, the D/A converter linearity estimate can be found from ideal histogram with linear histogram method.

Another possibility to enhance multi-site testing is the possibility of inexpensive on-chip digital waveform generation in its pure or slightly adapted form. As mentioned previously, dynamic parameters of the A/D converter are evaluated through the conventional postprocessing methods, such as histogram or FFT analysis, which exploit sine wave stimulus efficiency, i.e., negligible distortion and highly accurate and stable frequency. Employing similar methods to adapted pulse wave diminish advantages of these methods; spectrum of a pulse wave is distorted with harmonics related to the pulse rise and fall times, making accurate determination of $\mathrm{A} / \mathrm{D}$ converter parametric faults complex and time excessive. The spectral representation of adapted pulse wave is not only a function of sampling frequency and amplitude of the signal, as for sine wave stimuli, but a periodic function of a pulse rise and fall times as well. Additionally, the amplitudes of the expansion coefficients fall have the form of $\sin x / x$ with a slope of $-20 \mathrm{~dB} /$ decade demonstrating low-pass behavior. However, the two algorithms in [302] based on time-modulo reconstruction methods [303] simultaneously relieve the accuracy requirement of excitation source in line with recent efforts and offer possibilities for characterization of analog-to-digital converter error mechanisms as a consequence of parametric faults. Additionally, the reconstructed waveform shows errors of the A/D converter more visibly and intuitively [303].

## APPENDIX

## A.1. Time Mismatch

Let the original sampled data sequence $S=\left[x\left(t_{0}\right), x\left(t_{1}\right), x\left(t_{2}\right), \ldots, x\left(t_{m}\right), \ldots, x\left(t_{N}\right), x\left(t_{N+1}\right), \ldots\right]$ be divided into $N$ subsequences $S_{0}, S_{1}, S_{2}, \ldots, S_{N-1}$ as follows [115]:
$S_{0}=\left[x\left(t_{0}\right), x\left(t_{N}\right), x\left(t_{2 N}\right), \ldots\right]$
:
$S_{n}=\left[x\left(t_{n}\right), x\left(t_{N+n}\right), x\left(t_{2 N+n}\right), \ldots\right]$
!
$S_{N}=\left[x\left(t_{N-1}\right), x\left(t_{2 N-1}\right), x\left(t_{3 N-1}\right), \ldots\right.$

The $S_{n}$ is obtained by uniformly sampling the signal $x\left(t+t_{n}\right)$ at the rate $1 / N T$. Assume
$\overline{S_{n}}=\left[x\left(t_{n}\right), 0,0, \ldots(N-1 \quad z \operatorname{eros}), x\left(t_{N+n}\right), 0,0, \ldots\right]$
the original sequence $S$, can be represented as
$S=\sum_{n=0}^{N-1} \overline{S_{n}} z^{-n}$

Then, the digital spectrum, $X(\omega)$, of $S$ can be represented as
$X(\omega)=\frac{1}{N T} \sum_{n=0}^{N-1}\left[\sum_{k=-\infty}^{\infty} X^{a}\left(\omega-\frac{2 \pi k}{N T}\right) e^{j\left[\omega-(2 \pi k / N T) \mid \times t_{n}\right.}\right] \times e^{-j n \omega T}$

Let $r_{n} T, n=0,1, N-1$ be the sampling time offset encountered at the $n^{t h}$ sample-hold unit (positive $r_{n}$ means that the $n^{t h}$ sample is delayed), and $t_{n}$ real sampling time for $n^{t h}$ samplehold unit,
$r_{n} T=n T-t_{n}$
then (A-4) can be rewritten as
$X(\omega)=\frac{1}{T} \sum_{k=-\infty}^{\infty}\left[\sum_{n=0}^{N-1} \frac{1}{N} e^{-j\left(\omega-k \frac{2 \pi}{N T}\right)_{n} T} e^{-j k n \frac{2 \pi}{N}}\right] \times X^{a}\left(\omega-\frac{2 \pi k}{N T}\right)$

For a given sine wave $x(t)=\sin \left(\omega_{i j} t\right)$, the Fourier transform $X^{a}(\omega)$ is given by
$X^{a}(\omega)=j \pi\left[\delta\left(\omega+\omega_{\text {in }}\right)-\delta\left(\omega-\omega_{i n}\right)\right]$
where $\boldsymbol{\delta}$ is unit sample sequence $\boldsymbol{\delta}[x]=1$ at $x=0$, and 0 elsewhere, (A- 6 ) becomes [115]
$X(\omega)=\frac{1}{T} \sum_{k=-\infty}^{\infty}\left[A(k) j \pi\left(\delta\left(\omega+\omega_{i n}-k \frac{2 \pi}{N T}\right)-\delta\left(\omega-\omega_{i n}-k \frac{2 \pi}{N T}\right)\right)\right]$
where
$A(k)=\sum_{n=0}^{N-1}\left(\frac{1}{N} e^{-j r_{n} 2 \pi f_{n} / f_{s}}\right) e^{-j k k(2 \pi / N)}$

The digital spectrum given by (A-8) has $N$ pairs of line spectra, each pairs centered at the fractional of the sampling frequency, such as $f_{s} / N, \ldots,(N-1) f_{s} / N$.

Fundamental corresponds to $k=0$ while $k=1, \ldots N-1$ corresponds to the distortion. The signal amplitude is determined by $A(0)$ while the distortion amplitudes are determined by $A(n), n=1, \ldots, N-1 . A(k)$ is a DFT of the sequence of $\left[(1 / N) e^{-j r_{n} 2 \pi f_{0} / f_{s}}, n=0,1,2, \ldots, N-1\right]$.

Assuming $r_{n} 2 \pi f_{i n} / f_{s}<1$, the magnitude of the sidebands components can be expressed as:

$$
\begin{align*}
& \left|A(k)=\sum_{n=0}^{N-1}\left(e^{-j r_{n} 2 \pi f_{i n} / f_{s}}\right) e^{-j k k(2 \pi / N)}\right| \approx\left|\frac{1}{N} \sum_{n=0}^{N-1}\left(1-j 2 \pi r_{n} f_{i n} / f_{s}\right) e^{-j k n(2 \pi / N)}\right| \\
& =\left\{\begin{array}{l}
\frac{2 \pi f_{i n}}{N f_{s}}\left|\sum_{n=0}^{N-1} r_{n} n_{n}-j k n(2 \pi / N)\right| \quad \text { for } k \neq 0, \pm N \\
\left.1-\left(j 2 \pi f_{i n} / f_{s}\right)\left(\frac{1}{N} \sum_{n=0}^{N-1} r_{n}\right) \right\rvert\,=1 \text { for } k=0, \pm N
\end{array}\right. \tag{A-10}
\end{align*}
$$

The signal power is $A^{2} / 2$ and power density of a spurious due to the time mismatch is expressed as
$P_{r}^{\text {pher }}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1}\left(1-j 2 \pi r_{n} f_{i n} / f_{s}\right) e^{-j k n(2 \pi / N)}\right|^{2}=\frac{A^{2} 4 \pi^{2} f_{i n}^{2}}{2 N^{2} f_{s}^{2}} \sigma_{r}^{2}$

## A.2. Offset Mismatch

The offset mismatch can be modeled by adding a $d c$ level with the input signal that is unique for each $\mathrm{S} / \mathrm{H}$ unit. For a input signal $A \sin \left(\omega_{i n} t\right)+d_{n}$ with $n=0, \ldots, N-1$, the Fourier transform is given by
$X^{a}(\omega)=j \pi A\left[\delta\left(\omega+\omega_{i n}\right)-\delta\left(\omega-\omega_{i n}\right)\right]+2 \pi d_{n} \delta(\omega)$

If no timing error is assumed $\mathrm{r}_{\mathrm{n}}$ is zero. Substituting previous equation in (A-8),
$X(\omega)=\frac{1}{T} \sum_{k=-\infty}^{\infty} A j \pi \delta\left[\left(\omega+\omega_{i n}-\frac{2 \pi k}{N T}\right)-\left(\omega-\omega_{i n}-\frac{2 \pi k}{N T}\right)\right]+\frac{1}{T} \sum_{k=-\infty}^{\infty} A(k) 2 \pi \delta\left(\omega-\frac{2 \pi k}{N T}\right)$
where
$A(k)=\frac{1}{N} \sum_{n=0}^{N-1} d_{n} e^{-j k n(2 \pi / N)}$
The first term of (A-12) corresponds to the input signal, while the second term corresponds to the distortion caused by channel offset. The distortion is not signal dependent and appears at $n f_{s} / N$, where $n=0,1, \ldots, N-1$. From previous equation can be seen that the distortion consists of a sum of impulses. Each impulse corresponds to a complex exponential signal in the time domain $e^{j \omega}$. The power of the exponential signal is 1 . The factors $A(k)$ can be seen as the DFT of the sequence $d_{n} / N, n=0,1, \ldots, N-1$. Power density of a spurious due to the offset mismatch is expressed as
$P_{r}^{\text {spur }}(k)=\left.\left.\frac{1}{N^{2}}\right|_{n=0} ^{N-1} d_{n} e^{-j k r(2 \pi / N)}\right|^{2}=\frac{1}{N^{2}} \sigma_{d}^{2}$

## A.3. Gain Mismatch

To model gain mismatch, magnitude of one of the $\mathrm{S} / \mathrm{H}$ unit input signals is different. The largest difference occurs at the peaks of the sine wave. The signal is $a_{n} \sin \left(\omega_{i n} t\right)$ with $n=0, \ldots, N-1$. The Fourier transform is given by
$X^{a}(\omega)=j \pi a_{n}\left[\delta\left(\omega+\omega_{i n}\right)-\delta\left(\omega-\omega_{i n}\right)\right]$
If no timing error is assumed $r_{n}$ is zero. Substituting previous equation in (A-8),
$X(\omega)=\frac{1}{T} \sum_{k=-\infty}^{\infty}\left[A(k) j \pi\left(\delta\left(\omega+\omega_{i n}-k \frac{2 \pi}{N T}\right)-\delta\left(\omega-\omega_{i n}-k \frac{2 \pi}{N T}\right)\right)\right]$
where
$A(k)=\frac{1}{N} \sum_{n=0}^{N-1} a_{n} e^{-j k k(2 \pi / N)}$
for the gain mismatches in $N S / H$ units with spurious tones at $f_{s} / N \pm f_{i p}, 2 f_{s} / N \pm f_{i p}, \ldots,(N-$ 1) $f_{s} / N \pm f_{i n}$. Power density of a spurious due to the gain mismatch is expressed as

$$
\begin{equation*}
P_{r}^{\text {spur }}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1} a_{n} e^{-j k n(2 \pi / N)}\right|^{2}=\frac{A^{2}}{2 N^{2}} \sigma_{a}^{2} \tag{A-19}
\end{equation*}
$$

## A.4. Bandwidth Mismatch

To model frequency dependent bandwidth mismatch, the S/H Amplifiers are approximated as the ideal one-pole amplifiers. For a one-pole system, $A(s)=A_{0} /\left(1+s / \omega_{0}\right)$, the closed loop transfer function is
$\frac{V_{\text {out }}}{V_{\text {in }}}(s)=\frac{A(s)}{1+A(s) \beta}=\frac{A_{0}}{1+A_{0} \beta+\frac{s}{\omega_{0}}}=\frac{\frac{A_{0}}{1+A_{0} \beta}}{1+\frac{s}{\left(1+A_{0} \beta\right) \omega_{0}}}$

Recognizing that $A_{0} \beta » 1$, the previous equation becomes
$\frac{V_{\text {out }}}{V_{\text {in }}}(s)=\frac{1 / \beta}{1+\frac{s}{\beta A_{0} \omega_{0}}}=\frac{1 / \beta}{1+j \frac{f_{\text {in }}}{\beta A_{0} f_{0}}}=\frac{1}{1+j \frac{f_{\text {in }}}{f_{1}}} \approx 1-j \frac{f_{\text {in }}}{f_{1}}=b_{n}$
for $\beta=1$. For a given sine wave $x(t)=\sin \left(\omega_{i n} t\right)$, the Fourier transform $X^{a}(\omega)$ is given by
$X^{a}(\omega)=j \pi\left[\delta\left(\omega+\omega_{i n}\right)-\delta\left(\omega-\omega_{i n}\right)\right]$
and equation (A-8) with $r_{n}=0$ becomes
$X(\omega)=\frac{1}{T} \sum_{k=-\infty}^{\infty}\left[A(k) j \pi\left(\delta\left(\omega+\omega_{i n}-k \frac{2 \pi}{N T}\right)-\delta\left(\omega-\omega_{i n}-k \frac{2 \pi}{N T}\right)\right)\right]$
where
$A(k)=\frac{1}{N} \sum_{n=0}^{N-1} b_{n} e^{-j k n(2 \pi / N)}$
with $f_{1}$ unity-gain frequency and $b_{n}$ bandwidth offset experienced by the $n^{\text {th }} \mathrm{S} / \mathrm{H}$ amplifier with spurious tones at $f_{s} / N \pm f_{i,}, 2 f_{s} / N \pm f_{i,}, \ldots,(N-1) f_{s} / N \pm f_{i n}$. The signal power is $A^{2} / 2$ and power density of a spurious due to the gain-bandwidth mismatch is expressed as

$$
\begin{equation*}
P_{r}^{\text {spur }}(k)=\frac{A^{2}}{2 N^{2}}\left|\sum_{n=0}^{N-1} b_{n} e^{-j k n(2 \pi / N)}\right|^{2}=\frac{A^{2} f_{i n}^{2}}{2 N^{2} f_{1}^{2}} \sigma_{b}^{2} \tag{A-25}
\end{equation*}
$$

## A.5. General Expression

The general expression for spurious-free dynamic range (SFDR) is given by

$$
\begin{array}{lll}
S F D R=10 \log _{10}\left(P_{s} / P_{\text {spur }}\right)=10 \log _{10}\left(N^{2} \lambda_{x}\right) & \lambda_{\text {off }}=A^{2} / 2 \sigma_{d}^{2} & \lambda_{\text {time }}=\left(f_{s} /\left(2 f_{\text {in }}\right)\right)^{2} /\left(\pi^{2} \sigma_{r}^{2}\right)  \tag{A-26}\\
\lambda_{\text {gain }}=1 / \sigma_{a}^{2} & \lambda_{\text {bandudidth }}=\left(f_{1} / f_{\text {in }}\right)^{2} /\left(\sigma_{b}^{2}\right)
\end{array}
$$

where the input signal power is defined as $P_{s}=A^{2} / 2$.

## B.1. Histogram Measurement of ADC Nonlinearities Using Sine Waves

The histogram or output code density is the number of times every individual code has occurred. For an ideal A/D converter with a full scale ramp input and random sampling, an equal number of codes is expected in each bin. The number of counts in the $i$ th bin $H(i)$ divided by the total number of samples $N_{0}$, is the width of the bin as a fraction of full scale. By compiling a cumulative histogram, the cumulative bin widths are the transition levels.

The use of sine wave histogram tests for the determination of the nonlinearities of ana-log-to-digital converters (ADC's) has become quite common and is described in [285] and [304]. When a ramp or triangle wave is used for histogram tests (as in [305]), additive noise has no effect on the results; however, due to the distortion or nonlinearity in the ramp, it is difficult to guarantee the accuracy.

For a differential nonlinearity test, a one percent change in the slope of the ramp would change the expected number of, codes by one percent. Since these errors would quickly accumulate, the integral nonlinearity test would become unfeasible. From brief consideration it is clear that the input source should have better precision than the converter being tested. When a sine wave is used, an error is produced, which becomes larger near the peaks. However, this error can be made as small and desired by sufficiently overdriving the $\mathrm{A} / \mathrm{D}$ converter.

The probability density $p(V)$ for a function of the form $A \sin \omega t$ is

$$
\begin{equation*}
p(V)=\frac{1}{\pi \sqrt{A^{2}-V^{2}}} \tag{A-27}
\end{equation*}
$$

Integrating this density with respect to voltage gives the distribution function $P\left(V_{b}, V_{b}\right)$

$$
\begin{equation*}
P\left(V_{a}, V_{b}\right)=\frac{1}{\pi}\left\{\sin ^{-1}\left[\frac{V_{b}}{A}\right]-\sin ^{-1}\left[\frac{V_{a}}{A}\right]\right\} \tag{A-28}
\end{equation*}
$$

which is in essence, the probability of a sample being in the range $V_{a}$ to $V_{b}$. If the input has a $d c$ offset, it has the form $V_{0}+A \sin \omega t$ with density

$$
\begin{equation*}
p(V)=\frac{1}{\pi \sqrt{A^{2}-\left(V-V_{o}\right)^{2}}} \tag{A-29}
\end{equation*}
$$

The new distribution is shifted by $V_{o}$ as expected

$$
\begin{equation*}
P\left(V_{a}, V_{b}\right)=\frac{1}{\pi}\left\{\sin ^{-1}\left[\frac{V_{b}-V_{o}}{A}\right]-\sin ^{-1}\left[\frac{V_{a}-V_{o}}{A}\right]\right\} \tag{A-30}
\end{equation*}
$$

The statistically correct method to measure the nonlinearities is to estimate the transitions from the data. The ratio of bin width to the ideal bin width $P(i)$ is the differential linearity and should be unity.

Subtracting on LSB gives the differential nonlinearity in LSB's
$D N L(i)=\frac{H(i) / N_{t}}{P(i)}-1$

Replacing the function $P\left(V_{o}, V_{b}\right)$ by the measured frequency of occurrence $H / N_{b}$, taking the cosine of both sides of (A-30) and solving for $\hat{V}_{b}$, which is an estimate of $V_{b}$, and using the following identities
$\cos (\alpha-\beta)=\cos (\alpha) \cos (\beta)+\sin (\alpha) \sin (\beta)$
$\cos \left(\sin ^{-1} \frac{V}{A}\right)=\frac{\sqrt{A^{2}-V^{2}}}{A}$
yields to
$\hat{V}_{b}^{2}-\left(2 V_{a} \cos \left(\frac{\pi H}{N_{t}}\right)\right) \hat{V}_{b}-A^{2}\left(1-\cos ^{2}\left(\frac{\pi H}{N_{t}}\right)\right)+V_{a}^{2}=0$

In this consideration, the offset $V_{o}$ is eliminated, since it does not effect the integral or differential nonlinearity. Solving for $\hat{V}_{b}$ and using the positive square root term as a solution so that $\hat{V}_{b}$ is greater than $V_{a}$
$\hat{V}_{b}=V_{a} \cos \left(\frac{\pi H}{N_{t}}\right)+\sin \left(\frac{\pi H}{N_{t}}\right) \sqrt{A^{2}-V_{a}^{2}}$

This gives $\hat{V}_{b}$ in terms of $V_{a} \cdot \hat{V}_{k}$ can be computed directly by using the boundary condition $V_{0}=-A$ and using
$C H(k)=\sum_{i=0}^{k} H(i)$
the estimate of the transition level $\hat{V}_{b}$ denoted as a $T_{k}$ can be expressed as
$T_{k}=-A \cos \left(\pi \frac{C H_{k-1}}{N_{t}}\right), \quad k=1, \ldots, N-1$
$A$ is not known, but being a linear factor, all transitions can be normalized to $A$ so that the full range of transitions is $\pm 1$.

## B.2. Mean Square Error

As the probability density function associated with the input stimulus is known, the estimators of the actual transition level $T_{k}$ and of the corresponding $\mathrm{INL}_{k}$ value expressed in least significant bits (LSBs) are represented as random variables defined, respectively, for a coherently sampled sinewave
$s[m]=d+A \sin \left(2 \pi \frac{D}{M} m+\theta_{0}\right) \quad m=0,1, \ldots, M-1$
$T_{k}=d-A \cos \left(\pi \frac{C H_{k}}{M}\right), \quad k=1, \ldots, N-1 \quad \quad I N L_{k}=\left(T_{k}-T_{k}^{i}\right) / \Delta \quad k=1, \ldots, N-1(\mathrm{~A}-39)$
where $A, d, \theta_{0}$ are the signal amplitude, offset and initial phase, respectively, $M$ is the number of collected data, $D / M$ represents the ratio of the sinewave over the sampling frequencies. $T_{k}^{i}$ is the ideal $k$ th transition voltage, and $\Delta=F S R / 2^{B}$ is the ideal code-bin width of the ADC under test, which has a full-scale range equal to FSR. A common model employed for the analysis of an analog-to digital converter affected by integral nonlinearities describes the quantization error $\varepsilon$ as the sum of the quantization error of a uniform quantizer $\varepsilon_{q}$ and the nonlinear behavior of the considered converter $\varepsilon_{n}$. For simplicity assuming that $\left|I N L_{k}\right|<\Delta / 2$, we have:
$\varepsilon_{n}=\sum_{k=1}^{N-1} \Delta \operatorname{sgn}\left(I N L_{k}\right) i\left(s \in I_{k}\right)$
where $\operatorname{sgn}($.$) and i($ (.) represent the sign and the indicator functions, respectively, $s$ denotes converter stimulus signal and the non-overlapping intervals $I_{k}$ are defined as

$$
I_{k} \hat{=} \hat{l} \begin{array}{ll}
\left(T_{k}^{i}-I N L_{k}, T_{k}^{i}\right), & I N L_{k}>0  \tag{A-41}\\
\left(T_{k}^{i}, T_{k}^{i}-I N L_{k}\right), & I N L_{k}<0
\end{array}
$$

The nonlinear quantizer mean-square-error, evaluated under the assumption of uniform stimulation of all converter output codes, is given by

$$
\begin{equation*}
m s e=\int_{-\infty}^{\infty}\left[\varepsilon_{q}(s)+\varepsilon_{n}(s)\right]^{2} f_{s}(s) d s \tag{A-42}
\end{equation*}
$$

where $f_{s}$ represent $P D F$ of converter stimulus. Stimulating all device output codes with equal probability requires that

$$
\begin{equation*}
f_{s}(s)=\frac{1}{V_{M}-V_{m}} \cdot i\left(V_{m} \leq s<V_{M}\right) \tag{A-43}
\end{equation*}
$$

Thus, mse becomes

$$
\begin{equation*}
m s e=\frac{1}{V_{M}-V_{m}} \int_{V_{m}}^{V_{M}}\left[\varepsilon_{q}^{2}(s)+2 \varepsilon_{q}(s) \varepsilon_{n}(s)+\varepsilon_{n}^{2}(s)\right] d s \tag{A-44}
\end{equation*}
$$

Assuming $\Delta=\left(V_{M}-V_{m}\right) / N$, and exploiting the fact the mse associated with the uniform quantization error sequence is $\Delta^{2} / 12$

$$
\begin{equation*}
m s e=\frac{\Delta^{2}}{12}+\frac{1}{N \Delta} \sum_{k=1}^{N-1} \int_{I_{k}}\left[2 \Delta \operatorname{sgn}\left(I N L_{k}\right) \varepsilon_{q}(s)+\Delta^{2}\right] d s \tag{A-45}
\end{equation*}
$$

Since, for a rounding quantizer, $\varepsilon_{q}(s)=\Delta / 2-\Delta(s / \Delta-1 / 2)$, it can be verified that $\operatorname{sgn}\left(I N L_{k}\right)$ $\cdot \varepsilon_{q}(s)<0$, so that

$$
\begin{equation*}
\text { mse }=\frac{\Delta^{2}}{12}+\frac{1}{N} \sum_{k=1}^{N-1} I N L_{k}^{2} \tag{A-46}
\end{equation*}
$$

When characterizing A/D converters the SINAD is more frequently used than the mse. The SINAD is defined as

$$
\begin{equation*}
S I N A D=20 \log _{10} \frac{r m s_{(\text {signal })}}{r m s_{(\text {noise })}}[d B] \tag{A-47}
\end{equation*}
$$

Let the amplitude of the input signal be $A_{d B F S}$, expressed in $d B$ relative full scale. Hence, the rms value is then

$$
\begin{equation*}
r m s_{(\text {signal })}=\frac{\Delta 10^{\frac{A_{d B F S}}{20}} 2^{b-1}}{\sqrt{2}} \tag{A-48}
\end{equation*}
$$

The $r m s_{s_{\text {(rasis) }}}$ amplitude is obtained from the mse expression above so that

$$
r m s_{(\text {noise })}=\sqrt{m s e} \quad S I N A D_{I N L}=20 b \log _{10} 2+10 \log _{10} \frac{3}{2}+A_{d B F S}-10 \log _{10}\left(\frac{m s e}{\Delta^{2} / 12}\right)[d B] \text { (A-49) }
$$

To calculate the effective number of bits $E N O B$, firstly express the $S I N A D$ for an ideal uniform ADC and than solve for $b$

$$
\begin{align*}
& \operatorname{SINAD}_{(\text {ideal })}=20 \log _{10}\left(\frac{\sqrt{6} A 2^{b}}{F S R}\right) \\
& E N O B=\frac{\log _{2} 10}{20} \operatorname{SINAD}+\log _{2} \frac{F S R}{\sqrt{6} A} \tag{A-50}
\end{align*}
$$

Letting the amplitude $A=10^{4(A B F 5) / 20} \mathrm{FSR} / 2$, and incorporating above equation, the ENOB can be expressed as

$$
\begin{equation*}
E N O B_{I N L}=b-\frac{1}{2} \log _{2}\left(\frac{m s e}{\Delta^{2} / 12}\right)[d B] \tag{A-51}
\end{equation*}
$$

## B.3. Measurement Uncertainty

To estimate the uncertainty on the DNL and INL it is necessary to know the probability distribution of the cumulative probability $Q_{i}$ to realize a measurement $V<U B_{i}$, with $U B_{i}$ the uperbound of the $i$ th level

$$
\begin{equation*}
Q_{i}=P\left(V<U B_{i}\right)=\int_{V_{o}-V}^{U B_{i}} p(V) d V \tag{A-52}
\end{equation*}
$$

and using linear transformation

$$
\begin{equation*}
U B_{i}=-\cos \pi Q_{i} \tag{A-53}
\end{equation*}
$$

The variance and cross-correlation of $U B_{i}$ is derived using linear approximations. To realize the value $Q_{i}$, it is necessary to have $N_{i}$ measurements with a value $<U B_{i}$ and ( $N$ $N_{i}$ ) measurements with a value $>U B_{i}$. The distribution of $Q_{i}$ is a binomial distribution, which can be very well approximated by a normal distribution [285]

$$
\begin{align*}
P\left(Q_{i}^{\prime}\right) & =C_{N}^{N_{i}} P\left(V<U B_{i}\right)^{N_{i}}\left(1-P\left(V>U B_{i}\right)^{N-N_{i}}\right.  \tag{A-54}\\
& =C_{N}^{N_{i}} Q_{i}^{N_{i}}\left(1-Q_{i}\right)^{N-N_{i}}
\end{align*}
$$

with $Q_{i}^{\prime}$ the estimated value of $Q_{i}$. The mean and the standard deviation is given by

$$
\begin{equation*}
\mu_{Q_{i}^{\prime}}=Q_{i} \quad \sigma_{Q_{i}^{\prime}}=\sqrt{Q_{i}\left(1-Q_{i}\right) / N} \tag{A-55}
\end{equation*}
$$

which states that $Q_{i}^{\prime}$ is an unbiased estimate of $Q_{i}$. To calculate the covariance between $Q_{i}$ and $Q_{p}$ firstly, let's define
$Q_{0}=P\left(V>U B_{j}\right)$
$Q_{i j}=P\left(U B_{i}<V<U B_{j}\right)=1-Q_{i}-Q_{j}$
and the relation
$N_{j}=N_{i}+N_{i j}$
$N_{i}+N_{i j}+N_{0}=N$

$$
\begin{align*}
& \sigma_{N_{i} N_{j}}^{2}=\sigma_{N_{i}}^{2}+\sigma_{N_{i} N_{i j}}^{2}  \tag{A-57}\\
& \sigma_{N_{0}}^{2}=\sigma_{N_{i}}^{2}+\sigma_{N_{i j}}^{2}+2 \sigma_{N_{i} N_{i j}}^{2}
\end{align*}
$$

which leads to
$\sigma_{N_{i} N_{j}}^{2}=\left[\sigma_{N_{i}}^{2}+\sigma_{N_{0}}^{2}-\sigma_{N_{i j}}^{2}\right] / 2$
with

$$
\begin{align*}
\sigma_{N_{i}}^{2} & =N Q_{i}\left(1-Q_{i}\right) \\
\sigma_{N_{0}}^{2} & =N Q_{0}\left(1-Q_{0}\right)  \tag{A-59}\\
\sigma_{N_{i j}}^{2} & =N Q_{i j}\left(1-Q_{i j}\right)
\end{align*}
$$

or
$\begin{aligned} \sigma_{N_{i N}}^{2} & =N Q_{i} Q_{0}=N Q_{i}\left(1-Q_{j}\right) \\ \sigma_{Q_{i} Q_{j}}^{2} & =Q_{i}\left(1-Q_{j}\right) / N\end{aligned}$

To calculate the variance $\sigma_{U B}{ }^{2}$
$\sigma_{U B_{i}}^{2}=E\left[d U B_{i} d U B_{i}\right]=\pi^{2} \sin ^{2} \pi Q_{i} \sigma_{Q_{i}}^{2}=\pi^{2} \sin ^{2} \pi Q_{i} Q_{i}\left(1-Q_{i}\right) / N$

Similarly,
$\sigma_{U B_{i} U B_{j}}^{2}=E\left[d U B_{i} d U B_{j}\right]=\pi^{2} \sin \pi Q_{i} \sin \pi Q_{j} Q_{i}\left(1-Q_{j}\right) / N$

Since the differential nonlinearity of the $i$ th level is defined as the ratio

$$
\begin{equation*}
D N L_{i}=\frac{U B_{i}-U B_{i-1}}{L_{R}}-1 \tag{A-63}
\end{equation*}
$$

where $L_{R}$ is the length of the record, the uncertainty in $D N L_{i}$ and $I N L_{i}$ measurements can be expressed as

$$
\begin{align*}
& \sigma_{D N L_{i}}^{2}=\sqrt{\left[\sigma_{U B_{i}}^{2}+\sigma_{U B_{i-1}}^{2}-2 \sigma_{U B_{i} U B_{j}}^{2}\right]} / L_{R}  \tag{A-64}\\
& \sigma_{I N L_{i}}^{2}=\sigma_{U B_{i}} / L_{R}
\end{align*}
$$

The maximal uncertainty occurs for $Q_{i}=0.5$, thus the previous equation can be approximated with

$$
\begin{align*}
\sigma_{D N L_{i}}^{2} & \approx \sqrt{\pi / L_{R}} \times 1 / \sqrt{N}  \tag{A-65}\\
\sigma_{I N L_{i}}^{2} & =\pi / 2 L_{R} \times 1 / \sqrt{N}
\end{align*}
$$

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## Scientific Journals and Conferences Contributions as Appeared in This Thesis:

1. A. Zjajo, "Influence of Parametric Variations on Design of Multi-Step A/D Converters", Process Variability Workshop, IEEE Design, Automation and Test in Europe Conference, 2009, invited
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1. (Patent WO/2005/684289) "Apparatus For and Method of Implementing Time-Interleaved Architecture", Koninklijke Philips Electronics N.V., February 2005
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3. (Patent WO/2007/049210) "Analog IC Having Test Arrangement and Test Method for Such an IC", NXP B.V., May 2007
4. (Patent EP/2008/680744157) "Built-In Self-Test Apparatus and Method for Digital-to-Analog Converter", NXP B.V., January 2008
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6. (Patent WO/2008/125998) "Analog Circuit Testing and Test Pattern Generation", NXP B.V., October 2008
7. (Patent WO/2008/135917) "IC Testing Methods and Apparatus", NXP B.V., November 2008
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## SUMMARY

In general terms, the analog-to-digital (A/D) conversion process involves sampling the applied analog input signal and quantizing it to its digital representation, by comparing it to reference voltages before further signal processing in subsequent digital systems. Depending on how these functions are combined, different A/D converter architectures can be implemented with different requirements on each function. Practical realizations show the trend that, to a first order, converter power is directly proportional to the sampling rate. However, power dissipation required becomes nonlinear as the speed capabilities of a process technology are pushed to the limit. Pipeline and two-step/multistep converters tend to be the most efficient at achieving a given resolution and sampling rate specification.

This thesis is distinctive work as it covers the whole spectrum of design, test, debugging and calibration of multi-step A/D converters; it incorporates development of circuit techniques and algorithms to enhance the resolution and attainable sample rate of an A/D converter and to enhance testing and debugging potential to detect errors dynamically, to isolate and confine faults, and to recover and compensate for the errors continuously. The power proficiency for high resolution of multi-step converters by combining parallelism and calibration and exploiting low-voltage circuit techniques is demonstrated with a $1.8 \mathrm{~V}, 12$-bit, $80 \mathrm{MS} / \mathrm{s}, 100 \mathrm{~mW}$ analog to-digital converter [37] fabricated in five-metal layers $0.18-\mu \mathrm{m}$ CMOS process.

To relief the burden placed on IC design and manufacturing originated with everincreasing costs associated with testing and debugging of complex mixed-signal electronic systems, several circuit techniques and algorithms are developed and incorporated in proposed ATPG [187], DfT [219] and BIST [231] methodologies.

ATPG incorporates test pattern generation for wafer level test, thereby providing a quantitative estimate of the effectiveness and completeness of the testing process. With the Karhunen-Loève expansion method hereby proposed [187], the parameters of the transistors are modeled as stochastic processes over the spatial domain of a die, thus making parameters of any two devices on the die, two different correlated random variables. The bounds on the circuit response are calculated by performing a mathematical evaluation of the performance function attributes against physical tolerance limits defined by device mismatch yielding the significant CPU-time savings. The proposed Ney-man-Person statistical detector [207], which is a special case of the Bayes test, provides a workable solution when the a priori probabilities are unknown, or the Bayes risk is difficult to evaluate or set objectively. The tests are generated and evaluated taking into account the potential fault masking effects of process spread on the faulty circuit responses. To overcome system-test limitations of the structural current-based testing, the device-under-test is partitioned into smaller blocks with only limited additional hardware
by means of the power-scan DfT technique [219]. As the results of test pattern generator indicate, most quasi-static failures in various blocks of the twelve-bit two-step/multi-step A/D converter, depending on the degree of partitioning, are detectable through powersupply current structural test offering more then twenty fold reduction in test time in comparison to more traditional, functional histogram-based static or FFT-based dynamic A/D converter test. Besides ATPG and DfT, BIST approaches are similarly an efficient way to help decrease the test development and debugging costs. The BIST method and sine-wave signal generation proposed in this thesis rely on the programmable integrator, which allows continuous-time periodic analog signal generation [231]. The method has been evaluated on the prototype fabricated in $0.065-\mu \mathrm{m}$ CMOS and has the attributes of digital programming and control capability, robustness and low area overhead.

Measurement of process parameters fluctuations is paramount for stable control of transistor properties, and statistical monitoring and the evaluation of these effects enables the efficient development of the test patterns and test and debugging methods, as well as ensures good yields. With the use of dedicated sensors, which exploit knowledge of the circuit structure and the specific defect mechanisms, the method described in this thesis facilitates early and fast identification of excessive process parameter variation effects at the cost of at maximum $10 \%$ area overhead. As the number of on-chip sensors is finite due to area limitations, additional informations are obtained through statistical techniques. The implemented expectation-maximization algorithm [264] makes the estimation problem more tractable and also yields good estimates of the parameters for small sample sizes. To allow test guidance with the information obtained through monitoring process variations, the implemented adjusted support vector machine classifier [264] simultaneously minimizes the empirical classification error and maximizes the geometric margin.

The proposed debugging method [278] is applied after the converter stages and operates on the digital signal provided from the output. The feasibility of the method for on-line and off-line debugging and calibration has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal $0.09-\mu \mathrm{m}$ CMOS and evaluated on 12-bit multi-step A/D converter. Additionally, a debugging method for bandwidth mismatch in time-interleaved systems is introduced [291]. The employed adaptive filtering algorithm for error estimation offers a small number of operations per iteration and does not require correlation function calculation nor matrix inversions. To control the input to a filter, DfT is necessary, which allows forcing the input signals to the predefined values in each stage. The implemented design-for-test approach [282] permits circuit re-configuration in such a way that all sub-blocks are tested for their full input range allowing full observability and controllability of the device under test. Adding testing capability does not degrade the converter performance and has low impact on area and power consumption. Moreover, the debugging approach is extended to allow foreground calibration of the multi-step A/D converter [300].

## SAMENVATTING

In algemene termen bestaat het analoog-digitaal-conversieproces uit bemonstering van het toegepaste analoge ingangssignaal en kwantisering van dit signaal naar zijn digitale representatie, door het vergelijken van het signaal met referentiespanningen, voordat het signaal verder in een volgend digitaal systeem wordt bewerkt. Afhankelijk van hoe deze functies zijn gecombineerd, kunnen verschillende AD-conversiearchitecturen geïmplementeerd zijn, met verschillende vereisten voor elke functie. Praktische realisaties laten de trend zien dat, in een eerste orde benadering, het in de omzetter gebruikte vermogen recht evenredig is met de bemonsteringsfrequentie. Echter, de vermogensdissipatie stijgt niet-lineair als de frequentie, voor de gebruikte procestechnologie, tot het uiterste wordt opgedreven. Pipeline- en twee-staps-/multi-staps-convertors zijn meestal het meest efficiënt om de in de specificatie vastgestelde resolutie en bemonsteringsfrequentie te bereiken. Dit proefschrift toont de vermogensefficiëntie voor het bereiken van een hoge resolutie aan van een multi-staps-convertor met een combinatie van parallellisme, calibratie en het benutten van laagspanningstechnieken, door een 1.8 V , 12 -bits, $80 \mathrm{MS} / \mathrm{s}$ en 100 mW AD convertor [37] gefabriceerd in een 0.18 um CMOS-technologie met vijf metaallagen te laten zien.

Om de last te verlichten die op IC-design en -fabricage is geplaatst door de steeds toenemende kosten geassocieerd met testen en debuggen van complexe, gemengd-signaal elektronische systemen, zijn diverse circuittechnieken en -algoritmen ontwikkeld en opgenomen in de voorgestelde ATPG [187], DfT [219] en BIST [231] methodologieën.

ATPG betreft testpatroongeneratie voor rechtstreeks testen op de siliciumplak en levert daarmee een kwantitatieve schatting van de effectiviteit en volledigheid van het testproces. In de Karhunen-Loeve expansiemethode die wordt voorgesteld [187] zijn de parameters van de transistoren als stochastisch proces over het oppervlak van het IC gemodelleerd en dus zijn de parameters van elke twee componenten op het IC twee verschillende, gecorreleerde toevalsvariabelen. De grenzen van de circuitrespons worden berekend door een wiskundige evaluatie van de prestatiefunctieatributen uit te voeren, gebruik makend van de fysische tolerantielimieten gedefiniëerd voor device mismatch, wat belangrijke rekentijdbesparingen oplevert. De voorgestelde Neyman-Person statistische detector [207], die een speciaal geval van de Bayes test is, voorziet in een werkbare oplossing wanneer de a priori kansen onbekend zijn, of als de "Bayes risk" moeilijk te evalueren is. De testen worden gegenereerd en geëvalueerd rekening houdend met de potentiële maskeereffecten van de procesvariatie op de foutieve circuitrespons. Om beperkingen van de systeemtest gedurende het structurele stroomgebaseerde testen te overwinnen, worden de te testen onderdelen verdeeld in kleinere blokken met slechts beperkte additionele hardware, door middel van de vermogensscan DfT techniek [219]. Zoals de resultaten van de testpatroongenerator aangeven, zijn de meeste quasistatische fouten in verschillende blokken van de 12 -bits twee-staps/multi-staps AD convertor, afhankelijk van de mate van de opdeling, door een structurele voedingsstroomtest te detecteren, wat
een meer dan twintigvoudige reductie in testtijd oplevert in vergelijking met een meer traditionele, functionele, histogram-gebaseerde, statische of FFT-gebaseerde dynamische AD convertortest.

Behalve ATPG en DfT, zijn ook BIST benaderingen een efficiënte manier om de kosten van de testontwikkeling en het debuggen te verlagen. De BIST methode en sinussignaalgeneratie voorgesteld in dit proefschrift steunen op een programmeerbare integrator, die de generatie van een continue-tijd periodiek analoog signaal mogelijk maakt [231]. De methode heeft de kenmerken van digitale programmering en controle, robuustheid en lage overhead in chipoppervlakte.

Het meten van variaties van de procesparameters is heel belangrijk voor stabiele controle van transistoreigenschappen en statistische monitoring en de evaluatie van deze effecten maakt de efficiënte ontwikkeling van testpatronen en test- en debugmethodes mogelijk, alsmede verzekert goede yields. Met het gebruik van speciale sensoren, die kennis van de circuitstructuur en de specifieke defektmechanismen benutten, vergemakkelijkt de in dit proefschrift beschreven methode vroege en snelle identificatie van procesparametervari-atie-effekten ten koste van een overhead van maximaal $10 \%$ chipoppervlakte. Omdat het aantal op het IC aangebrachte extra sensoren eindig is door oppervlaktebeperkingen, wordt additionele informatie met behulp van statistische methodes verkregen. Het geïmplementeerde verwachtingsmaximilisatie-algoritme [264] maakte het schattingsprobleem meer handelbaar en levert goede schattingen van de parameters voor een kleine steekproefomvang. Om het leiden van de test door de informatie verkregen door het monitoren van procesvariaties mogelijk te maken, minimaliseert de geïmplementeerde aangepaste "support vector machine classifier" [264] tegelijkertijd de empirische klassificatiefout en maximaliseert hij de geometrische marge.

De voorgestelde debugmethode [278] is toegepast na elke conversiefase en opereert op het digitale signaal beschikbaar aan de uitgang. De bruikbaarheid van de methode voor on-line en off-line debuggen en calibratie is geverifiëerd door experimentele metingen aan een silicium prototype gefabriceerd in een standaard 0.09 um CMOS technologie met 6 metaallagen en geëvalueerd met een 12-bit multi-staps AD convertor. Additioneel wordt ook een debugmethode voor bandbreedtemismatch in "time-interleaved" systemen geïntroduceerd [291]. De gebruikte adaptieve filteralgoritmes voor de foutschatting gebruiken slechts een kleine aantal operaties per iteratie en vereisen geen correlatiefunctieberekening noch matrixinversies. Om de input van een filter te kunnen controleren is DfT nodig, die het mogelijk maakt om de ingangssignalen op een vooraf gedefiniëerde waarde voor elke conversiefase vast te zetten. De geïmplementeerde DfT benadering [282] maakt circuitherconfiguratie mogelijk op een zodanige manier dat alle subblokken kunnen worden getest voor hun volle ingangsbereik, en maakt daarmee volledige observeerbaarheid en controleerbaarheid van de geteste schakelingen mogelijk. Het toevoegen van testmogelijkheden verminderd de convertorprestatie niet en het heeft slechts een klein effect op chipoppervlakte en vermogensgebruik. Bovendien is de debugaanpak uitgebreid om "foreground" calibratie van de multi-staps AD convertor mogelijk te maken [300].

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## ABOUT THE AUTHOR

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