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FPGA Based Modular Control Platform for Switched Mode Power Converters

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Abstract—In educational as well as research environments there is a demand for an easy way to prototype switching converters. Several recurring standard tasks like pulse pattern generation, driving controllable switches and analog to digital conversion of physical quantities e.g. current, voltage and temperature, need to be performed. Because these standard tasks interfere with the research focus, a modular control platform for rapid prototyping is highly desirable. In this paper, a system is presented that provides an effective and flexible solution for these requirements.

Index Terms—DSP, FPGA, Matlab, ARCP.

I. Introduction

IN order to operate a Switching Mode Power Supply (SMPS) in its optimal operating point, closed loop control is of vital importance. Dedicated Application Specific Integrated Circuits (ASICs) are available for commonly used configurations, such as buck or boost controllers (e.g. the LM3485 by National Semiconductor), but often a more advanced and flexible solution is required. Integrated environments capable of providing such a solution are for example dSpace [1], a Field Programmable Gate Array (FPGA), a Digital Signal Processor (DSP), or a combination of DSP and FPGA [2].

Because Matlab/Simulink is the facto standard in R&D, it will be used as a development environment. To enable the user to implement new modules, the hardware architecture should be as flexible as possible, and therefore the backbone of the hardware will be an FPGA. Model Based Design is the Matlab/Simulink design flow, covering all necessary steps to convert a Golden Reference (GR, executable specification [3]) floating point model to fixed point bit and cycle true physical hardware. A test bench that was designed to check the GR, can be used throughout the entire design flow to enable continuous verification against the executable specification. Xilinx integration with Maltab/Simulink: System Generator (SG) further increases integration by enabling Hardware In the Loop (HIL) testing. HIL enables the design running on physical hardware to be verified against the GR using the same test bench. Besides this, HIL goes even one step further; its possible to use additional hardware peripherals like ADCs, on board RAM memory, MOSFET gate drivers etc., changing the test bench to the final in-circuit real-time application.

Various examples of system controllers based on the dSpace development platform have been presented [4]. The advantage of e.g. a dSpace system is that it can be set up very fast,

operating system drivers are available, and it is integrated in the Matlab/Simulink software, which shortens development time significantly. For basic PWM generation, the slave processor's PWM module is sufficient. For more challenging modulation schemes, one will soon run into the limitations of the standard dSpace system. A more advanced solution was therefore chosen, namely the P25M DSP-FPGA board [2].

In a typical application controling a SMPS, several recurring subsystems can be identified. This property will be used to our advantage to create a library of configurable basic building blocks that cut future development time. This enables the user to focus on algorithm development instead of re-inventing the wheel. Depending on the requirements, the user can fit the required modules together to form a complete system that will interface between the SMPS of interest, it's physical environment and Simulink.

To demonstrate the capabilities of the proposed system, an Auxiliary Resonant Commutated Pole (ARCP) Full Bridge (FB) down converter with Synchronous Rectification (SR) has been designed. This specific SMPS has been chosen for its high efficiency when it is correctly controlled. That directly points out the disadvantage of the ARCP-SR-FB, as it requires ten active devices, which should each be controllable with an approximated timing resolution of hundred nanoseconds. The FB configuration utilized as a dc/dc down converter has been presented in previous papers [5], [6].

To ensure fast integration of the DSP-FPGA modular platform in custom developed SMPSs, a set of switch driver boards has been designed. With these boards, the most common types of Active Semiconductor Devices (ASD) can be driven. Previous research on ASD gate driver circuits was presented in [7], [8]. Data sheets and application notes on gate driver ICs are also a good source of information, e.g. the IR2110 [9]. In this project, three types of gate driver circuits can be identified, i.e. direct (low-side), high-side (together commonly known as half bridge configuration) and floating drivers.

The paper is organized as follows. An overview of the implemented DSP-FPGA platform is given in Sec. II, and details on the accompanying software modules are described in Sec. III. In Sec. IV the set of predesigned MOSFET drivers is shown, required to drive the ARCP-SR-FB down converter presented in Sec. V. Simulation and compilation results are verified in the experimental results Sec. VI, and conclusions drawn from these results are stated in Sec. VII.

II. HARDWARE PLATFORM

Trouble free use of the platform can be achieved only if the requirements of the SMPS that needs to be controlled are met. Because these requirements are not known yet, the system has been set up such that its overqualified for most SMPSs. The specifications set for this platform are listed in Tab. I.

The total hardware platform is divided into three parts, namely the PC interface, the Isolation/Amplification, and the input filter stage. An overview of the structure is depicted in Fig. 1. Details on each of these modules are presented in Sec. II-A, Sec. II-B, and Sec. II-C respectively.

Table I
SPECIFICATIONS HARDWARE PLATFORM

Description	Amplitude	Max. Frequency
23 gate driver signals	0-18 V	40 MHz
4 digital inputs	0-5 V	40 MHz
4 isolated analog inputs (14 bit)	0-5 V	78 kHz
4 non isolated analog inputs (16 bit)	± 2 V	25 MHz

A. PC Interface Card

The PC interface card is designed to ensure high speed, and error free communication from the P25M system to the outside world over a maximum distance of 5 meter, using a SCSI cable. This is achieved using three differential line drivers (SN65LVDS389DBT) and one differential line receiver (SN65LVDS388ADBT, both [10]), each consisting of eight channels. The LVDS drivers are powered by the PC's common power supply.

B. Isolation, Amplification and ADC board

In order to supply the MOSFET driver boards in a safe way and with adequate signaling, the isolation, amplification, and Analog to Digital Converter (ADC) board (isolation board) was designed. It consists of a differential transceiver, an isolation barrier, and an amplification stage. It is furthermore equipped with eight analog and four digital inputs, which are designated as feedback signal from the SMPS to the P25M. The LVDS transceiver stage is complementary with the PC interface card.

The galvanic isolation in this system is required to ensure a high voltage dielectric isolation barrier between the PC and the SMPS, which is required for Safety Regulatory Approvals (SRA) and reduction of Electro Magnetic Compatibility (EMC) issues. The SRA is a guideline to guarantee safe design of equipment that is directly connected to 230 V_{ac} or industrial power systems, which is the case here. Regarding EMC, the galvanic isolation reduces common mode and ground loop problems. The isolation is accomplished for digital signals by using the Si8460 devices [11], and for the ADCs using the Isolated Sigma Delta Modulators (ISDM) AD7401 [12]. On the digital side of the ADC a clock pulse of 20 MHz is applied, and a 1 bit data stream with an average proportional to the analog input voltage is retrieved.
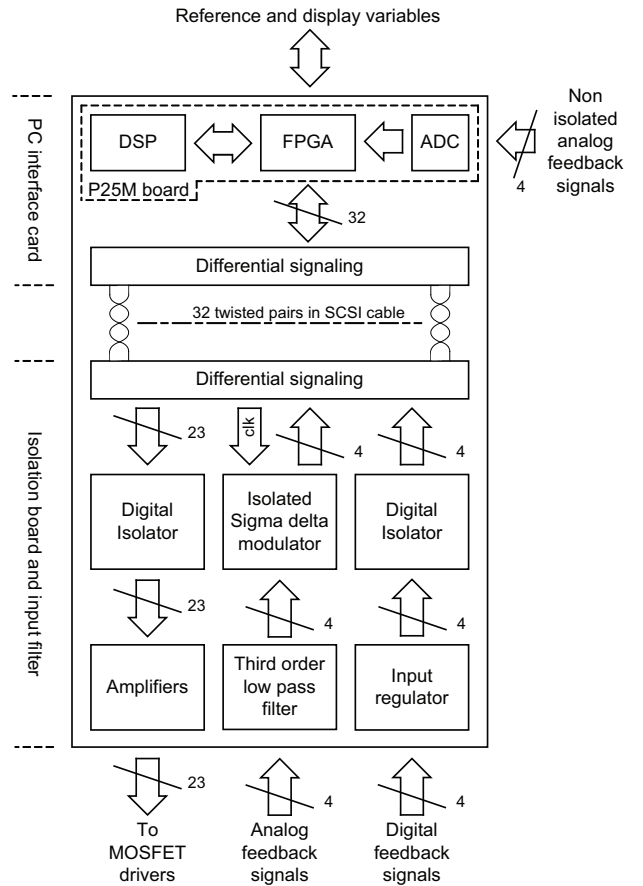

Figure 1. Schematic overview of hardware platform.

The AD7401 is used in the 0-200 mV input voltage range, and therefore ideally has a 14 bit resolution up to 78 kHz. Whether this resolution is reached in practice depends on many factors, e.g. adequate Printed Circuit Board (PCB) layout, and input filtering. The input voltage range is increased to 5 V by means of a resistance divider network, the input impedance is increased by an operational amplifier (op amp) in voltage follower mode.

C. Analog Input Signal Filter

As a result of the high $\frac{\partial V}{\partial t}$ present in SMPSs, and to avoid aliasing, the analog signal which is fed back for control must be filtered before it is applied to the ADC. To retrieve the output voltage of the SMPS, a third order low pass filter with a cut-off frequency of 7 kHz is designed. This filter is added to the system as a separate board because the analog filter requirements are different for each application.

III. FPGA SOFTWARE MODULES

In the scope of the modular platform, the minimal set of modules consists of analog inputs, control and pulse pattern generation. Initially FPGA development has been our focus. For future advanced control algorithms the floating point DSP will need to be used, [13].

A. ADC

For selecting suitable ADCs, several aspects are considered like sample rate, resolution and analog to digital side isolation. For each selected ADC a dedicated FPGA module will be written. The AD7401A was selected because of it's internal galvanic isolation barrier. The interface from the FPGA to the ADC is pretty straightforward. A Clock signal (up to 20 Mhz) is generated on the FPGA and per clock cycle, one bit of data is captured. In order to use this signal, decimation is usually required. Because every application has it's own requirements of resolution and/or sample rate, the decimator is configurable.

B. Pulse pattern generation

By studying the topology of the converter, all required sequences to control switches can be determined. Some events will require a highly accurate adjustable timing reference. Because of the discrete nature of FPGA technology, the dithering technique presented in [14] could be implemented to increase resolution. Ordinary counters are the preferred way to implement less critical fixed delays such as dead-time insertion for safe operation of a half bridge. Switching frequencies are typically in the kHz to several MHz range.

1) Development flow: In order to compensate for differences in driver delays, the delay from FPGA output to the actual MOSFET switching moment has to be measured. Both rising and falling edges (turn on and turn off) should be measured as they are different as depicted in Fig. 7. Also high and low side half bridge drivers can use nonidentical circuitry and therefore will have different timing properties.

By means of an initialization script the measurement values are rounded to integer numbers of clock cycles, in fact constants that allow efficient hard coding on the FPGA.

In the used power converter, every controlled timing event is referenced to a master clock. The demo power converter roughly features two groups of timing events related to each other by means of the phase shift between the full bridge legs. Within each group all events can be referenced to each leg's 50% duty cycle. For efficient implementation on the FPGA, all timing events within a group are referenced to the first event occurring in the group. The succeeding events will then accordingly be just simple integer numbers of clock events delay.

The actual group-timing that is generated on the FPGA is the desired timing plus the driver delay compensation.

2) Forbidden state prevention: When controlling a half bridge, care must be taken that the both switches on state never occurs. When the FPGA is being programmed through JTAG, or reset and loading from the configuration PROM, the FPGAs I/O Pins are put in a tri-state condition. Because the used LVDS buffers don't support tri-state signalling, programmable pull up/down or jumpers are used to define default/unharmful/safe signal states. In this manner the FPGA can be reprogrammed without problems, while being permanently connected to a fully powered SMPS.

IV. MOSFET DRIVERS

The proposed FPGA platform, allows drivers up to 40MHz to be driven directly. In order to operate the power converter,

several MOSFET driver boards were designed to drive gates directly, i.e. in half bridge configuration (low side & high side), and galvanically isolated. All gate drivers are built to support dynamic driving i.e. switched on and off at the typical switching frequency without the need for 50 % duty cycle (D). In the galvanically isolated drivers, this is achieved by the dc decoupling capacitor in series with the transformer (Fig. 2). A restriction on D, $0.1 \leq D \leq 0.9$ is a result of this method. The output voltage (V_{out}) will otherwise exceed the typically allowed gate source voltage of the power MOSFET. The direct drives are furthermore able to drive in static mode (on or off for sustained periods of time). As needs appear, more driver boards will be designed to perform required tasks.
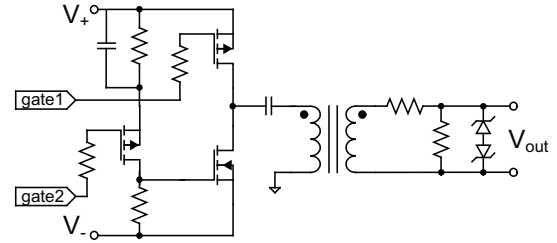

Figure 2. Half bridge floating gate driver circuit.

The functionality of the ARCP and SR MOSFET drivers is identical (Fig. 2), their designs however differ slightly due to different requirements. The MOSFETs that need to be driven by the SR driver have a much higher input capacitance, resulting in higher transformer currents. A transformer with a lower Equivalent Series Resistance (ESR) is therefore chosen. The driver consists of an level shifter and a half bridge stage. Because the output signals of the isolation stage are 0-10 V, the NMOS cannot be driven directly, the level shifter is included for that. The series resistor on the secondary side of the transformer reduces current peaks during transitions, the parallel resistor is for pull down and the zener diodes protect the gate of the power MOSFET against over voltage.

V. ARCP-FB-SR DOWN CONVERTER

Fig. 3 shows the proposed converter topology, and Tab. II shows the specifications set for this demo converter. The basic principle of the FB dc/dc converter is that an AC voltage is created across the primary of a transformer, and this voltage is rectified on the secondary side (PMC [15]). The input voltage (V_{in}) and winding ratio (k) of the transformer determine the maximum value of the V_{out}. Each of the switches is turned on for half the cycle time, minus a small period of dead time in between. Switches S_1 and S_4 are simultaneously on, just like S_2 and S_3, By varying the phase angle between $S_{1,4}$ and $S_{2,3}$, the effective voltage across the transformer can be adapted, and with it the output voltage. The ARCP and SR circuits are added to the FB converter to increase its efficiency over the full output power range.

The ARCP [16] circuit is used to minimize the switching losses by ensuring Zero Voltage Switching (ZVS). When switching the points A and B alternating between 0 and V_{in}, the voltage difference is $V_{in}/2$ with middle point M, which
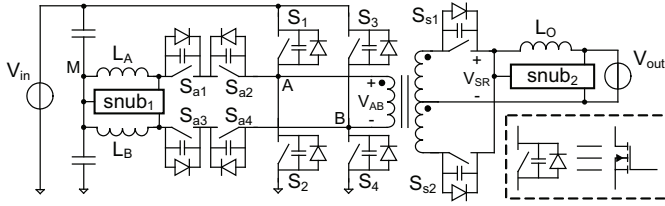
Figure 3. The proposed ARCP-FB-SR down converter.

is constant at $V_{in}/2$. If for example the voltage at point A must be transitioned from 0 towards V_{in} after S_2 has opened and before S_1 has closed, i.e. during the dead time (t_d), S_{a2} must be on. Due to the voltage across the inductor L_a being $V_{in}/2$, the resonant commutation phase between L_a and the drain source capacitance (C_{ds}) of S_1 and S_2 is initiated. The snubber circuit $snub_1$ is included to reduce the voltage peaks across the ARCP switches which are a result of resonance caused by $L_{a,b}$ together with the C_{ds} of S_{a1-4}.

The principle of SR aims at reducing the secondary rectifier losses by turning the MOSFET on during conduction of its anti-parallel diode [15]. The typical forward voltage drop is 0.7 V for a small signal diode, and around 1.5 V for a high power device when the nominal output load (R_{load}) of 2.3 Ω is considered. This would result in a conduction loss of 16 W per device. If during conduction of the diode the devices $S_{s1,2}$ are turned on, the conduction losses can be reduced. The on resistance ($R_{ds(on)}$) of the devices should therefore be lower than 70 mΩ. The device chosen (Tab. II) has an typical $R_{ds(on)}$ of 5 mΩ reducing the conduction losses to 1.1 W per device. The snubber circuit $snub_2$ is included to reduce the voltage peak across the SR switches which are a result of resonance caused by the secondary leakage inductance of the transformer together with the C_{ds} of $S_{s1,2}$.

Table II
SPECIFICATIONS ARCP-FB-SR DOWN CONVERTER

Parameter	Nominal value	Parameter	Value/device
V_{in}	400 V	k	7:1:1
V_{out}	48 V	$L_{A,B}$	8 μH
f_{sw}	100 kHz	S_{1-4}	STW45NM60
P_{out}	1 kW	S_{a1-4}	STP10NK60
R_{load}	2.3 Ω	$S_{s1,2}$	IRFP4568PbF

From the topology it is clear that the controlling degree of freedom is the phase shift (Phi) between the left and right leg of the full bridge. In each leg, during the dead-time of the corresponding FB leg, the ARCP circuit is activated to make sure that before the dead time has ended, the voltage of the MOSFETs has been adjusted in such a way that ZVS at turn on is achieved. The turn off of the ARCP circuit is less critical but should occur between the leg enters the next dead time interval. When the voltage across the terminals of the transformer (V_{AB}) is positive, the MOSFET, of which the internal anti-parallel diode as result of the applied voltage should conduct (S_{s1}), is switched on to reduce semiconductor

conduction losses.

When taking all dead times (FB_Dt, ARCP_Dt, and Syn-Rec_Dt) into account the actual implementation sequence shows the complexity of the 16 gate drive signals (Fig. 4). In each family of colored, numbered dots, all four timing sequences have been identified. By regarding the order of events, one can clearly see that an asymmetry is present between the sequences referenced to the right and left leg. Because the first event that occurs is switching off the synchronous rectifier in the right leg, this is the event to which all others in this family are referenced to. In order to prevent a phase shift, the timing of the left leg has to be compensated for it by adding an extra delay (and virtual event) to which al timing in the right leg families is referenced to.
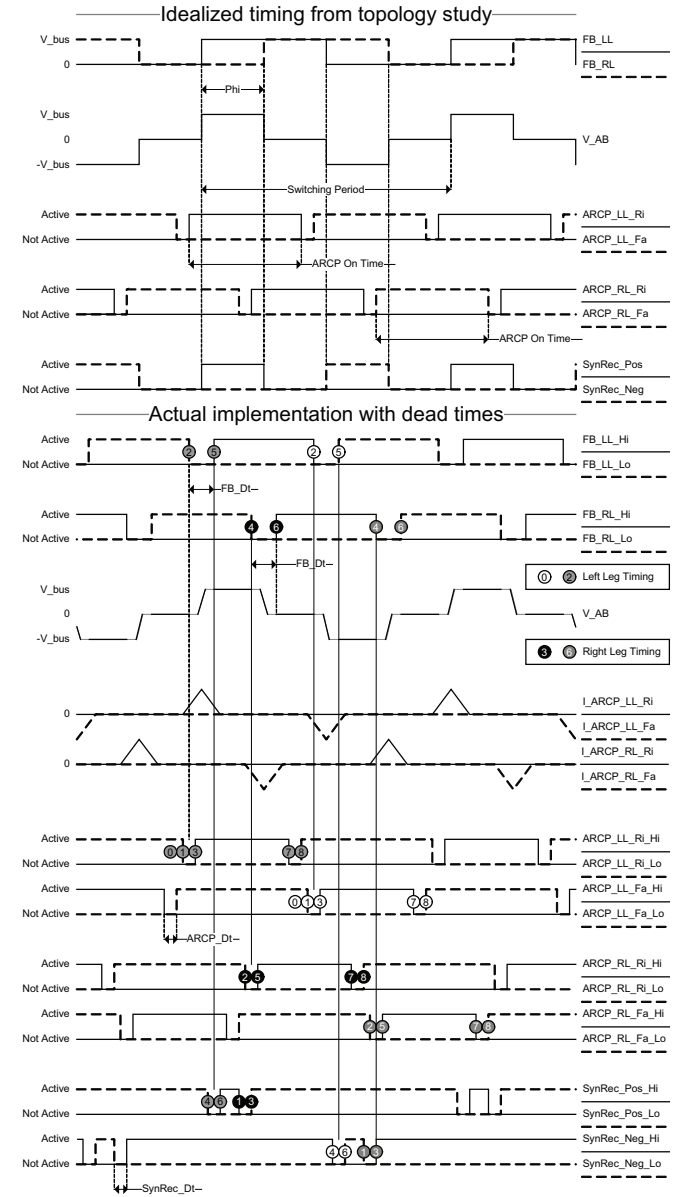

Figure 4. Gate timing for the ARCP-FB-SR down converter.

Efficiency simulations on the proposed circuit were performed in the configurations FB only (FB), FB with ARCP

(FB-ARCP), FB with SR (FB-SR), and with the total circuit (ARCP-FB-SR), with an constant R_{load} and for the indicated values of V_{out} (Tab. III). For both the simulated and measured efficiency, the topology efficiency is considered, excluding power consumption by control and driver circuits. From the results shown in this table it can be concluded that for maximum efficiency, the ARCP-FB-SR is the optimal configuration. What can also be recognized is that the same efficiency is simulated for high output power in the FB-SR and ARCP-FB-SR configuration. This is the result of the high transformer current that ensures ZVS in the FB-SR configuration, the ARCP can therefore be turned off at nominal output power.

Table III
SIMULATED EFFICIENCY OF GIVEN CONFIGURATIONS FOR VARIOUS V_{out}

V_{out}	Efficiency [%]			
	FB	FB-ARCP	FB-SR	ARCP-FB-SR
6 V	34	79	33	85
12 V	40	82	65	95
24 V	58	89	82	97
48 V	81	94	97	97

VI. EXPERIMENTAL RESULTS

In order to demonstrate the potential of the system, all described system parts were assembled in a prototype. A picture with all the indicated parts is shown in Fig. 5. The sizes of the isolation board and ARCP-FB-SR down converter are 100 x 160 mm, and 160 x 200 mm respectively.

To verify whether the implemented PC interface and isolation board meet the high frequency requirements set in Tab. I, measurements were carried out. A block shaped wave was applied to an input of the PC interface, and on the isolation board the corresponding output signal (V_{gate}) was fed back as digital input. The resulting signals measured at the output of the PC interface (V_{inter}) are depicted in Fig. 6 for the specified frequencies. Typical rise and fall times of V_{inter} are around 2 ns, variation of the duty cycle is caused by the inaccuracies in the input signal.

Timing delays as described in Sec. III-B1 were measured, Fig. 7 shows an example of the difference in rise and fall times of the SR MOSFET gate voltage. Timing compensations was added in the FPGA to ensure correct operation of the SMPS.

The total system efficiency was measured for the configurations FB, and FB-ARCP only, the timing of the SR driver was not correctly programmed and the component was excluded therefore. The gate and source of the SR drivers were short circuited, and their diodes were used for rectification. Tab. IV shows the results of the measurements. From these results it can be concluded that for high output powers, the ARCP circuit already increases efficiency. Although, the programmed ARCP timing is not yet optimal, efficiency at lower power levels is expected to increase after timing improvement.

The thermal stability of the SMPS was also measured, the temperature of the transformer depicted in Tab. IV was measured after 30 minutes of operation, and was stable.
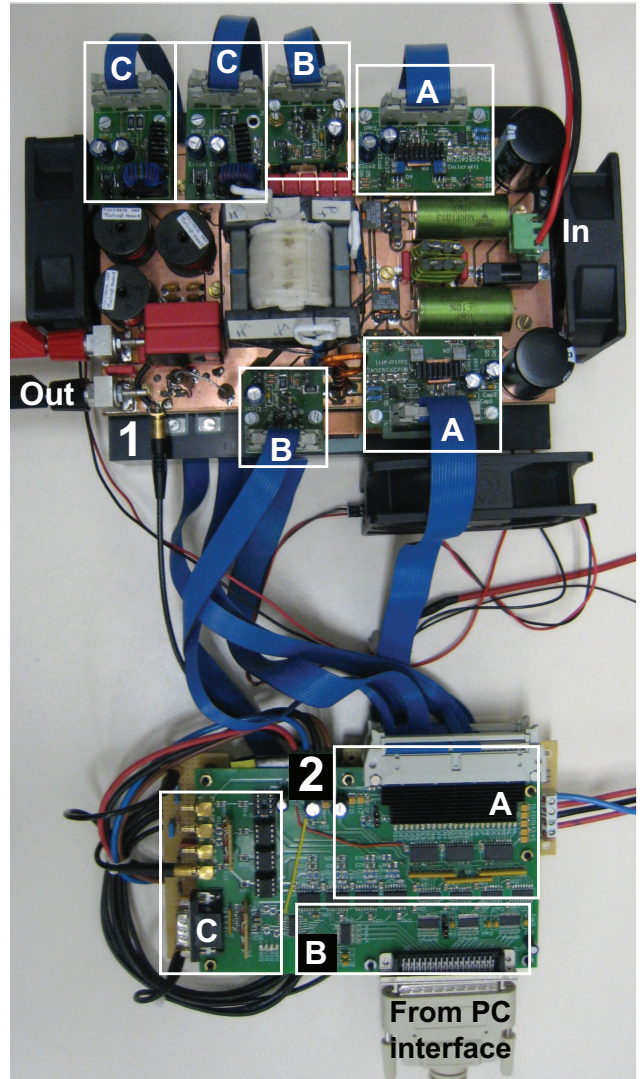

Figure 5. The build ARCP-FB-SR (1), and isolation board (2). The shaded areas indicate for 1: MOSFET drivers of ARCP (A), FB (B), and SR (C), and for 2: amplification (A), isolation (B), and ADCs (C).
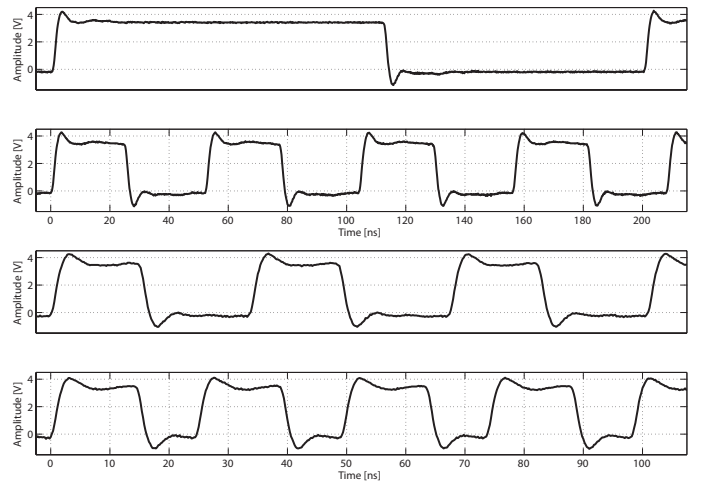

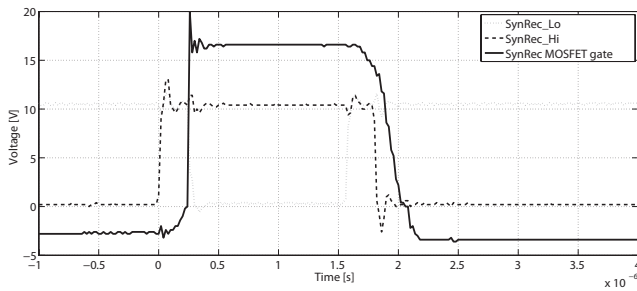Figure 6. V_{inter} for approximately 5, 20, 30, and 40 MHz.

Figure 7.   SR MOSFET driver and gate signals.

Table IV
MEASURED EFFICIENCY OF GIVEN CONFIGURATIONS FOR VARIOUS V_{out}

V_{out}	Efficiency [%]		Temperature Transformer [$^\circ C$]	
	FB	FB-ARCP	FB	FB-ARCP
6 V	38	37	102	97
12 V	62	61	72	69
24 V	86	89	50	56
48 V	92	94	40	36

VII. CONCLUSION

By utilization of this modular platform, SMPS projects can be prototyped faster in the future.

The first software modules implemented show that fast integration with a SMPS is possible, the library of modules can be extended to support specific needs. Additional effort must be put in FPGA programming to remove timing problems, and finalize full circuit measurements.

The designed MOSFET drivers work as intended and they can be used in future projects. Verification on ZVS and correct SR operation as well as efficiency measurements for all configurations should be added to the results.

In order to completely use the P25M board's potential, the correct combination of software package versions of six different vendors has to be installed.

Although our suggested isolated delta sigma ADC has several advantages, it also features impairable down sides. In order to obtain sufficient resolution, the bitstream has to be decimated. This means that during the interval needed to obtain the required resolution, switching events in the power converter can occur. Without taking measures, this will result in excessive amounts of unwanted switching noise. By utilizing the positional degree of freedom of the ADC's sampling moment, switching noise can be minimized.

ACKNOWLEDGMENT

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