An inductive down converter system-in-package for integrated power management in battery-powered applications

An Inductive Down Converter System-in-Package for Integrated Power Management in Battery-powered Applications

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***Abstract*—With the increasing number of voltage conversions that have to be efficiently implemented in a mobile device, the PCB space occupied by switched-mode DC-DC converters with external passive components will become unacceptably high. Therefore, a clear need exists for small-form-factor high-efficiency DC-DC converters having the necessary passive components integrated within one package. This will enable the integration of a DC-DC converter with the load and consequently the system integration of power management. This paper describes the measurement results of an integrated inductive down converter, where the active electronics (power stage and driver circuitry) has been implemented in 0.18-µm CMOS technology and the passive components (output LC filter and decoupling capacitor) have been implemented in a state-of-the-art proprietary passive-integration process technology using high-density trench-MOS capacitors (80 nF/mm^2) and an 8-µm thick copper top metallization layer. The active die of the converter has been flip-chipped on top of the passive die to reduce parasitic component values. This yields a System-in-Package (SiP) that achieves a step-down DC-DC conversion without any external components. Due to the limited inductance achievable with the used planar air coil in the acceptable area, the switching frequency of the DC-DC converter has been increased. At the same time, Zero-Voltage-Switching (ZVS) measures have been implemented to reduce the switching losses at this increased frequency. A maximum efficiency of 65% at 80 MHz has been achieved for an input voltage of 1.8 V, an output voltage of 1.1 V and an output current of 100 mA. After explaining the motivation behind integrated power management and the choice for an integrated inductive converter, this paper describes the main design aspects of the realized integrated inductive DC-DC down converter. Next, it presents some details of the used passive-integration process, the design of the passive die including the LC filter and the construction of the SiP. Finally, the measurement results of the converter are discussed and conclusions are drawn.**

I. INTRODUCTION

The number of features implemented in mobile devices increases dramatically leading to a multitude of different supply voltages, all of which need to be generated from a single battery voltage. For example, the current invasion of solid-state lighting applications, such as LED flash allowing improved photo quality, leads to different voltage and current requirements than other applications and therefore necessitates the addition of DC/DC converters to the system. At the same time, the continuous drive towards better autonomy has led to the use of voltage islands in digital ICs. In each voltage island the lowest possible supply voltage is used to run the connected digital circuitry at the optimum efficiency. This is commonly referred to as voltage scaling and leads to even more different supply voltages that need to be independently generated from the battery voltage [1].

For optimum efficiency, especially larger voltage differences need to be converted by switched-mode DC-DC converters, including capacitive and inductive DC/DC converters. Linear regulators yield unacceptably low efficiencies in this case. Capacitive converters have the advantage of not needing an inductor, which is often costly and bulky, but the control of the output voltage over input-voltage variations is limited since the voltage-conversion ratio is determined by the circuit topology. A possible solution to this problem is to vary the effective output resistance of the converter, e.g. by changing the duty cycle at which the switches are addressed, but this substantially decreases efficiency when the input-voltage range is relatively large [2]. For a large input-voltage range, which appears in all targeted mobile applications using a Li-ion battery, the alternative solution to maintain output-voltage regulation and acceptable efficiency is to implement multi-ratio capacitive converters where the appropriate ratio is chosen dependent on the input voltage and load requirements [3],[4]. However, in order to optimize the average efficiency over the input-voltage range the number of ratios may become rather high, leading to a relatively large number of capacitors.

Inductive DC-DC converters are attractive, since they enable good control of the output voltage over input-voltage and output-load variations by means of controlling the duty cycle of the power switches using only three passive components. Two capacitors are used for input decoupling and output filtering, respectively, and one inductor is used for energy transfer from input to output.

Both in the case of capacitive and inductive DC-DC converters, however, using external passive components to accommodate the increasing number of voltage conversions would lead to unacceptably high volume and cost. Therefore, the need arises for small-form-factor highly efficient DC-DC converters with package-integrated passive components. This enables integration of the DC-DC converter with the load, and, consequently, the system integration of power management. As mentioned above, inductive DC-DC converters are better able to

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handle the relatively large input-voltage range in Li-ion-battery-powered applications with a relatively low number of passive components. Since the voltage of the commonly used Li-ion battery is typically larger than the supply voltages for the ICs in a mobile device, this paper therefore focuses on integrated inductive down converters.

Air-core inductors are popular for realizing integrated inductors due to their relatively simple structure and good integration possibilities [5]-[8]. Since the required small volume and the low permeability of air limit the achievable inductance value, the switching frequency of the DC-DC converters has to be increased correspondingly, leading to low efficiencies without proper measures. The use of multiple air-core inductors in multi-phase Voltage-Regulator Module (VRM) applications has shown that efficiencies between 72% and 84% are possible for switching frequencies of 480 MHz and 100 MHz, respectively, for output powers above 10 W [5],[6]. However, for mobile applications the required output powers are much lower, complexity should be low and the height of SMD inductors inside the package is unacceptable. A reported two-phase interleaved buck converter achieves 64% efficiency for output powers between 300 mW and 400 mW at 65 MHz switching frequency, but a 0.18-µm SiGe process was used with an additional top copper metallization. This is unpractical for the integration with nm-CMOS circuits [7]. Similarly, a single-stage buck converter realized by adding additional process steps to a standard CMOS process to implement a MEMS-based inductor achieves an efficiency below 60% at 10 MHz and 75 mW output power [8].

This paper aims at demonstrating the feasibility of flip-chipping a standard-CMOS active die on top of a silicon-based passive-integration die for realizing an integrated DC-DC down converter. Since processing the passive die involves significantly fewer masks than processing a nm-CMOS active die, placing the relatively area-consuming passive components on a separate die makes sense from a low-cost point-of-view. The realized SiP aims at output powers in the 100-mW range and fits inside a standard QFP64 package.

Section II highlights the main design aspects of the integrated converter, including design of the active die and determination of the needed passive-component values. Section III gives more details on the used passive-integration process and the design of the passive die, particularly on the design of the LC output filter, and the complete SiP. The main measurement results are summarized in section IV. Finally, conclusions are drawn in section V.

II. Design Aspects of the Integrated DC-DC Down Converter

As described in section I, the use of a low-inductance integrated inductor necessitates a high switching frequency, which leads to increased switching losses without proper measures. Therefore, capacitive switching losses should be minimized using ZVS measures. In a buck converter with synchronous rectification, as considered in this paper, ZVS can be achieved by proper control of the power switches and by allowing the inductor current to go negative. This is explained with reference to the general block diagram of a synchronous buck converter with corresponding waveforms as shown in Fig. 1.

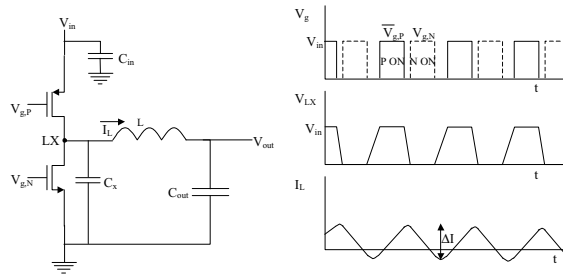


Figure 1. General block diagram of a synchronous DC-DC down converter with corresponding waveforms

When the PMOST is on (inverse of $V_{G,P}$ equal to V_{in} in Fig. 1), the inductor current I_L ramps up linearly. At the moment the PMOST switches off, the positive inductor current discharges the parasitic switch capacitance C_x at the switching LX node between the two power MOSTs. With proper control of the dead time between switching off the PMOST and switching on the NMOST, the NMOST can be switched on when the drain-source voltage is zero. The capacitive losses are now reduced, since C_x has been discharged by the inductor current I_L. When the NMOST is on ($V_{G,N}$ equal to V_{in}), current I_L ramps down linearly. When the current ripple ΔI is large enough, current through the NMOST will reverse and I_L will go negative. At the moment the NMOST switches off, I_L will now charge C_x. With proper dead-time control the PMOST can now be switched on when the drain-source voltage is zero, again reducing capacitive losses. Note that the transition times at the LX node depend on I_L and therefore on the load current. Therefore, in order to prevent that the MOSTs are switched on too early, leading to remaining capacitive switching losses, or too late, leading to parasitic body-diode losses, the dead-time control needs to be adaptive for optimum efficiency.

Various examples of adaptive dead-time control to reduce capacitive switching losses in high-switching-frequency synchronous DC-DC down converters can be found in literature [9],[10],[11]. The ZVS DC-DC down converter in [9] with an input voltage V_{in} of 40 V applies a constant-off-time controller, where the frequency is varied to modulate the duty cycle. This leads to a constant value of the current ripple ΔI large enough to ensure inductor-current reversal, since it is proportional to $V_{out}T_{off}$. A Delay-Locked-Loop (DLL) is used to ensure that the drain-source voltage V_{ds} crossing zero and the gate-source voltage V_{gs} passing the threshold voltage V_t occur at the same moment. The ZVS DC-DC down converter described in [10],[11] with V_{in}=2 V is used for Voltage-Regulator Module (VRM) applications. An additional capacitor is added in parallel to C_x to increase the high-low and low-high transition times at the LX node. This enables more precise adaptive dead-time control, since delays in e.g. comparators in the control loop and gate drivers become less influential. As in [9], V_{ds} zero-crossing and V_{gs} V_t-crossing comparators are used, the outputs of which are fed to an analog DLL.

The integrated DC-DC down converter described in this paper has a relatively low input voltage of 1.8 V. Moreover, its output power is relatively low, leading to relatively small power switches and therefore relatively small parasitic LX-node capacitance C_x. The losses $f_sC_xV_{in}^2$ at a switching frequency f_s of e.g. 50 MHz are

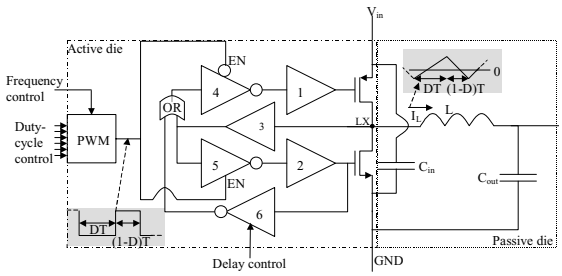


Figure 2. Block diagram of the integrated inductive DC-DC down converter

therefore in the same order as the power consumption of the adaptive dead-time controller reported in [11]. We therefore chose to implement a simpler ZVS scheme that may not be perfect, but also hardly consumes any additional power.

A block diagram of the implemented DC-DC down converter including the main components on the active and passive die is shown in Fig. 2. The active die contains the power stage, consisting of a PMOST and NMOST with corresponding drivers 1 and 2, digital circuitry to implement a simple form of ZVS for the reduction of capacitive switching losses and a Pulse-Width Modulation (PWM) generator. No closed-loop control has been implemented yet, because we chose to focus on the technological aspects of the construction of a two-die SiP DC-DC converter, keeping the active-die design as simple as possible. This implies that the desired V_{out} is obtained by setting the correct duty cycle D via a 6-bit digital input code externally. The frequency of the PWM generator is controlled externally as well. The passive die includes the decoupling capacitor C_{in}, inductor L and output capacitor C_{out}.

The ZVS operation of the power stage is achieved by monitoring the voltage at the LX node, see Fig. 2. First, consider switching off the PMOST at the end of the period DT. As soon as the PMOST has been switched off, the coil current I_L will discharge the LX node, leading to a rapid decrease in voltage. Buffer 3 will pass this falling edge on to the input of inverter 5, which is enabled by the PWM signal going 'high' at the start of period (1-D)T. As a result, the logic 'high' signal is passed on to driver 2, switching on the NMOST. The NMOST is switched off at the end of period (1-D)T by disabling inverter 5. When coil current I_L is negative (into the LX node), the LX-node voltage will increase. This is again detected by buffer 3, which passes the rising edge on to the input of inverter 4 via an OR port. Inverter 4 is enabled by the PWM signal going 'low' at the start of period DT. Now, the logic 'low' signal is passed on to driver 1, switching on the PMOST. For high load currents, I_L will no longer become negative. Therefore, an alternative path is needed to turn on the PMOST. When the gate of the NMOST goes 'low', the output of inverter 6 goes 'high' after a programmable delay. This signal is passed on in parallel to the LX-node signal path and will enforce the PMOST to switch on, even if the LX voltage is still low. This prevents a dead-lock situation, but should be avoided in nominal cases.

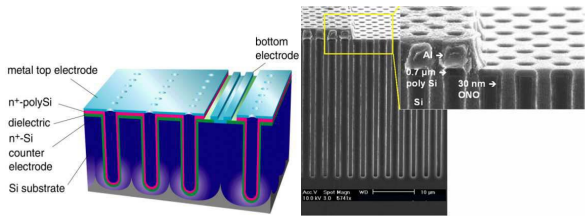
Sizing of the MOSTs in the power stage has been optimized by minimizing combined switching and resistive losses for a switching frequency of 50 MHz, an output current of 100 mA, and an inductance value of 20 nH. The PMOST was sized roughly a factor 3 larger than the NMOST to compensate for the mobility difference of holes and electrons. Based on the sizes of the power MOSTs, the driver circuits have been optimized for optimum efficiency [12]. The PMOST driver uses 4 stages and a tapering factor of 3.3, whereas the NMOST driver uses two stages and a tapering factor of 4.5. The active die was realized in standard 5-metal-layer 0.18-µm CMOS.

The chosen inductance value is a trade-off between occupied area and total efficiency. Given the inductance value of 20 nH, the output capacitor value was chosen to be 75 nF to obtain a maximum peak-to-peak voltage ripple at 50% duty cycle of 15 mV, excluding the influence of equivalent series inductance (ESL) and resistance (ESR) of the output capacitor. More information on the design of the LC output filter will be given in the next section. Since the switching frequency is relatively high, proper decoupling of the power stage is critical and particularly the series inductance in the connections of C_{in} should be very low. As will be described in the next section, the value of the decoupling capacitance was chosen as large as possible.

III. Passive-Integration Process, Passive-Die Design and SiP Construction

The proprietary Passive-Integration Connective Substrate (PICS^{TM}) process is silicon-based and provides a platform for the integration of resistors, capacitors and inductors [13],[14],[15]. It offers interesting advantages for realizing integrated DC-DC converters. First, it achieves large capacitance densities by utilizing trench-MOS capacitors. The PICS version used in this work achieves a density of 80 nF/mm^2 [15]. Secondly, an 8-µm thick copper top-metal layer available in this PICS version in addition to the first aluminum metal layer enables the design of spiral air-core inductors with reasonable performance. Fig. 3 illustrates the trench-MOS capacitor used to realize C_{in} and C_{out} as well a cross-sectional SEM image of the capacitor structure.

In order to form the high-density capacitors, pores of roughly 1 µm width and 30 µm depth are dry-etched in a high-resistivity (1-5 kΩcm) silicon substrate. The bottom electrode of the MOS capacitor structure in Fig. 3 is formed by making the pore walls of the structure highly conductive (n^+-doped bottom electrode). The dielectric is formed by an ONO (Oxide-Nitride-Oxide) layer. The thickness of 30 nm shown in Fig. 3b corresponds to a capacitance density of 30 nF/mm^2. The top electrode is formed by filling the pores with n-type in-situ-doped poly silicon. The top and bottom electrodes are then contacted with first-metal-layer aluminum. The achieved breakdown voltage at 80 nF/mm^2 capacitance density is 15.5 V, which



(a) (b)

Figure 3. (a) Schematic representation of the trench-MOS capacitor, (b) Cross-sectional SEM image of a complete trench-MOS capacitor structure in dry-etched silicon [13]

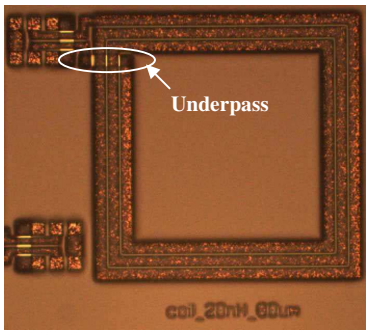


Figure 4. Photograph of the realized 20-nH planar air-core inductor in a separately laid-out version for wafer-level testing without the capacitor in the middle

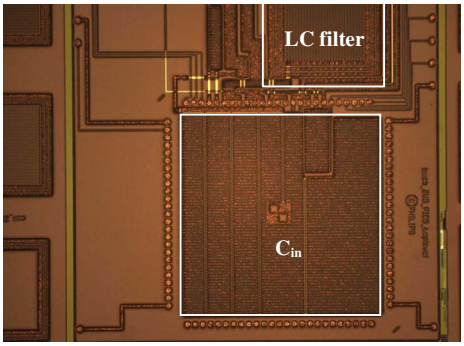
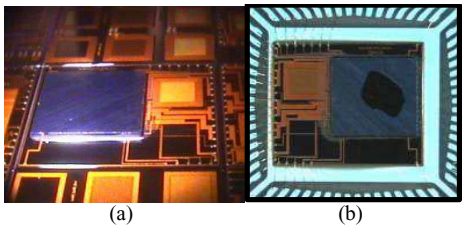


Figure 5. Photograph of the passive-die design



(a) (b)

Figure 6. (a) CMOS die flip-chipped on PICS wafer before dicing, (b) CMOS/PICS sandwich placed in QFP64 package

is sufficient for use in the low-voltage DC-DC converters as considered in this paper.

In a space-saving layout, the output capacitor C_{out} has been realized inside the 20-nH inductor. Since the output capacitance needed to be 75 nF, C_{out} occupied a surface area of 1.3 x 1.3 mm^2 to allow for some overhead for routing the connections to the capacitor electrodes. Since a square planar inductor type was chosen for simplicity of design, this implied that the inner dimension of the inductor needed to be 1.3 mm x 1.3 mm as a boundary condition. A basic mathematical model for planar air coils was used to calculate first-order inductor dimensions that were later optimized using electro-magnetic Momentum™ simulations. This led to an inductor design with 3 turns with 80-µm wide copper tracks spaced 8 µm apart, i.e. the minimum possible distance between two copper tracks. This led to a total area of the LC filter of 1.8 mm x 1.8 mm. The track width of the inductor was chosen as a compromise between parasitic series resistance and area, where the latter was restricted by the available package. The parasitic series resistance is also highly influenced by the length of the aluminum underpass used to contact the inner part of the winding. Moreover, the total area between the copper tracks forming the inductor and the aluminum underpass also determines the resonance frequency of the inductor, which should be significantly higher than the switching frequency. This also led to an optimization constraint, where the resonance frequency was chosen to be roughly 1 GHz. A photograph of a realized 20-nH planar air-core inductor without the capacitor in the middle is shown in Fig. 4. The differential Ground-Signal-Ground (GSG) probe pads for wafer testing of this inductor are shown top left. The position of the underpass has been indicated as well.

Very thin metal fingers have been used to alternately connect to the top and bottom electrodes of C_{out} to reduce eddy-current losses. This also led to splitting the capacitor up in many small-valued parallel capacitors. The copper top metal layer was used for routing for further reduction of the ESR and ESL of the capacitor. Since the bottom electrode of the capacitor had to be connected to the ground node of the DC-DC converter, the connection to this electrode also had to be routed to the outside of the inductor using an underpass. Various thin aluminum tracks were used in parallel here. The optimization criterion in this case was to balance the ESR of the capacitor, which increases with smaller track widths and/or less tracks in parallel, with the inductor resonance frequency that decreases with larger tracks widths and/or more tracks in parallel. Finally, capacitor C_{in} was designed in a similar way as C_{out}, using many small capacitors in parallel. Filling the complete available space underneath the active die with this capacitor maximized its value to roughly 300 nF. A photograph of the passive-die design is shown in Fig. 5. The bumping area for flip-chipping the active die is shown at the bottom, including decoupling capacitor C_{in}. The LC filter with output capacitor C_{out} in the middle can be partly seen at the top of Fig. 5.

The complete SiP was formed by flip-chipping the 0.18-µm CMOS active die facedown on the passive die using gold stud bumps and thermo compression. To reduce the impedance between the power-stage supply and ground connections on the active die and the decoupling capacitor and LC filter on the passive die three bumps were used in parallel for both the V_{in} and GND connections. After placing the active dies on the passive wafer, the passive wafer was diced and the resulting sandwiches of active-die-on-passive-die were bonded in standard QFP64 packages. Photographs of the flipped active die on top of the passive wafer before dicing and the diced CMOS/PICS sandwich inside the QFP64 package are shown in Fig. 6.

IV. Measurement Results

The LC filter has also been laid out separately elsewhere on the PICS wafer to investigate the impact of placing C_{out} inside the inductor. GSG probe pads and proper de-embedding structures were added to allow proper on-wafer characterization of the structures. The full impact of placing the capacitor in the middle of the inductor could not be predicted during design, since electro-magnetic simulation of the complete 3D capacitor structure was not possible with Momentum™. Only the impact of the thin metal connections to the capacitor could be taken into account. Fig. 7 shows the measured

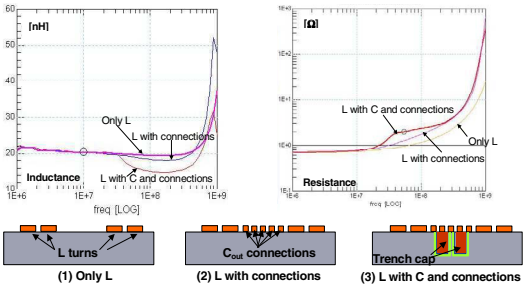


Figure 7. Measured inductance and resistance as a function of frequency for three inductor variants: (1) only L, (2) L with connections, (3) L with C and connections

inductance and resistance of the inductor as a function of frequency for three cases: an inductor with nothing inside (1, see Fig. 4 for a close-up photograph), an inductor with only the capacitor connections inside (2) and an inductor with the complete connected capacitor inside (3, also used in complete passive-die design in Fig. 5), see Fig. 7. The inductance decreases to roughly 16 nH at 50 MHz and the resistance increases to roughly 2 Ω at 50 MHz when the trench capacitor is added (case 3 in Fig. 7). Apparently, eddy-current losses in the diffusions in the capacitor are dominant. This will of course have a negative impact on the efficiency reported below. Resonance of the inductor indeed occurs at roughly 1 GHz.

The measured efficiency for various switching frequencies as a function of output current for an input voltage V_{in} of 1.8 V and fixed duty cycles of 62.4% and 42% are shown in Fig. 8 and Fig. 9, respectively. The same low delay was used for the inverter 6 at all switching frequencies, see Fig. 2. This implies that the maximum dead time between the PMOST switching on and the NMOST switching off equals this externally programmed delay, see Fig. 2.

In both Fig. 8 and Fig. 9, a higher efficiency is achieved for a higher switching frequency at low output currents. This suggests that ohmic losses due to the relatively large current ripple are dominant here. Apparently, these ripple losses are lower for higher switching frequency, implying that decreased ripple current has more impact than increased inductor resistance. For increasing output current the efficiency then increases due to larger output power. For higher switching frequencies the efficiency curve levels off earlier than expected. This is caused by the fact that the inductor current I_L is no longer negative, such that the PMOST is switched on after the externally

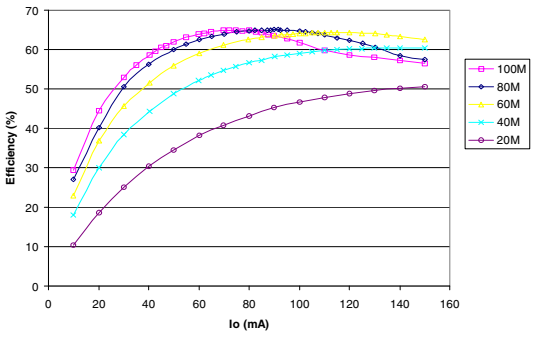


Figure 8. Measured efficiency as a function of output current for various switching frequencies (D=62.4%)

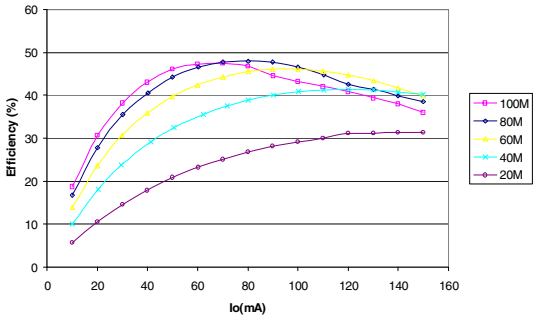


Figure 9. Measured efficiency as a function of output current for various switching frequencies (D=42%)

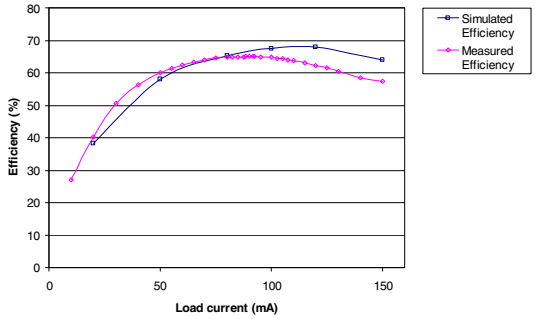


Figure 10. Comparison between simulated and measured efficiency as a function of output current for a switching frequency of 80 MHz and duty cycle of 62.4%

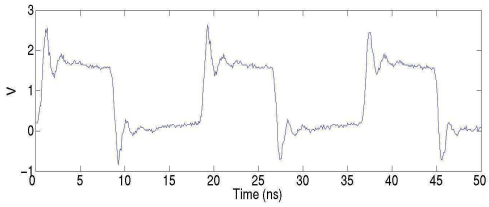


Figure 11. Measured LX-node voltage at a switching frequency of 50 MHz and output current of 15 mA

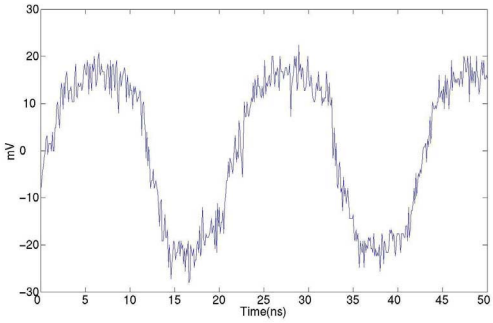


Figure 12. Measured output-voltage ripple at a switching frequency of 50 MHz and output current of 15 mA

controlled delay only. Body-diode conduction losses of the NMOST decrease the efficiency in this case. The higher the switching frequency, the lower the output current for which I_L is no longer negative (smaller ripple current ΔI) and the more impact the programmed delay has on the efficiency. In fact, the ZVS implementation was optimized for use around 50 MHz, where the efficiency is increased by a few percent compared to hard switching and where the alternative path is not used, see Fig. 2. Still, the maximum efficiency for D=62.4%

(V_{out}=1.1 V) is 65%, which is higher than a linear regulator would have for the same voltage conditions. The decrease of efficiency at larger output currents is caused by increased ohmic losses in combination with a lower increase in output power than anticipated. This latter aspect is caused by the absence of a control loop, which would vary the duty cycle such that V_{out} would remain constant at higher output current. The peak efficiencies at D=42% in Fig. 9 are lower at roughly 48%, compared to the peak efficiencies of 65% at D=62.4% in Fig. 8. This is caused by the lower output power at the same output current, since V_{out} is lower due to the lower duty cycle.

Fig. 10 shows a comparison between simulated and measured efficiency at a switching frequency of 80 MHz and a duty cycle of D=62.4%. An equivalent-circuit model was used for the inductor, which was fitted to the measurement results of 'L with C and connections' in Fig. 7. The simulations in Fig. 10 revealed that the main cause for the relatively low peak efficiency is the total ohmic resistance in the current path, which leads to substantial losses due to the relatively high ripple current ΔI to enable ZVS operation. Ohmic losses can be substantially reduced by moving C_{out} outside the inductor and by decreasing the on-chip connection resistance to the power switches. This would improve efficiency.

Fig. 11 shows the measured voltage at the LX node at a switching frequency of 50 MHz and an output current of 15 mA. The observed ringing in the LX-node voltage was caused by the measurement probe. No internal supply ringing was observed using additional sense wires to sense the internal supply voltages. This illustrates the effectiveness of the decoupling of the power stage. Due to the relatively low output current, the LX-node voltage indeed becomes positive at the end of the conduction period of the NMOST. This implies that the inductor current has reversed and that the ZVS scheme is functional in this case. Moreover, no body-diode losses can be observed from Fig. 11.

The output ripple voltage of the integrated DC-DC down converter for the same conditions as valid in Fig. 11 is shown in Fig. 12. The peak-to-peak ripple voltage is 35 mV, which is roughly a factor of two higher than the value of 15 mV for an ideal output capacitor described in section II. This is partly caused by the fact that the inductance is only 16 nH at 50 MHz. Another reason is that non-idealities in the output capacitor will increase the ripple voltage.

The realized integrated DC-DC down converter has a maximum input voltage of 1.8 V due to the used 0.18-µm CMOS process. Enabling Li-ion-battery input voltages by applying layout tricks in standard CMOS would enable a more favorable comparison between integrated DC-DC converters and linear regulators [16]. Since higher switching voltages would be used in this case, this would also be a better test case for implementation of ZVS measures.

V. CONCLUSIONS

An integrated inductive DC-DC down converter has been realized by flip-chipping a 0.18-µm CMOS active die containing the power stage, drivers and PWM signal generator on a passive-integration die containing the input decoupling capacitor and the output LC filter. The passive-integration process is based on trench-MOS capacitors and achieves an 80-nF/mm^2 capacitance density. An 8-µm thick copper top metal layer enables the integration of planar air-core inductors. The realized SiP does not need any external components and achieves a maximum efficiency of 65% at a switching frequency of 80 MHz, an input voltage of 1.8 V, an output voltage of 1.1 V and an output current of 100 mA. Future steps include optimizing the LC filter by moving the output capacitor outside the inductor, decreasing the connection resistances of the power switches and allowing direct Li-ion battery connection using layout tricks to implement high-voltage power switches in nm-CMOS. Application of integrated inductive DC-DC down converters is envisioned for enabling system integration of power management.

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