

Single-electron tunneling in InP nanowires

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Single-electron tunneling in InP nanowires

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We report on the fabrication and electrical characterization of field-effect devices based on wire-shaped InP crystals grown from Au catalyst particles by a vapor–liquid–solid process. Our InP wires are *n*-type doped with diameters in the 40–55-nm range and lengths of several micrometers. After being deposited on an oxidized Si substrate, wires are contacted individually via e-beam fabricated Ti/Al electrodes. We obtain contact resistances as low as ~ 10 k Ω , with minor temperature dependence. The distance between the electrodes varies between 0.2 and 2 μm . The electron density in the wires is changed with a back gate. Low-temperature transport measurements show Coulomb-blockade behavior with single-electron charging energies of ~ 1 meV. We also demonstrate energy quantization resulting from the confinement in the wire. © 2003 American Institute of Physics. [DOI: 10.1063/1.1590426]

Chemically synthesized semiconductor nanowires (or nanowhiskers) are attracting increasing interest as building blocks for a bottom-up approach to the fabrication of nanoscale devices and sensors. A key property of these material systems is the unique versatility in terms of geometrical dimensions and composition. Nanowires have already been grown from several semiconductor materials (group-IV elements,^{1,2} III-V,^{3–6} and II-VI compounds⁷), including structures with variable doping and composition, such as *n*-type/*p*-type InP,⁸ InAs/InP,⁵ GaAs/GaP,⁸ and Si/SiGe.² The growth technique is based on the vapor–liquid–solid (VLS) process⁹ occurring at metallic catalysts, such as nanometer-sized Au particles. The nanowire diameter is set by the catalyst dimension, typically 10–100 nm. The nanowire length is proportional to the growth time and can exceed hundreds of micrometers. The semiconductor is provided either by metalorganic vapor-phase sources,^{3,5} or by laser ablation.¹⁰ Many room-temperature applications have already been shown, such as single-nanowire field-effect transistors (FETs),⁴ diodes,⁸ and logic gates¹¹ combining both *n*-type and *p*-type nanowires. Very recently, nanowire heterostructures have been operated as resonant tunneling diodes at 4.2 K.¹² Yet, the low-temperature properties of nanowires and their potential for quantum devices are still widely unexplored.

In this letter, we describe the realization of FET devices from individual *n*-type InP nanowires. We discuss their transport properties down to 0.35 K, where single-electron tunneling and quantum effects can play a dominant role. We also provide details on the fabrication of the electrical contacts to the nanowires, a crucial aspect of the present work.

Our InP nanowires are grown via the laser-assisted VLS

method. A pulsed laser (193-nm ArF laser, 10 Hz, 100 mJ/pulse) is used to ablate from a pressed InP powder enriched with 1 mol% of Se, which acts as a donor impurity in InP. Nanowires grow from Au seeds formed after annealing a 2-Å-equivalent Au film deposited on a Si substrate with a superficial native oxide. During growth time (~ 30 min) the substrate temperature is kept at 475 °C. The resulting nanowires are 5–10 μm long with a diameter of 40–55 nm.

Immediately after growth, the nanowires are dispersed in chlorobenzene. A few droplets of this dispersion are deposited on a *p*⁺ Si substrate with a 250-nm-thick SiO₂ overlayer. To favor the adhesion of the nanowires, the surface is functionalized with a self-assembled monolayer of 3-aminopropyltriethoxysilane (APTES).¹³ Optical imaging is used to locate the nanowires with respect to a reference pattern of predefined Pt markers. The nanowires are then individually contacted with a pair of metal electrodes (source and drain leads) defined by electron-beam lithography (see upper inset to Fig. 1). The distance *L* between the source and drain electrodes is varied between 0.2 and 2 μm .

The contact electrodes consist of thermally evaporated Ti(100 nm)/Al(20 nm). Before metal deposition, samples are treated with BHF for 20 s in order to etch the oxide layer around the nanowires.¹⁴ As-deposited contacts show high resistance, typically in excess of 10 G Ω . The contact resistance improves drastically after forming-gas rapid thermal annealing at 475 °C for 60 s (for a discussion of the interface reaction between Ti and InP we refer to Ref. 15).

We have characterized over ten devices at different temperatures *T*. At room temperature, *I*–*V* characteristics are linear (see dashed lines in Fig. 1), with resistances *R* as low as 30 k Ω . Despite sample-to-sample fluctuations, *R* appears to increase with *L*, as shown in the lower inset to Fig. 1. A linear fit yields $R = 40 \text{ k}\Omega + 45 \text{ k}\Omega/\mu\text{m} \times L$, where the con-

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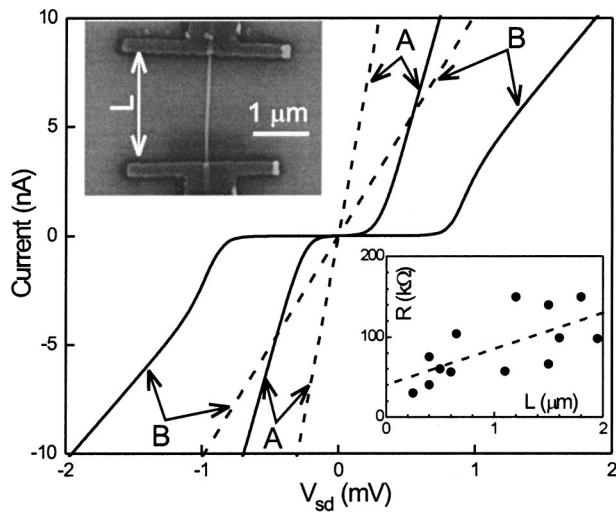


FIG. 1. I - V characteristics at room temperature (dashed lines) and 0.35 K (solid lines), for devices A and B. Upper inset: scanning-electron micrograph of device B. Lower inset: length dependence of the room-temperature source-drain resistance. Each solid circle refers to a different device. The dashed line is a linear fit.

stant term and the slope coefficient can be taken as rough estimates of the total contact resistance and the wire resistivity, respectively.

Below a few Kelvin, the I - V characteristics develop a nonlinearity around zero bias. This behavior, common to all measured devices, is shown in Fig. 1 for device A ($L=0.20 \mu\text{m}$), and B ($L=1.95 \mu\text{m}$), respectively the shortest and longest devices measured. The zero-bias suppression of the conductance has a pronounced dependence on the voltage V_g applied to the p^+ Si substrate. This is a characteristic fingerprint of Coulomb-blockaded transport, which becomes dominant at low temperatures. In fact, an electronic island, formed inside the nanowire segment between source and drain electrodes, leads to Coulomb blockade of transport when $k_B T < e^2/C$, where C is the total capacitance of the island.¹⁶ At source-drain voltages, V_{sd} , larger than e/C , the slope of the low- T trace is close to the corresponding room- T value, indicating little T -dependence of the contact resistance.

Figure 2(a) shows conductance G versus V_g for device C ($L=0.65 \mu\text{m}$) and D ($L=1.6 \mu\text{m}$, inset). Both traces exhibit sharp peaks corresponding to Coulomb-blockade oscillations. This clearly demonstrates that we have achieved single-electron control over the electronic charge and the transport properties of the nanowire. The Coulomb peaks have irregularly distributed sizes, and their V_g -spacing varies considerably, suggesting the formation of more than one electronic island along the nanowire. This interpretation is supported by the measurement shown in Fig. 2(b) where the differential conductance dI/dV_{sd} of device C is plotted on gray scale as a function of (V_g, V_{sd}) . In this plot, Coulomb blockade takes place within dark regions with the characteristic diamond shape. In some cases, such as for V_g between -40 and -90 mV, Coulomb diamonds are clearly separated from each other and have all their edges fully defined. This is characteristic of Coulomb-blockaded transport through a single electronic island. In other V_g -regions, however, diamonds overlap with each other, as we would expect for a

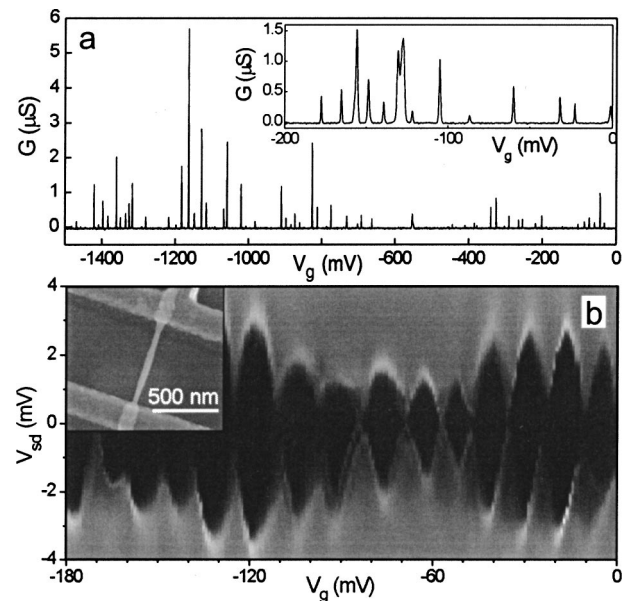


FIG. 2. (a) Conductance G versus back-gate voltage V_g measured at 0.35 K with a dc bias $V_{sd}=20 \mu\text{V}$. The two traces refer to devices C and D (inset). (b) Gray-scale plot of differential conductance dI/dV_{sd} versus (V_g, V_{sd}) . dI/dV_{sd} increases when going from dark to light gray. The measurement refers to device C, and was taken at 0.35 K with a lock-in technique at an ac bias excitation of $20 \mu\text{V}$. Inset: scanning electron micrograph of device C.

nanowire containing more than one (most likely two) islands in series. The V_g -dependent alternation of single- and double-island regimes, shown in Fig. 2(b), is representative of the general behavior in our devices. We would like to stress that such charge reconfigurations are found to be very stable and reproducible.

Each Coulomb diamond is associated with a well-defined number N of confined electrons. From the half-height (along V_{sd}) of the diamonds we estimate a charging energy $e^2/C \sim 1$ meV. The V_g -width of the diamonds is around 10–20 mV, from which we deduce $C_g/C \approx 1/7$, where C_g is the capacitance to the back gate.¹⁷ This implies that N decreases by ~ 100 when moving from right to left in Fig. 2(a). Based on separate studies,¹⁸ we believe this is still only a small fraction of the total amount of conduction electrons in the nanowire.

We now focus on a small V_g -range where device C exhibits single-island behavior. Figure 3 shows several dI/dV_{sd} vs V_g traces taken at different values of V_{sd} between 0 and -0.6 mV. The lowest trace ($V_{sd}=0$) shows two Coulomb peaks denoting transitions between successive charge states: say from $N-1$ to N (left peak), and from N to $N+1$ (right peak). At finite bias, each peak in dI/dV_{sd} splits proportionally to V_{sd} , as expected from ordinary Coulomb-blockade theory. The left-moving (right-moving) split-peak corresponds to the onset of tunneling from (to) the source (drain) lead. Interestingly, at larger V_{sd} , extra resonances appear between the split-peaks. Increasing V_{sd} , the V_g -positions of such resonances evolve parallel to one of the split-peaks, as emphasized by dashed lines. We recognize this behavior as characteristic of transport through a quantum-dot system with a discrete energy spectrum.¹⁹ The two extra resonances can be readily explained as the result of tunneling processes involving excited states of the quantum dot. The resonance on the right side of Fig. 3 denotes the onset of tunneling from

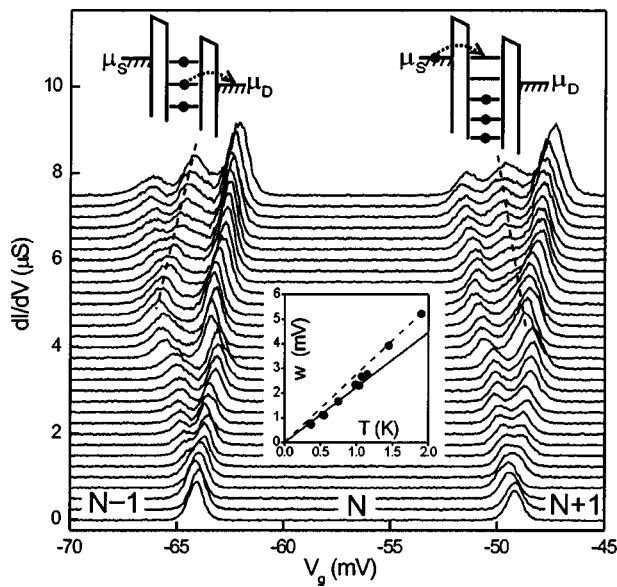


FIG. 3. dI/dV_{sd} vs V_g , for different dc values of V_{sd} , from 0 (lower trace) to -0.6 mV (upper trace) in steps of -0.02 mV. Dashed lines indicate the evolution of the peaks associated with tunneling via excited states. A simplified picture of the corresponding processes is given in the top insets. Bottom inset: full width at half-maximum w vs temperature T for the left Coulomb peak at $V_{sd}=0$. The solid (dashed) line is the theoretical prediction, $w = (C/eC_g) \times 3.52k_B T$ [$w = (C/eC_g) \times 4.35k_B T$], for the quantum (classical) regime (see Ref. 20). We used $C/C_g = 7.35$, obtained from the V_{sd} -dependence of the V_g -splitting.

the source lead to the first excited state with $N+1$ electrons (see top-right inset). The one on the left can be ascribed to the tunneling of an electron from the dot to the drain, which leaves the dot in an excited state with $N-1$ electrons (see top-left inset). The bias voltage for which the resonance associated to an N -electron excited-state begins to emerge is a direct measurement of the corresponding excitation energy, $\Delta E(N)$. We find $\Delta E(N-1) \approx 0.36$ MeV and $\Delta E(N+1) \approx 0.30$ meV.

Another sign of energy quantization is based on the T -dependence of the conductance peaks at $V_{sd}=0$. As expected for single-electron tunneling in quantum dots, lowering T gives an increased peak height as a result of resonant tunneling.¹⁶ This is, in fact, observed in the low- T limit (data not shown). The full width at half-maximum increases linearly with T , but with two different slopes, associated with the quantum ($k_B T < \Delta E$) and the classical ($k_B T > \Delta E$) regime.²⁰ In our case, the transition between the two regimes occurs at about 1.2 K [see Fig. 3(b)] corresponding to $\Delta E \sim 0.1$ meV, in agreement with the previous findings. Our observation of a discrete energy spectrum represents an im-

portant premise for a deeper investigation of quantum phenomena and the development of controllable quantum devices based on semiconductor nanowires.

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