An adaptive digital caliration of multi-step A/D converters.

Citation for published version (APA):
Zjajo, A., & Pineda de Gyvez, J. (2010). An adaptive digital caliration of multi-step A/D converters. In *Proceedings of the 2010 IEEE 10th International Conference on Signal Processing (ICSP), 24-28 October 2010, Beijing, China* (pp. 2456-2459). Institute of Electrical and Electronics Engineers. https://doi.org/10.1109/ICOSP.2010.5657033

DOI:
10.1109/ICOSP.2010.5657033

Document status and date:
Published: 01/01/2010

Document Version:
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

An Adaptive Digital Calibration of Multi-Step A/D Converters

Amir Zjajo
Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands

Jose Pineda de Gyvez
Eindhoven University of Technology
Den Dolech 2, 5612 AZ Eindhoven, The Netherlands

***Abstract*— A novel digital technique for efficient calibration of static errors in high-speed, high-resolution, multi-step ADCs is proposed. The parameter update within the calibration method is extended to include and correct effects of temperature and process variations. Additionally, to guide the verification process with the information obtained through monitoring process variations, expectation-maximization method is employed. The algorithm is evaluated on a prototype multi-step ADC converter with embedded dedicated sensors fabricated in standard single poly, six metal 0.09-µm CMOS.**

Keywords-calibration, sensors, process variation

I. INTRODUCTION

The static parameters of the multi-step A/D converter are determined by the analog errors in various A/D converter components and therefore, a major challenge in A/D converter calibration is to estimate the contribution of those individual errors to the overall A/D converter linearity parameters. The observation of important design and technology parameters, such as temperature, threshold voltage, etc., is enhanced with dedicated sensors embedded within the functional cores [1]. The steps causing discontinuities in the A/D converter's stage transfer functions can be analyzed, minimized or corrected with a wide variety of calibration techniques [2]-[4]. The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. In general, most of the calibration methods require that a reference signal is available in the digital domain, this being the signal that the actual stage output of the A/D converter is compared with. This reference signal is in the ideal case a perfect, infinite resolution, sampled version of the signal applied to the A/D converter under test. Nevertheless, in a practical situation, the reference signal must be estimated in some way. This can be accomplished by incorporating auxiliary devices such as a reference A/D converter, sampling the same signal as the A/D converter under test [2], or a D/A converter feeding a digitally generated signal to the A/D converter under test [3].

In this paper, such an A/D converter is augmented with dedicated sensors embedded within the converter to supplement the circuit calibration and to guide the verification process with the information obtained through monitoring process. As the number of on-chip sensors is finite due to area limitations, additional informations are obtained through the imputation method and its special case, multiple imputations based on expectation-maximization (EM) algorithm [5], which simultaneously minimizes the empirical classification error and maximizes the geometric margin. Furthermore, the proposed design-for-test (DfT) capabilities offer possibilities to estimate the reference signal for each individual stage by applying the steepest-descent processing method [6] to the output of the observed A/D converter. Additionally, in the proposed method the overlap between the conversion ranges of two stages is considered to avoid conflicting operational situations that can either mask faults or give an incorrect interpretation.

II. CALIBRATION ALGORITHM

Even though extensive research [7]-[10] has been done to estimate the various errors in different A/D converter architectures, the use of DfT and dedicated sensors for the analysis of multi-step ADCs to update parameter estimates has been negligible. The influence of the architecture on analog-to-digital converter modeling is investigated in [7], and in [8] with use of some additional sensor circuitry, pipeline A/D converter are evaluated in terms of their response to substrate noises globally existing in a chip. In [9], the differential nonlinearity test data is employed for fault location and identification of the analog components in the flash converter and in [10] is shown how a given calibration data set may be used to extract estimates of specific error performance.

Functional fault in each of the analog component in the multi-step A/D converter affects the transfer function differently [9] and analyzing this property form the basis of our approach. The overall examined multi-step A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers (Figure 1). In m+n+q multi-step A/D converter the m most significant bits are found from the first resistance ladder, the n mid bits are created in mid resistance ladder and the q least significant bits are generated from the third resistance ladder. Usually, the full range of the second resistance ladder is longer than one step in the first ladder. With this over-range compensation in the second ladder (e.g. similar principle is applicable to the third ladder as well) the static errors can be corrected since the signal still lies in the range of the second ladder. This means that the output of the A/D converter is redundant and it is not possible, from the digital output, to find the values from each subranging step without employing dedicated DfT. To set the inputs of the individual A/D converter stages at the wanted values, a scan-chain is available in the switch-matrix circuit. For mid-range A/D converter measurements, the coarse A/D converter values are prearranged since they determine mid-range A/D converter

978-1-4244-5900-1/10/$26.00 ©2010 IEEE

references, and similarly to evaluate the fine A/D converter both coarse and mid A/D converters decisions are set to predetermined value. The response of each of the individual A/D converter stages is subsequently routed to the test bus. The sub-D/A converter (implemented as a combination of the reference ladder and the switch matrix) settings are controlled by serial shift of data through a scan chain that connects all sub-D/A converter registers in serial. To capture the current settings of the sub-D/A converter, it is possible to freeze the contents of the sub-D/A converter registers in normal mode and shift out the data via the scan-chain. A test control bit per sub-D/A converter is available to adjust (increase) the reference current to obtain an optimal fit of sub-D/A converter output range to the A/D converter input range.

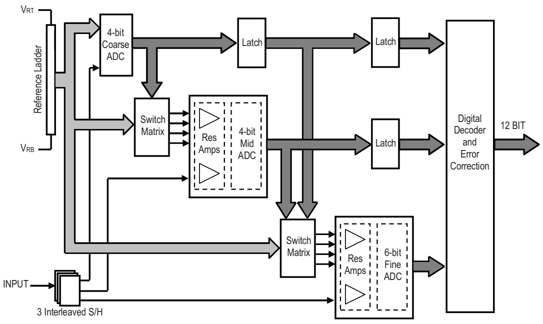

Figure 1: Block diagram of the 12-bit multi-step A/D converter.

Although a multi-step A/D converter makes use of considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. The conversion process therefore is susceptible to analog circuit and device impairments. If timing errors are not considered, the primary error sources present in a multi-step A/D converter are systematic decision stage offset errors (λ), stage gain errors (η), and errors in the internal reference voltages (γ). To facilitate the measurement of these fluctuations, the evaluation strategy as depicted in Figure 2 is proposed.

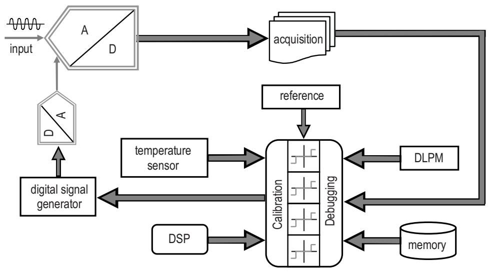

Figure 2: Conceptual view of the calibration loop.

The algorithm inputs are A/D converter measurement data, outputs of die-level process monitor (DLPM) circuits and temperature sensors and references needed to make a decision. The algorithm gives required information to the digital signal generator, whose outputs steer the sub-D/A converter, thereby closing the calibration loop. The DLPM measurements are directly related to asymmetries between the branches composing the circuit; for all primary error sources, we derive separate DLPMs by extracting (replicating) the targeted error contributor. Statistical data extracted through the die-level process monitor measurements provide the estimates $(W')^T=[\eta',\gamma',\lambda']$ with an initial value. It is important to note that because of the imbalanced utilization and diversity of circuitry at different sections of an integrated circuit, temperature can vary significantly from one die area to another and that these fluctuations in the die temperature influence the device characteristics thereby altering the performance of integrated circuits. In the implemented system, the temperature sensor [11] registers any on-chip temperature changes, and, if required, updates the estimation algorithm. The procedure to calibrate the entire multi-step A/D converter starts firstly from stage i to find the residue voltage V_{i+1} from back-end A/D converter output. Next, the stage input V_i based on the algorithm output V_{i+1} is recovered and at the end, first two steps to calibrate stage *i-1* are repeated until the first stage is reached. The calibration state machine controls the reference voltage switching in the D/A converters of the first two stages during the calibration hold phases. During normal operation calibration coding is simply the addition of two coefficients, which are selected according to the raw bits of the two first stages, to each un-calibrated A/D converter output word.

Calibration Algorithm

Initialization
- Initialize the input vector $D_{in}(0)$
- Force the inputs and collect the desired output $D_{out}(0)$
- Measure and set the initial value of the weights $W'(0)$
- Initialize the steepest descent update step μ=1
- Initialize the forgetting factor ζ

Data collection
- Collect N samples from the DLPM and temperature sensors
- Collect N samples from the AD converter

Update parameter estimate
1. Update the input vector $D_{in}(t+1)$ based on current available $W(t)$
2. Calculate the error estimate $W'(t)$
3. Generate the output estimate $D'_{out}(t)= D_{in}(t)\times W'(t)$
4. Calculate the estimation error $e(t) = D'_{out}(t)-D_{out}(t)$
5. Calculate the error estimate $W'(t+1)= W'(t)-\mu\times D_{in}(t)\times e(t)$
6. If $W'(t+1)> W'(t)$ decrease step size μ and repeat step 5
7. Increase the iteration index, t and repeat steps 1-6 for best estimate
8. If temperature changes update W_l' with new estimate W'

III. Algorithm for Process Variation Monitoring

Given the observation vector of the sensor's observations $x_i\in X$, the estimation of an unknown parameter vector $\theta\in\Theta$ designating true values of die-level process parameter variation would be relatively an easy task if the missing data vector $y_i\in Y$, assumed to be realizations of the random variables which are independent and identically distributed according to the probability $p_{XY|\Theta}(x,y|\theta)$, were also available. In this sense, the maximum likelihood (ML) estimation involves estimation of θ for which the observed data is the most likely, e.g. marginal probability $p_{X|\Theta}(x|\theta)$ is a maximum, where $p_{X|\Theta}(x|\theta)$ is the Gaussian mixture model given by the weighted sum of the Gaussian distributions. The parameters θ involve parameters (μ_y,Σ_y), $y\in Y$ of Gaussian components and the values of the discrete distribution $p_{Y|\Theta}(y|\theta)$, $y \in Y$. The logarithm of the probability $p(T_X|\theta)$ is referred to as the log-likehood $L(\theta|T_X)$ of θ with respect to the input set $T_X=\{(x_1,...,x_l)\}$, which contains only vectors of sensor's observations x_i. Obtaining optimum estimates through ML method thus involves two steps: computing the likelihood function and maximization over the set of all admissible sequences. To evaluate the contribution of the random parameter θ, analysis of the likelihood function requires computing an expectation over the joint statistics of the random parameter vector, a task that is analytically intractable. Even if the likelihood function can be obtained analytically off line, however, it is invariably a nonlinear function of θ, which makes the maximization step (which must be performed in real time) computationally infeasible. In such cases, the expectation-maximization algorithm provides a solution, albeit iterative, to the ML estimation problem. If some observations are missing, the algorithm allows obtaining the maximum likelihood estimates of the unknown parameters by a computational procedure which iterates, until convergence, between two steps. At each step of the EM iteration, the likelihood function can be shown to be non-decreasing [12]; if it is also bounded (which is mostly the case in practice), then the algorithm converges. In [13] is proved that an iterative maximization of $Q(\theta|\theta^{(t)})$ will lead to a maximum likelihood estimation of θ. For a broad class of probability density functions, including Gaussian mixture densities, at each iteration the new parameter estimate θ can be explicitly solved as the stationary point corresponding to the unique maximum of $Q(\theta|\theta^{(t)})$[12].

EM Algorithm

Initialization
- Initialize the data set $T_{XY}=\{(x_1, y_1),...,(x_l, y_l)\}$
- Initialize the parameter $\theta^{(0)}$

Data collection
- Collect N samples from the DLPMs

Update parameter estimate
1. Calculate $Q(\theta|\theta^{(n)})=E(\log p(X,Y|\theta)X, \theta^{(n)})$ – E step
2. Re-estimate θ by maximizing the θ-function $\theta^{(n+1)}=argmax_\theta\, Q(\theta|\theta^{(n)})$, estimate mean and variance – M step
3. Increase the iteration index, n
4. Stop when a stationary point $L(\theta^{(n-1)}|T_{XY})=L(\theta^{(n)}|T_{XY})$ is found.

IV. Experimental Results

The prototype of the multi-step A/D converter with dedicated embedded sensors was fabricated in standard single poly, six metal 0.09-μm CMOS. The core area is 0.6 mm^2 excluding bond pads. The A/D converter operates at 1.2 V supply voltage and dissipates 85 mW (without output buffers). In Figure 3 a micrograph of the test-chip is presented. Dedicated embedded sensors and the complete DfT occupy less than 10% of the overall area. Additionally, the test-chip contains a temperature sensor (located between coarse A/D converter and fine residue amplifiers) and matrix of one hundred and forty differential transistor pairs and ladder resistors divided into specific groups, which are placed in and around the partitioned multi-step A/D converter. Digital correction is at the lower right corner of the active area; and twelve bit output is produced at the pads on the bottom. The differential circuit topology is used throughout the design and multiple substrate taps are placed close to the noise sensitive circuits to avoid the noise injection. Repetitive single die-level process monitor measurements for each group of monitors are performed to minimize noise errors. Since the different transistors are measured sequentially the dc repeatability of the dc gate voltage source must be larger than the smallest gate-voltage offset to be measured. The repeatability of the source in measurement set-up was better than six digits, which are more than sufficient. The mixtures of Gaussians are initialized by applying the EM equations to the observed mixtures of two univariate Gaussian components based on die-level process monitors and coarse A/D converter DNL measurements. Each iteration is guaranteed to increase the likelihood, and finally the algorithm converges to a local maximum of the likelihood function in less than fifty iterations for the mean μ and a hundred and twenty for the variance σ, respectively.

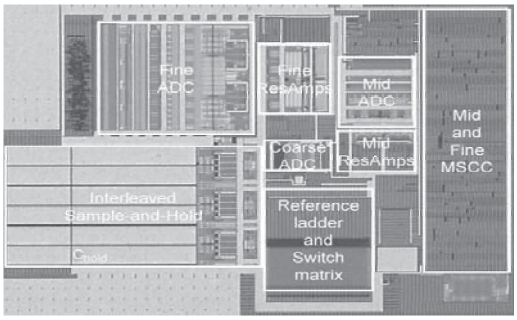

Figure 3: Chip micrograph

The calibration technique was verified in all stages with full scale inputs. If the analog input to the calibrated A/D converter is such that the code transition is i, then the code transition of the ideal A/D converter is either i or i+1. The offset between the digital outputs of these two converters for the range of analog inputs is denoted Δi_1 and Δi_2, respectively. If a calibrated A/D converter have no errors in the internal reference voltages γ and stage gain errors η, the difference between calibrated and ideal A/D converter outputs is constant regardless of the analog input, thus $\Delta i_1 = \Delta i_2$. If errors in the internal reference voltages γ and stage gain errors η are included, calibrated A/D converter incurs unique missing codes. The difference between Δ_{i1} and Δ_{i2} precisely gives the error due to missing codes that occurs when ideal A/D converter changes from i to $i+1$. In a similar manner the unique error due to missing codes at all other transitions can be measured for calibrated A/D converter. With the errors from missing codes at each transition measured, calibrated A/D converter stage is corrected by shifting converter's digital output as a function of the transition points such that overall transfer function of calibrated A/D converter is free from missing codes. As long as the input is sufficiently rapid to generate a sufficient number of estimates of Δ_{i1}, Δ_{i2}, for all i, there is no constraint on the shape of the input signal to the A/D converter. Constant offset between calibrated and ideal A/D converter appears as a common-mode shift in both Δ_{i1} and Δ_{i2}.Since the number of missing codes at each code transition is measured by subtracting Δ_{i2} from Δ_{i1}, the common mode is eliminated and thus input-referred offsets of calibrated A/D converter have no impact in the calibration scheme (under the practical assumption that the offsets are not large enough to saturate the output of the converter stages).

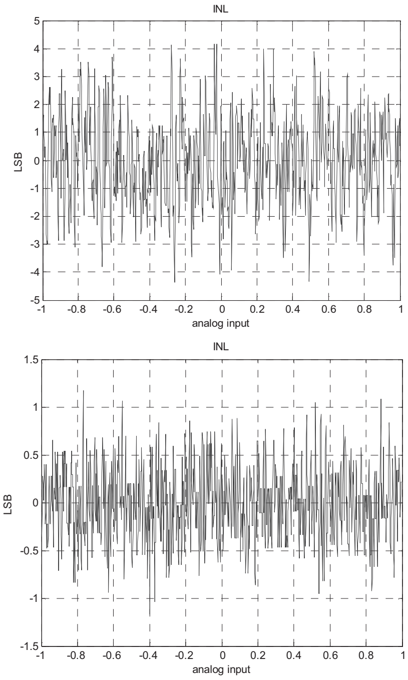

Figure 4: *top)*, INL curve before calibration. The INL is mainly caused by the ladder non-linearity. Errors affecting the reference divider introduce transition position errors since the transitions do not coincide with the range of the next stage; *bottom),* INL curve after calibration.

The largest correction values significantly decrease with the amount of samples. To account for an overall internal reference voltages γ, stage gain errors η and systematic offset λ, the algorithm provides the estimates with the final values $(W')^T=[\gamma',\eta',\lambda']$. As ideal A/D converter offers an ideal reference for calibrated A/D converter, the error signal used for the algorithm adaptation (which is formed by the difference of the two A/D converter outputs) is highly correlated with the error between them, thus steady state convergence of occurs within a relatively short time interval. At first, μ was set to 1/4 to speed up the algorithm, and then μ equal to 1/64 after 1000 iteration times to improve the accuracy. The advantage of the proposed method is that it gives unbiased estimates, so that the estimation accuracy can be made arbitrarily good by increasing the amount of estimation data. Although the accuracy increase quite slowly with the amount of data, evaluated A/D converter, however, use very high sample rates (above 50 MS/s) so some million samples are collected in less than second. The peak improvement is ±0.2 LSB for DNL measurement and ±2.9 LSB for INL (Figure 4). The calibration algorithm operates in all process corners and has a temperature range from 0-150ºC with a resolution of 9ºC. Table 1 illustrates the measurement results for coarse, mid, fine and total A/D converter.

	Coarse	Mid	Fine	Total
DNL	*± 0.4 LSB*	*± 0.5 LSB*	*± 0.6 LSB*	*± 0.7 LSB*
INL	*± 0.6 LSB*	*± 0.6 LSB*	*± 0.9 LSB*	*± 1.1 LSB*
THD	*-24.7 dB*	*-26.1 dB*	*-35.8 dB*	*-73 dB*
SNR	*28.3 dB*	*25.5 dB*	*37.4 dB*	*67 dB*

TABLE I – TEST RESULTS – MEAN VALUES

V. CONCLUSION

With the use of dedicated sensors, we facilitate early and fast identification of excessive process parameter variation effects at the cost of at maximum 10% area overhead. The flexibility of the concept allows the system to be easily extended with a variety of other performance sensors. The feasibility of the method for on-line and off-line calibration has been verified by experimental measurements from the Silicon prototype.

REFERENCES

[1] V. Petrescu, M. Pelgrom, H. Veendrick, P. Pavithran, J. Wieling, “Monitors for a Signal Integrity Measurement System”, *Proceedings of IEEE European Solid-State Circuit Conference*, pp. 122-125, 2006

[2] J. Tsimbinos, K.V. Lever, “Improved Error-Table Compensation of A/D Converters”, *IEE Proceedings - Circuits, Devices and Systems*, vol. 144, no. 6, pp. 343-349, 1997

[3] P. Händel, M. Skoglund, M. Pettersson, “A Calibration Scheme for Imperfect Quantizers”, *IEEE Transactions on Instrumentation and Measurement*, vol. 49, no. 11, pp. 1063-1068, 2000

[4] J.A. McNeill, M.C.W. Coln, D.R. Brown, B.J. Larivee, “Digital Background-Calibration Algorithm for “Split ADC” Architecture”, *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 56, no. 2, pp. 294-306, 2009

[5] G.J. McLachlan, T. Krishnan, *The EM algorithm and Extensions*, Wiley-Interscience, 1997

[6] J.E. Dennis, R.B. Schnabel, *Numerical Methods for Unconstrained Optimization and Nonlinear Equations*, Prentice-Hall, 1983

[7] P. Arpaia, P. Daponte, L. Michaeli, “Influence of the architecture on ADC error modelling”, *IEEE Transactions on Instrumentation and Measurement*, vol. 48, pp. 956-966, 1999

[8] K. Noguchi, T. Hashida, M. Nagata, “On-Chip Analog Circuit Diagnosis in Systems-on-Chip Integration”, *Proceedings of IEEE European Solid-State Circuit Conference*, pp. 118-121, 2006

[9] A. Charoenrook, M. Soma, “A Fault Diagnosis Technique for Flash ADC’s”, *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 43, pp. 445-457, 1996

[10] F.H. Irons, D.M. Hummels, I.N. Papantonopoulos, C.A. Zoldi, “Analog-to-Digital Converter Error Diagnosis”, *Proceedings of IEEE Instrumentation and Measurement Technology Conference*, pp. 732-737, 1996

[11] D. Schinkel, R.P. de Boer, A.J. Annema, A.J.M. van Tuijl, “A 1-V 15μW high-precision temperature switch”, *Proceedings of European Solid-State Circuit Conference*, pp. 77-80, 2001

[12] S. P. Lloyd, “Least Squares Quantization in PCM”, *IEEE Transactions on Information Theory*, vol. 28, no. 2, pp. 129-137, 1982

[13] C.H. Brown, “Asymptotic Comparison of Missing Data Procedures for Estimating Factor Loadings”, *Psychometrika,* vol. 48, pp. 269-292, 1983