A 70 GHz 10.2 mW self-demodulator for OOK modulation in 65-nm CMOS technology

A 70 GHz 10.2 mW Self-Demodulator for OOK Modulation in 65-nm CMOS Technology

Xia Li[1], Peter Baltus[1], Paul van Zeijl[2], Dusan Milosevic[1], Arthur van Roermund[1]

1 Eindhoven University of Technology, Eindhoven, 5600 MB, The Netherlands
2 Philips Research Eindhoven, Eindhoven, 5656 AE, The Netherlands

***Abstract* — A 70.86 to 79.29 GHz low-power self-demodulator for on-off-keying (OOK) modulation is realized in TSMC 65-nm CMOS technology. By using a frequency-sweeping injection-locked oscillator (IJLO), the OOK modulated 70 GHz signal is demodulated by itself in a passive mixer and an 8.43 GHz bandwidth is achieved at 10.2 mW power consumption from a 1-V supply. The conversion gain is 10 dB and constant over the entire bandwidth. The core area of the chip is 0.072 mm^2.**

***Index Terms* — Self-demodulator, injection-locked oscillator, frequency-sweeping tuning, on-off-keying, low power, passive mixer, CMOS.**

I. Introduction

Millimeter-wave (mmW) wireless communication draws lots of interest due to its capability to offer several GHz bandwidth and support multi-gigabit data rate. The typical applications are, for instance, point-to-point (p2p) data links, automotive radars, imaging and short-range communication like the wireless personal-area networks (WPAN). The on-chip quality factor of inductors in CMOS technology proves to be higher at such high frequencies while their sizes shrink on the other hand [1]-[2]. Moreover, the deep sub-micron CMOS technology, e.g. 65 nm CMOS is able to provide with an f_T up to 200 GHz, which enables the development of mmW circuits [3].

Power consumption becomes one of the bottlenecks of high data-rate mmW circuits, because the power dissipation historically increases sub-linearly with the data rate [4]. In order to decrease the power consumption, direct down-conversion receiver structure is preferably used to save the extra IF local oscillator (LO) and mixer power compared with the superheterodyne architecture. Besides, simple modulation scheme like on-off-keying (OOK) is often chosen due to its low complexity and low requirement for the system linearity.

To reduce the average power consumption, the low duty-cycle radio is a widely used approach except in the real-time or high-definition data streaming applications. The settling time of the receiver in such a radio becomes critical, which requires a fast LO path in the demodulator. However, a conventional oscillator with a phase-locked-loop (PLL) typically takes 40 to 300 μs to start up [5], which results in a 40kb to 0.3 Mb overhead per data packet assuming 1-Gbps data rate and a considerable part of power consumed during the settling period.

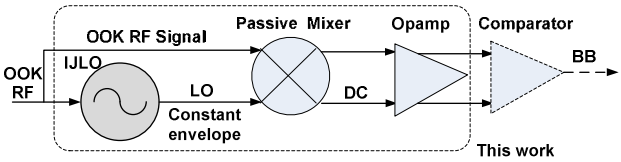

Fig. 1 A self-demodulator.

In this work, a low-power and fast self-demodulation scheme is proposed especially for OOK demodulation, as shown in Fig. 1. The OOK-modulated RF signal is split into two paths. One is used to trigger an injection-locked oscillator (IJLO) and the other one is sent directly to a passive mixer. If data is "1", a high DC level will appear at the output of the mixer whereas a low DC for data "0". The power consumption is reduced dramatically in this way. Besides, the IJLO exhibits fast settling and low phase noise features too.

The basic theory and design considerations of the IJLO and passive mixer are described in Section II. Measurement results are shown in Section III and conclusions are drawn in Section IV.

II. Design of the Self-Demodulator

The analysis, circuits and layout designs are discussed in this section.

A. Injection-Locked Oscillator

A significant drawback of the self-demodulation scheme is the "square-law", i.e. when multiplying a small RF signal (on the order of several mV's) by itself, the conversion loss is significant. Consequently, an IJLO is used to produce a constant-envelope high-voltage output which is in principle, a replica of the injected signal in frequency and phase noise but with a much higher voltage swing. The output signal of the IJLO is then used as the LO driver for the mixer, as shown in Fig. 2. Since the output voltage of the IJLO is determined by the bias current and almost constant at any injected power level, the "square-law" effect is eliminated in this way. In

978-1-4244-5760-1/10/$26.00 ©2010 IEEE

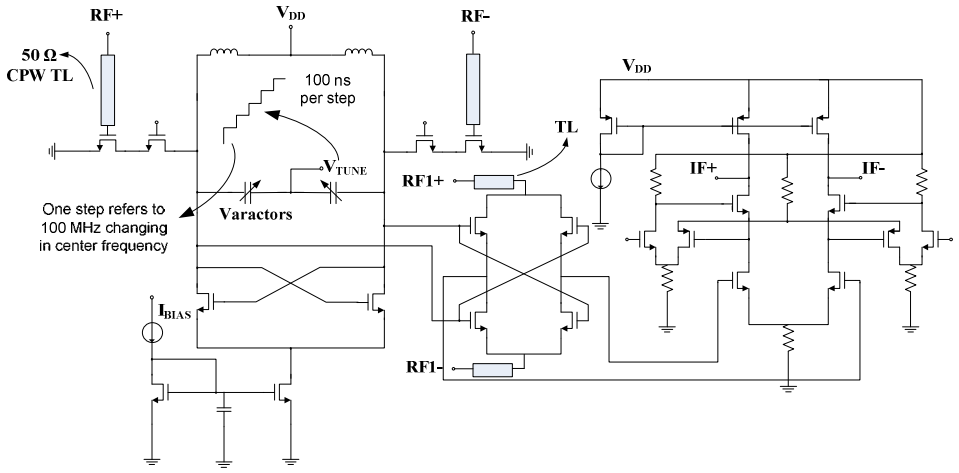

Fig. 2 Schematic of the self-demodulator (bias and controls are not shown).

addition, when the IJLO is locked to the input, the phase noise is reduced too [6].

Comparing to a conventional PLL, the frequency-sweeping IJLO is low-power and fast-settled, because: (1) its complexity is relatively low; (2) it does not require a feedback loop from low-frequency to high-frequency modules and it does not have the frequency pulling phase, so the stabilization time is theoretically shorter; (3) the LC tank can be narrowband with a high Q, so the bias current can be lower, and (4) the total locking range can be extended significantly without requiring high injection power, by using the frequency sweeping method.

The basic idea of the frequency-sweeping method is using an automatic frequency control module to tune the center frequency of the oscillator at a certain step (half of the single-step locking range). When the IJLO locks to the injected signal, the sweeping is stopped. The single-step locking range (double-side) ω_L of an IJLO can be calculated as [6]

$$\omega_L = \frac{\omega_0}{Q} \cdot \frac{I_{inj}}{I_{osc}} \tag{1}$$

where ω_0 is the free-running frequency, Q is the quality factor of the resonator, I_{inj} is the injection current and I_{osc} is the oscillation current. The single-step locking range does not require to be large as long as the total effective locking range is large enough to cover the entire frequency band, e.g. 8 GHz in this work.

Several issues should be taken into consideration. First, the IJLO is loaded with the input of the mixer, which is normally capacitive, so the LC tank of the IJLO should be designed together with the mixer. Second, in order to alleviate the LO leakage and so as the DC offset problem of the mixer, the IJLO should be preferably with a high-voltage instead of high-power output. Furthermore, when the OOK-modulated RF signal is injected, the output of the IJLO should be stable without being pulled away, so long data "0" string should be avoided by proper coding.

In order to reduce the parasitic capacitance, the gate widths of the cross-coupled transistors in the oscillator core are chosen as 2 μm*6 with the minimum length of 60 nm. The size of the MOScap is 400 nm*400 nm, which leads to a varable capacitance ratio (C_{max}/C_{min}) as 3. Adding the fixed capacitance, e.g. from the core and mixer transistors, the ratio is decreased to 2, which leads to a tuning range as 8 GHz for the IJLO.

B. Passive Mixer

A double-balanced passive mixer is chosen, as shown in Fig. 2, because: (1) it is low-power; (2) it has better linearity; (3) it generates low flicker noise. In principle, it only generates the flicker noise when both transistors in the pair are partially on or off under the current induced by the DC offset [8], but this problem is alleviated in this work due to the low-power IJLO scheme; (4) it helps to reduce the LO-RF isolation; (5) since the entire self-demodulator operates in the voltage domain, the power loss of the mixer is not very critical as long as the voltage conversion gain is sufficient and the output voltage is large enough to drive the baseband, e.g. a comparator which typically has a high input impedance at low frequencies.

When the LO voltage swing is large enough, the mixer core operates in the voltage domain and can be modelled as switch pairs. The voltage conversion gain of a double-balanced passive mixer is expressed as [9]

$$G_{c,v} = 20\log\left(\frac{2}{\pi}\left(\frac{Z_L}{Z_L + R_{on}//Z_{off}}\right) - \frac{2}{\pi}\left(\frac{Z_L}{Z_L + Z_{off}}\right)\right) \tag{2}$$

or

$$G_{c,v} = 20\log\left(\frac{2}{\pi}\left(\frac{Z_{off} - R_{on}}{(1+\frac{R_{on}}{Z_L})\cdot(1+\frac{Z_{off}}{Z_L})}\right)\right) \tag{3}$$

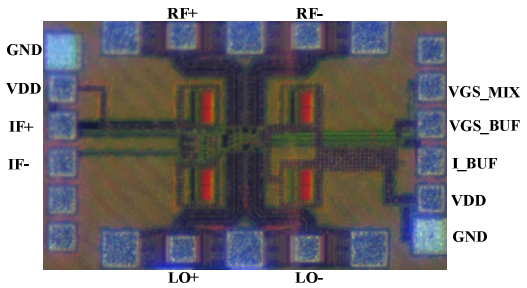

Fig. 3 Chip photo of the passive mixer standalone.

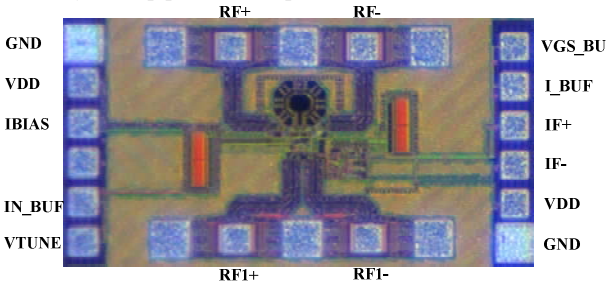

Fig. 4 Chip photo of the self-mixer.

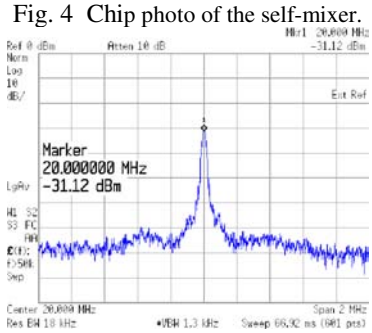

Fig. 5 Output spectrum of the passive mixer

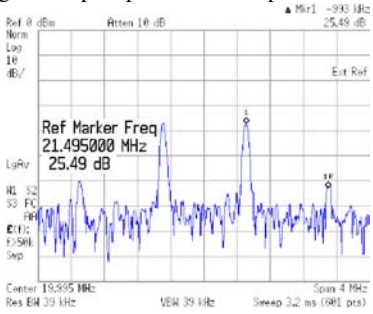

Fig. 6 IP3 test.

where Z_L is the load impedance, R_{on} is the impedance when the switch is on and Z_{off} is the impedance when the switch is off. $R_{on}/|Z_L|$ is assumed <<1 in (3).

From (2) and (3), it can be seen that three methods can be used to improve the $G_{c,v}$: increasing Z_{off}, decreasing R_{on} and increasing Z_L. Increasing Z_{off} means that smaller transistors should be chosen so that the gate-source and gate-drain capacitance is reduced. Besides, the loading capacitance for the IJLO is reduced too. This is very important because the input capacitance of the mixer affects both the IJLO center frequency and the tuning range, and minimum fixed capacitance would provide a maximum tuning range with the same varactors. However, small transistors lead to large R_{on} (the drain-souce on-impedance r_{ds}), which in turn degrades the voltage converion gain. In order to compensate for the degradation of $G_{c,v}$ and keep the small transistor size of the mixer as the optimum load for the IJLO, the output amplifier buffer is added, which offers a large impedance (the gates of small-size transistors) at low frequency.

The transistor size of the mixer core is chosen as 2 μm*2 for low parasitics. The gate-source voltage bias is chosen same as the threshold voltage 0.45 mV so that the switches work in the class B mode and a relatively small voltage swing is able to turn the switch on effectively. The output amplifier uses a folded cascode feedback to enhance the voltage gain. Besides, by tuning the current of the feedback module, the output bandwidth can be controlled. The total current consumption of the amplifier buffer is 1.2 mA and its bandwidth is larger than 1 GHz, which means the data rate of this self-demodulator can be higher than 1 Gbps.

III. Measurement Results

The chip photos of the passive mixer and the self-demodulator are shown in Fig. 3 and Fig. 4 respectively. The chip area of the self-demodulator is bondpad-limited and the effective area is 0.072 mm^2. Coplanar waveguide transmission (CPW) lines are used to connect the circuit core to the GSGSG bondpad with 50-Ohm tapers for measurement purpose. In order to measure the output of the self-demodulator accurately, the inputs of the IJLO and the mixer are separated (in principle they should be one unique input). As shown in Fig. 4, "RF+" and "RF-" are for the IJLO while "RF1+" and "RF1-" are for the mixer. In this way they can have a small frequency difference, e.g. 60 MHz, and the down-conversion result can be read from the spectrum analyzer clearly.

The output spectrum of the standalone passive mixer is shown in Fig. 6. Despite a 2 dB loss and 6 dB mismatch caused by the measurement setups, the output power to a 50-Ohm load is about -23 dBm, and the voltage conversion gain from the 50-Ohm source to the 50-Ohm load is -3 dB at 70 GHz. The DC power consumption of the mixer (the buffer amplifier) is 1.2 mA from a 1-V supply. The IP3 test is shown in Fig. 6 and the IIP3 is -14.75 dBm, which is mainly limited by the buffer amplifier. Since the OOK modulation does not require high linearity and the input level of the demodulator is normally low, e.g. from -60 to -30 dBm, this IIP3 level is quite acceptable.

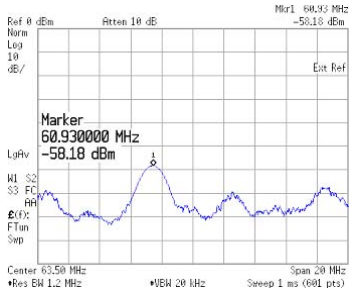

Fig. 7 Output spectrum when the IJLO free-runs (zero input).

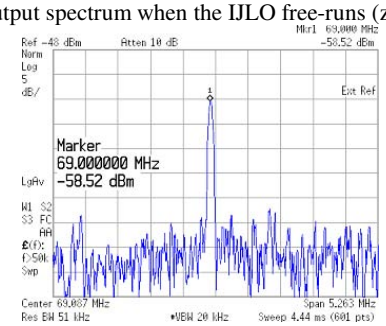

Fig. 8 Output spectrum when the IJLO is locked with -60 dBm input power.

The output spectrums of the self-demodulator with and without locking are shown in Fig. 7 and Fig. 8 respectively. It can be seen that the phase noise of the IJLO is dramatically improved after locking. The total locking range is measured to be from 70.86 to 79.29 GHz. The conversion gain of the self-demodulator is 10 dB with -60 dBm input power (de-embedding 8-dB output loss and I/O mismatch) to the mixer, and it is kept constant over the entire frequency band. The total power consumption is 10.2 mW (9 mW for the IJLO and 1.2 mW for the mixer) from a 1-V supply. Additional 4-mW power is consumed for the input buffer for measurement purpose. The simulated single-step settling time (with OOK modulated data with 10-ps rise time) of the self-demodulator is 140 ps, which is fast enough for the demodulation of the OOK data with 1 Gbps data rate. At the worst case, when the IJLO freely runs at 70.86 GHz and the injected signal is at 79.29 GHz, the simulated total initial settling time is 8.43 μs. The performance is summarized in Table 1.

IV. Conclusions

A 70.86 to 79.29 GHz self-demodulator is realized in TSMC 65 nm CMOS technology. By using the frequency sweeping acquisition method, the total locking range can be extended to 8.43 GHz (the same as the tuning range), and the conversion gain is about 10 dB. The DC power consumption of the core is about 10.2 mW from a 1-V supply. The theoretical maximum energy per bit (calculated by power consumption over the data rate) of the self-demodulator is 10.2 pJ/bit at 1 Gbps data rate.

TABLE I
Performance of the Self-Demodulator

	Measured Data
Technology	65-nm CMOS
Frequency (GHz)	70.86 to 79.29
Power consumption (mW)	10.2
Bandwidth (GHz)	8.43
Conversion gain (dB)	10
IIP3 (dB)	-14.75
Single-step settling time (ps)	140 (simulated)
Worst-case initial settling time (μs)	8.43 (simulated)
LO-RF isolation (dB)	20
Effective Die size (mm2)	0.072
Energy per bit (pJ/bit)	10.2

Acknowledgement

The authors wish to acknowledge the assistance and support of Philips Research Eindhoven.

References

[1] R. E. Amaya and Cornelius J. Verver, "A 60 GHz CMOS Balanced Downconversion Mixer with a Layout Efficient 90° Hybrid Coupler," in *Proc. 2009 IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, 2009.

[2] Burak Catli and Mona M. Hella, "A 60 GHz CMOS Combined mm-wave VCO/Divider with 10-GHz Tuning Range," in *2009 IEEE Custom Integrated Circuits Conference*, San Jose, 2009.

[3] Ali M. Niknejad, Hossein Hashemi, "mm-Wave Silicon Technology 60 GHz and Beyond," *2008 Springer Science and Business Media*, ISBN 978-0-76558-7, pp. 47-49.

[4] Behzad Razavi, "A 60-GHz CMOS Receiver Front-End," in 2006 IEEE Journal of Solid-State Circuits, vol. 41, No. 1, pp. 17-22.

[5] Changhua Cap, Yanping Ding, Kenneth K. O, "A 50-GHz Phase-Locked Loop in 0.13-μm CMOS," IEEE Journal of Solid-State Circuits, vol. 42, NO. 8, 2007, pp. 1649-1656.

[6] Behzad Razavi, "A Study of Injection Locking and Pulling in Oscillators," in *IEEE Journal of Solid-State Circuits*, vol. 39, No. 9, 2004, pp. 1415-1424.

[7] Xia Li, Peter Baltus, Paul van Zeijl, Dusan Milosevic, Arthur van Roermund, "A Low-Power, High-Sensitivity Injection-Locked Oscillator for 60 GHz WPAN Applications," in *Proc. 2009 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics*, Shanghai, 2009.

[8] Sining Zhou and Mau-Chung Frank Chang, "A CMOS Passive Mixer With Low Flicker Noise for Low-Power Direct-Conversion Receiver," in *IEEE Journal of Solid-State Circuits*, vol. 40, No. 5, May 2005, pp. 1084-1093.

[9] Krenar Komoni, Sameer Sonkusale and Geoff Dawe, "Fundamental Performance Limits and Scaling of a CMOS Passive Double-Balanced Mixer," in *IEEE Circuits and Systems and TAISA Conference*, 2008.