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Stability and Passivity of the Super Node Algorithm for EM Modeling of IC's

M.V. Ugryumova and W.H.A. Schilders

Abstract The super node algorithm performs model order reduction based on physical principles. Although the algorithm provides us with compact models, its stability and passivity have not thoroughly been studied yet. The loss of passivity is a serious problem because simulations of the reduced network may encounter artificial behavior which render the simulations useless. In this paper we explain why the algorithm delivers not passive reduced order models and present a way in order to overcome this problem.

1 Introduction

To increase their performance, the characteristic dimensions of interconnection systems are decreased and will decrease even further in the future. Higher speed makes the effect of higher frequency modes on the interconnection more important. Therefore, the analysis of the signal propagation on the interconnect system is important. However, this requires the solution of Maxwell's equations which is rather demanding from the point of view of which can hardly be used in conventional circuit simulators.

To be able to work with models for interconnect structures, a technique known as reduced order modeling is employed (for the various techniques, see [1]). One application where it is used is Fasterix. Fasterix is a layout simulation tool for electromagnetic behavior of interconnect systems such as PCBs, IC packages, filters and passive ICs [2]. As a first step in Fasterix a geometry preprocessor subdivides conductor into quadrilateral elements. In the lumped model derived directly from these elements, referred to here as the *original* (*full*) circuit model, the number of components in the circuit is of the order of the square of the number of elements.

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However, this full circuit model is inefficient, because of computer memory and CPU limitations imply that the interconnect system cannot realistically be simulated. The principle model in Fasterix is a *reduced* circuit model, which is derived from the full model by the *super node algorithm*. Such model runs much faster and has been shown to be equally accurate in frequency domain. The algorithm employs a small subset of the original nodes, so called *super nodes* [2]. The number of supernodes depends on the user-defined maximum frequency, i.e. the highest frequency at which the model has to be valid.

The advantage of the super node algorithm is that it is inspired by physical insight into the models, and produces reduced RLC circuits depending on the maximum predefined frequency. Although the algorithm provides us with compact models, some of them suffer from instabilities which can be observed during time domain simulations. Therefore investigation of stability and passivity properties of the algorithm is primary important.

The paper is build up as follows. In section 2, 3 and 4, we briefly show the concept of the super node algorithm. In section 5 stability and passivity properties applied to the algorithm are discussed whereas in section 6 a technique to preserve passivity of the reduced models is presented. In the last section, a numerical example is considered.

2 Full and reduced order models used in Fasterix

Fasterix translates electromagnetic properties of the interconnect system into a full circuit model which is described by the system of Kirchhoff's equations [3]:

$$(\mathbf{R}+s\mathbf{L})I-\mathbf{P}V=0 \tag{1}$$

$$\mathbf{P}^T I+s\mathbf{C}V=J \tag{2}$$

where $\mathbf{R}\in\mathbb{R}^{\varepsilon\times\varepsilon}$ is the resistance matrix, $\mathbf{L}\in\mathbb{R}^{\varepsilon\times\varepsilon}$ is the inductance matrix, $\mathbf{P}\in\mathbb{R}^{\varepsilon\times\eta}$ is an incidence matrix, $\mathbf{C}\in\mathbb{R}^{\eta\times\eta}$ is the capacitance matrix, $I\in C^{\varepsilon}$ is a vector of currents flowing in the branches, $V\in C^{\eta}$ is a vector of voltages at the nodes. Vector $J\in C^{\eta}$ collects the terminal currents flowing into the interconnection system. Value s is a complex number with negative imaginary part: $s=-j\omega$. Matrices $\mathbf{R}$, $\mathbf{L}$, $\mathbf{C}$ are symmetric and positive definite. Matrices $\mathbf{R}$,$\mathbf{L}$,$\mathbf{C}$,$\mathbf{P}$ are calculated by Fasterix. Example of the circuit with $\eta=3$ and $\varepsilon=2$ is shown in Figure 1. Components R_i, L_i and C_{ij} are corresponding elements of the matrices $\mathbf{R}$, $\mathbf{L}$ and $\mathbf{C}$.

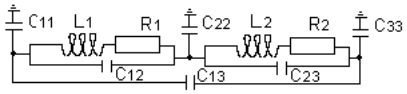

Fig. 1 Example of the original RLC circuit described by (1)-(2)

From (1)-(2) one can obtain the voltage to current transfer with admittance matrix $\mathbf{Y} : \mathbb{C}^{\eta} \to \mathbb{C}^{\eta}$

$$J = \underbrace{\left(\mathbf{P}^T(\mathbf{R}+s\mathbf{L})^{-1}\mathbf{P}+s\mathbf{C}\right)}_{\mathbf{Y}(s)} V. \tag{3}$$

It simply says that if V is given then J can be calculated using $\mathbf{Y}(s)$ for some $s = s_0$. Admittance matrix $\mathbf{Y}(s)$ describes the behavior of the full circuit.

The goal is to obtain a circuit of order η_1 (preferably $\eta_1 \ll \eta$). The ports of the original model are kept in the reduced one. The original and reduced circuits should have approximately the same behavior at these ports.

In order to obtain admittance matrix of the reduced circuit, Fasterix subdivides the set of all nodes in the circuit into two subsets $N \in Z^{\eta_1}$ and $N' \in Z^{\eta_2}$. Evidently $\eta = \eta_1 + \eta_2$. Set N contains super nodes, i.e. nodes which will be retained in the reduced circuit, and N' contains other nodes. Due to this, vectors V, J and matrices $\mathbf{P}$, $\mathbf{C}$ can be partitioned into blocks, see [2], [3] (chapter 8). Block matrix $\mathbf{P}_{N'}$ has full column rank. It is supposed that $J_{N'}$ consists of zeros.

If we consider the voltage in the super nodes as an input V_N, and currents flowing into the system through them as an output J_N, we come to the following system:

$$\left(\underbrace{\begin{pmatrix}\mathbf{R} & -\mathbf{P}_{N'}\\ \mathbf{P}_{N'}^T & \mathbf{0}\end{pmatrix}}_{\mathbf{G}} + s\underbrace{\begin{pmatrix}\mathbf{L} & \mathbf{0}\\ \mathbf{0} & \mathbf{C}_{N'N'}\end{pmatrix}}_{\mathbf{C}}\right) x = \underbrace{\begin{pmatrix}\mathbf{P}_N\\ -s\mathbf{C}_{N'N}\end{pmatrix}}_{\mathbf{B}_i(s)} V_N, \tag{4}$$

$$J_N = \underbrace{\left(\mathbf{P}_N^T \; s\mathbf{C}_{N'N}^T\right)}_{\mathbf{B}_o^T(s)} x + s\mathbf{C}_{NN}V_N, \tag{5}$$

where $x = \left(I\ , V_{N'}\right)^T$. It should be noted that in (4) matrix $\mathbf{G}$ is positive real, and matrix $\mathbf{C}$ is positive semi-definite. From (4)-(5) it follows that J_N is linearly related to V_N, i.e.

$$J_N = \underbrace{\left(\mathbf{B}_o^T(s)(\mathbf{G}+s\mathbf{C})^{-1}\mathbf{B}_i(s) + s\mathbf{C}_{NN}\right)}_{\mathbf{Y}_1(s)} V_N, \tag{6}$$

where $\mathbf{Y}_1(s)$ is admittance matrix of the reduced circuit. Expression (6) can be rewritten in the matrix form: $\mathbf{J}_N = \mathbf{Y}_1(s)\mathbf{V}_N$, where $\mathbf{V}_N = (\,V_N^1 \,\ldots\, V_N^{\eta_1}\,)$ is a matrix of predescribed vectors of voltages and $\mathbf{J}_N = (\,J_N^1 \,\ldots\, J_N^{\eta_1}\,)$ is a matrix of correspondent vectors of current. Further we assume that $\mathbf{V}_N$ is given and equals identity matrix. Therefore $\mathbf{J}_N = \mathbf{Y}_1(s)$.

In order to obtain the concrete RLC circuit described by $\mathbf{Y}_1(s)$, two approximations of $\mathbf{Y}_1(s)$ have to be performed. Derivation of them can be found in [3]. In this paper we will refer to them as $\mathbf{Y}_2(s)$ and $\mathbf{Y}_3(s)$. The last one will be considered in detail.

3 Admittance matrix for the full frequency range

In [3] the second approximation of $\mathbf{Y}_1(s)$ is constructed as

$$\mathbf{Y}_3(s) = \underbrace{\mathbf{P}_N^T \Psi \left(\Psi^T(\mathbf{R}+s\mathbf{L})\Psi\right)^{-1} \Psi^T \mathbf{P}_N}_{\mathbf{Y}_{RL}(s)} + s\mathbf{Y}_C, \tag{7}$$

where Ψ is a null space of $\mathbf{P}_N^T$. Term $\mathbf{Y}_{RL}(s)$ stays for the contribution of resistances and inductances in the circuit. Term $s\mathbf{Y}_C$ comes from the high frequency range approximation and stays for the capacitance contribution [3]. $\mathbf{Y}_{RL}(s)$ can be presented in the pole-residue form as

$$\mathbf{Y}_{RL}(s) = \sum_{i=1}^{n} \frac{\mathbf{H}_i}{(s-\lambda_i)} = \sum_{i=1}^{n} \frac{\left(\Psi^T \mathbf{P}_N x_i\right)\left(y_i^* \mathbf{P}_N^T \Psi\right)}{(s-\lambda_i)},\ n = \varepsilon - \eta_2. \tag{8}$$

where λ_i are the eigenvalues of the matrix pencil $(\Psi^T\mathbf{L}\Psi, -\Psi^T\mathbf{R}\Psi)$. Since $\Psi^T\mathbf{L}\Psi$ and $\Psi^T\mathbf{R}\Psi$ are positive definite then $\lambda_i \in \mathbb{R}$ and $\lambda_i < 0$. y_i, $x_i \in \mathbb{R}^{\eta_1}$ are left and right eigenvectors respectively [4].

4 Realization

In this section we will show how $\mathbf{Y}_3(s)$ in (7) can be translated into RLC circuit. The network described by $\mathbf{Y}_3(s)$ has branches between all nodes and ground and between all nodes. Each branch is calculated as follows [5]. Branch between node i and ground:

$$\mathbf{y}_{3,ii} = \sum_{j=1}^{n} \mathbf{Y}_{3,ij}. \tag{9}$$

Branch between node i and node j:

$$\mathbf{y}_{3,ij} = -\mathbf{Y}_{3,ij}, i \neq j. \tag{10}$$

All elements of $\mathbf{Y}_3(s)$ have the same poles λ_i, and these become the poles for the network branches when calculated by (9) and (10). Each branch in (9) and (10) is given as a rational function $\sum_{i=1}^{n} \frac{c_i}{s-\lambda_i} + se$. Using Foster's canonical form [5], the branch can be represented by an electrical network as shown in Figure 2. C, R_i, L_i are calculated as $C = e$, $R_i = -\lambda_i/c_i$, $L_i = 1/c_i$. Similar to the above, symmetric admittance matrix can be realized exactly by using a Π-structure template [6]. An example of the Π-structure template is shown in Figure 3, where each branch admittance is realized by the Foster's canonical form shown in Figure 2.

However Fasterix does not use straightforwardly this way of realization. Since calculation of all eigenvalues λ_i in (8) may be time consuming process, Fasterix first approximates $\mathbf{y}_3(s)$ with m ($m < n$) terms. It is done as following. The set

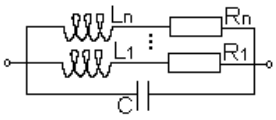

Fig. 2 Synthesization by electrical network

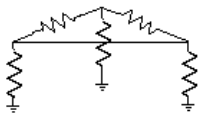

Fig. 3 A tree-port realization of the admittance matrix 3 by 3 based on Π-structure

of $m+1$ match frequencies, s_k, is chosen. This set consists of some large negative values between maximum predefined frequency $-\Omega$ and $-\max(\lambda_i)$, and some small negative values between $-\min(\lambda_i)$ and 0. For each s_k, corresponding admittance matrix has to be calculated. Elements of $\mathbf{Y}_3(s)$ approximate elements of $\mathbf{Y}_2(s)$ in frequency domain well therefore $\mathbf{Y}_2(s_k)$ instead of $\mathbf{Y}_3(s_k)$ can be used.

Solving the following set of $m+1$ equations

$$s_k \mathbf{y}_{C,ij} + \sum_{l=1}^{m} \frac{\widetilde{\mathbf{H}}_{l,ij}}{(s_k - \lambda_l)} = \mathbf{y}_{2,ij}(s_k),\ k = 1,...m+1. \tag{11}$$

for the coefficients $\mathbf{y}_{C,ij}$ and $\widetilde{\mathbf{H}}_{l,ij}$ is equivalent to determine the approximation of $\mathbf{y}_3(s)$ with $m < n$ terms. Like it was shown above, the reduced circuit consists of branches between every pair of circuit nodes. Each branch consists of m parallel connections of a series resistor R and inductor L, in parallel with a capacitor C. Thus for the branch between the circuit nodes i and j

$$R_l = -\lambda_l \widetilde{\mathbf{H}}_{l,ij}^{-1},\ L_l = \widetilde{\mathbf{H}}_{l,ij}^{-1},\ C = \mathbf{y}_{C,ij}. \tag{12}$$

Evidently m influences at the computational time of simulations. Fasterix chooses m depending on the size of the model. Usually $m \leq 8$. For carrying out simulations of the circuit we used PSTAR which is the Philips circuit simulator program.

5 Stability and Passivity

Circuits constructed using rational functions need to satisfy the stability and passivity conditions for a linear time-invariant passive system. The stability condition requires that for a stable system, the output response be bounded for a bounded input excitation [7]. Hence, the rational function representing a stable system has to satisfy the following stability conditions: (1) the poles lie on the left half of the s plane; (2) the rational function does not contain multiple poles along the imaginary axis of the s plain.

The passivity condition requires that a passive circuit does not create energy. Since non-passive models combined with a stable circuit can generate an unstable time-domain response, this condition becomes important when model need to be combined with other circuit for time-domain simulations.

Passivity is closely related to positive realness of the admittance matrix. The admittance matrix $\mathbf{Y}(s)$ is positive real if (1) $\mathbf{Y}(s)$ is analytic for all s with $Re(s) > 0$, (2) $\mathbf{Y}^*(s) = \mathbf{Y}(\bar{s})$ for all $s \in \mathbb{C}$, and (3) $\mathbf{Y}(s) + \mathbf{Y}^*(s) \geq 0$ for all s with $Re(s) > 0$.

Condition (1) means that the system is stable. Condition (2) refers to the system that has real response. And condition (3) is equivalent to that the real part of $\mathbf{Y}(s)$ is a positive semidefinite matrix at all frequencies.

In the super node algorithm, admittance matrix plays a role of a system function. Notice that $\mathbf{Y}_3(s)$ in (7) is stable (all poles $\lambda_i < 0$) but not positive real since $\mathbf{Y}_C$ is an indefinite matrix. However the following theorem holds.

Theorem 1. *Admittance matrix $\mathbf{Y}_{RL}(s)$ in (7) is positive real.*

Proof. In section 3 it was shown that all poles $\lambda_i < 0$ therefore the system is stable. It is trivial to check out the second condition of positive realness. Let $\mathbf{B}^T = \mathbf{P}_N^T \Psi$. We will show that the third one is satisfied:

$$\mathbf{Y}_{RL}^*(s) + \mathbf{Y}_{RL}(s) = \mathbf{B}^T \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^{-*} \mathbf{B} + \mathbf{B}^T \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^{-1} \mathbf{B} = \tag{13}$$

$$= \mathbf{B}^T \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^{-*} \left(\left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right) + \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^*\right) \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^{-1} \mathbf{B} =$$

$$= \mathbf{y}^* \left(\left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right) + \left(\tilde{\mathbf{R}} + s\tilde{\mathbf{L}}\right)^*\right) \mathbf{y},$$

with $\mathbf{y} = (\tilde{\mathbf{R}} + s\tilde{\mathbf{L}})^{-1}\mathbf{B}$. Thus it is sufficient to prove the positive realness for $\mathbf{W}(s) = \tilde{\mathbf{R}} + s\tilde{\mathbf{L}}$. For $s = \sigma + i\omega$ with $\sigma > 0$ we have:

$$\mathbf{W}^*(s) + \mathbf{W}(s) = (\tilde{\mathbf{R}} + s\tilde{\mathbf{L}})^* + \tilde{\mathbf{R}} + s\tilde{\mathbf{L}} = 2\tilde{\mathbf{R}} + 2\sigma\tilde{\mathbf{L}},$$

which is nonnegative definite. Thus, $\mathbf{Y}_{RL}(s)$ is positive real. ■

It is known [6] that a Π-structure template for realization of positive real admittance matrix guarantees construction of the passive circuit. However the important observation is that in the super node algorithm realization by the Π-structure template is applied to the approximation of $\mathbf{Y}_3(s)$ at a few frequency points s_k and not directly to $\mathbf{Y}_3(s)$. So if $\mathbf{Y}_3(s)$ was positive real, the constructed RLC circuit might not be passive. In the next section, a way to obtain positive real $\mathbf{Y}_3(s)$ will be suggested.

6 Passivity enforcement

In this section we present a technique in order to obtain positive real $\mathbf{Y}_3(s)$ which is efficient for the further realization. If both terms in (7) are positive real then $\mathbf{Y}_3(s)$ is positive real as well.

First we consider the term $s\mathbf{Y}_C$. Matrix $\mathbf{Y}_C$ is indefinite. Following the eigendecomposition $\mathbf{Y}_C = \mathbf{V} diag(\sigma_1, \sigma_2, \ldots, \sigma_{\eta_1})\mathbf{V}^{-1}$, all negative eigenvalues are set to zero. Subsequently, the matrix is reconstructed through the operation
$\tilde{\mathbf{Y}}_C = \mathbf{V} diag(\tilde{\sigma_1}, \tilde{\sigma_2}, \ldots, \tilde{\sigma_{\eta_1}})\mathbf{V}^{-1}$ where the modified quantities are denoted with "~". This procedure allows us to get $\mathbf{Y}_C$ positive definite and positive real $s\mathbf{Y}_C$.

Above it was shown that $\mathbf{Y}_{RL}$ is positive real. However the number of terms in $\mathbf{Y}_{RL}(s)$ is related to the number of RL elements in the circuit as $O(n\eta_1^2)$. Taking it into account, we are interested to obtain an efficient approximation of $\mathbf{Y}_{RL}(s)$ which consists of $k < n$ terms and determines the effective admittance function behavior. Positive realness of the new approximation must be preserved. One effective way to achieve it is to use modal approximation [4]. Modal approximation requires selection of dominant eigenvalues and these can be computed via full null space methods (QR, QZ) or iterative subspace methods [4].

A pole λ_j that corresponds to a residue $\mathbf{H}_j$ with relatively large $||\mathbf{H}_j||_2/|Re(\lambda_j)|$ is called a dominant pole, i.e. a pole that is well observable and controllable in the admittance function. In our case all λ_i are real and negative. An approximation of $\mathbf{Y}_{RL}(s)$ that consists of $k < n$ terms with $||\mathbf{H}_j||_2/|Re(\lambda_j)|$ above some value, determines the effective admittance function behavior [4]:

$$\tilde{\mathbf{Y}}_{RL}(s) = \sum_{i=1}^{k} \frac{\mathbf{H}_i}{s - \lambda_i}. \tag{14}$$

Since $\lambda_i < 0$ and $\mathbf{H}_i = (\mathbf{P}_N^T \Psi x_i)(y_i^* \Psi^T \mathbf{P}_N) > 0$, with $x_i = y_i$, then it follows that (14) is positive real. Thus applying a Π-structure template for realization of $\tilde{\mathbf{Y}}_3(s) = \tilde{\mathbf{Y}}_{RL}(s) + s\tilde{\mathbf{Y}}_C$ ensures construction of passive RLC circuit.

7 Numerical example

Fasterix model consists of two printed striplines, which are parallel to each other. The striplines are 1 mm wide and the length is 15 mm. For the maximum frequency 5 GHz , Fasterix generates mesh with 28 elements. Then this model is interpreted as a full RLC circuit with $\eta = 28$ nodes and $\varepsilon = 26$ RL-branches. In order to build reduced circuit, Fasterix chooses 15 super nodes and applies the super node algorithm.

For transient analysis, a trapezoidal pulse having rise/fall times of 1 ps and pulse width of 1 ns is applied to the pins of the lower strip. A 50 Ω resistor R_{out} is connected between two ports of the upper strip. The voltage is measured over R_{out} and regarded as output.

The transient response at the resistor R_{out} is given in Figure 4. It can be seen that the time response is unstable since initially the super node algorithm does not preserve passivity. However, the super node algorithm with proposed passivity enforcement preserves passivity. Shown in Figure 5 the two waveforms of the original and reduced circuits match very well. Table 1 shows a comparison between original and reduced models. The reduced model has large amount of RLC elements. Nevertheless, when the original circuit is of high order, the simulation time is reduced. This happens because the number of mutual inductances is zero. For this particular example $\mathbf{Y}_{RL}(s)$ contains $n = 25$ terms and it was truncated till $k = 4$ terms with the most dominant poles.

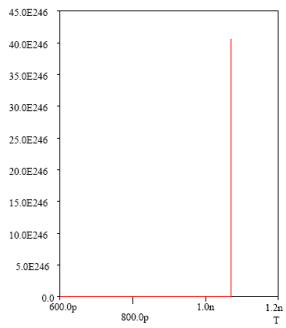

Fig. 4 Simulation in time domain

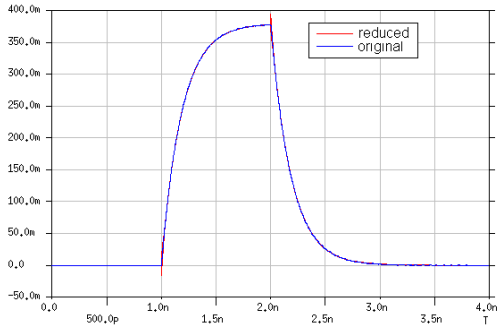

Fig. 5 Comparison of the original and reduced models

Table 1 Comparison of the original and the reduced models

system	dimension	R	L	C	L_{mutual}
original	28	26	26	91	245
reduced	15	420	420	120	0

8 Conclusions

In this paper an overview of a reduction technique, the super node algorithm, used in the EM tool Fasterix has been presented. This algorithm delivers stable models, however we have shown that passivity is not preserved. As a remedy, a technique for passivity enforcement based partly on the modal approximation was introduced. Realization was performed by using a Π-structure template. This strategy solves the problem of preserving passivity. However the time complexity of the modified version of the super node algorithm still needs to be investigated.

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