

Monolithic transformers for high frequency bulk CMOS circuits

Citation for published version (APA): Cheema, H. M., Sakian Dezfuli, P., Janssen, E. J. G., Mahmoudi, R., & Roermund, van, A. H. M. (2009). Monolithic transformers for high frequency bulk CMOS circuits. In W. J. Chappell (Ed.), *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2009 : SiRF '09 ; San Diego, CA, USA, 19 - 21 Jan. 2009* (pp. 1-4). Institute of Electrical and Electronics Engineers. https://doi.org/10.1109/SMIC.2009.4770512

DOI: 10.1109/SMIC.2009.4770512

Document status and date:

Published: 01/01/2009

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.

• The final author version and the galley proof are versions of the publication after peer review.

• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- · Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
 You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Monolithic Transformers for High Frequency Bulk CMOS Circuits

Hammad M. Cheema, Pooyan Sakian, Erwin Janssen, Reza Mahmoudi, Arthur van Roermund

Department of Electrical Engineering, Mixed-signal Microelectronics group, Eindhoven University of Technology, 5600 MB, Eindhoven, The Netherlands

Abstract — This paper presents two monolithic transformer structures exhibiting high self resonance frequencies(f_{SR}). Effect of positive and negative coupling factor on self resonance frequency is investigated. The transformer turn ratio and structure is selected to improve design and ease layout of a high frequency LNA and VCO. Measurement results of a transformer show good agreement with simulated values and demonstrate a coupling factor of 0.7 at 20 GHz.

Index Terms — CMOS integrated circuits, Coupling factor, Monolithic transformer, self resonance frequency.

I. INTRODUCTION

Monolithic transformers have been an intensely researched topic in recent years. Contrary to the traditional use in low frequency circuits, numerous reported applications and implementations of transformers in high frequency circuits have shown their benefits. At these frequencies, small footprint of these transformers fulfills the demand of high level integration and area disadvantage becomes less relevant. For instance, interstage matching and differential to single-ended conversion uptil 100 GHz can be achieved in low noise amplifiers and power amplifiers [1]-[3]. Bandwidth extension can be achieved for amplifiers and frequency dividers [4]. VCO's can utilize transformer coupled tanks and provide quadrature outputs [5]-[6]. Injection locked frequency dividers can use transformer feedback to enhance locking range [7].

However, the design of transformers, with accurate parametric values, for high frequency circuits remains a challenge. For a first-run success of integrated circuit components it is essential to use transformer models based on measured and characterized test-structures. It is important that self resonance frequency of the transformers is higher than their operating frequency in various circuits. Also, accurate inductance values and high-Q transformers are required for VCO resonators. Coupling factor (k) of the transformer determines the mutual inductance between transformer primary and secondary coils and a precise value is critical for circuits requiring phase accuracy, for instance in VCO's or baluns. This paper presents two monolithic transformer structures with high self resonance frequencies having applications in a LNA and a VCO. The transformer used in the LNA is fabricated to compare the measured results with simulations.

II. DESIGN OF TRANSFORMERS

The mutual coupling between primary and secondary part of the transformer can be achieved by interleaving the top-metal layer, stacking one metal layer over the other or a combination of both. The interleaving approach yields a high coupling factor for multi-turn inductors (few nH of inductance), however, when lower inductance (tens of pH) dictates the requirement of a single turn, the resulting coupling factor is reduced. In addition, side-wall capacitance between the adjacent thick top-metal reduces the self resonance frequency of the transformer. On the other hand, taking advantage of the 6-8 metal layers available in the modern CMOS technologies, the stacked approach provides high coupling factors and self resonance frequencies. In addition, the footprint of stacked transformer is smaller as compared to the interleaved structure.

A simple model of a transformer is shown in Fig. 1 which includes the parasitic capacitance and series resistance of the coils. In order to directly characterize the electromagnetic property of the transformer, both the primary and secondary side are modeled by current-controlled current sources (CCCS). C_1 and C_2 is the



Fig. 1. Transformer model including parasitics

$$Z_{in}\Big|_{I_2=0} = \frac{s^3 L_1(1-k^2)L_2(C_2+C_m)+sL_1}{s^2 L_1 C_1(s^2(1-k^2)L_2(C_2+C_m)+1)+s^2 L_2 C_2(s^2(1-k^2)L_1 C_m+1)+s^2(n^2-2kn+1)L_1 C_m+1}$$
(1)

capacitance to substrate, C_{M} is the interwinding capacitance and n is turn ratio of the transformer.

The input impedance (Z_{in}) can be calculated as in eq. 1(assuming the lower terminal of V_1 and V_2 are grounded and ignoring resistances for simplicity). In order to analyze the effect of positive and negative coupling, the limit is taken for $k \rightarrow 1$ and $k \rightarrow -1$ yielding:

$$\lim_{k \to 1} Z_{in} \Big|_{I_2=0} = \frac{1}{s(C_1 + n^2 C_2 + (1 - n^2)C_m) + \frac{1}{sL_1}}$$
$$\lim_{k \to -1} Z_{in} \Big|_{I_2=0} = \frac{1}{s(C_1 + n^2 C_2 + (1 + n^2)C_m) + \frac{1}{sL_1}}$$

$$(1+n^2)C_m > (1-n^2)C_m$$
 (2)

It is clear from (2) that the effective capacitance of the transformer is larger in case of negative coupling and due to the voltage gain increases for high n. Thus, a transformer with negative coupling has a lower resonance frequency as compared to a positively coupled transformer. Fig.2 shows the simulated resonance frequency of a typical transformer for $k = \pm 0.6$. In comparison with positive coupling factor, the f_{srF} is 27% lower for negative coupling.

A. Multi-turn stacked transformer for a LNA

The multi-turn transformer is used for feedback between source and drain of the LNA. In order to boost gain and noise performance, simulations show that the drain inductor should have a high Q-factor in comparison to source inductor. The Q-factor, ofcourse, depends on the selected width and length of these individual coils. Using simulation and subsequent linear fitting the self resonance



Fig. 3. f_{SRF} and Q-factor as a function of metal width

frequency and Q-factor are plotted in Fig.3 as a function of metal width keeping the inductance value fixed. Using this plot the width of the primary and secondary inductors are estimated.

The output isolation requirement (n/k=-Cgs/Cgd) dictates the use of negative coupling for the transformer [8]. The downside of this is the reduced f_{SR} , however, for a LNA design at 20 GHz, a simulated f_{SR} of 50 GHz is sufficient. The terminals of the transformer are on the opposite sides to maintain interconnect symmetry and facilitate measurements.

The expression (n/k=-Cgs/Cgd) also determines the turn ratio of the transformer. Using the capacitance values, a turn ratio of 1.5 is chosen with a coupling factor of 0.7 at 20 GHz. The primary inductor in Me6 has 3 turns and a simulated inductance of 410pH whereas the secondary in Me5 has 2 turns and inductance of 210pH (See Fig.4). The crossover point is made in Me4 with maximum number of vias to reduce series resistance. The simulated Q-factor of primary and secondary inductor is 10 and 9 at 20 GHz, respectively. The area of the transformer is 56 x 56 µm.



Fig. 2. Inductance at the input of transformer for positive and negative coupling



Fig. 4. Transformer structure for LNA

B. Single-turn stacked transformer for a VCO

In a high frequency VCO resonator design, it is crucial to maintain a high Q-factor and, for accuracy of oscillation frequency, minimize the associated parasitics. Keeping this motivation in mind, the transformer for a 60 GHz VCO was implemented as a single turn primary coil in Me6 and a single turn secondary coil in Me5. The top metal in the available technology is 3.4µm thick and yields a high Q-factor owing to lower loss.

The transformer does not have long terminals for connections, rather the horizontal space between the terminals is just kept large enough to fit-in the varactors. This approach greatly helps to ease routing and also decreases the interconnect parasitics considerably. Me1 is placed under the transformer to provide isolation and reduce capacitive coupling to the substrate (see Fig. 5).

The orientation of the primary and secondary coils results in positive coupling yielding a high self resonance frequency of 360 GHz as shown in Fig.6. The simulated inductance for the primary and secondary coils is 66.5pH and 69.8pH with a Q-factor of 16 and 14, respectively at 60 GHz as shown in Fig.7. The coupling factor of 0.8 is calculated using H-parameters. The foot-print of the transformer is very small and occupies $54 \times 52 \mu m$.

III. LAYOUT AND TECHNOLOGY

The simulations of both transformers have been carried out in ADS Momentum using a stack file based on TSMC



Fig. 6. Self-resonance frequency and coupling factor of VCO transformer

65nm bulk CMOS technology. In order to verify the design and simulation results, the transformer for LNA was fabricated. It is connected to the bondpads via 50 Ω coplanar waveguides (CPW) to match with the measurement system. The CPW are kept perfectly symmetrical on both sides as shown in Fig.10. Open and short de-embedding structures are used to de-embed the transformer from the CPW and bondpads. Due to area limitation, a line structure could not be taped-out. The transformer periphery was excluded from automatic dummy filling to avoid performance degradation.

The transformer is fabricated in a TSMC 65nm bulk CMOS process having six metallization layers. The top metal being $3.4\mu m$ thick and about 2 μm away from the substrate is best suited for inductor and transmission line designs. Me5 is $0.9\mu m$ thick and placed exactly under the primary coil.



Fig. 7. Inductance and Q-factor of VCO transformer



Fig. 5. Transformer structure for VCO

IV. MEASUREMENT RESULTS

The LNA transformer was measured on-wafer using high frequency differential probes (GSGSG) and 180° hybrid coupler. An Agilent E8361A PNA network analyzer is used for s-parameter measurements. Cascade Microtech impedance standard substrate (ISS) is utilized for calibration of the PNA. The de-embedding of the bonpads and CPW is done by open and short structures available on wafer. Several die samples of the transformer were measured from 10-40GHz. Due to the missing line de-embedding structure, it was difficult to measure above 30 GHz and the measured results show deviation from the simulated values above this frequency.

The simulated and measured inductance values demonstrate good agreement and are shown in Fig.8. The coupling factor between primary and secondary part of the transformer is shown in Fig.9. At 20GHz, the measured coupling factor of 0.67 is slightly lower than the simulated value of 0.7.

V. CONCLUSION

As enabling components for a high frequency LNA and VCO, two transformer structures exhibiting high self



Fig. 8. Inductance measurement and simulation between 10-40 GHz



Fig. 9. Coupling factor measurement and simulation between 10-40 GHz



Fig. 10. Die micrograph of LNA transformer

resonance frequency and coupling factor are presented. The fabricated test structure demonstrates good agreement between measured and simulated results.

ACKNOWLEDGEMENTS

The authors would like to thank Henry van der Zanden, Bob Theunissen and Paul van Zeijl of Philips research Eindhoven for technology access and tape-out assistance.

REFERENCES

- T.Yao et al., "60-GHz PA and LNA in 90-nm RF-CMOS," *IEEE RFIC Symp. Dig.*, June 2006.
- [2] B. Afshar et al., "A Robust 24mW 60GHz Receiver in 90nm Standard CMOS," *IEEE ISSCC*, pp.182-183 and 605, Feb., 2008.
- [3] C. Weyers et al., "A 22.3dB Voltage Gain 6.1dB NF 60GHz LNA in 65nm CMOS with Differential Output," *IEEE ISSCC*, pp.192-193 & 606, Feb., 2008.
- [4] Hammad M. Cheema et al., "A 40 GHz, Broadband, Highly Linear Amplifier Employing T-coil Bandwidth Extension Technique," *IEEE RFIC Symp. Dig.*, pp. 645-648, June 2008.
- [5] Alan W.L.Ng et al., "A 1-V 17-GHz 5-mW CMOS Quadrature VCO Based on Transformer Coupling," *IEEE JSSCC*, Vol. 42, pp.1933-1941, Sept. 2007.
- [6] E. van der Heijden et al., "Colpits VCOs for low phase noise and low power applications with transformer coupled tank", *IEEE RFIC Symp. Dig.*, pp. 653-656, June 2008.
- [7] Yu-Hang Wong et al., "A 50-to-62 GHz Wide-Locking-Range CMOS Injection Locked Frequency Divider with Transformer Feedback," *IEEE RFIC symp. Dig.*, pp. 435-438, June 2008.
- [8] D.J. Cassan et al., "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS," IEEE JSSCC, Vol. 38, pp. 427-435, March 2003.