Quality-driven SoC architecture synthesis for embedded applications.

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Quality-driven SoC Architecture Synthesis for Embedded Applications

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The recent spectacular progress in modern nanoelectronics created a big stimulus towards development of SoCs for embedded applications. Unfortunately, it also introduced unusual silicon and system complexity and heterogeneity, which result in many serious SoC development issues. Additional difficult to solve issues are due to very high throughput and low energy demands of many modern embedded applications. These issues cannot be resolved without new more adequate system architecture concepts, as well as, methods and EDA-tools for an adequate system-level design exploration and multi-objective optimal system architecture synthesis. This tutorial discusses the problems of multi-objective optimal architecture synthesis and trade-off exploitation for complex hard real-time embedded heterogeneous multi-processor SoCs, and model-based semi-automatic architecture synthesis methods that enable its effective and efficient solution. It thoroughly discusses the abstract models of the architecture design issue that involve the abstract system behavior models, system platform models and multi-objective decision models, as well as, the construction of the models and their usage for the actual system architecture exploration and multi-objective optimal architecture synthesis. In the role of examples, it uses the system architecture exploration and synthesis methods and the corresponding EDA-tools that we recently developed, and the SoC architectures synthesised with our tools for several real-world designs related to the newest highly demanding wireless communication and multimedia standards.

Biography

Dr. Lech Jóźwiak is an Associate Professor, Head of the Section of Digital Circuits and Formal Design Methods, at the Faculty of Electrical Engineering, Eindhoven University of Technology, The Netherlands. He is an author of the methodology of *quality-driven design of electronic systems*, *information-driven approach to digital circuit synthesis*, and theories of *information relationships and measures* and *general decomposition of discrete relations* that have a considerable practical importance. He is also a creator of a number of practical products in the fields of application-specific embedded systems and EDA tools. His research interests include system, circuit, information and design theories and technologies, decision theory, artificial intelligence, embedded systems, SoC design, (re-)configurable and high-performance computing, multi-objective circuit and system optimization, and system analysis and validation. He is an author of more than 150 journal and conference papers, some book chapters, and several tutorials at international conferences and summer schools. He is an Editor of "Microprocessors and Microsystems", "Journal of Systems Architecture" and "International Journal of High Performance Systems Architecture". He is a Director of EUROMICRO; co-founder and Steering Committee Chair of the EUROMICRO Symposium on Digital System Design (DSD); Advisory Committee and Organizing Committee member in the IEEE International Symposium on Quality Electronic Design (ISQED); and program committee member of many other

conferences. He is an advisor and consultant to the industry, Ministry of Economy and Commission of the European Communities. He recently advised the European Commission in relation to Embedded and High-performance Computing Systems for the purpose of the Framework Program 7 preparation. In 2008 he was a recipient of the Honorary Fellow Award of the International Society of Quality Electronic Design for "Outstanding Achievements and Contributions to Quality of Electronic Design". His biography is listed in *"The Roll of Honour of the Polish Science"* of the *Polish State Committee for Scientific Research* and in *Marquis "Who is Who in the World"* and *"Who is Who in Science and Technology"*.