An 1mA Ultra-low Power FHSS TX Front-end Utilizing Direct-modulation with Digital Pre-distortion

A 1 mA Ultra-Low-Power FHSS TX Front-End Utilizing Direct Modulation With Digital Pre-Distortion

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***Abstract*—This paper deals with the system and circuit-level aspects of an ultra-low-power robust wireless node for an asymmetric wireless link. A single building block TX front-end for a frequency hopping spread spectrum (FHSS) transmitter implemented in silicon-on-anything (SOA) bipolar technology is presented. It is realized with a directly modulated RF cascoded Colpitts power voltage-controlled oscillator (VCO), a frequency locked loop for center frequency calibration, and a digital pre-distortion algorithm for accurate frequency bins synthesis. The TX front-end draws only 1 mA at −18 dBm output power. By combining digital system techniques for frequency hopping and merging the VCO and the power amplifier (PA), a robust solution is obtained for indoor ultra-low-power wireless links. The proposed pre-distortion concept allows reduction of the hardware complexity, while the combination of a cascode output buffer and a common-collector Colpitts VCO allows us to reduce the complete FHSS front-end to a single building block that directly drives the antenna through a balun. A dedicated digital algorithm on the receiver side reduces the center frequency offset from a maximum value of 8.2 MHz to less than 8 ppm avoiding the use of any crystal on the transmitter side. Precision in the hopping synthesis is obtained by employing a ST-DFT based demodulator with differential encoding and an offset sending technique. The novel FHSS-predistortion concept has been verified by realizing a full wireless link that achieves a bit error rate better than 1.1% at −25 dBm output power while transmitting across an 8 meters indoor non-line-of-sight (NLOS) path.**

***Index Terms*—Frequency hopping, low-power, pre-distortion, transmitter, wireless sensor networks.**

I. Introduction

MANY wireless applications in the consumer home today, and in the ambient intelligent home of the future, will require only very low data rates (<1 kb/s) and can accept a low quality of service (QoS).

Different scenarios can be foreseen to fulfill the requirements of different applications. Among these scenarios, several applications benefit from an asymmetric network in which the transmitter is required to be cheap, small and ultra-low power, while the receiver will be a residential gateway (RG) or a basestation with a virtually unlimited power budget and relatively higher allowable cost and form factor. In this scenario, while the transmitter will be implemented as a low complexity node, most of the required complexity for a robust link can be shifted to the RG. The RG can communicate with other RGs or a local computer by means of a high data rate wired, as well as wireless, connection.

The portable devices should be able to transmit reliably data under huge power constraints. Unfortunately, the harsh indoor environment presents, due to fading and strong signal attenuation, a great obstacle to reliable wireless communications when the system is power constrained. The use of the overcrowded ISM bands makes this scenario even worse.

Commonly referred to as frequency hopping spread spectrum (FHSS), hopping across multiple frequencies is a proven way to sidestep interferences and overcome RF challenges by using agility rather than brute force (i.e., increasing the transmitted power). Another technique to increase the robustness of the radio link is the direct sequence spread spectrum (DSSS). Nevertheless, this technique is not sufficient in the face of common interferers (like Wi-Fi or Bluetooth) without a significant increase in the processing gain (PG). This makes power consumption higher due to longer synchronization time and increased operating frequency of the baseband circuitry [1].

Though increased communication link robustness can be achieved and a very large network can be handled by employing CDMA techniques, a larger complexity has to be faced at both the physical (PHY) and the media access control (MAC) layers. Indeed, at the PHY layer a more complex frequency synthesizer, while at the MAC layer a more complex synchronization are required. The latter can be solved on the RG side by employing a parallel search algorithm [1] to synchronize the PN codes on the receiver and transmitter sides.

In this paper, a novel FH synthesizer technique is proposed based on digital frequency pre-distortion, which reduces the complexity of the hopping synthesizer. The required communication robustness is achieved on the receiver side using an offset insensitive demodulation algorithm and DSP techniques to overcome nonidealities in the transmitted spectrum.

In this way, a robust 64-channel FSK modulated wireless link to an RG in the 915 MHz ISM band is demonstrated while sinking only 1 mA from a 2 V power supply at −18 dBm transmitted power. This low current consumption is achieved by merging the voltage-controlled oscillator (VCO) and the

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power amplifier (PA) in a single RF block, which is directly coupled to the antenna using a balun and a current buffer. The link showed a raw bit error rate (BER) smaller than 1.1% at −25 dBm transmitted power in a common office environment with TX and RX antennas placed in a non-line-of-sight (NLOS) condition and at 8 meters distance.

The paper is organized as follows. In Section II, the design approach to an ultra-low-power wireless transmitter is presented. Starting from these considerations, a new kind of FHSS synthesizer is introduced in Sections III and IV. Section V presents the experimental results and Section VI gives conclusions.

II. Design Philosophy of Ultra-Low-Power Transmitters

Receiver sensitivity depends on the noise figure (NF), noise bandwidth, and the required signal-to-noise (SNR) ratio of the demodulator. The NF depends on the receiver architecture and technology used and in an asymmetric scenario can be considered to be smaller than 10 dB. For a chosen modulation scheme and a certain desired BER, the required SNR is fixed, apart from implementation losses in the demodulator. The only parameter left is the noise bandwidth which ultimately affects the data rate.

To meet the required ultra-low-power target, the transmitter node has to be duty-cycled; it wakes up, it transmits the required data and it falls back into an ultra-low-power mode called idle mode. Let us consider P_{idle}, the power consumption in the idle mode, P_{tx}, the power radiated from the antenna including the PA efficiency, and P_{diss}, the power used by all the circuitry excluding the PA. Then the average power consumption of the transmitter node can be approximated by

$$P_d = P_{\text{tx}}\frac{T_{\text{tx}}}{T} + P_{\text{diss}}\frac{(T_{\text{tx}}+T_{\text{wu}})}{T} + P_{\text{idle}}\frac{(T-T_{\text{tx}}-T_{\text{wu}})}{T} \tag{1}$$

where T_{tx} is the time required for each transmission, T_{wu} is the wake-up time of the transmitter (i.e., the time required to start up the circuitry and to acquire the synchronization), and T is the time interval between two consecutive transmissions. The duty-cycle of the system, d, can be defined as the ratio between the time required to transmit the data and the time between two consecutive transmissions. This time is the sum of the wake-up time, the transmission time and the time in which the transmitter is in the idle mode. The transmission time depends on the packet length L_{pack} and on the data rate D

$$T_{\text{tx}} = \frac{L_{\text{pack}}}{D}. \tag{2}$$

From these considerations, (1) can be rewritten as

$$P_d = (P_{\text{tx}}+P_{\text{diss}})\times d + P_{\text{idle}}(1-d) + (P_{\text{diss}}-P_{\text{idle}})\times d\frac{T_{\text{wu}}}{T_{\text{tx}}}. \tag{3}$$

The required transmitted power is given by [2]

$$P_{\text{tx}} = N_0 \times \frac{B_{\text{noise}}}{B_{\text{data}}} \times \frac{E_b}{N_0} \times \text{NF}\cdot D\cdot L \tag{4}$$

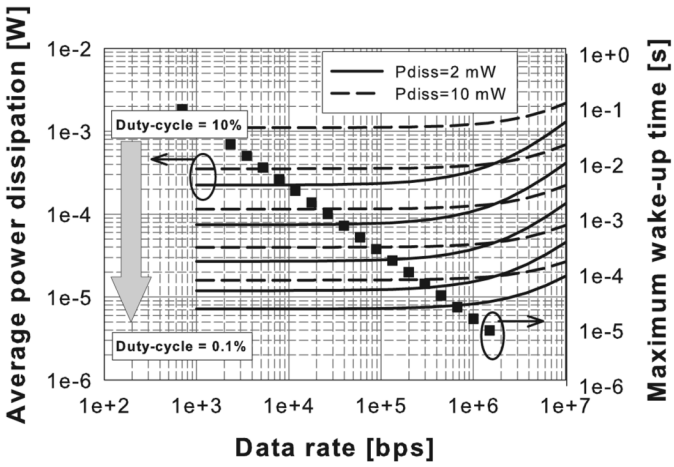


Fig. 1. Average transmitter power consumption as a function of the data rate (Packet length of 1000 bits).

where E_b is the energy per bit of information, N_0 is the additive white Gaussian noise (AWGN) spectral density, B_{noise}[1] is the noise bandwidth, B_{data}[2] is the data bandwidth, and L represents the path losses due to propagation.

From (3), it can be seen that for a fixed transmission distance ($\propto P_{\text{tx}}$), the power consumption can be reduced by reducing the duty-cycle and the data rate, and by making the wake-up time small compared to the transmission time. This last requirement becomes difficult to achieve in an FHSS system at high data rates due to PN code synchronization. Therefore, reducing the data rate will help to relax the wake-up time for a given $(T_{\text{wu}}/T_{\text{tx}})$. The transmitter average power consumption as a function of the data rate for different duty-cycles is plotted in Fig. 1. At high data rates, the average power consumption is dominated by the transmitted power. At data rates below a threshold value the average power consumption is dominated by the pre-PA power. This threshold value depends on the pre-PA power dissipation and it is lower for lower values of the pre-PA power dissipation. From Fig. 1, when the pre-PA power dissipation (P_{diss}) is 2 mW, this threshold value is around 100 kb/s, while at pre-PA power of 10 mW it is located around 1 Mb/s. At higher data rates, the wake-up time has to decrease considerably to keep the contribution to the average power consumption negligible. Though the mains-supplied RG node has a relatively large power budget, synchronization times below 1 ms are not easily achievable. Therefore, from the previous analysis it is possible to conclude that a good strategy toward the reduction in the average transmitter power consumption consists of reducing the data rate and decreasing the synchronization time for a given node duty-cycle.[3]

[1]The 2-FSK noise bandwidth can be approximated by the Carson rule as $B_{\text{noise}} = 2(\Delta f + f_m)$ where $f_m = (2/T_s)$ with T_s the symbol period.

[2]For a 2-FSK modulated signal it equals four times the data rate.

[3]In this analysis, the duty-cycle is fixed. This is the reason why the average power consumption does not increase at very low data rate. The analysis wants to show that given a certain data rate to achieve a certain QoS, then there is no need to increase the instantaneous data rate above this value. This is valid only if a fixed duty-cycle is considered.

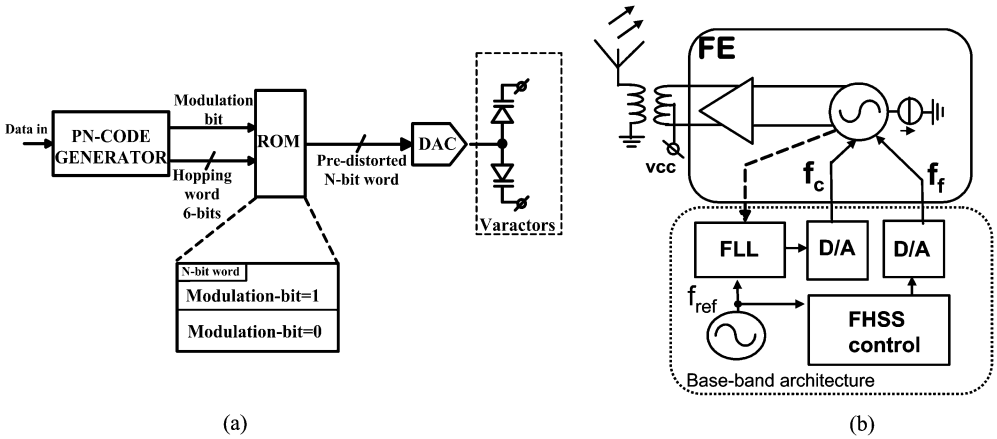


Fig. 2. Frequency pre-distortion-based FH transmitter. (a) Frequency pre-distortion conceptual block diagram. (b) Transmitter architecture.

A. Transmitter Design General Guidelines

To reduce the costs for the user, the transmitter nodes and the RGs will use the ISM bands which are license free. The commonly used ISM bands are the 915 MHz band (available only in the U.S.) and the worldwide-available 2.4 GHz band. In recent years, a large number of new standards made the 2.4 GHz band highly overcrowded both in the number of users and in power levels employed. Furthermore, the presence of continuous interferers like the microwave oven makes this band a very harsh environment for ultra-low-power networks. For this work, the 915 MHz band was chosen. However, the described techniques can be equally well used in the 2.4 GHz band.

The most straightforward modulation scheme employed commonly in FH systems is the frequency shift keying (FSK) modulation. In this work, a robust wideband 2-FSK modulation scheme was employed (modulation index larger than five).

A high level of integration and reduction in the average power consumption can be achieved by employing a simple direct up-conversion scheme. Nevertheless, this architecture suffers from an important drawback: the disturbance coming from the PA output and being injected in the local oscillator (LO). This drawback can be alleviated by shifting the output spectrum far from the LO frequency [3] or by shielding the VCO tank from the antenna by using a current buffer. In this way, the front-end, in a single block, combines both the VCO required for the up-conversion and the PA required to transmit the information through the channel. As a result, both operations are performed by a single RF building block.

Prior to any data transmission, transmitter and receiver should synchronize their center frequencies and PN codes in time. Given the limited power budget on the transmitter side, this process has to be fast and mostly handled by the receiver. Therefore, the transmitter will first calibrate its center frequency in such a way that all the hopping channels lie inside the specified bandwidth (i.e., 915 MHz ISM band). The RG will then align its center frequency to the transmitter center frequency employing a dedicated algorithm [4]. Data transmission will start after synchronization of the PN codes.

III. Transmitter Architecture

Traditional FHSS systems are based on a phase-locked loop (PLL) [5] with a digitally controlled variable divider or on a direct-digital frequency synthesizer (DDFS) [6] and a digital-to-analog converter (DAC) that is used to translate the discrete time periodic waveform from the DDFS in a continuous waveform with specified spectral characteristics. Both these methods require complex hardware.

In this paper, a new architecture is proposed, which requires simple digital techniques and low-complexity, low-frequency analog building blocks, based on frequency pre-distortion. A conceptual block diagram of the proposed architecture is depicted in Fig. 2(a).

The incoming data, together with the desired hopping code, addresses a particular word cell in the ROM. The ROM has been split into two blocks depending on the modulation bit. In each memory cell, the pre-distorted word is stored that will drive the DAC with a defined data bit. The DAC then directly drives the varactor array, changing the capacitance and therefore the VCO oscillation frequency according to the desired frequency bin and data.

The frequency locked loop (FLL) in the baseband [see Fig. 2(b)] measures the VCO signal, and calibrates the output frequency via the coarse tune input f_c of the front-end (FE), to ensure that the complete TX band falls within the ISM band. Making use of a pilot tone generated by the transmitter node and transmitted to the RG, the algorithm can recover an offset of up to 8.2 MHz, with a precision of 7 kHz (<8 ppm at 915 MHz), in less than 300 μs [4]. This corresponds to less than one bit overhead at 1 kb/s and three bits overhead at 10 kb/s.

The FLL and the DAC are realized on a printed circuit board (PCB) and they make use of an ultra-low-power microcontroller for their operation. The DAC consumes only 100 μA during operation. Only one of the DACs will be operational during transmission. Indeed, the DAC and the dividers used for coarse calibration are switched off after the initial self-calibration. Because the coarse calibration is performed only once, it will not contribute to the total power consumption during normal operation. Once this calibration is performed, the FLL and related dividers are also powered down, thus not contributing to the total power dissipation. The fine tune input of the VCO in the front-end, f_f, is directly modulated by the baseband to realize a slow-hopping (1 ms per hop) FHSS transmitter with 64 channels, employing wideband 2-FSK, and able to establish a 1–10 kb/s wireless link with an RG.

The $f_{\rm ref}$ signal is generated by the internal microprocessor oscillator and it is used to lock the transmitter center frequency to the 915 MHz band center frequency within 1% accuracy. This accuracy can be achieved by either factory alignment of the local oscillator or by using a factory calibrated on-chip oscillator of a standard low-power microprocessor. In this work, the second solution was preferred.

A. Frequency Pre-Distortion

The frequency of an *LC* type oscillator and the tank capacitance are related by the following well-known relation:

$$f_{\rm osc} = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

where L and C are the total capacitance and inductance of the tank, respectively, and $f_{\rm osc}$ is the oscillation frequency. This, in practice, is realized by using a varactor diode, which has a capacitance that varies nonlinearly with its reverse voltage. Therefore, by applying the correct voltages to the varactor diodes, it is possible to synthesize all the required frequency bins with minimum hardware complexity (virtually only a VCO).

In an FHSS system, the various frequency bins are addressed in a pseudo-random fashion. Pseudo-random codes are generated in the digital domain, while the varactor diodes require an analog control voltage. Consequently, a DAC is required as interface between the digital world and the analog world. While passing from the digital world to the analog world several nonidealities can affect the precision with which the frequency bins are generated. The main sources of error in this conversion process are the following:

- DAC quantization error (deterministic);
- Varactor nonlinearity (deterministic and stochastic);
- DAC integral nonlinearity (INL) (stochastic);
- Square-root relation between frequency and tank capacitance (deterministic).

All these nonidealities in the transmitter chain can be divided into two groups. One group has a deterministic behavior and it does not vary due to process spread. The square-root nonlinear relation and the DAC quantization error fall into this category. The other group has a stochastic behavior. This means that it will depend on the process spread and therefore a different behavior can be expected for different ICs.

1) Deterministic Errors: The nonlinear relation between frequency and tank capacitance can be easily corrected by mapping the required frequencies in required capacitance values. From these values, knowing the varactor characteristic, a set of required voltages can be mapped and knowing the DAC specifications a set of digital words, which can be stored in a ROM, can be derived.

Therefore, neglecting for the moment the stochastic nature of the DAC linearity and of the *C–V* characteristic of the varactor, the problem can be simplified to the correct choice of DAC resolution to reduce the residual frequency error below a certain threshold.

The quantization error, will produce a nonlinear frequency error passing through the nonlinear *C–V* characteristic of the varactor and through the square-root relation between frequency and tank capacitance.

Looking at the square-root relation, when the overall capacitance is the smallest (at higher frequencies), an error on the capacitance due to quantization, will produce the largest error in the synthesized frequency. In this situation, the reverse voltage applied to the varactor is at its maximum value (for example, −1.6 V). In this region, the varactor exhibits a highly linear behavior, contributing less to the overall frequency error. In these conditions, the frequency error is mainly caused by the quantization error passing through the square-root relation.

Close to the minimum reverse voltage (for example, −0.2 V), the varactor characteristic is highly nonlinear. In this case, the frequency error is mainly caused by the quantization error passing through the varactor nonlinearity, while the square-root relation will minimally contribute to it.

In both cases, a maximum capacitance error can be defined above which a frequency error larger than the required threshold is present at least in one of the synthesized frequency bins. These maximum errors are ($\Delta C_{\sqrt{LC}}$ and $\Delta C_{\rm var}$) defined as follows in the two cases

$$\Delta C_{\sqrt{LC}} = \frac{1}{[(2\pi(f_{\max} + \Delta f)]^2 L} - C_{\min} \tag{6}$$

$$\Delta C_{\rm var} = \frac{1}{[2\pi(f_{\min} - \Delta f)]^2 L} - C_{\max} \tag{7}$$

where $f_{\max}$ is the highest channel center frequency, $f_{\min}$ is the lowest channel center frequency, Δf is the maximum allowed residual frequency error, $C_{\min}$ is the capacitance at the highest channel frequency, $C_{\max}$ is the capacitance at the lowest channel frequency and L is the *LC*-tank inductance value.

The maximum acceptable frequency error after pre-distortion can be derived by the following considerations. PN-codes orthogonality has to be preserved. This means that the relative position of the channels along the frequency grid has to remain unchanged with respect to the ideal case. From this consideration, a maximum frequency error equal to the inter-channel spacing is allowed (for example, 100 kHz). If a 100 kHz maximum channel frequency shift is considered, then there would be the possibility that two channel become adjacent to each other (the inter-channel spacing becomes zero). In this situation, if the specification on the oscillator phase-noise remains unchanged, the amount of noise leaking in the adjacent channels increases degrading the SNR in those channels. In order not to degrade the BER in the adjacent channels considerably, a 0.5 dB maximum degradation on the phase-noise was considered.[4] Under this condition, a maximum uncorrected frequency error of 25 kHz can be tolerated [2].

Considering a 1.4 V swing on the varactor control voltage, an inductance value of 4.1 nH, and 64 channels placed around 915 MHz (ISM band), it can be found from equations (6), (7) that the largest error comes from the quantization error passing through the varactor nonlinear *C–V* characteristic. This is shown in Fig. 3. In this figure, three curves are represented. The two solid lines curves represent the calculated (via (6) and (7)) and

[4]The error probability of a noncoherent BFSK modulated signal is given by $(1/2)e^{-(E_b/2N_0)}$. Considering a 0.1% initial BER, a 0.5 dB degradation in the phase-noise translates into a 0.5 dB degradation in the SNR at the demodulator input and therefore into a BER close to 0.2%.

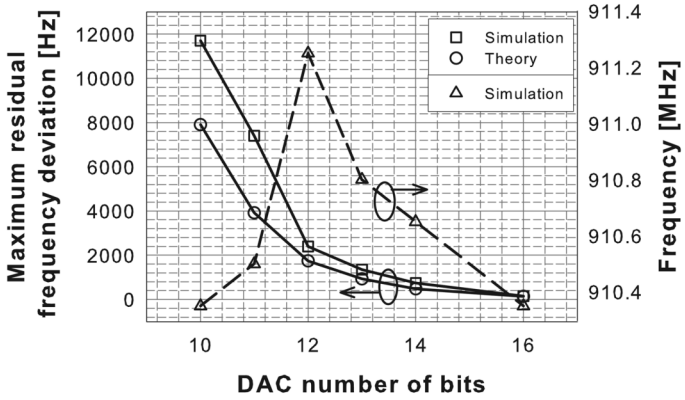


Fig. 3. Maximum uncorrected frequency error and its position in the frequency band versus DAC number of bits.

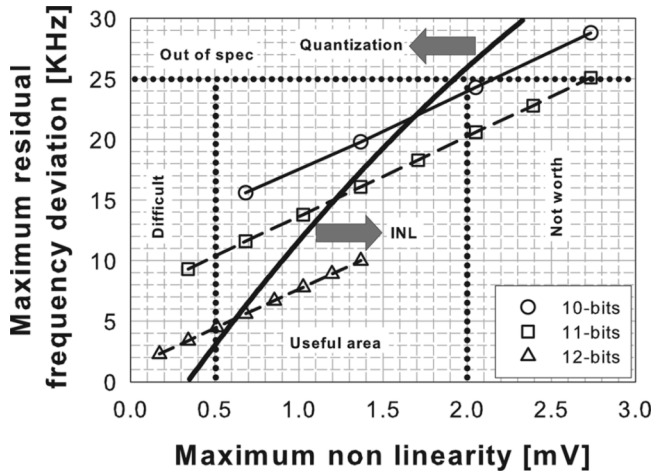


Fig. 4. Effect of DAC INL on the residual frequency error.

simulated maximum residual frequency error after pre-distortion is applied versus the DAC resolution (DAC INL equal to zero). The dotted line curve represents the position in the frequency range at which the aforementioned frequency error occurs. As can be seen, the largest frequency error due to the quantization error occurs at the lower portion of the frequency range.[5]

Given the previous considerations and looking at Fig. 3, in which all the the nonlinearity sources are considered, it can be concluded that the frequency error coming from the DAC quantization error is mainly caused by the nonlinear mapping of this error in the frequency domain via the *C–V* characteristic of the varactor.

Given that the maximum residual frequency error has to be lower than 25 kHz, it can be concluded that a 10 bit DAC is sufficient to achieve the required specification.

2) Stochastic Errors: In the previous analysis, the DAC was considered linear and the spread on the varactor capacitance was neglected. In the real case, they would affect the overall residual frequency error.

Given a certain DAC, its nonlinear behavior can be taken into account by applying a dedicated pre-distortion table. Unfortunately, the INL of each DAC will be different due to its statistical behavior. Therefore, this would require a different programmable look-up table per chip, which can be costly for a system which aims to be very cheap. As a result, it is necessary to fulfill the required specifications on the residual frequency error even when the DAC statistical properties do change.

A DAC model was built in Simulink, which also includes its nonlinear behavior [2]. The results are shown in Fig. 4. Here, both the quantization and the INL of the DAC are considered. Roughly four regions can be recognized. The upper region (*Out of spec*) does not fulfill the maximum residual frequency offset requirement. Then there are two regions called *Difficult* and *Not worth*. The first region presents a difficult task for the designer due to harsh requirements in terms of maximum INL. The second one, while relaxing the INL requirements, necessitates the design of a higher resolution DAC than in the *Useful area*

[5]Given 64 channels and a 150 kHz separation between adjacent channels, the minimum and maximum channel frequencies are 910.35 MHz and 919.65 MHz, respectively.

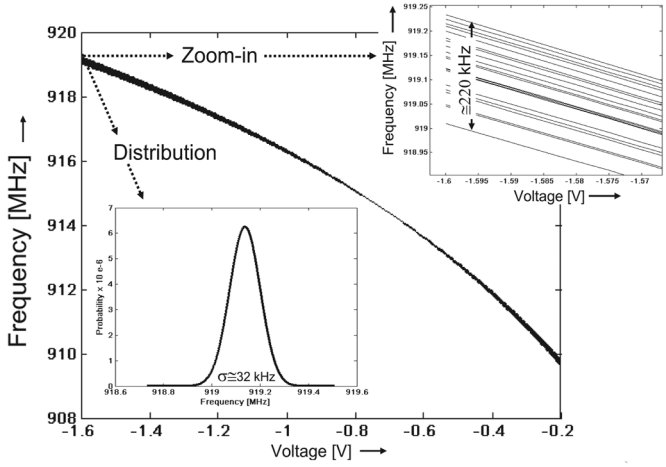


Fig. 5. Measured fine tuning range for 20 IC samples (same DAC).

to fulfill the maximum residual frequency error specification. Designing one more bit of resolution generally requires more area and more power. So the design of the DAC is near optimum inside the *Useful area* in Fig. 4.

Indeed, in this region the INL requirements are not too harsh and the residual frequency error due to the combined effect of both quantization error and DAC INL is smaller than the 25 kHz specification. This region is divided into two by the bold line. This line represents the points at which the contribution of the quantization error and of the INL to the residual maximum frequency error are equal. Therefore, the right part of this area is dominated by the INL error while the left part is dominated by the quantization error. Reducing the number of bits will reduce the chip area and in the end the costs and the power consumption of the DAC. As a result, given the low-frequency operation of the DAC, a lower resolution DAC, which does not require an extremely small INL, can be chosen.

Among different DAC specifications which fulfill the maximum residual frequency error requirement, given the previous considerations and looking at Fig. 4, a 10 bit DAC with an INL between 1 and 1.5 mV can be chosen as a near-optimum solution.

The last source of error is the variation in the *C–V* characteristic of the varactor due to the process spread. As regards the

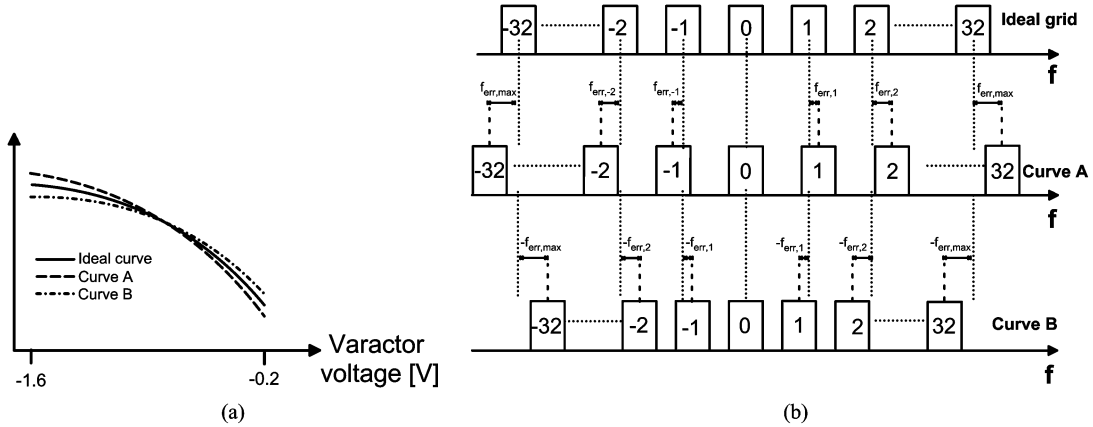


Fig. 6. Effect of the *C–V* varactor characteristic spread on the frequency synthesis. (a) The two extreme cases in Fig. 5. (b) Effect on the channel position in the frequency band.

DAC INL, this problem can be corrected by a dedicated pre-distortion look-up table. Though this is an effective solution, it can be costly.

Fig. 5 shows the measured fine tuning range of 20 IC samples, each calibrated to a common center frequency (915 MHz) via coarse tuning [namely f_c in Fig. 2(b)]. The channel bin tuning voltages are generated by the DAC, driven by the baseband microprocessor. The look-up table in the ROM was not changed and also the DAC is the same, therefore the final effect is only due to the process spread on the varactor. Although the maximum frequency deviation of 20 ICs within the same batch were found to be no more than 220 kHz ($\sigma \approx 32$ kHz), inter-batch spreads would be larger.

In Fig. 6(a), the two extreme cases in Fig. 5 are plotted. The effect of the varactor spread (in the two aforementioned extreme cases) on the position in the band of the frequency bins for a given pre-distortion table is illustrated in Fig. 6. It can be seen that due to the difference in the varactor *C–V* characteristic, there is a frequency offset accumulating while moving from channel 1 to channel 32 or from channel -1 to channel -32. There is a maximum error in channel $+32$ or -32, as can also be seen from the measured curves in Fig. 5. Given the monotonicity of the *C–V* varactor characteristic, the amount of frequency error due to the different *C–V* characteristics between two adjacent channels is negligible compared with the frequency error due to the quantization error. Unfortunately, if the pre-distortion table is kept the same for all the ICs in a batch, this phenomenon will pose a problem on the receiver side. Due to its statistical dependence on the process, the absolute position of the last channel with respect to the ideal position will be known with a precision of ± 110 kHz (see Fig. 5). All the other channel positions will be known with a precision better than that.

Therefore, on the receiver side the channel bandwidth has to be as large as 370 kHz while the inter-channel spacing larger than 185 kHz. This is clearly shown in Fig. 7. Indeed, the absolute position of the channel can spread 110 kHz (at 4 sigma) in both directions. Furthermore, the quantization error plus the INL of the DAC will add 25 kHz more uncertainty, in the worst case, in the channel position. Finally, the two channels should not overlap in the worst case and therefore the center frequency of the adjacent channel has to be at least the bandwidth apart

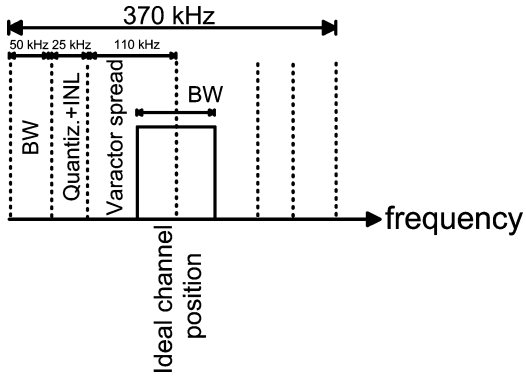


Fig. 7. Minimum inter-channel spacing when varactor spread is considered.

(in this case, 50 kHz). Therefore, the baseband filter has to span two times 185 kHz which makes 370 kHz.

If all the 64 channels are utilized, then the occupied bandwidth will be around 12 MHz. Given that no crystal has to be used, this will pose some stricter requirements on the reference frequency accuracy. Indeed the accuracy has to become better than 0.75% in this case, while in the implemented case it can be relaxed to 1%. On the other hand, FCC rules demand only 25 hopping channels for power levels below 0.25 W (which is generally the case for ultra-low-power wireless nodes). Therefore, another possibility is to still keep the 1% accuracy for the reference frequency but to reduce the number of hopping channels.

B. Data Recovery

FSK modulation is very sensitive to frequency offsets. For example, in a correlator type demodulator the frequency offset has to be much smaller than the data rate for a BER lower than 1%. If a 1 kb/s data rate is chosen, then the residual offset has to be no more than a few hundred hertz. Looking at Figs. 4 and 3, it can be seen that a DAC with more than 14 bits is needed for a reasonable INL requirement.

Furthermore, a technological solution or calibration circuitry would be needed on the transmitter side in order to correct for the statistical variation of the *C–V* varactor curve. Therefore, the choice of the demodulator on the receiver side is crucial in order to reduce the complexity on the transmitter side.

In [7], several demodulator topologies were studied, with respect to their performances, in the presence of static frequency errors (these errors are caused by the statistical properties of the DAC and of the varactor and therefore are time invariant in first approximation). The short-time DFT (ST-DFT) algorithm, through differential encoding, shows a remarkable immunity against static frequency offsets. Furthermore, it can be applied in the digital domain which has the potential to be low power. Indeed, if a zero-IF architecture is employed, due to the small-signal bandwidth, the operating frequency of the ADC will be around 100 ksample/s at the Nyquist rate (signal bandwidth equal to 50 kHz).

As shown in [8], the capability of the ST-DFT algorithm to reject the frequency offset depends upon the condition that the offset is slowly varying. In other words, the frequency offset should vary at a rate smaller than the data rate. Therefore, the offset between two consecutive bits can be considered the same and it will be canceled out when differential encoding is applied. In this way, also the frequency error due to temperature and power supply variations can be tracked and actively canceled out without requiring any additional circuitry.

While differential encoding can cancel out, when applied to two consecutive bits, frequency errors induced by temperature or power supply variations, it cannot cancel the frequency error induced by the statistical properties of the DAC and of the *C–V* varactor characteristic. Indeed, in the particular case of the proposed FHSS system, each bit is sent on a different channel, which is affected by a different offset due to the INL distribution of the DAC as well as the varactor *C–V* characteristic spread.

This means that two different bits will have two different offsets and, therefore, the simple differential encoding cannot cancel it out. Therefore, a straightforward way to cope with such a problem is to again use a dedicated look-up table for each IC. Though this approach guarantees an easy solution to the previous problem, it will increase the cost of the final wireless node due to an increase in testing and calibration costs.

Another solution is to send information about the offset present at that particular hopping frequency when hopping begins. The principle is depicted in Fig. 8. In the figure, the offset is sent as a high logic level, but it can be chosen to be a low logic level as well. Due to the fact that the offset and the data are now sent on the same frequency bin, they are both affected by the same frequency error (due to the statistical properties of the DAC INL and the *C–V* characteristic of the varactor). The differential encoding, therefore, can provide in this case the final cancellation. The drawback of such a solution is an increase in the effective data rate. Given the large modulation index employed ($m > 5$) and the low data rate, there will be no severe drawback on the receiver side. Therefore, this technique was chosen for the proposed implementation.

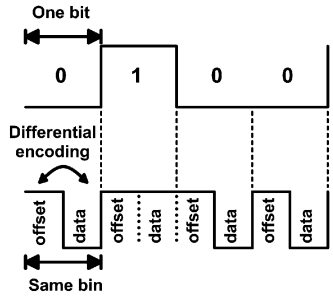


Fig. 8. Residual offset cancellation technique.

IV. Transmitter Design

In modern wireless communication systems, cross-coupled oscillators have been preferred over other topologies for monolithic integrated circuit implementation, because they are easily realized using CMOS technology and differential circuitry. An implementation using this topology has been described in [3] and [9]. It consists of three different RF blocks: *LC* oscillator, frequency divider, and PA, and achieves good performances. Each of these blocks has its own bias current while only part of the current in the PA is finally radiated. Therefore, the pre-PA current consumption is a substantial portion of the overall transmitter current consumption. Furthermore, due to the use of the tail current source, cross-coupled-based oscillators present phase-noise performances worse than classical types of oscillator with one of the active device ports grounded. In the end, this requires a larger DC current for a given phase-noise specification.

To reduce the pre-PA current consumption, the PA and the VCO have been merged in a power-VCO. The PA is a current buffer which has been cascoded with a VCO based on a configuration with one of the ports of the active device grounded. In this case, a Colpitts topology has been chosen arranged in a common-collector configuration. A simplified schematic of the RF front-end is depicted in Fig. 9.

In this way, current consumption is minimized, pulling is reduced due to better isolation between the tank and the load, and no PA is required, but the cascode stage can directly drive the antenna through a balun. Therefore, a single block RF front-end is obtained.

A. Power-VCO Specifications

The phase-noise requirement for the VCO at 450 kHz[6] from the carrier can be derived using the following equation:

$$L_{\Delta f} \leq P_{\mathrm{ws}} - P_{\mathrm{us}} - \mathrm{BW} - \mathrm{SNR} - \mathrm{NF} - 3\ \mathrm{dB} \qquad (8)$$

where P_{ws} is the power of the wanted signal, P_{us} is the power of the unwanted signal, $L_{\Delta f}$ is the phase-noise expressed in dBc/Hz at a certain frequency offset from the carrier, BW is the noise bandwidth, NF is the receiver noise factor, SNR is the required signal-to-noise ratio at the demodulator input, and the 3 dB takes into account the phase-noise contribution of the receiver oscillator (assumed identical to the TX oscillator). Considering a relaxed NF of 15 dB, a BW of 50 kHz (which is enough for a data rate smaller than 5 kb/s using wideband FSK as modulation technique), and a required SNR of 5 dB (which translates to $E_b/N_0 = 11$ dB @ 0.1% BER), the VCO phase-noise at 450 kHz far from the carrier should be lower

[6]Considering that frequency bins are equally spaced by 150 kHz and the most stringent requirement at the third and beyond channel.

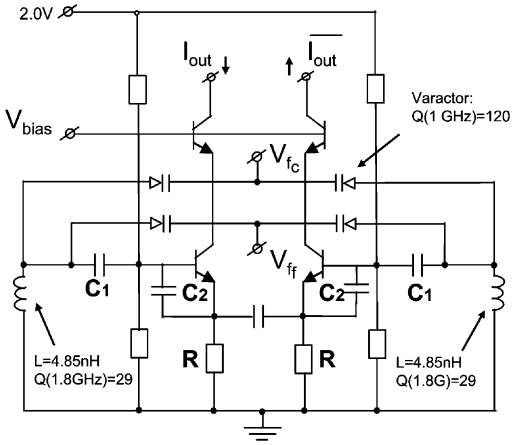


Fig. 9. Circuit schematic of the differential cascoded Colpitts power-VCO.

TABLE I
COLPITTS POWER VCO SPECIFICATIONS

	Value	Unit
Output power	>-25	dBm
Phase noise	<-100	dBc/Hz @ 450 kHz
Coarse tuning range	>40	MHz
Fine tuning range	>7.5	MHz

than -100 dBc/Hz. For the required coarse tuning range, the following equation can be derived:

$$\Delta f = \frac{1}{2\pi\sqrt{L(C_T - \Delta C_T)}} - \frac{1}{2\pi\sqrt{L(C_T + \Delta C_T)}} \tag{9}$$

where L is the inductance value, C_T is equal to the sum of the varactor capacitance, and the series of the feedback capacitances C_1 and C_2 and ΔC_T is equal to

$$\Delta C_T \simeq \frac{C_1^2 \Delta C_2 + C_2^2 \Delta C_1}{(C_1 + C_2)^2} \tag{10}$$

where ΔC_1 and ΔC_2 are the spreads, referred to the nominal value, of the feedback capacitances C_1 and C_2. The spread of the inductance can be considered negligible compared to the process spread of the capacitances. If a $\pm 10\%$ process spread is considered for the capacitances, then the required coarse tuning range should be larger than 40 MHz. Considering a hopping system with at least 50 hopping channels equally spaced by 150 kHz, the required fine tuning range is around 7.5 MHz. The VCO requirements are summarized in Table I.

B. Power-VCO Design Procedure

To reduce the overall power consumption, the phase-noise requirements for the VCO should be met at the minimum bias current. Therefore, for a low-noise oscillator design, a low-noise input stage with a high input impedance is required, and a final stage with a high output power capability and a high output impedance is needed [10].

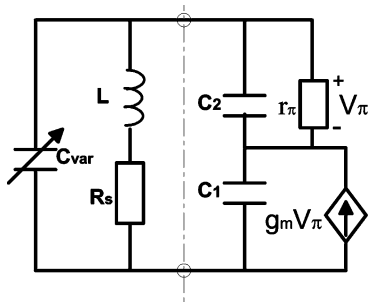


Fig. 10. Common-collector Colpitts small-signal AC equivalent.

The Colpitts oscillator is generally arranged in a common-base or common-collector configuration. Due to its inverting relation between input and output, the common emitter configuration requires an additional inverting stage and therefore it is not easily applicable in a Colpitts configuration. The common-base configuration has a relatively low input impedance, reducing the in-circuit Q of the tank, which is a disadvantage at high frequencies. On the other hand, it shows the highest output impedance for the same output power. To simultaneously have a high input and output impedance, a common-collector configuration with a cascoded buffer stage may be used avoiding any intermediate buffer stage through current reuse.

The AC small-signal model for a single-ended common-collector Colpitts oscillator is shown in Fig. 10. The positive feedback realized by the capacitances C_1 and C_2 produces a negative resistance in series with two capacitances when the β of the transistor is sufficiently large. The necessary condition to have a steady-state oscillation is that the negative resistance lumped element is larger than the total loss of the tank, which means

$$g_m > \omega^2 (C_v + C_{12})(C_1 + C_2) R_s \tag{11}$$

where all the tank losses have been lumped in the resistance R_s, C_{12} is equal to $\frac{C_1 C_2}{C_1 + C_2}$ and C_v is the varactor capacitance. In reality, C_1 also takes into account the parasitic base-emitter capacitance of the transistor.

A relation between bias current and output power at the fundamental frequency can be derived considering that the AC current component at the resonant frequency is the same as in the common-base configuration [11].

$$I_{\omega_0} = 2I_B \frac{I_1(\frac{V_m}{V_T})}{I_0(\frac{V_m}{V_T})} \tag{12}$$

where I_1 is the modified Bessel function of the first kind and order one. The current component at the fundamental will divide itself between the impedance seen looking toward the tank and the impedance constituted by the capacitance C_1 in parallel with the emitter degeneration resistance R.

Calling these two impedances Z_1 and Z_2, respectively, and calling the equivalent impedance between the base and the

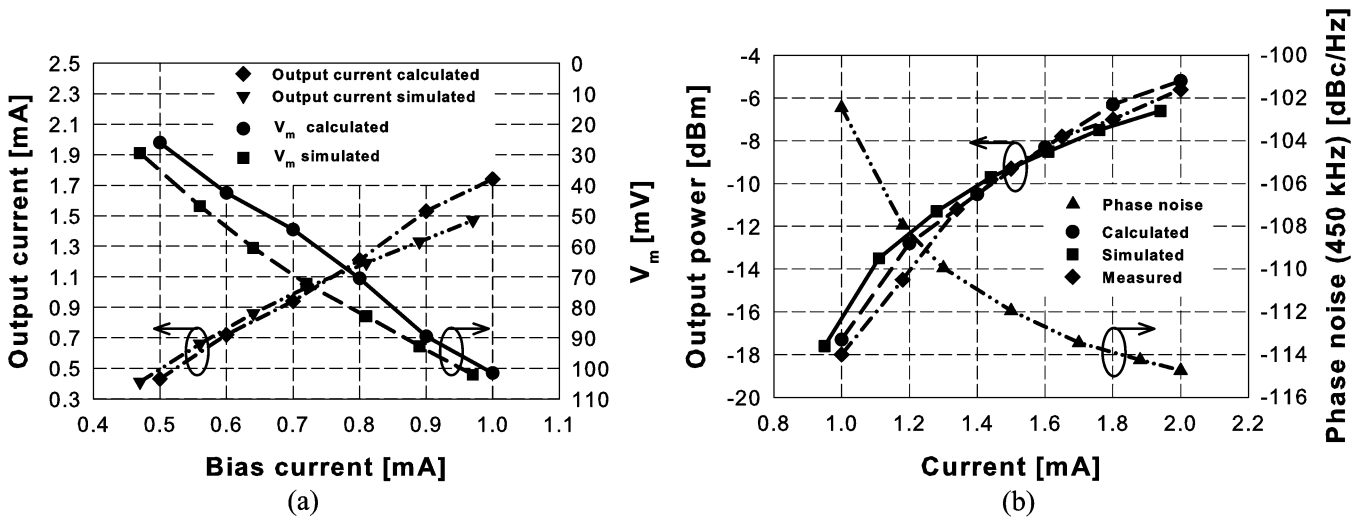


Fig. 11. Predicted, simulated and measured performances for the Colpitts based power-VCO. (a) Output current and V_m amplitude versus bias current I_B for the single-ended Colpitts power-VCO. (b) Output power and phase-noise at 450 kHz offset versus bias current.

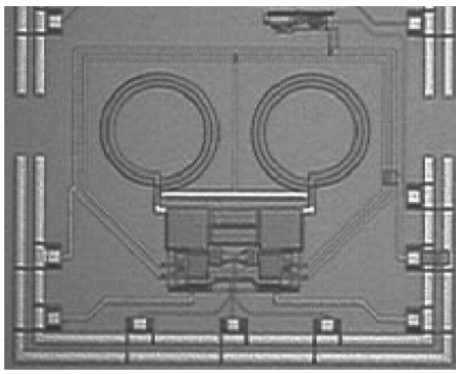


Fig. 12. Micrograph of the differential cascoded Colpitts power-VCO.

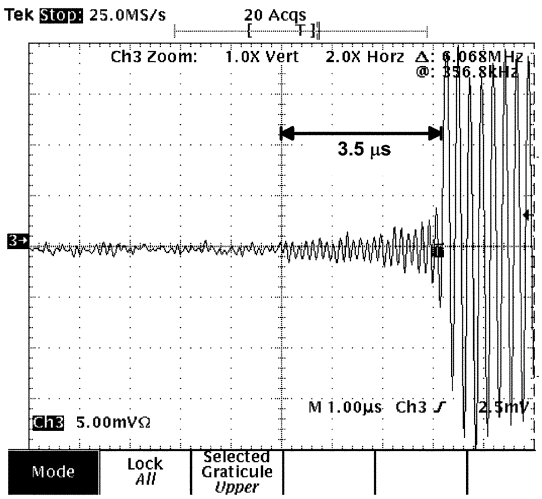


Fig. 13. Oscillator start-up time.

emitter of the bipolar junction transistor (BJT) Z_π, the amplitude of the sinusoidal voltage across the base-emitter junction can be expressed by the following:

$$V_m = 2I_B \frac{I_1\left(\frac{V_m}{V_T}\right)}{I_0\left(\frac{V_m}{V_T}\right)} \left| \frac{Z_1}{Z_2 + Z_1} Z_\pi \right|. \tag{13}$$

Equation (13) should be solved numerically to obtain the value of V_m and therefore the current component at the fundamental frequency. Simulated and predicted results for both the output current and base-emitter signal voltage V_m are represented in Fig. 11(a). As can be seen, the theoretical analysis can accurately predict the required DC current for a certain signal current at the fundamental frequency and therefore for a certain output power.

V. Simulation and Experimental Results

The ultra-low-power transmitter was realized in a bipolar process, which is produced on SOI wafers followed by a substrate transfer to glass [12]. Fig. 12 shows the die photograph of the RF front-end. The active chip area is 3.6 mm^2.

For short-range wireless communication power ranges between -20 dBm and -5 dBm can assure communication over 10 meter distance in the indoor environment. From Fig. 11(b), it can be seen that the required bias current for the power-VCO ranges approximately between 1 and 2 mA to obtain an output power between -18 dBm and -5 dBm. Predicted, simulated, and measured results show a good agreement, allowing minimization of the current consumption for a given set of output power and phase-noise specifications. Indeed, in Fig. 11(b) the phase-noise varies between -102 dBc/Hz and -115 dBc/Hz when the bias current changes between 1 and 2 mA, which is always above the required specification given in Table I. At the lower current consumption (1 mA), the output power on a common 50 Ω antenna is around -18 dBm (excluding cable losses). Given the fact that the system has to be duty-cycled for energy-saving reasons, it is important that VCO start-up time is small compared to the transmission time. In Fig. 13, the measured oscillator start-up time is plotted.[7] The start-up time is

[7]The oscillator frequency in Fig. 13 is an alias of the synthesized frequency due to the sampling rate used in the measurement setup. Indeed, the 25 Ms/s rate is lower than required by the Nyquist theorem.

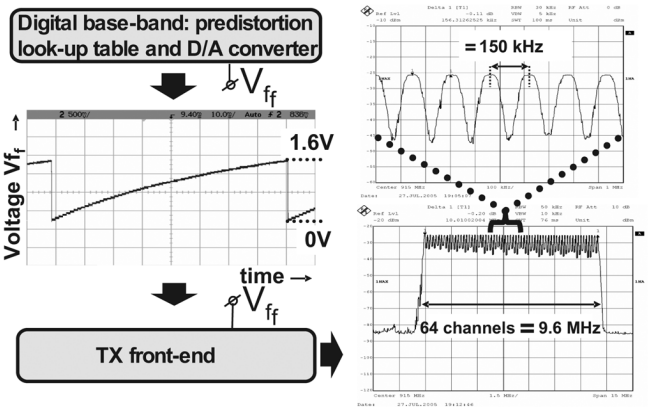


Fig. 14. Pre-distortion chain with measured DAC pre-distorted output voltage and output spectrum of TX front-end.

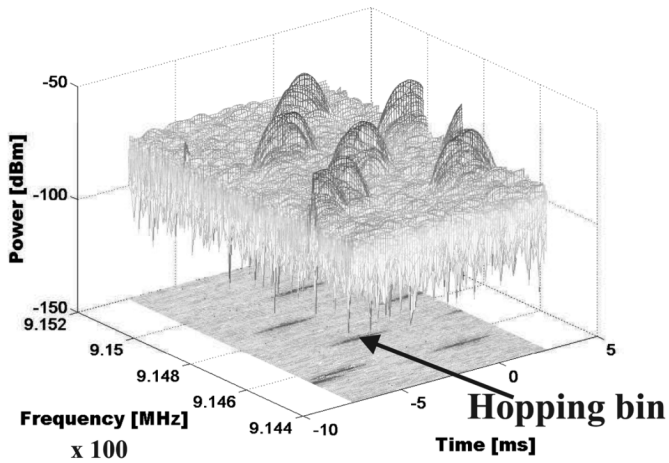
around 3.5 μs. Considering a 10 kb/s data rate, this is a small fraction of the transmission time. Therefore, it negligibly contributes to the average power dissipation of the wireless node.

To demonstrate a reliable wireless link at the specified output power levels and phase-noise specifications and to prove the predistortion concept, a FH transmitter was realized. Two isotropic antennas placed 8 meters apart were used in a non-line-of-sight (NLOS) configuration in a normal office environment.

The receiver is composed by the combination of the NI PXI-5660 down-converter plus a 14 bit, 64 Msample/s digitizer and a demodulation software implemented on a normal PC. The sensitivity of the instrument during reception on a 50 kHz bandwidth is about −88 dBm. In Fig. 14 the whole chain, from the look-up table in the microprocessor up to the evenly spaced FH spectrum is shown. In the measurement results shown in Fig. 14, the 64 channels are addressed sequentially rather than in a pseudo-random fashion. As can be seen, the output of the DAC has a nonlinear shape in time due to the frequency pre-distortion. As can be seen from Fig. 14, an almost linear frequency grid has been obtained with a maximum inter-channel error smaller than 5 kHz.

The transmitted power including cable and board losses is −25 dBm while the receiver employs a ST-DFT demodulation algorithm and a superheterodyne architecture for demodulation with a sensitivity of −88 dBm. In this condition, the measured raw BER is lower than 1.1% at 1 kb/s data rate and 1 khop/s hopping rate. Even though this figure of merit looks high, it has to be considered that no forward error correction (FEC) code has been applied. For the applications of interest, a Reed–Solomon code would be best suited. When this kind of error correction code is applied starting from a 10^{-2} raw BER, it can be proved [13] that a 10^{-6} BER can be achieved both in a fading channel as well as in the presence of a partial band jamming. Looking at a common target application like a temperature sensor, one transmission of a few hundred bits packet every ten minutes gives a good QoS. Now, supposing that the errors during a transmission are uniformly distributed, the packet error rate can be calculated to be 0.03%[8] for a FEC BER of 10^{-6} and a 300 bits packet length.

[8]Supposing the errors in a packet uniformly distributed is a worst case scenario especially for burst based communications. The formula used to derive the packet error rate (PER) starting from the channel BER is in this simplified case $\mathrm{PER} = 1 - (1 - \mathrm{BER})^N$.



(a)

Parameter	FE(1mA)	FE(2mA)	Unit
Technology	SOA		
Active chip area	3.6		mm^2
V_{cc}	2		V
Max. Front-end current (20 samples)	1	2	mA
Max. Front-end dissipation (20 samples)	2	4	mW
Baseband dissipation	0.4		mW
Total active FHSS TX dissipation	2.4	4.4	mW
Min. coarse tuning range (20 samples)	50		MHz
Min. fine tuning range (20 samples)	10		MHz
Worst case phase noise (20 samples)	-102	-115	dBc/Hz @ 450 kHz
Output power	-18	-5	dBm
Raw BER (8 meters distance, P_{out}=-25 dBm)	< 1.1E-2		

(b)

Fig. 15. Received spectrum and RF front-end's performance summary. (a) Received power spectrum (8 meters distance, NLOS condition, and −25 dBm transmitted power). (b) RF front-end's performance summary.

This translates to an error about every 20 days which is good for this application especially if an acknowledge signal is also used to further reduce the PER.

The overall measured transmitter power consumption is 2.4 mW from a 2 V power supply (−18 dBm output power). The baseband and the mixed signal circuitry including the DSP dissipate 0.4 mW mostly consumed in the DACs. If the coarse calibration DAC [see Fig. 2(b)] is switched off after the first initial calibration, the power consumption reduces to about 2.2 mW.

In Fig. 15, the received spectrum before demodulation is shown together with a summary of the performance of the realized front-end. This spectrum has been measured while using the front-end disclosed in this paper. However, it should be noticed that when calibrated to the same output power, the described front-end and the one disclosed by the authors in their previous works [2], [3], [9] give the same output spectrum. Only the absolute position of the frequency peaks will vary due to the process spread on the varactor *C–V* curves (DAC and board are kept the same).

Looking at Table II, the transmitter compares well with other spread-spectrum transmitters. It can be seen that a further reduction in the overall power consumption can be obtained by employing simpler modulation schemes together with dedicated technologies [14], [15] or by matching to high ohmic antennas

TABLE II
COMPARISON WITH STATE-OF-THE-ART WPAN TRANSMITTERS

Ref.	Freq.[MHz]	Process	Architecture	Modulation	Data-rate [kbps]	P_{out}[a] [dBm]	P_{tx}[b] [mW]	V_{supply}[V]	η_{tx}[%][c]
[17]	2400	0.13μm CMOS	One channel	FSK	300-500	-5	1.8	0.4	17.8
[18]	2400	0.18μm CMOS	DSSS	BPSK	200	>0	18	1.8	5.6
[14]	1900	0.13μm CMOS	Two channels	OOK	40	1.6	8.4	1.2	17.2
[16][d]	900	0.25μm CMOS	One channel	FSK	20	-6	1.3	3	19.2
[19]	900	0.18μm CMOS	DSSS	BPSK	40	0	28.8	1.8	3.5
[15][e]	1900	0.13μm CMOS	One channel	OOK	50	0	1.6	0.3	31.5
[20]	2400	0.18μm CMOS	DSSS	BPSK	200	1	42	1.8	3
This work	**900**	**SOA Bipolar**	**FHSS**	**FSK**	**1-10**	**-5**	**4.4**	**2**	**7.4**

[a]Radiated power
[b]Transmitter power
[c]Transmitter efficiency
[d]A 400 Ω antenna is used.
[e]FBAR resonators are used.

[16] and using one- or two-channel communication links [14]–[17]. In this work, a primary goal was the robustness of the wireless link together with the low power consumption but employing standard technological solutions. In this sense, the method compares favorably with all the spread-spectrum-based solutions known by the authors and published in literature but also present on the market in terms of efficiency.

VI. CONCLUSION

The implementation of a "microwatt network," envisioned in the AmI concept, has a unique set of design constraints that focuses attention on a small required bandwidth, a low duty-cycle operation, a short communication range, and challenging requirements in average and peak power dissipation minimization. Nevertheless, a robust wireless link is mandatory. A method to improve the wireless link robustness is to use frequency diversity techniques like frequency hopping.

In this paper, the basic choices in the design of an ultra-low-power wireless node have been highlighted and a new synthesizing technique for an FH asymmetric network has been proposed.

This technique is based on a novel frequency pre-distortion concept, with a complete feed-forward implementation of the frequency synthesizer. Nevertheless, the accuracy in the frequency synthesis is comparable with more complex and more power-hungry implementations of the frequency synthesizer.

Furthermore, by combining the VCO and the PA through the use of a cascode stage, a single block RF front-end has been proposed. Developed equations allow us to simply choose the main oscillator parameters in a common-collector Colpitts VCO to meet the requirements in terms of output power and phase-noise. To demonstrate the feasibility of the novel FH synthesizer and the possibility to reduce the front-end to a single block, an FH transmitter has been realized and a communication link established in a common office environment. Measurement results demonstrated a BER smaller than 1.1% at -25 dBm output power and 8 meters distance between TX and RX in a NLOS condition. The hopping synthesizer draws only 1.2 mA (at -18 dBm output power) from a 2 V power supply or 2.2 mA (at -5 dBm output power).

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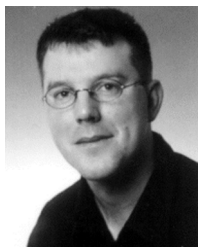

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