# High-accuracy switched-capacitor techniques applied to filter and ADC design 

Citation for published version (APA):
Quinn, P. J. (2006). High-accuracy switched-capacitor techniques applied to filter and ADC design. [Phd Thesis 1 (Research TU/e / Graduation TU/e), Electrical Engineering]. Technische Universiteit Eindhoven. https://doi.org/10.6100/IR611679

## DOI:

10.6100/IR611679

Document status and date:
Published: 01/01/2006

## Document Version:

Accepted manuscript including changes made at the peer-review stage

## Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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# High-Accuracy Switched-Capacitor Techniques Applied To Filter And ADC Design 

Patrick John Quinn

## Cover design:

different capacitor implementations are shown for various SC circuits; background is a SEM image of the cross-section of a high-density metal filament capacitor in 65 nm CMOS.
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# High-Accuracy Switched-Capacitor Techniques Applied To Filter And ADC Design 

## PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de Rector Magnificus, prof.dr.ir. C.J. van Duijn, voor een commissie aangewezen door het College voor

Promoties in het openbaar te verdedigen
op woensdag 13 september 2006 om 16.00 uur
door

## Patrick John Quinn

geboren te Dublin, Ierland

Dit proefschrift is goedgekeurd door de promotor:
prof.dr.ir. A.H.M. van Roermund

Samenstelling promotiecommissie:<br>prof.dr.ir. J.H. Blom (Voorzitter)<br>prof.dr.ir. A.H.M. van Roermund (Promotor)<br>prof. ir. A.J.M. van Tuijl (UT)<br>prof.dr.ir. G.C.M. Meijer (TUD)<br>prof.dr.ir. P.G.M. Baltus<br>prof.dr.ir. J.W.M. Bergmans<br>prof.dr.ir. R.H.J.M. Otten<br>dr.ir. J.A. Hegt

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Quinn, Patrick J.

High-accuracy switched-capacitor techniques applied to filter and ADC design / by Patrick John Quinn. - Eindhoven : Technische Universiteit Eindhoven, 2006.
Proefschrift. - ISBN-10: 90-386-1813-1
ISBN-13: 978-90-386-1813-5
NUR 959
Trefw.: geschakelde capaciteiten / elektronische filters / analoog-digitale conversie / CMOSschakelingen.
Subject headings: switched capacitor filters / analogue-digital conversion / CMOS integrated circuits /mixed analogue-digital integrated circuits.

To Orla, Siobhán, and my parents

## Abstract

In this thesis, innovative techniques are proposed as alternatives to traditional switchedcapacitor (SC) charge-transfer techniques for the more accurate creation of key functions such as required for analogue signal conditioning and data conversion. Active charge transport with the help of an amplifier is replaced by passive (delta) charge redistribution with reduced dependency on capacitor mismatch and with the amplifier used predominantly for buffering. Orthogonal hardware modulation is used in conjunction with N -path filtering, thus achieving very high accuracy, while preventing the problem of pattern noise. A floating-hold buffer is proposed which enables accurate addition of signal voltages without requiring precisely matching and linear components. The new methods have been applied to the design of CMOS SC bandpass filters and algorithmic ADC stages (both cyclic and pipelined). The intrinsic accuracies achieved go beyond those achieved with previous state-of-the-art solutions with a consequent reduction in power for the same speed applications.

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## List Of Symbols And Abbreviations

## Symbols

$A_{0} \quad$ Amplifier DC gain
$B_{x} \quad$ Spectral bandwidth of $x$, where $x$ is RF, IF, or ch (channel)
$C_{f b} \quad$ OTA external feedback capacitance
$C_{i n} \quad$ OTA external input capacitance
$C_{L} \quad$ OTA external load capacitance
$C_{L_{f i x}} \quad$ Permanently connected amplifier external load capacitance including parasitics
$C_{L_{s w}} \quad$ Switching amplifier load capacitance
$C_{\text {Leff }} \quad$ Effective load capacitance the amplifier sees at its output
$C_{o x} \quad$ Gate capacitance per unit gate area
$f_{s} \quad$ Sampling frequency
$f_{\text {sig }} \quad$ Signal frequency
$g_{m} \quad$ The small signal transconductance defined at the bias current
$L \quad$ Effective gate length of MOST
$m \quad$ Discrete time variable
$Q \quad$ Quality factor
QT Charge transfer (SC circuit), where signal charge is transferred completely from one capacitor to the other through the active intervention of an amplifier
$r \quad$ Pole radius in $z$-domain
$s \quad$ Laplace frequency variable
$S \quad$ Scaling factor
$T \quad$ Sampling period
$t_{\text {slew }} \quad$ Slewing time
$V_{R E F} \quad$ Reference voltage
$V_{D D} \quad$ Supply voltage
$V_{o n} \quad$ The MOST "on" voltage, or gate over-drive voltage, defined as $V_{G S}-V_{T}$, required to keep the MOST biased at the edge of saturation with all voltages and currents fixed at their DC bias levels
$V_{d s(s a t)} \quad$ Defined as $V_{g s}-V_{T}$, it is the minimum instantaneous drain -source voltage required

| $V_{\text {margin }}$ | to ensure the MOST stays in saturation <br> Extra voltage safety margin above $V_{o n}$ to ensure MOST stays biased inside strong saturation - generally, $V_{d s(s a t)}<V_{o n}+V_{\text {marg in }}$ |
| :---: | :---: |
| $v_{\text {sat }}$ | Maximum charge carrier velocity in silicon ( $1.1 \times 10^{5} \mathrm{~m} \mathrm{~s}^{-1}$ ) |
| $\underset{W}{V_{T_{p}}}\left(V_{T_{n}}\right)$ | Threshold voltages for PMOSTs(NMOSTs) - note $V_{T_{P}}$ is assumed to be positive Effective gate width of MOST |
| $X_{Y}$ | DC bias value of $x$, with $y$ the descriptor - $x$ is generally a current, $i$, or a voltage, $v$ |
| $x_{y}$ | AC value of $x$ with $y$ a descriptor |
| $X_{y}$ | Total instantaneous value of $x$, where $X_{y}=X_{Y}+x_{y}$ $z$-domain frequency variable |
| $z$ | $z$-domain frequency variable |
| $\beta_{f b}$ | Closed loop amplifier feedback factor |
| $\delta Q$ | Delta charge flow technique referring to a new class of SC circuit |
| $\delta-Q R$ | Delta charge redistribution |
| $\varepsilon_{s}$ | Static settling error resulting mainly from finite amplifier DC gain |
| $\varepsilon_{d}$ | Dynamic settling error resulting mainly from finite amplifier bandwidth |
| $\varepsilon$ | Total combined settling error of a SC circuit at the end of a clock period |
| $\varphi_{x}$ | Defines a clock phase $x$ |
| $\gamma$ | Attenuation factor due to capacitive division from the signal input of a SC circuit to the differential input of the OTA |
| $\kappa$ | Ratio of OTA output parasitic capacitance to its input parasitic capacitance |
| $\mu_{\text {eff }}$ | Effective inversion layer charge carrier mobility, including the effect of vertical field mobility degradation |
| $\mu_{0}$ | Inversion layer charge carrier mobility, when low vertical field (typically, $5 \times 10^{10}$ $\mu \mathrm{m}^{2} \mathrm{~V}^{-1} \mathrm{~s}^{-1}$ ) |
| $\theta$ | Process dependent factor inversely proportional to the oxide thickness (typically, $24 \AA / d_{o x} \mathrm{~V}^{-1}$ ) |
| $\sigma(\Delta \mathrm{X})$ | Standard deviation of $\Delta \mathrm{X}$ |
| $\tau$ | Time constant of linear step response |
| $\omega_{c l}$ | Closed loop bandwidth in radians/s |
| $\omega_{o l}$ | Open loop bandwidth in radians/s |
| $\omega_{T}$ | Radial transition frequency |
| $\omega_{u}$ | Unity gain radial frequency, where the gain of the amplifier is reduced to 1 |
| \\| | In parallel with (used for parallel combinations of resistors or capacitors) |

## Abbreviations

| ADC | Analogue-to-digital converter |
| :--- | :--- |
| ASD | Analogue sampled data |
| ASIC | Application specific integrated circuit |
| ATE | Automatic test equipment |
| BIST | Built-in-self-test |
| BPF | Bandpass filter |
| CAD | Computer aided design |
| CMFB | Common mode feedback |
| CMRR | Common mode rejection ratio |
| DAC | Digital-to-analogue converter |
| DEC | Digital error correction |
| DITO | Dual-input telescopic OTA |
| DNL | Differential non-linearity |
| DS | Double sampling |
| ENOB | Effective number of bits |
| FD | Fully differential |
| FOM | Figure of merit |
| FPGA | Field programmable gate array |
| FS | Full scale (of ADC) |
| GBW | Gain-bandwidth (defined in radians per second) |
| HF | High frequency |
| HPF | Highpass filter |
| IC | Integrated circuit |
| IF | Intermediate frequency |
| IMD | Intermodulation distortion |
| I/O | Input/output interface |
| INL | Integral non-linearity |
| IP | Intellectual property (block) |
| ITRS | International Roadmap for Semiconductors |
| LF | Low frequency |
| LHP | Left half $s$-plane |
| LHS | Left hand side |
| LPF | Lowpass filter |
| LSB | Least significant bit |
| MDAC | Multiplying DAC |
| OOST | MOS transistor |
| MSB | Most significant bit |
| Orthogonal hardware modulation |  |
| Oversampling ratio, f $/ f_{\text {sig }}$ |  |
| OHR |  |


| OTA | Operational transconductance amplifier |
| :--- | :--- |
| PM | Phase margin (in degrees) |
| PSRR | Power supply rejection ratio |
| PVT | Process, voltage supply and temperature variations |
| RF | Radio frequency |
| RGC | Regulated cascode - this term is used interchangeably with the term active feed- <br>  <br> back cascode |
| RHP | Right half $s$-plane |
| RHS | Right hand side |
| RMS | Root mean square |
| S\&H | Sample-and-hold |
| SNR | Signal-to-noise ratio |
| SC | Switched-capacitor |
| SE | Single-ended |
| SEM | Scanning electron microscope |
| SiP | System in package |
| SITO | Single-input telescopic OTA |
| SoC | System-on-a-chip |
| SR | Slew rate |
| SS | Single sampling |
| T\&H | Track-and-hold |
| VHF | Very high frequencies |
| VLSI | Very large scale integration |

## Chapter 1

## Introduction

Silicon technology, and in particular some variant of CMOS, will be around for many years to come [1],[2]. CMOS is the most appropriate technology for implementation of single-chip solutions, not just because of the ease of combination of RF, analogue, and digital circuits on one substrate but because of the extensive range of intellectual property (IP) available. Analogue processing will always be on chip because of the ever present need of a digital-signalprocessor (DSP) to interact with the real analogue world. For example, some $70 \%$ of all microcontroller revenue is generated by microcontrollers containing embedded analogue-to-digital converters (ADC) with a resolution of 8 -bits or more [9]. Indeed, analogue-digital interfaces are rapidly becoming the performance bottle-neck to the advancement of system-on-a-chip (SoC) solutions in leading-edge CMOS processes. Moore's Law has come to mean that the number of transistors on the same size chip doubles every two years [4] (originally every three years[3]). DSP capability has, indeed, increased by two orders of magnitude in the past decade. On the other hand, ADC resolution, for each application frequency range, has increased by only 2 -bits in the same period of time! [5]. Thus, the major analogue IC design challenges are still in the area of analogue-to-digital conversion (ADC) and accompanying analogue signal conditioning circuitry [6]. There continues to be a disparity between what ADCs can deliver and what integrated digital-signal-processing systems demand. According to the latest 2005 ITRS perspective, at the current rate of ADC evolution, it will take another 22 years before present day all digital receivers can be fully integrated [8]!

### 1.1 Cost-Performance Trade-offs in IC Design

The product and/or chip architect needs to adopt appropriate techniques to get the best costperformance trade-off using the latest available combination of user/market data, technology and best design practices. The product is only viable at a certain cost. For that cost, a minimum combination of user features must be integrated which meet a minimum performance specification.

There is a reciprocity at work in the relationship between cost and performance. For this
reason, cost is placed at the nucleus of the diagram of Fig. 6.1, while performance is represented by the outer bands. Three unique bands are identified which define the processes at work in the definition phase of a new chip product. At each level, there are trade-offs that inter-play at that level. The outer band is the user- or, indeed, human-interface ring in which issues such as functionality, product specification, innovation and time-to-market are pre-dominantly in the hands of the people engaged in the design. The middle ring represents the technologies available for implementation of the product definition distilled out of the outer ring. Finally, the inner ring represents the fundamental design space trade-offs (namely power, speed, accuracy and die area [10]) which are required to be combined in some optimal way to ultimately create a chip product to specification which is cost efficient.

A specific example of the cost-performance trade-off is in the area of IC technology. As technology shrinks, overall digital performance improves (but at the cost, for instance, of new process development, increased power density, increased leakage, etc.), while analogue performance deteriorates. CAD tools need to be updated to cope with the extra complexity and demands of each technology generation and transistor and interconnect models need to be updated with the new process parameters before complex VLSI design can be undertaken. Hence, a sweet-spot needs to be found per product per technology generation for the best balance between cost and performance.

### 1.2 Modern IC Design Challenges

There is a major drive to single chip solutions for system implementations of many diverse mixed-signal consumer and telecommunications products. These days, it is neither economical, nor indeed robust design practice, to have critical components, such as analogue-to-digital converters (ADCs), filters and digital-to-analogue converters (DACs) off-chip. The first billion transistor chips are coming on to the mass consumer market. This rapid evolution is being fuelled by the rapid advance of deep sub-micron CMOS technologies through aggressive scaling according to Moore's Law [4], [11].

Continual improvement in overall performance of digital VLSI is the driving factor to continual CMOS technology scaling (with scaling factor $S$ ). The most direct improvements are:

- Lower cost per transistor - with $\sim S$ - (although transistor density increases with $1 / S^{2}$, wafer processing costs also go up by $\sim 1 / S$ per generation);
- More transistors per unit area - with $\sim 1 / S^{2}$;
- Lower power consumption per digital function per unit load - with $\sim S^{2}$ (mainly due to voltage scaling);
- Higher speed - with $\sim 1 / S$ (mainly due to capacitor down-scaling, lower threshold voltages, and lower resistance interconnect).
There are, however, significant limitations to device scaling which are already beginning to impact current CMOS processes ( $90 \mathrm{~nm}, 65 \mathrm{~nm}$ ). The ability to scale down the lithography through ever smarter mask creation techniques is not at issue. The main concern is the fundamental ability of transistors to continue to operate properly with continued scaling [12]. This affects digital and analogue IC design in different ways.


Fig. 6.1 Cost-Performance reciprocity for new generation products.

### 1.2.1 Digital IC Design Challenges

The main challenges in digital IC design come from continued process scaling and these are summarized in the following bullet points:

- One of the major issues for continued digital scaling is soft errors, where the energy stored on a gate is continually scaling to such an extent that extraneous high-energy particles can simply discharge it. Error correction can help alleviate this but at the cost of extra resources and power dissipation.
- Another issue is gate leakage through the inability of a transistor to fully switch off with lowering supply voltages (due to the reducing threshold voltages required to compensate for reduced switching speed with lower supplies), as well as gate leakage caused by the reduction of the thickness of the gate-oxide.
- Power density is increasing with every new technology generation [12]. Increasing transistor densities means that designers can place more functionality on chip every generation. Increased transistor leakage also means that a chip wastes more power in idle mode. Chip area is also increasing per generation due to improved wafer processing. 300 mm wafers are now standard for the latest commercially available 65 nm technology,
so that die sizes of greater than $1 \mathrm{~cm}^{2}$ are now easily manufacturable [11]. Hence, increased chip area, combined with increased power density, means that total SoC power is increasing at the rate of $50-100 \%$ per CMOS generation [13]. While the overall system/board level solution can have a dramatic reduction in power consumption through the continued integration of key functions on chip, the increased power consumption on chip reduces chip reliability.
- Electromigration (EM) deserves a mention, where decreasing metal width causes increasing current density (with $1 / S$ ) which can cause interconnect to break.


### 1.2.2 Analogue IC Design Challenges

The analogue designer must usually make do with a CMOS process crafted for digital performance. Only the second point from the previous section is a main point of concern for integrated analogue circuits when subject to device scaling. While high performance digital circuits require switches to be fast with leakage a secondary (power) concern, analogue circuits must have both fast and low-leakage switches. In analogue circuits, gate and drain leakage currents contribute to static power consumption and leakage from sampling capacitors. This leakage current corrupts sampled signals, degrading analogue performance. The primary concern, though, for analogue IC design, is the scaling of supply voltage that accompanies device scaling [7]. This has a number of detrimental consequences:

- While digital power consumption reduces quadratically with supply voltage, analogue power consumption increases linearly with supply voltage for the same operating precision [section 7.7.2].
- Transistor gain reduces for a given aspect ratio and given $V_{\text {margin }}$. The obtainable gain of the MOS transistor is a factor $\sim S$ per generation smaller than predicted using the squarelaw model [14], [15]. This is primarily due to the lowering of the output resistance from short channel effects, whereas transconductor efficiency $\left(g_{m} / I_{d s}\right)$ doesn't change much. Note that new wafer processing techniques, such as strained silicon, can offset this effect somewhat.
- Dynamic range reduces, on the one hand because of reduced headroom, and on the other hand because of increased noise (greater device thermal and flicker noise - due mainly to smaller physical sizes - and greater digital noise coupling from faster clock rates), as well as increased device non-linearity.
- Although component matching improves due to the more accurate lithography of each technology generation, it does not directly track the accompanying lowering of supply voltage. Hence, mismatch-induced offsets become an increasing fraction of signal levels, causing a reduction in circuit reliability.


### 1.2.3 Test Challenges

Test is becoming an increasingly important constituent, and in many cases a gating item, of the overall cost-performance design space for large scale VLSI SoCs. The cost of test does not directly scale with process technology, die size, nor pin count [7]. The use of traditional exter-
nal test methods on automatic test equipment (ATE) is becoming less feasible for SoC devices, since such SoCs have only a limited number of I/O (input-output interfaces) while more and more IP cores are being co-integrated on the same die.

To help improve testability, Design for Test (DfT) methodologies are becoming an inherent part of the IC design process which require consideration at the outset of product planning [17]. While DfT for digital test is firmly established, DfT for mixed-signal test remains a challenge. One approach is model based testing [18] which relies on reduced performance testing of mixed-signal blocks and then extracting complete test information through making use of established models of the analogue block architectures. Another approach is built-in-self-test (BIST), in which mixed-signal parts of the SoC effectively test themselves and create test histograms which can be read from user-defined test registers by a JTAG bus interface to the ATE. Indeed, the value proposition of BIST is becoming more attractive as the cost of implementing complex hardware solutions on chip gets cheaper. Smart on-chip BIST [P.17] can offer a way forward for testing complex mixed-signal SoCs which can help alleviate the conflicting requirements of shorter test times and increasing test accuracies per mixedsignal function (especially embedded data converters). ASICs require the implementation of dedicated hardware routines for the sake of BIST. On the other hand, programmable general purpose chips, such as DSPs and FPGAs, can make use of their own re-programmable resources to implement very complex test routines for both digital and mixed-signal BIST just for the purposes of speeding up final test.

### 1.2.4 Process and Design Work-Arounds

Experts are no longer declaring that CMOS will soon hit a brick-wall [4] because every time this appears to be the case, both process and chip designers innovate their way past the current set of barriers. Process improvements include low- $k$ dielectric, for reduced interconnect capacitance and increased device efficiency $\left(g_{m} / I_{d s}\right)$, strained silicon, etc. Process work-arounds include self-adaptive silicon with intelligent voltage regulation of moated n-wells and p-wells, as well as power supplies, in order to "centre" the silicon for the device specification (e.g. [P.31]). Design work-arounds include error-correction, self-calibration, smart power-down, sleeper transistors, etc.

The increasing cost of manufactured CMOS devices means that extra process options, such as thick-oxide devices and moat isolation, add relatively little to the overall cost. Such extra options are now standard on all leading-edge CMOS processes. In this way, advanced innovative integrated analogue circuitry can co-exist with the latest deep-submicron digital circuitry on the one substrate (e.g. Xilinx 65 nm mixed-signal SoC, Chapter 10). Not just sensitive analogue circuitry but digital circuitry too benefit from improved performance and reliability. Indeed, most digital ICs need to interface with the real analogue world, which require I/O to work at a voltage much higher than present day digital transistors allow (e.g. 2.5 V I/O but 1 V transistors: V5). Alternative solutions can be implemented in the packaging arena using Sys-tem-in-a-Package ( SiP ) solutions, where a leading edge digital die co-exits with a mixed-signal die from an older technology either on the one package substrate, or as stacked dice. SiP
solutions are still very expensive when compared to dual-oxide, moated leading-edge digital processes.

### 1.3 Switched Capacitors for Analogue Signal Conditioning

Switched capacitor (SC) analogue sampled-data-processing is a proven excellent candidate for implementing critical analogue functions before entering the digital-signal-processing domain in an embedded mixed-signal environment. SC circuits, for embedding in digital VLSI, are attractive for a number of reasons:

- Implementation is fully compatible with modern digital CMOS, requiring just:
- Amplifiers (whose only requirement is to reach end-values between clock transitions, so that non-linearities are tolerable: DC gain and bandwidth are the key parameters see Chapter 4);
- Capacitors (metal interconnect capacitors are sufficient in most cases);
- Clocked switches.
- Accuracies of key parameters depend on a stable clock frequency (primary parameters) as well as capacitor ratios (secondary parameters) and remain accurate with temperature and aging.
- Easy migration to the latest CMOS processes with only limited small signal parameters and matching data necessary.
- Benefit from technology down-scaling by virtue of the linear down-scaling of capacitors, even if a thick-oxide technology option is used alongside the thin-oxide digital.
- No tuning required.
- Re-configurability and re-programmability which can co-function with re-configurable logic.
- Analogue memory and accurate long time-constants.
- Easier functional self-testing, more aligned to digital functional self-test than pure analogue self-test.


### 1.4 Key Points for High Performance SC Design

SC circuits come in many forms but a number of key design points should be followed to ensure that the chosen implementation has low distortion and low power and is area efficient, robust, and sufficiently accurate. This is especially important for high-performance SC bandpass filters and SC based Nyquist-rate ADCs which aim to squeeze the best out of the IC process. The main points to consider are summarized here:

- Parasitic-insensitive configurations should always be chosen.
- Configurations centred around closed loop amplifiers are key to achieving this.
- Avoid transfer dependency on top/bottom plate capacitors, as well as amplifier input and output capacitance.
- No signal-dependent charge-feedthrough or clock-feedthrough on to signal capacitors.
- Balanced differential design and early clocking (e.g. early switching of amplifier input nodes) are key to achieving this.
- Single charge transfer between stage input and output.
- Avoid serial connection of capacitors and/or amplifiers. Use parallelization where possible.
- Circuit configuration should not change with clock phase.
- With no clock phase dependency, the circuit can be optimized to operate in one configuration only.
- Avoid continuous-time paths via the amplifier between SC block input and output.
- For accurate bandpass filters, the sample clock should be used to determine the centre frequency $f_{0}$, whereas a simple capacitor ratio should be used to determine the $Q$.
- The clock is the highest accuracy design parameter in the system, so that it alone should set the most critical specification, i.e. $f_{0}$, The next most accurate design parameter is capacitor matching so that this should be used to determine the next most critical specification, the $Q$.
- Maximize amplifier settling time to full sample clock period through the use of doublesampled or $N$-path techniques.
- Optimize SC circuit configuration such that amplifier feedback factor can be maximized and amplifier loading can be minimized - this ensures power efficiency.
- Create error budget and distribute over all error sources such that no one error dominates - Establish all static and dynamic error sources (see presentation in section 8.2.1).
- Establish critical specifications which must be achieved, e.g. $f_{0}$ accuracy, signal range, linearity, noise, etc.
- Include all interface circuitry in final modelling and simulation, especially reference generation, bias circuitry, clock circuitry, etc.
- Simulations should be done across PVT corners and include full RC extraction with Monte-Carlo analysis.


### 1.5 Scope of thesis

Conventional SC circuit techniques are primarily limited in accuracy by a) capacitor matching and b) the accuracy with which a differential amplifier can squeeze charge from one capacitor to another in a given time frame, usually one sample-clock period. Alternative strategies to such conventional SC approaches that achieve higher accuracy is the main focus of this thesis. The techniques proposed are analogue based and enable the achievement of more accurate system specifications than previously possible. The new techniques are just as amenable to further digital accuracy enhancement via calibration and/or correction as traditional methods. Two application areas are explored in the course of this thesis for exploitation of the proposed techniques, viz. SC filters and algorithmic ADCs - both cyclic and pipelined. Furthermore, efficient system level design procedures are explored in each of these two areas.

### 1.6 Outline of thesis

The main ideas used to achieve high-accuracy in SC design are introduced in Chapter 2. Orthogonal design procedures in SC filter and ADC design are introduced. Proposed delta-charge-flow SC techniques are presented at conceptual level and compared against traditional charge-transfer approaches.

The next two chapters deal with the design of amplifiers for SC applications. Chapter 3 presents SC amplifier design at black-box level and homes in on the specific aspects of amplifier design for SC circuits. Chapter 4 examines amplifier architectures and explores design strategies suitable for SC applications.

Chapters 5 and 6 are dedicated to SC filter design. The concepts of orthogonal hardware modulation and delta-charge-redistribution are exploited in Chapter 5 for the design of lowsensitivity and high-accuracy SC bandpass filters. Reduced sensitivities of centre frequency and quality factor to component mismatch is demonstrated and evaluated for the proposed bandpass filters. The realizations of SC bandpass filters in standard CMOS, making use of the concepts developed in Chapter 5, are presented in Chapter 6. Very high accuracies going beyond previous state-of-the-art proposals are demonstrated for TV and radio applications.

The following four chapters are allocated to ADC design with special emphasis placed on the contributions of the proposed concepts to improved ADC performance. Chapter 7 deals with ADC design at black-box level. Models are presented to aid ADC analysis, while minimum theoretical and practical power limits are derived in terms of conversion accuracy and sample rate. Chapter 8 is devoted to the detailed analysis of algorithmic ADCs, both cyclic and pipelined. The effects of errors on the ADC transfer are demonstrated and error bounds derived. The improved overall performance of a pipelined ADC through the use of hardware scaling and a multi-bit front-end stage is analyzed. A model is proposed to estimate the power per stage and overall power consumption of a pipelined ADC. A new implementation for algorithmic ADCs, both cyclic and pipelined, is proposed in Chapter 9. The realization of the float-ing-hold-buffer is developed and applied to the creation of a new 1.5-bit stage which is the key component of these ADCs. Overall improved performance, including reduced sensitivity to capacitor mismatch, compared to traditional algorithmic ADC design methods is demonstrated. Chapter 10 presents practical realizations of ADC circuits based on the new methodologies. A 12-bit algorithmic ADC requiring no calibration or correction or compensation routines is developed. Included in the ADC system is a versatile track-and-hold based on the floating-hold-buffer, which can handle a number of different types of analogue inputs and transform them into a differential sampled-data signal for further processing by the core ADC. The ADC is embedded in 65 nm CMOS in a complex SoC and proven to be very robust. Two pipelined ADCs with hardware scaling have been designed with two separate specifications, namely high-accuracy, medium-speed and medium-accuracy, high-speed.

Finally, in Chapter 11, general conclusions are drawn based on the work of this thesis.

## Chapter 2

## Key Concepts For Accurate SC Design

Analogous to noise, it is possible to improve matching by increasing the areas of the devices to be matched [16]. In contrast to noise, though, it is possible to achieve accuracy beyond the effective matching of components through either a) trimming, b) calibration, or c) innovative circuit techniques. This final option is explored in this thesis in the area of switched-capacitor (SC) design, where the primary block specification is not allowed to be dependent on simple component matching only (here signal capacitors). Two areas are chosen to demonstrate this, viz. high-accuracy bandpass filter (BPF) design and high-accuracy analogue-to-digital converter (ADC) design. For BPFs, the centre frequency $f_{0}$ is the primary specification, followed by the $Q$-value. For the widely used algorithmic ADCs (i.e. the cyclic and pipelined ADCs), the primary block specification is the accuracy with which the functions $\times 2$ and $\pm V_{r e f}$ can be realized. The accuracy of realization of these key functions determines the accuracy of the whole ADC (see Chapter 8).

The ability to achieve higher functional accuracy beyond the accuracy of component matching alone through improved analogue means (c), has a direct knock-on effect in lower cost and lower power and area compared to (a) and (b) above. Note that digital calibration means is not advocated against here. Instead, it is advocated that analogue innovation needs to be explored first to obtain a reasonable solution before digital calibration needs to be employed. Undoubtedly, digital calibration will play an increased role in improved overall performance but generally speaking, for any given technology, an analogue solution to an analogue problem will outweigh a digital solution to an analogue problem. The analogue solutions should be portable across process generations and not rely on the vagaries of the particular process the circuits are designed in. In this respect, the solutions presented here for SC design are as portable from technology generation to generation as conventional SC techniques.

The main techniques used to achieve high-accuracy in SC BPF and ADC design are explored at conceptual level only in this chapter. This sets the scene for the rest of the thesis.

### 2.1 Orthogonal Design Procedures in Filter and ADC Realizations

Orthogonality in the design process is defined by breaking the system design down into relatively independent sub-designs, or indeed problems to be solved, which when taken together give rise to an optimal overall system solution. Orthogonality in the design flow is exploited in each of the main application areas for high-accuracy SC design, namely filter (Chapter 5) and ADC design (Chapter 9).

In SC filter design, a unique design method, namely orthogonal hardware modulation, can be used in conjunction with $N$-path techniques as a means of preventing pattern noise [P.5]. Basically, the number of paths $N$ is derived independently of the filter order $n$. An optimal choice is motivated by a trade-off between speed/power/area, on the one hand, and the avoidance of in-band artefacts, on the other hand, resulting from practical implementation issues such as path mismatch and clock feedthrough.

In ADC design, a method is devised which, to the first order, avoids transfer imperfections resulting from capacitor mismatch [P.6]. Such imperfections are inherent in contemporary SC ADC approaches in which the core functions of signal multiplication and reference subtraction depend on capacitor ratios and the accuracy with which charge can be actively transferred between capacitors. The method devised in this thesis depends on breaking the ADC function down into simple independent constituent parts, namely simple addition of the input signal (to replace multiplication), as well as the application of reference subtraction through simple level shifting independent of capacitor ratios, or indeed absolute capacitor values [P.10]. The contemporary approach is to use active transport of signal charge between capacitors to achieve the same functionality.

### 2.2 Delta Charge Flow SC Techniques

Delta Charge Flow ( $\delta-Q$ ) SC techniques provide a means for implementing basic analogue functionality using SC techniques more accurate than contemporary charge transfer ( $Q T$ ) SC techniques [19]. Pure $\delta$ - $Q$ SC circuits do not require charge transfer from signal capacitor to signal capacitor via the amplifier virtual earth node. Instead, only a delta charge $\delta Q$ flows in the virtual earth node of the amplifier due to the presence of parasitic capacitors at the amplifier input terminals [P.23]. If no parasitic capacitors were present, the amplifier would behave like an ideal buffer. On the other hand, for $Q T$ type SC circuits, charge is completely transferred from one signal capacitor to another signal capacitor via the virtual earth node of the amplifier. This signal charge transfer $Q$ is combined with the parasitic charge transfer $\delta Q$ present in $\delta$ - $Q$ circuits.

A simple representative example of each type of circuit is depicted in Fig. 2.1. The most basic example of a $Q T$ SC circuit is shown in Fig. 2.1(a) for the implementation of a sample-and-hold (S\&H) stage (with non-overlapping clocks clk1 and clk2 of period $T$ ). At the end of each $c l k 1$ transition, a charge packet of value $Q[m T]=C_{1} \cdot V_{i n}\left[\left(m-\frac{1}{2}\right) T\right]$ is transferred from input capacitor $C_{1}$ to the amplifier feedback capacitor $C_{2}$. An output voltage of $V_{\text {out }}[m T]=\frac{C_{1}}{C_{2}} \cdot V_{\text {in }}\left[\left(m-\frac{1}{2}\right) T\right]$ is developed, which is a sampled and delayed version of the

(a)
(b)

Fig. 2.1 Juxtaposed figures of a $S \& H$ implemented using either
(a) Basic charge-transfer (QT) SC stage;
(b) Basic delta-charge flow $(\delta-Q) S C$ stage.
input signal available for processing by the following SC stage. The circuit block transfer is dependent on the ratio of capacitors $\left(C_{1}, C_{2}\right)$, which are designed to be of nominally equal value for the most accurate transfer of unity gain. The most basic example of a $\delta$ - $Q \mathrm{SC}$ circuit is shown in Fig. 2.1(b) which again implements a $S \& H$ stage. The sampled output voltage $V_{\text {out }}[m T]=V_{\text {in }}\left[\left(m-\frac{1}{2}\right) T\right]$ is developed independently of either the capacitance values or matching of any signal capacitors.
The $\delta-Q$ SC circuits can be defined by the following three key characteristics:

1) When needed (e.g. filter design, section 2.2.2), primary signal charge transport occurs via passive charge redistribution between signal capacitors without the aid of an active element, namely an amplifier;
2) Secondary charge transport $(\delta Q)$ via the amplifier virtual earth node is only to compensate for charge imbalance caused by the presence of unavoidable parasitic capacitors at the signal capacitors top and bottom plates and amplifier input terminals;
3) Amplifier is used primarily to provide a buffered output signal commensurate to the voltage spanning some combination of signal capacitors.
Since $Q T$ SC circuits, by their very nature, contain signal capacitors connected between the amplifier inputs and external low impedance nodes (e.g., amplifier outputs or reference grounds), the amplifier needs to work much harder in the case of $Q T$ circuits compared to their $\delta-Q$ equivalents due to the smaller amplifier feedback factor $\beta_{f b}$. For example, $\beta_{f b}$ for the $Q T$ S\&H of Fig. 2.1(a) is about half that of the $\delta$ - $Q$ equivalent, Fig. 2.1(b). The $Q T$ stage is very flexible, though, in that all the functions of buffering, voltage down-scaling and voltage upscaling can be carried out by one and the same stage, namely Fig. 2.1(a). On the other hand,
the basic $\delta-Q \mathrm{~S} \& \mathrm{H}$ buffer stage needs to be modified considerably in order to implement either voltage down-scaling or up-scaling.

Both $\delta-Q$ and $Q T$ SC techniques use bottom plate sampling ${ }^{1)}$ with early clocking, while all the other usual techniques for incremental accuracy improvement such as charge compensation [20], [21], double-sampling and various low voltage techniques like switched-opamp [22] are just as applicable to $\delta$ - $Q$ type structures as $Q T$ structures. Hence, these adaptations will not be entered into in this thesis, since they are well covered in the literature and give the same incremental accuracy improvements in both cases. Instead, $\delta-Q$ SC techniques are an example of disruptive innovation for accuracy improvement in that they don't rely on the further refinement of existing $(Q T)$ techniques.

Three sub-classes of $\delta$ - $Q$ SC circuit can be identified according to the function they perform, namely the sample-and-hold buffer stage, delta-charge-redistribution stage and $C+C$ stage. Each such sub-class is explained briefly at conceptual level in the following.

### 2.2.1 The Sample-And-Hold Stage: Voltage Buffer

This circuit stage, Fig. 2.1(b), has been presented in the previous paragraph as the most basic example of a $\delta-Q$ SC stage. It is not new and is well explored in the literature [23], [24], and as such won't be discussed further in this thesis. Essentially, on one clock period, capacitor $C$ switches to sample the input signal voltage $V_{i n}$, while on the other clock period, $C$ switches into the feedback loop of the amplifier. The amplifier maintains the voltage on the capacitor despite the presence of parasitic capacitance at each capacitor node and the connection of a

[^0]

Fig. 2.2 Illustration of bottom-plate sampling in part of a SC circuit.
(a)

(b)

(c)


Fig. 2.3 (a) Basic implementations of (a) $\delta$-QR SC stage and (b) C+C SC stage.
(c) Components for accurate implementation.
load capacitor at the amplifier output. The held output voltage neither depends on the ratio of signal capacitors nor indeed on the parasitic nodal capacitors.

### 2.2.2 The Delta-Charge-Redistribution Stage: Voltage Down-Scaler

The delta-charge-redistribution $(\delta-Q R)$ stage provides a means of signal voltage down-scaling through passive charge sharing between signal capacitors connected in parallel [P.23]. Active charge transfer in $Q T$ SC filters is replaced by passive charge redistribution in $\delta$ - QR SC filters. It is demonstrated at conceptual level in Fig. 2.3(a). Signals $V_{1}$ and $V_{2}$ are initially sampled on to capacitors $C_{1}$ and $C_{2}$, respectively. Subsequently, the capacitors are placed in parallel and their charge is combined. The combined signal charge, initially sampled on to each of capacitors $C_{1}$ and $C_{2}$, is subsequently redistributed between $C_{1}$ and $C_{2}$ according to their relative capacitance values. The output voltage is:

$$
\begin{equation*}
V_{\text {out }}=V_{1} \cdot \frac{C_{1}}{C_{1}+C_{2}}+V_{2} \cdot \frac{C_{2}}{C_{1}+C_{2}} . \tag{2.1}
\end{equation*}
$$

Note that $V_{1}$ and $V_{2}$ can be any signals with any delay.
An example of the application of $\delta-Q R$ techniques can be found in SC filter design. For example, a recursive SC filter can be created by replacing $V_{1}$ by $V_{i n}$ and $V_{2}$ by a single clock delayed version of $V_{\text {out }}$. Hence, in the $z$-domain, and assuming one clock transfer delay, (2.1) becomes:

$$
\begin{equation*}
V_{\text {out }}(z)=V_{\text {in }}(z) \cdot z^{-1} \cdot \frac{C_{1}}{C_{1}+C_{2}}+V_{\text {out }}(z) \cdot z^{-1} \cdot \frac{C_{2}}{C_{1}+C_{2}} . \tag{2.2}
\end{equation*}
$$

This reduces to:

$$
\begin{equation*}
\frac{V_{\text {out }}(z)}{V_{\text {in }}(z)}=\frac{C_{1}}{C_{1}+C_{2}} \cdot \frac{z^{-1}}{1-\frac{C_{2}}{C_{1}+C_{2}} \cdot z^{-1}}, \tag{2.3}
\end{equation*}
$$

which is the transfer of a first order lowpass filter. The gain at DC is guaranteed to be unity and is not dependent on capacitor ratios. In fact, a key characteristic of $\delta-Q R$ SC filters, in general, is that the transfer gain is unity at the filter centre frequency (which translates to DC for a lowpass filter).

The main problem with a practical realization of Fig. 2.3(a) is the presence of parasitic capacitance at the top and bottom signal capacitor plates and at the amplifier input terminals. This gives rise to an unpredictable result, since the parasitic capacitor values will appear in the transfer equation of (2.3). So although the $\delta-Q R$ concept is right for filter design, a parasitic insensitive implementation is needed and this forms the subject matter of Chapters 5 and 6.

### 2.2.3 $C+C$ Concept: Voltage Up-Scaler

The $C+C$ stage provides a means for signal addition through the serial combination of signal carrying capacitors [P.6]. It is demonstrated conceptually in Fig. 2.3(b). Again, signals $V_{1}$ and $V_{2}$ are initially sampling on to capacitors $C_{1}$ and $C_{2}$, respectively. These capacitors are then placed in series and a buffer used to read the voltage spanning both capacitors to create a simple addition. If the same signal is sampled on to each of $C_{1}$ and $C_{2}$, then a signal multiplication by two is possible. Via this intuitive illustration of concept, it is already possible to demonstrate how capacitor mismatch has little effect on the signal addition or signal doubling operations of the $C+C$ SC circuit. However, the presence of parasitic nodal capacitors diminishes the practicality of the solution of Fig. 2.3(b). Instead, parasitic insensitive solutions will be developed later in the thesis. An example of the application of the $C+C$ concept is in algorithmic ADC design (cyclic and pipelined) where very high intrinsic accuracy is achievable [P.9].

### 2.3 The Floating-Hold-Buffer

The floating-hold-buffer, [P.6], [P.7], is a fundamental building block which implements the following function:

$$
\begin{equation*}
V_{\text {out }}=V_{\text {in }}+V_{\text {hold } 0} . \tag{2.4}
\end{equation*}
$$





Fig. 2.4 Operating principle of Floating-Hold-Buffer.

Applications requiring such a function, for instance, are high accuracy ADCs and re-configurable track-and-holds of the form proposed in this thesis. Consider the conceptual implementation shown in Fig. 2.4. The hold voltage $V_{\text {hold }}^{0} 0$ is initially sampled on to capacitor $C$ and $C$ is subsequently placed in series with a signal source $V_{i n}$ and buffered to form the output. Unfortunately, due to the presence of the input nodal parasitic capacitance $C_{p a r}$ - see Fig. 2.4 - the circuit delivers the following modified version:

$$
\begin{equation*}
V_{\text {out }}=\left(V_{\text {in }}+V_{\text {hold } 0}\right) \cdot \frac{C}{C+C_{\text {par }}}+V_{\text {out }} \cdot z^{-1} \cdot \frac{C_{\text {par }}}{C+C_{\text {par }}} . \tag{2.5}
\end{equation*}
$$

Effectively, due to the presence of $C_{p a r}$, the floating hold voltage on $C, V_{\text {hold }}$, is modified from the ideal $V_{\text {hold } 0}$ to become:

$$
\begin{equation*}
V_{\text {hold }}=V_{\text {hold } 0} \cdot \frac{C}{C+C_{\text {par }}}+\left(V_{\text {out }} \cdot z^{-1}-V_{\text {in }}\right) \cdot \frac{C_{\text {par }}}{C+C_{p a r}} . \tag{2.6}
\end{equation*}
$$

Clearly, a parasitic insensitive solution is required to enable a high accuracy implementation of the floating-hold-buffer. In Chapters 9 and 10, a method is demonstrated which can achieve this.

### 2.4 Conclusions

The most important themes of orthogonal design procedures in SC filter and ADC design, as well as $\delta$ - $Q$ SC circuit techniques, were explored at conceptual level in this chapter. The $\delta$ - $Q$ SC circuits distinguish themselves from their $Q T$ counterparts in the functional requirements of the amplifier and the reduced reliance on capacitor matching. Basically, $\delta$ - $Q$ SC circuits come down to either placing two capacitors in parallel or series to create either voltage downscaling or voltage up-scaling. The trick is how to do this in order to achieve a high-accuracy result which can operate independently of the presence of parasitic nodal capacitors. This forms the central tenet of the thesis.

Other ideas are developed in the course of the thesis to solve various design problems. Examples are pipelined ADC optimization with multi-bit input stage, amplifiers, comparator, track-and-holds. The SC techniques presented here are fully compatible with CMOS technology and have been proven on CMOS down to 65 nm .

## Chapter 3

## SC Amplifier Design At Black-Box Level

The amplifier is the most important component in a SC circuit. It is crucial at system architecture level to be able to ascertain the amplifier performance requirements. In this respect, a black-box model of the amplifier is useful for distilling out those parameters which affect SC circuit performance without getting caught up in amplifier implementation details. This is why such implementation details are left to the following chapter.

The achievement of a sufficiently high amplifier gain for most SC applications is not a major design challenge, even for low voltage applications. On the other hand, the achievement of an optimized settling performance is a much more complex task. For this reason, the major emphasis in this chapter is on optimizing amplifier settling performance. This chapter considers a more detailed model of amplifier settling than is generally used for SC circuits. In particular, not just the minimization of settling time by the correct balance of capacitive loading and amplifier dimensioning is considered but a model is presented to aid the analysis of non-linear settling effects. The modelling approach presented here is independent of amplifier architecture resulting in tractable expressions for SC amplifier design at black-box level.

### 3.1 Amplifier Design Considerations

The amplifier has two primary tasks in standard SC circuits. Firstly, it enables the active transport of signal charge from one signal capacitor to another without the signal charge leaking to parasitic capacitors. For instance, on clock cycle $\varphi_{2}$ in branch $1\left(\mathrm{br}_{1}\right)$ of the double-sampling SC $Q T$ stage of Fig. 3.1, the signal charge on $C_{i n}$ is transferred to $C_{f b}$ via the virtual earth node of the amplifier. Secondly, it functions as a buffer so that the voltage on a capacitor can be measured without affecting the charge on that capacitor. Again, in Fig. 3.1, the voltage on $C_{f b}$ can be measured by a following SC stage without charge on $C_{f b}$ being lost. Considering the discrete-time nature of SC circuits, the signal at the output of the amplifier is only valid at each clock transition, at which point the following stage reads this signal voltage in. In this respect, the step response of the amplifier is of prime importance. Unlike continuous-time circuits, the step response may be non-linear - the amplifiers may slew or even have overshoot - as long as
the end value is reached within a specified error bound within one clock period [44],[P.4]. This feature alone makes SC circuits very attractive for inclusion with digital VLSI compared to their continuous-time counterparts. An example is shown in Fig. 3.2 of the step response of a SC sample-and-hold (S\&H) circuit.

### 3.2 The Settling Error Model

Limitations in practical amplifier performance affect the accuracy of charge transfer from $C_{\text {in }}$ to $C_{f b}$ on each clock period [26], [27]. Limited DC gain determines how close to zero the virtual earth of a charge transfer SC circuit such as Fig. 3.1 can go. It causes a static error, $\varepsilon_{s}$, which is the relative error in the end-value of the output voltage, $V_{\text {out }}$, at $t=\infty$ compared to when the amplifier DC gain is infinite. It can include some degree of voltage dependence. The dynamic settling error, $\varepsilon_{d}$, is determined by the limited bandwidth of the amplifier and is the relative error made by the amplifier in trying to achieve $V_{\text {out }}[t=\infty]$ after a predetermined amount of time, say one clock period $T$, compared to when the bandwidth is infinite. It can include some non-linearity due to slewing and so should be optimized for the largest expected step input.

With $G \cdot V_{\text {step }}$ the step change $V_{\text {out }}$ would make from one clock transition to the next in the absence of circuit imperfections ( $G$ is the transfer gain, which is 1 for a $\mathrm{S} \& \mathrm{H}$ ), the actual step change in output from sample to sample is modified by $\varepsilon$, to give:

$$
\begin{equation*}
V_{\text {out }}[m T]-V_{\text {out }}[(m-1) T]=(1-\varepsilon) \cdot G \cdot V_{\text {step }}[m T] . \tag{3.1}
\end{equation*}
$$

The total relative settling error $\varepsilon$ is composed of both the static and dynamic contributions:

$$
\begin{equation*}
\varepsilon=\varepsilon_{s}+\varepsilon_{d} \tag{3.2}
\end{equation*}
$$

### 3.2.1 Static Error

Considering the amplifier control model presented in Fig. 3.3(a) for a standard charge-transfer SC circuit, $\varepsilon_{s}$ resulting from a limited DC gain, $A_{0}$, is obtained as:

$$
\begin{equation*}
\varepsilon_{s}=\frac{1}{A_{0}} \cdot\left(1+\frac{C_{i n}+C_{i n_{p a r}}}{C_{f b}}\right) . \tag{3.3}
\end{equation*}
$$

$A_{0}$ is well approximated by $g_{m} \times r_{o}$ - see Fig. 3.3(c). Non-linearity in $g_{m}$ has practically no effect on $A_{0}$, since the amplifier inputs always settle back to the same virtual earth level at the


Fig. 3.1 SC integrator with double-sampling input stage.


Fig. 3.2 Illustration of a sample-and-hold step response.
end of each clock period. Only variability in $r_{o}$ has some effect on $A_{0}$ for large output signal swings. An $A_{0}$ of at least $65-70 \mathrm{~dB}$ is achievable for supplies down to 1 V using some of the techniques presented in Chapter 4. This is sufficient for most applications. With such gains, non-linearity has only a minuscule influence on transfer distortion. Instead, the main focus of attention in amplifier design for SC circuits is how to achieve sufficient dynamic settling accuracy and how to keep a handle on distortion resulting from slewing. For these reasons, the topic of dynamic settling accuracy forms the bulk of the remainder of this chapter.

### 3.2.2 Dynamic Error

The block diagram of a typical feedback amplifier together with its frequency transfer characteristic are shown in Fig. 3.3. $A(\omega)$ is the frequency dependent open-loop gain, $\beta_{f b}$ is the feedback factor, and $\alpha$ is the feedforward factor. The gain-bandwidth product, $G B W$, is given by the DC gain times the open-loop bandwidth $\omega_{o l}$ of the amplifier. For a predominantly first order amplifier, where all parasitic poles due to extra internal nodes and from the switches are more than double $1 / \beta_{f b}$ times the dominant pole in the closed loop system, the $G B W$ can be approximated by the cut-off frequency where the gain is reduced to 1 [27]. Hence, the time constant of the amplifier in a closed loop configuration, with $A_{0} \gg 1 / \beta_{f b}$, is given by:

$$
\begin{equation*}
\tau=\frac{1}{\omega_{c l}}=\frac{1}{\beta_{f b} \cdot G B W} . \tag{3.4}
\end{equation*}
$$

Here, the closed loop bandwidth, $\omega_{c l}$, and $G B W$ are each expressed as a radial frequency. The radial $G B W$, as defined here, is also known as the transition frequency, $\omega_{T}$. The resulting relative dynamic settling error, for negligible slewing, is:

$$
\begin{equation*}
\varepsilon_{d}=e^{-\frac{T}{\tau}} . \tag{3.5}
\end{equation*}
$$

How this error is influenced by the non-linear effect of slewing is the subject of section 3.4.
Since the amplifier is required to drive a predominantly capacitive load, an OTA (Operational Transconductance Amplifier) with a high impedance output (current driven) is preferred


Fig. 3.3 (a) Amplifier feedback control model
(b) Frequency transfer of amplifier
(c) Settling model for SC charge-transfer circuit.
to an Opamp with a low impedance output (voltage driven). This is to avoid unnecessary extra dissipation in the output stage and to allow the dominant pole in the system to be formed by the effective load capacitance and not by an internal opamp node (e.g. a Miller Opamp). The (capacitive) feedback ensures that the output impedance in a closed loop configuration is low in fact the output resistance of the closed loop OTA is only larger than that of a unity buffer configuration by a factor of $1 / \beta_{f b}$. Consider a typical representation of a SC feedback amplifier between clock transitions shown in Fig. 3.3(c). The total extrinsic input capacitance is represented by $C_{i n}$, the feedback capacitance by $C_{f b}$, while the total extrinsic load capacitance is given by $C_{L}$. The total amplifier parasitic capacitances seen at the input and output nodes are represented by capacitors $C_{i n_{p a r}}$ and $C_{o u t} p_{p a r}$, respectively. For instance, the SC integrator circuit of Fig. 3.1 can be represented by the circuit in Fig. 3.3(c) for analysis of its settling behaviour. The feedback factor is just:

$$
\begin{equation*}
\beta_{f b}=\frac{C_{f b}}{C_{i n}+C_{i n_{p a r}}+C_{f b}} . \tag{3.6}
\end{equation*}
$$

The $G B W$ is given by $g_{m} / C_{L_{e f f}}$, where $C_{L_{e f f}}$ is the total effective load capacitance the amplifier sees at its output:

$$
\begin{equation*}
C_{L_{e f f}}=C_{L}+C_{o u t_{p a r}}+\beta_{f b} \cdot\left(C_{i n}+C_{i n_{p a r}}\right) . \tag{3.7}
\end{equation*}
$$

From (3.4), the dominant closed-loop linear settling time constant is given by:

$$
\begin{equation*}
\tau=\frac{1}{\beta_{f b}} \cdot \frac{C_{L_{e f f}}}{g_{m}} . \tag{3.8}
\end{equation*}
$$

The complete relative settling error of a standard charge-transfer SC circuit becomes:

$$
\begin{equation*}
\varepsilon=\frac{1}{g_{m} \cdot r_{o}} \cdot\left(1+\frac{C_{i n}+C_{i n}}{C_{f b}}\right)+e^{-\frac{T \cdot \beta \cdot g_{m}}{C_{e f f}}} . \tag{3.9}
\end{equation*}
$$

Note a better formulation for $\tau$, for the sake of more insightful calculations, is:

$$
\begin{equation*}
\tau=\frac{1}{g_{m}} \cdot\left[\frac{C_{L \text { total })}}{\beta_{f b}}+C_{i n(\text { total })}\right] . \tag{3.10}
\end{equation*}
$$

Hence, for the circuit of Fig. 3.3(c), the linear time constant becomes:

$$
\begin{equation*}
\tau=\frac{1}{g_{m}} \cdot\left[\left(C_{L}+C_{o u t_{p a r}}\right) \cdot \frac{\left(C_{i n}+C_{i i_{p a r}}+C_{f b}\right)}{C_{f b}}+\left(C_{i n}+C_{i n_{p a r}}\right) .\right. \tag{3.11}
\end{equation*}
$$

Although the specific settling accuracy requirements at application level will be dealt with in Chapters 5, 7 and 8 in the context of filters and ADCs, for many applications, the amplifier is required to reach its end value to within $0.2 \%$ between clock transitions. A DC gain of $65-70 \mathrm{~dB}$ is achievable down to low supply voltages without compromising the settling response. This leaves about a further $0.1 \%$ error tolerance for incomplete settling $\left(\varepsilon_{d}\right)$. For a single-sampling realization, a maximum of half a clock period is allowed for settling, requiring $\tau<T / 14$. The OTA bandwidth needs to be over 2 times greater than the clock frequency. On the other hand, for a double-sampling realization, the full clock period is reserved for settling
and this translates to $\tau<T / 7$. Now the OTA bandwidth only needs to be of the order of the clock frequency.

High-frequency (HF) applications of SC circuits [28] (typically IF filtering, decimation, sub-sampling) usually have to deal with a wide spectrum of frequencies ( $B_{R F}$ ) from which, eventually, a relatively small frequency channel $\left(B_{c h}\right)$ must be distinguished and processed at baseband - see Fig. 3.4. The most important function of the IF filter is to reduce the dynamic range requirements of the following stage, often an ADC. The relative steepness factor of the filtering required at these frequencies (with bandwidth $B_{I F}$ ) is much lower than required for low frequency baseband processing (with bandwidth $B_{c h}$ ), even after sub-sampling. This translates into a lower settling requirement, and hence relative accuracy requirement, at IF compared to baseband without compromising overall accuracy. A $5 \tau$ settling specification is much more typical of HF applications.

### 3.3 Design Procedure for Optimized Settling

This section sets out the most important design considerations for designing an OTA that minimizes the linear settling time constant, $\tau$ (thus maximizing the $G B W$ ). This ensures a minimum power solution. The procedure is summarized in Fig. 3.5. Firstly, a choice is made for a single-ended or fully-differential solution depending on the required application. Next, a choice is made for the capacitor sizes, depending principally on noise and mismatch considerations. The OTA architecture is then chosen depending on such design issues as supply voltage, bandwidth, DC gain, noise, current consumption and active area. The next important choice to be made is for the $V_{o n}$ voltage of the input differential stage. This choice balances the needs for a maximum $g_{m}$, good transistor matching, low noise, maximum output signal range and low distortion as a result of slewing behaviour. Finally, it is possible to calculate what the DC bias current of the OTA must be in order to maximize the $G B W$ while allowing a maximum amount of slewing. This section continues by examining an OTA for SC applications with an NMOS differential input (e.g. Fig. 3.6) but the findings are general for all OTA types.

### 3.3.1 Single-Ended or Fully-Differential

At circuit block level, depending on the SC application, the designer must make a choice on whether a single-ended (SE) or fully-differential (FD) OTA is more suitable. A FD realisation is often preferred because of its high common-mode noise immunity when the SC block is


Fig. 3.4 An example of a SC IF filtering application.


Fig. 3.5 Design procedure for a SC OTA.
placed in a noisy environment. The signal handling ability is double that of a SE realisation for the same supply voltage. However, because of the doubling of the number of switching branches, the circuit area is almost doubled, while the switch thermal noise is 3 dB higher than a SE realisation for the same capacitor sizes. For the same OTA architecture, the OTA noise and power dissipation remain the same. Note that the noise of the switches usually dominates the noise of the OTA since the OTA's own noise is largely bandlimited by its own closed-loop bandwidth before it folds back.

From the foregoing discussion, it is imperative to increase the signal range of the FD SC circuit by a factor of 2 compared to the equivalent SE SC circuit for optimum signal processing. The net result is at least a 3 dB better $S N R$ for a 3 dB extra total power dissipation. For HF applications, the extra dissipation in the clock drivers is also important to the total power budget - the power dissipated by these drivers is doubled due to the doubling of the switch capacitance and the accompanying wiring capacitance. Thus, in reality, the total power dissipation is more than 3 dB higher for a FD SC circuit for a maximum $S N R$ improvement of only 3 dB . Often the signal to be processed is delivered by a separate chip delivering a SE output and it may be required for the SC circuit to deliver the processed signal to a following chip which, in turn, requires a SE input. The extra conversions from single-ended to differential and back again cost power and area and just add noise. This may be undesirable in such applications and a single-ended design could be more suitable.

### 3.3.2 Capacitor Sizes

The next choice the designer is faced with is signal capacitor sizing. Initially, the designer is only interested in capacitor ratios, since these correspond, for instance, to the filter coefficients to be implemented by the SC circuit block. The information the designer needs to make a choice for the absolute capacitor sizes is the noise specification (allowed $k T / C$ ), whether or not a SE or FD circuit is to be built, the signal swing (depending on $V_{D D}$ and $V_{r e f}$ ), the worst case capacitor mismatch (depending on the worst case aliasing and linear distortion that can be tolerated), and the worst case circuit dynamics (charge transfer inaccuracy due to finite OTA bandwidth and the effect of parasitic poles and zeros).

### 3.3.3 OTA Architecture

A black box OTA specification for SC applications can be developed independently of OTA architecture. The eventual choice of OTA architecture is motivated by such issues as available power supply, signal handling, excess power dissipation, excess noise, CMRR, PSRR and area. For this reason, this topic is deferred to Chapter 4 for detailed presentation.

The OTA architecture should be implemented such that the non-dominant pole is considerably higher in frequency than the unity gain frequency of the OTA. The phase margin, $P M$, for a single-stage or multi-stage OTA can be approximated by:

$$
\begin{equation*}
P M \approx 90^{\circ}-\tan ^{-1}\left(\frac{G B W}{\omega_{p a r}\left(\text { or } \omega_{c c}\right)}\right) . \tag{3.12}
\end{equation*}
$$

A good design strategy is to ensure that the parasitic pole $\omega_{p a r}$ (or indeed the second pole at


Fig. 3.6 Illustration of differential OTA transfer characteristic.
$\omega_{c c}$ due to the compensation capacitor in a two-stage OTA) is always more than double the $G B W$. This ensures the OTA has a $P M$ of at least $60^{\circ}$ and that the SC circuit settling response is at least critically damped and can be effectively modelled as a first order settling system.

### 3.3.4 Choice of $V_{\text {on }}$

When it comes to the design of the OTA itself, the first choice the designer must make is for the value of the $V_{o n}$ voltage of the input differential pair - see Fig. 3.6-which should be derived from the circuit block specifications. The voltage $V_{o n}$, assuming a quadratic MOST characteristic and $\beta=\mu \cdot C_{o x} \cdot \frac{W}{L}$, is defined here as:

$$
\begin{equation*}
V_{o n}=V_{g s}-V_{T}=\sqrt{\frac{I}{\beta}} \tag{3.13}
\end{equation*}
$$

and is the gate overdrive voltage assuming DC bias conditions with no AC signals. Here, $I / 2$ is the unmodulated drain current of each input MOST. The $V_{o n}$ is essentially an input bias variable. (Note that $V_{d s(s a t)}$, as defined in the symbol list, is the same as $V_{o n}$ for quiescent conditions only). The $V_{o n}$ is determined principally by current consumption, $g_{m}$, noise, matching and output signal range, as well as the allowable distortion resulting from slewing at maximum signal levels. Each of these points will be treated separately in the following sub-sections.

### 3.3.4.1 OTA Transconductance

Once the SC configuration is known for the intended design, and the circuit block level specifications are known, the transconductance, $g_{m}$, follows immediately.
The $g_{m}$ of each input NMOST is related to $V_{o n}$ by [25]:

$$
\begin{equation*}
g_{m}=\left.\frac{\partial I_{d s}}{\partial V_{g s}}\right|_{I_{d s}=\frac{I}{2}}=\frac{I}{V_{o n}} . \tag{3.14}
\end{equation*}
$$

The actual DC current is calculated through optimizing the speed of the chosen SC circuit, to be described in section 3.3.5. From (3.14), a small $V_{o n}$ is required for a large $g_{m}$.


Fig. 3.7 Illustration of 4 basic single-stage OTA types for the same SC application, each with the same $g_{m}$ and same current density per MOST. The linear settling time-constant per stage is the same, given by $\tau=\left(1 / g_{m}\right) \cdot\left[\left(C_{i n}+C_{f b}\right) \cdot C_{L} / C_{f b}+C_{i n}\right]$.

In Fig. 3.7, four basic OTA input stage types are illustrated together with their settling models for application in equivalent SC circuits. The linear settling time constant $\tau$ and transconductance are the same in each case. The $g_{m}$ 's of Fig. 3.7(a), (b), and (d) are the same as the $g_{m}$ of each input MOST. Only in the case of the differential to single-ended OTA of Fig. 3.7(c), (which avoids the use of the bandwidth limiting current mirror of Fig. 3.7(d) but at the cost of double the power consumption), is the OTA $g_{m}$ only half the $g_{m}$ of each input MOST. Note that although the linear settling performance of each OTA is the same, the slew rate of configurations (a) and (b) is only half that of (c) and (d).

### 3.3.4.2 Matching Considerations

A basic consideration in the choice of OTA transistor sizes and hence $V_{o n}$ is mismatch. The extended model for the variance of random parameter mismatch, $\Delta P$, of nominally identical MOSTs, with aspect ratio $W / L$ at distance $D_{x}$, can be written as:

$$
\begin{equation*}
\sigma^{2}(\Delta P)=\frac{A_{P 1}^{2}}{W \cdot L}+\frac{A_{P 2}^{2}}{W \cdot L^{2}}+\frac{A_{P 3}^{2}}{W^{2} \cdot L}+S_{\Delta P}^{2} \cdot D_{x}^{2}, \tag{3.15}
\end{equation*}
$$

where the technology dependent factors $A_{P 1}, A_{P 2}, A_{P 3}$ represent the area dependency, short channel effects, and narrow channel effects, respectively [16]. The final term $S_{\Delta P}$ gives the influence of device proximity on the mismatch variance. The primary mismatch term is that containing $A_{P 1}$, while the next term $A_{P 2}$ is becoming ever more important for deep sub-micron devices with small gate lengths of less than 100 nm . The contribution from the proximity term $S_{\Delta P}$ is found to be insignificant for device separations of less than $500 \mu \mathrm{~m}$. Even in modern day processes, MOST mismatch in analogue design can still be reasonably approximated using the first term in $A_{P 1}$, even down at 65 nm [29].

The mismatches in $V_{T}$ and $\beta$ MOST parameters are the most important contributors to overall device mismatch and are found via measurement to be statistically independent [16]. In both cases, the mismatch variance per MOST is primarily dependent on the inverse gate area:

$$
\begin{align*}
\sigma^{2}\left(\Delta V_{T}\right) & =\frac{A_{V_{T}}^{2}}{W \cdot L},  \tag{3.16}\\
\text { and } \quad \sigma^{2}\left(\frac{\Delta \beta}{\beta}\right) & =\frac{A_{\beta}^{2}}{W \cdot L} . \tag{3.17}
\end{align*}
$$

This dependence has been shown to hold for both strong saturation and weak inversion [30].
For a differential pair biased in strong inversion, such as in Fig. 3.6, and assuming the quadratic model holds for the current-voltage relationship (3.13), the variance of the total input voltage offset due to mismatch between the nominally identical NMOSTs and mismatch in its drain currents can be derived as:

$$
\begin{align*}
\sigma^{2}\left(V_{\text {offset }}\right) & =2 \cdot \sigma^{2}\left(\Delta V_{g s_{n}}\right) \\
& =2 \cdot \sigma^{2}\left(\Delta V_{T_{n}}\right)+\frac{1}{2} \cdot V_{o n_{n}}^{2} \cdot\left(\frac{\sigma^{2}\left(\Delta \beta_{n}\right)}{\beta_{n}^{2}}+\frac{\sigma^{2}\left(\Delta I_{d}\right)}{I_{d}^{2}}\right) . \tag{3.18}
\end{align*}
$$

Since the current mismatch in the input NMOST pair must be the same as that in the PMOST current sources for a differential realization, or indeed in the PMOST current mirror of a sin-
gle-ended realization, then the variance of the relative drain current mismatch normalized to $I_{d}^{2}$ is:

$$
\begin{equation*}
\frac{\sigma^{2}\left(\Delta I_{d}\right)}{I_{d}^{2}}=\frac{\sigma^{2}\left(\Delta I_{d}\right)}{(I / 2)^{2}}=\frac{\sigma^{2}\left(\Delta \beta_{p}\right)}{\beta_{p}^{2}}+4 \cdot \frac{\sigma^{2}\left(\Delta V_{T_{p}}\right)}{V_{o n_{p}}^{2}} . \tag{3.19}
\end{equation*}
$$

Hence, the total input referred offset voltage variance can be found from substituting (3.19) into (3.18):

$$
\begin{equation*}
\sigma^{2}\left(V_{\text {offset }}\right)=2 \cdot \sigma^{2}\left(\Delta V_{T_{n}}\right)+2 \cdot \sigma^{2}\left(\Delta V_{T_{p}}\right) \cdot\left(\frac{V_{o n_{n}}}{V_{o n_{p}}}\right)^{2}+\frac{1}{2} \cdot V_{o n_{n}}^{2} \cdot\left(\frac{\sigma^{2}\left(\Delta \beta_{n}\right)}{\beta_{n}^{2}}+\frac{\sigma^{2}\left(\Delta \beta_{p}\right)}{\beta_{p}^{2}}\right) . \tag{3.20}
\end{equation*}
$$

For the usual operating conditions of analogue circuits, it has been shown that $V_{T}$ mismatch dominates over $\beta$ mismatch [30]. The condition for which both sources of mismatch make an equal contribution to the random input offset voltage is defined by the corner $V_{o n}$ voltage, $V_{o n_{C}}$ :

$$
\begin{equation*}
V_{o n_{C}}=2 \cdot \frac{A_{V_{T}}}{A_{\beta}} . \tag{3.21}
\end{equation*}
$$

For submicron CMOS, $A_{V_{T_{n}}} / A_{\beta_{n}}$ is typically in the range $0.5-1.0 \mathrm{~V}$. Hence, for $V_{o n}$ smaller than about $1.0 \mathrm{~V}, V_{T}$ mismatch is still more significant than $\beta$ mismatch and the first two $V_{T}$ mismatch terms of (3.20) dominate the $\beta$ mismatch terms.
$V_{o n_{p}}$ is often two to three times larger than $V_{o n_{n}}$ for the following main reasons. Since the PMOST current sources don't need to have a large $g_{m}, \beta_{p}$ of the PMOST current sources is usually a lot less than $\beta_{n}$ of the input stage. Secondly, the PMOST current sources are usually designed with non-minimum gate lengths in order to create a reasonably high output resistance. A further justification for allowing $V_{o n_{p}}$ to be much larger than $V_{o n_{n}}$ is that it is usual to choose a low reference voltage (of less than $V_{D D} / 2$ ) in (HF) SC circuits, since this enables the use of NMOST switches only which can be three to four times smaller than their PMOST counterparts for the same resistance. From this it can be concluded that the systematic mismatch in threshold voltages of the input stage MOSTs, $\Delta V_{T_{n}}$, is the dominant source of mismatch in OTAs for SC applications, where $\sigma^{2}\left(V_{\text {offset }}\right) \approx 2 \cdot \sigma^{2}\left(\Delta V_{T_{n}}\right)$.

From the above considerations for input-stage mismatch, as well as the need for a large OTA $g_{m}$ and large output signal range, the $V_{o n}$ of the input stage MOSTs should be designed as small as possible but sufficient to ensure the input differential pair is biased well into strong inversion. Typically, input stage $V_{\text {on }}$ should be in the range of $150-250 \mathrm{mV}$ for 2.5 V supply voltage applications. Furthermore, when biasing those transistors which cascode the input differential pair, an extra voltage margin, $V_{\text {margin }}$, is needed to ensure the differential pair doesn't enter its linear region with a consequent sharp fall off in OTA DC gain. $V_{\text {margin }}$ is typically about 100 mV . Under equilibrium conditions, the drain-source voltage of each input stage MOST is set at:

$$
\begin{equation*}
V_{d s(\text { input pair })}=V_{o n}+V_{\text {margin } n} . \tag{3.22}
\end{equation*}
$$

### 3.3.4.3 Influence of Channel Mobility Factor

The value for the mobility factor, $\mu$, used in the preceding formulae for the MOST $\beta$ factor, is not constant. For sub-micron CMOS, mobility reduction should also be taken into account
when determining the $V_{o n}$, where the simplified single-dimensional MOST model is no longer totally accurate [31]. The first effect of interest is vertical field mobility degradation, where the field between the gate and the channel causes the charge carriers in the channel to slow down for high gate-source voltages due to the increasing pull on the inversion layer towards the gateoxide silicon interface. The effective mobility, $\mu_{e f f}$, is given by:

$$
\begin{equation*}
\mu_{e f f}=\frac{\mu_{0}}{1+\theta_{1} \cdot V_{o n}+\theta_{2} \cdot\left(\sqrt{V_{s b}+2 \cdot \phi_{F}}-\sqrt{2 \cdot \phi_{F}}\right)}, \tag{3.23}
\end{equation*}
$$

where $\mu_{0}$ is the low field mobility (typically, $5 \times 10^{10} \mu \mathrm{~m}^{2} \mathrm{~V}^{-1} \mathrm{~s}^{-1}$ ), and $\theta_{1}$ is a process dependent factor inversely proportional to the oxide thickness (typically $\frac{24 \mathrm{~A}}{d_{o x}} \mathrm{~V}^{-1}$ ). Since the back-gate voltage, $V_{s b}$, has a similar effect on reducing mobility in the channel as does $V_{g s}$, this is accounted for in (3.23) by adding an extra term $\theta_{2} \cdot\left(\sqrt{V_{s b}+2 \cdot \phi_{F}}-\sqrt{2 \cdot \phi_{F}}\right)\left(\theta_{2}\right.$ is a constant of approximately $0.5 \mathrm{~V}^{-1}$ ).

The second effect is horizontal field mobility degradation. The electric field between the source and drain propels carriers along the channel with their velocity being directly proportional to the horizontal field strength for low field strengths. With increasing horizontal field strength, the carriers velocity tapers off eventually reaching velocity saturation ( $v_{\text {sat }}$ ) for large field strengths. The mobility factor needs to be further modified to include $v_{\text {sat }}$, so that:

$$
\begin{equation*}
\mu=\frac{\mu_{e f f}}{1+\frac{\mu_{e f f} \cdot V_{d s}}{L \cdot v_{s a t}}}, \tag{3.24}
\end{equation*}
$$

where $\mu e f f$ is obtained from (3.23). For silicon, $v_{s a t}$ is a constant of value $1.1 \times 10^{5} \mathrm{~ms}^{-1}$. Equation (3.24) for $\mu$ should be used to include all electric field effects.

### 3.3.4.4 Choice of Gate Lengths

In order to achieve a large $G B W$ and low input stage $V_{o n}$ for say HF applications, the input stage MOSTs require a large $W / L$. Moreover, the gate capacitance must be kept to a minimum to maximize speed. This leads to the conclusion that the $L$ of the input devices must be chosen to be the minimum size available in the process. The price to be paid is a small worsening of the input stage mismatch but it was concluded in section 3.3.4.2 above that this is not significant when a small $V_{o n_{n}}$ is chosen. Furthermore, it was argued in 3.3.4.2 that the PMOST current sources in a FD OTA should have large gate lengths. Note that SE OTAs (with differential input), based on the model shown in Fig. 3.7(d), are less suitable for HF applications than FD OTAs due to the presence of a large parasitic pole at the mirror node. The most important consideration in the choice of the $L$ 's for those MOSTs other than the input stage MOSTs is how to achieve the required DC gain without compromising headroom. A trade-off should be made between choosing a larger $L$ and the use of extra cascoding with the consequent reduction in output headroom and degradation in high frequency performance.

### 3.3.5 Minimum Settling Time Constant and Bias Current

Once the MOST current densities ( $I / 2 \cdot W$ ) and signal capacitor values are known, the design procedure continues by optimizing the OTA design to achieve a minimum value of the linear
settling time constant, $\tau$. The absolute value of $W / L$ will then follow.
The assumption is made that:

$$
\begin{equation*}
C_{\text {outpar }}=\kappa \cdot C_{\text {inpar }}, \tag{3.25}
\end{equation*}
$$

where all the parasitic capacitances in the OTA scale with $W$ of the input devices. $C_{\text {outpar }}$ results from the junction capacitances at the drain nodes of all the output devices, as well as their gatedrain overlap capacitances. $\kappa$ is typically between 0.5 and 2 depending on OTA topology and required output signal range. Other parasitic capacitances, in particular wiring capacitance, can be lumped together with the external load $C_{L}$, or with the input capacitor $C_{i n}$, for the sake of calculating the settling response. The linear time constant, $\tau$ from (3.11), becomes:

$$
\begin{gather*}
\tau=\frac{1}{\mu \cdot C_{o x} \times \frac{W}{L} \cdot V_{o n}} \cdot\left[\frac{1}{C_{f b}} \cdot\left(C_{i n}+\frac{2}{3} \cdot \mu \cdot C_{o x} \cdot W \cdot L+C_{f b}\right) \cdot\left(C_{L}+\kappa \cdot \frac{2}{3} \cdot \mu \cdot C_{o x} \cdot W \cdot L\right)\right.  \tag{3.26}\\
\left.+C_{i n}+\frac{2}{3} \cdot \mu \cdot C_{o x} \cdot W \cdot L\right] .
\end{gather*}
$$

Note that the amplifier transconductance $g_{m}$ and input capacitance $C_{i n p a r}$ are related via the transition frequency $\omega_{T}$ (frequency of unity current gain) of the input devices by:

$$
\begin{equation*}
g_{m}=\omega_{T} \cdot C_{\text {inpar }} \tag{3.27}
\end{equation*}
$$

For a $0.25 \mu \mathrm{~m}$ CMOS process, the normalized settling time constant $\tau \cdot \omega_{T}$ of the SC amplifier of Fig. 3.1 is plotted in Fig. 3.8 as a function of $C_{i n} / C$ for different values of the stage gain $G=\frac{C_{i n}=G \cdot C}{C_{f b}=C}$. A value of $\kappa=0.7$ is taken here for a telelescopic type OTA, while a fixed load capacitance of $C$ is assumed. The input device sizes can be chosen to optimize the stage time constant for a given gain. In fact, the value of $W$ which minimizes $\tau$ is found by differentiating $\tau(3.26)$ with respect to $W$ and then finding that value of $W$ which sets the result to zero, i.e.


Fig. 3.8 Normalized settling time constant as a function of normalized input capacitance for different stage gains.

$$
\begin{equation*}
W_{\tau_{\text {min }}}=\frac{3 \cdot \sqrt{C_{i n} \cdot C_{L}+C_{f b} \cdot\left(C_{i n}+C_{L}\right)}}{2 \cdot C_{o x} \cdot L \cdot \sqrt{\kappa}} . \tag{3.28}
\end{equation*}
$$

Equation (3.28) can be substituted into (3.26) to obtain $\tau_{\text {min }}$. Since $W_{\tau_{\text {min }}}$ is now known, and since the current density of the input devices is known through their $V_{o n}$, it follows that the corresponding bias current, $I_{\tau_{\text {min }}}$, of each input MOST can now be found. Note that $\tau_{\text {min }}$ is inversely proportional to $V_{o n}$ as expected, since the input device $f_{T}$, and thus the $G B W$ of the OTA, is directly proportional to $V_{o n}$, where:

$$
\begin{equation*}
G B W=\frac{\mu \cdot C_{o x} \cdot \frac{W}{L} \cdot V_{o n}}{C_{L_{e f f}}} . \tag{3.29}
\end{equation*}
$$

### 3.4 OTA Slewing Requirement in SC Applications

In this section, the minimum requirements on OTA slew rate are examined and design guidelines given. The dynamic error arising from incomplete settling under extreme signal conditions will be quantified for a CMOS OTA in a SC application.

### 3.4.1 The Slew Rate Model

In sections 3.2 and 3.3, the OTA dynamic performance has been examined in terms of its linear settling response - in effect, the small signal response. Here, the generalized condition for OTA slewing is presented. The OTA in a SC circuit begins to slew when, for a given input signal frequency, the amplitude of the input signal is increased to a point where the output can no longer follow the input in a linear manner. Alternatively, for an input signal of a given amplitude, the OTA in a SC circuit begins to slew when the frequency of the input signal is increased to a point where the output can no longer follow the input in a linear manner. Both these cases define the point when the OTA is said to be slew rate limited.

Before the settling performance of the SC stage can be finally optimized, the large signal slewing effects must be taken into account [32]. This is of particular relevance for HF applications, where the slewing part of the total settling period can be relatively large when compared with LF applications, such as audio. The limitations in linear settling described in the previous sections only cause linear distortion - in essence, only the accuracy of the desired transfer function is affected. Slewing has the additional effect of creating non-linear distortion, so producing higher harmonics and intermodulation products of the output signal [33]. Because of the sampled data nature of SC circuits, slewing is only of major concern when making the transition from the sampled data domain to the continuous time domain, for instance just before the output reconstruction filter. In the pure sampled data path, amplifier slewing for maximum signal handling can account for at least $20 \%$ of the total settling time.

With $V_{\text {out }}$ the instantaneous output voltage of the SC circuit, the minimum OTA slew rate, $S R$, to ensure no slewing occurs, is given by the initial slope of the linear settling response for the maximum expected step change, i.e.

$$
\begin{equation*}
S R \geq\left.\frac{\delta}{\delta t} V_{\text {out }}\left(t=0^{+}\right)\right|_{\max } \tag{3.30}
\end{equation*}
$$

For dominant first order settling, the maximum rate of change at the output is $E_{\max } / \tau$, where $E_{\max }$ is the maximum expected output step change in going from one sample instant to the next. Hence,

$$
\begin{equation*}
S R \geq \frac{E_{\max }}{\tau} . \tag{3.31}
\end{equation*}
$$

This provides a starting point for analysing the $S R$ in an actual SC application.

### 3.4.2 Minimum OTA Tail Current for No Slewing

Assuming a Class A fully-differential OTA, such as shown in Fig. 3.6(a), with a tail current $I$, then a maximum current of $\pm I / 2$ is available at the output nodes for charging and discharging the external capacitance. During the slewing period, no linear feedback occurs to the OTA input node. From the OTA transfer characteristic of Fig. 3.6(b), it can be seen that the OTA slews when the differential input voltage falls outside the range $\pm \sqrt{2} V_{\text {on }}$. The slew rate, is given by:

$$
\begin{equation*}
S R=\frac{I / 2}{C_{L(e f f)}} . \tag{3.32}
\end{equation*}
$$

For a SC circuit processing a sinewave signal of frequency $f_{i n}$, the oversampling ratio $(O S R)$ of the circuit is:

$$
\begin{equation*}
O S R=f_{s} / f_{i n} \tag{3.33}
\end{equation*}
$$

Consider now such a signal with maximum amplitude $A_{\max }$. The maximum rate of change at the SC circuit output occurs when the sample instants are placed symmetrically around the zero crossings (centred at $V_{\text {ref }}$ ). Such a situation is illustrated in Fig. 3.9 for an $O S R$ of 6. In general, to guarantee no slewing occurs in a SC application, the minimum $S R$ is bounded by:

$$
\begin{equation*}
S R \geq 2 \cdot \frac{A_{\max }}{\tau} \cdot \sin \left(\frac{\pi}{O S R}\right) \tag{3.34}
\end{equation*}
$$

This is the same for either single-sampling or double-sampling. Equation (3.34) provides a direct relationship between the small signal and large signal properties of the OTA. Combining (3.32) and (3.34), the minimum OTA tail current to ensure no slewing is given by:


Fig. 3.9 Specifying condition for no slewing with max. $O S R=6$.


Fig. 3.10 Capacitor configuration seen at SC circuit input at $t=0^{+}$.

$$
\begin{equation*}
I \geq 4 \cdot \frac{\left.A_{\max } \cdot C_{L(e f f)}\right)}{\tau} \cdot \sin \left(\frac{\pi}{O S R}\right) . \tag{3.35}
\end{equation*}
$$

### 3.4.3 Calculation of Slew Time, $\boldsymbol{t}_{\text {slew }}$

The SC OTA is often allowed to slew for a certain amount of its total settling time, depending on the maximum distortion allowed under extreme large signal conditions. As for the linear settling case of section 3.3, the non-inverting SC charge transfer stage of Fig. 3.1 is used as reference. Initially, the input signal capacitor $C_{\text {in }}$ is charged up to a voltage level, $V_{\text {step }} . V_{\text {step }}$ is just the instantaneous value of $V_{\text {in }}$ after sampling, i.e. $V_{\text {in }}\left(t=0^{+}\right)=V_{\text {step }}$. One clock period $T$ later, $C_{\text {in }}$ is inverted and connected to the differential input stage of the OTA. The OTA does not react immediately because of its limited bandwidth [33]. Instead, the charge on $C_{\text {in }}$ is distributed between all capacitors connected to the OTA input node (see the equivalent input path in Fig. 3.10). Note, it is assumed that the time constant of the SC branches is significantly smaller than the OTA settling time constant. The effect is to create a small voltage jump at the OTA differential input given by:

$$
\begin{gather*}
V_{d}\left(t=0^{+}\right)=\gamma \cdot V_{\text {step }},  \tag{3.36}\\
\text { where } \quad \gamma=\frac{C_{\text {in }}}{C_{\text {in }}+C_{\text {in }(p a r)}+\frac{C_{f f} \cdot\left(C_{L}+C_{\text {out }(p a r)}\right)}{\left.C_{f b}+C_{L}+C_{\text {out }(\text { par })}\right)}} .
\end{gather*}
$$

The initial output voltage jump, $V_{\text {out }}\left(t=0^{+}\right)$, can simply be derived through calculating the feedforward voltage of $V_{d}$ to the output, i.e.

$$
\begin{equation*}
V_{\text {out }}\left(t=0^{+}\right)=\frac{C_{f b}}{C_{f b}+C_{L}+C_{\text {out }(\text { par })}} \cdot \gamma \cdot V_{\text {step }} . \tag{3.38}
\end{equation*}
$$

Consider now the form of the step input voltage $V_{d}$ depicted in Fig. 3.11. The maximum input step size for which the OTA remains operating in its linear region is $\sqrt{2} V_{o n}$ (e.g., Fig. 3.6). When the magnitude of $\gamma \cdot V_{\text {step }}$ exceeds $\sqrt{2} V_{\text {on }}$, the OTA delivers its maximum current of $\pm I / 2$, which is the condition for slewing. Hence, the following equation can be set up, assuming the OTA makes a smooth transition from the slewing region to the linear settling region of its step response characteristic:

$$
\begin{equation*}
\left|\frac{\gamma \cdot V_{\text {step }}-\sqrt{2} \cdot V_{\text {on }}}{t_{\text {slew }}}\right|=\left|\frac{\sqrt{2} \cdot V_{\text {on }}}{\tau}\right| . \tag{3.39}
\end{equation*}
$$

(a)


Fig. 3.11 Variation of OTA input voltage $V_{d}$ for step change in $V_{i n}$
(a) Non-overlapping clocks $\varphi_{1}, \varphi_{2}$
(b) Linear settling only
(c) Slewing followed by linear settling.

Note (3.39) is set up assuming $V_{d}\left(t=0^{-}\right) \approx 0$, since it is usually only a small fraction of $V_{o n}$ and so may be ignored for this calculation of $t_{\text {slew }}$ without too much inaccuracy. Now, $t_{\text {slew }}$ can be calculated directly in terms of $\tau$ to be:

$$
\begin{equation*}
t_{\text {slew }}=\tau \cdot\left(\frac{\gamma \cdot\left|V_{\text {step }}\right|}{\sqrt{2} \cdot V_{\text {on }}}-1\right) . \tag{3.40}
\end{equation*}
$$

What (3.40) shows is that the slew time depends directly on the linear settling time constant of the OTA. Minimization of the settling time constant, such as described in section 3.3, implies the slew time is also minimized for a given signal amplitude above $\sqrt{2} V_{o n}$. If because of distortion considerations the slew time is too large, $V_{\text {on }}$ must be increased by increasing the OTA quiescent current and reducing the input stage gate widths. The linear time constant optimization procedure should be repeated with this new data.

The model presented here is valid for the general OTA types presented in Chapter 4. For telescopic and folded cascode OTAs, the maximum output current is just $\pm I / 2$, where $I$ is the
tail current. The current gain OTA can deliver a maximum output current of $\pm N \times I / 2$, where $N$ is the current gain factor. On the other hand, for OTAs where the dominant time constant is not dictated by the load capacitance - for example, the Miller OTA - it is possible to have an input slewing (due to the Miller capacitance $C_{c}$ ) which is different to the output slewing (due to $C_{L}$ ). However, the following argument justifies the use of the above slew rate model for such two stage OTAs.

For a properly designed two-stage OTA, the dominant settling time constant is formed by the Miller capacitance instead of the load capacitance - see section 4.1.2.3. The phase margin should be greater than $60^{\circ}$ - see (3.12). Hence, the following condition must hold true in a closed loop configuration:

$$
\begin{equation*}
\frac{g_{m_{\text {out }}}}{C_{L}+C_{c}}>2 \cdot \frac{g_{m_{\text {in }}}}{C_{c}}, \tag{3.41}
\end{equation*}
$$

where $g_{m_{\text {in }}}$ and $g_{m_{\text {out }}}$ are the input and output stage transconductances, respectively. The slewrate model presented here applies to the input slewing, caused by a shortage of current in the input differential pair for large input steps. Assuming similar current densities for the input and output stages, the required compensation implies that if the input stage satisfies the conditions for slewing, then the output stage will automatically satisfy the slewing requirement. Indeed, for a well designed two-stage OTA, the following condition should be satisfied:

$$
\begin{equation*}
\frac{I_{\text {out }}}{C_{L}+C_{c}}>\frac{I_{\text {in }}}{C_{c}} . \tag{3.42}
\end{equation*}
$$

### 3.4.4 Dynamic Settling Error including OTA Slewing

When the OTA slews at the beginning of its step response, the relative settling error $\varepsilon_{d}$ at the end of each sample period becomes signal level dependent. Linear settling starts directly after the transition from the slewing period (see Fig. 3.11). With $n$ defined as:

$$
\begin{equation*}
n=\frac{T-t_{\text {slew }}}{\tau} \tag{3.43}
\end{equation*}
$$

the total relative dynamic settling error, including slewing contribution, becomes:

$$
\begin{equation*}
\varepsilon_{d}=\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma \cdot V_{\text {step }}} \cdot e^{-n}, \quad \text { for }\left|V_{\text {step }}\right|>\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma} . \tag{3.44}
\end{equation*}
$$

After substitution of $t_{\text {slew }}$ from (3.40), the step change in output voltage in the presence of both static and dynamic errors is obtained from (3.1) to be:

$$
\begin{array}{ll}
V_{\text {out }}[m T]-V_{\text {out }}[(m-1) T]= \\
{\left[\begin{array}{ll}
V_{\text {step }} \cdot \frac{C_{\text {in }}}{C_{f b}} \cdot\left(1-\frac{\left.C_{\text {fb }}+C_{\text {in }}+C_{\text {in }(\text { par }}\right)}{g_{m} \cdot \text { out }^{\prime} \cdot C_{f b}}\right) \cdot\left(1-e^{-\frac{T}{\tau}}\right), & \text { for }\left|V_{\text {step }}\right| \leq \frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma} \\
V_{\text {step }} \cdot \frac{C_{\text {in }}}{C_{f b}} \cdot\left(1-\frac{\left.C_{f b}+C_{\text {in }}+C_{\text {in }(\text { par }}\right)}{g_{m} \cdot \text { out } \cdot C_{f b}}\right) \cdot\left(1-\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma \cdot V_{\text {step }}} \cdot e^{-\left(\frac{T}{\tau}+1-\frac{\gamma \cdot\left|V_{\text {step }}\right|}{\sqrt{2} \cdot V_{\text {on }}}\right)}\right), & \text { for }\left|V_{\text {step }}\right|>\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma}
\end{array}\right.} \tag{3.45}
\end{array}
$$



Fig. 3.12 Percentage THD due to slewing for a symmetrical SC circuit with $V_{\text {on }}=0.15 \mathrm{~V}, \tau=5 \mathrm{~ns}, \gamma=0.4$ and different signal amplitudes, $A$.

With linear settling only, the settling of the SC circuit is independent of signal level. However, once amplifier slewing occurs, signal level dependency is introduced in the end values and distortion results. A Taylor series expansion of (3.45) for the partially slewing case demonstrates this. Ultimately, the choice of $\varepsilon_{d}$ for the maximum expected signal amplitude is governed by the maximum acceptable distortion, for example as discussed for the error model of an ADC in section 8.2.1. In Fig. 3.12, a guide to estimating the distortion introduced by slewing in a charge-transfer SC circuit is shown for different signal amplitudes as a function of sample frequency.

### 3.5 Conclusions

The design strategy for a SC OTA is summarized in Fig. 3.5. Firstly, a suitably low $V_{o n}$ is chosen for reasons mentioned in section 3.3 - principally high $g_{m}$, optimized matching, low noise and high signal handling. From this, the current density $(I / 2 \cdot W)$ of the input stage is found and then based on the minimization of linear settling time, the actual values of $W$ and $I$ can be ascertained. All the transistor dimensions in the OTA can then be determined based on this small signal optimization. Large signal conditions, however, have the ultimate say in the final dimensioning of the OTA. If, after the small signal optimization described in section 3.3, the slew rate is not yet sufficient for the largest signal levels envisaged, as analysed in section 3.4, the $V_{\text {on }}$ must be increased and the small signal optimization process repeated.

## Chapter 4

## Amplifier Architectures for SC Applications

Having presented the strategy for OTA design at a macro level for SC applications in Chapter 3, the next step is to choose a suitable OTA architecture for a dedicated application. The main issues addressed by the choice of OTA architecture are DC gain, parasitic poles and zeros, signal range, and excess power and noise, as well as how best to make use of the properties of SC circuits to enhance OTA gain and settling performance. All these issues are considered in this chapter for a wide range of amplifiers and design insights offered.

### 4.1 Review of Amplifier Architectures

The purpose of this section is to review and analyse those amplifier architectures used predominantly in SC circuits. This sets the background for introducing new circuits and design techniques later on. Firstly, primary OTA stages are reviewed. Next, primary OTA stages with either pre- or post-cascaded stages for improvement of gain without loss of signal range are analysed for their suitability for use in SC circuits.

### 4.1.1 Primary OTA Stages

Primary OTA stages are defined here to be those amplifiers which have a dominant settling pole defined by the $g_{m}$ of the input stage and output capacitive load $C_{L_{e f f}}$. They are either sin-gle-stage (telescopic) or dual-stage (current mirror, folded) in which the signal current from the differential input stage is mapped to the high impedance output stage. These stages are firstly reviewed here.

### 4.1.1.1 Telescopic OTA

The basic single-stage, (single-input) telescopic OTA, or SITO, is the simplest amplifier structure and was used as reference in Chapter 3. Single-ended and differential examples are shown
in Fig. 4.1. The telescopic OTA is the most efficient OTA possible, where the same DC bias current is used both to determine the overall $g_{m}$ of the OTA and determine the output drive capability, or slew rate [34], [35]. The price to be paid is the limited signal range in a single reference application. If the inputs and outputs are held at the same reference level, then the input differential pair determines the maximum signal swing for symmetrical signals. This is just $\pm\left|V_{T_{-}}-V_{o n_{p}}\right|$ for a cascoded telescopic OTA. Sometimes the cascode transistors $\left(M_{P_{4}}, M_{P_{5}}\right)$ are removed so as to increase the signal range by $\pm\left|V_{o n_{P}}\right|$. However, the gain of the OTA is reduced by the gain of the cascode $\left(\sim g_{m} r_{o}\right)$ and there is a strong Miller coupling of the gate-drain overlap capacitance - this is elaborated in section 4.3.2.

The input referred noise variance of the telescopic OTA is:

$$
\begin{equation*}
\overline{v_{n}^{2}}=\frac{16}{3} \cdot k \cdot T \cdot\left(\frac{1}{g_{m_{P 2}}}+\frac{g_{m_{N 1}}}{g_{m_{P 2}}^{2}}\right) \cdot \Delta f, \tag{4.1}
\end{equation*}
$$

where, in order to obtain the total input referred noise power, $\Delta f$ needs to be integrated over the equivalent noise bandwidth.

A modification to the basic SITO is shown in Fig. 4.2, in which the P-cascodes are self biased. The idea here is to make use of the strong back-gate effect of PMOSTs in a CMOS Nwell process. The common N -well of the input PMOSTs and the current source is connected to $V_{D D}$, while the common N -well of the P-cascodes $\left(M_{P_{4}}, M_{P_{5}}\right)$ are connected to the commonsource terminal of the input pair $\left(M_{P_{2}}, M_{P_{3}}\right)$. Typically, there is a large voltage over the current source both because the input reference voltage is chosen low and the current source needs to be biased strongly into saturation for a high output resistance - often the current source is cascoded. The difference in back-gate voltages between $\left(M_{P_{4}}, M_{P_{5}}\right)$ and $\left(M_{P_{2}}, M_{P_{3}}\right)$ is sufficient to ensure that the input pair remains in saturation. Two variants are shown. In Fig. 4.2(a),


Fig. 4.1 (a) Basic (single-input) telescopic OTAs: (a) differential, and (b) single-ended with high compliance current mirror.


Fig. 4.2 Telescopic OTA employing self-biased cascodes with
(a) symmetrical $P$-cascodes suitable for buffer
(b) gates of $P$-cascodes attached to + input, suitable for SC amplifiers.
the gate of cascode $M_{P_{4}}$ is connected to the gate of input PMOST $M_{P_{2}}$, while $M_{P_{5}}$ and $M_{P_{3}}$ are gate connected - this is symmetrical and is suitable for use as a buffer, with $V_{\text {out }}$ connected to $V_{i n_{n}}$. Fig. 4.2(b) is more suitable for use in a SC amplifier, where the gates of both $\left(M_{P_{4}}, M_{P_{5}}\right)$ are connected to $V_{i n_{n}}$. This avoids the coupling between the input and output that would occur with the gate-drain capacitance of $M_{P_{5}}$ in Fig. 4.2(a) when in an amplifier configuration. In a SC charge transfer stage, $C_{i n}$ can be connected between the stage input and $V_{i n_{n}}$, while $C_{f b}$ can be connected between $V_{\text {out }}$ and $V_{i n_{n}}$. A further variant of Fig. 4.2(a) and (b) is possible by connecting the N -wells of each of $\left(M_{P_{4}}, M_{P_{5}}\right)$ to their own sources. This increases the back-gate differential even further, thus further biasing the input stage $\left(M_{P_{2}}, M_{P_{3}}\right)$ into saturation. However, this also reduces the frequency of the parasitic pole at the sources of $\left(M_{P_{4}}, M_{P_{5}}\right)$ due to the N -well capacitance at these points and the extra wide diffusions, since the sources of $\left(M_{P_{4}}, M_{P_{5}}\right)$ can no longer directly overlap the drain diffusions of $\left(M_{P_{2}}, M_{P_{3}}\right)$.

### 4.1.1.2 Current Mirror OTA

The second type of primary OTA stage is the current mirror OTA of Fig. 4.3, where the signal current in each of the arms of the telescopic OTA is mirrored to an output stage [36]. Unlike the telescopic OTA, the input and output requirements are decoupled. The same reference voltage can be used at the input and the output, while the output signal range is decoupled from the signal range limitations of the input differential pair. A symmetrical output signal can vary to
within $2 \cdot V_{\text {on }}$ of each supply rail. The DC bias current needed to drive the output load is decoupled from the DC bias current needed to create the $g_{m}$ of the OTA. The current gain factor between $\left(M_{N_{1}}, M_{N_{2}}\right)$ and $\left(M_{N_{5}}, M_{N_{6}}\right)$ can be set by the designer with a factor of 1-4 being the usual choices. The larger the factor, the lower the output resistance though. The DC gain of the current mirror amplifier is the same as the telescopic OTA for equal input and output DC bias currents, namely:

$$
\begin{equation*}
A_{0}=-g_{m_{M P 6}} \cdot\left(g_{m_{M N 4}} \cdot r_{O_{M N 4}} \cdot r_{O_{M N 2}} \| g_{m_{M P 4}} \cdot r_{O_{M P 4}} \cdot r_{o_{M P 2}}\right) . \tag{4.2}
\end{equation*}
$$

The frequency response of the current mirror amplifier is much poorer than the telescopic OTA due to the presence of a large parasitic pole at the current mirror nodes. The dominant pole is again just $\omega_{P_{1}}=g_{m_{\text {in }}} / C_{L}$. Using NMOS current mirrors with a PMOS input stage, instead of PMOS current mirrors, helps to push this parasitic pole as far away as possible. With $M$ the current gain factor (i.e. $\left.\frac{W}{L}\right|_{M_{N 1}}=\left.M \cdot \frac{W}{L}\right|_{M_{N 5}}$ ), this pole is given by:

$$
\begin{equation*}
\omega_{P_{2}}=\frac{g_{m_{M N 6}}}{C_{g s_{M N 6}} \cdot(1+M)+C_{g d_{M P 8}}+C_{g d_{M N 2}} \cdot\left(1+\frac{g_{m_{M N 2}}}{g_{m_{M N 4}}}\right)+C_{d b_{M N 6}}+C_{d b_{M P 8}}} . \tag{4.3}
\end{equation*}
$$

Here, it is assumed that the impedance seen at the output of the OTA is much smaller than the output resistance of the OTA alone. Otherwise, the feedforward Miller effect of the overlap capacitance $C_{g d_{M N 2}}$ can become much greater than the intrinsic gain factor $g_{m_{M N 2}} / g_{m_{M N 4}}$. This Miller capacitance then creates a second large parasitic pole at the cascode node of transistors $M_{N_{2}}$ and $M_{N_{4}}$. This phenomenon is explained in more detail in section 4.3.2. Note the presence of transistors $\left(M_{P_{7}}, M_{P_{8}}\right)$. These are not essential but help reduce the size of the capacitance at the parasitic mirror node for HF applications. $\left(M_{P_{7}}, M_{P_{8}}\right)$ can be say 4 times smaller than $\left(M_{P_{5}}, M_{P_{6}}\right)$, with a corresponding increase in their $V_{\text {on }}$ voltage by a factor of 2. Typically,


Fig. 4.3 Fully differential current mirror OTA.
for a PMOS input stage as shown, the drain-bulk junction capacitance can be larger than the gate-source capacitance of each of the NMOS mirror transistors $\left(M_{N_{5}}, M_{N_{6}}\right)$. Thus, the addition of $\left(M_{P_{7}}, M_{P_{8}}\right)$ replaces the contribution of $C_{d b_{M P 5(6)}}+C_{g d_{M P 5(6)}}$ with $C_{d b_{M P 7(8)}}+C_{g d_{M P 7(8)}}$ which is about a quarter the size.

Although the input voltage of the PMOS differential pair can vary up to a maximum of $\pm\left|\sqrt{2} \cdot V_{o n_{P}}\right|$ before slewing, the minimum allowed input reference level is not set by $\left|\sqrt{2} \cdot V_{o n_{P}}\right|$ but by the minimum voltage span needed to keep the series of MOSTs $M_{N_{5}}$ to $M_{P_{5}}$ in their active regions. Hence, $V_{\text {ref }}>2 \cdot\left(V_{\text {on }}+V_{\text {margin }}\right) \approx 600 \mathrm{mV}$.

With a current mirror factor $M$, the input referred noise variance becomes:

$$
\begin{equation*}
\overline{v_{n}^{2}}=\frac{16}{3} \cdot k \cdot T \cdot\left(\frac{1}{g_{m_{P 5}}}+\frac{g_{m_{N 1}}+g_{m_{P 1}}}{M^{2} \cdot g_{m_{P 5}}^{2}}\right) \cdot \Delta f . \tag{4.4}
\end{equation*}
$$

The contribution of the cascodes can become significant at higher frequencies but have been left out of (4.4). For similar load conditions as the telescopic OTA, the current mirror OTA (with $M=1$ ) generates about double the noise of the telescopic.

### 4.1.1.3 Folded OTA

The third type of primary OTA structure is the folded cascode OTA [37]. This OTA is used with the same design aim as the current mirror OTA, i.e. increased output range when the same reference voltage is used at the input and the output. It has a strong similarity in structure to the current mirror OTA, with the mirror being replaced by current folding. The folded OTA, however, has a lower DC gain than the telescopic or current mirror OTAs. This is because, although the $g_{m}$ is the same for the same input DC bias current, the output resistance is lower. Here too, transistors $\left(M_{P_{7}}, M_{P_{8}}\right)$ have been added to reduce parasitic capacitance at the folding


Fig. 4.4 Fully differential folded cascode OTA.
node and, specifically for the folded OTA, to increase the resistance of the PMOS input stage as seen by the folded node and hence increase the overall output resistance. The DC gain becomes:

$$
\begin{equation*}
A_{0}=-g_{m_{M P 6}} \cdot\left(\left(g_{m_{M N 4}} \cdot r_{o_{M N 4}} \cdot r_{o_{M N 2}}\left\|r_{o_{M N 6}}\right\| g_{m_{M P 8}} \cdot r_{o_{M P P}} \cdot r_{o_{M P 6}}\right) \|\left(g_{m_{M P 4}} \cdot r_{o_{M P 4}} \cdot r_{o_{M P 2}}\right)\right) . \tag{4.5}
\end{equation*}
$$

Typically, the DC gain of a standard telescopic or current mirror OTA is in the order of 1000, whereas the gain of the folded cascode OTA depicted is in the order of 700. The main nondominant pole is created at the folded cascode node with value:

$$
\begin{equation*}
\omega_{P_{2}}=\frac{g_{m_{M N 4}}+g_{m b_{M N 4}}}{C_{g s_{M N 4}}+C_{g d_{M P 8}}+C_{d b_{M N 2}}+C_{d b_{M N 6} 6}+C_{d b_{M P 8}}} . \tag{4.6}
\end{equation*}
$$

It is important, when designing the folded cascode OTA, to ensure that the current in the output stage is always greater than the current flowing in the input stage, or else the current source transistors $\left(M_{N_{1}}, M_{N_{5}}\right)$ or $\left(M_{N_{2}}, M_{N_{6}}\right)$ can be forced into their linear operating regions during slewing, requiring a long recovery time before normal linear settling operation of the OTA can resume. Typically, the current in the output stage is up to $25 \%$ larger than in the input stage. Since the current mirror is replaced by a current source in the first stage, the minimum reference can go as low as $\left|\sqrt{2} \cdot V_{o n_{P}}\right|$, meaning the inputs can go right down to $V_{S S}$. Finally, the noise power generated by the folded OTA is about the same as that of the current mirror OTA (with $M=1$ ) for equal loads.

### 4.1.1.4 General Conclusions for the Three Primary OTA Stages

For similar applications, requiring similar bandwidth OTAs, the telescopic OTA uses only half the power and generates only half the noise of either the current mirror or folded OTAs. The main reason for using either the current mirror or folded OTAs is increased signal range, especially when the input and output reference voltages are the same. Although, in theory, the input and output current biasing can be different, in practice they are chosen about the same (with the folded OTA needing some extra output current as explained above), with similar $V_{o n}$ 's being used throughout. Sometimes the three primary OTA stages are referred to as load compensated OTAs, since the load capacitance determines the gain-bandwidth $\left(g_{m} / C_{L_{\text {eff }}}\right)$.

When the extra flexibility is needed of a dual-stage OTA, the current mirror OTA is preferable to the folded for a number of reasons. For similar sizing, the current mirror OTA provides almost double the DC gain of the folded and the non-dominant pole at the current mirror node of Fig. 4.3 is higher in frequency than at the folded node of Fig. 4.4. It is not recommended, however, using the current mirror OTA for single-ended applications in which a second (PMOS) current mirror is used for the differential to single-ended conversion. This adds an extra pole and feedforward zero to the transfer. A proposal to get around this is presented in section 10.4. For either dual-stage OTA, the designer should use a PMOS input stage with NMOS current mapping. This ensures that the reference voltage can be chosen low which is often desirable in that (a) the non-dominant OTA pole is created at a NMOS current mapping node, and (b) NMOS only switches can be used at all the virtual earth and reference nodes. A final point with respect to high frequency applications is that the Miller capacitance occurring
at the gate-drain overlap in the current mirror OTA ( $C_{g d_{M N 2}}$ ) is only half that of the folded OTA ( $C_{g d_{M N 2}}+C_{g d_{M N 6}}$ ). That this Miller capacitance can become a serious problem will be illustrated in section 4.3.2. The minimum input voltage for the folded-cascode OTA is lower than for the current mirror OTA, which can reach down to ground level.

### 4.1.2 OTA Cascade Stages

The designer may want improvement in DC gain without loss of signal range. The most popular way of achieving this is by adding pre- or post-cascade stages. The main aim of the pre-cascade stage is to provide a " $g_{m}$ boost" either through buffering or a pre-gain. This stage has a low gain and a wide bandwidth. On the other hand, the main aim of the post-cascade stage is to gain up the output signal, while usually providing for extra output signal range. This stage includes a forward coupling capacitance which determines the overall closed-loop bandwidth of the OTA circuit. These pre- and post-cascade stages are flexible enough that they can be applied to all three primary OTA stages. The various forms of both types of stage are presented in the following.

### 4.1.2.1 Pre-buffer Stage

Fig. 4.5(a) shows the pre-buffer stage. Although any combination of NMOS or PMOS transistors can be used for the pre-buffer stage and following differential input, a principal design requirement is to be able to use equal input and output common mode levels. Preferably, a telescopic second stage is employed to avoid the extra power/area/speed overheads of the current mapping OTAs of sections 4.1.1.2 and 4.1.1.3. This limits the design to a PMOS buffer with a


Fig. 4.5 Pre-cascade stages with (a) pre-buffer, and (b) pre-gain stages.

PMOS input differential pair or an NMOS buffer with NMOS differential pair. Of these, the latter is the better choice for a number of reasons. The NMOS buffer stage has less than a $1 / 3$ of the input capacitance of a PMOS stage for the same $g_{m}$, maximizing the speed of the overall OTA. The non-dominant pole at the buffer output is also minimized by following it up with an NMOS telescopic OTA stage.

Consider, a buffered NMOS OTA such as shown in Fig. 4.5(a); the minimum common mode reference level that can be chosen is:

$$
\begin{equation*}
V_{r e f}>2 \cdot V_{T_{n}}+3 \cdot V_{o n_{n}} . \tag{4.7}
\end{equation*}
$$

Furthermore, if a singly cascoded telescopic OTA stage is chosen, as exemplified by Fig. 4.5(a), the minimum output level that can be tolerated is $V_{\text {ref }}-2 \cdot V_{T_{n}}$. Hence, the maximum symmetrical voltage swing with respect to $V_{r e f}$ becomes:

$$
\begin{equation*}
V_{\max }= \pm 2 \cdot V_{T_{n}} . \tag{4.8}
\end{equation*}
$$

Equivalently, for a PMOS buffer with a PMOS differential pair, the maximum signal swing is $\pm 2 \cdot V_{T_{p}}$, whereas the minimum reference level that can be chosen is $V_{r e f}>2 \cdot V_{T_{n}}+2 \cdot V_{o n_{n}}$.

### 4.1.2.2 Pre-gain Stage

This type of stage, illustrated in Fig. 4.5(b), uses a simple pre-amplifier to boost up the signal delivered to the main amplifier (preferably a telescopic OTA stage, as discussed in 4.1.2.1). It also serves to buffer the input. The common gate NMOS load is a more elegant solution than the more traditional NMOS diode load, since it shields the telescopic OTA stage inputs from supply voltage variations. Furthermore, the input stage gain of $\left(g_{m_{N 4}}+g_{n b_{N 4}}\right) /\left(g_{m_{N 6}}+g_{n b_{N 6}}\right)$ can be set quite accurately due to the matching of like transistors. The minimum value for the reference level is $V_{r e f}>V_{T_{n}}+2 \cdot V_{o n_{n}}$. A positive feature of this stage is that there is no requirement to have the output tied to the input like for the pre-buffer stage of Fig. 4.5(a), since the


Fig. 4.6 Folded OTA with Miller coupled output stage.


Fig. 4.7 Equivalent AC model for folded OTA with Miller output stage.
input level of the second stage is set independently by the common-gate bias level $V_{\text {refn }}$ rather than the common-mode reference level $V_{\text {ref }}$ Hence, the signal range can span $V_{T_{n}}+2 \cdot V_{o n_{n}}$ up to $V_{D D}-2 \cdot V_{o n_{p}}$ with $V_{r e f}$ set in between.

### 4.1.2.3 Miller Output Stage

Fig. 4.6 shows an implementation of a folded OTA together with a Miller coupled output stage. A large increase in DC gain is possible, through the multiplication of the gains of the folded stage and Miller stage. A cascoded output common source stage is used. The equivalent AC diagram is in Fig. 4.7. The dominant (open-loop) pole of this OTA - created at the interface of the folded and Miller stages - is given by:

$$
\begin{equation*}
\omega_{P 1} \cong-\frac{1}{r_{o_{\text {mid }}}\left(C_{\text {mid }}+g_{m_{o u t}} \cdot r_{o L} \cdot C_{c}\right)+r_{o_{L}} \cdot C_{L}}, \tag{4.9}
\end{equation*}
$$

where:

$$
\left.\begin{array}{l}
r_{o_{m i d}}=g_{m_{M N 4}} \cdot r_{o_{M N 4}} \cdot r_{o_{M N 2}} \| g_{m_{M P 4}} \cdot r_{o_{M P 4}} \cdot r_{o_{M P 2}} \\
r_{o_{L}}=g_{m_{M N 6}} \cdot r_{o_{M N 6}} \cdot r_{o_{M N 5}} \| g_{m_{M P 11}} \cdot r_{o_{M P 11}} \cdot r_{o_{M P 9}} \\
C_{m i d}=C_{d b_{M N 4}}+C_{g d_{M N 4}}+C_{d b_{M P 4}}+C_{g d_{M P 4}}+C_{g s_{M N 5}}+C_{d b_{M N 7}}+C_{g d_{M N 5}} \cdot\left(1+\frac{g_{m_{M N 5}}}{g_{m_{M N 6}}+g_{m b} b_{M N 6}}\right.
\end{array}\right) .
$$

The first non-dominant pole is created at the output due to the localized closed-loop second gain stage. The equation for this pole can be simply set up with the aid of equation (3.10):

$$
\begin{equation*}
\omega_{P 2} \cong-\frac{g_{m_{\text {out }}}}{C_{L} \cdot\left(1+\frac{C_{\text {mid }}}{C_{c}}\right)+C_{\text {mid }}} . \tag{4.11}
\end{equation*}
$$

Finally a RHP zero, due to the feedforward path in this second stage, is created at:

$$
\begin{equation*}
\omega_{Z} \cong-\frac{1}{C_{c} \cdot\left(\frac{1}{g_{m_{\text {out }}}}-r_{\text {mil }}\right)}, \tag{4.12}
\end{equation*}
$$

where $r_{\text {mil }}$ is the linear "on" resistance of $M_{N_{7}}, r_{o n_{M_{N 7}}}$. By changing the W/L of $M_{N_{7}}$, it is possible to either set $\omega_{Z}$ to zero or, else say, to allow $\omega_{Z}$ cancel $\omega_{P 2}$. Note, the combination of $\omega_{P 1}$ and $\omega_{P 2}$ gives the familiar open loop pole-splitting where, as $C_{c}$ increases from zero, $\omega_{P 1}$ decreases in frequency while, at the same time, $\omega_{P 2}$ increases in frequency.

The inclusion of $r_{o n_{M_{N 7}}}$ avoids the creation of a RHP zero which would deteriorate the phase margin by the same amount as a LHP pole at the same frequency [37], [38]. However, it is difficult to control the exact value of $\omega_{Z}$. Typically, $C_{c}$ is a capacitor created with interconnect which has poor tracking with $r_{o n_{M_{N 7}}}$. In fact, $\omega_{Z}$ can vary by as much as $\pm 20 \%$ across PVT due to the variability of the linear $r_{o n_{M_{N 7}}}$ and the poor tracking with $C_{c}$, even if gate-oxide capacitors are used to create $C_{c}$. Indeed, making $r_{o n_{M_{N 7}}}$ nominally equal to $C_{c}$ (in order to remove the zero altogether) is not a good idea, since the zero can drift into the RHP with variations in PVT and reduce the phase margin of the amplifier considerably.

### 4.1.2.4 Ahuja Output Stage

Although the standard Miller OTA has always been a popular choice for 2-stage cascaded OTAs, the OTA with Ahuja output stage [39] is proving more popular for modern day digital CMOS processes, particularly for low voltage operation [38]. The Ahuja output stage, sometimes called a cascoded Miller stage, is illustrated in Fig. 4.8 in combination with a folded OTA. No linear MOS resistor is needed, instead use is made of the well controlled $g_{m}$ of a common gate MOST in the OTA primary stage. Since the class A output of the OTA primary stage contains both N - and P-cascoding, a choice exists of either using the NMOS (folded node) or PMOS (cascoded DC current source node) for connecting $C_{c}$ to the output. These two cases have been split up into Type I (Fig. 4.8(a)) and Type II(Fig. 4.8(b)), respectively. To simplify the analysis of the folded OTA with Ahuja output stage, an AC equivalent circuit is given in Fig. 4.9.

(a)

(b)

Fig. 4.8 Half Folded OTA with Ahuja output stage showing
(a) Type I, feedforward coupling via folded node, and
(b) Type II, feedforward coupling via cascoded current source node.

The DC gain of the complete OTA is the same as the Miller, namely:

$$
\begin{equation*}
A_{0}=\frac{g_{m_{\text {in }}} \cdot g_{m_{\text {Ncasc }}} \cdot g_{m_{\text {out }}}}{g_{m_{\text {Ncasc }}} \cdot g_{o_{\text {mid }}} \cdot g_{o_{L}}+g_{o_{\text {fold }}} \cdot g_{o_{\text {mid }}} \cdot g_{o_{L}}} \cong \frac{g_{m_{\text {in }}}}{g_{o_{\text {mid }}}} \cdot \frac{g_{m_{\text {out }}}}{g_{o_{L}}} . \tag{4.13}
\end{equation*}
$$

In the Type I Ahuja OTA of Fig. 4.8(a), the AC feedforward path is tapped off the signal carrying half of the primary OTA stage. For the folded OTA, this means connecting $C_{c}$ to the folded node. This is also possible with the other primary OTA stages; for instance in the current mirror OTA of Fig. 4.3, this would mean tapping the drain of $\left(M_{N_{1}}, M_{N_{2}}\right)$. On the other hand, in the Type II Ahuja OTA, the AC feedforward path via $C_{c}$ is tapped off the cascode node of the DC current source of the primary OTA output stage. For the folded OTA with PMOS input differential stage of Fig. 4.8(b), $C_{c}$ is tapped off the P-cascode point between $M_{P_{1}}$ and $M_{P_{3}}$. The Type II Ahuja is the more robust implementation.

Assuming for each MOST $g_{m} \gg g_{o}$, the three main poles of this OTA can be ascertained. Firstly, the dominant pole is just the same as for the Miller (equation (4.9)), which is essentially the Miller gained up $C_{c}$ in combination with the folded OTA output conductance. The first non-dominant pole is created by the $g_{m}$ of the output stage with the effective capacitance it sees, namely:

$$
\begin{equation*}
\omega_{P 2} \cong-\frac{g_{\text {mout }}}{\frac{C_{L} \cdot C_{\text {mid }}}{C_{c}}+C_{\text {mid }}} . \tag{4.14}
\end{equation*}
$$

Note how this pole is slightly higher than the Miller non-dominant pole of (4.10) due to the influence of the current buffer in series with $C_{c}$ in the feedback of the Miller (which is essentially the extra feature of the Ahuja over the standard Miller) - see Fig. 4.9. The feedback factor has been reduced to just $C_{c} / C_{m i d}$. A second non-dominant pole is created in this architecture by the input resistance of the current buffer transistor $\left(1 / g_{m_{\text {casc }}}\right)$ of either $M_{N_{3}}$ of Fig. 4.8(a), or $M_{P_{3}}$ of Fig. 4.8(b)) in combination with the series combination of $C_{c}$ and $C_{L}$, namely:

$$
\begin{equation*}
\omega_{P 3} \cong-\frac{g_{m_{\text {casc }}}}{\frac{C_{c} c_{L}}{C_{c}+C_{L}}} . \tag{4.15}
\end{equation*}
$$

In summary, the Ahuja is a Miller amplifier with some extra advantages gained through implementing the Miller resistance with a current buffer, instead of a MOST operating in its


Fig. 4.9 Equivalent AC model for folded OTA with Ahuja output stage showing addition of current buffer over that of standard Miller.
linear operating region. Complicated control circuitry is avoided, such as may be needed in the standard Miller OTA, to keep the Miller resistance constant under all operating conditions. The Type II Ahuja, in particular, is the more robust design, where $C_{c}$ is attached to a common gate MOST which carries essentially a constant current. This gives a relatively constant $g_{m}$ independent of signal current fluctuations. Furthermore, the Ahuja overcomes the following problems associated with the Miller OTA with active linear MOST resistor: reduced PSRR due to a) $C_{c}$ being directly coupled to the gate of the common source output stage, and b ) the gate of the MOST resistor being directly tied to $V_{D D}$. Lastly, since the linear MOST resistor is non-linear with output voltage fluctuations, it means there is asymmetry between both halves of the differential Miller OTA giving distortion.

Finally, even when the Miller and Ahuja output stages are applied to fully-differential amplifiers, they are still sensitive to noise on the $V_{S S}$ line, with a consequent degradation in PSRR particularly at high frequencies. The PSRR can be improved with extra circuit complexity by converting either the Miller or Ahuja output stage into a differential-pair stage. The conversion of the Ahuja output stage is shown in Fig. 4.10. The transconductance of the output stage is essentially preserved, even with power supply variations. The down side is that another CMFB loop is needed for the output stage, separate from the input stage. Furthermore, since the headroom is reduced by an extra $\pm V_{o n_{n}}$, the NMOS cascodes ( $M_{N_{8}}$ of Fig. 4.8) have been removed, reducing the overall gain.

### 4.2 The Dual-Input Telescopic OTA

The OTA determines to a large extent the overall performance of the SC circuit. Single-stage OTAs are often used in high-frequency SC applications because of their high power efficiency and low noise. The most common form of single-stage OTA is the telescopic OTA which was


Fig. 4.10 OTA with Ahuja output stage which has improved PSRR.
presented in its many forms in section 4.1.1.1. This structure is firstly quickly reviewed in a SC context for reference before the improved dual-input version with improved efficiency is dealt with.

### 4.2.1 The SC Single-Input Telescopic OTA

The most straight forward amplifier technique for SC applications is the single-input telescopic OTA (SITO), which is essentially a differential-pair with a cascoded output stage. An example of a SITO with a PMOS input-stage is illustrated in Fig. 4.11. It is configured as a high-speed double-sampling sample-and-hold which was first introduced in the discussion on $\delta-Q$ SC techniques in Chapter 2. For this discussion, an NMOS input-stage could also be chosen but the advantage of a PMOS input-stage is that it enables the use of a low reference voltage ( $V_{r e f}$ ) and hence the use of NMOS-only switches. Switches with relatively small aspect ratios can be used which results in smaller clock-feedthrough, particularly when low-value signal capacitors are needed.

Since the SITO gives a predominantly first order response, the gain-bandwidth product of the SITO is given by:

$$
\begin{equation*}
G B W_{S I T O}=\frac{g_{m_{p}}}{C_{L_{e f f}}} . \tag{4.16}
\end{equation*}
$$

Here $g_{m_{p}}$ is the transconductance of the input stage and $C_{L_{e f f}}$ is the effective load capacitance after equation (3.7). The second important parameter of the OTA is the open-loop DC gain, $A_{0}$. For the SITO, $A_{0}$ is given by:


Fig. 4.11 Single-input telescopic OTA (SITO) in double-sampling S\&H configuration.

$$
\begin{equation*}
A_{0_{\text {SITO }}}=g_{m_{p}} \cdot\left(r_{o_{p}} \| r_{o_{n}}\right), \tag{4.17}
\end{equation*}
$$

where $r_{o_{p}}$ and $r_{o_{n}}$ are the small-signal output resistances looking back into the PMOS side and NMOS side, respectively. Typically, for a good design, $r_{o_{p}}$ is made approximately equal to $r_{o_{n}}$.

### 4.2.2 SC DITO Architectures

The approach proposed here for improving amplifier bandwidth and gain is a dual-input telescopic OTA (DITO) and is based on a single amplifier topology [P.3]. The DITO is created by the splitting up of the NMOS current source (transistors $M_{N}$ and $M_{N}{ }^{\prime}$ ) of the SITO so that it acts as an NMOS input differential pair. The first variant of DITO - referred to as DITO ${ }_{A}$ shown in Fig. 4.12 in a high-speed $S \& H$ configuration - includes the further addition of a current source which is slotted in below the NMOS differential-pair. For comparison, similar device geometries are assumed as for the SITO of Fig. 4.11. The sample-and-hold feedback capacitors, $C$, are split in 2 between the top and bottom halves of the DITO. The sample-andhold functionality is now mirrored between the top half of the OTA with a PMOS input-stage ( $M_{P}, M_{P}{ }^{\prime}$ ) and the bottom half of the OTA with an NMOS input stage $\left(M_{N}, M_{N}{ }^{\prime}\right)$.

Two further variations of the DITO are illustrated in Fig. 4.13. DITO $_{\mathrm{B}}$ is formed by


Fig. 4.12 Dual-input telescopic $\operatorname{OTA}\left(\mathrm{DITO}_{A}\right)$ in double-sampling $S \& H$ configuration.


Fig. 4.13 Derived forms of the DITO: (a) $\mathrm{DITO}_{B}$, and (b) $\mathrm{DITO}_{C}$.
removing the PMOST and NMOST tail stages and converting it to Class A/B operation. Consequently, a lower supply voltage can be used, while it has the inherent advantage that no separate common-mode feedback (CMFB) loop is necessary. Finally, DITO $_{C}$ uses a single set of capacitors (not split in 2 as for DITOs A and B), and a single reference. The gates of $M_{N}$ and $M_{P}$ are connected together as are the gates of $M_{N}{ }^{\prime}$ and $M_{P}{ }^{\prime}$. This too has the advantages of a low $V_{D D}$ and no separate CMFB being needed. However, its signal range is limited and the references for the P - and N -inputs can't be set independently as for DITOs A and B .

A concern for high frequency differential applications is CMFB, since it is difficult to create differential and common-mode feedback loops which work independently. Differential settling, in particular, can be affected by the settling of the CMFB loop, and the CMFB capacitors create an extra load at the output of the OTA. DITOs B and C, when applied in doublesampling $\delta$ - $Q$ filters, have inherent CMFB, making them particularly suitable for high frequency differential applications.

From a realization point of view, DITO $_{A}$ and DITO $_{\mathrm{B}}$ are more suitable for CMOS processes with no available poly-poly capacitor option [P.3]. Although the capacitors and switches are equally divided between the top and bottom parts of these DITOs, extra routing is necessary to connect up the doubled number of capacitors and switches. When poly-metal (sandwich or filament) capacitors are used to realize the SC circuits, the area occupied by this extra routing is small compared to the area of the poly-metal capacitors themselves and is not considered a big overhead. On the other hand, when a capacitor option is available, DITO $_{C}$ is more suitable for a compact solution [P.6].

### 4.2.3 Design Considerations

A few points can be made about the design of the DITO. The indicated DC tail-current, $I$, is effectively used twice in the DITO, once for the P-input stage and once for the N -input stage. Since the device geometries are the same as those of the SITO of Fig. 4.11, the $G B W$ of the DITO becomes:

$$
\begin{equation*}
G B W_{\text {DITO }}=\frac{g_{m_{n}}+g_{m_{p}}}{C_{L_{\text {eff }}}}, \tag{4.18}
\end{equation*}
$$

where $C_{L_{e f f}}$ is the same defined effective load capacitance as for the SITO. This improvement in $G B W$ of the DITO with respect to the SITO (see (4.16)) can be achieved with no extra current consumption and no extra hardware. Practically, the DITO gives a factor of 2 improvement $\left(g_{m_{p}}=g_{m_{n}}\right)$ in $G B W$ for the same bias current, $I$. Since the addition of the 2 extra transistors can be interpreted in the same way as the doubling of the aspect ratio of the P -input transistors of the SITO amplifier (to maintain equal device current densities, $g_{m_{p}}$ of the SITO should be doubled by doubling the $W / L$ of the P-input stage and doubling the tail current, $I$ ), a power saving of $50 \%$ can be achieved when compared to the SITO under the same load conditions. Furthermore, the slew-rate is double that of the SITO for equal bias current and load conditions, since the DITO can draw or deliver the full bias current, $I$, into the load. This is particularly beneficial in high frequency SC applications, where slew-rate settling time can occupy a large proportion of the total available settling time (section 3.4.3).


Fig. 4.14 Comparison of DITO and SITO open loop frequency transfers for similar device geometries and current consumption.

Another consequence of doubling the input transconductance for the same bias current of the DITO is that the open-loop DC gain is also doubled:

$$
\begin{equation*}
A_{0_{\text {DITO }}}=\left(g_{m_{p}}+g_{m_{n}}\right) \cdot\left(r_{o_{p}} \| r_{o_{n}}\right) . \tag{4.19}
\end{equation*}
$$

A graphical summary of the small signal improvements of the DITO over that of the SITO is presented in Fig. 4.14. Only the open-loop bandwidth ( $\omega_{o l}$ ) of both the SITO and the DITO is the same for similar biasing and device dimensions, where:

$$
\begin{equation*}
\omega_{o l}=\frac{1}{C_{L_{e f f}} \cdot\left(r_{o_{p}} \| r_{o_{n}}\right)} \tag{4.20}
\end{equation*}
$$

### 4.2.4 Amplifier Noise

Firstly, for reference, the noise contribution of the SITO is calculated using the single-ended equivalent noise model of Fig. 4.15(a). The two important noise contributors are from the input transistor $M_{P}$, via RMS noise voltage $v_{n_{p}}$, and the current source transistor $M_{N}$, via RMS noise voltage $v_{n_{n}}$. All other MOSTs either produce common-mode noise (tail-current) or relatively low noise that they can be neglected (cascodes). The total equivalent thermal noise variance referred to the OTA input is given by:

$$
\begin{equation*}
\overline{v_{n_{\text {SITO }}}^{2}}=2 \cdot\left(\frac{g_{m_{p}}^{2} \cdot \overline{v_{n_{p}}^{2}}+g_{m_{n}}^{2} \cdot \overline{v_{n_{n}}^{2}}}{g_{m_{p}}^{2}}\right) \cdot \Delta f, \tag{4.21}
\end{equation*}
$$

where the factor 2 arises from the differential operation of the OTA.
Fig. 4.15(b) shows the equivalent single-ended noise model of the DITO, where again the only noise contributors are transistors $M_{P}$ and $M_{N}$. However, $M_{N}$ now acts as an input transistor in parallel with $M_{P}$ and so the equivalent noise variance at the DITO input is:

$$
\begin{equation*}
\overline{v_{n_{\text {DITO }}}^{2}}=2 \cdot\left(\frac{g_{m_{p}}^{2} \cdot \overline{v_{n_{p}}^{2}}+g_{m_{n}}^{2} \cdot \overline{v_{n_{n}}^{2}}}{\left(g_{m_{p}}+g_{m_{n}}\right)^{2}}\right) \cdot \Delta f . \tag{4.22}
\end{equation*}
$$

Assuming $g_{m_{p}}=g_{m_{n}}$, then the total equivalent input noise variance for both differential OTAs
becomes:

$$
\begin{align*}
& \overline{v_{n_{S I T O}}^{2}}=4 \cdot \overline{v_{n_{p}}^{2}} \cdot \Delta f,  \tag{4.23}\\
& \text { whereas }  \tag{4.24}\\
& \overline{v_{n_{D I T O}}^{2}}=\overline{v_{n_{p}}^{2}} \cdot \Delta f .
\end{align*}
$$

From this it can be concluded that the DITO produces a quarter of the noise power of the SITO, assuming similar load capacitance, transistor geometries, and biasing currents are used.

Heuristically, the DITO can be envisaged as the folding down of the top half of the SITO to the bottom half and vice-versa. The net result is that for each differential output there is a current source of $I / 2$ connected between $V_{D D}$ and the output and another current source of $I / 2$ connected between the output and $V_{S S}$. These current sources do then nothing else except increase the power consumption of the OTA by $50 \%$ and quadruple the noise power produced by the OTA and so they may be discarded.

### 4.2.5 Signal Range

One of the problems often quoted with regard to the SITO is the required shift in commonmode level between input and output. Considering the P-input SITO illustrated in Fig. 4.11, and assuming a single PMOS cascode stage is used, then the output level can't go any higher than the input common-mode level plus $\left|V_{T_{p}}-V_{o n_{p}}\right|$.Hence, for equal input and output common mode levels, the maximum signal range is just $\pm\left|V_{T_{p}}-V_{o n_{p}}\right|$. For a 3.3 V supply and $V_{T_{p}} \approx 0.7 \mathrm{~V}$, this would imply a maximum swing of just $\pm 0.5 \mathrm{~V}$

For $\mathrm{DITO}_{\mathrm{A}}$ on the other hand, the input and output common-mode levels can be made the same $\left(V_{r e f}^{c m}\right.$ $)$ and independent of the input common-mode levels of the P-input and N -input transistor pairs, namely $V_{\text {ref }}^{p}$ and $V_{\text {ref }}^{n}$. With single cascoding, the DITO maximum signal range is:

$$
\begin{equation*}
V_{\text {max }_{\text {DITO }}^{A}}= \pm\left(V_{\text {ref }_{p}}-V_{\text {ref }_{n}}+V_{T_{p}}+V_{T_{n}}-V_{\text {on }_{p}}-V_{\text {on }_{n}}\right) \tag{4.25}
\end{equation*}
$$

The choices of $V_{\text {ref }}$ and $V_{\text {ref }}$ determine the common-mode input levels of the P-input and N input stages, where:

$$
\begin{equation*}
V_{\text {ref }_{n}} \geq V_{T_{n}}+2 \cdot V_{o n_{n}} \quad \text { and } \quad V_{\text {ref }_{p}} \leq V_{D D}-V_{T_{p}}-2 \cdot V_{o n_{p}} \tag{4.26}
\end{equation*}
$$


(a)

(b)

Fig. 4.15 Single-ended equivalent noise models for (a) the SITO, and (b) the DITO.
in order to ensure that the input transistors and the tail-current sources remain in saturation for proper operation. Hence, the maximum signal voltage swing becomes:

$$
\begin{equation*}
V_{\text {max }_{\text {DITO }}^{A}}= \pm\left(V_{D D}-3 \cdot V_{o n_{p}}-3 \cdot V_{o n_{n}}\right) . \tag{4.27}
\end{equation*}
$$

This is the maximum voltage swing that can be processed safely by SC circuits based on DITO $_{A}$. Note that in the Class A/B DITO ${ }_{B}$ variant, the signal range is increased by $2 \cdot V_{\text {on }}$ to $V_{\text {max }_{\text {DITO }}^{B}}= \pm\left(V_{D D}-2 \cdot V_{\text {on }_{p}}-2 \cdot V_{\text {on }_{n}}\right)$. Considering, for instance, the sample-and-hold circuit of Fig. 4.12, the inputs and outputs can be regarded intuitively as being on a sliding potentiometer, sliding up and down between $V_{\text {ref }_{p}}$ and $V_{\text {ref }_{n}}$. Through the use of $V_{\text {ref }}^{p}$ and $V_{r e f_{n}}$ in this way, the complete circuit can be regarded as having one virtual common-mode reference voltage, namely $V_{\text {ref }}^{c m}$. Note that this degree of freedom is removed for DITO ${ }_{C}$ of Fig. 4.13(b), due to the connecting together of the N - and P - inputs. The maximum swing is also reduced to just $\pm\left(V_{T_{p}}+V_{T_{n}}-V_{o n_{p}}-V_{o n_{n}}\right)$.

In general, DITOs A and B are more suitable for video applications because of their larger potential signal handling capabilities and because these filters are often combined with digital signal processing where no poly-poly capacitor option is available to keep the die cost down. DITO $_{C}$ is suitable, for instance, for radio IF processing, where signal handling is lower and where an analogue CMOS process with double-poly option is available.

### 4.3 Cascode Frequency Response Design Issues

The main purpose of cascoding is to increase amplifier gain. The cascode has already been examined extensively in this chapter in its application to the various amplifier architectures. The cost of cascoding is two-fold: 1) the frequency response of the amplifier is degraded and 2) the signal range is reduced [40]. The former is mainly a concern for HF applications. The latter is important for low voltage designs and will be further examined section 4.5.

This section deals with the frequency response of the cascode and, in particular, when it is used in SC amplifier stages. In 4.3.1, an examination is made of the effect of the frequency response of the cascode on the settling response of the SC amplifier stage. The relatively unknown phenomenon of low frequency Miller multiplication will be elucidated in 4.3.2. Neutralization as a way of reducing $C_{g d}$ Miller multiplication will be addressed, finally, in 4.3.3.

### 4.3.1 The Effect of Cascoding on the Closed-Loop Settling Response

For most applications, as described in section 3.2, the SC circuit incorporating the OTA is designed to have a predominantly first order settling response. Two types of SC circuit were distinguished in Chapter 2, namely the $\delta$ - $Q$ and $Q T$ SC circuits. In Fig. 4.16, the settling models for both of these types of SC circuit are illustrated. The feedback capacitor $C_{f b}$ of the standard $Q T$ circuit of Fig. 4.17(a), creates a right half-plane Miller zero at a position of $g_{m} / C_{f b}$. This is normally substantially higher than the $G B W$ so as not to affect the step response of the SC circuit.

To help examine more exactly what cascoding does to the settling response, the model of
(a)

(b)


Fig. 4.16 Settling models for (a) QT, and (b) $\delta$-Q SC circuit for similar external loadings.
the cascoded OTA of Fig. 4.17 is used. The biggest trouble-maker is $C_{c a s}$ which is the total effective capacitance at the cascode node to AC ground. It is approximated by:

$$
\begin{equation*}
C_{c a s}=C_{g s_{c a s}}+C_{d_{i n}}+\left(1+\frac{g_{m}}{g_{m_{c a s}}+g_{m b_{c a s}}}\right) \cdot C_{g d_{i n}} \tag{4.28}
\end{equation*}
$$

where $C_{g s_{c a s}}$ is the gate source capacitance of the cascode MOST, $C_{d_{i n}}$ the diffusion capacitance at the cascode node, and $C_{g d_{i n}}$ the gate drain overlap capacitance of $M_{i n} . C_{c a s}$ is responsible for creating a parasitic pole and zero which slow up the settling response of the SC circuit. Note that the factor $\left(1+g_{m} / g_{m_{\text {cas }}}+g_{m b_{c a s}}\right)$ is a Miller multiplication factor for high frequency operation, where it assumed that the impedance seen at Out is low. This subject will be treated in more detail in sections 4.3.2 and 4.4.2.

The signal transfer of the $Q T$ circuit, including the model for the cascoded OTA, can be found after nodal analysis to be:

$$
\begin{equation*}
\frac{V_{\text {out }}(s)}{V_{\text {in }}(s)}=-\frac{C_{\text {in }}}{C_{f b}} \cdot \frac{1-s \cdot \tau_{\text {mil }(Q T)}-s^{2} \cdot \tau_{\text {mil }(Q T)} \cdot \tau_{c a s}}{1+s \cdot \tau_{1 s t(Q T)}+s^{2} \cdot \tau_{1 s t(Q T)} \cdot \tau_{c a s}}, \tag{4.29}
\end{equation*}
$$

where

$$
\begin{align*}
& \tau_{1 s t(Q T)}=\frac{1}{g_{m}} \cdot\left[\frac{C_{L}}{C_{f b}} \cdot\left(C_{f b}+C_{i n}+C_{i n_{p a r}}\right)+C_{i n}+C_{i n_{p a r}}\right] \\
& \tau_{m i l(Q T)}=\frac{C_{f b}}{g_{m}}, \quad \tau_{c a s}=\frac{C_{c a s}}{g_{m_{c a s}}+g_{m b_{c a s}}} . \tag{4.30}
\end{align*}
$$

Note that the dominant time constant, defined here as $\tau_{1 s t(Q T)}$, can be recognized from (3.10) as the time constant for the first order response. The time constant $\tau_{\operatorname{mil}(Q T)}$ is created by the Miller effect through $C_{f b}$, and finally $\tau_{c a s}$ is created at the cascode node through its capacitance, $C_{\text {cas }}$. Secondary poles due the output resistance $\left(r_{o}\right)$ of the transistors can be ignored, since $1 / g_{m} \ll r_{o}$. For the NMOS cascoded differential pair used in this example, and assuming a simple N-well CMOS process, backgate modulation effectively increases the transconductances of the cascode transistors. The backgate effect of the NMOS cascode can account for a


Fig. 4.17 Simplified model for OTA including cascode;
(a) OTA half circuit, and (b) lumped AC model.
reduction of its input impedance by around $30 \%$.
For comparison, the signal transfer of the $\delta$ - $Q$ circuit of Fig. 4.16(b), after inclusion of the effect of the cascode, is found to be:

$$
\begin{equation*}
\frac{V_{\text {out }}(s)}{V_{\text {in }}(s)}=\frac{1+s \cdot \tau_{\text {mil }(\delta-Q)}+s^{2} \cdot \tau_{\text {mil }}\left(\delta-Q \cdot \tau_{\text {cas }}\right.}{1+s \cdot \tau_{1 s t((\delta-Q)}+s^{2} \cdot \tau_{1 s t( }(\delta-Q)} \cdot \tau_{c a s} . \tag{4.31}
\end{equation*}
$$

Here, $\tau_{c a s}$ is the same as for the $Q T$ case, while:

$$
\begin{align*}
& \tau_{1 s t(\delta-Q)}=\frac{1}{g_{m}} \cdot\left[\frac{C_{L}}{C_{f b}} \cdot\left(C_{f b}+C_{i n_{p a r}}\right)+C_{i n_{p a r}}\right] \\
& \tau_{m i l(\delta-Q)}=\frac{C_{i i_{p a r}}}{g_{m}} . \tag{4.32}
\end{align*}
$$

Two basic differences, assuming equal extrinsic loading, can be observed between equations (4.29) and (4.31) for the influence of the cascode on the closed loop response of $Q T$ and $\delta-Q$ circuits. Firstly, the cascode in combination with the feedback capacitor $C_{f b}$ causes the $Q T$ circuit to have double RHP zeroes which can cause a considerable reduction in phase margin if $C_{c a s}$ is too large. On the other hand, the $\delta-Q$ has double LHP zeroes which don't affect stability. Secondly, the non-dominant Miller pole is at lower frequencies in the $Q T$ circuit $\left(C_{f b} / g_{m}\right)$ compared to the $\delta-Q\left(C_{i n} / g_{m}\right)$. In general, therefore, the cascode degrades the frequency response of the $Q T$ circuit more than it does the $\delta$ - $Q$ circuit.

The principle reason for using a cascode circuit is to increase the output resistance of the OTA, and hence its DC gain. It should be designed according to the criteria presented in section 3.3, i.e. a small $V_{\text {on }}$ voltage (with minimum gate length). The design should be such that it doesn't significantly affect the settling response of the SC filter. $C_{c a s}$ should be as small as possible so as not to degrade the frequency behaviour of the OTA. Since no extra electrical contact needs to be made with the cascode node, the source diffusion of the cascode may exactly overlap the drain diffusion of the MOST being cascoded (for instance, a MOST of the input differential pair) avoiding the use of metal contacts. In this way, the intermediate (at cas-


Fig. 4.18 Low frequency cascode representations: (a) large signal, and (b) small signal.
code node) diffusion capacitance is minimized by minimizing the distance between the gates.
In general, it can be stated that the cascode should be designed such that $\tau_{c a s}<\tau_{\text {mil }}$ and $\tau_{c a s} \ll \tau_{1 s t}$. The $Q T$ circuit has greater difficulty in meeting this requirement due to its inherently larger $\tau_{\text {mil }}$.

### 4.3.2 Low Frequency Miller Multiplication

Referring to Fig. 4.18, the total resistance seen at the cascode node can be found using nodal analysis to be:

$$
\begin{equation*}
R_{c a s}=\frac{1}{\left(1+g_{m_{\text {cas }}}+g_{m b}\right) \cdot \frac{r_{o_{c a s}}}{r_{\text {cas }}+r_{L}}+\frac{1}{r_{o_{\text {oin }}}}} \tag{4.33}
\end{equation*}
$$

(4.33) shows that $R_{\text {cas }}$ is formed by $r_{o_{i n}}$ in parallel with the series combination of $r_{o_{c a s}}$ and $r_{L}$ divided down by the gain of the cascode. The output impedance of the OTA is comprised of $r_{L}$ in parallel with $C_{L_{e f f}}$. For SC circuits, $r_{L}$ just represents the resistance seen at the P-side of the OTA which is very high (and should be nominally equal to the N -side), while $C_{L_{e f f}}$ is the total effective capacitance seen at the OTA output node. At high frequencies, the output impedance is dominated by $C_{L_{\text {eff }}}$ and becomes small. Hence, the impedance seen at the cascode node becomes just $\frac{1}{g_{m_{c a s}}}\left\|\frac{1}{g_{m b c a s}}\right\| r_{o_{c a s}} \| r_{o_{i n}}$, which is approximately just $\frac{1}{g_{m_{c a s}}}$. However, at low frequencies approaching DC, the OTA output impedance is dominated by $r_{L}$ and is very large. This reveals the crux of the problem, since the gain from the input node to the cascode node also increases rapidly towards lower frequencies. In fact, the gain to the cascode node at DC becomes:

$$
\begin{equation*}
A_{0(c a s)}=\frac{V_{c a s}}{V_{i n}} \approx g_{m_{i n}} \cdot r_{o_{i n}}, \tag{4.34}
\end{equation*}
$$

which is the full gain of the input transistor $M_{i n}$. This means that the gate-drain overlap capac-
itance of $M_{i n}$ gets Miller multiplied by $g_{m_{i n}} \cdot r_{o_{i n}}$. For an OTA with NMOS input transistors, the effective $C_{g d_{i n}}$ can increase by 20-30 to become even larger than $C_{g s_{i n}}$.

### 4.3.3 Neutralization

One technique to reduce the effect of low frequency Miller $C_{g d}$ multiplication is neutralization through the use of source and drain tied cross-coupled MOSTs [41], such as shown for a SITO in Fig. 4.19. Each cross-coupled MOST is half the size of each input stage MOST so that its combined $C_{g d}$ and $C_{s d}$ overlap capacitances match $C_{g d_{i n}}$ of an input MOST. The technique depends on the exact differential operation of the circuit, where the parasitic signal dependent current that flows in the Miller multiplied $C_{g d_{i n}}$ is cancelled by an opposite phased parasitic signal dependent current that flows through the capacitor connected from the cascode node to the gate of the opposite input MOST. Note too, that neutralization is also useful for reducing non-linear effects like kick-back (such as in comparators) where switching noise from a subsequent switching stage couples back into the differential pair of the previous stage.

Another example of the application of neutralization is illustrated in Fig. 4.20 for a low voltage Miller OTA. Here, no cascoding is permissible due to limited signal range. Hence, $C_{g d_{i n}}$ of each input MOST is multiplied up by $g_{m} \cdot r_{o}$ for all frequencies. Neutralization has an obvious benefit for this application, since the effective parasitic Miller capacitance at each output of the first stage is reduced from $g_{m} \cdot r_{o} \times C_{g d_{i n}}$ to just approximately $2 \cdot C_{g d_{i n}}$.

The use of neutralization brings with it some disadvantages. It causes an increase in the capacitance at the drains of the input MOSTs. For the examples of the SITO and Miller OTA given, neutralization impacts stability due to the reduction in frequency of the OTA non-dominant pole. The area of the input stage is also almost doubled and the layout more complicated due to the need for interweaving the input stage MOSTs with cross-coupled MOST capacitors for maximum effectiveness.


Fig. 4.19 Neutralization using cross-coupled MOSTs.


Fig. 4.20 Neutralization applied to a low voltage Miller OTA.

### 4.4 Boosting the $\boldsymbol{g}_{\boldsymbol{m}}$ of a Cascode Stage using Active Feedback

Active cascode feedback increases the gain of the cascode by the gain of the feedback amplifier without the need for Miller compensation capacitors for stability. To reduce low frequency Miller multiplication, the dynamic time constant at the drains of the input MOSTs needs to be reduced. One method already explored was that of neutralization in section 4.3 as part of a generalised cascode design strategy. Instead of concentrating on the Miller capacitance, a better design strategy is the boosting of the $g_{m}$ of the cascodes with active feedback. Obviously cascoding must be allowed in the circuit before this technique can be applied. One exception is the low voltage Miller OTA, so that neutralization, for instance, is the best solution here.

Active cascode feedback (in what is termed a regulated cascode, or RGC [42], [43]) is examined in this section with particular emphasis being placed on high frequency performance and its ability to reduce low frequency cascode Miller capacitance multiplication.

### 4.4.1 The RGC with High Frequency Design Considerations

The functional implementation of the RGC is illustrated in Fig. 4.21(a). The simplest embodiment of such a differential RGC is demonstrated in Fig. 4.21(b) using two common source amplifiers.

The differential half circuit of the SITO with active feedback cascode is shown in Fig. 4.22(a) together with the parasitic capacitors. The associated small signal model is given in Fig. 4.22(b) which includes the output resistors of each stage. The dominant poles and zero have been calculated using the small signal model. It is again assumed that for each stage $g_{m} \gg g_{o}$ (normally a factor of about 30), whereas $g_{m_{c a s}}$ is only a few times larger than $g_{m b}{ }_{c a s}$ due to the large body effect of the NMOS cascode. Hence, $g_{m b c a s}$ is included in the calcula-


Fig. 4.21 Differential RGC applied to a SITO (a) and the simplest embodiment of such (b).
tions for the non-dominant poles and zeros. For the calculation of the node resistances and DC gains, $g_{m}$ and $r_{o}$ are used while all capacitances are set to zero.

The resistance seen at the output node is:

$$
\begin{equation*}
R_{\text {out }}=r_{o_{L}} \|\left[r_{o_{\text {in }}}+r_{o_{c a s}}+r_{o_{\text {in }}} \cdot r_{o_{c a s}} \cdot\left(g_{m b_{c a s}}+\left(1+g_{m_{A}} \cdot r_{o_{A}}\right) \cdot g_{m_{c a s}}\right)\right] . \tag{4.35}
\end{equation*}
$$

In what follows, it is assumed that $C_{g d_{c a s}} \ll C_{L}$. The dominant open loop pole frequency is:

$$
\begin{equation*}
\omega_{p_{1}} \cong \frac{1}{R_{\text {out }} \cdot C_{L}} . \tag{4.36}
\end{equation*}
$$

Since the gate of the cascode is no longer at AC ground due to the intervention of the active feedback, an extra pole and LHP zero is introduced by the feedback OTA [46]. The two principal non-dominant poles and non-dominant LHP zero are calculated to be:

$$
\begin{gather*}
\omega_{p_{2}} \cong \frac{g_{m_{A}}}{C_{o_{A}} \cdot\left(1+\frac{g_{m b_{c a s}}}{g_{m_{\text {cas }}}}\right)+C_{g s_{c a s}} \cdot\left(\frac{g_{m_{A}}+g_{m b_{c a s}}}{g_{m_{c a s}}}\right)},  \tag{4.37}\\
\omega_{p_{3}} \cong \frac{g_{m_{A}}+g_{m b_{c a s}}}{C_{o_{A}}+C_{g d_{i n}}+\frac{C_{o_{A} A} \cdot C_{g d_{i n}}}{C_{g s_{c a s}}}+\frac{g_{m_{\text {cas }}}+g_{m b_{c a s}}}{C_{g s_{c a s}}+C_{g d_{i n}}+\frac{C_{g s_{c a s}} C_{g d_{i n}}}{C_{o_{A}}}},}  \tag{4.38}\\
\omega_{z} \cong \frac{g_{m_{A}}}{C_{o_{A}} \cdot\left(1+\frac{g_{m b_{c a s}}}{g m_{\text {cas }}}\right)+C_{g s c a s} \cdot \frac{g_{m b_{c a s}}}{g m_{\text {cas }}}} . \tag{4.39}
\end{gather*}
$$

From the above equations, a high frequency pole-zero doublet is created by the RGC, namely $\omega_{p_{2}}, \omega_{z}$. These frequencies are fairly closely matched and is a characteristic of gain boost amplifiers in general [46]. The second non-dominant pole $\left(\omega_{p_{3}}\right)$ is at least 4 times higher than the pole/zero doublet and can be ignored. If not properly designed, the pole/zero doublet can create a slow settling component in the closed loop settling response of the complete amplifier.


Fig. 4.22 OTA half circuit with RGC (a), and small signal model (b).
The magnitude of this slow settling component relative to the final value of the step response of the complete amplifier is given by [45]:

$$
\begin{equation*}
\left|k_{\text {slow }}\right|=\left|\frac{\omega_{z}-\omega_{p_{2}}}{\omega_{c l} \mid \beta_{f b}}\right|, \tag{4.40}
\end{equation*}
$$

where $\omega_{c l}$ and $\beta_{f b}$ are the closed loop bandwidth and feedback factor of the main amplifier, respectively. For correct settling performance, $k_{\text {slow }}$ should be smaller than the static settling error $\varepsilon_{s}$ (see equation (3.3)). Reducing the dimensions of the RGC amplifier to such an extent that a low frequency pole-zero doublet plays any role in the settling response of the overall amplifier is a poor strategy, since there is only a narrowband of $\left|\omega_{z}-\omega_{p_{2}}\right|$ for which some sort of cancellation of the pole $\omega_{p_{2}}$ occurs to make the amplifier emulate a much faster first order response. Due to a lack of good tracking between $\omega_{z}$ and $\omega_{p_{2}}$, such cancelling can't be guaranteed over PVT.

To ensure that the settling response of the complete amplifier is not affected by the doublet, the time constant of the doublet must be smaller than the time constant of the complete amplifier. Furthermore, for good stability, the frequency of the doublet should be lower than the non-dominant pole of the complete amplifier. These are, generally, easy conditions to meet
in practice, since the load capacitance of the complete amplifier is much larger than that of the RGC allowing small currents and transistor sizes for the RGC compared to the main amplifier itself. The main amplifier can be optimized for maximum $G B W$ practically independent of the active feedback RGC amplifiers. The RGC amplifiers are then designed to provide a large DC gain with the same current densities as in the main amplifier but scaled transistor widths.

In general, it can be stated that the RGC applied to standard OTAs (such as the SITO, or folded cascode) offers a great alternative to the use of cascade gain stages such as discussed in 4.1.2. The benefits are fewer stages, less power, and better stability (and thus higher frequency performance) than OTAs using cascaded stages. They are also a better alternative to double and triple cascodes, since such cascodes demand too much headroom in modern day processes. Low voltage RGC alternatives for high speed will be discussed in 4.5.

### 4.4.2 Reducing Low Frequency Miller Multiplication

The RGC is more than just a gain boost - it boosts the $g_{m}$ of the cascodes by increasing its value by the gain of the active feedback amplifier, which in the case of the of Fig. 4.21(b) is circa $25-30 \mathrm{~dB}$. Hence, the low frequency Miller multiplication of $C_{g d_{i n}}$ is reduced by $25-30 \mathrm{~dB}$. This offers a better alternative to neutralization for high speed applications, since neutralization loads the cascode nodes enormously. As shown by the following equation for the resistance looking into the cascode node, the effective transconductance of the cascode has been increased by a factor of $(1+A)$ due to the active feedback:

$$
\begin{equation*}
R_{c a s}=\frac{1}{\left[1+\left((1+A) \cdot g_{m_{c a s}}+g_{m b c a s}\right) \cdot r_{o c a s}\right] \frac{1}{r_{o_{c a s}}+r_{L}}+\frac{1}{r_{o_{i n}}}} . \tag{4.41}
\end{equation*}
$$



Fig. 4.23 DC gain to the cascode node, $A_{0(\text { cas }}$, as function of effective load impedance, $\left|z_{L}\right|$.

To illustrate the reduction in low frequency Miller multiplication with active cascode feedback, Fig. 4.23 shows a graph of the DC gain to the cascode node $A_{0(c a s)}$ as a function of the effective OTA load impedance $\left|z_{L}\right|$. As discussed in 4.3.2, the standard cascode has the worst performance for increasing output impedance. Here, for small values of $\left|z_{L}\right|, A_{0(\text { cas })}$ converges to approximately -1 , since the effective impedance at the cascode node converges to approximately $\frac{1}{g_{m_{c a s}}} \| \frac{1}{g_{m b_{c a s}}}$.

### 4.5 Low Voltage High Frequency RGC Architectures

This section begins by examining the suitability of RGCs to low voltages. Then the fairly common approach of using level shift buffers is presented together with its performance limitations. Next, two novel approaches are introduced for true low voltage high performance RGCs suitable for high frequency operation (i.e. the RGC is not operating in weak inversion). Note that the low voltage main amplifiers demonstrated in this section have no tail current source so to reduce the minimum $V_{D D}$ by an extra $V_{o n}$.

### 4.5.1 Suitability of RGCs for Low Voltage

RGCs are a good candidate for low voltage applications, as long as the active feedback amplifier can be designed to tolerate low voltages. In comparison to the standard cascode of section 4.3 with fixed biasing, the biasing of the RGC of section 4.4 is self-adaptive depending on the instantaneous current carried by the cascode MOST. For the standard cascode, the minimum output voltage for all MOSTs to remain in saturation is given by:

$$
\begin{equation*}
V_{\text {out }(c a s)} \geq \sqrt{\frac{I_{\text {max }} / 2}{\frac{1}{2} \mu \cdot C_{o x} \frac{W_{\left(M_{\text {in }}\right)}}{L_{\left(M_{i n}\right)}}}}+\sqrt{\frac{I_{\text {max }} / 2}{} \frac{\frac{1}{2} \cdot \mu \cdot C_{o x} \frac{W_{\left(M_{c a s}\right)}}{L_{\left(M_{c a s}\right)}}}{}} . \tag{4.42}
\end{equation*}
$$

On the other hand, the minimum output voltage of the RGC is:

$$
\begin{equation*}
V_{\text {out }(R G C)} \geq \sqrt{\frac{I_{\text {max }} / 2}{\frac{1}{2} \mu \cdot C_{o x} \cdot \frac{W_{\left(M_{\text {in }}\right)}}{L_{\left(M_{\text {in }}\right)}}}}+\sqrt{\frac{I / 2}{\frac{1}{2} \mu \cdot C_{o x} \cdot \frac{W_{\left(M_{\text {cas }}\right)}}{L_{\left(M_{c a s}\right)}}}} . \tag{4.43}
\end{equation*}
$$

Here, $I$ is the OTA tail current, while $I_{\text {max }}$ is the maximum current expected to flow to the output. Considering, for instance, that $I_{\text {max }}$ can be double the value of $I$ during OTA slewing, and assuming similarly sized $M_{\text {in }}$ and $M_{\text {cas }}$, then:

$$
\begin{equation*}
V_{\text {out }(R G C)_{\text {min }}} \cong \frac{3}{4} \cdot V_{\text {out }(\text { cas })_{\text {min }}} . \tag{4.44}
\end{equation*}
$$

### 4.5.2 LV RGC using Level Shift Buffers

The conventional method for creating a LV RGC that avoids the active feedback transistors entering weak inversion is to employ a level shift buffer. This method is illustrated in Fig. 4.24 for a differential main amplifier with NMOS RGCs incorporating PMOS buffers. Looking at


Fig. 4.24 Conventional method to LV RGC employing PMOS level shift buffers.
say the RHS of the amplifier, the minimum output voltage becomes:

$$
\begin{equation*}
V_{o u t_{\text {min }}}=V_{o n_{M_{N 4}}}+\left(V_{g s_{M_{N 6}}}-V_{g s_{M_{P 2}}}\right) . \tag{4.45}
\end{equation*}
$$

For an optimal design in terms of dynamic range, the term in brackets in (4.45) should be made equal to $V_{o n_{M}}$. However, because of varying PVT conditions, this equality cannot be guaranteed and so with $\left(V_{g s_{M_{N 6}}}-V_{g s_{M_{P 2}}}\right)>V_{o n_{M_{N 2}}}$, a safe design margin is to allow $\left(V_{g s_{M_{N 6}}}-V_{g s_{M_{P 2}}}\right)=2 \cdot V_{o n_{M_{N 2}}}$. This method has the advantage that the RGC will remain operational even during slewing of the input differential pair enabling the amplifier to recover quickly from fast transients.

A disadvantage of this method, with the addition of the level shift buffers, is that it increases the current consumption and area of the basic NMOS RGC amplifier by a factor of 45. It is only of real benefit for reducing the operational voltage of NMOS RGCs, since for PMOS RGCs it is difficult to guarantee that $V_{g s_{n}}>V_{g s_{p}}$ under all circumstances. A further disadvantage is that the PMOS buffers significantly reduce the frequency of operation of the complete RGC. The non-dominant pole at the cascode node of the main amplifier is reduced in frequency due to the effective addition of the gate-source capacitance of the PMOS buffer compared to the standard RGC. The gate-source capacitance of this buffer also adds to the feedforward capacitance of the RGC discussed in 4.4.1, reducing the frequency of the LHP zero.

### 4.5.3 LV RGC using Folded Cascode Voltage Sensing

Referring to Fig. 4.25, the main OTA cascode node voltages are now sensed by NMOS transistors $\left(M_{N_{5}}, M_{N_{6}}\right)$ through their sources much like a folded cascode. The necessary phase inversion is obtained through the use of the PMOS current mirrors $\left(M_{P_{1}}, M_{P_{2}}\right)$ and $\left(M_{P_{3}}, M_{P_{4}}\right)$. The voltage at the gates of $\left(M_{N_{5}}, M_{N_{6}}\right)$ are set at a $V_{g s}$ above $V_{o n}+V_{\operatorname{margin}}$ of both $\left(M_{N_{1}}, M_{N_{2}}\right)$. Note that care must be taken under slewing conditions to ensure that the current in the RGC


Fig. 4.25 LV RGC using NMOS source voltage sensing through folding.
doesn't go to zero: this would give rise to hefty settling transients. Hence, transistors $\left(M_{N_{7}}, M_{N_{8}}\right)$ are added which bleed off a small current continuously.

The two main advantages of this technique are: 1) the OTA output voltage can go right down to $2 V_{\text {on }}$ with the LV RGC stage still operational, and 2) the extra capacitance at the folded nodes X and Y is only that of the gate-source capacitances of the NMOS folded cascode - similar to the standard "high-voltage" RGC. The use of the PMOS current mirror in this LV RGC shouldn't impact the stability of the complete OTA too severely, since it only processes small signal current changes. The input transistors $\left(M_{N_{1}}, M_{N_{2}}\right)$ must be designed to accommodate the extra current $I / n$ of the RGC.

### 4.5.4 LV RGC using Dynamic Biasing

A new method is introduced here which enables a high performance low voltage RGC to be created. As demonstrated in Fig. 4.26, the technique makes use of the analogue-sampled-data nature of the application through the use of switched-capacitors to create the level shift. Effectively, a floating battery is created between the cascode points of the main amplifier (namely, the drains of $\left(M_{N_{1}}, M_{N_{2}}\right)$ and the gates of the active feedback transistors $\left(M_{N_{7}}, M_{N_{8}}\right)$. The values of the capacitors $C_{A}$ and $C_{B}$ are not critical in terms of matching so that $C_{A}$ can be chosen to be of the order of 200 fF for an amplifier with $G B W$ of a few hundred MHz . The time constant $C_{A} / C_{B} \cdot f_{c l k}$ may be a few clock cycles long.

There are four key advantages of using this RGC with dynamic biasing. 1) Signal range: $V_{\text {ref }_{1}}$ can be created accurately at a level of $V_{o n_{n}}+V_{\text {margin }}$, while $V_{\text {ref }}^{2}$ is set at $V_{T_{n}}+V_{o n_{n}}$. These voltages can be made to track for different PVT conditions using replica biasing. Hence, with this technique, the OTA of Fig. 4.26 can work comfortably with an output voltage swinging from $2 \cdot V_{o n_{n}}$ and $V_{D D}-2 \cdot V_{o n_{p}}$ while having fully operational P- and N -side RGCs. 2) Robust to slewing: this method is very robust to slewing of the input differential-pair transistors com-


Fig. 4.26 Proposed RGC using switched-capacitor dynamic biasing.
pared to all the other methods presented. Even if one input MOST is off during slew$\operatorname{ing}\left(M_{N_{1}}\right.$ or $\left.M_{N_{2}}\right)$ the RGC remains fully operational with no nasty kick-in effect during the transition from slewing to linear settling. 3) High-speed operation: the NMOS RGC can be built without any recourse to PMOSTs or mirroring. 4) Extra cascoding allowed in the active feedback amplifier without compromising head-room in the main amplifier - this is illustrated with the use of $\left(M_{N_{5}}, M_{N_{6}}\right)$ in Fig. 4.26. A disadvantage of this technique is that capacitance at the cascode nodes of the main amplifier is increased. This is another reason for keeping the values of $C_{A}$ and $C_{B}$ low. Furthermore, there can be an area disadvantage, since the capacitors need to be floating which may imply the use of metal-metal capacitors in standard CMOS processes. However, gate-oxide capacitors can be used to good effect here, since although nonlinear with voltage, they switch between fixed voltages on both sides of the OTA and no mismatch distortion should arise.

### 4.6 OTA DC Gain Improvement using Partial Positive Feedback

It is possible to increase the effective output resistance of an OTA by adding an extrinsic negative resistance at its output [47]. This can be created through partial positive feedback. The effect is to increase gain without the addition of local negative feedback loops such an Miller stages or gain-boost stages. The OTA frequency response doesn't have to be sacrificed for the sake of higher gain so that it is particularly suitable to higher frequency SC applications. The following two subsections present the general design procedure for application in SC circuits as well as an improved CMOS implementation.


Fig. 4.27 AC equivalent of QT SC circuit, including added negative output conductance $g_{o n}$.

### 4.6.1 OTA Design Strategy

The partial positive feedback technique is demonstrated here for a $Q T$ circuit, although the technique is equally valid for a $\delta$ - $Q$ circuit. Conductances are used instead of resistances for ease of analysis. Consider again the $Q T$ of Fig. 4.16(a) with the inherent output conductance, $g_{o p}$, as well as the added negative output conductance, $g_{\text {on }}$. Other secondary effects are left out of the picture for this discussion, e.g. $C_{i n p a r}, R_{f b}$, and the cascodes. The equivalent AC diagram is given in Fig. 4.27. With $\tau$ the settling time constant, $\tau_{\text {mil }}$ the Miller time constant, and $g_{o}=g_{o p}-g_{o n}$, the transfer function after nodal analysis is found to be:

$$
\begin{equation*}
\frac{V_{\text {out }}(s)}{V_{\text {in }}(s)}=-\frac{C_{\text {in }}}{C_{f b}} \cdot \frac{1}{1+\frac{1}{A_{0} \cdot \beta_{f b}}} \cdot \frac{1-s \cdot \tau_{m i l}}{1+s \cdot \tau \cdot \frac{1}{1+\frac{1}{A_{0} \cdot \beta_{f b}}}, ~} \tag{4.46}
\end{equation*}
$$

$$
\begin{equation*}
\beta_{f b}=\frac{C_{f b}}{C_{f b}+C_{i n}} \quad A_{0}=\frac{g_{m}}{g_{o}} \tag{4.47}
\end{equation*}
$$

$$
\text { where } \quad \tau=\frac{1}{g_{m}} \cdot\left(\frac{C_{L}}{\beta_{f b}}+C_{i n}\right) \quad \tau_{m i l}=\frac{C_{f b}}{g_{m}}
$$

Unconditional stability of the closed transfer function of (4.46) is simply guaranteed by:

$$
\begin{equation*}
\left|A_{0} \cdot \beta_{f b}\right| \gg 1 \tag{4.48}
\end{equation*}
$$

In this case, the closed-loop pole is always in the LHP. This holds even if $A_{0}$ is negative! Equation (4.46) can now be approximated by:

$$
\begin{equation*}
\frac{V_{\text {out }}(s)}{V_{i n}(s)} \approx-\frac{C_{i n}}{C_{f b}} \cdot\left(1-\frac{1}{A_{0} \cdot \beta_{f b}}\right) \cdot \frac{1-s \cdot \tau_{m i l}}{1+s \cdot \tau \cdot\left(1-\frac{1}{A_{0} \cdot \beta_{f b}}\right)} . \tag{4.49}
\end{equation*}
$$

If $A_{0} \cdot \beta_{f b}$ is positive ( $g_{o}$ positive), then the pole frequency is increased slightly. Similarly, if $A_{0} \cdot \beta_{f b}$ is negative ( $g_{o}$ negative), the pole frequency is reduced a little. The response remains stable and first order.

It is not only possible to design for a nominal zero static error, $\varepsilon_{s}$, at the end of the settling period through using positive feedback, but the dynamic settling error, $\varepsilon_{d}$, can also be nominally compensated for to create a nominally zero total error. In this case, the OTA is designed such that $\varepsilon_{s} \approx-\varepsilon_{d}$. This means the output resistance is designed to be nominally slightly negative. The total relative settling error $\left(\varepsilon \approx \varepsilon_{s}+\varepsilon_{d}\right)$, including component variations, will just end up being slightly positive or negative depending on the eventual sign of $g_{o}$.


Fig. 4.28 Output resistance cancellation through positive feedback:
(a) Low resistance cancellation, (b) High resistance cancellation.

### 4.6.2 Circuit Implementation of Partial Positive Feedback

The technique is best applied to fully differential OTAs due to the nominally exact impedance balancing of the positive and negative outputs. Direct creation of a negative output resistance is not feasible though, since whenever two transistors outputs are connected in parallel, their (positive) output resistances always add in parallel. Instead, partial positive feedback is created by employing a negative transconductance $\left(-g_{m}\right)$ steered by the negative output voltage in order to cancel the OTA output conductance.

The modified conventional approach [48] to output resistance cancellation through positive feedback is shown in Fig. 4.28(a) [49]. In the absence of the positive feedback MOSTs, denoted $M_{n A}$ and $M_{n B}$, the OTA gain is just that of a single MOST:

$$
\begin{equation*}
A_{0} \approx-\frac{g_{m_{p 2}}}{\frac{g_{m_{n 1} 1} \cdot g_{n 3}}{g_{n 3}}} . \tag{4.50}
\end{equation*}
$$

The addition of $M_{n A}$ and $M_{n B}$ cause a reduction of the effective output conductance and hence an increase in DC gain:

$$
\begin{align*}
A_{0} & =-\frac{g_{m_{p 2}}}{\frac{g_{o_{p} 2} \cdot g_{m_{p} 4}}{g_{o_{p 4}}}+\frac{g_{m_{n 3}}}{g_{o_{n 3}}}\left(g_{m_{n 1}}+g_{o_{n 1}}-g_{m_{n B}}+g_{o_{n B}}\right)} \\
& \approx-\frac{g_{m_{n 3}} \cdot\left(g_{o_{p 2}}+g_{o_{n 1}}+g_{o_{n B}+}+g_{m_{n 1}}-g_{m_{n B}}\right)}{\frac{g_{o_{p 2}}}{g_{n 3}},} \tag{4.51}
\end{align*}
$$

in which it is assumed that the gain of the P- and N-cascodes are the same, i.e. $\frac{g_{o_{p} 4}}{g_{m_{p 4}}} \approx \frac{g_{o_{n 3}}}{g_{m_{n 3}}}$. An important aspect to the implementation of Fig. 4.28(a) is the inclusion of the cascode MOSTs $\left(M_{n 3}, M_{n 4}\right)$ which ensures improved output conductance cancellation over the full output signal range compared to say [48].

Some unfavourable aspects of this particular approach are: 1) since the objective is cancellation of low resistances $\left(1 / g_{m}\right)$, mismatch of $\left(M_{n 1}, M_{n B}\right)$, and $\left(M_{n 4}, M_{n A}\right)$ can reduce the output resistance substantially, 2) substantial extra capacitance at the $M_{n 3}$ cascode node $\approx 2 \cdot\left(C_{g s_{n 1}}+C_{d_{n 1}}\right)$, and 3) the output level can only go down to $V_{T_{n}}+2 \cdot V_{o n_{n}}$.

Consider now the improved partial positive feedback conductance cancellation approach of Fig. 4.28(b). Again a telescopic OTA is used to which a cross-coupled differential pair with sense transistors $\left(M_{p A}, M_{p B}\right)$ is added at the PMOST cascode nodes. The DC gain becomes:

$$
\begin{align*}
A_{0} & =-\frac{g_{m_{p 2}}}{\frac{g_{o_{n 1}} \cdot g_{m_{n 3}}}{g_{o_{n 3}}}+\frac{g_{m_{p 4}}}{g_{o_{p 4}}} \cdot\left(g_{o_{p 2}}+g_{o_{p B}}-g_{m_{p B}}\right)} \\
& \approx-\frac{g_{m_{p 2}}}{\frac{g_{m_{n 3}}}{g_{o_{n 3}}} \cdot\left(g_{o_{p 2}}+g_{o_{n 1}}-g_{m_{p B}}\right)}, \tag{4.52}
\end{align*}
$$

where again the gains of the P - and N -cascodes are the same and $g_{o_{p B}} \ll g_{o_{p 2}}$. The important difference here is the exclusion of the cancellation of a large transconductance (e.g. $g_{m_{n 1}}$ and $g_{m_{n B}}$ of (4.51)). This means a small PMOST, with transconductance $2 / A_{M O S T}$ smaller than the transconductance of the main OTA MOSTs, is sufficient to create the conductance cancellation. Furthermore, no extra parasitic poles are created.

In summary, partial positive feedback for DC gain improvement is particularly attractive for use in SC circuits, especially for application at high frequencies with low power. The key point with regard to the realizations here is that the negative resistance compensation occurs at a cascode node and not at the OTA output like in conventional approaches. The output resistance cancellation techniques can be used without any effect on circuit stability or linearity [50]. A gain increase of at least 12 dB over full signal range and PVT corners is possible with Fig. 4.28(b), which is often sufficient to avoid the use of more power hungry, larger area, and less stable two-stage and gain boost techniques.

### 4.7 Optimization of SC Settling Response with Inclusion of Feedback Loop Switches

Unlike the cascode circuit, the switch is an essential component in a SC circuit. In particular for HF SC circuits with switched feedback capacitor $C_{f b}$ (e.g. in $N$-path filters), the resistance of the feedback switches $R_{f b}$ can significantly influence the settling performance. The noise contribution of $R_{f b}$ is normally much less than the noise contributed by other switches in the SC circuit, since it is heavily filtered by the closed loop transfer function of the OTA. The choice of signal capacitor sizes is determined by noise and matching considerations - see 3.3.2. The feedback switches are preferably designed as small as possible in order to keep their charge feedthrough as small as possible and to keep down their contribution to the parasitic


Fig. 4.29 Settling models for (a) $Q T$, and (b) $\delta-Q$ SC circuits including feedback switch resistance.
capacitance. The minimum size of these switches is set by the maximum acceptable resistance that can be tolerated in the feedback path. The effect of $R_{f b}$ on the settling response, as well as a design strategy which includes $R_{f b}$ in the settling response, are discussed in the following.

### 4.7.1 Effect on Settling of Switch Resistance in OTA Feedback Loop

Consider again the settling models for the $Q T$ and $\delta-Q$ SC circuits shown in Fig. 4.29(a) and (b), respectively, but now with the inclusion of $R_{f b}$. Since the output resistance of the OTA always satisfies $R_{o} \gg\left\{1 / g_{m}, R_{f b}\right\}$, the closed loop transfer function of the $Q T$ circuit, including $R_{f b}$, can be written as:

$$
\begin{equation*}
\left.\frac{V_{\text {out }}(s)}{V_{\text {in }}(s)}\right|_{Q T}=-\frac{C_{i n}}{C_{f b}} \cdot \frac{1+s \cdot C_{f b}\left(R_{f b}-\frac{1}{g_{m}}\right)}{1+s \cdot \tau_{1 s t(Q T)}+s^{2} \cdot\left(C_{i n}+C_{i p_{p a r}}\right) \cdot C_{L} \cdot \frac{R_{f b}}{g_{m}}} . \tag{4.53}
\end{equation*}
$$

Similarly, the transfer function of the $\delta-Q$ circuit can be written as:

$$
\begin{equation*}
\left.\frac{V_{\text {out }}(s)}{V_{\text {in }}(s)}\right|_{\delta-Q}=\frac{1+s \cdot\left(\frac{C_{i p_{p a r}}}{g_{m}}\right)}{1+s \cdot \cdot_{1 s t}(\delta-Q)^{+s^{2} \cdot} \cdot C_{i n_{p a r}} \cdot C_{L} \cdot \frac{R_{f b}}{g_{m}}} . \tag{4.54}
\end{equation*}
$$

The dominant time constants, $\tau_{1 s t(Q T)}$ and $\tau_{1 s t(\delta-Q)}$, were identified in (4.30) and (4.32), respectively. It is evident from these equations that the $\delta-Q$ circuit has higher frequency dominant and non-dominant poles compared to the $Q T$ circuit for the same component values, enabling it to reach its end value quicker. The Miller zero of the $\delta$ - $Q$ circuit is due only to $C_{i n_{p a r}}$, and is independent of the size of the switch resistance. This allows optimization of a second order response, without having to worry about the locus of the Miller zero. On the other hand,
for the $Q T$ circuit, the position of the Miller zero is a more critical issue due to its dependence on $R_{f b}$.

### 4.7.2 Switch Design Strategy for Speed-up

The SC circuit should be designed such that its step response approaches a first order response. The usual approach to sizing the $R_{f b}$ switch is to choose it as small as possible for the sake of low charge feedthrough while not too small that $R_{f b}$ (adversely) affects settling response. In some literature [51], proposals have been made for optimizing the step response in such a way that if the output has to settle to within an error band of $E \cdot(1 \pm \Delta)$ in a single clock period, that the first (and thus maximum) overshoot should just touch off $E \cdot(1+\Delta)$ before settling back to within the error band at the end of the clock period [44]. Although, ideally, this gives the quickest step response, it can't be guaranteed under all signal conditions and for all process corners. Think of varying large signal conditions (with non-linearities caused by varying diffusion capacitors and MOST resistances), process spreads, supply voltage changes and large temperature fluctuations - so designing for such an underdamped response is not a good idea in practice.

The proposal here is to let $R_{f b}$ be designed in to the settling process. This resistor is allowed to perform a double function, namely (a) increasing the frequency of the closed loop dominant pole (while reducing the frequency of the closed loop non-dominant pole), and (b) nominal cancellation of the non-dominant pole (in $Q T$ case).

Starting with the $Q T$ circuit, a value of $R_{f b}<1 / g_{m}$ creates a low frequency RHP Miller zero, degrading the phase margin. This should be avoided, meaning $R_{f b}$ should be chosen larger than $1 / g_{m}$. Equation (4.53) can be solved for $R_{f b}$ such that a LHP zero results which cancels the non-dominant second pole. Two solutions result for $R_{f b}$, namely:

$$
\begin{align*}
& R_{f b_{1(Q T)}} \rightarrow \frac{1}{g_{m}} \cdot \frac{C_{f b}+C_{i n}+C_{i n_{p a r}}}{C_{f b}} \\
& R_{f b_{2(Q T)}} \rightarrow \frac{1}{g_{m}} \cdot \frac{C_{f b}+C_{L}}{C_{f b}} . \tag{4.55}
\end{align*}
$$

Normally, $C_{L}>C_{i n}+C_{i n_{p a r}}$, and so the larger resistance value results from choosing $R_{f b_{2}}$ as the nominal value for $R_{f b}$. Furthermore, the value of $R_{f b}$ to cause breakaway of the poles is found to be:

$$
\begin{equation*}
R_{f b_{b r e a k}(Q T)}=\frac{\left(C_{i n}+C_{i n_{p a r}}+C_{L}+\frac{\left(C_{i n}+C_{i n_{p a r}}\right) \cdot C_{L}}{C_{f b}}\right)^{2}}{4 \cdot g_{m} \cdot\left(C_{i n}+C_{i n_{p a r}}\right) \cdot C_{L}} \tag{4.56}
\end{equation*}
$$

$R_{f b_{b r e a k}(Q T)}$ represents the condition for critical damping, in which case both poles are equal and real. It is recommended to design $R_{f b}<R_{f b_{b r e a k(Q T)}}$ to ensure a stable and fast step response for all process and signal conditions. In other words, avoid designing for a nominally underdamped response. Note that when $R_{f b}=R_{f b_{b r e a k(Q T)}}$ is chosen, the frequency of the dominant pole is increased by $100 \%$ compared to when no resistance exists in the feedback loop.


Fig. 4.30 Root Locus plots of charge transfer (QT) SC circuits for varying feedback switch resistance, $R_{f b}$ - see (4.55), (4.56).


Fig. 4.31 Root Locus plot of $\delta$-Q SC circuits for varying feedback switch resistance, $R_{f b}$.
This means a $100 \%$ increase in settling speed compared to the ideal first order case, sketched in section 3.2.

The movement of the poles and zero as $R_{f b}$ varies from 0 to $R_{f b_{b r e a k}(Q T)}$ is illustrated for the $Q T$ circuit in the root locus plots of Fig. 4.30. For $R_{f b}>1 / g_{m}$, the Miller zero moves to the LHP. Cancellation of the second higher frequency pole occurs for $R_{f b}=\left\{R_{f b_{1}}, R_{f b_{2}}\right\}$. Finally, critical damping is achieved for $R_{f b}=R_{f b_{b r a k}(Q T)}$, after which the poles become complex (shown by the dashed lines).

Considering next the $\delta$ - $Q$ circuit, only one solution exists for the value of $R_{f b}$ for which non-dominant pole zero cancellation occurs, i.e.

$$
\begin{equation*}
R_{f b_{(\delta-Q)}} \rightarrow \frac{1}{g_{m}} \cdot \frac{C_{f b}+C_{i n_{p a r}}}{C_{f b}} \approx \frac{1}{g_{m}} . \tag{4.57}
\end{equation*}
$$

It is clear, therefore, that there is no need for such pole-zero cancellation in $\delta$ - $Q$ circuits, since the LHP zero at radial frequency $-g_{m} / C_{i n_{p a r}}$ is much higher than the first non-dominant pole. The $\delta$ - $Q$ circuit is essentially a closed-loop second order (all-pole) system after inclusion of the effect of $R_{f b}$. Again, to enable a $100 \%$ speed improvement, a value for $R_{f b}$ just under the breakaway value should be chosen, where:

$$
\begin{equation*}
R_{f b_{b r e a k}(\delta-Q)}=\frac{\left(C_{i n_{p a r}}+C_{L}+\frac{C_{i n_{p a r}} \cdot C_{L}}{C_{f b}}\right)^{2}}{4 \cdot g_{m} \cdot C_{i n} \cdot C_{L}} . \tag{4.58}
\end{equation*}
$$

The root locus plot is shown in Fig. 4.31 for the $\delta-Q$ circuit as $R_{f b}$ varies from 0 to $R_{f b_{b r a k}(\delta-Q)}$. The zero position doesn't play a significant role in the $\delta$ - $Q$ circuit, and it can be treated as a second order system for the settling response.

The foregoing discussion will now be illustrated with a design example. Consider equivalent $Q T$ and $\delta-Q$ SC circuits designed to drive the same load, $C_{L}$. The OTA and all external capacitors are assumed to be the same. The difference in design approach between both circuits is that the $Q T$ circuit needs an extra capacitor $C_{\text {in }}$ for operation, while the feedback switch resistor, $R_{f b}$, may be designed to be much larger in the $\delta-Q$ circuit compared to the $Q T$ circuit for the same settling response (due to the much smaller effective capacitance seen by the OTA inputs).


Fig. 4.32 Step response curves of QT SC circuit for various values of $R_{f b}$.


Fig. 4.33 Step responses of $\delta Q$ SC circuit with $R_{f b}$ for equivalent loading to $Q T$ circuit
Taking a specific example with values typical for high frequency applications: the OTA transconductance, $g_{m}$, is $5 \mathrm{~mA} / \mathrm{V}$, while $C_{i n}$ (for $Q T$ only) and $C_{f b}$ are $1 \mathrm{pF}, C_{i n_{p a r}}$ is 0.3 pF and the load $C_{L}$ is 3 pF . Using equation (4.55), the values of $R_{f b}$ for pole zero coincidence in the $Q T$ circuit are $460 \Omega$ and $800 \Omega$, respectively. The value for $R_{f b_{\text {break }(Q T)}}$ is $862 \Omega$ from (4.56). The step response curves can be found in Fig. 4.32 for various values of $R_{f b}$. Note that the $Q T$ circuit inverts the signal at the output. It can be seen that choosing a value of $R_{f b}=R_{f b_{b r e a k(Q T)}}$
doubles the speed of the circuit. Above this resistance value, the circuit step response shows overshoot. For $R_{f b}<1 / g_{m}$, the $Q T$ circuit shows pre-shoot (extra lag) due to the RHP Miller zero - this evident for the $R_{f b}=50 \Omega$ (A) case shown.

Using the same capacitor values as for the $Q T$ circuit, the step response curves for the $\delta-Q$ circuit can be found in Fig. 4.33. Here, there is no signal inversion. The step response is less sensitive to relative variations in the value of $R_{f b}$ than is the $Q T$ circuit. Because of the higher feedback factor, the pole breakaway frequency of -379 MHz for the $\delta-Q$ circuit is about double the -194 MHz of the $Q T$ circuit.

### 4.8 Conclusions

Single-stage amplifiers are especially suitable for use in SC circuits because they are genuinely high-bandwidth load-compensated amplifiers which have predictable settling performance across PVT for very high power efficiency. Unfortunately, their signal range is limited, especially for those applications that require equal input and output common-mode reference levels. For instance, the telescopic OTA can only swing by $\pm\left|V_{T}-V_{\text {on }}\right|$. A suitable single-stage alternative was proposed in this chapter based on the DITO which has dual inputs via complementary PMOS and NMOS differential pairs, high signal range up to $\pm\left(V_{D D}-2 \cdot V_{o n_{p}}-2 \cdot V_{o n_{n}}\right)$ for equal input and output reference levels and yet double the power efficiency of the standard telescopic OTA. It achieves this by exploiting the inherent level shift properties of the switching signal capacitors.

Low voltage design techniques suitable for use with SC circuits have been addressed. Traditional design methods for increasing OTA gain based on double and triple cascoding become unsuitable because of limited signal range, while cascaded amplifiers are difficult to control to get a good step response. RGCs are an attractive alternative for DC gain enhancement, since they can be added to single-stage amplifiers, which with the use of good design practices described in section 4.4 , won't significantly affect settling response. Furthermore, low voltage implementations have been shown to be possible without degrading frequency response.

Finally, design techniques are presented which are particularly suitable for high frequency SC circuits. These are the use of partial positive feedback to improve the DC gain of single-stage OTAs, and the inclusion of the OTA feedback loop switch resistance as part of the overall SC settling response. In each case a strategy is proposed which enables performance improvement without any power dissipation penalty.

## Chapter 5

## Low-Sensitivity SC BPF Concepts

New implementations of SC N -path filters are presented in this chapter. Improved accuracy is achieved through application of two concepts - orthogonal hardware modulation and deltacharge redistribution. Low centre frequency $\left(f_{0}\right)$ and quality factor $(Q)$ sensitivities of the proposed SC $N$-path bandpass filters to component spreads are demonstrated and evaluated.

The SC filters presented here differentiate themselves from BPFs used in bandpass sigma delta modulators in that not just accurate $f_{0}$ but also accurate $Q$ are primary design parameters. For narrowband bandpass sigma delta modulators, the aim is to create a SC resonator with as high a $Q$ as possible without great concern for the accuracy of the $Q$. However, for communications applications requiring an analogue front-end with high selectivity, such as FM, video IF and many digital communications applications in which group delay is important, a tight specification on filter $Q$ is important. Hence, all filters presented in this chapter are judged on the sensitivity, and hence ultimate accuracy, that can be achieved in the presence of known component inaccuracies - predominantly due to amplifier limitations and the effects of loading capacitors.

Initially, the sensitivity of SC filters to component variations is compared to that of CT filters. An analysis is presented to quantify the effect of inaccurate filter coefficients on the accuracy of $Q$ and $f_{0}$ in SC BPFs. Next, orthogonal hardware modulation is presented as a means for avoiding in-band artefacts in SC $N$-path filters. The chapter continues by introducing delta-charge redistribution in the context of SC integrators and a comparison is made with traditional charge transfer equivalents. A state-of-the-art SC biquad BPF is presented and analyzed as an application example of charge transfer techniques. It provides a reference for comparison against SC $N$-path equivalents. Finally, three SC $N$-path BPFs are proposed in which delta-charge redistribution is applied in different ways to create the same bandpass filter function. Their relative performances are analyzed and conclusions drawn for implementation.

### 5.1 Sensitivity comparison of SC and CT Filters

The purpose of this section is to do a high level review and comparison of the performance
sensitivity of SC filters and CT RC filters (or equally Gm-C filters [52]) to component inaccuracies. This sets the scene for introducing SC filters for high-accuracy integrated filter realizations, especially BPFs. The two main differences between SC and CT filters are in the requirements of the amplifiers (generally OTAs in both cases) and the means of creating the filters time constants. Typical examples of an RC filter stage and a SC filter stage are shown in Fig. 5.6 as part of a later discussion.

The effect of limited amplifier DC gain is the same for both CT and SC filters. Essentially, the integrator poles are shifted slightly away from DC ( $s=0$ in the $s$-domain or $z=1$ in the $z$-domain), to a frequency of approximately $G B W / A_{0}$. On the other hand, the requirements on amplifier bandwidth are generally much less in SC filters than in CT filters. Since the SC integrator stage (Fig. 5.6(b)) is created using a "fixed delay" by virtue of its sampled data operation, limited amplifier bandwidth mainly gives rise to a gain error in a SC integrator, where:

$$
\begin{equation*}
H(z) \approx\left(1-e^{-t / \tau}\right) \cdot H_{\text {ideal }}(z), \quad z \rightarrow e^{j \cdot \frac{2 \pi f}{f_{s}}} . \tag{5.1}
\end{equation*}
$$

The way the centre frequency $f_{0}$ shifts as a result of limited amplifier bandwidth is demonstrated in Fig. 5.1. In a filter system (e.g. biquad SC BPF) with fixed $G B W$ amplifiers, as the sampling frequency $f_{s}$ (and hence $f_{0}$ ) increases, the centre frequency error $\left(\Delta f_{0}\right)$ rises initially very slowly according to (5.1) but eventually an inflexion point is reached when the amplifier starts to slew and the $\Delta f_{0} / f_{0}$ will deviate off significantly. By contrast, the dominant RC time constant of a continuous-time (CT) integrator (Fig. 5.6(a)) is a first order design parameter which is used for the creation of filter poles in, for instance, a biquad BPF built of such integrators. As $f_{0}$ increases, the error in $f_{0}$ increases in a predominantly linear manner, since the phase shift in each amplifier increases linearly with frequency and this error adds directly to the designed phase shift in the damped integrators within the CT RC BPF. Note a detailed analysis is provided later in this chapter for the sensitivity of SC BPFs to limited DC gain and GBW.

Other points to note: the $R \times C$ time constant within an RC BPF cannot be guaranteed to the same accuracy as the SC time constant - of the form $C_{1} /\left(C_{2} \cdot f_{s}\right)$ created through matched capacitor ratios - due to inevitable process spreads and temperature dependence; indeed the


Fig. 5.1 Comparison of $B P F f_{0}$ sensitivity to amplifier GBW for
(a) continuous-time and (b) switched-capacitor implementations.
" $R$ " itself is generally non-linear, whereas SC time constants can be made signal level insensitive; RC filter stages are resistively loaded which affects the filter frequency characteristic and overall stability, whereas there is only capacitive loading in SC filters giving rise to clean, stable and relatively process insensitive step responses in going from stage to stage. The amplifiers in RC filters (typically OTAs) may never slew, otherwise severe harmonic distortion results. This generally keeps the maximum operating frequency of the RC filter well below the $G B W$ of the amplifiers and also implies that it can handle only small signals (much smaller than power supply) which in turn affects the achievable SNR. SC filters, of course, suffer from charge feedthrough and clock feedthrough effects, full $k T / C$ noise, as well as aliasing, especially in $N$-path realizations [P.4]. The $N$-path filter approach is popular for accurate realizations of SC BPFs but judicious design is required, and this is the focus of the following sections.

### 5.2 BPF Function Including Hardware Imperfections

Although $f_{0}=f_{s} / 4$ is arbitrarily chosen for this discussion, it is a popular choice of centre frequency for bandpass filters, since it is half way along the usable baseband frequency range of 0 to $f_{s} / 2$. This results in the simplest pre-filtering. Furthermore, simple accurate multiplier coefficients can be used (i.e. $0,-1,+1$ ) for shifting signals down to 0 Hz , or indeed from around 0 Hz up to around $f_{s} / 4$, which is handy in communications transceivers.

The ideal BPF $z$-domain transfer function, with guaranteed centre frequency of $f_{s} / 4$, centre frequency gain $G$ and pole radius $r$ (determines $Q$ ) and assuming one clock delay transfer, is given by:

$$
\begin{equation*}
H_{b p f}(z)=G \cdot \frac{z^{-1}}{1-r^{2} \cdot z^{-2}} . \tag{5.2}
\end{equation*}
$$

In the presence of hardware imperfections, to be expected in the actual SC embodiment of the BPF, the transfer gets modified to become:

$$
\begin{equation*}
H_{b p f}(z)=G \cdot\left(1-\varepsilon_{G}\right) \cdot \frac{z^{-1}}{1-2 \cdot \varepsilon_{1} \cdot z^{-1}+\left(1-\varepsilon_{2}\right)^{2} \cdot r^{2} \cdot z^{-2}} \tag{5.3}
\end{equation*}
$$

A single delay $\left(z^{-1}\right)$ error path is created feeding the output back to the input with value $2 \varepsilon_{1}$, while the pole radius (and hence $Q$ ) gets modified by an error term $\varepsilon_{2}$, and the gain is in error by $\varepsilon_{G}$. The errors result in displacement of the poles in the $z$-domain, such as depicted in Fig. 5.2. The complex conjugate poles, including the relatively small errors $\varepsilon_{1}, \varepsilon_{2}$, are derived as:

$$
\begin{align*}
z_{p_{1}, p_{2}} & =\varepsilon_{1} \pm \frac{1}{2} \cdot \sqrt{\varepsilon_{1}^{2}-4 \cdot r^{2} \cdot\left(1-\varepsilon_{2}\right)^{2}} \\
& \approx \varepsilon_{1} \pm j \cdot r \cdot\left(1-\varepsilon_{2}\right) . \tag{5.4}
\end{align*}
$$

The radial deviation $\theta$ from the ideal pole position $\pi / 2$, as shown in Fig. 5.2, is obtained as:

$$
\begin{align*}
\theta & =\tan ^{-1}(x / y) \\
& \approx \tan ^{-1} \frac{\varepsilon_{1}}{r \cdot\left(1-\varepsilon_{2}\right)} . \tag{5.5}
\end{align*}
$$



Fig. 5.2 Representation of second order BPF in the z-plane which has both amplitude and phase inaccuracies.

Since $\theta$ is relatively small in an $N$-path filter realization, the following approximation can be made:

$$
\begin{equation*}
\theta \approx \frac{\varepsilon_{1}}{r} . \tag{5.6}
\end{equation*}
$$

This translates into a relative centre frequency shift of:

$$
\begin{align*}
\frac{\Delta f_{0}}{f_{0}} & =\frac{\theta}{\pi / 2} \\
& \approx \frac{2 \cdot \varepsilon_{1}}{r \cdot \pi} \tag{5.7}
\end{align*}
$$

In order to calculate the quality factor $Q$ of the BPF in the $z$-domain, the $s$-domain representation of a BPF with complex-conjugate poles is first invoked. The $s$-domain pole positions, assuming correct $f_{0}$ and $Q$, are given by [25]:

$$
\begin{equation*}
s_{p_{1}, p_{2}}=-\frac{\pi \cdot f_{0}}{Q} \pm j \cdot 2 \cdot \pi \cdot f_{0} \cdot \sqrt{1-\frac{1}{4 \cdot Q^{2}}} . \tag{5.8}
\end{equation*}
$$

The equivalent $z$-domain pole positions are obtained as:

$$
\begin{align*}
z_{p_{1}, p_{2}} & =e^{-\frac{\pi \cdot f_{0}}{Q \cdot f_{s}}} \cdot e^{ \pm j \cdot \frac{2 \cdot \pi \cdot f_{0}}{f_{s}}} \cdot \sqrt{1-\frac{1}{4 \cdot Q^{2}}} \\
& =z_{\text {radius }} \cdot e^{ \pm j \cdot z_{\text {angle }}} \tag{5.9}
\end{align*}
$$

In the non-ideal case, the radius and angle frequency are given by:

$$
\begin{equation*}
z_{\text {radius }}=\left(1-\varepsilon_{2}\right) \cdot r \text { and } z_{\text {angle }}=\frac{\pi}{2}-\theta . \tag{5.10}
\end{equation*}
$$

From (5.9) and (5.10), the $Q$ factor can be resolved as:

$$
\begin{equation*}
Q=\frac{\sqrt{\left(\frac{\pi}{2}-\frac{\varepsilon_{1}}{r}\right)^{2}+\left(\ln \left[\left(1-\varepsilon_{2}\right) \cdot r\right]\right)^{2}}}{2 \cdot \ln \left[\left(1-\varepsilon_{2}\right) \cdot r\right]} . \tag{5.11}
\end{equation*}
$$

For moderate to high $Q$ filters $(r>0.9), \ln (r)^{2} \ll\left(\frac{\pi}{2}\right)^{2}$ so that $Q$ is predominantly determined by $r$ and $\varepsilon_{2}$. Hence, the following approximation can be made:

$$
\begin{equation*}
Q \approx \frac{\pi}{4 \mid \ln \left[\left(1-\varepsilon_{2}\right) \cdot r\right]} . \tag{5.12}
\end{equation*}
$$

Note that the ideal value of $Q$ depends on $r$ only, where:

$$
\begin{equation*}
Q_{(\text {ideal })} \approx \frac{\pi}{4 \mid \ln [r]]} . \tag{5.13}
\end{equation*}
$$

Hence, the relative variation in $Q$ can be obtained as follows:

$$
\begin{align*}
\frac{\Delta Q}{Q} & =\frac{Q-Q_{\text {(ideal) }}}{Q_{(\text {ideal })}} \\
& \approx \frac{1}{1+\frac{1-r}{\varepsilon_{2} \cdot r}} . \tag{5.14}
\end{align*}
$$

Based on the above analysis, we now have a means for evaluating the effect of circuit non-idealities (due to amplifiers and parasitic capacitors) on the transfer of the SC bandpass filters. The non-ideality factors $\varepsilon_{1}, \varepsilon_{2}$ can be evaluated per SC circuit realization and the resultant relative centre frequency and $Q$ shifts derived.

### 5.3 SC BPF Based on Modified $N$-Path Design Technique

SC $N$-path design, together with associated artefacts, are first examined in this section. Next, the concept of orthogonal hardware modulation, in the context of modified SC N -path filters, is explored as a means to reducing the effects of such artefacts.

### 5.3.1 High- Q BPF Construction

The power of using analogue sampled data (ASD) techniques is that highly accurate circuits can be realized based on relative accuracy on-chip (through capacitor ratios in SC circuits), and on absolute accuracy off-chip (clock frequency). Moreover, the clock can be used to determine an accurate positioning of the filter characteristic in the frequency domain. Consider, for instance, the classic $N$-path technique [53], [54]: through $N$-path hardware modulation of a filter function $F(z)$, the Nyquist bandwidth is increased $N$ times and a new filter function $F\left(z^{N}\right)$ arises. In this way, it is possible to transform a sampled lowpass filter (with poles centred around DC), or a sampled highpass filter (with poles centred around half its sample frequency), to a BPF. In Fig. 5.3, for example, the Nyquist bandwidth of the single-pole highpass filter is expanded 3 times through hardware modulation, to create a $3^{\text {rd }}$ order $N$-path filter with a bandpass response centred at $f_{s} / 6$. An $N$-path BPF can be realized in which the centre frequency $f_{0}$ is directly determined by the sample clock frequency (with frequency $f_{s}$ ) through $f_{s}=f_{0} \times 2 \cdot N$. An error in the coefficient value that determines the position of the pole only affects the bandwidth of the eventual BPF. Note that in classic $N$-path filters, the filter order is given by $N$ times the filter order of a single path.


Fig. 5.3 Known solution for accurate $f_{0}$ : the $N$-path technique.
(a) $1^{s t}$-order HPF, (b) $3^{r d}$-order 3-path BPF.

### 5.3.2 N-Path Design Issues

The two major problems in realizing the classic $N$-path filter using ASD techniques are pattern noise (modulation of DC ) and in-band aliasing (modulation of the signal), both of which are due to expected component mismatch between the $N$ paths. Path mismatch results in $f_{s} / N$ subsampling. For $N$-path BPFs based on a lowpass prototype, upsampled DC components appear at $f_{s} / N, 2 f_{s} / N, \ldots$, producing pattern noise within the passband. To avoid this, $N$-path BPFs based on a highpass filter prototype are preferred, e.g. Fig. 5.3. However, these filters suffer from in-band aliasing due to path mismatch, since the edge of the subsampling Nyquist bandwidth (e.g. $f_{s} / 6$ in Fig. 5.3) falls within the passband. This effect is visualized in Fig. 5.4(a) and (b). Consider an input signal spectrum, such as shown in Fig. 5.4(a), in which a small band of bandwidth $B$ centred at $f_{0}$ has to be filtered. When this spectrum is filtered by a classic 3-path BPF based on a highpass filter prototype $\left(f_{s}=6 f_{0}\right)$, path mismatch causes frequency components at $f_{0}+\delta F$ to fold back in attenuated form to $f_{0}-\delta F$, and vice versa. For $\delta F<B / 2$, in-band aliasing occurs. No pre- or post-filtering can alleviate this process. In theory, a symmetrical signal spectrum, such as in FM radio applications, would not be degraded by this symmetrical in-band aliasing. In practice, however, the centre of the FM IF band is never located at exactly the BPF centre frequency $f_{0}$ due to inaccuracies in the RF mixing and / or inaccuracy in the frequency arising from the clock frequency synthesizer. The FM signal becomes distorted due to the cross-modulation of Bessel components. Judicious system level design can help alleviate the effects of $N$-path mismatch, such as discussed next.


Fig. 5.4 Aliasing due to path mismatch in N-path filters: (a) Filter input spectrum, including band of interest B; (b) In-band aliasing in classic $N$-path filter ( $N=n$ ); (c) Out-of-band aliasing after decoupling number of paths $N$ from filter order $n(N>n)$.

### 5.3.3 Modified $\boldsymbol{N}$-Path Technique using Orthogonal Hardware Modulation

The solution is to introduce a design method, using orthogonal hardware modulation, which ensures that the consequences of hardware imperfections (giving rise to path mismatch) can be treated independently of the signal processing [P.6]. This is carried out in this design by introducing an extra degree of freedom, where the number of hardware paths $N$ (hardware modulation) is decoupled from the functional modulation factor $n$, as introduced by the transformation $z \rightarrow z^{n}$.

This design method is shown conceptually in Fig. 5.5 for two consecutive sample clock phases of a single path of a 5-path second order filter. Five pieces of similar hardware (5-path)

$N$ paths
(here: $N=5$ )

Fig. 5.5 Illustration of orthogonalization in an $N$-path filter.
are set out vertically - these can be, for instance, five sets of switched capacitors, each with three separate functions, namely sampling, charge redistribution and idling. The function rotation of each piece of hardware is set out horizontally in time, from one sample instant to the next. The functional modulation $n$ is determined by the delay between sampling and charge redistribution (here $n=2$ ). Every period $T_{\mathrm{s}}$, a new sample is taken and processed. For instance, at time $t=0$, hardware piece " 1 " samples the input; at $t=T_{s}$, " 5 " samples the input; at $t=2 \times T_{s}$, "4" samples the input, etc. After $5 T_{s}$, the whole process starts again. In this case, the hardware modulation is given by $N=5$.

The basis cell per path is normally a simple first or second order filter. For instance, a first order highpass filter cell is modulated to an $n^{\text {th }}$ order $N$-path filter, where $n$ just gives the number of resonance peaks contained in the Nyquist bandwidth of the $N$-path filter. Knowing $f_{0}$ and $n$, the sampling frequency $f_{s}$ is chosen as:

$$
\begin{equation*}
f_{s}=f_{0} \times 2 n \tag{5.15}
\end{equation*}
$$

Next, $N$ is chosen such that in the event of path mismatch (a) no sub-harmonics of the clock at integer multiples of $f_{s} / N$ (which are caused by the unwanted upsampling of DC components) appear within the frequency band of interest, (b) no aliasing from inside the band can occur back into the band (due to the unwanted subsampling of the signal with $f_{s} / N$ ) and (c) those frequency components from outside the filter band that are capable of folding back into the band can be attenuated in advance with the simplest pre-filter. Referring to Fig. 5.4(c), in order to satisfy points (a) and (b), $N$ must be chosen such that any subsampling Nyquist edge frequency (per path) doesn't fall within the BPF passband, i.e.

$$
\begin{equation*}
i \times \frac{f_{s}}{2 N} \notin\left[f_{0}-\frac{B}{2}, f_{0}+\frac{B}{2}\right], \quad i=0,1,2, \ldots \tag{5.16}
\end{equation*}
$$

Furthermore, to satisfy point (c) for ease of pre-filtering, $N$ should be chosen such that $f_{0}$ fits approximately half way in between two consecutive subsampling Nyquist edge frequencies, i.e.

$$
\begin{equation*}
N=\lfloor 1.5 \times n\rfloor \tag{5.17}
\end{equation*}
$$

For example, a $2^{\text {nd }}$ order BPF (poles at $\pm f_{s} / 4$ ), should have $N=3$; whereas, say, a $5^{\text {th }}$ order BPF (poles at $\pm f_{s} / 10, \pm 3 f_{s} / 10$ ) should have $N=7$. Note that for certain applications, the choice of $N$ may be ultimately determined by the need to avoid certain critical out-of band frequencies from folding back in band; for a radio application, this could be a nearby channel which is known to be very strong with respect to the wanted channel.

### 5.4 Delta Charge Redistribution ( $\delta \mathbf{- Q R}$ )

The concept of delta-charge redistribution in SC circuits was introduced in Chapter 2 and is a central theme in this thesis. Its application in SC filter design is described in this section. Some basic filter examples based on damped integrators are used for comparison to standard approaches.

### 5.4.1 $\delta$ - QR For Filter Design

A standard circuit solution for SC filter implementation, derived from the CT RC equivalent of Fig. 5.6(a), is based on the charge transfer ( $Q T$ ) stage drawn in Fig. 5.6(b) [25]. Here $C_{i n}$ samples the input voltage on one clock phase and has its charge transferred to integrator capacitor $C_{f b}$ on the following clock phase via the virtual earth node of the amplifier. The amplifier in the $Q T$ stage has the dual function of providing (a) charge transport via its virtual earth node (active charge redistribution) and (b) buffering so as to allow the following stage to read the output voltage without affecting the charge on the capacitors. Finite amplifier DC gain and bandwidth cause incomplete charge redistribution due to incomplete charge transfer in one clock cycle. $C_{\text {out }}$ is added to demonstrate how some delayed version of the output voltage, i.e. $V_{\text {out }}{ }^{\prime}$, can be fed back into the filter stage via a $Q T$ path for the creation of more complex recursive filter functions. Two (damped) SC stages similar to the one shown in Fig. 5.6(b), placed in series within a closed loop, form the basis of the SC biquad filter [55], much in use even for high frequency BPFs and examined in detail in section 5.5.1.

Instead of using the $Q T$ circuit, a more efficient circuit implementation is based on deltacharge redistribution $(\delta-Q R)$, illustrated in Fig. 5.6(c) [P.3], [P.6]. Here $C_{a}$ is used to both sample the input voltage and damp the integrator capacitor $C_{b}$. There is passive redistribution of charge between $C_{a}$ and $C_{b}$ by connecting them in parallel, which is unaffected by amplifier errors. In fact, the principal purpose of the amplifier is buffering only. Only the parasitic capacitances must be charged up from one clock cycle to the next - hence the term deltacharge redistribution. The circuit technique of Fig. 5.6(c) allows $N$-path with orthogonal hardware modulation, and delta-charge redistribution to be combined in one single stage, as presented in section 5.5. It is also possible to include a gain control function by adding extra capacitors at the input which regulate the amount of signal charge transferred to $C_{a}$ and $C_{b}$ in parallel. There is only a single transfer of charge from input to output, enabling high settling accuracy. Before proceeding with a comparison between different $Q T$ and $\delta-Q R$ high- $Q$ SC BPFs, it is helpful to examine the performance of a fundamental block in filter design - the (damped) integrator.


Fig. 5.6 (a) Active RC equivalent of SC damped integrator;
Comparison of (b) charge transfer ( $Q T$ ) and (c) delta-charge-redistribution ( $\delta Q R$ ) SC damped integrators as basis for a SC BPF.

### 5.4.2 $\delta$ - QR vs. QT SC Integrators

The QT SC integrator of Fig. 5.6(b) represents a considerable improvement in accuracy in comparison with the RC integrator of Fig. 5.6(a) when integrated on silicon. The RC damped integrator has a -3 dB frequency $1 /\left(2 \pi R_{f b} C\right)$ which is dependent on the matching of dissimilar components so that it is difficult to achieve accuracy of greater than 5-10\%. Even the DC gain, given by $-R_{i n} / R_{f b}$, can vary by the order of $1-2 \%$ due to the high spreads and temperature dependency of integrated diffusion type resistors. The $Q T$ integrator has a -3 dB frequency and DC gain that is dependent on the matching of similar components - capacitors - and hence can achieve accuracies of the order of $0.5 \%$ with metal-metal capacitors. It too has errors that arise from the non-idealities of the amplifier, mainly due to limited DC gain and bandwidth. This will be quickly evaluated for the $Q T$ integrator and then for the $\delta$ - $Q R$ integrator of Fig. 5.6(c).

Note, in the analysis here, only the damped integrator form of circuits Fig. 5.6(b),(c) will be used. As such, in the $Q T$ integrator, the feedback path via $C_{\text {out }}$ will be ignored, while in the $\delta-Q R$, it is assumed that $C_{b}$ only connects to $+V_{\text {out }}$. These results will be used as a basis for evaluating the more complex SC BPFs which follow in section 5.5.

The transfer function of the $Q T$ damped integrator including the effects of limited amplifier DC gain can be derived in the $z$-domain as:

$$
\begin{equation*}
H_{Q T_{\text {gainerr }}}(z)=\frac{V_{\text {out }}(z)}{V_{\text {in }}(z)}=\frac{C_{\text {in }}}{C_{f b}+C_{d}} \cdot \frac{1}{1+\frac{1}{A_{0} \cdot \beta}} \cdot \frac{z^{-1}}{1-z^{-1} \cdot \frac{C_{f b} \cdot}{C_{f b}+C_{d}} \cdot \frac{1+\frac{1}{A_{0}}}{1+\frac{1}{A_{0} \cdot \beta}}} . \tag{5.18}
\end{equation*}
$$

The amplifier DC gain is $A_{0}$ and the feedback factor is $\beta$, given by:

$$
\begin{equation*}
\beta=\frac{C_{f b}+C_{d}}{C_{f b}+C_{d}+C_{i n}+C_{p_{i}}} . \tag{5.19}
\end{equation*}
$$

$C_{p_{i}}$ is the effective parasitic capacitance that appears at the amplifier input node. The gain and phase errors are obtained from (5.18) as:

$$
\begin{equation*}
\varepsilon_{G_{Q T(\text { gainer })}} \approx \frac{1}{A_{0} \cdot \beta} ; \quad \varepsilon_{\mathrm{P}_{Q T(\text { gainer })}} \approx \frac{1-\beta}{A_{0} \cdot \beta} . \tag{5.20}
\end{equation*}
$$

The $Q T$ transfer function, including the effect of limited amplifier bandwidth, can be derived in the $z$-domain to be:

$$
\begin{equation*}
\left.H_{Q T_{B W e r r}}(z)=\frac{C_{i n}}{C_{f b}+C_{d}} \cdot\left(1-\Delta \cdot \frac{C_{f b}+C_{d}+C_{L_{f x}}+C_{L_{s w}}}{C_{L_{e f f}}}\right) \cdot \frac{z^{-\frac{1}{2}}}{1-z^{-1} \cdot \frac{C_{f b}}{C_{f b}+C_{d}} \cdot\left(1-\Delta \cdot \frac{C_{L_{f x}}}{C_{L_{e f f}}} \cdot\left(\frac{C_{L_{s w}}}{C_{L_{f i x}}}-\frac{C_{d}}{C_{f b}}\right)\right.}\right), \tag{5.21}
\end{equation*}
$$

where $\Delta$ is the linear settling error term of the form $\Delta=e^{-\frac{T}{2 \cdot \tau}}$, assuming single-sampling with settling in a half clock period ( $T / 2$ ). Note the load capacitance has been split into a "fixed" term $C_{L_{f i x}}$, which includes all permanently connected parasitic capacitance at the amplifier output node, and a "switching" term $C_{L_{s w}}$, which includes all the active signal switching capacitance at the output. The effective load capacitance $C_{L_{\text {eff }}}$ follows the definition of Chapter 3 . The gain and phase error terms are obtained as:

$$
\begin{equation*}
\varepsilon_{G_{Q T(B W e r r)}} \approx \Delta \cdot \frac{C_{f b}+C_{d}+C_{L_{f i x}}+C_{L_{s w}}}{C_{L_{e f f}}} ; \quad \quad \varepsilon_{\left.\mathrm{P}_{Q T(B W e r r)}\right)} \approx \Delta \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}} \cdot\left(\frac{C_{L_{s w}}}{C_{L_{f i x}}}-\frac{C_{d}}{C_{f b}}\right) . \tag{5.22}
\end{equation*}
$$

For lightly damped integrators, such as found in medium to high $Q$ filters, $\varepsilon_{P} \ll \varepsilon_{G}$ and the only main concern is a gain error. A key point to note in the $Q T$ (damped) integrator transfer function is that the gain at DC is nominally equal to $C_{i n} / C_{f b}$ which, although more accurate than the RC integrator, is still dependent on the ratio of capacitors. The damped $Q T$ integrator is used as the basis for the SC biquad, explored in section 5.5.1.

Turning now to the $\delta-Q R$ damped integrator, the transfer function including the effects of limited amplifier DC gain can be derived as:

$$
\begin{equation*}
H_{\delta Q R_{\text {gainerr }}}(z)=\frac{V_{\text {out }}(z)}{V_{\text {in }}(z)}=\frac{C_{a}}{C_{a}+C_{b}} \cdot \frac{1}{1+\frac{1}{A_{0} \cdot \beta}} \cdot \frac{z^{-1}}{1-z^{-1} \cdot \frac{C_{b}}{C_{a}+C_{b}} \cdot \frac{C_{b}}{1+\frac{1}{A_{0}} \cdot \frac{C_{b}+C_{p_{i}}}{1+\frac{1}{A_{0} \cdot \beta}}} . . . . ~} . \tag{5.23}
\end{equation*}
$$

The gain and phase errors, resulting from amplifier limited gain, are obtained as:

$$
\begin{equation*}
\varepsilon_{G_{\delta-Q R(\text { gainerr })}} \approx \frac{1}{A_{0} \cdot \beta} ; \quad \quad \varepsilon_{\mathrm{P}_{\delta-Q R(\text { gainerr })}} \approx \frac{1}{A_{0}} \cdot\left(\frac{1-\beta}{\beta}-\frac{C_{p_{i}}}{C_{b}}\right) \approx 0 . \tag{5.24}
\end{equation*}
$$

The feedback factor for the $\delta-Q R$ is higher than the $Q T$ equivalent ( $>2 / 3$ for narrowband filters), since there is no signal capacitance connected at its input, i.e.

$$
\begin{equation*}
\beta=\frac{C_{a}+C_{b}}{C_{a}+C_{b}+C_{p_{i}}} . \tag{5.25}
\end{equation*}
$$

Hence, the gain and phase errors in the $\delta-Q R$ damped integrator are smaller than in the $Q T$ equivalent. Finally, the $\delta-Q R$ transfer function including the effects of limited amplifier bandwidth is:

$$
\begin{equation*}
H_{\delta Q R_{B W e r r}}(z)=\frac{C_{a}}{C_{a}+C_{b}} \cdot\left(1-\Delta \cdot \frac{C_{L_{f i x}}+C_{L_{s w}}}{C_{L_{e f f}}}\right) \cdot \frac{z^{-\frac{1}{2}}}{1-z^{-1} \cdot \frac{c_{b}}{C_{a}+C_{b}}\left(1-4 \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}}\left(\frac{c_{L_{s w}}}{C_{L_{f i x}}}-\frac{C_{a}}{C_{b}}\right)\right)} . \tag{5.26}
\end{equation*}
$$

The resulting gain and phase errors are:

$$
\begin{equation*}
\varepsilon_{G_{\delta-Q R(B W e r r)}} \approx \Delta \cdot \frac{C_{L_{f i x}}+C_{L_{s w}}}{C_{L_{e f f}}} ; \quad \varepsilon_{\left.\mathrm{P}_{\delta-Q R(B W e r r)}\right)} \approx \Delta \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}} \cdot\left(\frac{C_{L_{s w}}}{C_{L_{f i x}}}-\frac{C_{a}}{C_{b}}\right) . \tag{5.27}
\end{equation*}
$$

Although (5.27) looks not too dissimilar to (5.22), $\varepsilon_{G}$ and $\varepsilon_{P}$ are in fact smaller in the $\delta$ - $Q R$ integrator compared to the $Q T$ integrator for similar capacitor sizings $C_{a} \approx C_{d}$ and $C_{b} \approx C_{f b}$. This is because $\Delta$ is a lot less (exponentially) by virtue of the fact that $C_{L_{e f f}}$ is smaller for similar filter bandwidth and similar external loadings. Furthermore, the $Q T$ integrator is mostly used in filters such as the biquad, where the output voltage is fed back and summed with the input via a capacitor such as $C_{\text {out }}$ in Fig. 5.6(b). For example, for medium to high $Q$ filters, $\beta_{Q T}<\frac{1}{2} \cdot \beta_{\delta-Q R}$ translates to $\Delta_{\delta-Q R}<7 \cdot \Delta_{Q T}$.

The key point for the $\delta-Q R$ integrator is that the accuracy with which the transfer at DC (or within the passband of filters based on this block) can be realized is independent of capacitor ratios. A change in bandwidth, through a change in capacitor ratio, will have no effect on the transfer gain. The $\delta-Q R$ integrator requires just 2 capacitors for realization, while the $Q T$ integrator requires 3 capacitors to create the same, albeit less accurate, transfer. Finally, the $\delta-Q R$ integrator is substantially less sensitive to amplifier gain and bandwidth. The passband accuracy, together with reduced sensitivity to amplifier limitations, will be further exploited in the $\delta-Q R$ BPFs presented in section 5.5.

## 5.5 $\delta Q R N$-path SC BPFs

In this section, a state-of-the-art SC biquad is first analysed as an example of a $Q T$ SC BPF. Its limitations are evaluated in order to highlight the improved accuracy which can be achieved with the $\delta$ - QR $N$-path SC BPFs analysed thereafter. Three different types of $\delta$ - $Q R N$-path SC BPFs are presented and compared in performance. All the $N$-path BPFs presented here follow the guidelines for high performance SC design detailed in section 1.4.


Fig. 5.7 Biquad SC BPF suitable for high-speed, high-Q applications.

### 5.5.1 QT SC BPF Via State-Of-The-Art Biquad

A new general methodology is presented for a thorough analysis of the SC biquad which is intuitive clear and accurate. It includes the gain and phase errors introduced due to the non-idealities of the amplifiers and presence of parasitic capacitors. It is applicable to both single-sampling and double-sampling implementations.

SC biquads are essentially derived from their erstwhile RC biquad equivalents [56]. They are traditionally used for telecom type low frequency applications. Here, a state-of-theart SC biquad is presented which is suitable for high frequency, high- $Q$ BPFs - see Fig. 5.7. Note, a distinction is made in the literature between low- $Q$ biquads with large capacitor spreads and high- $Q$ biquads with low capacitor spreads. In the architecture presented here, a $Q$ of $10(30)$ can be realized with a maximum capacitor spread of $13(40)$. For good settling performance, the amplifiers have decoupled inputs and the capacitive loading is well balanced and equally distributed between both amplifiers.

Firstly, the ideal transfer of Fig. 5.7 is derived in the $z$-domain. The classic capacitor notations of the Fleischer $F$-type biquad are used [57]. Applying the charge conservation equation,

$$
\begin{equation*}
\sum_{\text {node } i} \Delta Q=0, \tag{5.28}
\end{equation*}
$$

at each amplifier virtual ground node, two simultaneous equations result containing $V_{\text {out }}$ and $V_{i n}$ :

$$
\begin{align*}
& C_{B} \cdot\left(V_{\text {out }}(z)-V_{\text {out }}(z) \cdot z^{-1}\right)+C_{F} \cdot\left(V_{\text {out }}(z) \cdot z^{-1}\right)-C_{A} \cdot\left(V_{1}(z) \cdot z^{-1}\right)=0  \tag{5.29}\\
& \text { and } C_{D} \cdot\left(V_{1}(z)-V_{1}(z) \cdot z^{-1}\right)-C_{H} \cdot V_{\text {in }}(z) \cdot z^{-1}+C_{C} \cdot V_{\text {out }}(z) \cdot z^{-1}=0 . \tag{5.30}
\end{align*}
$$



Fig. 5.8 Signal Flow representation of SC biquad including amplifier non-idealities.

These two equations are solved to obtain the biquad transfer function:

$$
\begin{equation*}
H_{\text {biq }(\text { ideal })}(z)=\frac{V_{\text {out }}(z)}{V_{\text {in }}(z)}=\frac{C_{A} \cdot C_{H}}{C_{B} \cdot C_{D}} \cdot \frac{z^{-1}}{1+z^{-1} \cdot\left(\frac{C_{F}-2}{C B}\right)+z^{-2} \cdot\left(1+\frac{C_{A} \cdot C_{C}}{C_{B} \cdot C_{D}} \frac{C_{F}}{C B}\right)} . \tag{5.31}
\end{equation*}
$$

Each of the centre frequency $f_{0}$ (via $C_{F}$ ), $Q$ (via $C_{C}$ ) and gain (via $C_{H}$ ) can be easily and independently tuned using capacitor ratios in this type of filter. For instance, putting $C_{F}=C_{B}$ places $f_{0}$ at $f_{s} / 4$. This tunability can also be its Achilles' heel in that it is quite sensitive to capacitor mismatch. Especially those applications requiring a tight $f_{0}$ and steady gain may not be realizable with the SC biquad, in spite of its superior accuracy over RC biquad equivalents.

At the heart of the SC biquad are the two $Q T$ SC filter stages, of the type analyzed in section 5.4.2 [55]. Each such $Q T$ stage has a gain error $\varepsilon_{G}$ and phase error $\varepsilon_{P}$, resulting from the limited DC gain and bandwidth of each amplifier. The proposed signal flow representation to aid analysis of the SC biquad is shown in Fig. 5.8. The non-ideal SC biquad transfer function, including the gain and phase errors in both amplifiers X and Y , can be derived from Fig. 5.8 to be:

$$
\begin{align*}
H_{b i q}(z) & =\frac{C_{A} \cdot C_{H}}{C_{B} \cdot C_{D}} \cdot\left(1-\varepsilon_{G_{X}}\right) \cdot\left(1-\varepsilon_{G_{Y}}\right) \times  \tag{5.32}\\
& \frac{z^{-1}}{1+z^{-1} \cdot\left(\frac{C_{F}}{C_{B}} \cdot\left(1-\varepsilon_{G_{Y}}\right)-\left(2-\varepsilon_{P_{X}}-\varepsilon_{P_{Y}}\right)\right)+z^{-2} \cdot\left(\left(1-\varepsilon_{P_{X}}-\varepsilon_{P_{Y}}\right)+\frac{C_{A} \cdot C_{C}}{C_{B} \cdot C_{D}} \cdot\left(1-\varepsilon_{G_{X}}-\varepsilon_{G_{Y}}\right)-\frac{C_{F}}{C_{B}} \cdot\left(1-\varepsilon_{G_{Y}}-\varepsilon_{P_{Y}}\right)\right)} .
\end{align*}
$$

Equation (5.31) is presented in the form which allows direct calculation of the $f_{0}$ and $Q$ deviations. Since the SC biquad analysed here is single-sampling, the configuration of each amplifier $(\mathrm{X}, \mathrm{Y})$ for each of clock phases clk1 and clk2 is different. As such, the feedback factors are different per amplifier per clock phase:

$$
\begin{array}{ll}
\beta_{X(c l k 1)}=\frac{C_{D}}{C_{D}+C_{p_{i} X}+C_{C}+C_{H}} & \beta_{X(c l k 2)}=\frac{C_{D}}{C_{D}+C_{p_{i X}}} \\
\beta_{Y(c l k 1)}=\frac{C_{B}}{C_{B}+C_{p_{i Y}}+C_{A}+C_{F}} & \beta_{Y(c l k 2)}=\frac{C_{B}}{C_{B}+C_{p_{i Y}}} \tag{5.33}
\end{array}
$$

The gain and phase errors need to be evaluated per amplifier and include the contributions on clk1 and clk2. Note that, in this analysis, each amplifier stage of the SC biquad reads in on clk1


Fig. 5.9 Effect of limited amplifier DC gain on SC biquad transfers with $C_{b}=C_{d}=1 \mathrm{pF}, C_{f}=2 \mathrm{pF}$ and $C_{h}=0.5 \mathrm{pF}$.
and reads out on clk2 but the analysis is equally valid for reading in on clk1 and reading out on clk2. Take, for instance, amplifier X:

$$
\begin{align*}
& \varepsilon_{G_{X}} \approx \varepsilon_{G_{X}(c l k 1)}+\varepsilon_{G_{X}(c l k 2)} \\
& \varepsilon_{P_{X}} \approx \varepsilon_{P_{X}(c l k 1)}+\varepsilon_{P_{X}(c l k 2)} \tag{5.34}
\end{align*}
$$

and similarly in the case of amplifier Y with $\varepsilon_{G_{Y}}, \varepsilon_{P_{Y}}$.
Firstly, the effect of amplifier DC gain (assumed to be $A_{0}$ for each amplifier for convenience) on the SC biquad transfer function is evaluated with the help of (5.20) to be:

$$
\begin{align*}
& \varepsilon_{G_{X}} \approx \frac{1}{A_{0}} \cdot\left(\frac{1}{\beta_{X(c l k 1)}}+\frac{1}{\beta_{X(c k 2)}}\right) \\
& \varepsilon_{P_{X}} \approx \varepsilon_{G_{X}}-\frac{2}{A_{0}} \tag{5.35}
\end{align*}
$$

and similarly for $\varepsilon_{G_{Y}}, \varepsilon_{P_{Y}}$ with $\beta_{Y(c l k 1)}$ and $\beta_{Y(c l k 2)}$. Secondly, the effect of limited amplifier bandwidth can be evaluated with the help of (5.22), making use of the result found for the single $Q T$ stage. For amplifier X :

$$
\begin{equation*}
\varepsilon_{G_{X}}=\Delta_{X(c l k 1)} \cdot \frac{C_{D}+C_{L_{f i x}}}{C_{\text {Leff }}(c k 1)}+\Delta_{X(c l k 2)} \cdot \frac{C_{D}+C_{A}+C_{L_{f i x}}}{C_{L e f f X}(c k 2)}, \tag{5.36}
\end{equation*}
$$

where the effective load capacitance for amplifier X per clock phase is:

$$
\begin{align*}
& C_{L_{\text {eff }}^{X(c k 1)}} \\
\text { and } & \left.C_{L_{L_{f i x X}}}+\beta_{X(c l k 2)}=C_{A}+C_{L_{f i x X}}+\beta_{X(c l k 2)} \cdot C_{p_{i X}}+C_{C}+C_{H}\right) \tag{5.37}
\end{align*}
$$

Similarly, for amplifier Y:

$$
\begin{equation*}
\varepsilon_{G_{Y}}=\Delta_{Y(c l k 1)} \cdot \frac{C_{B}+C_{L_{f i x}}}{C_{L_{\text {eff }}(c l k 1)}}+\Delta_{Y(c l k 2)} \cdot \frac{C_{B}+C_{C}+C_{F}+C_{L_{f x_{Y}}}}{C_{L e f f Y(c l k 2)}} . \tag{5.38}
\end{equation*}
$$



Fig. 5.10 SC biquad relative $f_{0}$ and $Q$ deviations from nominal as a function of amplifiers DC gain.
where the effective load capacitance for amplifier Y per clock phase is:

$$
\begin{array}{ll} 
& C_{L e f f_{Y(c l k 1)}}=C_{L_{f i x Y}}+\beta_{Y(c l k 11)} \cdot\left(C_{p_{i Y}}+C_{A}+C_{F}\right) \\
\text { and } & C_{L e f f_{Y(c l k 2)}}=C_{C}+C_{F}+C_{L_{f i x Y}}+\beta_{Y(c l k 2)} \cdot C_{p_{i Y}} . \tag{5.39}
\end{array}
$$

Note, the linear settling error $\Delta$ (related to the settling time constant $\tau$ ) must also be calculated per amplifier per phase. For example, for amplifier X:

$$
\begin{array}{ll}
\Delta_{X(c l k 1)}=e^{-\frac{T}{2 \cdot \tau_{X(c l k 1)}}} \text { where } \tau_{\mathrm{X}(\mathrm{clk} 1)}=\frac{1}{\beta_{X(c l k 1)}} \cdot \frac{C_{L_{\text {eff }}(c \mathrm{clk} 1)}}{g_{m X}} \\
\text { and } \quad \Delta_{X(c l k 2)}=e^{-\frac{T}{2 \cdot \tau_{X(c l k 2)}}} \quad \text { where } \tau_{X(\mathrm{clk} 2)}=\frac{1}{\beta_{X(c l k 2)}} \cdot \frac{C_{\text {Leff }}((c k 2)}{}  \tag{5.40}\\
g_{m X}
\end{array}
$$

and similarly for amplifier Y on clk1 and clk2. The calculations for $\varepsilon_{P_{X}}$ and $\varepsilon_{P_{Y}}$ can be derived in a similar straight-forward manner as for $\varepsilon_{G_{X}}$ and $\varepsilon_{G_{Y}}$.

The non-ideal SC biquad transfer function (5.31) is now compared to the generalized $z$ -


Fig. 5.11 Effect of limited GBW on SC biquad transfers with $C_{b}=C_{d}=1 \mathrm{pF}, C_{f}=2 \mathrm{pF}$ and $C_{h}=0.5 \mathrm{pF}:(a) G B W_{Y}=G B W_{X}$, and (b) $G B W_{Y}=2 \times G B W_{X}$.
domain bandpass filter transfer function (5.3), which includes errors due to gain (via $\varepsilon_{G}$ ), nonideal centre frequency (via $\varepsilon_{1}$ ) and $Q$ (via $\varepsilon_{2}$ ). The error terms are obtained as:

$$
\begin{gather*}
\varepsilon_{G}=\left(1-\varepsilon_{G_{X}}\right) \cdot\left(1-\varepsilon_{G_{Y}}\right)  \tag{5.41}\\
\varepsilon_{1}=\frac{r \cdot \pi}{2} \cdot\left(\frac{C_{F}}{C_{B}} \cdot\left(1-\varepsilon_{G_{Y}}\right)-\left(2-\varepsilon_{P_{X}}-\varepsilon_{P_{Y}}\right)\right)  \tag{5.42}\\
\varepsilon_{2}=1-\frac{1}{r} \cdot \sqrt{\left(1-\varepsilon_{P_{X}}-\varepsilon_{P_{Y}}\right)+\frac{C_{A} \cdot C_{C}}{C_{B} \cdot C_{D}} \cdot\left(1-\varepsilon_{G_{X}}-\varepsilon_{G_{Y}}\right)-\frac{C_{F}}{C_{B}} \cdot\left(1-\varepsilon_{G_{Y}}-\varepsilon_{P_{X}}\right)} . \tag{5.43}
\end{gather*}
$$

The required value of $r$ (and hence $Q$ via (5.13)) is derived from (5.31) as:

$$
\begin{equation*}
r=\sqrt{1+\frac{C_{A} \cdot C_{C}}{C_{B} \cdot C_{D}}-\frac{C_{F}}{C B}} . \tag{5.44}
\end{equation*}
$$

All that is required now is to plug in values for $\varepsilon_{G_{X}}, \varepsilon_{G_{Y}}, \varepsilon_{P_{X}}, \varepsilon_{P_{Y}}$ (using either (5.35) for DC gain error, or (5.36) for bandwidth error) in order to obtain the final values of $\varepsilon_{G}, \varepsilon_{1}$ and $\varepsilon_{2}$.

The theory presented here has been confirmed to be correct using SpecteRF. Some plots of SC biquad transfers are shown in Fig. 5.9 and Fig. 5.11 for various amplifier errors. The nominal centre frequency $f_{0}$ is 10 MHz in all cases and $f_{0}$ is set at $f_{s} / 4$ through making $C_{f}=2 \cdot C_{b}$. The integrator capacitors $C_{b}$ and $C_{d}$ are 1 pF . The $Q$ is set by the integrator coupling capacitors $C_{a}$ and $C_{c}$, which couple the output of one integrator to the input of the next. The gain at $f_{0}$ is then set independently by $C_{h}$.

The transfer sensitivity to DC gain is clear from Fig. 5.9. The relative changes in $f_{0}$ and $Q$ away from their nominal values are depicted in Fig. 5.10(a) and (b), respectively. Although nominally $f_{0}$ doesn't depend on $C_{c}$ (see e.g. (5.31)), it can be seen from Fig. 5.10(a) that there is a secondary sensitivity to $C_{c}$ due to the effect it has on the gain and phase errors of mainly amplifier X. A centre frequency accuracy of better than $0.5 \%$ is difficult to guarantee for high $Q$ biquad filters. From Fig. 5.10(b), it can be seen that the $Q$ deviates strongly from its nominal value as the $Q$ value itself increases. For instance, when the biquad is designed for a $Q$ of 20, a DC gain of 60 dB only guarantees a $Q$ accuracy of $9 \%$.

The sensitivity to limited $G B W$ is highlighted in Fig. 5.11. The biquad is designed optimally when the $G B W$ of amplifier $\mathrm{Y}\left(G B W_{Y}\right)$ is set at twice the $G B W$ of amplifier $\mathrm{X}\left(G B W_{X}\right)$, due to amplifier X having twice the effective load capacitance. Two scenarios are depicted. In Fig. 5.11(a), choosing $G B W_{Y}=G B W_{X}$ makes the $Q$ and, in particular the $f_{0}$, have a strong dependency on $G B W$. On the other hand, in Fig. 5.11(b), $G B W_{Y}=2 \cdot G B W_{X}$ and the transfer sensitivity to $G B W$ is seen mostly in the $Q$ and is aligned to the transfer sensitivity to DC gain. The reduced sensitivity of $f_{0}$, in particular, to amplifier settling accuracy is confirmed with the curves of Fig. 5.12(a), while the $Q$ sensitivity to settling accuracy is depicted in Fig. 5.12(b).

The popular SC biquad, while very versatile in terms of its programmability, is not always suitable for high accuracy applications, particularly those requiring tight centre frequency and $Q$ specifications. Furthermore, they are power hungry, requiring 2 heavily loaded amplifiers, and are less suitable for high frequency applications then the $N$-path type BPF to be presented next.

### 5.5.2 Hybrid $N$-Path SC BPF $(Q T / \delta-Q R)$

The first SC $N$-path BPF presented here is derived from the $Q T$ charge re-circulation principle proposed in the patent [P.21] and used in a resonator type BPF in [58]. It represents the most advanced and accurate implementation based on $Q T$ techniques but combined with $\delta-Q R$ (hence $Q T / \delta-Q R$ hybrid). The $Q T / \delta-Q R$ operates with a 3 phase clock, clk1-3 and is fully differential.

The charge transfer occurs with the capacitor pairs $C_{b_{p}}, C_{b_{n}}$ in this concept. At the end of one clock phase, a set of amplifier feedback capacitors, say $C_{b_{p 1}}, C_{b_{n 1}}$, contains the latest sample of the differential output voltage. Two clock periods later, capacitors $C_{b_{p 1}}, C_{b_{n 1}}$ are discharged between ground and the opposite amplifier virtual ground inputs. In so doing, the charge previously held on $C_{b_{p 1}}, C_{b_{n 1}}$ is inverted and transferred via the amplifier virtual earth input nodes to the next set of feedback capacitors $C_{b_{n 3}}, C_{b_{p 3}}$. This creates the two clock inverting delay $\left(-z^{-2}\right)$ required by the recursive BPF and which forms the basis of the inverting neg-


Fig. 5.12 $S C$ biquad relative $f_{0}$ and $Q$ deviations from nominal as a function of the number of settling time constants with $G B W_{Y}=2 \times G B W_{X}$.
ative delay patented in 1992 [P.21]. The capacitor pairs $C_{a_{p}}, C_{a_{n}}$ are used in the same way as for all the $\delta$ - $Q R$ filters, in that they are used for both sampling the differential input voltage on one clock period and for damping on the following clock period through charge recombination in the amplifier feedback loop with $C_{b_{p}}, C_{b_{n}}$.

The equivalent amplifier loading diagram for each clock phase is shown in Fig. 5.14, without the input parasitic of $C_{p_{i}}$, fixed output parasitic $C_{L_{f i x}}$ and equivalent external switching capacitance $C_{L_{s w}}$. The transfer function of the $Q T / \delta-Q R$ BPF can be reduced to the familiar form of equation (5.3), with $G=C_{a} /\left(C_{a}+C_{b}\right)$ and $r=\sqrt{C_{b} /\left(C_{a}+C_{b}\right)}$ :

$$
\begin{equation*}
H_{Q T / \delta-Q R}(z)=\frac{V_{\text {out }}(z)}{V_{\text {in }}(z)}=\frac{C_{a}}{C_{a}+C_{b}} \cdot\left(1-\varepsilon_{G}\right) \cdot \frac{z^{-1}}{1-2 \cdot \varepsilon_{1} \cdot z^{-1}+\left(1-\varepsilon_{2}\right)^{2} \cdot \frac{C_{b}}{C_{a}+C_{b}} \cdot z^{-2}} . \tag{5.45}
\end{equation*}
$$

The gain error term $\varepsilon_{G}$, centre frequency error term $\varepsilon_{1}$, and $Q$ error term $\varepsilon_{2}$ can be individually obtained for the cases of limited amplifier DC gain and limited amplifier bandwidth.

Consider first the effect of DC gain $A_{0}$ on the BPF transfer. Applying charge conserva-


Fig. 5.13 $Q T / \delta$-QR SC BPF based on combination of charge-transfer and charge-recombination.
tion, $\sum \Delta Q=0$, at the amplifier input nodes, and then applying the $z$-transform, gives:

$$
\begin{align*}
& C_{P_{i}} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}\right)-\left(-\frac{V_{\text {out }}}{A_{0}} \cdot z^{-1}\right)\right) \\
+ & C_{b} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}\right)-\left(\frac{V_{\text {out }}}{A_{0}} \cdot z^{-2}-\left(-V_{\text {out }} \cdot z^{-2}\right)\right)\right) \\
+ & C_{b} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)-\left(\frac{V_{\text {out }}}{A_{0}} \cdot z^{-2}\right)\right) \\
+ & C_{a} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)-\left(-V_{\text {in }} \cdot z^{-1}\right)\right)=0 . \tag{5.46}
\end{align*}
$$

Solving (5.46), the transfer can be reduced to the form of (5.45) with the following error factors:


Fig. 5.14 Equivalent schematic of $Q T / \delta-Q R B P F$ showing capacitive loading per clock phase.

$$
\begin{equation*}
\varepsilon_{G(\text { gainerr })} \approx \frac{1}{A_{0} \cdot \beta} ; \quad \varepsilon_{1(\text { gainerr })} \approx \frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}} ; \quad \varepsilon_{2(\text { gainer })} \approx \frac{1}{A_{0} \cdot \beta} \cdot\left|\frac{1}{2}-\beta\right| . \tag{5.47}
\end{equation*}
$$

The feedback factor is given by:

$$
\begin{equation*}
\beta=\frac{C_{a}+C_{b}}{C_{a}+2 \cdot C_{b}+C_{p_{i}}}, \tag{5.48}
\end{equation*}
$$

and most often $\beta<\frac{1}{2}$.
Secondly, in the presence of limited amplifier bandwidth, the error factors are obtained as:

$$
\begin{equation*}
\varepsilon_{G(B W e r r)} \approx \Delta \cdot \frac{C_{L_{\text {tot }}}}{C_{L_{\text {tot }}}+\frac{\left(C_{a}+C_{b}\right) \cdot C_{p_{i}}}{C_{a}+C_{b}+C_{p_{i}}}} ; \varepsilon_{1(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{L_{\text {fix }}}}{C_{L_{\text {tot }}+\frac{\left(C_{a}+C_{b}\right) \cdot C_{p_{i}}}{}}^{C_{a}+C_{b}+C_{p_{i}}}} ; \varepsilon_{2(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{a}+C_{b}+C_{L_{\text {tot }}}}{C_{L_{\text {tot }}+}+\frac{\left(C_{a}+C_{b}\right) \cdot C_{p_{i}}}{C_{a}+C_{b}+C_{p_{i}}}} \tag{5.49}
\end{equation*}
$$

where $\Delta$ is the linear settling error term of the form $\Delta=e^{-\frac{T}{\tau}}$. The total output load capacitance $C_{L_{\text {tot }}}$ includes the fixed and switched load capacitance:

$$
\begin{equation*}
C_{L_{t o t}}=C_{L_{f i x}}+C_{L_{s w}}, \tag{5.50}
\end{equation*}
$$

while the effective load capacitance $C_{L_{e f f}}$ is given by(3.7):

$$
\begin{equation*}
C_{L_{e f f}}=C_{L_{t o t}}+\beta \cdot C_{p_{i}} . \tag{5.51}
\end{equation*}
$$

Although charge transfer is used to transport and invert charge from one $C_{b}$ capacitor at the amplifier input to another $C_{b}$ capacitor in the amplifier feedback, the amplifier is not loaded by the large $C_{b}$ capacitors. On the other hand, the feedback factor is small, which adversely affects the settling time constant of the filter. Note also the elimination of centre frequency charge transfer capacitor ratio gain error (such as found in the $Q T$ integrator and


Fig. 5.15 $\delta-Q R-I ~ S C ~ B P F ~ c h o s e n ~ f o r ~ i m p l e m e n t a t i o n . ~$
biquad) by virtue of the combined input sampling / output charge recombination $C_{a}$ capacitors.
The $Q T / \delta-Q R$ BPF is a pre-cursor to a complete $\delta$ - $Q R$ BPF to be presented in the next two sections.

### 5.5.3 $\delta$ - $Q R$ Type I $N$-path SC BPF $(\delta-Q R-I)$

The $\delta$ - QR -I BPF [P.3] is the first of two $N$-path BPFs whose operation is based purely on delta-charge-redistribution; the $\delta-Q R-I I$ variant is elaborated on in the next section. Similar to the $Q T / \delta$ - QR BPF, the $\delta$ - QR $-I$ BPF of Fig. 5.15 operates from a 3 phase clock. The basic principle of operation here is that the differential voltage across a set of $C_{b}$ feedback capacitors, for instance $C_{b_{p 1}}, C_{b_{n 1}}$, is mirrored on to a second set of $C_{b}$ capacitors connected to the amplifier outputs: $C_{b_{p 2}}, C_{b_{n 2}}$. Two clock periods later, $C_{b_{p 2}}, C_{b_{n 2}}$ are swapped around and


Fig. 5.16 Equivalent schematic of $\delta-Q R-I ~ S C ~ B P F$ showing capacitive loadings.
placed in the feedback loop of opposite sides of the amplifier. In this way, the circuit block output voltage is inverted and delayed by 2 clock periods to create the inverting delay $\left(-z^{-2}\right)$ required by the filter algorithm. The capacitor pairs $C_{a_{p}}, C_{a_{n}}$ have the same input sampling and damping/charge redistribution function as previously described for the $Q T / \delta-Q R$ BPF.

The equivalent amplifier loading diagram per phase is shown in Fig. 5.16. It also demonstrates the function of each path as it progresses through each clock phase, i.e. sample, idle, and passive charge redistribution. In fact, the state shown in Fig. 5.16 compares to phase 1 of Fig. 5.5. This circuit implements the requirements for delta-charge redistribution explained in sections 2.2.2 and 5.4.1.

The transfer function of the $\delta-Q R-I \mathrm{BPF}$, including error terms $\varepsilon_{G}, \varepsilon_{1}$, and $\varepsilon_{2}$, is:

$$
\begin{equation*}
H_{\delta-Q R-I}(z)=\frac{C_{a}}{C_{a}+C_{b}} \cdot\left(1-\varepsilon_{G}\right) \cdot \frac{z^{-2}}{1-2 \cdot \varepsilon_{1} \cdot z^{-1}+\left(1-\varepsilon_{2}\right)^{2} \cdot \frac{C_{b}}{C_{a}+C_{b}} \cdot z^{-2}} . \tag{5.52}
\end{equation*}
$$

A transfer delay of two clock periods is preferred with the $\delta-Q R-I$ filter for layout reasons, to keep the clock sequencing the same for the $C_{a}$ and $C_{b}$ capacitors and so have each $C_{a}$ and $C_{b}$ pair serviced by the same clocks.

Firstly, a derivation is made of the transfer function error terms for the case of limited amplifier DC gain. The charge conservation equation at the amplifier input nodes of the $\delta-Q R-I$ stage yields:

$$
\begin{align*}
& C_{P_{i}} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}\right)-\left(-\frac{V_{\text {out }}}{A_{0}} \cdot z^{-1}\right)\right) \\
+ & C_{b} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)+\left(-V_{\text {out }} \cdot z^{-2}\right)\right) \\
+ & C_{a} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)-\left(-V_{\text {in }} \cdot z^{-2}\right)\right)=0 . \tag{5.53}
\end{align*}
$$



Fig. 5.17 $\delta-Q R-I I S C B P F$.

After solving (5.53) and reducing to the form of (5.52), the gain error terms are obtained as:

$$
\begin{equation*}
\varepsilon_{G(\text { gainerr })} \approx \frac{1}{A_{0} \cdot \beta} ; \quad \varepsilon_{1(\text { gainerr })} \approx \frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}} ; \quad \varepsilon_{2(\text { gainer })} \approx \frac{1}{2 \cdot A_{0} \cdot \beta}, \tag{5.54}
\end{equation*}
$$

with the $\delta-Q R-I$ feedback factor given by:

$$
\begin{equation*}
\beta=\frac{C_{a}+C_{b}}{C_{a}+C_{b}+C_{p_{i}}} . \tag{5.55}
\end{equation*}
$$

In a similar manner, the error terms due to finite amplifier bandwidth are obtained as:

$$
\begin{equation*}
\varepsilon_{G(B W e r r)} \approx \Delta \cdot \frac{C_{L_{\text {tot }}}}{C_{L_{e f f}}} ; \quad \varepsilon_{1(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}} ; \varepsilon_{2(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{L_{t o t}}-C_{a}}{C_{L_{e f f}}} . \tag{5.56}
\end{equation*}
$$

Note that the switching load capacitance now effectively includes $C_{b}$ at the output which is an addition compared to the $Q T / \delta-Q R$ and $\delta-Q R-I I$ filters. This extra $C_{b}$ load capacitance slows down the operation of the $\delta-Q R-I$ filter, in the same as the extra $C_{b}$ input capacitance does for the $Q T / \delta-Q R$ filter. The final $\delta-Q R-I I$ filter eliminates the need for an input or output $C_{b}$ capacitor but it comes with its own issues as explained next.

### 5.5.4 $\delta$-QR Type II $N$-path $\operatorname{SC} \operatorname{BPF}(\delta-Q R-I I)$

The $\delta$ - QR - II BPF was first invented by the author at Philips in 1997 [59] (and later evaluated in Philips Semiconductors, Nijmegen) as part of a video IF filter and analogue/digital video
demodulation system but never patented. A similar technique using the same basic principles for use in resonator BPFs, although with a charge transfer input stage for transporting the input charge onto the integration capacitor and no $C_{a}$ charge redistribution damping stage, was published later in [60], [61].

Analogous to the $Q T / \delta-Q R$ BPF, the $\delta-Q R-I I$ BPF of Fig. 5.17 recycles the integrated charge every couple of clock cycles (to create $-z^{-2}$ ) but the mode of charge recycling differs. Whereas the $Q T / \delta-Q R$ filter transports charge from integration capacitor to integration capacitor via the amplifier virtual earth node every 2 clock periods, the $\delta-Q R-I I$ filter reuses the same charge on the feedback integration capacitors by swapping around the capacitors $C_{b_{p}}$, $C_{b_{n}}$, every 2 clock periods. This is a multiplexing operation so that, for instance, $C_{b_{p 1}}, C_{b_{n 1}}$ get swapped around on clock phases 1 and 3 , while capacitors $C_{b_{p 2}}, C_{b_{n 2}}$ get swapped around on clock phases 2 and 4 . Clearly, 4 clock phases, each with frequency $f_{s} / 4$, are needed to realize this filter. The capacitor pairs $C_{a_{p}}, C_{a_{n}}$ have the same input sampling and damping/charge redistribution function as for the previous 2 N -path BPFs, except that they operate with multiplexing clocks clkA and clkB of frequency $f_{s} / 2$.

The transfer function of the $\delta-Q R-I I$ filter is similar to that of the $\delta-Q R-I$ apart from the single transfer delay resulting from the double sampling $C_{a}$ capacitors:

$$
\begin{equation*}
H_{\delta-Q R-I I}(z)=\frac{C_{a}}{C_{a}+C_{b}} \cdot\left(1-\varepsilon_{G}\right) \cdot \frac{z^{-1}}{1-2 \cdot \varepsilon_{1} \cdot z^{-1}+\left(1-\varepsilon_{2}\right)^{2} \cdot \frac{C_{b}}{C_{a}+C_{b}} \cdot z^{-2}} . \tag{5.57}
\end{equation*}
$$

Including DC gain error, charge conservation at the amplifier input yields:

$$
\begin{align*}
& C_{P_{i}} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}\right)-\left(-\frac{V_{\text {out }}}{A_{0}} \cdot z^{-1}\right)\right) \\
+ & C_{b} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)-\left(\frac{V_{\text {out }}}{A_{0}} \cdot z^{-2}-\left(-V_{\text {out }} \cdot z^{-2}\right)\right)\right) \\
+ & C_{a} \cdot\left(\left(-\frac{V_{\text {out }}}{A_{0}}-V_{\text {out }}\right)-\left(-V_{\text {in }} \cdot z^{-1}\right)\right)=0 . \tag{5.58}
\end{align*}
$$

The error terms resulting from limited DC gain are obtained for the $\delta-Q R-I I$ BPF as:

$$
\begin{equation*}
\varepsilon_{G(\text { gainerr })} \approx \frac{1}{A_{0} \cdot \beta} ; \quad \varepsilon_{1(\text { gainerr })} \approx \frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}} ; \quad \varepsilon_{2(\text { gainer })} \approx \frac{1}{2 \cdot A_{0} \cdot \beta} \cdot(1-\beta) . \tag{5.59}
\end{equation*}
$$

The high feedback factor is the same as for the $\delta-Q R-I$ filter. The error terms for limited amplifier bandwidth can be derived as:

$$
\begin{equation*}
\varepsilon_{G(B W e r r)} \approx \Delta \cdot \frac{C_{L_{\text {ot }}}}{C_{L_{e f f}}} ; \varepsilon_{1(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}} ; \varepsilon_{2(B W e r r)} \approx \frac{\Delta}{2} \cdot \frac{C_{L_{\text {ot }}}}{C_{L_{e f f}}}, \tag{5.60}
\end{equation*}
$$

with

$$
\begin{equation*}
C_{L_{\text {tot }}}=C_{L_{f i x}}+C_{L_{s w}} . \tag{5.61}
\end{equation*}
$$

The major issue with the $\delta$ - QR - II filter is that because of the lack of an idle phase, direct clock feedthrough appears at $f_{c l k} / 4$, which is right in the middle of the passband. A second related issue is that there is in-band aliasing due to aliasing around multiples of $f_{c l k} / 4$. These in-band artefacts can't be reduced or removed by pre-/post-filtering. Basically, equation


Fig. 5.18 Deviations of (a) $f_{0}$ and (b) $Q$ with amplifier DC gain for the $Q T / \delta-Q R, \delta-Q R-I$, and $\delta-Q R-I I S C$ BPFs. Note all $f_{0}$ deviations are approximately the same.
(5.16) for OHM is not satisfied since, for the $\delta$ - $Q R-I I$ filter, $N$ must be chosen according to $N=2 \times n \times m, m \in\{1,2, \ldots\}$. Hence, great care needs to be taken with the layout of this filter so that positive and negative sides of the amplifier are exactly symmetrical with respect to capacitive loading, parasitic capacitances from the amplifier and switches, and routing to and from the amplifier.

### 5.5.5 Performance Comparison of $N$-path SC BPF Stages

The performances of the 3 different $N$-path BPFs for $f_{0}$ and $Q$ are compared graphically in figures Fig. 5.18 to Fig. 5.21. The SC biquad is not included in this comparison, since $f_{0}$ and $Q$ accuracies are less than what can be achieved with $N$-path filters. Unless otherwise stated, the $N$-path filters compared here share the following design parameters: $f_{s}=44 \mathrm{MHz}, Q=28, C_{p_{i}}=0.3 \mathrm{pF}, C_{a}=0.14 \mathrm{pF}$. The reason for this is that these are approximately the specifications of a single stage of the radio IF BPF discussed and designed in Chapter 6. The exact specification, though, doesn't affect the generalizations that can be made in
(a)

(b)


Fig. 5.19 Centre frequency sensitivities of (a) $Q T / \delta-Q R$ and $(b) \delta-Q R-I S C$ BPFs to $n=T / \tau$. Note $\delta-Q R-I I$ curves are approximated by $Q T / \delta-Q R(a)$ above.
comparing the different filters.
Consider first the effect of limited DC gain on all filters. From Fig. 5.18(a), it can be seen that all 3 N -path filters show the same sensitivity of $f_{0}$ to DC gain (i.e. same $\varepsilon_{1(\text { gainerr })}$ ), since they all have the same dependency on amplifier input parasitic $C_{p_{i}}$. On the other hand, $Q$ sensitivities differ. The best performing filter for sensitivity of $Q$ to DC gain is the $Q T / \delta-Q R$ see Fig. 5.18(b). The main reason for this can be understood with the help of (5.46) and (5.47), where each $C_{b}$ capacitor, before being placed in the amplifier feedback, is pre-charged with $-V_{\text {out }} / A_{0}$ from 2 clock periods earlier. Hence, the $\varepsilon_{2}$ term for $Q$ deviation can be very small. A DC gain of 60 dB gives a centre frequency deviation of less than $0.075 \%$ for all medium to high- $Q$ filters, while it ensures a $Q$ deviation of less than $0.5 \%$ for the $Q T / \delta-Q R$ and the $\delta-Q R-I I$ BPFs but $2 \%$ deviation for the $\delta-Q R-I$ BPF.

Consider next the effect that limited amplifier bandwidth has on performance. Accuracy in the context of settling is defined as that accuracy in $f_{0}$ or $Q$ achieved after a certain specified number of closed loop amplifier time constants - this is usually the number of time constants


Fig. 5.20 $Q$ factor sensitivities of (a) $Q T / \delta-Q R B P F$ and (b) $\delta-Q R-I B P F$ to $n=T / \tau$. Note $\delta-Q R-I I$ curves are approximated by $Q T / \delta-Q R(a)$ above.
elapsed in one clock period: $n \cdot \tau=\frac{1}{f_{s}}$. Fig. 5.19 shows the $f_{0}$ sensitivities of the different BPFs, while Fig. 5.20 shows the $Q$ sensitivities. Clearly, when measured in units of $\tau$, the $\delta-Q R-I \mathrm{BPF}$ settles to a given accuracy in a smaller number of $\tau$ compared to the $Q T / \delta-Q R$ or $\delta-Q R-I I$ filters. For instance, with a $C_{p_{i}}$ of 0.3 pF , it takes the $Q T / \delta-Q R$ and $\delta-Q R-I I$ BPFs $4 \frac{1}{2} \tau$ to reach $0.1 \% f_{0}$ deviation, whereas the $\delta-Q R-I$ BPF requires $3 \frac{1}{2} \tau$. Similarly, for a $Q$ of 30 , the $Q T / \delta-Q R$ and $\delta-Q R-I I$ BPFs require $7 \frac{1}{2} \tau$ to reach $2 \% Q$ accuracy, whereas the $\delta$ - $Q R-I$ BPF requires $6 \frac{1}{2} \tau$. Note that in all cases, the $Q$ deviation can be partially compensated for by slightly "over-designing" the capacitor ratio $C_{b} / C_{a}$, since the median effects of limited amplifier gain-bandwidth can be predicted at layout through simulation. This also has little effect on $f_{0}$ accuracy due to the independence of $f_{0}$ from capacitor ratios in these N -path filters.

For a fair comparison of settling accuracy, the curves in Fig. 5.19 and Fig. 5.20 don't give the complete picture, since clearly $\tau$ differs from one filter to the next due to each filter's different equivalent load capacitance. The curves in Fig. 5.21 better show this comparison,


Fig. 5.21 Normalized comparison of (a) $f_{0}$ and $(b) Q$ deviations with number of time constants per clock period for the $Q T / \delta-Q R, \delta-Q R-I$, and $\delta-Q R-I I B P F s$; Time constants are normalized to those of $\delta-Q R-I B P F ; Q=30$ and $C_{p_{i}}=0.3 p F$.
where all BPF accuracies are set out against one and the same time constant - in this case all BPF $\tau$ 's are normalized to the $\tau$ of the $\delta-Q R-I$ BPF. Now a different picture develops, in which the $\delta$ - QR -II BPF has clearly the best $f_{0}$ and $Q$ accuracy of the $3 N$-path BPFs when all filter amplifiers have equally loaded $G B W \mathrm{~s}$. The $\delta-Q R-I$ BPF is a good second and the $Q T / \delta$ - $Q R$ BPF falls somewhat behind. The main reason for the good settling performance of the $\delta$ - $Q R-I I$ BPF is that it is never externally loaded by integration capacitor $C_{b}$, either by virtue of charging it up at the output as in the $\delta-Q R-I$ BPF or by having it as a charge transfer input stage such as in the $Q T / \delta-Q R$ BPF.

Unfortunately, unavoidable clock feedthrough noise and mirror frequency noise around the centre frequency $\left(f_{0}=f_{s} / 4\right)$ makes the $\delta$ - QR - II BPF unusable for many high-selectivity applications, especially those IF applications (e.g. radio or video) that require post-filter gain and/or automatic gain control, since the clock feedthrough could be of the order of the signal itself, reducing dynamic range. Cascading of filter stages with intermediate variable gain would further accentuate this clock feedthrough. The $\delta-Q R-I I$ BPF is discounted for applica-
tions requiring high $S F D R$ like video and $\mathrm{AM} / \mathrm{FM}$ radio, such as examined in Chapter 6. Note that if the output of the $\delta-Q R-I I$ BPF is followed by an ADC, the clock feedthrough could be filtered out in the digital domain. Therefore, not just the signal conditioning is more expensive, due to the higher dynamic range requirements of the ADC to cater for the extra passband noise, but the digital signal processing is more expensive due to the required inclusion of a sharp notch filter. A good choice, therefore, for BPF implementation is the $\delta-Q R-I$ concept, since it follows the guidelines under orthogonal hardware modulation of section 5.3.3, where the number of hardware paths can be kept independent of the filter order. It is also the next best candidate for filter accuracy. The SC $N$-path recursive BPFs presented in Chapter 6 are based around the $\delta-Q R-I$ concept. Table 5.1 summarizes the main points of comparison for each $N$ path concept.

Table 5.1 Performance Comparison of the 3 N-path BPF Concepts

|  | $Q T / \delta-Q R$ | $\delta-Q R-I$ | $\delta-Q R-I I$ |
| :---: | :---: | :---: | :---: |
| $f_{0}$ error due to DC gain, $\varepsilon_{1(\text { gainerr })}$ | $\frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}}$ | $\frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}}$ | $\frac{1}{2} \cdot \frac{C_{p_{i}}}{C_{a}+C_{b}} \cdot \frac{1}{A_{0}+\frac{1}{\beta}}$ |
| $Q$ error due to DC <br> gain, $\varepsilon_{2(\text { gainerr })}$ | $\frac{1}{A_{0} \cdot \beta} \cdot\left\|\frac{1}{2}-\beta\right\|$ | $\frac{1}{2 \cdot A_{0} \cdot \beta}$ | $\frac{1}{2 \cdot A_{0} \cdot \beta} \cdot(1-\beta)$ |
| $f_{0}$ error due to OTA <br> BW, $\varepsilon_{1(B W e r r)}$ | $\frac{\Delta}{2} \cdot \frac{C_{L_{f i x}}}{C_{L_{t o t}}+\frac{\left(C_{a}+C_{b}\right) \cdot C_{p_{i}}}{C_{a}+C_{b}+C_{p_{i}}}}$ | $\frac{\Delta}{2} \cdot \frac{C_{L_{f i x}}}{C_{L_{e f f}}}$ | $\frac{\Delta}{2} \cdot \frac{C_{L_{f i x}}}{C_{L_{\text {eff }}}}$ |
| $Q$ error due to OTA BW, $\varepsilon_{2(B W e r r)}$ | $\frac{\Delta}{2} \cdot \frac{C_{a}+C_{b}+C_{L_{t o t}}}{C_{L_{\text {tot }}}+\frac{\left(C_{a}+C_{b}\right) \cdot c_{p_{i}}}{C_{a}+C_{b}+C_{p_{i}}}}$ | $\frac{\Delta}{2} \cdot \frac{C_{L_{\text {tot }}}-C_{a}}{C_{L_{\text {eff }}}}$ | $\frac{\Delta}{2} \cdot \frac{C_{L_{\text {lot }}}}{C_{L_{\text {eff }}}}$ |
| Feedback factor, $\beta$ | $\frac{C_{a}+C_{b}}{C_{a}+2 \cdot C_{b}+C_{p_{i}}}$ | $\frac{C_{a}+C_{b}}{C_{a}+C_{b}+C_{p_{i}}}$ | $\frac{C_{a}+C_{b}}{C_{a}+C_{b}+C_{p_{i}}}$ |
| Power for given settling accuracy $\propto$ | $C_{L_{\text {lot }}}+C_{b}+C_{p_{i}}+C_{L_{\text {ot }}}\left(\frac{c_{b}+C_{p_{i}}}{C_{a}+C_{b}}\right)$ | $c_{L_{\text {lot }}}+C_{b}+C_{p_{i}}+c_{p_{i}} \cdot\left(\frac{c_{L_{\text {lot }}}+C_{b}}{C_{a}+C_{b}}\right)$ | $c_{L_{\text {tot }}}+C_{p_{i}}+C_{p_{i}}\left(\frac{c_{L_{\text {Lot }}}}{C_{a}+C_{b}}\right)$ |
| Noise power spectral density at $f_{0}$ | $\left(2 \cdot \frac{k T}{C_{a}}+N_{\text {OTA }}\right) \cdot \frac{2}{f_{s}}$ | $\left(2 \cdot \frac{k T}{C_{a}}+N_{\text {OTA }}\right) \cdot \frac{2}{f_{s}}$ | $\left(2 \cdot \frac{k T}{C_{a}}+N_{\text {OTA }}\right) \cdot \frac{2}{f_{s}}$ |
| Clk feedthru +aliasing | (+) Out-of-band. Can be removed thru pre-/post-filtering. | (+) Out-of-band. Can be removed thru pre-/post-filtering. | (-) In-band. <br> Cannot be removed thru pre-/post-filtering. |

### 5.6 Conclusions

It was shown in this chapter how delta-charge redistribution $(\delta-Q R)$ can be applied to create highly accurate $N$-path SC BPFs. Essentially, an inverted delayed version $\left(-z^{-2}\right)$ of the output voltage is created in 3 unique ways in the 3 different $\delta$ - $Q R$ SC $N$-path BPFs presented here. They all share the common property that the only input to the circuit is through a capacitor $C_{a}$ which acts as a feeder of input signal charge to the integration capacitor $C_{b}$ via charge redistribution alone. It has the extra function of providing controlled damping for an accurate $Q$. All filters require a single OTA and have matched configurations from clock to clock.

Orthogonal hardware modulation (OHM) was elucidated in the context of SC N -path filters, where the number of hardware paths $N$ is chosen independent of the functional modulation factor $n$ in order to avoid in-band interference.

The first BPF $(Q T / \delta-Q R)$ relies on a combination of charge transfer ( $Q T)$ and $\delta-Q R$. Although accurate, it is slowed down by a large input capacitance $C_{b}$ and is the least accurate of the three BPFs. The second BPF $(\delta-Q R-I)$ is based on pure $\delta-Q R$ for its operation but requires charging of an output capacitance $C_{b}$ - it follows all the guidelines, though, for accurate SC filter design (section 1.4). The final BPF $(\delta-Q R-I I)$ is also based on pure $\delta-Q R$ and is the fastest of all three. The $\delta-Q R-I I$ BPF is deficient in one important requirement for OHM in that the number of paths $N$ must be some multiple of $2 n$, where $n$ is the filter order. Hence, there is no idle phase. Clock feedthrough noise and mirror frequency components appear in band due to practical implementation limitations. In this respect, the $\delta-Q R-I$ BPF is found most suitable for implementation in an analogue front-end for high-selectivity applications.

## Chapter 6

## High-Accuracy $\boldsymbol{\delta}$ - $\boldsymbol{Q} \boldsymbol{R}$ SC BPF Design And Measurements

This chapter focuses on two CMOS implementations of high-frequency SC BPFs that draw on the design concepts developed in Chapter 5, i.e. delta-charge redistribution $(\delta-Q R)$ and orthogonal hardware redistribution (OHM). The first BPF to be presented is called a TV Cloche filter and is required in conventional terrestrial television receivers for high-frequency de-emphasis of SECAM TV video signals[62]. It is one of the most difficult TV filters to integrate on chip with sufficient accuracy [63]. The second BPF to be presented is an integrated version of the IF channel selection filter in FM radio receivers with a centre frequency of 10.7 MHz [64]. Up till now, the limitations of integrated radio selectivity filters in terms of power dissipation, dynamic range and cost, are such that it is still required to use an external ceramic 10.7 MHz bandpass filter. This design demonstrates a CMOS SC IF filter that can be integrated with most of the rest of the FM receiver, eliminating external components and printed circuit board area.

Each SC BPF is firstly placed in a system context and the adaptation of the traditional TV receiver, in the case of the Cloche filter, and the portable radio receiver, in the case of the 10.7 MHz IF BPF, are examined. Next, the detailed circuit design and layout of each filter is explored followed by a presentation of the chip measurement results. Finally, a summary is given of this work and its significance.

### 6.1 SC Video BPF - the TV Cloche Filter

This section presents the design of a low power, high dynamic range recursive SC video BPF in a standard digital CMOS process through the use of poly-metal1-metal2 sandwich capacitors for the realization of the filter coefficients. The main purpose of the filter to be described is to produce a particular non-linear phase characteristic in a video channel as well as the creation of selectivity. This filter is shown to be highly linear with low power and is designed as part of an integrated multi-standard TV colour decoder in an embedded application.

System level considerations for implementation of the SC Cloche filter are first explored


Fig. 6.1 Spectrum of (a) video input signal (CVBS) and (b) Cloche BPF transfer response.
in this section. Next, the SC filter circuit design is examined. The dual-input single-stage telescopic OTA with very high current efficiency, proposed in Chapter 4, is implemented as part of the design. Next, the layout and floor-planning are explained and finally chip measurements are detailed.

### 6.1.1 System Level Considerations

One of the most critical circuit blocks needed in a present-day multi-standard TV colour decoder is the Cloche video BPF for demodulation of the French / East European TV standard, SECAM (SEquential Couleur À Mémoire) [62], [63]. Two separate FM modulated colour subcarriers are used in the SECAM TV system to carry the colour information which is transmitted on a TV line-sequential basis. On one TV line the blue colour difference information (B-Y) is transmitted on a subcarrier of nominal frequency 4.25 MHz , whereas on the following TV line the red colour difference information ( $\mathrm{R}-\mathrm{Y}$ ) is transmitted on a colour subcarrier of nominal frequency 4.406 MHz . The luminance information ( Y ), on the other hand, is transmitted in the same way from line to line and has a bandwidth extending from 0 to 6 MHz . Both signals are transmitted together as one composite TV signal (called CVBS for Composite Video Burst and Synch) such as shown in Fig. 6.1(a). Before addition of the two signals in the transmitter, however, high frequency pre-emphasis is applied to the chrominance. This pre-emphasis filter is designed to keep the colour subcarrier amplitude, and thereby its visibility, low in de-saturated or dark areas of the picture, while at the same time keeping the noise immunity of the signal high in the bright and saturated areas. Since the chrominance is FM modulated, the group delay "distortion" produced in the transmitter must be undone or equalized by the high frequency de-emphasis filter in the chrominance path of the SECAM demodulator. This is the main function of the Cloche BPF.

(b)

(c)


Fig. 6.2 Sampled-data SECAM decoder including SC Cloche filter.

The required specifications of an integrated Cloche video BPF under all operating conditions can be summarized as follows:

- $f_{\text {cloche }}=4.286 \mathrm{MHz}( \pm 20 \mathrm{kHz})$
- $Q=16 \pm 1$
- Full signal handling capability for differential video signals $\left(2 \mathrm{~V}_{\mathrm{pp}}\right.$ nominal, extending to $5 \mathrm{~V}_{\mathrm{pp}}$, worst case).
The last point mentioned implies a 5 V supply voltage $\left(V_{D D}\right)$ is required if input attenuation is to be avoided.

An example of how the SC Cloche filter fits into a sampled-data SECAM TV FM receiver is shown in Fig. 6.2(a) (after patent [P.22]). The signal spectra illustrating the operation of the receiver are shown in Fig. 6.3. One of the most important reasons for the choice of $f_{s}=6 f_{\text {cloche }}$ as sample frequency is that this is the lowest sample frequency which makes the proposed system in Fig. 6.2 feasible: the following explanation motivates this.


Fig. 6.3 Spectra of signal progression through SECAM decoder.

Being a discrete-time channel, no hard amplitude limiting can be used as in a standard continuous-time (SECAM) FM receiver. Otherwise, the clipping action would create substantial phase errors and hence aliased distortion products of the signal. Instead, amplitude normalization occurs through the combined use of a slow ACC (automatic colour-level control) and a fast ACC. The fast ACC is a replacement for the limiter. However, even a very good ACC circuit produces some distortion. For this reason, the input signal is not transferred to DC after the

Cloche filter via mixing (Fig. 6.3(a),(b)) but to an intermediate frequency which pushes any distortion produced out of band. This is why mixing takes place with $3 / 2 f_{\text {cloche }}$ so that the filtered SECAM chrominance signal is transferred to $1 / 2 f_{\text {cloche }}$ and its image gets transferred to $5 / 2 f_{\text {cloche }}$ (Fig. 6.3(c)). The images are removed using simple lowpass filters with a zero at $5 / 2 f_{\text {cloche }}$ (Fig. 6.3(d),(e)). Now that it has been decided to mix the input signal with $3 / 2 f_{\text {cloche }}$, the Cloche BPF before the mixers should be clocked at a frequency that is an even multiple of $f_{\text {cloche }}-$ after the OHM procedure of section 5.3.3 - and should also be a multiple of the mixing frequency $3 / 2 f_{\text {cloche }}$ to allow for a robust realization of the mixers with the simplest coefficients (viz. -1 and +1 ). From these considerations, it follows that the Cloche BPF should operate at $f_{s}=6 f_{\text {cloche }}$, with $n=3$ (equation (6.15)).

The proposed fast ACC (Fig. 6.2(b)) [P.23] is novel in that it is a feedback gain control, instead of the conventional complex feedforward type [P.1]. In this way, the squarers don't have to process varying amplitudes, since the input has regulated amplitude $A$, instead of varying $E(t)$ as in the feedforward type. The circuit implementation is much simpler as a result. Some distortion is inevitably produced (Fig. 6.3(f)), as explained earlier, but because of the decoder architecture, it remains out of the signal band. In fact, only the $11^{\text {th }}$ harmonic folds back which is of no consequence.

The output signals of the controllable amplifiers of the fast ACC are applied to the respective inputs of an FM demodulator [P.1], which furnishes chrominance signals B-Y and R-Y. Fig. 6.3(g) illustrates the FM to AM conversion. These chrominance signals B-Y and RY are, together with a luminance signal Y derived from the CVBS input signal, applied to a colour matrix circuit to produce colour signals R, B and G. Finally, these colour signals are applied to a colour display unit via a set of output amplifiers.

### 6.1.2 Design of SC Cloche Filter Circuitry

The implementation of the SC Cloche BPF in a standard $0.8 \mu \mathrm{~m}$ CMOS process is described in this section. Firstly the filter architecture is explained and then the details of the SC circuitry, amplifier and layout are described.

### 6.1.2.1 Filter Architecture

With $n=3$, the required number of paths for implementation of the Cloche BPF as an $N$-path SC BPF is $N=4$ after equation (5.17). The pseudo-4-path filter implementation, with 4 (passive) multiplexed feedback paths, is depicted at functional level in Fig. 6.4 with $f_{s}=6 f_{\text {cloche }}$, i.e. 25.716 MHz . Assuming all feedback paths in Fig. 6.4 are equal, the total filter transfer function is given by:

$$
\begin{align*}
H(z) & =\left(1-r^{3}\right) \cdot \frac{z^{-3}}{1+r^{3} \cdot z^{-3}},  \tag{6.1}\\
r & =e^{-\frac{\pi \cdot f_{0}}{Q \cdot f_{s}}} \tag{6.2}
\end{align*}
$$

with
from equation (5.9). In this filter, the centre frequency depends primarily on the chosen clock, whereas the $Q$-factor depends only on a simple capacitor ratio via the damping coefficient $r^{3}$.


Fig. 6.4 Functional representation of pseudo-4-path recursive comb BPF.

Poles are placed exactly at frequencies $\pm f_{\text {cloche }}$ and $3 f_{\text {cloche }}$.
The group delay transfer function $\tau_{g}$ of the BPF is found from:

$$
\begin{align*}
\tau_{g}(\omega T) & =-\frac{d}{d(\omega T)} \arg [H(\omega T)] \\
& =-\frac{3 \cdot r^{3} \cdot T \cdot\left[r^{3}+\cos [3 \omega T]\right]}{1+r^{6}+2 \cdot r^{3} \cdot \cos [3 \omega T]} . \tag{6.3}
\end{align*}
$$

The maximum group delay at $f_{\text {cloche }}=f_{s} / 6$ can be derived as:

$$
\begin{equation*}
\tau_{g_{M A X}}=\frac{3 \cdot r^{3} \cdot T}{1-r^{3}} . \tag{6.4}
\end{equation*}
$$

Note that the group delay is exactly symmetrical with respect to the centre frequency, since this is the pole frequency at $f_{\text {cloche }}$, with further poles appearing at exact multiples of $2 f_{\text {cloche }}$ in the positive and negative frequency directions.

The frequency spectrum of the incoming SECAM video signal is sketched in Fig. 6.1(a) together with the frequency response of the sampled-data Cloche BPF in Fig. 6.1(b). It can be seen that because of the superimposed luminance signal in the chrominance channel which can extend from 0 to 6 MHz , the Cloche BPF at 4.286 MHz should avoid intermodulation between the wanted chrominance and the unwanted luminance.

The filter represented in Fig. 6.4 is an example of a filter designed using the guiding principles of OHM presented in section 5.3.3. Only the feedback path needs to be multiplexed, where 4 paths are required to realize a delay of 3 sample periods. This has an important advantage with respect to unwanted aliasing resulting from any path mismatch, since in a direct 3path filter, aliasing occurs of frequencies at $f_{\text {cloche }}+\delta f$ back to $f_{\text {cloche }}-\delta f$ and vice-versa. Hence, with any path mismatch, aliasing occurs of in-band frequencies in the direct 3-path BPF. On the other hand, in this pseudo-4-path realization with multiplexed feedback path, aliasing only occurs of out-of-band frequencies back to in-band frequencies in the BPF. For example, frequency components at $1 / 2 f_{\text {cloche }}, 2 f_{\text {cloche }}$ and $5 / 2 f_{\text {cloche }}$ fold to $f_{\text {cloche }}$ due to any path mismatch. This filter architecture offers the possibility of reducing any aliasing due to capacitor mismatch by pre-filtering. Pre-filtering has no effect on in-band aliasing in a direct


Fig. 6.5 Simplified schematic of $\delta$-QR SC Cloche BPF.

3-path BPF solution. For a video Cloche BPF, only luminance frequencies around $1 / 2 f_{\text {cloche }}$ are of any concern. In addition, any clock feedthrough noise peaks appear out-of-band at multiples of $3 / 2 f_{\text {cloche }}$, which are outside the video baseband and thus are not visible in terms of fixed pattern noise on the television screen.

The SC realization, shown in Fig. 6.5, is based on the $\delta$ - $Q R-I$ concept presented in Chapter 5. The pole damping factor of (6.1) is given by:

$$
\begin{equation*}
r=\left(\frac{C_{b}}{C_{a}+C_{b}}\right)^{\frac{1}{3}} \tag{6.5}
\end{equation*}
$$

Full range video signals can be processed by the BPF without any need for input attenuation


Fig. 6.6 Amplifier used in Cloche BPF together with just two anti-phase filter paths.
which would only reduce the overall $S N R$. For the SC Cloche BPF with $Q=16$ and $f_{\text {cloche }}=4.286 \mathrm{MHz}$, it follows from (6.2) that $r=0.9678$. From (6.5), $C_{b}=C_{a} \cdot r^{3} /\left(1-r^{3}\right)$, giving $C_{b}=9.693 \times C_{a}$. Sandwich capacitors of poly-M1-M2 were used, which in spite of their large bottom plate capacitance (of the order of 0.7 times the active capacitance), it was still possible to design a high-frequency filter suitable for video processing because of the high feedback factor achievable with the $\delta-Q R$ filter technique employed. The size of $C_{a}$ was based on achieving an acceptable matching and $S N R$ for video. Here, $C_{a}$ has an effective value of 271.2 fF , while $C_{b}$ has an effective value of 2628 fF . The OTA $g_{m}$ is nominally $4.6 \mathrm{~mA} / \mathrm{V}$. The external load capacitance has been extracted to be 10.2 pF and the closed-loop bandwidth is 44 MHz for a feedback factor 0.65 . Equivalently, the circuit has a nominal settling time-constant of 3.5 ns which is lower than strictly necessary for this design. However, extra margin was built in to the design to account for slow process parameters, high die temperatures, slewing and clock non-overlap times.


Fig. 6.7 Cloche BPF amplifier including SC common-mode feedback.

### 6.1.2.2 SC BPF Amplifier

The amplifier used in the design of the SC video BPF is based on the DITO amplifier proposed in 4.2 and shown in Fig. 6.6. Only 2 differential anti-phase filter paths are depicted for ease of illustration. The active signal capacitors $C_{a}$ and $C_{b}$ of Fig. 6.5 are each split in 2 between the top and bottom halves of the OTA, so that there is a mirroring of the functionality of the SC BPF for the top half of the OTA with a PMOS input stage as for the bottom half with an NMOS input stage. The P - and N -inputs have been designed in such a way that the $g_{m}$ 's of both inputs are nominally the same and that the capacitance of each input is nominally the same. Any mismatch between the top and bottom halves, however, is in principle not important since it was shown in section 4.2 that both P - and N -inputs work in unison with respect to the input and output signals. The settling performance is determined by the parallel combination of the P - and N - sides of the OTA. The P -inputs are dimensioned as 7 parallel strips each of value $30 / 1$ giving a total W/L of $210 / 1$ for each PMOS input transistor. The N-inputs, in turn, are dimensioned as 4 parallel strips of 30/1.6 giving a total W/L of 120/1.6 for each NMOS input transistor. The nominal tail currents of the OTA are set at $600 \mu \mathrm{~A}$. This results in $g m_{P}$ being $2.2 \mathrm{~mA} / \mathrm{V}$, whereas $g m_{N}$ is $2.4 \mathrm{~mA} / \mathrm{V}$ and hence the total effective transconductance


Fig. 6.8 Chip micrograph of Cloche Video BPF.
becomes $4.6 \mathrm{~mA} / \mathrm{V}$.
Only NMOS switches were used in this design. As will be demonstrated in section 6.1.2.4, $C_{a}$ is split in 2 with each half having its own set of switches. Similarly, each capacitor $C_{b}$ is split into 18 sub-capacitors, each with its own set of switches. Transistors of size 6/0.8 were used for those switches switching at $V_{\text {refp }}$ and at the input and output voltage levels, whereas switches of only $3 / 0.8$ were used for those switches switching at $V_{\text {refn }}$. Double PMOS cascoding was used in order to balance up the output resistances looking back into the PMOS and NMOS sides. The biasing of all the cascodes was implemented using a form of replica biasing [68]. The reference voltages $V_{\text {refp }}$ and $V_{\text {refn }}$ were chosen as 3 V and 1.2 V , respectively. Simulations showed that the DC gain of the OTA remained above 70dB for a voltage swing of $6 \mathrm{~V}_{\mathrm{pp}}$. Note that $V_{\text {refp }}$ could have been chosen as high as 3.5 V but because only NMOS switches were used, this would have required the use of too large switches for an acceptable "on" resistance.

### 6.1.2.3 Common-Mode Feedback

A SC common-mode feedback (CMFB), shown in Fig. 6.7, has been adopted for the DITO. Double-sampling is used, whereby each clock cycle, the output common-mode voltage $V_{C M}=\left(V_{\text {out }_{p}}+V_{\text {out }_{n}}\right) / 2$ is sampled onto two gate-oxide capacitors in parallel; this common voltage is then integrated onto a gate-oxide capacitor, $C_{i n t}$. The voltage on $C_{i n t}$ is compared to


Fig. 6.9 Floor-plan for layout of one side of Cloche BPF.
the common-mode reference level $V_{\text {refcm }}$ via a small auxiliary differential-pair. Around half of the N -input tail current is determined by the CMFB circuit, with the rest determined by a fixed current source. This is done to increase the settling time-constant of the CMFB circuit with respect to the differential-mode circuit and so ensure stability of the CMFB. The CMFB circuitry occupies about $15 \%$ of the total OTA area.

### 6.1.2.4 Chip Layout

The Cloche BPF circuitry was prototyped in a standard $0.8 \mu \mathrm{~m}$, single-poly, double-metal CMOS process [P.3]. The chip micrograph is shown in Fig. 6.8. To ensure proper interfacing for the sake of testing, an input track-and-hold (T\&H) is used to directly sample the input video signal, while a sample-and-hold (S\&H) output buffer is placed after the Cloche BPF for external probe measurements. The clock circuitry and voltage references have also been included on chip. The essential approach to the layout of the BPF is depicted in Fig. 6.9 for the top half of the filter only. This represents the positive input side to the OTA, with the negative input side having a similar construction. It was noted in section 6.1.2.2 that capacitors $C_{a}$ and $C_{b}$ are split in 2 between the top and bottom halves of the OTA, i.e. the P- and N-inputs. Furthermore, each capacitor, $C_{b} / 2$ is split into 9 sub-capacitors and laid out with respect to each capacitor $C_{a} / 2$ as illustrated in Fig. 6.9. These individual sub-capacitors have their own set of switches so that the environment for the capacitor $C_{a} / 2$ is imitated for each of the 9 sub-capacitors of $C_{b} / 2$ for improved matching with process variations. It was mentioned in section 6.1.2.1 that $C_{a}$ has an effective capacitance of 271.2 fF , so that each individual capacitor $C_{a} / 2$ has a value of 135.6 fF , whereas $C_{b}$ has a value of 2628 fF giving each sub-capacitor of $C_{b}$ a


Fig. 6.10 Measured group delay characteristic with a peak of $1.29 \mu s$ at $f_{\text {cloche }}$.
value of 146 fF or $1.077 \times C_{a} / 2$. The sub-capacitors of $C_{b}$ are so constructed that their area capacitance and edge capacitance are scaled by 1.077 with respect to $C_{a} / 2$. Precautionary measures were taken in the design to help reduce substrate pick-up [65]. Separate analogue and digital supplies are used, as well as replica biasing for the OTAs. An N-well connected to a reference is placed under each capacitor for shielding. The area of the SC Cloche BPF is $0.75 \mathrm{~mm}^{2}$. Had a double-poly capacitor option been available, then the area of the filter could have been reduced to $0.25 \mathrm{~mm}^{2}$ in $0.8 \mu \mathrm{~m}$ CMOS.

### 6.1.3 Measurement Results

In this section, the typical measurement results are presented from 12 randomly chosen chip samples. These measurements were made using a 5 V supply voltage at room temperature. With the clock frequency set at 6 times the nominal frequency, i.e. 25.716 MHz , the frequency was measured as $4.283 \mathrm{MHz}(-0.07 \%$ error $)$, while the $Q$ was measured as 15.8 compared to the design value of 16 ( $-1.25 \%$ error). The all-important group delay characteristic has been measured on a network analyser and is displayed in Fig. 6.10. The peak group delay at $f_{\text {cloche }}$ was calculated in equation (6.4) to be $3 \cdot r^{3} \cdot T /\left(1-r^{3}\right)$, which for $r=0.9678$ becomes $29 \times T$. However, this calculation does not include the 3 clock period delay required for the realization of the SC Cloche BPF, noted in (6.1), plus the 2 extra clock delays due to the T\&H and the $\mathrm{S} \& \mathrm{H}$ in the measurement path. Hence the total delay at $f_{\text {cloche }}$ should be $34 \times T$. With $T=1 / f_{S}=38.9 \mathrm{~ns}$, the total group delay including the 5 clock period phase delay should be 1322 ns . The network analyser performs a simple differentiation of the phase characteristic of the Cloche filter and returned a peak group delay value of $1.29 \mu \mathrm{~s}$.

The measured bandpass transfer characteristics are shown in Fig. 6.11 for 5 clock frequencies ranging from 6 MHz to 30 MHz . It can be seen that the frequencies remain fixed at $1 / 6$ of the clock frequency, while the $Q$ remains relatively constant at around 16, being only dependent on a simple capacitor ratio. For the higher sampling frequencies, the transconductance of


Fig. 6.11 Measured BPF transfers for five different clock frequencies.
the OTA and the switch resistances play an increasing role in the incomplete settling of the filter between clock periods which help to reduce the centre frequency and $Q$ of the filter. The full sample-and-hold characteristic is visible for a clock frequency of 6 MHz in the frequency span shown. Fig. 6.12 shows the resultant noise spectrum at the chip output after 10,000 averages on a spectrum analyzer. The peak noise spectral density was measured as $177 \mathrm{nV} / \sqrt{\mathrm{Hz}}$, which also includes the noise produced by the T\&H, the S\&H and the active measurement probe in the measurement path.

The intermodulation performance can be seen in Fig. 6.13, where 1\% intermodulation (IM3) was measured for 2 input signals at a level of 13.1 dBm (or $2.85 \mathrm{~V}_{\mathrm{pp}}$ ) with 40 kHz separation. The total noise was measured as $118 \mu \mathrm{~V}_{\text {RMS }}$ which means the filter dynamic range becomes 79 dB for $1 \%$ IM3. The dominant clock feedthrough was at a frequency of half the input reference clock frequency and was measured to be about $1 \mathrm{mV}_{\mathrm{pp}}$. The maximum output voltage was $6 V_{\text {pp }}$ before the required specifications of the Cloche BPF were no longer achieved.

Aliasing was measured by injecting frequencies at $1 / 2 f_{\text {cloche }}$ and $2 f_{\text {cloche }}$ and measuring their output at $f_{\text {cloche }}$. Aliasing levels at or below -55 dB were measured at $f_{\text {cloche }}$, which is more than adequate for this application.

The Cloche BPF can also be characterized via its impulse response - see Fig. 6.14. Effectively a pulse of 0110 is applied at the input. After each period of the output waveform, the amplitude falls off with a factor of $e^{-\pi / Q}$. Hence, the $Q$ factor can obtained by dividing successive amplitudes $\left(E_{1}, E_{2}\right)$ to give:

$$
\begin{equation*}
Q=-\frac{\pi}{\ln \left[\frac{E_{2}}{E_{1}}\right]} . \tag{6.6}
\end{equation*}
$$

The attenuation of the impulse response is just $\left(1-r^{3}\right)$, or about -20 dB . The centre frequency of the Cloche BPF can also be ascertained from the measured impulse response by examining


Fig. 6.12 Noise spectral density at filter output after 10,000 averages on a spectrum analyzer.


Fig. 6.13 $1 \%$ IM3 for two input signals of $2.9 V_{p p}$ and 40 kHz separation.
the rotation of the sampling clock moments from one cross-over point to the next and comparing this to the resonance frequency of the impulse response. It was possible in this way to confirm the Cloche BPF centre frequency as 4.283 MHz .

Finally, the functional performance of the SC Cloche BPF was tested using a SECAM video signal as input. In Fig. 6.15, the response can be seen of the Cloche BPF to a video frequency sweep of 3.9 MHz to 4.5 MHz . The pre-emphasis characteristic in the transmitter is equalized by the receiver integrated Cloche filter. No attenuation of the video input signal is required by the integrated Cloche filter and it is capable of handling the full signal range of those video signals delivered via an external SCART cable or from the video IF stage.

A summary of the SC Cloche BPF measurements is presented in Table 6.1.


Fig. 6.14 Measured impulse response of Cloche SC BPF.


Fig. 6.15 Cloche SC BPF response to a SECAM video signal frequency sweep.

Table 6.1 Measured Performance of the SC Cloche BPF

| IC Technology | $0.8 \mu \mathrm{~m}$ CMOS - no options |
| :---: | :---: |
| Area BPF | $0.75 \mathrm{~mm}^{2}$ |
| Supply | Single 5 V |
| Clock Freq for Cloche BPF | $6 \times 4.286 \mathrm{MHz}=25.716 \mathrm{MHz}$ |
| centre frequency $f_{0}$ | 4.283 MHz |
| $Q$ factor | 15.8 |
| Power Consumption | 4 mW |
| Noise spectral density @ $f_{0}$ | $177 \mathrm{nV} / \sqrt{\mathrm{Hz}}$ |
| Max Output | $6 \mathrm{~V}, \mathrm{pp}$ |
| CMRR @ $f_{0}$ | 56 dB |
| PSRR @ $f_{0}$ | 32 dB |
| Dynamic Range $(1 \%$ IM3) | 79 dB |



Fig. 6.16 SC IF filter for portable FM radio.

### 6.2 10.7MHz SC Radio IF BPF

In this section, a low power $6^{\text {th }}$ order SC bandpass filter (BPF), with added selectable gain control, is presented for 10.7 MHz radio IF selectivity. It goes further than previous designs in the literature in achieving the required specifications of a portable FM radio receiver. The filter design is based on the $\delta$ - QR -I SC $N$-path technique of Chapter 5 , which, through a process of orthogonal hardware modulation, is tolerant of some path mismatch. All the required circuitry - including sample-and-holds and clocks - are placed on board the IC to get a complete picture of the performance of the filter. Firstly, in this section, the radio IF BPF is placed in a system context and the required specifications are explained for embedding in a complete integrated solution. Next, the circuit design and layout are presented followed finally by the lab measurement results.

### 6.2.1 System Context

Practically every FM receiver made today makes use of at least one 10.7 MHz ceramic BPF for channel selectivity [64]. Some high quality applications, such as car radio, even require 4 ceramic BPFs [66]. This BPF must distinguish the wanted FM band of 200 kHz from the broadband IF signal after demodulation in the RF front-end. Although ceramic filters have the advantages of being cheap and reliable, they cost printed circuit board (PCB) area and require input and output pins. Although passive, they require input and output buffering and are susceptible to pick-up from the PCB. For car radio, as mentioned, the chain of 4 BPFs requires 8 pins and buffers.

CMOS technology offers the possibility of integration of both receiver and digital processing circuitry on a single chip if an extremely accurate and high dynamic range CMOS IF filter is available. Since the RF gain control range is limited in CMOS designs, an IF filter that can provide some of this gain control is preferred. Fig. 6.16 shows a general simplified FM receiver chain, including the possible application of the SC filter. All radio receivers have a readily available crystal reference frequency, so the clock generation for the SC BPF is not a significant overhead. Some pre-filtering is needed, as was explained in section 5.3, in order to attenuate those frequency components that can alias in to the filter band. The BPF contains a distributed coarse gain control with a range of 36 dB in steps of 6 dB . The fine gain control with


Fig. 6.17 Functional design of Radio IF SC BPF.
a range of 6 dB (in steps of 0.2 dB ) can be implemented in the subsequent digital hardware. The possibility of integrating the ceramic BPF function gives the designer extra flexibility - a centre frequency of 10.7 MHz is no longer necessary and another more convenient frequency could be chosen. Note, however, a 10.7 MHz centre frequency is chosen here for the sake of direct comparison with existing 10.7 MHz filter solutions. Unlike a ceramic filter, an active BPF has no insertion loss (containing even a gain in this case), but it has a limited dynamic range. The integrated BPF should not contribute significantly to a reduction in performance of the fully integrated receiver compared to one in which an external ceramic filter is used.

The typical specifications of such a ceramic filter are $10.7 \mathrm{MHz} \pm 30 \mathrm{kHz}$. The 3 dB bandwidth is 200 kHz [66]. A group delay variation of $<1 \mu \mathrm{~s}$ within this bandwidth is acceptable for FM demodulation. An integrated version of this filter should, therefore, have a $Q$ higher than 53. It was also estimated that, for portable radio applications, the intermodulation-free dynamic range should be greater than 70 dB . Since chip area and power dissipation are very important for low cost portable radio applications, the goal was set of maximizing performance for a chip area of under $1 \mathrm{~mm}^{2}$ in $0.6 \mu \mathrm{~m}$ CMOS and a dissipation of circa 15 mW .

### 6.2.2 Design of Radio IF Filter Circuitry

The block schematic of the SC IF filter, together with peripheral circuitry, is depicted in Fig. 6.17. A single $2^{\text {nd }}$ order BPF with a $Q$-factor of 55 would have a bandwidth that is too sensitive to process variations, so instead the $Q$-factor has been spread over a cascade of three identical fully differential $2^{\text {nd }}$ order BPF sections. Since the centre frequency $f_{0}$ is principally dependent on the clock, $N$-path $\delta$ - QR BPF sections can be cascaded while still maintaining a very accurate centre frequency for the overall filter. A cascade of standard SC biquad filters, on the other hand, would show too high a centre frequency sensitivity. In general, for $k$ cascaded $2^{\text {nd }}$ order


Fig. 6.18 Radio IF SC filter design.
sections, the $Q$ of each section is given by (see Appendix):

$$
\begin{equation*}
Q_{\text {sect }}=Q_{t o t} \cdot \sqrt{2^{\frac{1}{k}}-1} \tag{6.7}
\end{equation*}
$$

For $k=3, Q_{\text {sect }}$ should be 28 . Each BPF section provides a selectable gain of $0 \mathrm{~dB}, 6 \mathrm{~dB}$ and 12 dB for use by the IF AGC. The filter is preceded by a track-and-hold (T\&H) to allow for accurate sampling of the wide-band continuous-time input signal. Finally, a sample-and-hold buffer $(\mathrm{S} \& \mathrm{H})$ is added for measurement purposes. All stages are driven by an on-board 3phase clock.

### 6.2.2.1 SC Filter Design

A second order $(n=2) N$-path BPF requires $N=3$, as discussed in section 5.3. With path mismatch, frequency components around $1 / 3 f_{0}$ and $5 / 3 f_{0}$ fold back in attenuated form around $f_{0}$. This can be reduced by a simple pre-filter. With $n=2$, the sample frequency of the radio IF BPF is $f_{S}=4 f_{0}=42.8 \mathrm{MHz}$, in which the two poles are placed at exactly $z= \pm j r$. The filter is realized based on delta-charge redistribution in order to create a low sensitivity $Q$.

In Fig. 6.18, the circuit schematic of one 3-path BPF section is depicted [P.6]. It makes use of the $\delta-Q R-I$ stage of Fig. 5.15, in which the amplifier is shared between the paths. The input signal is sampled on $C_{a}$, while the negative output signal is sampled on $C_{b}$. After two sample clock periods, the charges on both these capacitors are combined passively by switching both capacitors in parallel. The combined capacitors $C_{a}, C_{b}$, are also placed in the feedback loop of an OTA in order to buffer the voltage on these capacitors for read out. The voltage


Fig. 6.19 Selectable gain control for IF AGC.
transfer function can be written in the $z$-domain as:

$$
\begin{equation*}
H(z)=\left(1-r^{2}\right) \cdot \frac{z^{-2}}{1+r^{2} \cdot z^{-2}}, \tag{6.8}
\end{equation*}
$$

where

$$
\begin{equation*}
r=\left(\frac{C_{b}}{C_{a}+C_{b}}\right)^{\frac{1}{2}} . \tag{6.9}
\end{equation*}
$$

The pole displacement factor $r$, and hence the $Q$, is determined by a simple ratio of capacitors $C_{a}, C_{b}$. A $Q$ of 28 per BPF section requires $C_{b}$ to be 20 times larger than $C_{a}$. To make $Q$ less sensitive to process variations, $C_{b}$ is created from 20 parallel $C_{a}$ capacitors, each with its own set of switches. A $C_{a}$ of 140 fF is chosen based principally on $k T / C$ noise considerations.

The BPF presented here is capable of providing a more accurate transfer function than previous $N$-path filters [54], or parallel switched biquads [70]. This increased accuracy is because (a) delta-charge redistribution is used in which the filter action occurs through the passive redistribution of charge, from which the filter transfer arises; (b) orthogonal hardware modulation improves signal integrity; (c) only a single transfer of charge is needed between input and output, making $f_{0}$ and $Q$ less sensitive to settling inaccuracy; (d) the $Q$ is determined by a simple ratio of capacitors $C_{a}, C_{b}$, making the $Q$ less sensitive to capacitor spreads; (e) BPF sections can be easily cascaded for increased selectivity while still maintaining low $f_{0}$ and $Q$ sensitivities.

### 6.2.2.2 Selectable Gain Control

The BPF section has a nominal 0 dB gain at $f_{0}$. It is possible to multiply up the filter gain without the need for an extra amplifier. Instead, one or more $C_{a}$ capacitors sample the input signal


Fig. 6.20 Track-and-Hold.
and transfer their charge to output capacitor combination $C_{a}+C_{b}$, as shown in Fig. 6.19. In each BPF section, a gain of $0 \mathrm{~dB}, 6 \mathrm{~dB}$ or 12 dB can be selected. For the total filter, this means a potential programmable gain of 0 dB to 36 dB in steps of 6 dB . In order to avoid noise and distortion variations with each gain setting, the impedance seen at the BPF OTA input is not allowed to vary with the gain setting. This is achieved by replacing those $C_{a}$ capacitors that switch between the input signal and the OTA input with dummy $C_{a}$ capacitors that switch between the reference voltage and the OTA input. Similarly, the impedance at the output of the stage preceding the filter section is kept constant by maintaining the switching of all the $C_{a}$ capacitors, even if some of these capacitors are not used for the subsequent gain control.

### 6.2.2.3 Track-and-Hold

The T\&H has been designed for low distortion and low noise. The circuit diagram is shown in Fig. 6.20. It is again a fully differential 3-path construction. Only NMOS switches are used, with the input switches being designed extra large $(15 / 0.6)$ to reduce sensitivity to channel resistance modulation. Each sampling branch has a small switch (3/0.6) connected to $V_{\text {ref }}$, the turn-off time of which is controlled by a single fast turn-off early clock ( $\phi^{*}$ ) switching at frequency $f_{s}$. In this way, clock feedthrough and non-uniform sampling are reduced significantly. In addition, the need for exact phase matching of clocks $\phi_{1-3}$ is avoided. The noise is kept low by choosing $C_{s}$ to be 400 fF . Note that the measurement $\mathrm{S} \& \mathrm{H}$ is made in a similar way to the T\&H, except that extra OTAs have been placed in parallel in order to drive the chip output capacitance. The S\&H design has been optimized to guarantee a good linear settling response under nominal signal conditions. Some slewing cannot be avoided, particularly for large signals ( $>0.5 \mathrm{~V}_{\mathrm{pp}}$ ).


Fig. 6.21 Dual-input differential transconductance amplifier for Radio IF BPF.

### 6.2.2.4 Amplifier

A single-stage dual-input telescopic OTA is used to realize all the amplifiers, as depicted in Fig. 6.21 and presented in section 4.2.2. The NMOS and PMOS input stages are connected together in this design and not separated out as previously in the Cloche BPF of section 6.1. This is because, in this design, with the use of a compact poly-poly capacitor option, the extra routing that would be needed to connect up the split capacitors and switches would take up too much area relative to the area taken up by each capacitor. The DC tail current NMOS transistor to $V_{s s}$ is removed for two reasons. Firstly, a single low $V_{r e f}$ of 1 V can be chosen for the input and output sides, meaning small NMOS-only switches can be used with reduced on-resistance modulation and reduced signal dependent clock feedthrough. Secondly, no separate commonmode feedback (CMFB) circuitry is needed, since the NMOS differential stage has inherent CMFB control [67]. The advantages of this are that the OTA can settle very quickly without being affected by the response of an external CMFB circuit; the power is kept down, since the BPF doesn't have to drive the extra load capacitors needed to sense the output voltage for a CMFB control circuit, and the dissipation of such extra circuitry is avoided. The maximum output signal swing for proper operation of the OTA, assuming single PMOS and NMOS cascodes, is given by $\pm\left(V_{D D}-3 \cdot V_{o n_{p}}-2 \cdot V_{o n_{n}}\right)$. The swing becomes severely limited, however, when equal input and output references are chosen. In this case, $V_{r e f}$ must be chosen as $\left(V_{T_{n}}+V_{o n_{n}}\right)$. Now the output swing becomes just $\pm\left(V_{T_{n}}-V_{o n_{n}}\right)$, which in the case of the designed OTA is $\pm 0.6 \mathrm{~V}$. This is adequate, however, for radio IF processing. Furthermore, with a supply of 3.3 V , it is still possible to create a cascoded single-stage amplifier with a DC
(a)

(b)


Fig. 6.22 Clock circuitry (a) with latch circuit (b).
gain of greater than 1000. Special attention must be paid to the biasing, though, to ensure that all transistors remain optimally biased into saturation (with a nominal $V_{\text {on }}$ of just under 200 mV ), even for varying supply, process and temperature conditions. The OTA has been simulated to have an open-loop DC gain greater than 61 dB and a $G B W$ greater than 125 MHz for a 3.5 pF differential load.

### 6.2.2.5 Clock

The clock generator circuitry, shown in Fig. 6.22, has been placed on chip together with the SC filter. The reference clock is divided by three, producing three $120^{\circ}$ phase shifted clocks $\phi_{1-3}$ with 1:2 duty cycles. The early sampling clock $\phi^{*}$ always switches off earlier (by about 4 ns ) than each of $\phi_{1-3}$. The loading and routing of each of the clocks are the same for good mutual matching. The total clock circuitry, including buffer drivers, consumes only 4.2 mW from a 3.3 V supply.

### 6.2.2.6 Layout

The SC radio IF filter is integrated using a $0.6 \mu \mathrm{~m}$ double-poly double-metal, 5 V analogue CMOS technology $\left(V_{T_{n_{0}}}=0.75 \mathrm{~V}\right)$ with high resistance substrate. A chip micrograph can be seen in Fig. 6.23. The area of the three BPFs, T\&H and clock, is $0.69 \mathrm{~mm}^{2}$. Strict matching of the three paths of each BPF section is maintained. The crossing of sensitive nodes (e.g. the OTA inputs) with clock signals is avoided. There are no overlaps between the OTA inputs and


Fig. 6.23 Chip micrograph of 10.7 MHz Radio IF SC BPF.
outputs, and the analogue input signal is kept away from all other signal nodes to avoid crosstalk signal distortion. The clocks in Metal 1 are transported over the chip much like coax cables, enclosed by Poly and Metal 2 layers. Current flow is kept within the cables and not allowed to return via the substrate. In this way, all signal nodes are kept clean of any clock interference.

### 6.2.3 Measurement Results

All the measurements were carried out with a 3.3 V supply and 42.8 MHz clock. Measured for 25 samples of the same batch, the $f_{0}$ is 10.6784 MHz (instead of 10.7 MHz ) with a $3 \sigma$ peak-peak variation of just $\pm 0.024 \%$; the $Q$ is $55.1 \pm 1.0 \%$ ( $3 \sigma$ ). The small shift downwards in centre frequency is caused by the limited DC gain of the OTA in combination with the extra input capacitance at its input terminals from all the switched gain control capacitors. The frequency transfers for gain settings of 0 to 36 dB in steps of 6 dB are shown in Fig. 6.24. The gain deviates no more than $1 \%$ from the target value, apart from a fixed attenuation of about 0.6 dB due to settling errors. A zoom-in on the $f_{0}$ deviation for the 0 dB setting can be seen in Fig. 6.25. The measured group delay is shown in Fig. 6.26, where it can be ascertained that the in-band group delay variation is less than $0.5 \mu \mathrm{~s}$, meeting the requirements of portable FM radio applications.

In Fig. 6.27, a plot is given of the measured $1 \% 3^{\text {rd }}$ order intermodulation distortion (IM3) for two $0.5 \mathrm{~V}_{\mathrm{pp}}$ input signals at frequencies of $f_{0} \pm 7.5 \mathrm{kHz}$. The total noise measured at the output is $226 \mu \mathrm{~V}_{\text {RMS }}$, resulting in a dynamic range of 58 dB for $1 \% \mathrm{IM} 3$. It was found that the measurement $S \& H$ made a significant contribution to the total distortion. Since the $S \& H$ is not considered part of the application of the IF BPF, as noted in section 6.2.1, the dynamic


Fig. 6.24 Filter transfer plots for different gain settings.


Fig. 6.25 Measured $f_{0}$ deviation from 10.7 MHz .
range when corrected for this is greater than 61 dB .
An important item for $N$-path filters is the matching performance. As this filter is based on a 3-path construction, any path mismatch causes $1 / 3 f_{s}$, or $4 / 3 f_{0}$, sub-sampling. Components at $1 / 3 f_{0}, 5 / 3 f_{0}, 7 / 3 f_{0}$, etc. are mirrored in attenuated form to $f_{0}$. A measurement signal at $1 / 3 f_{0}$ isn't a good choice because the $3^{\text {rd }}$ harmonic of the signal generator appears directly at $f_{0}$. For this reason, the next possible frequency is used: $5 / 3 f_{0}$. Fig. 6.28 shows the combined plot of the input at $5 / 3 f_{0}(17.83 \mathrm{MHz})$ and the output at $f_{0}(10.7 \mathrm{MHz})$ for a single measurement. The signal level at $f_{0}$ is found to be less than $0.05 \%$ of the input level for all 25 samples measured. Another frequency component can be found at $1 / 3 f_{s}(14.27 \mathrm{MHz})$ and is caused by a slight timing mismatch between the three clock phases. However, the magnitude is very small ( 400 $\mu \mathrm{V}_{\text {RMS }}$ ) and constant and won't be a problem for FM radio. The CMRR has been measured to be more than 55 dB and the PSRR to be more than 29 dB within the passband of the filter.
The total power consumption, including the T\&H and clock circuitry, is 16.1 mW , correspond-
ing to a power per pole of just 2.7 mW . All the measurement results are summarized in Table 6.2 together with a performance comparison with some previous designs. For the portable radio application intended for this BPF, cost price (circuit area) and power consumption are important design constraints, as discussed in section 6.2.1. For these design constraints, the measured dynamic range of 61 dB does not meet the required dynamic range, set at a minimum of 70 dB . One way to improve the $S N R$ for nominal signal levels ( 0 dB gain setting) is to remove the dummy capacitors at the BPF OTA input (section 6.2.2.2) - this would give a 6 dB improvement in $S N R$. Furthermore, an increase in $S N R$ can only come at the expense of increased die area and power. For instance, the $S N R$ of the BPF can be increased by 3 dB for every doubling of the value of the signal capacitors. The $g_{m}$ 's of the BPF OTAs must then also be doubled to maintain the same settling accuracy. This can be done by doubling the area of the input transistors of the OTAs and doubling their current consumption.

Note that despite the realization of this design in a somewhat older CMOS technology $(0.6 \mu \mathrm{~m})$, the techniques used are still just as valid. Indeed, realizing this 10.7 MHz filter solution in a modern day process would make even better results possible. Despite the older technology, the specifications achieved are still unsurpassed to this day! An example of a more recent design in $0.35 \mu \mathrm{~m}$ CMOS is shown in the second column of Table 6.2 [71]. While the paper quotes this design for comparison, the specifications achieved lag this work.

Table 6.2 Measured Radio IF Filter Performance and Comparison to Other Solutions

|  | This design | Silva-Martinez[71] | Nagari [72]] | Song [73] |
| :---: | :---: | :---: | :---: | :---: |
| IC Technology | $0.6 \mu \mathrm{~m}$ CMOS | $0.35 \mu \mathrm{~m} \mathrm{CMOS}$ | $1.2 \mu \mathrm{~m}$ CMOS | $2.25 \mu \mathrm{~m}$ CMOS |
| Area | $0.69 \mathrm{~mm}^{2}$ | $0.84 \mathrm{~mm}^{2}$ | $1.6 \mathrm{~mm}^{2}$ | $2 \mathrm{~mm}^{2}$ |
| Filter order | $6(\mathrm{SC})$ | $6(\mathrm{SC})$ | $2(\mathrm{SC})$ | $6(\mathrm{SC})$ |
| centre frequency $f_{0}$ | 10.7 MHz | 10.7 MHz | 10.7 MHz | 10.7 MHz |
| $f_{0}$ deviation $\Delta f_{0}$ | $-0.2 \%$ | $-0.5 \%$ | $-1 \%$ | $-3 \%$ |
| Max measured $f_{0}$ variance | $0.024 \%(3 \sigma)$ |  | $\pm 0.4 \%$ | $\pm 0.4 \%$ |
| $Q$ factor | 55 | 23 | 10 | 27 |
| In-band group delay var, $\Delta \tau_{0}$ | $0.56 \mu \mathrm{~s}$ |  |  |  |
| Total output noise | $226 \mu \mathrm{~V}_{\text {RMS }}$ | $295 \mu \mathrm{~V}_{\mathrm{RMS}}$ | $707 \mu \mathrm{~V}_{\mathrm{RMS}}$ | 1.1 mV RMS |
| Dynamic range (1\% IM3) | 61 dB | 58 dB | 58 dB | 34 dB |
| Supply voltage | 3.3 V | 3 V | 3 V | 10 V |
| Power dissipation (w/o clock) | 12 mW | 54 mW | 23 mW | 500 mW |
| Power/pole | 2.7 mW | 9 mW | 11.5 mW | 83.3 mW |



Fig. 6.26 Passband group delay characteristic.


Fig. 6.27 Measured 1\% IM3 for two signals of $0.5 V_{p p}$ (including $S \& H$ distortion).

### 6.3 Conclusions

Low power and very accurate SC bandpass filters have been proved feasible in CMOS for both video and radio embedded system applications. A highly linear (79dB dynamic range) video bandpass filter with tight specifications on centre frequency $(4.3 \mathrm{MHz})$ and $Q$ (16) was designed in a two metal standard $0.8 \mu \mathrm{~m}$ CMOS process. Despite the large amount of parasitic capacitance that must be charged and discharged each clock cycle, a power efficient implementation is possible through the use of a delta-charge redistribution filter architecture. Furthermore, the use of a single-stage dual-input telescopic OTA is highly efficient in terms of current consumption and helps to keep the noise low. The filter can handle signals up to $6 \mathrm{~V}_{\mathrm{pp}}$ for a 5 V supply voltage and is suitable for the processing of video signals which can have large variations in signal amplitude.


Fig. 6.28 Path mismatch measurement for $f_{0}$ of 10.7 MHz .

A low power and very accurate $6^{\text {th }}$ order SC bandpass filter has been proved feasible in CMOS for 10.7 MHz radio IF selectivity. Through the combination of the $N$-path technique, orthogonal hardware modulation and SC delta-charge redistribution, it is possible to design a bandpass filter that is more accurate than ceramic filters for radio applications. In addition, it is possible to combine a selectable gain with each BPF section, in which the total noise and distortion is independent of the gain setting. The high $Q\left(55\right.$ at $\left.f_{0}\right)$ and centre frequency accuracy ( $f_{0}$ of $10.6784 \mathrm{MHz} \pm 0.024 \%$ ) are not achieved using previous methods for integrated radio IF filters. The complete chip, including clock and track-and-hold, consumes 16 mW at 3.3 V and this too is much less than recently reported SC and CT IF filters. Indeed, this power is offset by the elimination of the power needed in current designs to drive off-chip filters. However, the dynamic range of 61 dB is not yet good enough for portable FM radio applications and needs improving to about 70 dB (at the expense of extra power and die area). Note that this design was one of the "conference highlights" of the ISSCC in 2000 [P.5] and was covered extensively in the electronic press [69].

### 6.4 Appendix: Bandwidth Shrinkage of Cascaded Filter Stages

Consider a first order lowpass filter in the $s$-domain: it's transfer function is given by:

$$
\begin{equation*}
H_{\text {sect }}(s)=\frac{1}{1+\frac{s}{2 \cdot \pi \cdot f \cdot f_{b w(s e c t)}},} \tag{6.10}
\end{equation*}
$$

where $f_{b w(s e c t)}$ is the 3 dB fall-off frequency defining its bandwidth. The transfer function for a cascade of $k$ such stages becomes:

$$
\begin{equation*}
H_{t o t}(s)=\left(\frac{1}{1+\frac{s}{2 \cdot \pi \cdot f b w(s e c t)}}\right)^{k} . \tag{6.11}
\end{equation*}
$$

Denoting the bandwidth of all the cascaded stages by $f_{b w(t o t)}$, then the magnitude of the result-
ant filter drops off by $1 / \sqrt{2}$ at this frequency, i.e.

$$
\begin{gather*}
\left|H_{t o t}(s)\right|_{s \rightarrow j \cdot 2 \cdot \pi \cdot f_{b w(t o t)}}=\left|\frac{1}{1+j \cdot \frac{f_{b w(t o t)}}{f_{b w}(s e c t)}}\right|^{k}=\frac{1}{\sqrt{2}}  \tag{6.12}\\
\Rightarrow\left(\frac{1}{\sqrt{1+\frac{f_{b w(t o t)}}{f_{b w(s e c t)}}}}\right)^{k}=\frac{1}{\sqrt{2}} \tag{6.13}
\end{gather*}
$$

Hence, the total bandwidth of $k$ cascaded stages can be related to the bandwidth of a single stage by:

$$
\begin{equation*}
f_{b w(t o t)}=f_{b w(\sec t)} \cdot \sqrt{2^{\frac{1}{k}}-1} . \tag{6.14}
\end{equation*}
$$

Equation (6.14) can be generalized to include a bandpass filter, which in effect is formed by the shifting of the centre frequency of an equivalent lowpass filter from DC to the centre frequency $f_{0}$. Hence, the $Q$ per bandpass filter stage is related to the overall $Q$ of a cascade of $k$ such filter stages by:

$$
\begin{equation*}
Q_{\text {sect }}=Q_{t o t} \cdot \sqrt{2^{\frac{1}{k}}-1} \tag{6.15}
\end{equation*}
$$

## Chapter 7

## ADC Design At Black-Box Level

Up till this point, the thesis has focused on filtering for the application of proposed concepts for high-accuracy design using switched capacitors. Now the focus shifts to analogue-to-digital converter (ADC) design, which is the second most important application area for SC techniques. To start off, this chapter deals with the design of the ADC at the generic black-box level. Firstly, the most important performance specifications are explained and formulated. The signal processing of the ADC can be broken down into three basic functions, namely the anti-aliasing pre-filter, the sampler, and the quantizer. Although the anti-aliasing filter is not fundamental to the ADC operation, some form of analogue pre-filtering is almost always needed due to the sampled-data operation of the ADC. The signal path of the black-box ADC is shown in Fig. 7.1. Each of the ADC sub-blocks are examined and modelled, in this chapter, for how they affect the quality of the conversion process from analogue to digital. Finally, models are proposed to represent the ADC conversion efficiency. Limits are derived for the minimum signal-to-noise ratio and minimum power of the generic ADC.

### 7.1 ADC Black Box Representation

The function of an analogue-to-digital converter (ADC) is to convert an analogue signal, that is continuous in time and amplitude, into a digital signal that is discrete in time (sampled) and discrete in amplitude (quantized). The sequence of signal processing steps to create the ADC function is shown in Fig. 7.1. The analogue input signal, $x(t)$, is first bandlimited, $x_{a}(t)$, so as to ensure that the subsequent sampler cannot alias any input signal components back into the signal frequency passband of interest. Nyquist converters, which can digitize analogue signals right up to half the sampling frequency, $f_{s} / 2$, are widely used in communications applications and require the use of high quality lowpass anti-aliasing filters with flat passband, sharp transition band and linear phase for most of the Nyquist band. Aliasing can be detrimental to ADCs for communications application since unwanted spurs get aliased back into the passband which cannot be distinguished from the signal itself, reducing the dynamic range of the ADC accordingly. The sampler succeeding the anti-aliasing pre-filter produces a discrete-time representa-


Fig. 7.1 Basic operations pertaining to an $A D C$.
tion, $x_{s}[m]$, of the bandlimited signal $x_{a}(t)$. Finally, $x_{s}[m]$ is quantized in amplitude by the $N$ bit quantizer to become $x_{q}[m]$ and encoded as a sequence of $N$ bits in the binary encoder, $x_{d}$. The sampler, quantizer and binary encoder are fundamental operations pertaining to the ADC, while the pre-filter is a necessary pre-requisite to bandlimit the input and ensure high quality performance of the ADC.

The output of the $N$-bit ADC, $x_{d}$, is a bit sequence ranging from the MSB (most significant bit) to the LSB (least significant bit). It is represented as:

$$
\begin{equation*}
x_{d}=\left\{b_{N-1}, b_{N-2}, \ldots, b_{1}, b_{0}\right\} . \tag{7.1}
\end{equation*}
$$

Note that depending on the quantizer, the LSB may appear first and the MSB last. The FS (full scale range) is the maximum analogue input range that can be quantized [74]. An ideal $N$-bit quantizer divides the $F S$ into $2^{N}$ uniform quantization levels, each with step size (or code width) $\Delta$. The quantization step size $\Delta$ represents the analogue equivalent of 1 LSB of the quantizer and is given by:

$$
\begin{equation*}
\Delta=\frac{F S}{2^{N}} . \tag{7.2}
\end{equation*}
$$

In practical realizations, the $F S$ is usually defined by a differential voltage reference range,

$$
\begin{equation*}
F S=V_{r e f_{p}}-V_{r e f_{n}} \tag{7.3}
\end{equation*}
$$

where $V_{\text {ref }_{p}}$ and $V_{\text {ref }}^{n}$ form a stable differential voltage reference. The equivalent analogue value of any digital code between 0 and $F S$ is given by:

$$
\begin{equation*}
D=F S \cdot \sum_{i=0}^{N-1} b_{i} \cdot 2^{-N+i} \tag{7.4}
\end{equation*}
$$

The transfer characteristics are shown in Fig. 7.2 for a 10-bit quantizer in both unipolar and bipolar modes. Unipolar mode in Fig. 7.2(a) is defined for a unipolar input ranging from 0 to $F S$, while bipolar mode in Fig. 7.2(b) is defined for a bipolar input going from 0 to $-F S / 2$ and 0 to $+F S / 2$. The characteristics are defined here with the quantizer threshold levels spread evenly across the full scale range of $F S$ to give $2^{N}$ codes, or $2^{N}-1$ evenly spaced thresholds. This is the way the codes have been defined for the new ADCs presented in Chapters 8 and 9 .
(a)

(b)


Fig. 7.2 ADC Characteristics with (a) unipolar and (b) bipolar.

The use models of unipolar and bipolar quantizers will be presented in Chapter 10.

### 7.2 Performance Specifications

The quality of an ADC is measured by way of (i) its static or DC performance and (ii) its dynamic or AC performance. High accuracy measurement ADC applications require very good static performance, whereas communications applications place much more emphasis on the dynamic performance. The most common and meaningful specifications are presented here.

### 7.2.1 Static Error Specifications

The key to understanding the static performance of ADCs is to compare the ideal and nonideal transfer characteristics for DC signals. Static errors usually arise due to mismatch in circuit components and non-symmetry in the IC layout. Measurement results must show performance at high and low temperatures and supply voltages. The different forms of static error to be expected in an ADC realization are explained briefly in the following.

### 7.2.1.1 Offset and Gain Errors

Gain and offset errors should include all possible sources including, for instance, the reference generation. These errors are shown in Fig. 7.3 for a unipolar input range - they have similar effect to errors which occur in an analogue amplifier. The transfer characteristic is of the form $D=O+G \times A$, where $D$ is the output digital code, $A$ the analogue input, $O$ the offset, and $G$ the gain error. For a unipolar ADC, $O$ is ideally 0 , while for a bipolar ADC, $O$ is ideally -1 MSB. Thus, the offset error is given by how much $O$ deviates from its ideal value in LSBs. The gain error for ADCs is defined by the error at full-scale minus the offset error, as shown in Fig.


Fig. 7.3 ADC gain and offset characteristics.
7.3. It may be measured in LSBs or as a percentage of full-scale. Usually the ADC is used in combination with a microcontroller, or DSP, and as such the offset and gain errors can be calibrated away. However, the dynamic range, i.e. the effective analogue input range before overranging the ADC , is reduced as a consequence.

### 7.2.1.2 Differential Non-linearity (DNL)

The DNL error refers to how much a code width deviates from the ideal value of 1 LSB. The definition of the instantaneous DNL [75] is:

$$
\begin{equation*}
D N L_{i}=\frac{x_{a}\left(Q_{i+1}\right)-x_{a}\left(Q_{i}\right)}{\Delta}-1, \quad i=0, \ldots 2^{N}-2 \tag{7.5}
\end{equation*}
$$

with $Q_{i}$ and $Q_{i+1}$ adjacent transition levels for analogue input $x_{a}$. When one refers to the DNL of an ADC, the maximum DNL is usually implied, be it positive or negative. Examples of DNL error are shown in Fig. 7.4(a), where the non-ideal transfer characteristic is set against the ideal stair-case ADC transfer function. The quantization error produced by the non-ideal ADC transfer is shown in Fig. 7.4(b) and it is set against the ideal sawtooth quantization error expected of an ideal ADC with 0 DNL error. Note the quantizer characteristic is centred in such a way that 0 analogue input gives 0 digital output and the digital output codes are centred around each LSB starting at 0,0 . The ideal sawtooth varies now between $\pm 1 / 2$ LSB. It is important that the ADC produces no missing codes in order to guarantee monotonic behaviour. This implies the maximum DNL error must always be less than +/- 1 LSB.


Fig. 7.4 (a) Ideal and non-ideal ADC transfer functions (3-bit) (b) Quantization error functions.

### 7.2.1.3 Integral Non-linearity (INL)

The INL error refers to the maximum deviation of the actual ADC transfer function from a straight line drawn through the first and last code transitions after correction for offset and gain errors. This is often referred to as end-point INL and gives a more pessimistic but useful estimation of the non-linearity than referring the linearity of the ADC characteristic to an arbitrary best fit curve drawn through the output codes (best-fit INL). Generally, the best-fit INL is only half that of the end-point INL and is not so widely used anymore to specify professional data converters. The INL is defined by the accumulation of DNL errors over the complete ADC characteristic [75]:

$$
\begin{equation*}
I N L=\sum_{i=0}^{N-1} D N L_{i} . \tag{7.6}
\end{equation*}
$$

### 7.2.2 Dynamic Error Specifications

The dynamic performance of an ADC is obtained by examining its AC characteristics when a spectrally pure sinewave is applied to the input. This is best done by performing an FFT on the output data and examining the spectrum for artefacts such as noise and distortion. The most important dynamic specifications are explained briefly in the following.

### 7.2.2.1 Signal-to-Noise Ratio (SNR)

The $S N R$ is specified for full scale input amplitude and should include all noise contributions in the band of interest - usually up to the Nyquist frequency $\left(f_{s} / 2\right)$. This is summarized as:

$$
\begin{equation*}
S N R=10 \times \log \left(\frac{\text { Max Signal Power }}{\text { Total Noise Power in Freq Band of Interest }}\right) . \tag{7.7}
\end{equation*}
$$

A variant of this definition is to include the power of the distortion components with the noise power, and this is called the signal-to-noise and distortion ratio, or $S N D R$. Typically the $S N R$ is dominated by quantization noise and circuit thermal noise but also includes other noise sources such as noise emanating from the references and power supplies, glitches, measurement setup noise, etc. See section 7.7.1 for analysis of $S N R$.

### 7.2.2.2 Effective Number of Bits (ENOB)

For real ADCs, the ENOB is often used instead of $S N R$ or $S N D R$, since it gives a better indication of ADC accuracy: it is defined at a specific input frequency and sampling rate. The ENOB is defined to include all measured sources of noise and distortion in an ADC:

$$
\begin{equation*}
E N O B=\frac{S N R_{\text {measured }}-1.76}{6.02} \tag{7.8}
\end{equation*}
$$

### 7.2.2.3 Total Harmonic Distortion (THD)

The THD of an ADC gives the ratio of the power of all the harmonics of the input signal to the power of the fundamental. It is usually specified up to a certain number of harmonics, k , with k usually in the range of 6 to 10 (i.e., up to the $10^{\text {th }}$ harmonic). Furthermore, it assumed that the input signal is close to full scale. The $\mathrm{k}^{\text {th }}$ order THD is defined as:

$$
\begin{equation*}
T H D_{k}=10 \times \log \left(\sum_{i=2}^{k} \frac{A_{i}^{2}}{A_{1}^{2}}\right), \tag{7.9}
\end{equation*}
$$

which is expressed in negative dBs with respect to the fundamental, $A_{1}$.

### 7.2.2.4 Spurious Free Dynamic Range (SFDR)

The $S F D R$ is widely used as a measure of the quality of high-speed ADCs for communications applications. It is defined as the ratio of the power of the signal fundamental tone to the power of the largest spurious component in a certain frequency range:

$$
\begin{equation*}
S F D R=10 \times \log \left(\frac{A_{1}^{2}}{A_{\text {spur }}^{2}}\right), \tag{7.10}
\end{equation*}
$$

with $A_{1}$ the RMS value of the fundamental and $A_{\text {spur }}$ the RMS value of the largest spurious component. The $S F D R$ is expressed either as a function of the signal fundamental amplitude $(\mathrm{dBc})$ or as a function of the ADC full scale (dBFS). The frequency range is almost always the Nyquist band from 0 to $f_{s} / 2$ in Nyquist ADCs. The $S F D R$ is a function of the amplitude and frequency of the input tone as well as the sampling frequency.

In a well designed ADC system, the spurious component will be a harmonic of the fundamental and is usually well below the level of the noise floor. The SFDR is a very important measure for ADCs in IF bandpass applications or in sub-sampling applications, since the spurious tone can be interpreted as an adjacent channel.

### 7.2.2.5 Intermodulation Distortion (IMD)

ADCs required for radio receiver and transmitter applications are best further characterized for linearity by measuring their $I M D$. Generally two-tone intermodulation is used, where two tones at frequencies $f_{1}$ and $f_{2}$ with amplitudes slightly less than $F S / 2$ are applied to the ADC. The FFT is examined for spurious tones at frequencies of:

$$
\begin{equation*}
f_{I M D_{m, n}}=\left[a \times f_{1} \pm b \times f_{2}\right]_{\text {modulof } f_{s}}, \tag{7.11}
\end{equation*}
$$

where $a$ and $b$ are positive integers greater than or not equal to 0 . The $I M D$ is calculated as:

$$
\begin{equation*}
I M D=10 \times \log \left(\frac{A_{I M D}^{2}}{A_{1}^{2}}\right), \tag{7.12}
\end{equation*}
$$

where $A_{1}$ represents the amplitude of either of the original input tones and $A_{I M D}$ is the amplitude of the IMD product. Generally, the IMD of an ADC is specified for a third order product which can fall in band, such as $2 f_{1}-f_{2}$ or $2 f_{2}-f_{1}$.

### 7.3 Anti-Aliasing Pre-Filter

The function of the anti-aliasing pre-filter is to band-limit the analogue input signal in such a way that any signal components which fold back within the signal bandwidth after sampling are well below the quantization noise level. In the interests of low cost, small board space, low power and design flexibility, a simple lowpass pre-filter is often preferred. The bandwidth of the pre-filter is generally much less than the Nyquist bandwidth to facilitate a wide transition band [76]. Over-sampling by the sampler combined with digital decimation and down-sampling immediately after the ADC can then be used. Part of the decimation and down- sampling can, of course, be performed in the analogue sampled data (ASD) domain directly after the sampler through the use of SC filtering, as discussed in Chapter 5. Digital and/or ASD filtering is accurate, enabling the creation of accurate notch and bandpass characteristics. A sharp transition band can be created with flat amplitude and linear-phase in the passband. Integrated dig-


Fig. 7.5 Aliasing in the time domain with a sampling frequency of 1 MHz and signal frequencies of 0.1 and 0.9 MHz .
ital and ASD filters can be programmed for different characteristics depending on signal conditions and system specifications.

The sampling theorem of C.E. Shannon [77] states that any continuous-time signal can be completely recovered from its samples if, and only if, the sampling rate is greater than twice the signal bandwidth. Frequency folding caused by sampling creates sampled signal representations at frequencies $\left.f_{\text {in }}\right|_{\text {modulo }\left(f_{s}\right)}$ and $\left.\left(f_{s}-f_{\text {in }}\right)\right|_{\text {modulo( }\left(f_{s}\right)}$. Aliasing occurs when $f_{\text {in }}>f_{s} / 2$. This restriction on the frequency content of the signal $x_{a}(t)$ is illustrated with an example in Fig. 7.5. The signal frequency of 0.9 MHz sampled at a rate of 1 MHz cannot be distinguished from a signal frequency of 0.1 MHz due to undersampling giving rise to aliasing of 0.9 MHz back to 0.1 MHz .

Oversampling can be used to ease the specifications of the anti-aliasing pre-filter. Consider two cases of pre-filter shown in Fig. 7.6. For a given maximum signal bandwidth, $f_{b w}$, the filter dynamic range is determined by the attenuation achieved of input frequency components beyond the filter transition band given by $f_{s}-2 \times f_{b w}$. Clearly, as $f_{s}$ goes beyond $2 \times f_{b w}$, the required complexity of the pre-filter reduces dramatically. For instance, in Fig. 7.6(a), the filter characteristic is shown for when $f_{s}=3 \times f_{b w}$, while in Fig. 7.6(b) the required pre-filter characteristic is shown for when $f_{s}=6 \times f_{b w}$. The transition band to achieve the same dynamic range increases by a factor of 4 from $f_{b w}$ to $4 \times f_{b w}$ after doubling the sampling frequency.

High quality ADCs require a flat in-band frequency response to ensure no bits are lost due to attenuation across the signal bandwidth. Consider, for instance, the gain characteristic of a first order lowpass filter given by:

$$
\begin{equation*}
L(f)=\frac{L(0)}{\sqrt{1+\left(\frac{f}{f_{b w}}\right)^{2}}} . \tag{7.13}
\end{equation*}
$$

The gain loss in LSBs across the signal bandwidth is shown in Fig. 7.7, assuming an input sig-


Fig. 7.6 Anti-aliasing pre-filter characteristic for ADC with (a) sampling frequency $f_{s}$ and (b) sampling frequency $2 f_{s}$.
nal at full-scale amplitude. It can be seen clearly how very sensitive an ADC is to the roll-off in pre-filter gain characteristic. So even just buffering the input signal can produce a significant deterioration in ADC quality because of roll-off across the buffer bandwidth.

### 7.4 Sampling

Clean sampling is key to the accurate conversion of the analogue input signal to a sampleddata representation. Any inaccuracies here due to mis-timing of the sample clock edges lead directly to an inaccurate digital representation of the input signal. This is examined and quantified in this section.

### 7.4.1 Sampling Jitter

Generally, a high performance track-and-hold (T\&H) is used as a dedicated sampler to create an accurate analogue sampled data signal (discrete time) which is subsequently quantized by the ADC (discrete amplitude). For high-speed ADC applications, the sampling jitter or aperture jitter of the sample clock can have a big impact on performance [78]. Many applications, such as wideband radio, require sub-sampling of signals that are at frequencies beyond the sample clock frequency. Note, however, that once the signal is acquired by the sampler of a switched-capacitor ADC, clock jitter causes no further degradation of performance.

Consider an analogue waveform $x_{a}(t)$, shown in Fig. 7.8, which is sampled at a nominal


Fig. 7.7 Effective bit loss over filter bandwidth for different ADC resolutions.
instant in time, given by $t=t_{0}$. An error in the signal amplitude $\varepsilon_{\tau}$ arises from the uncertainty in the sampling moment given by $\tau$. This amplitude error is defined by:

$$
\begin{equation*}
\varepsilon_{\tau}\left(t_{0}\right)=x_{a}\left(t_{0}+\tau\right)-x_{a}\left(t_{0}\right) . \tag{7.14}
\end{equation*}
$$

Since the aperture uncertainty $\tau$ is very small compared to the time period between sample moments, (7.14) can be approximated by a first order Taylor expansion making the amplitude error proportional to the product of $\tau$ and the derivative (or slope) of the input signal at the sampling instant $t_{0}$ :

$$
\begin{equation*}
\varepsilon_{\tau}\left(t_{0}\right) \approx \tau \times \dot{x}_{a}\left(t_{0}\right) . \tag{7.15}
\end{equation*}
$$

The jitter noise power of the error amplitude $\varepsilon_{\tau}$ is obtained by getting its variance $\sigma_{J}^{2}$. Assuming the jitter has a Gaussian distribution with zero mean value, the jitter noise power becomes:

$$
\begin{equation*}
\sigma_{J}^{2}=E\left[\varepsilon_{\tau}^{2}(t)\right]=E\left[\tau^{2} \times \dot{x}_{a}^{2}(t)\right] \tag{7.16}
\end{equation*}
$$

With $\tau$ statistically independent of $\dot{x}_{a}(t)$, equation (7.16) can be simplified to:

$$
\begin{equation*}
\sigma_{J}^{2}=\sigma_{\tau}^{2} \times E\left[\dot{x}_{a}^{2}(t)\right], \tag{7.17}
\end{equation*}
$$

where $\sigma_{\tau}$ represents the RMS jitter.
Consider the specific case of sampling a sinusoidal input signal of frequency $f_{i n}$ and amplitude $A$, then

$$
\begin{equation*}
\dot{x}_{a}(t)=2 \pi f_{i n} A \cos \left(2 \pi f_{i n} t\right) . \tag{7.18}
\end{equation*}
$$

The average power of $\dot{x}_{a}{ }^{2}(t)$ is obtained by integrating its power spectral density $S_{\dot{x}}(f)$ over all of frequency, i.e.


Fig. 7.8 Analogue waveform sampled by clock with aperture jitter.

$$
\begin{equation*}
E\left[\dot{x}^{2}(t)\right]=\int_{-\infty}^{\infty} S_{\dot{x}}(f) d f \tag{7.19}
\end{equation*}
$$

The autocorrelation function, $R_{\dot{x}}(t, \tau)$, of $\dot{x}_{a}(t)$ is given by:

$$
\begin{align*}
R_{\dot{x}}(t, \tau) & =E\left[\dot{x}_{a}(t+\tau) \times \dot{x}_{a}(t)\right] \\
& =\left(2 \pi f_{i n}\right)^{2} \times \frac{A^{2}}{2} \times \cos \left(2 \pi f_{i n} \tau\right) . \tag{7.20}
\end{align*}
$$

The power spectral density is found by taking the Fourier transform of the autocorrelation function. Hence,

$$
\begin{equation*}
S_{\dot{x}}(f)=\pi^{2} \times f_{i n}^{2} \times A^{2} \times\left[\delta\left(f-f_{i n}\right)+\delta\left(f+f_{i n}\right)\right] . \tag{7.21}
\end{equation*}
$$

The total average jitter noise power is obtained using (7.17) and (7.19) to be:

$$
\begin{equation*}
\sigma_{J}^{2}=\sigma_{\tau}^{2} \times 2 \pi^{2} f_{i n}^{2} A^{2}, \tag{7.22}
\end{equation*}
$$

which is worst at the edge of the Nyquist interval, $f_{s} / 2$. The jitter noise power increases with the square of the signal amplitude, while the signal-to-jitter noise ratio becomes:

$$
\begin{equation*}
S J N R=\frac{\sigma_{S}^{2}}{\sigma_{J}^{2}}=\frac{A^{2} / 2}{\sigma_{\tau}^{2} \times 2 \pi^{2} f_{i n}^{2} A^{2}}=\frac{1}{\left(\sigma_{\tau} 2 \pi f_{i n}\right)^{2}}, \tag{7.23}
\end{equation*}
$$

which is independent of the input signal level. Thus, signal amplitude has no effect on the SJNR, since any changes in signal amplitude produce equal changes in jitter noise via the slew rate of the signal. Furthermore, the sampling frequency has no effect, since the amplitude error is only affected by the timing error of the sampling instant and not by how many sampling instants there are per unit time. Note that in an oversampling application, the $S J N R$ is reduced by the oversampling ratio $f_{s} / 2 f_{b w}$, since the jitter noise is spread out over the Nyquist interval,


Fig. 7.9 Effective bits achievable against peak-to-peak aperture jitter for different analogue signal frequencies.
whereas the band of interest extends only to $f_{b w}$. A decimation filter is used in the digital domain to remove frequency components above $f_{b w}$ before sub-sampling.

The $S J N R$ can be evaluated once the probability density function (PDF) of the jitter is known. Typically, the jitter has a near-Gaussian PDF where it is usually assumed that the peak-to-peak jitter is 6 times the RMS jitter, i.e.

$$
\begin{equation*}
\tau_{p p}=6 \times \sigma_{\tau} \tag{7.24}
\end{equation*}
$$

Note, for a near-Gaussian distribution, the standard deviation $\sigma$ is approximated as $1 / 6 \times$ ( $m a x$ value - min value), where $99.73 \%$ of all cases fall within the $\pm 3 \sigma$ of the mean. The SJNR can now be re-written as:

$$
\begin{equation*}
S J N R_{d B}=20 \log \left(\frac{6}{2 \pi f_{i n} \tau_{p p}}\right)=20 \log \left(\frac{1}{f_{i n} \tau_{p p}}\right)-0.4 \mathrm{~dB} . \tag{7.25}
\end{equation*}
$$

The effective bits of resolution are calculated using equation (7.8) and plotted in Fig. 7.9 against the peak-to-peak jitter for different values of the input signal frequency. The jitter power is inversely proportional to the square of the instantaneous input frequency but independent of the signal bandwidth. Therefore, sub-sampling applications, where a narrowband signal at several hundreds of MHz is shifted to lower frequencies through undersampling, can put a severe requirement on the sampling clock. So for instance, an input signal at 100 MHz subsampled to, and quantized at, 10 MHz must be sampled with a clock that has 10 times lower jitter than a signal that is directly sampled and quantized at 10 MHz in order to achieve the same number of effective bits.

### 7.4.2 Sample Clock Phase Noise Related to Allowable Sampling Jitter

Consider a sinusoidal input signal of frequency $f_{\text {in }}$ spanning the full scale range of the ADC (FS), i.e. $F S / 2 \times \sin \left(2 \pi f_{\text {in }} t\right)$. The maximum jitter occurs at the $t=0$ transition point of the sinusoid. The allowable peak-peak jitter is such that a maximum $\pm 1$ LSB error occurs with respect to the zero transition point. Hence, the maximum amplitude error span is $\pm \Delta$. The peak-peak jitter giving rise to this maximum amplitude error span is:

$$
\begin{align*}
\tau_{p p} & =\frac{2 \Delta}{\text { slope at } t=0}=\frac{2 \times F S / 2^{N}}{2 \pi f_{\text {in }} \times F S / 2} \\
& =\frac{1}{2^{N-1} \pi f_{\text {in }}} \tag{7.26}
\end{align*}
$$

The worst case jitter occurs for the fastest expected input signal. When sampling at the Nyquist rate $\left(f_{\text {clk }}=2 f_{\text {in }}\right)$, then:

$$
\begin{equation*}
\tau_{p p}=\frac{1}{2^{N-2} \pi f_{c l k}} . \tag{7.27}
\end{equation*}
$$

The phase noise of the clock is directly related to the jitter through its frequency, so that:

$$
\begin{equation*}
\phi_{p p}=2 \pi f_{c l k} \times \tau_{p p} \tag{7.28}
\end{equation*}
$$

After substituting equation (7.27) for $\tau_{p p}$, the peak-peak phase error becomes:

$$
\begin{equation*}
\phi_{p p}=2^{-N+3} . \tag{7.29}
\end{equation*}
$$

Note that the RMS phase noise is related to the RMS jitter through $\sigma_{\phi}=2 \pi f_{c l k} \times \sigma_{\tau}$. Assuming $6 \cdot \sigma$ jitter, the phase noise is also near-Gaussian with $\phi_{p p}=6 \cdot \sigma_{\phi}$. Thus, the RMS phase noise (in radians) is given by:

$$
\begin{equation*}
\sigma_{\phi}=2^{-N+2} / 3 \tag{7.30}
\end{equation*}
$$

The sample clock phase error depends only on the ADC resolution and is independent of sample frequency. It should be small compared to the quantization noise as discussed in section 7.6.

### 7.4.3 Sample Clock Noise Spectrum

Usually some kind of frequency synthesizer based on a phase locked loop (PLL) is used to generate a clock signal for sampling whose frequency is locked to an external off-chip reference frequency. This is modelled in Fig. 7.10. The PLL output frequency $f_{\text {clk }}$ is generated to be some multiple $M$ of $f_{\text {ref }}$. The ideal input to the controlled oscillator - for instance a voltage controlled oscillator (VCO) - is a DC voltage which exactly determines the output frequency. It is of the form:

$$
\begin{equation*}
f_{\text {out }}=f_{0}+K_{\text {osc }} \cdot V_{\text {ctrl }} \tag{7.31}
\end{equation*}
$$



Fig. 7.10 A typical PLL clock synthesizer.
where $f_{0}$ is the nominal centre frequency of the VCO for a zero valued control voltage. Noise in the phase detector is averaged out in the loop filter. A large time constant in the loop filter is often preferred, especially when a noisy but stable clock reference is used. The circuit noise of the VCO itself is suppressed in the narrow bandwidth of the PLL. Beyond the bandwidth of the PLL, the VCO is essentially free-running so that its noise is directly transferred to the output.

The phase noise originates mostly in the VCO [79]. It is modelled in Fig. 7.11(a) with equivalent input and output noise voltages of $v_{n_{i}}$ and $v_{n_{o}}$, respectively. The frequency of the VCO is modulated by $v_{n_{i}}$ which causes phase noise. The phase noise mechanism of the VCO in a narrow-band PLL can be modelled using narrow-band FM modulation. Consider one specific interfering signal of radial frequency $\omega_{m}$ and amplitude $\hat{v}_{n}$ :

$$
\begin{equation*}
v_{n}=\hat{v}_{n} \cdot \cos \left(\omega_{m} t\right) \tag{7.32}
\end{equation*}
$$

With $\hat{c}$ the amplitude of the VCO output and $K_{\text {osc }}$ the transfer gain and $M$ the frequency divider ratio, the VCO frequency is modulated by $v_{n}$ to become:

$$
\begin{align*}
v_{o s c} & =\hat{c} \cdot \cos \left[\omega_{c l k} t / M+\phi(t) / M\right] \\
& =\hat{c} \cdot \cos \left[\omega_{c l k} t / M+\int K_{o s c} \hat{v}_{n} \cos \left(\omega_{m} t\right) / M d t\right] \\
& =\hat{c} \cdot \cos \left[\frac{\omega_{c l k}}{M}\left(t+\frac{K_{o s c} \hat{v}_{n}}{\omega_{m} \omega_{c l k}} \cdot \sin \left(\omega_{m} t\right)\right)\right] . \tag{7.33}
\end{align*}
$$

The peak-peak phase jitter is obtained as:

$$
\begin{equation*}
\tau_{p p}=2 \frac{K_{o s c} \hat{v}_{n}}{\omega_{c l k} \omega_{m}} \tag{7.34}
\end{equation*}
$$

while the peak-peak phase error becomes:

$$
\begin{equation*}
\phi_{p p}=\frac{\omega_{c l k}}{M} \cdot \tau_{p p}=2 \frac{K_{o s c} \hat{c}_{n}}{M \omega_{m}} \tag{7.35}
\end{equation*}
$$

Note that although the jitter remains the same independent of the divider ratio $M$, the phase noise, on the other hand, is reduced by a factor of $M$.



Fig. 7.11 (a) Noise model of VCO, (b) phase change versus time for small single frequency interference, (c) single-sideband phase noise power spectral density.

Equation (7.33) for the VCO output is in the form of a frequency modulation (FM), and can be written as:

$$
\begin{equation*}
v_{o s c}=\hat{c} \cdot \cos \left[\omega_{c l k} t / M+\beta_{m} \cdot \sin \left(\omega_{m} t\right)\right], \tag{7.36}
\end{equation*}
$$

where $\beta_{m}=K_{o s c} \hat{v}_{n} / M \omega_{m}$ is the modulation index corresponding to peak phase deviation. This can be further expanded to become:

$$
\begin{equation*}
v_{o s c}=\hat{c} \cdot \cos \left(\omega_{c l k} t\right) \cdot \cos \left[\beta_{m} \cdot \sin \left(\omega_{m} t\right)\right]-\hat{c} \cdot \sin \left(\omega_{c l k} t\right) \cdot \sin \left[\beta_{m} \cdot \sin \left(\omega_{m} t\right)\right], \tag{7.37}
\end{equation*}
$$

which gives rise to the Bessel function representation of FM. For small values of $\beta_{m}(<0.1)$, (7.37) can be further simplified using $\sin (x) \approx x$ and $\cos (x) \approx 1$, as follows:

$$
\begin{align*}
v_{\text {osc }} & \approx \hat{c} \cdot \cos \left(\omega_{c l k} t\right)-\hat{c} \cdot \beta_{m} \cdot \sin \left(\omega_{c l k} t\right) \cdot \sin \left(\omega_{m} t\right) \\
& =\hat{c} \cdot\left[\cos \left(\omega_{c l k} t\right)-\frac{\beta_{m}}{2} \cdot \cos \left(\left(\omega_{c l k}-\omega_{m}\right) t\right)+\frac{\beta_{m}}{2} \cdot \cos \left(\left(\omega_{c l k}+\omega_{m}\right) t\right)\right] . \tag{7.38}
\end{align*}
$$



Fig. 7.12 Carrier-to-Noise ratio measured on oscillator spectral distribution.

The phase variation in time of the output clock signal with small single frequency interference is shown in Fig. 7.11(b), while its single-sideband power spectral density is shown in Fig. 7.11(c).

The relative height of the modulation frequency components compared to the carrier gives rise to the carrier-to-noise ratio $(C N R)$ of the oscillator - Fig. 7.12. The $C N R$ is the most frequent figure-of-merit for the quality of the clock source. It is defined by a power ratio of the carrier to the interference measured in a 1 Hz bandwidth at an offset of $f_{m}$ from the carrier frequency $f_{c l k}$ in $\mathrm{dBc} / \mathrm{Hz}$. Hence, (using radial frequencies):

$$
\begin{equation*}
C N R\left(\omega_{m}\right)=20 \log \left(\frac{2}{\beta_{m}}\right)=20 \log \left(\frac{2 \omega_{m}}{\Delta \omega}\right)=20 \log \left(\frac{2 M \omega_{m}}{K_{o s c} \hat{v}_{n}}\right) \tag{7.39}
\end{equation*}
$$

Note that the above analysis includes only the input noise of the $\operatorname{VCO}\left(v_{n_{i}}\right)$, while the additive output noise is ignored $v_{n_{o}}$ since it is usually much smaller. The effect of the dividers is to reduce the phase noise of the VCO by a factor of $M$ (equation (7.35)). However, the additive output white noise $v_{n_{o}}$ is not reduced by $M$. Furthermore, both the dividers itself and the clock buffers produce noise. This should all be accounted for to get a true indication of the clock noise.

### 7.5 Quantization

As noted in 7.3, the input sampler does not cause a loss of information as long as the sampling rate is greater than the Nyquist bandwidth. Quantization, on the other hand, produces an irreversible conversion error, where a continuous range of amplitudes is mapped on to a finite set of digital codes. Quantization noise is examined in this section for both the usual uniform quantization interval approximation and a more realistic non-uniform quantization approximation. The spectral content of the quantization is then examined and harmonically related error terms are analysed.

### 7.5.1 Quantization Noise

The quantizer can be modelled as in Fig. 7.13, where the quantization errors $e[m]$ can be seen as additive white noise that is linearly summed with the sampled input signal, $x_{s}[m]$. The conditions for this to hold true can be summarized using Bennett's assumptions [80]:

1) the input signal range can never exceed the quantizer range (no saturation);
2) there are a large number of quantizer levels (high-resolution and low correlation with input signal);
3) all codes are uniformly distributed over their quantization intervals;
4) all quantizer levels are exercised regularly (busy - non-DC) to remove correlation between the input signal and quantization levels.
The signal-to-quantization noise power ratio is the usual way of characterizing the quantizer. This will be examined in the following.


Fig. 7.13 Quantizer model with additive noise for linear analysis.


Fig. 7.14 Probability density function of additive noise assuming uniform coding model.

### 7.5.1.1 Uniform coding model

With the conditions set out by Bennett holding true, the quantization error, $e$, can be seen as having equal probability of taking on any value in the range of $-\frac{\Delta}{2}$ to $+\frac{\Delta}{2}$, as illustrated in Fig. 7.14 [81]. The linearised quantization noise model is shown in Fig. 7.13. Assuming that all the quantization levels are equally distributed and mutually separated by 1 LSB , the noise power, or variance, of the quantization error can be calculated as follows:

$$
\begin{align*}
\sigma_{\Delta(u n i f)}^{2} & =\int_{-\infty}^{\infty} e^{2} \cdot \rho_{\Delta}(e) \cdot d e \\
& =\frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^{2} \cdot d e \\
& =\frac{\Delta^{2}}{12} . \tag{7.40}
\end{align*}
$$

This is the classical result for quantization noise and represents the minimum quantization noise condition for uniform code widths of 1 LSB .


Fig. 7.15 ADC transfer and error functions for the long and short coding model.

### 7.5.1.2 Long and short coding model

The ubiquitous uniform code model of 7.5.1.1 gives too optimistic a noise level to represent a real ADC. A more realistic model is the alternating code model, where it is assumed that the ADC transfer characteristic can be divided up in to a series of long and short quantization intervals, such as shown in Fig. 7.15. An equal number of long and short codes occur over the full scale range of the ADC. Again, the quantization errors are modelled statistically as being uniformly distributed over an interval of $\pm \frac{\Delta_{L}}{2}$ for the long codes and $\pm \frac{\Delta_{S}}{2}$ for the short codes. This is illustrated in Fig. 7.16.

The noise power for the long codes can be obtained as:

$$
\begin{equation*}
\sigma_{\Delta_{L}}^{2}=\frac{\Delta_{L}^{2}}{12}, \tag{7.41}
\end{equation*}
$$

while the noise power for the short codes becomes:

$$
\begin{equation*}
\sigma_{\Delta_{S}}^{2}=\frac{\Delta_{S}^{2}}{12} \tag{7.42}
\end{equation*}
$$

The total quantization noise power is obtained by adding the individual noise contributions of the long and short codes, each weighted by their relative contributions over a 2 LSB interval:

$$
\begin{equation*}
\sigma_{\Delta \text { (ater) }}^{2}=\frac{\Delta_{L}}{2 \Delta} \times \sigma_{\Delta_{L}}^{2}+\frac{\Delta_{S}}{2 \Delta} \times \sigma_{\Delta_{S}}^{2} . \tag{7.43}
\end{equation*}
$$

With the quantity $D N L$ representing the scalar value of the DNL , then $\Delta_{L}$ and $\Delta_{S}$ can be defined as:

$$
\begin{align*}
& \Delta_{L} \tag{7.44}
\end{align*}=1+D N L \times \Delta
$$

Substituting into (7.43),

$$
\begin{equation*}
\sigma_{\Delta(\text { alter })}^{2}=\frac{\Delta^{2}}{24} \times\left[(1+D N L)^{3}+(1-D N L)^{3}\right] . \tag{7.45}
\end{equation*}
$$

Finally, the total RMS noise related to the DNL becomes:

$$
\begin{equation*}
\sigma_{\Delta(\text { alter })}=\frac{\Delta}{\sqrt{12}} \times \sqrt{1+3 D N L^{2}} . \tag{7.46}
\end{equation*}
$$

### 7.5.1.3 Signal-to-Quantization Noise Ratios

The signal-to-quantization noise ratio, $S Q N R$, is obtained by relating the power, $\sigma_{S}^{2}$, of a sinusoidal input signal with amplitude $A$ to the quantization noise power, $\sigma_{\Delta}^{2}$. Assuming the generalized long and short code quantization model of 7.5.1.2, then

$$
\begin{equation*}
S Q N R=\frac{\sigma_{S}^{2}}{\sigma_{\Delta}^{2}}=\frac{A^{2} / 2}{\Delta^{2} / 12 \times\left(1+3 D N L^{2}\right)}=6 \times\left(\frac{A}{\Delta}\right)^{2} \times \frac{1}{1+3 D N L^{2}} . \tag{7.47}
\end{equation*}
$$

In the specific case of a full scale sinusoidal input, where $A$ becomes $F S / 2$, then


Fig. 7.16 Probability density functions for long ( $L$ ) and short (S) coding model.


Fig. 7.17 Decrease of SQNR with DNL, using long and short coding model.

$$
\begin{equation*}
S Q N R_{F S}=6 \times \frac{\left(2^{N} / 2 \times \Delta\right)^{2}}{\Delta^{2}} \times \frac{1}{1+3 D N L^{2}}=\frac{3}{2} \times 2^{2 N} \times \frac{1}{1+3 D N L^{2}} . \tag{7.48}
\end{equation*}
$$

In decibels, this becomes:

$$
\begin{equation*}
S Q N R_{F S}=6.02 N-10 \log \left(1+3 D N L^{2}\right)+1.76 \mathrm{~dB} \tag{7.49}
\end{equation*}
$$

The decrease in SQNR with increasing DNL error compared to ideal uniform quantization is plotted in Fig. 7.17. For instance, taking long codes of +0.5 DNL and short codes of -0.5 DNL, representing code widths of 1.5 and 0.5 LSBs respectively, the noise is increased by 2.43 dB compared to the classical ideal case of uniform 1 LSB code widths. Clearly, as the DNL approaches $\pm 1$ LSBs, every second code goes missing and we get a return of the uniform coding condition but with 1 less effective bit.

The classical maximum $S Q N R$ is obtained for $A$ equal to $F S / 2$ and assuming uniform coding, i.e. $D N L=0$ :

$$
\begin{equation*}
S Q N R_{M A X}=6.02 N+1.76 \mathrm{~dB} . \tag{7.50}
\end{equation*}
$$

The quantization noise models of sections 7.5.1.1 and 7.5.1.2 were derived using the additive white noise analogy, where the quantization noise power is uniformly distributed in the Nyquist interval extending from $-f_{s} / 2$ to $+f_{s} / 2$. However, the signal with maximum bandwidth extending from $-f_{b w} / 2$ to $+f_{b w} / 2$ is often oversampled so that quantization noise appearing in the signal bandwidth is reduced by the oversampling ratio $f_{s} / 2 f_{b w}$. Furthermore, for completeness, account should be taken for when the maximum signal amplitude doesn't reach $F S / 2$. Hence, the maximum theoretical $S Q N R$ that can be achieved becomes:

$$
\begin{equation*}
S Q N R_{M A X}=6.02 N+10 \log \left(\frac{f_{s}}{2 f_{b w}}\right)+20 \log \left(\frac{2 A}{F S}\right)+1.76 \mathrm{~dB} . \tag{7.51}
\end{equation*}
$$



Fig. 7.18 Quantization error resulting from 4-bit uniform sampling of a sinusoid.

The signal-to-noise ratio increases by 6 dB or 1-bit for every 2 octaves the input is oversampled or just 3 dB per octave.

### 7.5.2 Quantizer Distortion

The quantizer error output is not signal independent uniform noise as generally assumed but is instead a deterministic function of the input signal. The discrete amplitude nature of the quantized signal results from the jumps in amplitude from level to level of the quantizer. An example is shown in Fig. 7.18 of the quantization error produced by the 4-bit quantization of a sinusoid. Spectral analysis of the quantizer output reveals a series of discrete harmonics not predicted by the white noise model of section 7.5.1. The correlation of the quantized noise of the output signal with the input signal becomes stronger as the quantizer resolution goes lower [82]. The correlation is strongest for a 1-bit quantizer, where the output is just a square wave. A model to examine the spectral content of the quantized error signal for a sinusoidal input signal is developed in the following.

Since the quantized signal $x_{q}(t)$ is inherently periodic, its Fourier series representation can be used to analyze its distortion [83]. Consider the representation of $x_{q}(t)$ as a continuous staircase signal with period $2 \pi$. The staircase signal can be seen to be made up of a summation


Fig. 7.19 Quantized inverse cosine signal for purposes of calculation of Fourier coefficients.
of rectangular pulses of height $\Delta$, the normalized quantization step. (The case for a 3-bit unipolar ADC is shown in Fig. 7.19). Note the choice of phase of the input signal makes no difference. For convenience of analysis, the input signal is chosen to be a negative cosine function.

The Fourier series of the periodic quantizer function $x_{q}(t)$ is:

$$
\begin{equation*}
x_{q}(t)=\frac{a_{0}}{2}+\sum_{k=1}^{\infty}\left[a_{k} \cdot \cos \left(k \omega_{0} t\right)+b_{k} \cdot \sin \left(k \omega_{0} t\right)\right] \quad \text { with } \omega_{0}=\frac{2 \pi}{T} . \tag{7.52}
\end{equation*}
$$

Using $\theta=\omega_{0} \cdot t$ with period $2 \pi$, the series of Fourier coefficients, $a_{k}$ and $b_{k}$ can be written as:

$$
\begin{align*}
& a_{k}=\frac{1}{\pi} \int_{0}^{2 \pi} x_{q}(\theta) \cos (k \theta) d \theta  \tag{7.53}\\
& b_{k}=\frac{1}{\pi} \int_{0}^{2 \pi} x_{q}(\theta) \sin (k \theta) d \theta . \tag{7.54}
\end{align*}
$$

The first term $\frac{a_{0}}{2}$ is the average value and can be determined by inspection, or by setting $k=0$ in (7.53).

Two simplifications can be made in obtaining the Fourier series. First, since the applied signal is an inverse cosine (even), the quantized output is even and, hence, $b_{k}=0$. Secondly, since the output waveform is symmetrical about $\theta=\pi$, only the coefficients between 0 and $\pi$ need to be evaluated and the result doubled. The phase is defined in such a way that as $\theta$ extends from 0 to $\pi$, the input level extends from 0 to $F S$ - see Fig. 7.19. Consider now a rectangular pulse of height $\Delta$, extending from $-\cos ^{-1}\left(\frac{\Delta}{2}\right)$ to $\pi$, used to compose the quantized
output $x_{q}(\theta)$. The Fourier coefficients of this rectangular pulse are

$$
\begin{align*}
a_{k}= & \frac{2}{\pi} \int_{-\cos ^{-1}\left(\frac{\Delta}{2}\right)}^{\pi} \Delta \cos (k \theta) d \theta \\
= & -\frac{2 \Delta}{\pi k} \sin \left(k \cos ^{-1}\left(\frac{\Delta}{2}\right)\right) . \tag{7.55}
\end{align*}
$$

The frequency coefficients $a_{k}$ are obtained by summing all of $a_{k}^{*}$ for each rectangular pulse used to build up the quantized output to give:

$$
\begin{equation*}
a_{k}=-\frac{2 \Delta}{\pi k} \sum_{m=1}^{2^{N-1}} \sin \left(k \cos ^{-1}\left(m-\frac{1}{2}\right) \Delta\right) \tag{7.56}
\end{equation*}
$$

Finally, the quantized output signal $x_{q}(\theta)$ can be obtained from:

$$
\begin{equation*}
x_{q}(\theta)=\frac{a_{0}}{2}+\sum_{k=1}^{\infty} a_{k} \cos (k \theta) . \tag{7.57}
\end{equation*}
$$

The relative harmonic distortion, in dBc with respect to the fundamental, is obtained as:

$$
\begin{equation*}
H D_{k}=20 \log \left(\frac{a_{k}}{a_{1}}\right) . \tag{7.58}
\end{equation*}
$$

Two frequency plots of the quantization harmonic distortion are presented in Fig. 7.20 for (a) 6 -bit and (b) 9-bit quantization. The maximum distortion is found to occur at $2^{N} \pi$ times the fundamental frequency. This is the same as the relationship between the period of the input signal and the period of the quantization error [84]. For instance, the harmonic number for maximum distortion of a 9-bit ADC has been simulated to be 1596 (Fig. 7.20(b)), which is approximately $2^{9} \pi$.

Clearly from the simulations of Fig. 7.20, the maximum harmonic level is always somewhat larger than the $3^{\text {rd }}$ harmonic and this difference increases as the quantizer resolution increases. Simulations were carried out to examine these effects and they are presented in Fig. 7.21. The variation of the relative level of the maximum harmonic component with respect to the fundamental for increasing resolutions $N$ is shown in Fig. 7.21(a). The maximum distortion level is seen to decrease at a rate of $-8.2 \mathrm{~dB} / \mathrm{bit}$ from simulations. The increase of the harmonic number with resolution is shown in Fig. 7.21(b), and this appears to follow the $2^{N} \pi$ rule to within a few $\%$. Note, approximating the maximum harmonic level as that of the $3^{\text {rd }}$ harmonic level is a reasonable one, in which case the level of the third harmonic with respect to the fundamental is approximately given by $-9 N \mathrm{dBc}\left(10 \cdot \log \left(1 / 2^{3 \cdot N}\right)\right.$, where $N$ is the effective quantizer resolution.

The above discussion of quantization distortion is based on uniform quantization. Typically, the quantization levels are spaced in a slight non-uniform manner, the distribution of which depends largely on the type of ADC chosen. In reality, errors resulting from non-ideal


Fig. 7.20 Quantization noise spectrum for (a) 6-bit and (b) 9-bit uniform quantizers.


Fig. 7.21 Maximum harmonic level (a), and its harmonic number (b), plotted as a function of quantizer resolution.
active components used to create the ADC will add to the errors due to quantization. These non-idealities are examined in the case of algorithmic and pipelined ADCs in the following chapters.

### 7.6 Effective Bits

The quality of a real ADC is best quantified by estimating its resolution in effective bits [74]. This is done by replacing the ideal $S Q N R_{M A X}$ over the complete Nyquist bandwidth with the actual measured $S N R$ in equation (7.50) and calculating out the effective number of bits, or $E N O B$, so that:

$$
\begin{equation*}
E N O B=\frac{S N R_{\text {measured }}-1.76}{6.02} \tag{7.59}
\end{equation*}
$$

Alternatively, the $E N O B$ can be related to the ideal number of bits $N_{i d e a l}$, where no reference needs to be made to the idealized uniform coding model, using:

$$
\begin{equation*}
E N O B_{L S B}=N_{\text {ideal }}-\log _{2}\left(\frac{\sigma_{\Delta(\text { measured })}}{\sigma_{\Delta(\text { ideal })}}\right) . \tag{7.60}
\end{equation*}
$$

The $S N R$ should be measured as a function of the input frequency as it is varied from 0 Hz up to $f_{s} / 2$. The typical variation of the ENOB as the input signal is swept in frequency is illustrated in Fig. 7.22. A related measured parameter of interest is the full scale effective resolution bandwidth $E R B$, or sometimes called the full scale analogue bandwidth. It is defined as the input frequency where the ENOB of the ADC response to a full scale sinusoidal input reduces by 3 dB with respect to its value at very low frequencies. Note the measurement must include all the usual artefacts of circuit noise, jitter and non-linearities.

The combined signal-to-noise ratio for both jitter (7.22) and quantization (7.46) of the black-box ADC can be calculated as:


Fig. 7.22 Reduction of ENOB with input frequency and definition of ERB.


Fig. 7.23 Dynamic range reduction due to jitter for a 14-bit ADC and increasing $f_{i n}$.

$$
\begin{align*}
\operatorname{SQJNR}=\frac{\sigma_{S}^{2}}{\sigma_{\Delta}^{2}+\sigma_{J}^{2}} & =\frac{A^{2} / 2}{\frac{1}{12} \cdot\left(\frac{A}{2^{N-1}}\right)^{2} \cdot\left(1+3 \cdot D N L^{2}\right)+2 \cdot\left(\sigma_{\tau} \cdot \pi \cdot f_{i n} \cdot A\right)^{2}} \\
& =\frac{1}{\frac{1+3 \cdot D N L^{2}}{3 \times 2^{2 \cdot N-1}}+\left(\sigma_{\tau} \cdot 2 \cdot \pi \cdot f_{i n}\right)^{2}} . \tag{7.61}
\end{align*}
$$

Using equations (7.59) and (7.61), the SQJNR as a function of the RMS jitter is plotted in Fig. 7.23 for (a) 0 LSB DNL and (b) 0.5 LSB DNL for a 14-bit ADC. Similarly in Fig. 7.24, the effective bit loss as a function of the RMS clock phase noise (discussed in section 7.4.2) is shown. The phase noise and hence jitter level can be determined below which the quantization noise dominates. The -0.3 LSB loss indicated in the figure is a reasonable level: it corresponds to the one standard deviation of phase jitter of equation (7.30). As part of the ADC design strategy, the phase noise contribution should remain insignificant compared to other noise sources.

To take a couple of examples: a 10 -bit ADC requires a sample clock with less than 1.3


Fig. 7.24 Effective Bits lost as a function of RMS clock phase noise.
$\operatorname{mrad}\left(0.075^{\circ}\right)$ RMS phase error which for say a 100 MHz sample rate means an RMS jitter of less than 2.1 ps ; a 14-bit ADC requires a clock with less than $81.4 \mu \mathrm{rad}\left(0.0047^{\circ}\right)$ error which for a 10 MHz sample rate requires an RMS clock jitter of less than 1.3 ps. Crystal oscillators have RMS jitter less than 0.2 ps , so that with careful design of the clock coupling network (especially the clock buffers), an RMS jitter of less than 0.4 ps is possible.

### 7.7 ADC Conversion Efficiency

The minimum $S N R$ and power limits are derived in this section for the generic ADC model for given conversion speed and accuracy specifications. Finally, figures of merit for area and power are presented as a means for comparing the efficiency of ADCs with different specifications, architectures and technologies.

### 7.7.1 Minimum $\operatorname{SNR}$ Limit

The total noise power of an $\operatorname{ADC} \sigma_{N_{A D C}}^{2}$ is related to the quantization noise power $\sigma_{\Delta}^{2}$ and the total thermal noise power $\sigma_{N_{t h}}^{2}$ by:

$$
\begin{equation*}
\sigma_{N_{A D C}}^{2}=\sigma_{\Delta}^{2}+\sigma_{N_{t h}}^{2} . \tag{7.62}
\end{equation*}
$$

No correlation is assumed here between the quantization noise and thermal noise. Equation (7.62) can be re-written to include the quantization and thermal signal-to-noise ratios, $S N R_{\text {quantiz }}$ and $S N R_{\text {thermal }}$, respectively [74]:

$$
\begin{equation*}
\sigma_{N_{A D C}}^{2}=\sigma_{\Delta}^{2} \cdot\left(1+\frac{S N R_{\text {quantiz }}}{S N R_{\text {thermal }}}\right) . \tag{7.63}
\end{equation*}
$$

The $S N R_{A D C}$ can be directly related to both $S N R_{\text {thermal }}$ and $S N R_{\text {quantiz }}$ after re-arranging equation (7.63):

$$
\begin{equation*}
S N R_{A D C}=S N R_{\text {quantiz }} \cdot \frac{1}{1+k}, \tag{7.64}
\end{equation*}
$$

in which $k$ is defined here as:

$$
\begin{equation*}
k=\frac{S N R_{\text {quantiz }}}{S N R_{\text {thermal }}} . \tag{7.65}
\end{equation*}
$$

It is important not to over-design the ADC for a thermal noise which is a lot lower than the quantization noise, since then the ADC dissipates too much power for the sake of a small improvement in overall $S N R_{A D C}$. Similarly, the thermal noise should not dominate the quantization noise. A good compromise is to achieve a design that degrades the overall $S N R_{A D C}$ by no more than 1.76 dB , which brings the $S N R_{A D C}$ down to the resolution level calculation of $S N R$, i.e. $S N R_{A D C}(\mathrm{~dB}) \sim 6 \cdot N$. This occurs when the thermal noise power is set at or below half the quantization noise power, or $k \leq \frac{1}{2}$. The ideal $S N R_{\text {quantiz }}$ is derived from equation (7.48) for 0 DNL to be:

$$
\begin{equation*}
S N R_{\text {quantiz }}=\frac{3}{2} \cdot 2^{2 \cdot N} \tag{7.66}
\end{equation*}
$$

Hence, with $k<\frac{1}{2}$, it follows that:

$$
\begin{equation*}
S N R_{\text {thermal }}>3 \cdot 2^{2 \cdot N} \tag{7.67}
\end{equation*}
$$

This is the minimum signal-to-thermal noise ratio allowed when designing an ADC to achieve a specified resolution of $N$.

Consider now an ADC in which the input signal voltage $V_{\text {sig }}$ is acquired by a capacitor $C$ and further processed by an amplifier and associated capacitors. The thermal noise power is given by:

$$
\begin{equation*}
\sigma_{N_{t h}}^{2}=\frac{k T}{C} \cdot\left(1+F_{N e}\right), \tag{7.68}
\end{equation*}
$$

where $F_{N e}$ is the excess noise factor which includes all other switching capacitors and amplifier noise. Note that the ADC is assumed to be functional over the full Nyquist bandwidth. For a sinusoidal input signal spanning the full scale range of the $\operatorname{ADC}(F S)$, the signal power is:

$$
\begin{equation*}
V_{s i g}^{2}=\frac{F S^{2}}{8} . \tag{7.69}
\end{equation*}
$$

The signal-to-noise ratio resulting from thermal noise, $S N R_{\text {thermal }}$, is calculated to be:

$$
\begin{equation*}
S N R_{\text {thermal }}=\frac{V_{\text {sig }}^{2}}{\sigma_{N_{t h}}^{2}}=\frac{C \cdot F S^{2}}{8 \cdot k T \cdot\left(1+F_{N e}\right)} . \tag{7.70}
\end{equation*}
$$

Now the minimum sampling capacitor value can be found based on the required minimum thermal $S N R$ by combining equations (7.67) and (7.70) to give:

$$
\begin{equation*}
C>24 \cdot 2^{2 \cdot N} \cdot\left(1+F_{N e}\right) \cdot \frac{k T}{F S^{2}} . \tag{7.71}
\end{equation*}
$$

Equation (7.71) will be used to establish the lower bound on ADC power consumption in the next section.

### 7.7.2 Minimum Power Limits

The minimum theoretical and practical power consumption limits of a generic ADC are calculated in this section. This serves as a useful comparison to actual power consumption calculations in section 8.3.

### 7.7.2.1 Minimum Theoretical Power Limit

The most power efficient amplifier only requires current from the supply to charge the sampling capacitors with no supply current being wasted. This implies an amplifier in class B operation where the only load capacitors are the sampling capacitors. The power consumption is given by:

$$
\begin{equation*}
P=V_{D D} \cdot\left|\frac{I_{a v g}}{\eta}\right|, \tag{7.72}
\end{equation*}
$$

where $I_{\text {avg }}$ is the average current over time to charge the load capacitors, while $\eta$ is the amplifier efficiency. For a class B amplifier, the maximum efficiency is $\eta=\frac{\pi}{4}$. The average power consumption required to charge a total system capacitance of $\alpha \cdot C$ at a rate of $f_{s}$ becomes:

$$
\begin{equation*}
P=\alpha \cdot \frac{2}{\pi} \cdot V_{D D} \cdot F S \cdot C \cdot f_{s} . \tag{7.73}
\end{equation*}
$$

The minimum theoretical power consumption for a sinusoidal input signal spanning full scale is obtained by substituting the minimum sampling capacitance value of (7.71):

$$
\begin{equation*}
P_{\min }>\alpha \cdot\left(1+F_{N e}\right) \cdot \frac{48}{\pi} \cdot 2^{2 \cdot N} \cdot \frac{V_{D D}}{F S} \cdot f_{s} \cdot k T . \tag{7.74}
\end{equation*}
$$

Finally, the absolute minimum power consumption is obtained for maximum dynamic range, when $F S=V_{D D}$, i.e.

$$
\begin{equation*}
P_{\min }>\alpha \cdot\left(1+F_{N e}\right) \cdot 15 \cdot 2^{2 \cdot N} \cdot f_{s} \cdot k T . \tag{7.75}
\end{equation*}
$$

The theoretical minimum ADC power consumption using this idealized model depends only on the resolution $N$, the sampling frequency $f_{s}$ and the thermal energy $k T$. Note, if the input signal is a continuous voltage with a level of $F S$, the power consumption of equation (7.73) changes to:

$$
\begin{equation*}
P=\alpha \cdot F S^{2} \cdot C \cdot f_{s} \tag{7.76}
\end{equation*}
$$

while the minimum power consumption using the switched capacitor theoretical model of the ADC increases to:

$$
\begin{equation*}
P_{\min (F S)}>\alpha \cdot\left(1+F_{N e}\right) \cdot 24 \cdot 2^{2 \cdot N} \cdot f_{s} \cdot k T . \tag{7.77}
\end{equation*}
$$

### 7.7.2.2 Minimum Practical Power Limit for Class A Operation

Consider a class A CMOS OTA used to charge and discharge the sampling capacitors and load capacitors associated with the ADC. The average power consumption is given by:

$$
\begin{equation*}
P=V_{D D} \cdot I . \tag{7.78}
\end{equation*}
$$

The maximum current that can be delivered to or drawn from the load is $I$. For a long channel
model and strong inversion, the supply current is related to the transconductance of the input differential pair through:

$$
\begin{equation*}
I \propto g_{m} \cdot V_{o n} / 2 \tag{7.79}
\end{equation*}
$$

The power consumption becomes:

$$
\begin{equation*}
P=\left(1+F_{P e}\right) \cdot V_{D D} \cdot g_{m} \cdot V_{o n} / 2, \tag{7.80}
\end{equation*}
$$

where $F_{P e}$ is the excess power factor resulting from the extra power dissipated in comparison to an ideal single-stage amplifier (mostly due to the extra current required by the added amplifier output stage and biasing). The $g_{m}$ of the amplifier is related to its settling time constant $\tau$ through equation (3.8):

$$
\begin{equation*}
g_{m}=\frac{1}{\beta} \cdot \frac{C_{L_{e f f}}}{\tau}=\frac{\alpha \cdot C}{\tau}, \tag{7.81}
\end{equation*}
$$

where $\alpha \cdot C$ is the equivalent capacitance the amplifier must drive. Hence,

$$
\begin{equation*}
P=\left(1+F_{P e}\right) \cdot \frac{V_{D D} \cdot V_{o n}}{2} \cdot \frac{\alpha \cdot C}{\tau} . \tag{7.82}
\end{equation*}
$$

The amplifier is often nominally designed such that the residual settling error after 1 clock period is less than 0.5 LSBs at $N-1$ bit level for an $N$-bit ADC. However, as explained in Chapter 8 , while the residual settling error after the first conversion of an algorithmic ADC only needs to be 0.5 LSB accurate, 0.25 LSBs is taken to allow a safety margin for production. Thus the settling error must satisfy:

$$
\begin{equation*}
e^{-\frac{1}{f_{s \cdot \tau}}}<2^{-(N+1)} \tag{7.83}
\end{equation*}
$$

Solving for $\tau$ gives:

$$
\begin{equation*}
\tau<\frac{1}{f_{s}} \cdot \frac{1}{(N+1) \cdot \ln (2)} . \tag{7.84}
\end{equation*}
$$

Substituting this settling requirement for $\tau$ into (7.82), as well as equation (7.71) for the minimum value of $C$ to satisfy the $S N R$ requirement, gives:

$$
\begin{equation*}
P>\alpha \cdot\left(1+F_{P e}\right) \cdot\left(1+F_{N e}\right) \times 12 \times 2^{2 \cdot N} \cdot \frac{V_{D D} \cdot V_{o n}}{F S^{2}} \cdot(N+1) \cdot \ln (2) \cdot f_{s} \cdot k T . \tag{7.85}
\end{equation*}
$$

Again the minimum power consumption occurs for the maximum signal range of $F S=V_{D D}$, so that (7.85), for class A operation, simplifies to:

$$
\begin{equation*}
P_{\min (\text { class A) }}>\alpha \cdot\left(1+F_{P e}\right) \cdot\left(1+F_{N e}\right) \times 8 \times 2^{2 \cdot N} \cdot \frac{V_{o n}}{V_{D D}} \cdot(N+1) \cdot f_{s} \cdot k T . \tag{7.86}
\end{equation*}
$$

This expression for the minimum power of a practical ADC shows the inverse relationship between power and supply voltage, $V_{D D}$. An increase in power supply allows for a proportional increase in maximum signal swing which then reduces the noise power requirement quadratically for a given ADC resolution. A direct power comparison between current state-of-the-art and proposed circuit techniques for cyclic and pipelined ADCs will be presented in Chapter 9.

### 7.7.3 ADC Figures of Merit

Area and power figures of merit, i.e. $F O M_{\text {area }}$ and $F O M_{\text {power }}$, are useful measures of the relative performance of ADCs because they compare objectively the efficiency of different design solutions. They are defined as:

$$
\begin{equation*}
F O M_{\text {area }}=\frac{A}{2^{E N O B} \cdot f_{s}} \mathrm{~nm}^{2} / \text { conversion }-\mathrm{Hz}, \tag{7.87}
\end{equation*}
$$

and

$$
\begin{equation*}
F O M_{\text {power }}=\frac{P}{2^{E N O B} \cdot f_{s}} \mathrm{pJ} / \text { conversion, } \tag{7.88}
\end{equation*}
$$

where $E N O B$ is the effective number of bits, $f_{s}$ is the sample frequency in $\mathrm{MHz}, A$ is the active area in $\mu \mathrm{m}^{2}$ and $P$ is the power consumption measured in $\mu \mathrm{W}$. These $F O M$ s normalize area and power into silicon area use and energy use per ADC conversion. They can be used to compare all types of converters irrespective of architecture, frequency of operation or type and generation of process used. State of the art values are $F O M_{A}=100 \mu \mathrm{~m}^{2} /$ conversion and $F O M_{p}=1 \mathrm{pJ} /$ conversion. There are three primary reasons for the continual improvement in efficiency of ADCs, namely shrinking technology size, improving design techniques, and novel design solutions. The new ADC design technique presented in this thesis for use in 65 nm technology is testament to this. Direct comparisons based on these figures of merit will be presented in Chapter 10.

### 7.8 Conclusions

Key ADC specifications were firstly presented here to form a reference for the analysis in this thesis. The three basic blocks of the ADC, namely the pre-filter, sampler and quantizer were examined in detail, while the expected non-idealities were modelled and formulated. The transfer characteristic of the pre-filter can distort the analogue signal due either to non-uniformity in the passband or roll-off affecting signal frequencies. Inaccurate sampling due to noise on the sample clock edges can have a big impact on the performance of high-frequency (sub-sampling) ADCs for communications applications. This was modelled and the resultant effective bit loss demonstrated as a function of clock jitter, sample frequency and resolution. The quantization process was shown to be inherently non-linear. A realistic coding model was proposed to reflect the influence of varying DNL on the quantization process and resultant equivalent noise. A simplified model for quantizer distortion was proposed. Finally, models were presented for calculating the minimum expected signal-to-noise ratio in an ADC, while both the minimum theoretical and practical power limits were derived in terms of the conversion accuracy and sample rate.

## Chapter 8

## Design Criteria For Cyclic And Pipelined ADCs

This chapter focuses on system level design of algorithmic ${ }^{1}$ type ADCs which can be either cyclic or pipelined. Firstly, the ADC is reviewed at an algorithmic and system level. Next, the effects of hardware constraints on ADC accuracy are critically examined with specific attention paid to static and dynamic performance. The effects of errors on the ADC transfer characteristic are simulated and error bounds derived. Finally, those specific design issues affecting pipelined ADCs are examined. The performance of a pipelined ADC can be enhanced via the use of a multi-bit front-end stage and analogue hardware scaling down the remaining low-resolution back-end stages. This is critically analysed. Finally, a model is proposed to estimate the power per stage and hence total power consumption of the pipelined ADC.

There is no specific focus in this chapter on circuit level realizations, except that a reference design is used to help clarify the origin of various circuit level imperfections. The general theory presented is decoupled from actual circuit realizations. The specifics of various circuit architectures for the implementation of cyclic/pipelined ADCs, including the proposed improved approach, are left to Chapter 9. Note that cyclic and pipelined are used interchangeably for the analysis in this chapter, since they are both algorithmic ADCs. Where specific design issues affect only one or other type, these will be highlighted.

### 8.1 Operation of Cyclic and Pipelined ADCs

The algorithm governing the operation of the cyclic and pipelined ADC is described at a high level in this section. Digital error correction through the use of code redundancy is also described. For presentation purposes, the analogue voltages are assumed to be differential and symmetrical about 0 , while the digital bit representations of the data is assumed to be bipolar. The full-scale range is defined over $\pm V_{r e f}$ and given by $F S=2 \cdot V_{r e f}$.

[^1]
### 8.1.1 The ADC Algorithm

Any continuous analogue voltage $V_{a}$ can be approximately represented in a $N$-bit binary form according to the following recursive binary-search algorithm [85]:

$$
\begin{align*}
V_{\text {out }_{i}} & =2 \cdot V_{i n_{i-1}}-D_{i} \cdot V_{\text {ref }} \\
\text { where } \quad V_{\text {in }}^{i} &
\end{align*}=\left\{\begin{array}{ll}
V_{\text {out }}, & \forall i \neq 1 \\
V_{\text {onalog_in }}, & i=1
\end{array}\right\} \begin{array}{ll}
\text { and } \quad D_{i} & =\left\{\begin{array}{cc}
1, & V_{\text {in }}>0 \\
-1, & \text { otherwise },
\end{array}\right.  \tag{8.1}\\
i & =1,2, \ldots, N .
\end{array}
$$

$V_{\text {ref }}$ determines the resolvable input signal range, where $V_{\text {analog_in }} \in\left[+V_{\text {ref }},-V_{\text {ref }}\right]$ and $D_{i}, i=1,2, \ldots, N$, is mapped onto $b_{i}, i=1,2, \ldots, N$ to give the binary representation of $V_{\text {analog_in }^{\prime}}: b_{1} b_{2} \ldots b_{N}$. Voltage $V_{\text {out }_{i}}, i=1,2, \ldots, N$, in (8.1) is referred to as the analogue residue voltage for the $i$-th iteration. An algorithmic ADC [86] based on (8.1) can be realized either as a cyclic ADC [87] if the recursiveness of (8.1) is mapped on to a single piece of hardware, or a pipelined ADC [88] if the recursive algorithm is mapped to a pipelined cascade of hardware stages.

Redundancy is often used to avoid the ADC going out of range in the presence of offsets in comparators and amplifiers. The coding mechanism used (Redundant Signed Digit) is explained in section 8.1.2. The generalized single stage of an cyclic/pipelined ADC, employing redundancy, is depicted in Fig. 8.1. In the bottom path, the sub-ADC reacts instantaneously to the analogue input signal to produce a coarse digital representation. The resultant digital code is output to a digital decoder, while at the same time it is converted back to its gained- up analogue equivalent ${ }^{2}$ ) by the equally coarse sub-DAC. This is then subtracted from the gained up and delayed (to compensate the sub-DAC clock delay) version of the input signal to produce the output residue voltage. The residue output re-circulates in the cyclic ADC so that the sample rate is the clock rate divided by the number of iterations. The pipelined ADC, on the


Fig. 8.1 Generalized Algorithmic block conversion stage.

[^2]other hand, is composed of a cascade of such algorithmic blocks so that the sample rate is the clock rate - i.e. the throughput rate of the complete pipelined ADC is equal to the throughput rate of each individual stage. The latency of both the pipelined and cyclic converters is the same when the pipeline contains a cascade of similar algorithmic blocks. However, in the pipeline, it is possible to decouple the conversion rate from the conversion time, or latency, since different resolution algorithmic blocks may be used per stage.

The generalized transfer function of the algorithmic block stage $i$ is:

$$
\begin{equation*}
V_{\text {out }_{i}}=G_{i} \cdot V_{i n_{i-1}}-V_{D A C_{i}}, \tag{8.2}
\end{equation*}
$$

with $G_{i}$ the binary form stage gain. The voltage levels of the sub-DAC output of stage $i$, $V_{D A C_{i}}$, are given by:

$$
\begin{equation*}
V_{D A C_{i}}=D_{i} \cdot V_{r e f}= \pm(l-1) \cdot V_{r e f} \text {, with } l \in\left\{1,2, \ldots, G_{i}\right\} . \tag{8.3}
\end{equation*}
$$

The input voltage is compared against the nearest quantized level of the sub-ADC, given by:

$$
\begin{equation*}
V_{A D C_{i}}= \pm \frac{l-\frac{1}{2}}{G_{i}} \cdot V_{r e f}, \text { where } l \text { is an integer for } l \in\left\{1, \ldots, G_{i}-1\right\} \tag{8.4}
\end{equation*}
$$

Note the gain multiplication factor inherent in the relationship for $V_{D A C_{i}}$, since the gain factor in the digital path must match the gain factor in the analogue path before subtraction. Hence, Fig. 8.1 is true to the actual hardware realization, such as discussed in section 8.2.

The equivalent (since not explicitly present in system) N -bit quantized version of the analogue input voltage after $N S$ stages of the pipelined ADC (or after $N S$ rotations of the cyclic ADC with all $G_{i}$ the same) is obtained as the binary weighted summation of each stage's output, i.e.

$$
\begin{equation*}
\tilde{V}_{\text {analog_i_ }=}=V_{D A C_{1}}+\frac{V_{D A C_{2}}}{G_{1}}+\cdots+\frac{V_{D A C_{N S}}}{\prod_{i=1}^{N S-1} G_{i}} . \tag{8.5}
\end{equation*}
$$

The remaining residue voltage (referred back to the input) after the final conversion of the cyclic/pipelined ADC is given by:

$$
\begin{equation*}
V_{\text {residue }(\text { final })_{i n}}=V_{\text {analog_in }}-\tilde{V}_{\text {analog_in }} . \tag{8.6}
\end{equation*}
$$

The actual residue voltage outputted on the final ADC cycle is:

$$
\begin{equation*}
V_{\text {residue }(\text { final })_{\text {out }}}=V_{\text {residue }(\text { final })_{i n}} \cdot \prod_{i=1}^{N S} G_{i} . \tag{8.7}
\end{equation*}
$$

The number of pipeline stages, or cyclic rotations, $N S$ is not necessarily equal to the total resolution $N$, since more than 1 bit can be resolved per stage. Furthermore, a final flash converter may be used to quantize the final residue voltage, $V_{\text {residue }}(\text { final })_{\text {out }}$, and hence ultimately determine the last few LSBs (usually a 1-3 bit flash is used). In general, the total ADC resolution is:

$$
\begin{equation*}
N=\sum_{i=1}^{N S} \log _{2} G_{i}+F, \tag{8.8}
\end{equation*}
$$



Fig. 8.2 Signal transfer characteristics of a RSD converter (a) for a 2-bit stage and (b) for a 3-bit stage (or after two consecutive 2-bit stages).
where $F$ is the resolution of the extra final flash stage if one is used. The total number of stages becomes $N S+F$. Errors in the final flash quantization levels determine what the ultimate error in ADC quantization will be. Usually 1-bit redundancy is employed per stage for redun-dant-signed-digit decoding (RSD [89]) so that for a $K$-bit stage, $K-1$ bits are effectively resolved and the stage gain factor becomes $G_{i}=2^{K-1}$. Moreover, if every stage is $K$-bits, then the total resolution $N$ becomes:

$$
\begin{equation*}
N=N S \cdot(K-1)+F \tag{8.9}
\end{equation*}
$$

The ideal transfer characteristics of 2-bit (1-bit effective) and 3-bit (2-bit effective) ADC stages are shown in Fig. 8.2(a) and (b), respectively. Note the residue plot of the 3-bit stage is the same as the transfer of two 2-bit stages in series. As an example, take the 3-bit ADC stage and normalize the full scale range such that $V_{\text {analog_in }} \in[-1,+1]$. The stage design parameters can be tabulated as follows:

Table 8.1 Design parameters for 3-bit ADC stage

| Stage resolution | $K=3$ |
| :---: | :---: |
| Transfer Gain | $G_{i}=2^{K-1}=4$ |
| ADC thresholds | $V_{A D C_{i}}=\left\{-\frac{5}{8},-\frac{3}{8},-\frac{1}{8},+\frac{1}{8},+\frac{3}{8},+\frac{5}{8}\right\}$ |
| DAC codes | $\{000,001,010,011,100,101,110\}$ |
| DAC output levels | $V_{D A C_{i}}=\{-3,-2,-1,0,+1,+2,+3\}$ |

### 8.1.2 Digital Output Decoding

The digitized output version of the analogue input signal is formed through the use of what is conventionally termed a DEC (Digital offset Error Correction) block which uses Redundant Signed Digit decoding. The primary function of the DEC is to combine the outputs after each


Fig. 8.3 Digital output decoding in an NS-stage pipelined ADC.
rotation of the cyclic ADC, or after each stage of the pipelined ADC, while at the same time correcting for the effect of DC offsets in each stage, as long as the offset per stage is bounded by $\pm \frac{V_{\text {ref }}}{4}$ [90], [91]. More complicated DECs include digital calibration circuitry to compensate for the effects of capacitor mismatch [92], [93], [94] when trying to achieve better than 10 -bit accuracy in conventional approaches. The proposed techniques of Chapters 9 and 10 demonstrate how to achieve high-accuracy while avoiding the overhead of calibration.

The DEC is demonstrated symbolically in Fig. 8.3 for a pipelined $N$-bit ADC of 2-bits per stage (1-bit redundant). The situation for a cyclic ADC is similar, except that one single stage is used recursively. Assuming the latency per stage is one sample clock period, each stage's digital output code is suitably delayed (with the LSB stage codes having no relative delay and the MSB stage codes having $N S$ clock periods delay) such that all the codes arrive together at the inputs of the full-adder block. The final LSB stage can be just another 2-bit stage with its LSB output tied off (as shown in Fig. 8.3) or a dedicated flash stage with its output bits concatenated to the output of the full-adder and its MSB output used as the overlap bit for addition to the LSB output of the first pipeline stage.

The operation of each ADC stage is governed by the following set of equations:

$$
\begin{align*}
& V_{\text {out }}^{i}
\end{align*}=2 \cdot V_{i n_{i}}-D_{i} \cdot V_{\text {ref }} \text {, where }, \begin{array}{rr}
1, & V_{i n_{i}}>\frac{V_{\text {ref }}}{4} \\
D_{i}= & -\frac{V_{r e f}}{4} \leq V_{i n_{i}} \leq \frac{V_{r e f}}{4}  \tag{8.10}\\
-1, & -\frac{V_{r e f}}{4}>V_{i n_{i}} \\
i=1,2, \ldots, N S .
\end{array}
$$

The purpose of the (single) algorithmic block in the case of the cyclic converter, or the series of algorithmic blocks in the case of the pipelined converter is to perform the arithmetic of (8.10). The algorithm is implemented as shown in the shaded insert of Fig. 8.3 for a single stage with the 1.5 -bit sub-ADC resolving the input range into 3 regions given by $\left\langle b_{i, 1}, b_{i, 0}\right\rangle \in\{\langle 0,0\rangle,\langle 0,1\rangle,\langle 1,0\rangle\}$. The 2 bits from each stage are suitably delayed and added in the DEC starting at the LSB stage and working back to the MSB stage with one bit overlap from stage to stage. The resultant output level of the $N$-bit ADC is obtained by doing a simple binary weighted summation of the DEC output bits $\left\langle d_{1}, \ldots, d_{N}\right\rangle$, where $d_{1}$ is the MSB:

$$
\begin{equation*}
d_{\text {out }}=V_{\text {ref }} \cdot \sum_{i=1}^{N} d_{i} \cdot 2^{N-i} \tag{8.11}
\end{equation*}
$$

Note that the DEC doesn't actually remove analogue offset (i.e. not a calibration) - it only reduces the sensitivity of the digital signal reconstruction to the effects of analogue offset. Otherwise, each stage amplifier and comparator would have to be designed with an offset of less than $1 / 2$ LSB of the resolution of the remaining stages. The DEC, therefore, helps to achieve higher ADC resolutions and hence lower power and circuit area compared to when no DEC is present.

### 8.2 Accuracy Limitations of Cyclic/Pipelined ADCs

This section deals with the cyclic/pipelined ADC composed of 2-bit stages ( $K=2$ ) with 1-bit redundancy. Extension of the discussion to higher resolution stages is straight forward. The 2bit stage is the most effective for achieving high throughput with high accuracy and low power [95]. It can be advantageous to have a higher resolution front-end stage in a pipeline ( $K=3$ to 5 typically) to reduce the accuracy requirements of the following 2-bit stages. This will be dealt with in section 8.3.1. The errors shown on the transfer characteristics which accompany the following discussion are accentuated compared to what would normally be expected for the purposes of illustration. However, familiarity with the effect a particular error can have on the transfer characteristic of the ADC will help identify the source of any serious errors should they arise in fabrication, e.g. due to a large systematic offset in one of the stages of a pipelined ADC.

For reference purposes in this section, the contemporary charge-transfer switched-capac-


Fig. 8.4 Contemporary single-ended SC charge transfer ( $C$ - $>C$ ) implementation of cyclic/pipelined ADC stage ( $K=2$ ).
itor (SC) stage implementation of Fig. 8.4 will be used [90] (the $C \rightarrow C$ method as defined in Chapters 2 and 9). However, the discussion is not dependent on any one circuit implementation but is generally applicable to the circuit level design of cyclic/pipelined ADC stages. The circuit shown operates with two mutually non-overlapping clocks $c l k 1$ and $c l k 2$. The SC MDAC circuit performs the level shifting, analogue multiplication by 2 and sample-and-hold buffering. On $c l k 1$, the input signal $V_{i n}$ is sampled on to $C_{1}$ and $C_{2}$ in parallel, while at the same time the sub-ADC determines whether it falls into the top, middle or bottom of the ADC reference range. At the end of the clk1, $V_{\text {in }}$ is completely sampled on to $C_{1}$ and $C_{2}$, while the output of the sub-ADC is latched and held. On clk2, $C_{1}$ is switched and placed across the amplifier, closing its negative feedback loop, while at the same time only one of the input switches of $C_{2}$ is closed by the sub-DAC using only one of clock signals top, mid, bot, connecting $C_{2}$ to either $+V_{r e f}, 0$, or $-V_{\text {ref }}$. By choosing $C_{1}=C_{2}$, a nominal transfer gain of $1+C_{2} / C_{1}=2$ is achieved. The errors associated with the practical implementation of an individual ADC stage will be dealt with in the following [P.15].

### 8.2.1 Lumped Error Model

The cyclic ADC, or each individual stage of the pipelined ADC, is specified such that all the accumulated errors at the end of the conversion process remain within $1 / 2$ LSB of the correct code so as to ensure that there is never a missing code. Note that 1 LSB is enough for monotonicity but $1 / 2$ LSB is specified to be safe. The total fractional error $\varepsilon_{\text {tot }}$ is the accumulation of all stage errors referred back to the input, i.e.

$$
\begin{equation*}
\varepsilon_{t o t}=\sum_{i=1}^{N S} \frac{\varepsilon_{i}}{\prod_{j=1}^{i} G_{j}}, \tag{8.12}
\end{equation*}
$$

where $\varepsilon_{i}$ is the net fractional stage error. Usually 1-bit redundancy is employed per stage for RSD decoding [89] so that for a $K$-bit stage, $K-1$ bits are effectively resolved and the stage gain factor becomes $G_{i}=2^{K-1}$. Hence, the total error becomes:

$$
\begin{equation*}
\varepsilon_{t o t}=\sum_{i=1}^{N S} \frac{\varepsilon_{i}}{2^{(K-1) \cdot i}} . \tag{8.13}
\end{equation*}
$$

The magnitude of the largest allowed total input referred voltage error is

$$
\begin{equation*}
\left|V_{\varepsilon_{t o t}}\right| \leq \varepsilon_{t o t} \cdot V_{r e f} . \tag{8.14}
\end{equation*}
$$

The magnitude of the total voltage error should be less than $1 / 2$ LSB to reliably guarantee monotonicity of the ADC, i.e.

$$
\begin{align*}
& \varepsilon_{\text {tot }} \cdot V_{\text {ref }} \leq \frac{L S B}{2}\left(=\frac{1}{2} \cdot \frac{2 \cdot V_{r e f}}{2^{N}}\right) \\
& \quad \Rightarrow \varepsilon_{t o t} \leq \frac{1}{2^{N}} . \tag{8.15}
\end{align*}
$$

Alternatively, each individual stage should be designed to have a total input referred voltage error of less than $1 / 4 \mathrm{LSB}$ of the total effective resolution of the remaining stages. Note that this is set approximately at the level of the quantization noise error of the remaining stages, which is $L S B / \sqrt{12} \approx 1 / 4 L S B$. Assuming each stage is $K$-bits, the total fractional output error for a stage $i$ is specified as:

$$
\begin{align*}
& \varepsilon_{i} \cdot V_{r e f} \leq \frac{1}{4} \cdot \frac{2 \cdot V_{\text {ref }}}{2^{N-(K-1) i}} \\
& \quad \Rightarrow \varepsilon_{i} \leq \frac{1}{2^{N-(K-1) \cdot i+1}} . \tag{8.16}
\end{align*}
$$

The stage error arises from the addition of all the errors from various static $\left(\varepsilon_{s}\right)$ and dynamic $\left(\varepsilon_{d}\right)$ sources. Usually, the stage is designed such that the dynamic and static errors add up in roughly equal measure. Hence, for the usual $K=2$-bit stage, the following conditions are set for $\varepsilon_{s}, \varepsilon_{d}$ of each stage in order to ensure a robust design:

$$
\begin{equation*}
\varepsilon_{s, d} \leq 2^{-(N-i+2)} . \tag{8.17}
\end{equation*}
$$

The various sources of static and dynamic errors are described in the following subsections [P.15].

The worst-case INL can be evaluated from the standard deviation of the total equivalent input error $\left(\sigma_{t o t}\right)$. The error should be obtained for the expected worst case code transition, for instance when $V_{\text {in }}$ crosses $\frac{V_{\text {ref }}}{4}$. Assuming a Gaussian distribution for the voltage difference $\varepsilon$ between the actual and ideal transfers, the INL can be obtained as the expected value of $|\varepsilon|$ at the worst case transition point:

$$
\begin{align*}
I N L=E[|\varepsilon|] & =\int_{-\infty}^{\infty}|\varepsilon| \cdot \frac{1}{\sqrt{2 \cdot \pi \cdot \sigma_{\text {tot }}^{2}}} \cdot e^{-\frac{\varepsilon^{2}}{2 \cdot \sigma_{t o t}^{2}}} d \varepsilon \\
& =\sqrt{\frac{2}{\pi}} \cdot \sigma_{t o t} . \tag{8.18}
\end{align*}
$$

This gives a direct relationship between the expected value of the INL and the RMS value of the total equivalent error referred back to the input of the ADC.

### 8.2.2 Limitations on Static Accuracy

Static error types, and their effect on the cyclic or pipelined transfer characteristics, are investigated in this section. The effects on simulated ADC transfer characteristics are portrayed and error bounds are derived.

### 8.2.2.1 Offset Errors

There are two basic forms of offset which have different effects on the ADC transfer. Firstly, there is input offset which adds up with the input signal to the stage. This offset is due mainly to the amplifier and to a lesser extent to the switches. The transfer function in this case is of the form:

$$
\begin{equation*}
V_{\text {out }_{i}}=G_{i} \cdot\left(V_{\text {in }}^{i} \text { }+V_{\text {off }}^{\text {in }} \text { }\right)-D_{i} \cdot V_{\text {ref }}, \tag{8.19}
\end{equation*}
$$

where the offset gets multiplied up by the stage gain. The second form of offset is that due to the comparators. This has the effect of shifting either one or both of the decision levels of the sub-ADC.

As explained in section 8.1.2, the total offset from all sources must remain within the bounds of $\pm \frac{V_{\text {ref }}}{4}$ to avoid saturating the following stage and causing missing codes. Note that this requirement is not dependent on the required accuracy of the whole ADC, nor accuracy of each individual stage. The offset does accumulate according to equation (8.12) though, so that some applications requiring low ADC offset will need some kind of active offset cancellation mechanism. Proposals in this regard are discussed in Chapter 10.

Simulated graphs showing the effects of excessive offsets going beyond $\pm \frac{V_{r e f}}{4}$ are shown in Fig. 8.5 to Fig. 8.7. The grey curves show the ideal and the black the non-ideal transfers. In Fig. 8.5, the effects of input offset going beyond $\pm \frac{V_{\text {ref }}}{4}$ are shown. Consider Fig. 8.5(a), (b), (c), (d), where the input offset goes beyond $+\frac{V_{\text {ref }}}{4}$ : the ADC transfer characteristic shows a single wide code for when the stage output voltage exceeds $+V_{\text {ref }}$, followed by missing codes, the number of which depends on how much the stage output voltage exceeds $+V_{\text {ref }}$ In Fig. 8.5(e)(h), the input offset goes under $-\frac{V_{\text {ref }}}{4}$, in which case the ADC characteristic first has missing codes followed by a single wide code. In Fig. 8.6, the separate effect of sub-ADC comparator offsets exceeding $\pm \frac{V_{\text {ref }}}{4}$ in stage 1 are demonstrated for both the top and bottom comparators. Similarly, in Fig. 8.7, the effects of excessive bottom and top comparator offsets in stage 2 are illustrated

### 8.2.2.2 Capacitor Mismatch Gain Errors

The effects of capacitor mismatch gain errors on the transfer characteristic will be shown here. The details of capacitor mismatch when comparing existing and proposed solutions will be set forth in Chapter 9.

(b) ADC transfer with stage 1 offset=+5Vref/16


(d) ADC transfer with stage 2 offset $=+5 \mathrm{~V}$ ref $/ 16$

(e) Stage 1 transfer with stage 1 offset=-5Vref/16





Fig. 8.5 Effects of excessive input offset on the ADC transfer characteristics.


Fig. 8.6 Effects of excessive stage 1 comparators offsets on ADC transfer characteristics.


Fig. 8.7 Effects of excessive stage 2 comparators offsets on ADC transfer characteristics.

The generalized transfer function of the ADC stage (e.g. $C \rightarrow C$ and $C+C$ of Chapter 9 ) including capacitor mismatch errors is:

$$
\begin{equation*}
V_{\text {out }}=2 \cdot V_{\text {in }} \cdot\left(1+\frac{\Delta_{c}}{2}\right)-D \cdot V_{\text {ref }} \cdot\left(1+\Delta_{c}\right) \tag{8.20}
\end{equation*}
$$

where $\Delta_{c}$ is the term due to capacitor mismatch. In the specific case of Fig. 8.4, $\Delta_{c}$ represents the mismatch of nominally equal capacitors $C_{1}$ and $C_{2}$. The fractional stage output error due to capacitor mismatch is calculated in the more general context of a multi-bit front-end in section 8.3.1. The capacitor matching requirement for a 2-bit stage can be derived as:

$$
\begin{equation*}
\sigma_{\Delta_{C}} \leq \frac{1}{3 \times 2^{N-i-1}} \tag{8.21}
\end{equation*}
$$

where $i$ is the stage number. An important observation with this kind of gain error is that there is always an exact mapping of the following input values to output values, irrespective of $\Delta_{c}$ :

$$
\begin{equation*}
V_{\text {in }} \in\left\{-V_{\text {ref }}, 0,+V_{\text {ref }}\right\} \rightarrow V_{\text {out }} \in\left\{-V_{\text {ref }}, 0,+V_{\text {ref }}\right\} . \tag{8.22}
\end{equation*}
$$

This suggests a very effective way of calibrating out capacitor mismatch errors by extrapolating between these correctly mapped points.

The effects of capacitor mismatch errors in stage 1 are illustrated in Fig. 8.8. Positive capacitor mismatch errors (Fig. 8.8(a)-(c)) cause a series of wide codes (code widths greater than 1 LSB ) and negative code jumps resulting in non-monotonicity. Negative capacitor mismatch errors (Fig. 8.8(d)-(f)), on the other hand, cause a series of narrow codes (code widths less than 1 LSB ) and positive code jumps, resulting in missing codes. Fig. 8.9(a) and (b) show the result of positive capacitor mismatch in stage 2 . Here again there are wide codes corresponding to the six transition points from the ADC input to the second stage output. Furthermore, there are also two sets of missing codes at $\pm \frac{V_{\text {ref }}}{4}$ which are the transition points of the previous stage. A similar scenario exists for negative capacitor ratio errors (Fig. 8.9(c) and (d)), except that wide codes are replaced by narrow codes and negative and positive code jumps are interchanged.

### 8.2.2.3 Amplifier Gain Errors

The OTA, in a switched-capacitor configuration of a stage $i$ along the pipeline, must linearly amplify the input voltage by a factor of 2 over the full scale range of $-V_{\text {ref }}$ to $+V_{\text {ref }}$ to within a maximum error of $2^{-(N-i+2)}$. As a result of the sampled-data operation of the stage, only end values count. Hence, only DC gain variations around $\Delta V_{i n}=0$ count, since the differential OTA input always settles back to around 0 V as the stage output end value is reached. The OTA DC gain has an essentially even characteristic and the DC gain doesn't vary much for final settled values around $\Delta V_{\text {in }}=0$ whether the outputs end up at 0 V with $\Delta V_{\text {in }}=0$ or at $\pm V_{\text {ref }}$ with $\Delta V_{\text {in }}=2 \cdot V_{\text {ref }} / A_{0\left(\Delta V_{\text {in }}=2 \cdot V_{r e f}\right)}$.

The stage transfer function, including amplifier gain error $\varepsilon_{A_{0}}$, is:

$$
\begin{equation*}
V_{\text {out }_{i}}=\left(2 \cdot V_{i n_{i}}-D_{i} \cdot V_{r e f}\right) \cdot\left(1+\varepsilon_{A_{0}}\right), \tag{8.23}
\end{equation*}
$$



Fig. 8.8 Effects of stage 1 capacitor mismatch errors on ADC transfer characteristics.

$$
\begin{equation*}
\text { where } \quad \varepsilon_{A_{0}} \approx-\frac{1}{A_{0} \cdot \beta_{f b}} . \tag{8.24}
\end{equation*}
$$

In general, the DC gain requirement for stage $i$ is:

$$
\begin{equation*}
A_{0}>\frac{1}{\beta_{f b}} \cdot 2^{N-i+2} \tag{8.25}
\end{equation*}
$$

To take an example, say the SC ADC stage of Fig. 8.4 is designed as the first stage in a 12-bit pipeline, or as the main stage of a 12-bit cyclic ADC. The feedback factor is $\beta_{f b}=C_{1} / C_{1}+C_{2}$ for this specific realization. Hence, with $C_{1}=C_{2}$ nominally, $\beta_{f b}=\frac{1}{2}$ and with $i=1$, the log amplifier DC gain is required to be $A_{0}(\mathrm{~dB})>84 \mathrm{~dB}$ ! Note that this stage, classified as the $C \rightarrow C$ in


Fig. 8.9 Effects of stage 2 capacitor mismatch errors on $A D C$ transfer characteristics.

Chapter 9, can be improved on by using the proposed $C+C$ stage in which the amplifier DC gain requirement reduces to only 78 dB to achieve 12 -bit resolution.

An important observation with this kind of gain error is that there is always an exact mapping of the zero crossings irrespective of DC gain error, be it linear or non-linear, i.e. $V_{\text {in }} \in\left\{-\frac{V_{r e f}}{4}, 0,+\frac{V_{\text {ref }}}{4}\right\} \rightarrow 0$. The ADC characteristics corresponding to DC gain errors (which
only give rise to missing codes) in either of stage 1 or stage 2 are illustrated in Fig. 8.10. only give rise to missing codes) in either of stage 1 or stage 2 are illustrated in Fig. 8.10.

### 8.2.3 Limitations on Dynamic Accuracy

This section investigates and analyses the main limitations affecting the dynamic performance of cyclic/pipelined ADCs. Error bounds are derived [P.15].

### 8.2.3.1 Linear and Non-linear Settling Constraints

The settling error model of section 3.4 can be used to ascertain the requirement per ADC stage to settle within a certain error defined by the resolution of that stage. The stage amplifier slews when the step voltage at the amplifier differential input goes beyond the maximum linear input range of $\sqrt{2} \cdot V_{o n}$ which corresponds to it delivering its maximum current $I$ to the load. The dynamic settling error $\varepsilon_{\text {settle }}$ caused by the amplifier not settling out in sample period $T$, was derived as:


Fig. 8.10 Effects of DC gain error and linear settling error on ADC transfer.

$$
\begin{gather*}
\mathcal{E}_{\text {settle }}=\left\{\begin{array}{c}
e^{-n}, \quad V_{\text {step }} \leq \frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma} \\
\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma \cdot V_{\text {step }}} \cdot e^{-n}, \quad V_{\text {step }}>\frac{\sqrt{2} \cdot V_{\text {on }}}{\gamma}, \\
\text { where } \quad n=\frac{T-t_{\text {slew }}}{\tau} \text { and } \quad t_{\text {slew }}=\tau \cdot\left(\frac{\gamma \cdot V_{\text {step }}}{\sqrt{2} \cdot V_{\text {on }}}-1\right) \cdot
\end{array}\right. \tag{8.26}
\end{gather*}
$$

This error must be no larger than the required stage dynamic settling error, $\varepsilon_{\text {settle }} \leq 2^{-(N-i+2)}$. The effect of combined finite settling time and finite slew rate is shown in Fig. 8.11. The limited settling time produces a similar effect to limited DC gain (see Fig. 8.10) in the sense that end values are not achieved within a sampling clock interval. This is a linear effect, unlike limited slew rate which is input level dependent. This is clear from Fig. 8.11, where large input levels up to $\pm V_{\text {ref }}$ cause a tapering off effect leading to poor INL and harmonic distortion. Note again that the zero crossings are correctly mapped in spite of the non-linear distortion.

### 8.2.3.2 Thermal Noise

The output noise power produced by a single ADC stage, such as that of Fig. 8.4, with a read phase (clkl) and write phase (clk2), has 3 constituents:


Fig. 8.11 Effects of non-linear settling errors on ADC transfer characteristics.

$$
\begin{equation*}
\sigma_{N_{\text {stage }}}^{2}=\sigma_{N_{\text {OTA }}}^{2}+\sigma_{N_{C_{\text {read }}}}^{2}+\sigma_{N_{C_{\text {write }}}}^{2} \tag{8.28}
\end{equation*}
$$

with $\sigma_{N_{\text {amp }}}^{2}$ the amplifier noise sampled only in the write phase and $\sigma_{N_{C_{\text {read }}}}^{2}, \sigma_{N_{C_{\text {write }}}}^{2}$ the noise produced by the switches in the read and write phases, respectively. The thermal noise power produced by the differential amplifier (OTA), referred to the output, is given by:

$$
\begin{equation*}
\sigma_{N_{O T A}}^{2}=\frac{16}{3} \cdot k T \cdot \frac{1}{g_{m}} \cdot\left(1+N_{e_{O T A}}\right) \cdot B_{N_{O T A}} \cdot \frac{1}{\beta_{f b}^{2}}, \tag{8.29}
\end{equation*}
$$

where $\frac{16}{3} \cdot k T \cdot \frac{1}{g_{m}}$ is the noise power spectral density of a differential pair and $N_{e_{O T A}}$ is the noise excess factor depending on the OTA architecture used. The amplifier input noise power is multiplied by $G^{2}=1 / \beta_{f b}^{2}$, which is the noise power gain from stage input to output. For an essentially first order amplifier settling response, the amplifier noise bandwidth is approximately:

$$
\begin{equation*}
B_{N_{O T A}} \approx \frac{1}{4 \cdot \tau_{O T A}}=\frac{\beta_{f b} \cdot g_{m}}{4 \cdot C_{L_{e f f}}} \tag{8.30}
\end{equation*}
$$

with $\tau_{O T A}$ the linear settling time constant, $\beta_{f b}$ the feedback factor and $C_{L_{e f f}}$ the total effective load capacitance (equation (3.7). Hence, the amplifier noise power formula can be reduced to:

$$
\begin{equation*}
\sigma_{N_{O T A}}^{2}=\frac{4}{3 \cdot \beta_{f b}} \cdot \frac{k T}{C_{L_{e f f}}} \cdot\left(1+N_{e_{\text {OTA }}}\right) . \tag{8.31}
\end{equation*}
$$

For the specific case of the SC ADC stage of Fig. 8.4, the switch noise contributions for the read and write phases can be calculated as:

$$
\begin{equation*}
\sigma_{N_{C_{\text {read }}}}^{2}=\frac{2}{\beta_{f b}^{2}} \cdot \frac{k T}{C_{1}+C_{2}} \text { and } \sigma_{N_{C_{\text {write }}}}^{2}=\frac{2 \cdot B_{N_{\text {OTA }}}}{B_{N_{\text {swit }}}} \cdot\left(\frac{k T}{C_{1}}+\frac{k T}{C_{2}}\right) . \tag{8.32}
\end{equation*}
$$

The factor 2 in (8.32) is for the differential case and the ratio $B_{N_{\text {OTA }}} / B_{N_{\text {swit }}}$ is the bandwidth reduction factor in the write phase, since the switch noise (for $C_{1}$ at the OTA input and $C_{2}$ in the feedback path of the OTA) is limited by the effective OTA noise bandwidth $B_{N_{\text {OTA }}}$ and not the bandwidth of each capacitor branch with its associated switches, $B_{N_{\text {swit }}}$. Note that since the noise in the read phase is pre-sampled, it is not affected by the amplifier bandwidth. Generally, $B_{N_{\text {OTA }}} \ll B_{N_{\text {swit }}}$ and with $C_{1}=C_{2}$, the ADC stage output noise power for full Nyquist operation, can be reduced to:

$$
\begin{equation*}
\sigma_{N_{\text {stage }}}^{2} \approx \frac{1}{\beta_{f b}^{2}} \cdot\left(\frac{4}{3} \cdot \beta_{f b} \cdot \frac{k T}{C_{L_{e f f}}} \cdot\left(1+N_{e_{\text {OTA }}}\right)+\frac{k T}{C}\right) \tag{8.33}
\end{equation*}
$$

Now the total noise power of the cyclic/pipelined ADC can be calculated by summing the noise power of each stage after it has been referred back to the input of the ADC. The equivalent input noise power for each stage is obtained by dividing the stage output noise power by the signal gain up to that stage. If all stages are similar, then the power gain factor per stage is just $1 / \beta_{f b}^{2}$, and the total equivalent noise calculated back to the input is:

$$
\begin{equation*}
\sigma_{N_{\text {tot }}}^{2}=\sigma_{N_{\text {stage }}}^{2} \cdot \beta_{f b}^{2} \cdot\left(1+\beta_{f b}^{2}+\beta_{f b}^{4}+\ldots\right) \approx \sigma_{N_{\text {stage }}}^{2} \cdot \frac{\beta_{f b}^{2}}{1-\beta_{f b}^{2}} \tag{8.34}
\end{equation*}
$$

Substituting (8.33) into (8.34), the total input-referred ADC noise power ends up as:

$$
\begin{equation*}
\sigma_{N_{t o t}}^{2} \approx \frac{1}{1-\beta_{f b}^{2}} \cdot\left(\frac{4}{3} \cdot \beta_{f b} \cdot \frac{k T}{C_{L_{e f f}}} \cdot\left(1+N_{e_{O T A}}\right)+\frac{k T}{C}\right) \tag{8.35}
\end{equation*}
$$

Based on noise considerations, the signal capacitor $C$ can be derived. Using the arguments of section 7.7.1, where thermal noise is allowed to degrade the total $S N R$ by just 1.76 dB , the thermal noise power is specified with respect to the quantization noise power $\sigma_{\Delta}^{2}$ by $\sigma_{N_{\text {tot }}}^{2} \leq \frac{1}{2} \cdot \sigma_{\Delta}^{2}$. Hence,

$$
\begin{equation*}
\frac{1}{1-\beta_{f b}^{2}} \cdot\left(\frac{4}{3} \cdot \beta_{f b} \cdot \frac{k T}{C_{L_{e f f}}} \cdot\left(1+N_{e_{O T A}}\right)+\frac{k T}{C}\right) \leq \frac{1}{24} \cdot \frac{F S^{2}}{2^{2 N}} . \tag{8.36}
\end{equation*}
$$

This formula is representative of the noise for the cyclic ADC and the pipelined ADC without scaling. The general case of the pipeline with scaling will be dealt with in section 8.3.2.

The minimum value of $C$, based on noise considerations, can be found for the SC ADC stage of Fig. 8.4. Assuming the parasitic capacitance at the amplifier input is relatively small compared to $C$, and since there is no scaling along the pipeline, $C_{L_{e f f}}$ is given by $C_{L_{\text {eff }}}=C_{1}+C_{2}+\beta_{f b} \cdot C_{2}$, which with $\beta_{f b}=C_{1} / C_{1}+C_{2}$ and $C_{1}=C_{2}=C$, we get $\beta_{f b}=\frac{1}{2}$ and $C_{L_{\text {eff }}}=\frac{5}{2} \cdot C \cdot N_{e_{\text {OTA }}}$ is typically in the range of 1 (single-stage OTA) to 2 (dual-stage OTA) $N_{e_{\text {OTA }}}=2$ is chosen here. Equation (8.36) now reduces to:

$$
\begin{equation*}
\frac{28}{15} \cdot \frac{k T}{C} \leq \frac{1}{24} \cdot \frac{F S^{2}}{2^{2 N}} . \tag{8.37}
\end{equation*}
$$

The minimum value of $C$ in order to satisfy the noise requirements becomes:

$$
\begin{equation*}
C \geq 45 \cdot k T \cdot \frac{2^{2 N}}{F S^{2}} \tag{8.38}
\end{equation*}
$$

Reference curves are shown in Fig. 8.12 for the minimum capacitor value to be chosen in order to meet a given signal-to-noise specification at a given operating temperature. For instance, a 12-bit ( $N$ ) differential application with 1 V signal range $(F S)$ and full Nyquist operation at room temperature, requires $C \geq 3.1 \mathrm{pF}$. Note the importance of maximizing signal range for the sake of minimizing signal capacitance, so that if the signal range is doubled to 2 V , the capacitance is reduced by a factor of $4(C=3 / 4 \mathrm{pF})$ for the same 12-bit performance (although the minimum detectable signal increases by 2 also).

Note that $S N R$ is not always taken as a measure of the performance of an ADC. Particularly in high-frequency communications applications such as in receiver analogue front-ends and many other sub-sampling applications, the ADC linearity is often the number one specification. The reason is that channel selection is done to isolate a narrow band of frequencies out of the total Nyquist interval via a highly selective (off-chip) pre-filter. Hence, after down-sampling or frequency shifting to baseband, the effective $S N R$ is increased many times. For instance, a 14-bit $10 \mathrm{MS} / \mathrm{s}$ ADC refers to achieving an $\operatorname{SFDR}$ (and thus usually DNL) at the 14bit level, whereas the $S N R$ might only be at the 12-bit level or even less (e.g. Analog Devices [96], Berkeley [97]). This is also the case for the 14-bit pipelined ADC design presented in Chapter 10.


Fig. 8.12 Minimum capacitor values based on noise considerations to achieve a given resolution in a pipelined $A D C$.

### 8.3 Pipelined ADC Specific Design Issues

The pipelined ADC offers the extra design freedom over the cyclic ADC of being able to tailor each individual stage to produce an optimized cascade. Specifically, the front-end stage can be designed to resolve 2 or more bits ( $K>2$ ), while at the same time area/power scaling can be applied to the back-end stages. The generalized pipelined ADC with multi-bit front-end and scaled back-end is demonstrated in Fig. 8.13.

Usual analyses assume that noise is the limiting factor to pipelined ADC capacitor choice and allowed scaling [99], [100]. In fact it is capacitor matching which ultimately limits ADC performance, since although the required $S N R$ can always be reached through increasing the unit capacitor size, this is not true of capacitor matching. In modern CMOS processes, increasing capacitor size only improves matching up to a point, beyond which matching only disimproves. It is very difficult to achieve better than 9-bit linear capacitor matching in a CMOS process, especially for metal-metal type capacitors.

Note, the majority of published ADCs of more than 9-bit resolution rely on digital calibration techniques. Such digital calibration techniques are very promising but up till now add considerably to the cost (area and power) of the converter solution, recent examples being [97] and [98]. The position of this thesis is to achieve intrinsic accuracy beyond 9-bits without relying on any calibration techniques. The first approach to achieving this for pipelined ADCs is to use multi-bit front-ends. This was first proposed by Analog Devices [96], based mostly on qualitative reasoning. The analysis put forward here (sub-section 8.3.1) justifies this approach.

This section starts off by demonstrating analytically the accuracy improvement that can be achieved through the use of a multi-bit front-end stage in a pipelined ADC. Next, a design algorithm is presented for optimized stage scaling for given power and error constraints. Finally, the power consumption of a scaled pipelined ADC is calculated.

### 8.3.1 Design Optimization of Multi-bit Input Stage

The multi-bit front-end stage provides an elegant way of improving the linearity of a pipelined ADC (Fig. 8.13) beyond the 9-10 bit level (capacitor matching limitation) without having to


Fig. 8.13 Generalized pipelined ADC for optimized scaling.
resort to capacitor trimming nor calibration [96], [P.16]. The intention is to have a high enough resolution in the first stage that the resolution of the remaining stages can be comfortably achieved using a 2 -bit stage without excessive area and power.

This section will show a new analytical approach to estimating the required number of bits of a front-end stage (or if needs be, front-end stages) in order to be able to proceed with a "standard" 2-bit pipeline stage [P.16]. Standard is used reservedly here since there are different implementations possible for the 2-bit pipeline stages, including the high-accuracy $C+C$ stage proposed in Chapter 9.

The generalized circuit diagram of a $K$-bit charge transfer $C \rightarrow C$ MDAC, suitable for use in a front-end stage, is shown in Fig. 8.14. The stage transfer is:

$$
\begin{equation*}
V_{\text {out }_{1}}=2^{K-1} \cdot V_{\text {in }_{1}}-V_{D A C_{1}}, \tag{8.39}
\end{equation*}
$$

where $2^{K-1}$ is the stage gain, assuming overlap of the first stage LSB with the second stage MSB for redundancy. The DAC voltage levels, which are created by multiplication of the reference voltage by capacitor ratios, are given by:

$$
\begin{gather*}
V_{D A C_{1}}=V_{r e f} \cdot D_{1},  \tag{8.40}\\
\text { where } \quad D_{1} \in\left\{0, \pm \frac{C_{2}}{C_{1}}, \pm \frac{C_{2}+C_{3}}{C_{1}}, \ldots, \pm \sum_{i=2}^{2^{K-1}} \frac{C_{i}}{C_{1}}\right\} . \tag{8.41}
\end{gather*}
$$

Let amplifier feedback capacitor $C_{1}$ have nominal value $C$, so that in the presence of capacitor mismatches,

$$
\begin{equation*}
\frac{C_{2}}{C_{1}}=1+\Delta_{C_{2}}, \frac{C_{2}+C_{3}}{C_{1}}=2+\Delta_{C_{2}}+\Delta_{C_{3}}, \text { etc. } \tag{8.42}
\end{equation*}
$$

Each of $\Delta_{C_{i}}$ represents the relative capacitor mismatch of $C_{i}$ with respect to $C$. The first stage output including the effects of capacitor mismatches becomes:

$$
\begin{equation*}
V_{\text {out }_{1}}^{\prime}=V_{i n_{1}} \cdot\left(2^{K-1}+\sum_{i=2}^{2^{K-1}} \Delta_{C_{i}}\right)-V_{\text {ref }} \cdot D_{1}, \tag{8.43}
\end{equation*}
$$

where $D_{1} \in\left\{0, \pm\left(1+\Delta_{C_{2}}\right), \pm\left(2+\Delta_{C_{2}}+\Delta_{C_{3}}\right), \ldots, \pm\left[\left(2^{K-1}-1\right)+\sum_{i=2}^{2^{K-1}} \Delta_{C_{i}}\right]\right\}$.
Note that not just the gain but also the DAC levels are affected by capacitor mismatch. The stage output voltage error, produced as a result of capacitor mismatch, becomes:

$$
\begin{gather*}
\varepsilon_{\Delta_{C}}=V_{\text {out }_{1}}^{\prime}-V_{\text {out }_{1}}=V_{\text {in }} \cdot \sum_{i=2}^{2^{K-1}} \Delta_{C_{i}}-V_{\text {ref }} \cdot \Delta D_{1},  \tag{8.45}\\
\text { with } \Delta D_{1} \in\left\{0, \pm \Delta_{C_{2}}, \pm\left(\Delta_{C_{2}}+\Delta_{C_{3}}\right), \ldots, \pm \sum_{i=2}^{2^{K-1}} \Delta_{C_{i}}\right\} . \tag{8.46}
\end{gather*}
$$



Fig. 8.14 Multi-bit front-end MDAC circuit stage for pipelined ADC.

The worst case condition for this multi-bit MDAC circuit stage (Fig. 8.14) is when the input voltage just trips the first comparator level of the sub-ADC. This is because, at this point, $V_{\text {ref }} \cdot \frac{C_{2}}{C_{1}}$ gets subtracted off the minimal detected input level to give the worst case relative voltage error. Hence, with $V_{i n}=\frac{V_{\text {ref }}}{2^{K}}$ and $\Delta D_{1}=\Delta_{C_{2}}$ in (8.45),

$$
\begin{align*}
\varepsilon_{\Delta_{C}} & =\frac{V_{r e f}}{2^{K}} \cdot \sum_{i=2}^{2^{K-1}} \Delta_{C_{i}}-V_{r e f} \cdot \Delta D_{1} \\
& =\frac{V_{r e f}}{2^{K}} \cdot\left[\sum_{i=3}^{2^{K-1}} \Delta_{C_{i}}+\left(1-2^{K}\right) \cdot \Delta_{C_{2}}\right] \tag{8.47}
\end{align*}
$$

The RMS residue voltage error arising from capacitor mismatch is derived as:

$$
\begin{align*}
\sigma_{\text {err } r_{C}} & =\frac{V_{\text {ref }}}{2^{K}} \cdot \sqrt{\left(2^{K-1}-2\right) \cdot \sigma_{\Delta_{C}}^{2}+\left(1-2^{K}\right)^{2} \cdot \sigma_{\Delta_{C}}^{2}} \\
& =\sigma_{\Delta_{C}} \cdot \frac{V_{r e f}}{2^{K}} \cdot \sqrt{2^{2 \cdot K}-3 \cdot 2^{K-1}-1 .} \tag{8.48}
\end{align*}
$$

This error term should be less than a $1 / 4 \mathrm{LSB}$ of the resolution of the remaining stages, i.e.

$$
\begin{align*}
\sigma_{e r r_{C}} & \leq \frac{F S}{4 \cdot 2^{N-K+1}} \\
& \leq \frac{V_{\text {ref }}}{2^{K}} \cdot \frac{1}{2^{N-2 \cdot K+2}} . \tag{8.49}
\end{align*}
$$

Combining (8.48) and (8.49), the allowable matching accuracy of the capacitors in the multibit front-end MDAC circuit stage is set by:

$$
\begin{equation*}
\sigma_{\Delta_{C}} \leq \frac{1}{2^{N-2 \cdot(K-1)} \cdot \sqrt{2^{2 \cdot K}-3 \cdot 2^{K-1}-1}} . \tag{8.50}
\end{equation*}
$$

This closed form useful relationship gives the minimum required capacitor matching in a $K$-bit front-end in order to achieve an overall $N$-bit ADC accuracy.

A plot is made in Fig. 8.15 depicting the required matching accuracy of the capacitors in the $K$-bit front-end stage as a function of the pipeline resolution $N$ for a few different values of $K$. Take, as an example, a 12 -bit converter. For conventional $K=2$-bit pipeline stages (with 1 bit overlap from stage to stage), the MDAC capacitors require 11.6 bits matching. This is too high for fabricated capacitors. If, say, metal-metal plate capacitors are employed in the standard $C \rightarrow C$ type MDACs, then an RMS matching of no better than 9 -bits can be expected in standard CMOS. The required resolution of the front-end stage can be ascertained in order to ensure that stages 2 to $N S$ can be standard 2-bit $C \rightarrow C$ type stages using standard metal capacitors of up to 9-bit matching. From the graph of Fig. 8.15, it follows that the front-end stage must have $K=5$ in order for the ADC to achieve 12-bit accuracy.

It is not wise from the point of view of power and area to go beyond a 5-bit front-end stage [99] so that, for instance, when a 14 -bit pipelined ADC is specified, a tapering of the resolutions is needed over the first few stages. This can be designed with the aid of the graph of Fig. 8.15: the first stage should be no greater than $K_{1}=5$-bits, leaving 10 -bits effective resolution for the second stage onwards, so it should be $K_{2}=3$-bits which in turn leaves 8 -bits effective resolution for the third stage onwards, and hence $K_{3}=2$-bits with each following stage being 2-bits. A 5:3:2...: 2 pipeline is required. Area and power scaling may be applied to the remaining $K=2$ stages - a subject dealt with in the next subsection. Note that it is quantified in Chapter 9 that based on the new proposed $C+C$ technique, 14-bit intrinsic accuracy is achievable without needing a multi-bit front-end stage which can save considerable power and area.

To summarize, each increase of 1 bit of resolution of the front-end stage reduces the required resolution of the remaining stages by almost 1 bit. There is still only 1-bit overlap of the first stage LSB with second stage MSB for redundancy in order to digitally desensitize for offset. In a practical design, a single multi-bit front-end followed directly by standard 2-bit stages is preferable, since a tapering of bits per stage adds a lot of analogue complexity and is best avoided if possible [96], [102]. There are a number of down sides, though. Firstly, the


Fig. 8.15 Required capacitor matching in multi-bit front-end for different resolutions.
amplifier $G B W$ increases with each bit compared to a standard 2-bit stage for the same effective resolution. This is principally because of the lower feedback factor, given by:

$$
\begin{equation*}
\beta_{f b}=\frac{1}{1+\sum_{i=2}^{2^{K-1}} \frac{c_{i}}{c_{1}}} . \tag{8.51}
\end{equation*}
$$

Both the bandwidth and DC gain need to increase commensurately with each extra bit in the front-end stage. Secondly, a sample-and-hold stage becomes a necessity in order to drive all the extra signal capacitors and the $2^{K-1}$ comparators. Thirdly, since the sensitivity to comparator offset is increased by $2^{K-1}$, each of the $2^{K-1}$ comparators will require more area and power than comparators for a 2-bit stage. For these reasons, the front-end stage rarely goes beyond 4 bits (with 14 comparators connected to the input).

### 8.3.2 Design Optimization of Scaled Pipelined ADCs

Pipelined ADCs are predominantly designed for mid-to-high frequency applications - the power consumption is dominated by the (static) power consumption of the stage amplifiers required to charge up the associated signal capacitors to a specified accuracy in a given sample period. As explained in section 8.2.2.1, there is relatively little dynamic power consumed by the dynamic comparators in the low-resolution sub-ADCs, while the associated digital processing doesn't consume much power either. On the other hand, scaling of static power (and hence area, since the gate overdrive voltages - $V_{o n}$ 's - must be maintained through active area scaling with current) in consecutive pipelined ADC stages is possible in order to reduce overall power consumption compared to un-scaled pipelines while maintaining the same specified accuracy [101], [102]. Note that the digital circuitry and the sub-ADC practically don't scale. Scaling is not always applied because of the increased design complexity and time-tomarket but when applied, scaling only makes sense for $K=2$ (back-end) stages. As discussed in section 8.3.1, the design objective is to get down to a $K=2$ stage as early as possible and progress to the end of the pipeline with $K=2$ stages. Scaling of, say, 3-bit stages may be useful in a high-resolution, low-frequency application where slewing, limited $G B W$, parasitic capacitance and charge injection play less of a role. However, a more gradual scaling of higher-speed $K=2$ stages is more power and area efficient [95], [96].

The power consumed relative to the first stage depends on the stage scaling factor and the number of stages $N S$ :

$$
\begin{equation*}
P=P_{1} \cdot\left(1+\sum_{i=2}^{N S} \prod_{j=1}^{i-1} S_{j}\right) \tag{8.52}
\end{equation*}
$$

For constant stage to stage scaling of $S$, (8.52) can be simplified to:

$$
\begin{equation*}
P=P_{1} \cdot \frac{1-S^{N S}}{1-S} . \tag{8.53}
\end{equation*}
$$

Stage 1 here can represent either the first stage of the complete pipelined ADC which uses all similarly scaled stages, or it can represent the first stage following the multi-bit front end stage


Fig. 8.16 Pipeline power consumed and total error power relative to that in stage 1 .
after which there is constant scaling of similar stages. The power consumed relative to the first stage is shown in Fig. 8.16. The figure illustrates that below a scaling factor of about 0.7, the power in the pipelined ADC is dominated by the power consumed in the first few stages only. At a scaling factor of 0.7 , the pipeline power converges to about 3.5 times the power of the first stage, regardless of the number of stages.

The pre-dominant error sources in a pipeline stage are due to thermal noise $\sigma_{N_{\text {stage }}}$ and capacitor mismatch $\sigma_{e r r_{C}}$, both of which are directly proportional to the size of the stage signal capacitors. They add in a non-correlated way to give the stage output noise power of:

$$
\begin{equation*}
\sigma_{e}^{2}=\sigma_{N_{\text {stage }}}^{2}+\sigma_{\text {err }}^{C} \tag{8.54}
\end{equation*}
$$

Both $\sigma_{N_{\text {stage }}}$ and $\sigma_{\text {err }}$ were calculated in section 8.2 for a contemporary SC stage implementation. Scaling down the pipeline, while reducing power consumption, has the deleterious effect of reducing conversion accuracy too due to increased noise and capacitor mismatch. In general, the relationship between the input referred total error power and the first stage error power is given by:

$$
\begin{equation*}
\sigma_{e_{\text {tot (in) }}}^{2}=\frac{\sigma_{e}^{2}}{G_{1}^{2}} \cdot\left(1+\sum_{i=2}^{N S} \frac{1}{\prod_{j=2}^{i} S_{j}} \cdot \frac{1}{\prod_{k=2}^{i} G_{k}^{2}}\right) . \tag{8.55}
\end{equation*}
$$

For constant scaling $S$ and stage gain $G$, (8.55) reduces to:

$$
\begin{equation*}
\sigma_{e_{\text {tot (in) }}^{2}}^{2}=\frac{\sigma_{e}^{2}}{G^{2}} \cdot\left(1+\sum_{i=2}^{N S}\left(\frac{1}{S \cdot G^{2}}\right)^{i-1}\right), \tag{8.56}
\end{equation*}
$$

which can be simplified to:

$$
\begin{equation*}
\sigma_{e_{\text {tot (in) }}}^{2}=\frac{\sigma_{e}^{2}}{G^{2}} \cdot \frac{1-\left(\frac{1}{G^{2} \cdot S}\right)^{N S}}{1-\frac{1}{G^{2} \cdot S}} . \tag{8.57}
\end{equation*}
$$

The increase in input referred error power relative to the input referred error power of the first stage alone is also shown in Fig. 8.17 for $G=2$.

The design goal is to minimize the power-error product to achieve the most power efficient design that achieves the specified accuracy. Note that the power-error product is inversely proportional to the power efficiency. The curves of Fig. 8.17 can be used as a guide to obtaining an optimal stage scaling factor for the highest power efficiency in a practical design. Ideally, a scaling factor $S$ of 0.5 should be used along the pipeline of 2-bit stages but, in practice, a value of $S$ between 0.5 and 0.7 is better to take account of non-scaling parasitic capacitance.

### 8.3.3 Estimation of Static Power Consumption of Pipelined ADCs

Up till now, the power consumption of the scaled pipeline has been evaluated with respect to the power of the first stage. Now it will be shown how to evaluate the actual power per stage, so that the an estimate can be made of the total power consumption of the scaled pipeline. As explained in section 8.3.2, the MDAC amplifiers dominate the power consumption. Based on the model presented in Chapter 3 for amplifier dynamic settling, the power consumption of a single pipeline stage $i$, operating with supply voltage $V_{D D}$, can be estimated in order for it to achieve a particular settling accuracy for an expected maximum step change in input voltage, $V_{\text {step }_{\text {in }}(\max )}$. The amplifier drives an equivalent load capacitance $C_{L_{\text {eff }}}$, which includes the 2 scaled sample capacitors of the following stage. The stage $i$ power consumption $P_{i}$ is obtained from Chapter 3 as:


Fig. 8.17 Optimization curves for power-error product as function of scaling.

$$
\begin{equation*}
P_{i}=\left(1+P_{e}\right) \cdot \frac{4 \sqrt{2} \cdot V_{o n} \cdot V_{\text {oD }} \cdot C_{L_{e f f}}}{\tau_{i}}, \tag{8.58}
\end{equation*}
$$

where $P_{e}$ is the excess amplifier power compared to that of a $100 \%$ efficient single-stage amplifier and includes biasing. Typically, it is in the range of 0.2 (single-stage) to 1.5 (dualstage). The factor of 4 includes a differential realization (x2) with single-sampling (x2), where the stage is assumed to settle within $T / 2$. The stage time constant $\tau_{i}$ is obtained by solving the following equation for the dynamic settling accuracy of a $K$-bit stage for maximum expected signal excursions (see equations (8.16),(8.17),(8.26),(8.27) for single-sampling):

$$
\begin{align*}
& \varepsilon_{d}=2^{N-(K-1) \cdot i+2} \\
& =\frac{\sqrt{2} \cdot V_{o n}}{\gamma \cdot V_{\text {step }}^{\text {in }}}(\max ) \quad . \quad e^{-\left(\frac{T}{\tau_{i}}+1-\frac{\gamma \cdot V_{\text {step }}\left(p_{i n}(\max )\right.}{\sqrt{2} \cdot V_{\text {on }}}\right)} . \tag{8.59}
\end{align*}
$$

(8.59) is solved for $\tau_{i}$ to give:

$$
\begin{equation*}
\tau_{i}=\frac{T}{\frac{\gamma \cdot V_{\text {sep }} p_{i n}(\max )}{\sqrt{2} \cdot V_{o n}}}-\left(1+\log _{e}\left(\frac{\gamma \cdot V_{\text {step }}(\max )}{\sqrt{2} \cdot V_{o n}} \cdot 2^{-N+(K-1) i-2}\right)\right) . \tag{8.60}
\end{equation*}
$$

The stage $i$ power consumption required to achieve maximum step excursions is derived in terms of known parameters after substituting (8.60) into (8.58):

$$
\begin{equation*}
P_{i}=\left(1+P_{e}\right) \cdot \frac{4 \sqrt{2} \cdot V_{o n} \cdot V_{D D} \cdot C_{L_{\text {eff }}}}{T} \cdot\left(\frac{\gamma \cdot V_{\text {step }}(\max )}{\sqrt{2} \cdot V_{\text {on }}}-1-\log _{e}\left(\frac{\gamma \cdot V_{\text {step }}(\max )}{\sqrt{2} \cdot V_{o n}} \cdot 2^{-N+(K-1) \cdot i-2}\right)\right) . \tag{8.61}
\end{equation*}
$$

Finally, the total power consumption of the pipelined ADC is obtained from:

$$
\begin{equation*}
P_{t o t}=\sum_{i=1}^{N S} P_{i} . \tag{8.62}
\end{equation*}
$$

Here, $P_{i=1}$ is the power of the first stage, which can be the multi-bit front-end described in 8.3.1, while $P_{i=2} \cdots P_{i=N S}$ are the powers of each of the scaled back-end stages obtained from (8.52).

### 8.4 Conclusions

In this chapter, analytical expressions to describe the functional operation of cyclic and pipelined ADCs have been derived. A lumped error model was developed to account for static and dynamic errors due to hardware imperfections. The effects of specific errors on the ADC transfer characteristics were described. It was emphasized that familiarity with the effects specific errors have on the ADC characteristics can be a useful means for debugging hardware errors after ADC fabrication. An error analysis was presented to aid the design of the pipeline multibit front-end stage. It was demonstrated and quantified how the capacitor matching requirement can be reduced in high-resolution pipelined ADCs. A multi-bit front-end stage should only be used if ADC accuracy cannot be achieved using $K=2$-bit stages alone. The function of
the multi-bit front-end is to translate the ADC accuracy requirement down to the level of the achievable accuracy of the first $K=2$ stage. From there on in, each $K=2$ stage should be scaled by a factor of between 0.5 and 0.7 until such stage that parasitics and charge feedthrough effects begin to play a large role. Next, a pipeline power and noise scaling analysis was presented and explained. Finally, the power consumption per ADC stage was derived in terms of known parameters.

## Chapter 9

## Capacitor Matching Insensitive HighResolution Low-Power ADC Concept

A new implementation for cyclic and pipelined ADCs is presented in this chapter. A floating-hold-buffer is proposed which enables accurate addition of signal voltages without requiring precisely matching and linear components. A 1.5-bit algorithmic stage based on this floating-hold-buffer is presented and analysed in which voltage multiplication is replaced by voltage addition. The new technique is compared against existing techniques from the literature and the relative benefits are analysed.

### 9.1 The ADC Algorithm Re-visited

To emphasize the hardware pertaining to existing implementations, the residue transfer function of equation (8.1) is rewritten as:

$$
\begin{equation*}
V_{\text {out }}=2 \times V_{\text {in }}-1 \times D \cdot V_{r e f} . \tag{9.1}
\end{equation*}
$$

The multiplier factors (1 and 2) depend on capacitor ratios in existing charge transfer hardware realizations of this equation. Charge is actively transferred from capacitor to capacitor via the virtual earth node of an OTA so that the accumulated charge on the feedback capacitor of the OTA produces $V_{\text {out }}$ (e.g. the contemporary SC implementation of Fig. 8.4). This method is limited by the inaccuracies of capacitor matching as well as any non-linearity of capacitors. Both the gain accuracy and 1.5 -bit sub-DAC output levels shifts are affected (see equation (8.20) and Fig. 8.8).

In the method proposed here, the MX2 (multiply-by-2) stage is implemented without using multiplication (i.e. charge transfer) but instead an accurate analogue adder is employed. Furthermore, the sub-DAC voltage is added without the need for charge transfer. In fact, formula (9.1) is rewritten as $V_{\text {out }}=V_{\text {in }}+V_{\text {in }}-D \cdot V_{\text {ref }}$ to emphasize implementation. This will be presented next.

(a)


(f)

Fig. 9.1 Methods for creation of MX2 function with (a) charge transfer $C \rightarrow 2 C$, with a realization (b); (c) charge transfer and flip around $C \rightarrow C$, with a realization (d); (e) voltage adder $C+C$ with components for realization ( $f$ ).

### 9.2 Review of SC Concepts for Analogue Addition

In this section, a concept is presented for implementing the arithmetic operations (9.1) of the ADC in analogue hardware without using multiplication. Analogue multiplication, within the context of a SC circuit, is a series of voltage-to-charge and charge-to-voltage conversions known also as the charge transfer technique ( $Q T$ ).

Typical concepts for creation of the MX2 function are shown in Fig. 9.1(a), (c). Voltage multiplication by 2 occurs in Fig. 9.1(a) $(C \rightarrow 2 C)$ through the charge transfer of $Q=V_{0} \cdot 2 C$ of capacitor $C_{1}=2 C$ to another capacitor $C_{2}=C$, initially discharged, via a virtual earth node
to become $2 V_{0}$ [88]. This method is sensitive to the ratio of capacitors $C_{1} / C_{2}$. An adaptation of this method is shown in Fig. 9.1(c), which is called a charge transfer with flip-around technique $(C \rightarrow C)$, where both $C_{1}=C$ and $C_{2}=C$ are pre-charged with $V_{0}$, after which the charge on $C_{1}$ is transferred to $C_{2}$ [90], [91]. A half bit of extra accuracy can be achieved with the $C \rightarrow C$ circuit compared to the $C \rightarrow 2 C$ circuit but in practical applications no better than 9-10-bits accurate multiplication-by-2 is realistic nor has been shown possible using these methods in standard CMOS processes. Example implementations of these $Q T$ multiplication concepts are demonstrated in figures Fig. 9.1(b),(d), where the virtual earth node is created within the feedback loop of an OTA. The 1.5 -bit sub-DAC function is also created by multiplying the DAC voltage by a factor of 1 (nominally $\left.\left(C_{1}=C\right) \div\left(C_{2}=C\right)\right)$ through charge transfer via the virtual earth node to the output capacitor $C_{2}$. This DAC charge is added to the signal charge in $C_{2}$ to create the ADC stage function.

An alternative concept $(C+C)$, which is new for creation of the MX2 function, is based on voltage addition [P.8], [P.25]. Capacitors can be used for addition, as demonstrated in Fig. 9.1(e), where instead of multiplying $V_{0}$ by 2 , voltage addition occurs by first charging each of $C_{1}$ and $C_{2}$ to $V_{0}$ and then placing these capacitors end to end, with say the plate (3) of $C_{2}$ connected to plate (2) of $C_{1}$. Furthermore, to fulfil the 1.5 -bit sub-DAC function, the output can be easily and independently level shifted by adding a voltage at plate (2) of $C_{1}$. This concept is an example of orthogonalization (Chapter 2) of the ADC design process, in that the actual common multiplication of the signal and DAC voltages in traditional methodologies is split out into separate independent functions in this new proposal, based on simple addition within the same circuit stage.

When realized in a CMOS process, both top- and bottom-plate terminals of $C_{1}, C_{2}$ have parasitic coupling capacitance. This parasitic capacitance results in an inaccurate MX2 function. While the $C+C$ concept of Fig. 9.1(e) is simple, its accurate implementation is difficult Fig. 9.1(f). In fact, direct implementation of the $C+C$ concept is only suitable for low resolution ADCs of less than 8-bits.

### 9.3 The Floating-Hold-Buffer for Accurate Analogue Addition

A method is proposed in this section to accurately implement the basic voltage summation concept ( $C+C$ ) of Fig. 9.1(e), i.e. a way of stacking capacitors (with pre-defined voltages) with high accuracy. To this end, a floating-hold-buffer [P.7], [P.11] is proposed with one input and one output, where the output voltage is defined by the input voltage plus a fixed offset (the hold voltage), the offset being held independently of the input voltage (i.e. of the form $V_{\text {out }}=V_{\text {hold }}+V_{\text {in }}$ ).

Usually a single capacitor ( $C$ ) is used to sample and hold a voltage - see, for example, Fig. 9.2(a),(b). Assume that $C$ is used as a floating hold capacitor so that the only way for charge to escape from its top plate terminal is through the parasitic capacitor $C_{p a r}$ associated with the top plate - Fig. 9.2(c). The voltage across $C$ in the hold mode is then given by:

$$
\begin{equation*}
V_{\text {hold }}=V_{\text {hold }_{0}}+V_{A} \cdot \frac{C_{p a r}}{C} \tag{9.2}
\end{equation*}
$$

where $V_{\text {hold }}^{0}$ is the initial correct value of the hold voltage at the sample moment and $V_{A}$ is a floating voltage at node A. According to (9.2), $V_{\text {hold }}$ depends on $V_{A}$. This limits the quality of the floating voltage hold circuitry employing a single sampling capacitor $C$.

Consider now two such capacitors used to sample $V_{C 1_{0}}, V_{C 2_{0}}$ - Fig. 9.3(a). The equations for the voltages across each of $C_{1}, C_{2}$ in the hold mode, Fig. 9.3(b), are:

$$
\begin{equation*}
V_{C 1}=V_{C 1_{0}}+V_{A} \cdot \frac{C_{p a 1_{1}}}{C_{1}}, \quad V_{C 2}=V_{C 2_{0}}+V_{B} \cdot \frac{C_{p a r_{2}}}{C_{2}} . \tag{9.3}
\end{equation*}
$$

If we now set the condition in the hold mode that the voltages at the capacitor top plates are held equal, i.e. $V_{A}=V_{B}$, then the voltage held across both capacitors of Fig. 9.3(b) becomes:

$$
\begin{equation*}
V_{C 1}-V_{C 2}=\left(V_{C 1_{0}}-V_{C 2_{0}}\right)+V_{A} \cdot\left(\frac{C_{p a 1_{1}}}{C_{1}}-\frac{C_{p a r_{2}}}{C_{2}}\right) . \tag{9.4}
\end{equation*}
$$

Defining the voltage held as $V_{\text {hold }}=V_{C 1}-V_{C 2}$, with the initial correct hold voltage at the sample moment given by $V_{\text {hold }_{0}}=V_{C 1_{0}}-V_{C 2_{0}}$, equation (9.4) can be re-written as:

$$
\begin{equation*}
V_{\text {hold }}=V_{\text {hold }_{0}}+V_{A} \cdot\left(\frac{C_{p a 1_{1}}}{C_{1}}-\frac{C_{p a_{2}}}{C_{2}}\right) . \tag{9.5}
\end{equation*}
$$

Since $\left|\frac{C_{p a \eta_{1}}}{C_{1}}-\frac{C_{p a r_{2}}}{C_{2}}\right| \ll \frac{C_{p a r}}{C}$, then hold voltage (9.5) is significantly less sensitive to $V_{A}$ when compared to equation (9.2) for a single capacitor implementation. Recall that $V_{A}=V_{B}$, and the only path for the top plate charge to escape is through the parasitics. This implies that nodes A and $B$ must be physically disconnected.

Fig. 9.3(c) shows the implementation of the floating hold circuitry employing $C_{1}, C_{2}$ and a single-ended OTA. The OTA equalizes the voltages at the top plates of $C_{1}$ and $C_{2}$ by means of the negative feedback loop through $C_{1}$, thus satisfying $V_{A}=V_{B}$ of (9.5). $V_{\text {in }}$ drives the bottom plate of $C_{2}$ causing a corresponding change in node voltage B at the OTA positive input. The hold voltage $V_{\text {hold }}$ defined across $C_{1}$ and $C_{2}$ is insensitive to the voltage at the input terminal $V_{i n}$. For each capacitor $C_{1}$ and $C_{2}$, there is only parasitic charge displacement between the top plate and the parasitic coupling capacitance connected to the top plate at the OTA input side. This is another example of the application of delta-charge-flow $(\delta-Q)$ techniques (defined in Chapter 2) in that charge flow between the signal capacitors via the OTA virtual earth node is purely due to the presence of parasitic nodal capacitance.


Fig. 9.2 (a) Sampling cap during sample phase, (b) sampling cap within hold circuitry, and (c) its connection to high impedance input of active element during hold phase.


Fig. 9.3 (a) $C_{1}$ and $C_{2}$ in sample phase, (b) hold phase, (c) proposed implementation using amplifier.

This high accuracy floating-hold-buffer operates such that the output is unity gain buffered from the input while maintaining a fixed pre-determined hold voltage between output and input. This is the fundamental building block needed for accurate voltage addition.

### 9.4 Implementation of $\boldsymbol{C}+\boldsymbol{C}$ ADC Stage

This section develops an application of the $C+C$ concept to a 1.5 -bit algorithmic ADC stage for use in cyclic and pipelined ADCs [P.25]. Recall that all the arithmetic required to carry out equation (9.1) can be done with analogue voltage addition. Since the resolution of the algorithmic ADC is limited by the precision with which (9.1) can be implemented, the accurate floating buffer of section 9.3 is employed.

An input voltage is sampled using two pairs of capacitors $C_{1_{a}}, C_{2_{a}}$ and $C_{1_{b}}, C_{2_{b}}$ - see Fig. 9.4. Each of these pairs of capacitors is used to create the feedback of a floating-holdbuffer of Fig. 9.3(c). A single-ended implementation of the $1.5-$ bit ADC stage is shown in Fig. 9.4(b). Two floating-hold-buffers connected in series double the sampled voltage. This function creates the MX2, while the toggle switch in Fig. 9.4(b) represents the connection to the 1.5 -bit sub-DAC and hence this fulfils the implementation of the arithmetic of (9.1). Note that if each floating-hold-buffer has the same single-pole settling, then the settling time of both buffers in series increases by just one time constant. For a 12 -bit ADC, this means a $12 \%$ reduction in speed compared to a single buffer circuit.

The differential configuration - defined in [103] - assumes that any signal propagates undisturbed through a pair of traces with identical impedance and coupling to surrounding components and signals. The differential configuration is preferred to the single-ended because, for example, of improved noise immunity and linearity. A differential implementation of the $C+C$ concept is shown in Fig. 9.4(c). Note that in order to obtain a differential architecture, a series connection of floating-hold-buffers is replaced by a star connection. One floating buffer with $C_{1_{a}}, C_{2_{a}}$ is used to obtain an accurate buffered version of the input, while
the other floating buffer with $C_{1_{b}}, C_{2_{b}}$ creates an accurate inversion so that the output voltage is double that of the input. The connection to the differential 1.5 -bit sub-DAC is again represented by the two toggle switches. This is then the differential implementation of (9.1).

Another feature of the differential 1.5 -bit ADC stage proposed in Fig. 9.4(c) is that it is inherently common-mode stable, unlike conventional differential ADCs employing charge transfer techniques which require common-mode feedback to achieve stability. Furthermore, because the sampling technique in Fig. 9.4(a) is well suited to both differential and singleended sampling, and because the circuits in Fig. 9.4(b), (c) are suitable for driving singleended and differential lines, respectively, it is easy to build very accurate single-ended to differential and differential to single-ended conversion using the proposed design solutions.

The proposed merged implementation of the 1.5 -bit ADC stage of Fig. 8.1, comprising the $\mathrm{S} \& \mathrm{H}, \Sigma, \mathrm{MX} 2$ and 1.5 -bit sub-DAC is demonstrated in Fig. 9.5. The ADC using the $C+C$ technique is fully differential with the signal range given by $V_{\text {ref }}=\left(V_{\text {refp }}-V_{\text {refn }}\right)$. Assume that the DAC output is initially at $V_{\text {refcm }}$, i.e. differential 0 V ; then on a given cycle of the ADC, say phase 1, differential output voltage $V_{\text {out }}=V_{0}$ is present across the series combination of $C_{3_{a}}$ and $C_{3_{b}}$ placed in parallel with the series combination of $C_{4_{a}}$ and $C_{4_{b}}$. On the following cycle, phase $2, V_{0}$ is applied across the top OTA with $C_{3_{a}}$ between the top OTA output and its negative input and $C_{3_{b}}$ placed between the OTA positive input and the top output terminal of the DAC. Similarly, across capacitors $C_{4_{a}}$ and $C_{4_{b}}$, a further $V_{0}$ is available between the bottom output of the DAC and the output of the bottom OTA. The net effect after phase 2 is that a voltage of $V_{\text {out }}=2 \times V_{0}$ is present between both output terminals of the OTAs. If the DAC voltage should change to either $+V_{\text {ref }}$ or $-V_{\text {ref }}$, then $V_{\text {out }}$ is directly shifted by either $+V_{\text {ref }}$ or $-V_{r e f}$ with no charge transfer errors.


Fig. 9.4 Proposed C + C MX2, Summer and 1.5-bit sub-DAC level shift, (a) pre-charge phase, (b) single-ended, (c) differential.


Fig. 9.5 Proposed implementation of $C+C$ 1.5-bit ADC stage.

### 9.5 Practical Performance Issues

The maximum resolution of a practical switched capacitor 1.5-bit ADC stage is limited primarily by capacitor mismatch and less so by finite amplifier gain and charge feedthrough from the switches. For the purposes of comparison, the popular $C \rightarrow C$ technique is evaluated and compared with the proposed $C+C$ technique for the implementation of the 1.5 -bit ADC stage. Similar capacitors are assumed to be used in both cases for the sampling and processing of the differential input signal, Fig. 9.6(a).

Consider first the $C \rightarrow C$ circuit in hold mode, Fig. 9.6(b), with all relevant parasitic capacitances included. The transfer function, including capacitor mismatch, is:

$$
\begin{equation*}
V_{\text {out }_{C \rightarrow C}}=V_{\text {in }} \cdot 2 \cdot\left(1+\frac{1}{2} \cdot \frac{\Delta C}{C}\right)-D \cdot V_{r e f} \cdot\left(1+\frac{\Delta C}{C}\right), \tag{9.6}
\end{equation*}
$$

where the relative signal capacitor mismatch is given by $\Delta C / C=\frac{1}{2} \cdot\left(\Delta C_{1} / C_{1}+\Delta C_{2} / C_{2}\right) \cdot$ Here, it is assumed that $\Delta C \ll C$. Finite amplifier gain deteriorates the transfer function even further to produce a total fractional transfer gain error of:

$$
\begin{equation*}
\varepsilon_{C \rightarrow C}=\frac{1}{2} \cdot \frac{\Delta C}{C}-\frac{1}{A_{0} \cdot \beta_{C \rightarrow C}}, \tag{9.7}
\end{equation*}
$$

where the feedback factor $\beta_{C \rightarrow C}$ is given by:

$$
\begin{equation*}
\beta_{C \rightarrow C}=\frac{C}{2 \cdot C+2 \cdot C_{p a r_{12}}+C_{p a r_{1}}} . \tag{9.8}
\end{equation*}
$$



Fig. 9.6 (a) Differential input sampling; Comparison of (b) $C \rightarrow C$ and (c) $C+C$ circuit architectures after inclusion of parasitic nodal capacitors.

Due to the strong influence of capacitor mismatch on the $C \rightarrow C 1.5$-bit stage, no better than $0.1 \%$ gain error can be expected so that some form of calibration or trimming must be used to achieve an ADC accuracy of greater than 10-bits. Calibration usually adds latency to the cyclic ADC (e.g. by a factor of 4 in [104]) and increases area and power consumption not only as a result of the added calibration circuitry but because of the extra parasitic loading on analogue circuit nodes and the consequent increase in amplifier power.

Consider next the $C+C$ 1.5-bit ADC stage of Fig. 9.6(c) with its associated signal capacitors and parasitic nodal capacitors. The voltage transfer function of the $C+C$ stage is:

$$
\begin{equation*}
V_{\text {out }_{C+C}}=V_{\text {in }} \cdot\left(1+\left(\frac{C_{2}}{C_{2}+C_{p a r_{2}}}\right) \cdot\left(\frac{C_{1}+C_{\text {par }}}{} C_{1}\right)\right)-D \cdot V_{\text {ref }} \cdot\left(\frac{C_{2}}{C_{2}+C_{p a r_{2}}}\right) \cdot\left(\frac{C_{1}+C_{p a r_{1}}}{C_{1}}\right) . \tag{9.9}
\end{equation*}
$$

Defining $\Delta C_{p a r} / C_{p a r}=\frac{1}{2} \cdot\left(\Delta C_{p a r 1} / C_{p a r 1}+\Delta C_{p a r 2} / C_{p a r 2}\right)$ as the relative mismatch of the equivalent input parasitic capacitors $C_{p a r_{1}}$ and $C_{p a r_{2}}$, equation (9.9) can be rewritten as:

$$
\begin{equation*}
V_{o u t}^{C+C}=2 \cdot V_{\text {in }} \cdot\left(1+\frac{C_{\text {par }}}{2 C} \cdot\left(\frac{\Delta C_{p a r}}{C_{p a r}}+\frac{\Delta C}{C}\right)\right)-D \cdot V_{\text {ref }} \cdot\left(1+\frac{C_{\text {par }}}{C} \cdot\left(\frac{\Delta C_{\text {par }}}{C_{p a r}}+\frac{\Delta C}{C}\right)\right) . \tag{9.10}
\end{equation*}
$$

A small transfer error is produced proportional to $C_{p a r} / C$ times the mismatch of the signal and parasitic capacitors. Note that the extra term of $\Delta C_{p a r} / C_{p a r}$ must be accounted for when calculating the effect of mismatch. After inclusion of the effect of the amplifier, the total gain error of the $C+C$ stage becomes:

$$
\begin{equation*}
\varepsilon_{C+C}=\frac{1}{2} \cdot\left(\frac{C_{p a r}}{C}\right) \cdot\left(\frac{\Delta C_{p a r}}{C_{p a r}}+\frac{\Delta C}{C}\right)-\frac{1}{\beta_{C+C}} \cdot\left(\frac{1}{A_{0}}+\frac{1}{2 \cdot C M R R}\right), \tag{9.11}
\end{equation*}
$$

with the feedback factor being given by:

$$
\begin{equation*}
\beta_{C+C}=\frac{C}{C+2 \cdot C_{p a r_{12}}+C_{p a r_{1}}} . \tag{9.12}
\end{equation*}
$$

Clearly, the intention is to make $C_{p a r} \ll C$ in order that the $C+C$ stage approach the ideal transfer, independent of the matching of $C$ or $C_{p a r}$. For an $N$-bit pipelined or cyclic ADC having at least 0.5 -bit accuracy, the required matching from Chapter 8 is $\sigma_{\varepsilon_{C+C}} \leq \frac{1}{3 \cdot 2^{N+1}}$.

OTA design techniques allow the attainment of very high $A_{0}$ and CMRR sufficient for at least 15-bit accuracy. Indeed the DC CMRR can be designed to be of the same order of magnitude as $A_{0}$ which is explained in Chapter 10. It is the capacitor matching that is the bottle neck to achieving higher than 10 bits accuracy in charge transfer based 1.5 -bit stage configurations, such as the $C \rightarrow C$ method.

Comparing formulae (9.7) and (9.11), the capacitor mismatch error of the $C+C$ method is reduced by $1 /\left(\frac{C_{\text {par }}}{C} \times\left(1+\frac{\Delta C_{p a r} / C_{p a r}}{\Delta C / C}\right)\right)$ compared to the $C \rightarrow C$ method. The relative capacitor mismatch errors are given by $\Delta C / C \propto 1 / \sqrt{C}$ and $\Delta C_{p a r} / C_{p a r} \propto 1 / \sqrt{C_{p a r}}$. From Chapter 10 , a $C / C_{p a r}$ ratio of 35 has been obtained in a $0.25 \mu \mathrm{~m}$ CMOS design. The matching of the parasitic capacitors (composed of both metal-metal and gate-oxide) are expected to be at least as good as the signal capacitors (metal-metal only), so that a conservative estimate for the improvement in capacitor mismatch error of the $C+C$ method compared to the $C \rightarrow C$ method is $\boldsymbol{C} / 2 C_{p a r}$. This implies (1) an extra 4 bits un-calibrated accuracy (linearity) is possible over previous 1.5 -bit conversion stages. Since the capacitors determine the efficiency of

Table 9.1 Performance comparison of all 3 ADC circuit architectures

|  | $C \rightarrow 2 C$ | $C \rightarrow C$ | $C+C$ (proposal) |
| :---: | :---: | :---: | :---: |
| Cap mismatch | $\frac{\Delta C}{C}$ | $\frac{1}{2} \cdot \frac{\Delta C}{C}$ | $\frac{1}{2} \cdot \frac{\Delta C}{C} \cdot \frac{2 \cdot C_{p a r}}{C}$ |
| Fdbk factor, $\beta_{f b}$ | $\begin{aligned} & \frac{C}{3 \cdot C+2 \cdot C_{p a r 12}+C_{p a r 1}} \\ & \approx 1 / 3 \end{aligned}$ | $\begin{aligned} & \frac{C}{2 \cdot C+2 \cdot C_{p a r 12}+C_{p a r 1}} \\ & \approx 1 / 2 \end{aligned}$ | $\begin{aligned} & \frac{C}{C+2 \cdot C_{p a r 12}+C_{p a r 1}} \\ & \approx 1 \end{aligned}$ |
| $A_{0}(\mathrm{~dB})$ for min 12-bit accuracy | 88dB | 84dB | 78dB |
| Equivalent cap, $C_{L_{e f f}} / \beta_{f b}$ | $\begin{aligned} & 22 / 3 \cdot C+\left(C_{\text {outpar }}+C_{\text {par } 12}+\frac{C_{\text {par } 1}}{2},\right. \\ & \approx 3 \times 22 / 3 \cdot C \end{aligned}$ | $\begin{aligned} & 21 / 2 \cdot c+\left(C_{\text {ouppar }}+C_{\text {par } 12}+\frac{C_{\text {par } 1}}{2}\right) \\ & \approx 2 \times 21 / 2 \cdot C \end{aligned}$ | $\begin{aligned} & 2 \cdot c+\left(C_{\text {oupar }}+C_{\text {par } 12}+\frac{C_{\text {par } 1}}{2}\right) \\ & \approx 2 \cdot C \end{aligned}$ |
| O/P Noise power | $6 \cdot \frac{k T}{C}+3 \cdot N_{\text {OTA }}$ | $4 \cdot \frac{k T}{C}+2 \cdot N_{\text {OTA }}$ | $2 \cdot \frac{k T}{C}+N_{\text {OTA }}$ |
| Power (for same speed) | $8 \cdot C \cdot\left(V_{D D} \cdot \frac{V_{\text {on }}}{2} \cdot \frac{1}{\tau}\right)$ | $5 \cdot C \cdot\left(V_{D D} \cdot \frac{V_{\text {on }}}{2} \cdot \frac{1}{\tau}\right)$ | $2 \cdot C \cdot\left(V_{D D} \cdot \frac{V_{\text {on }}}{2} \cdot \frac{1}{\tau}\right)$ |

the ADC, it is possible to create a highly efficient architecture using the proposed $C+C$ method giving rise to low power and small silicon area compared to previous techniques. A second benefit of the $C+C$ ADC architecture is that it is (2) relatively insensitive to capacitor non-linearity so that, for instance, small area gate-oxide capacitors may be used as signal capacitors.

The dynamic performance of the $C+C$ is also much improved compared to previous $C \rightarrow C$ techniques. (3) The feedback factor of the $C+C$ stage is approximately 1 , and almost double that of the $C \rightarrow C$. The benefits of a larger feedback factor are to be found in improved amplifier gain, lower power and lower noise. Note that the noise power of the $C+C$ ADC stage is decoupled from the gain of the stage. Switch charge feedthrough is largely cancelled at the input of each OTA due to the differential switching scheme, the balanced input impedances and voltage levels. The appropriate use of early clocking ensures that the residue output of the $C+C 1.5$-bit stage is cleanly sampled by the following stage before the switches connected around the OTA change phase. Finally, (4) no CMFB is required in a differential realization, further reducing power and improving overall stability and ruggedness. A summary of the relative performances of the existing $C \rightarrow 2 C, C \rightarrow C$ and the proposed $C+C$ circuit techniques is presented in Table 9.1.

### 9.6 Conclusions

A novel implementation of the 1.5 -bit algorithmic ADC stage for use in both cyclic and pipelined ADCs has been presented. Voltage multiplication has been replaced by accurate addition ( $C+C$ concept) and a floating-hold-buffer has been proposed for its implementation. The accuracy of the ADC employing the new circuitry is less sensitive to the matching accuracy and linearity of the sampling capacitors compared to previous circuit techniques presented in the literature.

An analytical equation has been obtained of the transfer error of the proposed algorithmic stage and it is compared with the analytical equation of the traditional charge-transfer algorithmic stage. With $C$ the value of the sampling capacitors and $C_{p a r}$ the parasitic capacitance at each differential amplifier input terminal, the proposed algorithmic stage has its sensitivity to capacitor mismatch reduced by a factor of $C / 2 C_{p a r}$ giving a corresponding improvement in linearity. Ensuring that $C_{p a r} \ll C$ suggests a high resolution ADC stage (12bits and beyond) can be practically realized without the need for calibration. Further performance benefits of the proposed $C+C$ based ADC circuit architecture include (2) low sensitivity to capacitor non-linearity, (3) improved feedback factor (almost unity) for low power and noise, and (4) no CMFB is needed for differential realizations.

## Chapter 10

## High-Accuracy ADC Design And Measurements

The main bulk of this chapter is dedicated to the design for CMOS integration of the principal ADC circuit blocks. Firstly, a high-level system overview is given of both measurement type and signal-chain type ADCs. Next, a new flexible track-and-hold (T\&H) is presented and discussed. The circuit implementation of the proposed cyclic ADC is then presented. A separate section is devoted to a proposed single-ended OTA with high CMRR, since it is a key circuit block needed for high quality operation of the T\&H and ADC. Finally, measurement results are documented of the fabricated 12-bit cyclic ADC, as well as simulation results of two laid out pipelined ADCs for 10-bit and 14-bit applications. They serve to demonstrate the potential of the $C+C$ concept to achieving uncalibrated high-accuracy or high-speed. The performances of these circuits in terms of their power and area figures-of-merit (FOMs) are compared to those of other published ADCs of the recent past.

### 10.1 System Overview

The ADC design at system level is reviewed in this section. A distinction is made between precision measurement applications and high-bandwidth communications applications. Different possible modes of operation of the ADC are discussed in order to provide a background for the descriptions of the various implementations later on in the chapter.

### 10.1.1 Application Space

There is an increasing trend to embed ADCs with the digital CMOS VLSI for applications requiring medium to high resolutions (10-14-bits) at sample frequencies up to a few MHz . This reduces cost, board space and board complexity, pin count and overall power consumption. For instance, such ADCs have become a ubiquitous peripheral in micro-controllers for servo applications, touch screens, measurement of supplies and die/board temperatures, etc. They are integrated as a small block on to the same digital substrate as the main digital


Fig. 10.1 $A D C$ system overview.
processing circuits. They need to be highly robust to work in a hostile digital VLSI environment. High speed ADCs, on the other hand, are still predominantly off-chip as standalone units mostly because older, well characterized IC processes are still needed to guarantee ADC performance and yield.

The cyclic ADC is an excellent choice of architecture for applications where die area and power consumption are at a premium and it is highly suitable to digital co-integration. On the other hand, the pipelined ADC is an excellent choice for applications demanding high speed with good linearity, such as in analogue receiver front-ends and other high-performance communications applications. Note that in such signal-chain applications, the linearity requirement is more important than the noise requirement. This is because noise can be filtered down the chain as the required channel(s) are usually highly over-sampled. On the other hand, intermodulation and harmonic distortion are directly related to the linearity of the converter and may not be easily removed. Conventionally, for signal-chain pipelined ADCs, resolution is determined by linearity not $S N R$. So, say, a 14-bit ADC might be linear to 14-bits but have an SNR of 72 dB which is only 12 -bits $E N O B$ using the conventional definition, section 7.6 [96], [97].

The core of both the cyclic and pipelined ADC is the highly efficient and robust 1.5 -bit algorithmic stage, the new $C+C$ implementation of which was presented in Chapter 9. It can be easily scaled in area and power down the pipeline for improved efficiency in pipelined converters, as detailed in Chapter 8.

### 10.1.2 ADC Architecture

A high-level block diagram of the cyclic or pipelined ADC is shown in Fig. 10.1. The Clock Generator provides various non-overlapping clocks and the Control Block allows the ADC to be configured for synchronous or asynchronous sampling and enter other specific modes of operation. The DEC block, described in section 8.1.2, composes the parallel $N$-bit output data, after correcting for comparator and amplifier offsets. The purpose of the (single) algorithmic block in the case of the cyclic converter, or the series of algorithmic blocks in the case of the pipelined converter, is to perform the arithmetic of (8.1). The algorithmic core is designed to be independent of the various modes of operation of the overall ADC system - see next section. These are taken care of by the T\&H. The flexible T\&H input stage delivers a fixed standardized sampled data signal to the ADC, independent of the type of analogue input signal


Fig. 10.2 Embedded monitoring application as part of a SoC.
received by the ADC system.
A measurement and monitoring application, which is part of a larger system on a chip, is demonstrated in Fig. 10.2. Besides the precision measurement ADC and reference generator, there are a number of other supporting circuits. Different integrated sensors detect die temperature as well as peaks, troughs and average values of many key internal voltages. External analogue inputs allow the ADC to monitor the physical environment of the circuit board or enclosure. An automatic channel sequencer allows a user-defined selection of the monitored parameters and specifies the order in which they are monitored. User programmable digital filtering is provided to reduce the noise of the measurement. As part of this monitoring application, user programmable alarm thresholds can also be set for the on-chip sensors. Thus, if an on-chip monitored parameter moves outside the user specified operating range, an alarm logic output becomes active. A register-file based interface allows easy access to the measured data and the control registers.

### 10.1.3 Flexible ADC Sampling Modes

For high accuracy voltage monitoring, quality differential sampling is needed even when sampling single-ended signals. The input is sampled with respect to the common mode noise source. The benefits of the concept are demonstrated with the help of Fig. 10.3. Common ground impedances $\left(R_{G}\right)$ can easily couple noise (e.g. spikes due to fast switching digital circuits) into other parts of the system. Noise of the order of 100 mV is typical in a printed circuit board subsystem which could cause 100's of LSBs errors in say a 12-bit ADC and consequently large measurement inaccuracies. The differential sampling scheme adopted here samples the signal (with the accompanying noise) on one terminal $\left(V_{p}\right)$ and the common mode noise only on the other terminal $\left(V_{n}\right)$. The noise is subtracted from the signal in the front-end $\mathrm{T} \& \mathrm{H}$, since it captures the difference between $V_{p}$ and $V_{n}$, and the cleaned-up signal is presented to the ADC for digitization. A high common-mode rejection is achieved which


Fig. 10.3 Equivalent differential input sampling scheme.
improves ADC performance in harsh noisy digital environments. There are three differential sampling modes for the ADC system, namely unipolar, bipolar and fully differential. These are explained briefly in the following.

### 10.1.3.1 Unipolar Mode

Unipolar operation is demonstrated conceptually in Fig. 10.4. The transfer function was shown in Fig. 7.2(a). The differential analogue input $\left(V_{p}-V_{n}\right)$ has an input range of 0 V to $V_{\max }$, where $V_{\max }$ is determined by the maximum signal voltage that can be handled by the ADC system. In this mode, $V_{p}$ is always positive with respect to $V_{n}$. Fig. 10.3 shows a typical application requiring unipolar sampling. The $V_{n}$ input is typically connected to a local ground or common mode signal. The common mode signal can vary from -0.1 V to 0.5 V typically (measured with respect to ground). If say the maximum input signal range is 0 V to $1 \mathrm{~V}\left(V_{p}-V_{n}\right)$, then the maximum signal on $V_{p}$ is 1.5 V so that the ADC can safely operate from a 2 V voltage supply. Typical applications for unipolar operation are power supply monitoring and temperature monitoring (via measuring the junction voltage of a diode).

### 10.1.3.2 Bipolar Mode

Fig. 10.5 shows conceptually the ADC operation in bipolar mode. The transfer function was shown in Fig. 7.2(b). In this mode, $V_{p}$ can swing either positive or negative with respect to $V_{n}$. Indeed, the signals on the positive and negative inputs can be unrelated AC signals having different DC levels. In Fig. 10.5, the maximum differential signal $\left(V_{p}-V_{n}\right)$ allowed is say $V_{p p}=1 \mathrm{~V}$, while the voltages on either of $V_{p}$ or $V_{n}$ cannot exceed $V_{\max }=1.5 \mathrm{~V}$ say but may go below 0 V .


Fig. 10.4 Equivalent unipolar analogue input sampling scheme.


Fig. 10.5 Equivalent bipolar analogue input sampling scheme.

The common mode signal on $V_{n}$ can vary between +0.5 V and 1 V . $V_{p}$ can swing $\pm 0.5 \mathrm{~V}$ around $V_{n}$. The peak voltage allowed on $V_{p}$ is then 1.5 V with respect to ground. The output code in bipolar mode is typically 2 's complement. An example of a bipolar application is a ratiometric measurement such as measuring the voltage differentially across a Wheatstone Bridge - see Fig. 10.6.

### 10.1.3.3 Fully differential mode

Fig. 10.7 shows fully differential operation of the ADC system. This mode is in fact the bipolar mode with the inputs driven differentially. The maximum voltage on $V_{p}, V_{n}$ is $V_{\max }$, while the common mode range is given by $V_{\max }-2 \cdot V_{p k}$. This mode is principally used for the acquisition of fully differential signals in a communications application.


Fig. 10.6 Bipolar application showing digitization of transducer outputs.


Fig. 10.7 Fully differential ADC operation and corresponding ADC range.

### 10.2 Proposed Reconfigurable Track-and-Hold

The most advanced T\&Hs currently available are based on what is often referred to as the "flip-around" sample-and-hold circuit architecture of the form shown in Fig. 8.4 [96]. These T\&Hs are inflexible in dealing with the broad range of input signals described in 10.1.3 required for measurement applications. The T\&H presented here uniquely provides a solution for combining all the possible modes of operation of the complete ADC (Fig. 10.1) in to one block. It alone determines the mode of operation of the complete ADC. The algorithmic ADC block following the T\&H need have no knowledge of the type of analogue signal at the ADC system input since, regardless of the type of analogue signal received, the T\&H always delivers a fully differential sampled data signal to the algorithmic ADC block which is limited to within the full-scale-range $(F S)$ of the $\mathrm{ADC}\left(V_{\text {refp }}-V_{\text {refn }}\right)$ and which is set at the correct com-mon-mode level for it to operate optimally $\left(V_{r e f c m}\right)$. It will be shown here that the T\&H can combine all the following functions of a) single-ended to differential conversion, b) processing
unipolar signals, c) processing bipolar signals, and d) processing fully differential signals.
The proposed T\&H [P.27], the circuit diagram of which is shown in Fig. 10.8, is realized using the floating-hold-buffer of Chapter 9 . Two common mode voltages are defined, namely the external common mode voltage $V_{\text {ext } c_{c m}}$ and the internal common mode reference voltage $V_{r e f c m}$. The value of $V_{\text {ext } c_{c m}}$ depends on whether unipolar or bipolar operation is chosen, whereas $V_{\text {refcm }}$ is always set approximately half way between the positive and negative references (or half $F S$ ), i.e. $V_{\text {refcm }}=\left(V_{\text {refp }}+V_{\text {refn }}\right) / 2$. The T\&H circuit takes care that the common voltage of the $\mathrm{T} \& \mathrm{H}$ amplitier is equal to $V_{\text {refcm }}$ and that $V_{\text {ext }}$ does not influence this common mode voltage. The clocks associated with the T\&H and ADC are shown later in Fig. 10.10.

### 10.2.1 The T\&H in Unipolar Mode

Consider first unipolar operation. $V_{\text {ext }}^{c m}$ is connected to 0 V to ensure that $V_{i n_{p}}$ and $V_{i n_{n}}$ are sampled directly with respect to the lowest expected input level, i.e. ground. Furthermore, $\mathrm{S}_{1}$ connects to $V_{\text {refn }}$ during the hold time when hld_clk is high, while $\mathrm{S}_{2}$ connects to $V_{\text {refp }}$. Looking at the top half of the T\&H of Fig. 10.8, when smp_clk is high, $V_{i n_{p}}$ is sampled across $C_{1_{a}}$ with respect to ground ( 0 V ). Similarly, $V_{i n_{n}}$ is sampled across $C_{1_{b}}$ with respect to ground. The amplifier external nodes are reset to $V_{\text {refcm }}$. Note, to ensure clean, non-signal dependent sampling of the analogue input signal, the following procedure needs to be followed. The switches


Fig. 10.8 Proposed configurable track-and-hold.
connected to $V_{\text {ext }}^{c m}$ must switch off before all the other switches. Furthermore, the input switches connected to $V_{i n_{p}}$ and $V_{i n_{n}}$ need to be relatively large to ensure a small resistance with low signal dependency. By switching off those switches connected to $V_{\text {ext }{ }_{c m}}$ first, a high impedance path is created through the signal capacitors $C_{1_{a}}$ and $C_{1_{b}}$. In this way, most of the signal dependent charge of the large input switches returns to the relatively low impedance signal source.

After the following clock transition, when $h l d \_c l k$ is high, $C_{1_{a}}$ is placed across the amplifier such that, between $V_{\text {out }_{p}}$ and the negative input terminal of the amplifier, a potential is created of the full value of $V_{i n_{p}}$ with respect to ground at the sampling instant (i.e. the instant when $s m p \_c l k_{-} e$ transitions from high to low). At the same time, $C_{1_{b}}$ is switched such that that side of $C_{1_{b}}$ which was connected to $V_{i n_{n}}$ during sampling, is now connected to $V_{\text {refn }}$ during the hold time, while the other side of the capacitor is connected to the positive input of the amplifier. The net effect is to create a voltage at $V_{\text {out }}^{p}$ which is equal to $V_{\text {in }_{p}}$ at the sampling instant from which the common unwanted voltage $V_{i n_{n}}$ has been stripped off. The maximum voltage that can appear on $V_{i n_{p}}$ is the full value of $V_{\text {refp }}$, while the maximum voltage that can appear on $V_{i n_{n}}$ is $V_{\text {refn }}$. The maximum difference voltage is therefore $V_{\text {refp }}-V_{\text {refn }}$, which is the full signal handling capability of the succeeding ADC. In the extreme case for example, with say $V_{\text {refp }}{ }^{-}$ $V_{\text {refn }}$ set at 1 V and $V_{\text {refn }}$ set at 0.5 V , then 1.5 V appears across $C_{1_{a}}$, while the negative terminal of the amplifier is brought right down to 0 V . Hence, $V_{\text {out }}$ is +1 V with respect to $V_{\text {refn }}$. Similarly for the bottom half of the circuit, except that $C_{2_{b}}$ now switches with respect to $V_{\text {refp }}$. So the bottom half of the circuit can also swing through the maximum signal range of $V_{\text {refp }}-V_{\text {refn }}$ but in anti-phase. In this way, a fully differential version of $V_{i n_{p}}$, with the common signal $V_{i n_{n}}$ removed, appears between the output terminals $V_{\text {out }_{p}}$ and $V_{\text {out }}^{n}$. Effectively, a single-ended to fully differential conversion of the wanted input signal has occurred and it is also shifted and placed neatly between $V_{\text {refp }}$ and $V_{\text {refn }}$. The signal $\left\{V_{\text {out }_{p}}, V_{\text {out }_{n}}\right\}$ can be further processed in the following ADC block as a fully differential signal.

### 10.2.2 The T\&H in Bipolar and Differential Modes

Consider next bipolar operation, in which case both switches $\mathrm{S}_{1}$ and $\mathrm{S}_{2}$ connect to $V_{\text {refcm }}$. Here, $V_{\text {ext } c m}$ should be chosen somewhere between $V_{\text {refn }}$ and $V_{\text {refcm }}$. For instance, as discussed in 10.1.3, if $V_{\text {refp }}$ is chosen as 1.5 V and $V_{\text {refn }}$ is chosen as 0.5 V , then $V_{\text {ext }}$ cm can be somewhere between 0.5 V and 1 V . Similar design reasoning is applied to the choice of switch sizes and their relative clock phases as was explained for unipolar operation. Looking again at the top half of the T\&H of Fig. 10.8: when smp_clk is high, $V_{i n_{p}}$ is sampled across $C_{1_{a}}$ with respect to $V_{\text {ext }}^{c m}$, while $V_{\text {in }_{n}}$ is sampled across $C_{1_{b}}$ with respect to $V_{\text {ext }}^{c m}$. At the same time, the inputs and output of the amplifier are reset to $V_{\text {refcm }}$. On the following period, when $h l d \_c l k$ is high, $C_{1_{a}}$ is placed across the amplifier, such that the difference between $V_{i n_{p}}$ and $V_{\text {refcm }}$ appears between $V_{\text {out }}^{p}$ and the negative amplifier input terminal. Meanwhile, $C_{1_{b}}$ is switched such that side of $C_{1_{b}}$ which was connected to $V_{i n_{n}}$ during sampling is connected to $V_{\text {refcm }}$, while the other side of the capacitor which was connected to $V_{\text {refcm }}$ is now connected to the positive input terminal of the amplifier. At the end of hld_clk, the positive output voltage becomes
$V_{\text {out }_{p}}=\left(V_{\text {in }_{p}}-V_{\text {in }_{n}}\right)+V_{\text {refcm }}$. The bottom half of the T\&H circuit operates in a similar manner, except that $V_{i n_{p}}$ and $V_{i n_{n}}$ are switched around, resulting in $V_{\text {out }}=\left(V_{i n_{n}}-V_{i n_{p}}\right)+V_{\text {refcm }}$. The net effect is to create a fully differential version of $\left(V_{i n_{p}}-V_{i n_{n}}\right)^{n}$ between the output terminals: $\left\{V_{\text {out }_{p}}, V_{\text {out }_{n}}\right\}$. Inputs $V_{\text {in }}$ and $V_{\text {in }}^{n}$ can be mutually independent and vary anywhere between 0 V and a maximum of $\frac{3}{2} \cdot\left(V_{\text {refp }}-V_{\text {refn }}\right)$.

The T\&H can also sample fully differential input signals in bipolar mode and process them such that they are placed neatly between $V_{\text {refp }}$ and $V_{\text {refn }}$ for further processing by a fully differential ADC. Thus the T\&H can be used in communications signal processing applications. It can also be used to subsample RF signals which can then be processed at lower speed in the ADC.

### 10.2.3 T\&H Summary

In summary, the proposed $\mathrm{T} \& \mathrm{H}$ accurately acquires the differential analogue input signal $\left(V_{i n_{p}}-V_{i n_{n}}\right)$, while stripping off the input common mode level, level shifts it so that it is placed between 2 reference levels $V_{\text {refn }}$ and $V_{\text {refp }}$, and holds the output so that it can be further processed by the following ADC (for instance, a cyclic or pipelined ADC). The block is such that all the various modes of operation of an ADC (as described in 10.1.3) can be determined purely by the appropriate configuration of the T\&H only. The subsequent ADC operates in exactly the same way, irrespective of the type of analogue input signal received via the T\&H. The circuit is fully symmetrical but no common-mode feedback circuit is needed. The solution is compact and requires just a single transfer between input and output. It is fast with a feedback factor of nearly 1 . The accuracy of the T\&H function is independent of both the matching accuracy and linearity of the signal processing capacitors used.

### 10.3 Proposed Cyclic ADC based on New Concept

The detailed circuit realization of a cyclic ADC, based on the $C+C$ concept presented in Chapter 9, is shown in Fig. 10.9. The waveforms governing the switching are shown in Fig. 10.10. All clocks are derived from mstr_clk which is provided off chip. The circuit operates in a double sampling manner with clocks $c l k 1$ and $c l k 2$ together with their early versions. The start of, say, a 12-bit conversion is determined by $A D C_{-}$clk going high, at which point the differential output of the $\mathrm{T} \& \mathrm{H}$ is sampled on $c l k 1$ via $V_{i n_{p}}, V_{i n_{n}}$ across $C_{1_{a}}$ and $C_{1_{b}}$ in series on the topside of the circuit, while it also sampled across $C_{2_{a}}$ and $C_{2_{b}}$ in series on the bottom side. At the same time, the T\&H signal is fed into the 1.5 -bit sub-ADC to obtain a coarse 2-bit representation of the input data which is fed into the DEC, which ultimately determines the MSB - see Fig. 10.1. Note that this read-in period overlaps with the read-out period of the last bit of the previous data word, i.e. the ADC is delivering the LSB of the previous analogue input sample while also reading in the next analogue sample for the following 12-bit conversion. In this way, a continuous conversion of the analogue input is obtained with no gaps, so that 12 cycles of the cyclic ADC produce 12 sequential bits and thus one data word. On ADC cycle 1, one $m s t r \_c l k$ period after being read in, the input signal is multiplied by 2 and the sub-DAC output


Fig. 10.9 Realization of cyclic ADC block based on $C+C$ method.


Fig. 10.10 Relative clock timings for $A D C$ and $T \& H$.
is subtracted off. The value of the sub-DAC output depends on what part of the voltage range $V_{\text {refn }}$ to $V_{\text {refp }}$ the input signal falls in to - see sections 8.1.1 and 9.4. The resulting output voltage across both amplifiers is then sampled by $C_{3_{a}}$ and $C_{3_{b}}$ in series, as well as $C_{4_{a}}$ and $C_{4_{b}}$ in series. This voltage is again fed to the sub_ADC to determine the MSB-1. For the 11 cycles following acquisition of the T\&H input signal, $A D C \_c l k$ is low and $A D C \_c l k \_n$ is high so that the differential output of the amplifiers is used as input for each following cycle or bit trial of the ADC. The last bit is determined absolutely and instantly with a 1-bit flash. A coarse 2-bit representation of the input signal per cycle is sent to the digital error correction (8.1.2) for decoding. There is no extra latency in this ADC so that, say for 12-b operation, each conversion of a sampled analogue input takes 12 clock cycles from MSB to LSB ( 1 clock delay for the $\mathrm{T} \& \mathrm{H}$ and 11 for the ADC ). At the end of the complete conversion cycle, a data ready signal (drdy) goes high, so that 12 -bit parallel data ( $N$-data) is ready to be accessed by a data bus during any of the 12 ADC bit trials of the following sample conversion.

### 10.4 Proposed Single-ended OTA with High CMRR

A high common-mode rejection ratio (CMRR) single-ended current-mirror OTA employing a novel current common-mode feedback (CMFB) is proposed here [P.9], [P.28]. The OTA input/output common mode range, die area, power and slewing are not affected by the addition of the CMFB circuit. However, the settling speed is reduced by $5-20 \%$. The current CMFB boosts the OTA CMRR by a factor of 30 while allowing integration of conventional OTA improvements. A unified approach relating the CMRR and transistor mismatches is proposed. The OTA was manufactured in a standard $0.25 \mu \mathrm{~m}$ CMOS process as a precision functional block of the 12-bit algorithmic ADC and T\&H.

### 10.4.1 The CMFB Requirement in Single-ended OTAs

The 12-bit differential algorithmic ADC that is at the core of this work cannot be implemented using differential OTAs. Instead, the ADC requires single-ended large input/output dynamic range OTAs with at least 78 dB CMRR and open loop gain. Single-stage OTAs are power efficient for high speed applications. The three primary OTA configurations, namely the telescopic, current mirror and folded cascode topologies were examined in detail in Chapter 4. The current mirror OTA provides a larger input/output dynamic range as compared to the telescopic OTA and, by means of the current mirror ratio, allows an efficient trade-off of power vs. speed which is not the case for the folded cascode OTA. A class A OTA with no push-pull action is preferred because it consumes a constant current and hence causes a minimum power supply noise. Based on these considerations a single-ended class A current mirror OTA with no push-pull action is chosen for the ADC and T\&H designs.

Contrary to the fully differential OTA, the single ended current mirror OTA does not have inherent first order cancellation of common mode signals [36]. A mechanism is required to guarantee the accurate tracking of the output common-mode level with respect to the input common-mode level. Thus while the 78 dB open loop gain can be achieved using standard


Fig. 10.11 Basic single-ended current mirror OTA.
design techniques, the targeted high CMRR is a design challenge that will be dealt with in this section.

Static CMRR for the conventional single ended current mirror OTA, depicted in Fig. 10.11, is given by:

$$
\begin{equation*}
C M R R=g_{m} \cdot R_{t}, \tag{10.1}
\end{equation*}
$$

where $g_{m}$ is the transconductance of the differential pair transistor M 1 or M 2 and $R_{t}$ is the impedance of the tail current source ( $r_{d s}$ for M5). Transistor non-idealities and mismatches produce an additional yet less significant contribution to the CMRR. The value of $g_{m}$ is usually fixed for the design computed to obtain a stable operation of the single-stage OTA for a nominal (minimum) capacitive load. On the other hand, the impedance of the differential pair tail current source can be increased using, for example, transistor cascoding, gain boosting [43] or replica-tail feedback [35]. Transistor cascoding reduces the input dynamic range and adds an extra pole and zero to the common mode gain transfer function. Gain boosting requires cascoding of the tail current source: while it improves the input dynamic range of the OTA, it reduces the common mode settling speed. Replica-tail feedback similarly improves input dynamic range but is sensitive to transistor mismatch.

Rail-to-rail OTA input stages employing both N - and P - differential pair transistors are not well suited for the high CMRR OTAs, both single-ended and differential, mainly because of the difference of the input offsets for the corresponding differential pairs [112]. This differential pair input offset difference cannot be reduced by any other means except by increasing the size of the differential pair transistors. As a result either the power consumption increases or the frequency response of the OTA deteriorates.

A new method is proposed here for improving the CMRR of the current mirror OTA. This method does not compromise power, slewing, die area and dynamic range of the OTA while the settling speed by is reduced by only $5-20 \%$ depending on the design. The proposed technique does not affect $g_{m}$ or $R_{t}$ in (10.1) and hence can be used in conjunction with cascod-
ing or impedance boosting of the tail current source to get an even higher CMRR. The proposed technique is explained in the following sub-section.

### 10.4.2 A New Current CMFB for the Single-ended Current Mirror OTA

In order to demonstrate the efficiency of the proposed current CMFB technique, the performance of the standard OTA in Fig. 10.11 is first discussed and then a new OTA employing the current CMFB is introduced. Performance of both OTAs is then compared.

Without loss of generality, assume that the standard OTA employs a 1:1 current mirror ratio (M4 equals M7). This ratio is common for high frequency OTAs with the first non-dominant pole being given approximately by the current mirror pole:

$$
\begin{equation*}
\omega_{p}=\frac{g_{m 4}}{C_{g s 4}+C_{g s 7}+C_{g d 7}+C_{g d 2}+C_{d 4}+C_{d 2}}, \tag{10.2}
\end{equation*}
$$

where $C_{g s}, C_{g d}$ and $C_{d}$ are the gate-source (gate-oxide and overlap), gate-drain (overlap) and drain (diffusion) capacitance respectively and the index refers to the corresponding transistor. Note that the Miller effect for $C_{g d 7}$ in (10.2) is not included because M7 is cascoded in practically all such OTAs to achieve high gain (e.g. final realization).

Denote the current through M6 (Fig. 10.11) by $I_{0} . I_{0}$ is also the maximum output current of the OTA that determines the slewing speed $I_{0} / C_{L}$, where $C_{L}$ is an OTA load capacitance including output parasitics. Since the OTA current mirror ratio is $1: 1$, the current through M5 is given by $2 I_{0}$. Thus the quiescent current of the OTA in Fig. 10.11 is $3 I_{0}$ and the maximum output current is $33 \%$ of the quiescent current.

The unwanted common-mode gain of the single-ended OTA in Fig. 10.11 arises due to the finite impedance of the tail current source M5. The input common mode level of the OTA modulates the voltage across the tail current source resulting in current variation through the differential pair transistors M1 and M2. This current variation is mirrored via M4 and M7 into the output of the OTA which is high impedance. If the output impedance of the OTA is Rout, then the differential and common mode gains $K_{d i f f}$ and $K_{c m}$ are given by:

$$
\begin{equation*}
K_{\text {diff }}=\frac{g_{m} \cdot R_{\text {out }}}{2}, \quad K_{c m}=\frac{R_{\text {out }}}{2 \cdot R_{t}} . \tag{10.3}
\end{equation*}
$$

Recall that $C M R R=K_{\text {diff }} / K_{c m}$ gives (10.1). Making the current through M4 insensitive to the current variations of the tail current source M5 suggests a novel approach to boosting the CMRR.

A basic current mirror OTA employing a proposed current CMFB (Fig. 10.12) allows a significant improvement in CMRR. The tail current source M5 is now $I_{0}$ as opposed to $2 I_{0}$ for the OTA in Fig. 10.11. Therefore the widths for M4 and M7 are scaled as 1:2. M1 and M2 are designed to have the same $g_{m}$ as in Fig. 10.11. An additional current branch with a fixed current $I_{0}$ is biased via M10. Transistors M8 and M9 employ the current CMFB. For the purpose of correct operation of the CMFB, transistors M3,M4,M8 and M9 are matched.

The operation of the circuit is as follows. Assume that initially the currents through M10, M5 and M6 are as depicted in Fig. 10.12. Hence, the currents through M8,M9,M3,M4 are


Fig. 10.12 Single-ended current mirror OTA with a proposed current CMFB.
given by $I_{0} / 2$. Due to the symmetry of the circuit, no current flows from node A to node B . Now consider a small current change via M5 (due to a common mode level change of the inputs of the OTA) to give $I_{0}+\delta I_{0}$. This current splits equally between differential pair transistors M1 and M2 to give $I_{0} / 2+\delta I_{0} / 2$ for each transistor. The current through M1 is further carried by a $1: 1$ current mirror (M3,M9) to give $I_{0} / 2+\delta I_{0} / 2$ via M9. Recall that transistors M 2 and M 9 experience an equal current change of $\delta I_{0} / 2$. Transistors M4 and M8 are in a MOS diode configuration connected to nodes A and B respectively. To prove that the currents through M4 and M8 does not change it is sufficient to state that injecting a current into node A and sinking the same current out of node B (which is physically the same metal connection) does not violate the DC operating point (voltage) of both nodes A and B. To help understand the circuit operation, the path of the common mode level dependent current $\delta I_{0}$ is depicted in Fig. 10.12 using dashed lines.

To prove that the proposed CMFB does not affect differential signals, one needs to demonstrate that there is no signal dependent current flowing between nodes A and B Fig. 10.12. Since the OTA differential input signal does not modulate the tail current voltage source, the sum of the two currents generated by M10 and M5 is also signal independent and given by $2 I_{0}$. By design, the sum of currents through M3 and M4 is equal to the sum of currents through M8 and M9. Since M3,M4,M8 and M9 provide the only path for the current generated by M5 and M10, a signal independent current $2 I_{0}$ is split equally between pairs of transistors M8,M9 and M3,M4. Transistor M10 injects a fixed current into node B, while transistors M8 and M9 sink a signal independent current out of node B . This implies that there is no signal dependent current flowing between nodes A and B.

The above analysis omits first order small effects such as the finite output impedance of the current mirror M3,M9. This simplification does not affect the analysis of the differential signal OTA response. However, the first order small effects are significant in analysis of the common mode signal OTA response and, in fact, determine the CMRR. An analytical expres-


Fig. 10.13 Single-ended current mirror OTA with enhanced current CMFB.
sion for the CMRR of the OTA in Fig. 10.12 is bulky but yet can be well approximated by:

$$
\begin{equation*}
C M R R=g_{m} \cdot R_{t} \cdot 2 \cdot g_{m 4} \cdot \frac{r_{d s 2} \cdot r_{d s 4}}{r_{d s 2}+r_{d s 4}} \tag{10.4}
\end{equation*}
$$

Comparing (10.4) with (10.1) reveals an improvement in CMRR by a factor of:

$$
\begin{equation*}
K_{i m p r}=2 \cdot g_{m 4} \cdot \frac{r_{d s 2} \cdot r_{d s 4}}{r_{d s 2}+r_{d s 4}} . \tag{10.5}
\end{equation*}
$$

In a standard CMOS $0.25 \mu m$ process, this factor is of the order of 30 for minimum length transistors. Since $R_{t}$ is doubled and $g_{m}$ is not modified for the OTA in Fig. 10.12, another improvement in CMRR by a factor of 2 is obtained (not reflected in (10.5)).

The OTAs in Fig. 10.11 and Fig. 10.12 consume the same power, providing maximum $33 \%$ of the quiescent current to the load. The OTAs have identical input/output dynamic range and occupy approximately the same area. Indeed, M3,M4,M8,M9 and M5,M10 of the OTA in Fig. 10.12 are half the size of M3,M4 and M5 of the OTA in Fig. 10.11, respectively. It is not so obvious that the first non-dominant poles are close to each other for both OTAs. Indeed, despite transistors M4 and M7 being scaled as 1:2 (Fig. 10.12) they are a part of the current mirror M4,M7,M8 with 1:1 current ratio. The pole of the current mirror M4,M7,M8 is about 5$20 \%$ lower than (10.2) due to additional parasitic diffusion and overlap capacitance of M9 and M10. The relative contribution of M9 and M10 to the current mirror pole is reduced when the gain of the current mirror is increased.

If the CMRR improvement factor (10.5) is not sufficient, an enhanced version of the circuit in Fig. 10.13 can be used. Two amplifiers in the circuit of Fig. 10.13 boost the transconductance of M3 and M4. If the gain of these amplifiers is $K_{\text {amp }}$, then the CMRR improvement factor (10.5) becomes:

$$
\begin{equation*}
K_{i m p r}=2 \cdot K_{a m p} \cdot g_{m 4} \cdot \frac{r_{d s 2} \cdot r_{d s 4}}{r_{d s 2}+r_{d s 4}} . \tag{10.6}
\end{equation*}
$$



Fig. 10.14 Differential transistor pair in ideal environment.

Thus the proposed CMFB can be used to boost the CMRR of the OTA to such an extent that other factors such as transistor mismatch limit the performance of the OTA.

### 10.4.3 Influence of Differential Transistor Mismatch on the OTA CMRR

Consider differential transistors M1 and M2 as depicted in Fig. 10.14. Vx1 and Vx2 are ideal voltage sources, while current source Ix1 has infinite impedance $R_{t}=\infty$. Without loss of generality, assume that the differential stage of Fig. 10.14 is incorporated into the OTA and that the current of Vx2 is further mirrored into the high output impedance of the OTA. Since the output impedance of the OTA makes an equal contribution to both the common-mode and dif-ferential-mode gains of the OTA (10.3), it can be excluded from the CMRR analysis. If M1 and M2 are matched, then according to (10.1), the CMRR of the idealized OTA is infinitely large $C M R R=\infty$.

Assume now that M1 and M2 are mismatched and characterized by $g_{m 1}, r_{d s 1}$ and $g_{m 2}, r_{d s 2}$. Simple arithmetic calculations show that the idealized OTA now has a finite CMRR given by:

$$
\begin{equation*}
C M R R_{\text {mismatch }}=\frac{g_{m 1} \cdot r_{d s t} \cdot g_{m 2} \cdot r_{d s 2}}{g_{m 1} \cdot r_{d s 1}-g_{m 2} \cdot r_{d s 2}} \tag{10.7}
\end{equation*}
$$

The numerator in (10.7) is a PMOST gain product for M1 and M2 and the denominator represents a $3 \sigma$ gain mismatch. Experimental measurements conducted at Xilinx Laboratory, San Jose, confirmed a 62 dB large-swing CMRR upper bound for the p-channel differential transistor pair using matched $\mathrm{L}=0.5 \mu m, \mathrm{~W}=10 \mu \mathrm{~m}$ MOSTs and biased at $V_{o n}=0.15 \mathrm{~V}$.

The approach taken here and the ensuing equation (10.7) is new and gives an incisive view to quantifying CMRR. It suggests a unified approach that relates all transistor mismatches in an OTA, be it single-ended or differential, to the OTA CMRR. Indeed, mismatch of transistors (other than M1 and M2) in the OTA cause a DC operating point variation for M1 and M 2 which in turn affects $g_{m 1}, r_{d s 1}$ and $g_{m 2}, r_{d s 2}$. It is worth mentioning that the gain mis-


Fig. 10.15 Schematic of the fabricated OTA.
match is a convenient term for explanation of (10.7), yet one should remember that commonly used $V_{t}$ mismatch, $g_{m}$ mismatch and gain mismatch are not uncorrelated [113].

### 10.4.4 Experimental Verification

A schematic of the implemented OTA is shown in Fig. 10.15. This OTA was fabricated in a standard $0.25 \mu \mathrm{~m}$ UMC process as a precision building block of the 12-bit algorithmic ADC and accompanying T\&H. The OTA is not accessible for direct measurements. Instead the lower bound for the OTA DC gain and CMRR can be obtained indirectly using the ADC measurements. The contribution of the OTA finite DC gain and CMRR into the INL of the fabricated ADC is given by:

$$
\begin{equation*}
I N L=2^{N} \cdot\left(\frac{1}{\text { Gain }}+\frac{1}{2 \cdot C M R R}\right) \tag{10.8}
\end{equation*}
$$

where $N=12$ is the number of bits or resolution of the ADC. The linearity test of the ADC demonstrated a 0.8 LSB INL at 12-bit level, discussed in section 10.6. Such performance is only possible if both the OTA DC gain and CMRR are greater than 78 dB . Thus the target specifications of the OTA are validated and the operation of the current CMFB is confirmed.

The proposed current CMFB allows boosting CMRR of the single-ended current mirror OTA until other performance limiting factors such as a transistor mismatch become dominant. The current CMFB does not affect the OTA power dissipation, slewing, die area and dynamic range yet reduces the settling speed by $5 \%-20 \%$.

### 10.5 Low-Reference Comparator

The circuit diagram of the dynamic comparator used in the ADC is shown in Fig. 10.16 - it contains only 10 transistors stacked 3 high. It is optimized for a low reference range by way of the PMOS input stages so as to enable fast switching at low level input voltages. Initially, the comparator is held in reset by keeping the Clk signal high. When Clk goes low, the comparator latches in a very short time. The direction and speed of latching for the differential output is determined by the resistive imbalance of triode-region PMOSTs $M_{7}$ and $M_{9}$ in comparison to $\mathrm{M}_{8}$ and $\mathrm{M}_{10}$ (assuming no further nominal mismatch of the left and right hand sides of the circuit). With signal input PMOSTs $\mathrm{M}_{7}$ and $\mathrm{M}_{9}$ having aspect ratio $W_{1} / L_{1}$ and reference input PMOSTs $\mathrm{M}_{8}$ and $\mathrm{M}_{10}$ with $W_{2} / L_{2}$, the threshold voltage at which the comparator flips is obtained for when the parallel resistance of $\mathrm{M}_{7}$ and $\mathrm{M}_{9}$ becomes equal to that of $\mathrm{M}_{8}$ and $\mathrm{M}_{10}$, i.e.

$$
\begin{equation*}
\frac{W_{1}}{L_{1}}\left(V_{i n_{p}}-V_{i n_{n}}\right)=\frac{W_{2}}{L_{2}}\left(V_{\text {ref }_{p}}-V_{r e f_{n}}\right), \tag{10.9}
\end{equation*}
$$

which for equal gate lengths reduces to:

$$
\begin{equation*}
\left.\left(V_{\text {in }_{p}}-V_{\text {in }_{n}}\right)\right|_{\text {threshold }}=\frac{W_{2}}{W_{1}}\left(V_{\text {ref }_{p}}-V_{\text {ref }_{n}}\right) . \tag{10.10}
\end{equation*}
$$

In this design, $V_{\text {refp }}$ and $V_{\text {refn }}$ are chosen as 1.4 V and 0.4 V , respectively. The comparator thresholds only need to be accurate to within $\pm 125 \mathrm{mV}$ of their nominal values, assuming no other analogue offsets in the ADC. Here, they were designed with a maximum $3 \sigma$ offset of 100 mV across corners. This meant very small transistor sizes could be chosen, namely $\mathrm{M}_{7}$ and $M_{9}$ with $4 / 0.6$ and $M_{8}$ and $M_{10}$ with $4 \times 4 / 0.6$. The average power dissipation is only $250 \mu \mathrm{~W}$ per comparator from a 2 V supply at a 40 MHz clock rate.


Fig. 10.16 Dynamic comparator for operation with low supply and low references.


Fig. 10.17 Die photograph showing partitioning of blocks in $0.25 \mu \mathrm{~m}$ CMOS prototype.

### 10.6 Cyclic ADC Fabrication and Measurement Results

The ADC, including all the circuits presented in the previous sub-sections, was prototyped in a standard $0.25 \mu \mathrm{~m}$ CMOS process. A picture of the die showing the partitioning of the blocks can be seen in Fig. 10.17.

The 8 ADC sample capacitors and 4 T\&H capacitors are each 2 pF and composed of inter-digitated metal-metal capacitors. Metal layers M1, M2, M3 form the main active capacitance, being laid out in thin strips to create well coupled inter-digitated bottom and top plates. N -well, Poly and M4 are used for shielding.

The circuit works to full specification off a 2 V supply. The amplifier DC gain and CMRR were simulated to be above 78 dB across process and temperature corners, which is sufficient for this embedded 12-bit application. The parasitic input capacitance $C_{p a r}$ of section 9.5 is given approximately by the gate-drain overlap capacitance of one transistor (36fF) of the input differential pair together with the wiring capacitance at its gate (20fF). Hence, $C / 2 C_{p a r}$ is given by $2 / 2 \times 0.056 \approx 17$ which equates to about 4 bits improved accuracy (linearity) over previous charge transfer approaches. In this design, $V_{\text {refp }}$ and $V_{\text {refn }}$ were created as 0.4 V and 1.4 V , respectively. This equates to about $2 \cdot\left(V_{\text {on }_{n}}+V_{\text {marg in }_{n}}\right)$ above ground for the NMOS side and $3 \cdot\left(V_{\text {on }_{p}}+V_{\text {margin }_{p}}\right)$ below the supply for the PMOS side of the amplifier.

Detailed measurements were carried out on 40 samples. The complete ADC with DEC, clocks and comparators occupy $0.15 \mathrm{~mm}^{2}$ - Fig. 10.17. The total power consumption including digital circuitry is 5.5 mW . Typical DNL and INL plots are presented in Fig. 10.18(a) and (b). DNL of less than 0.25 LSBs and INL of less than 0.8 LSBs at 12-bit level are achieved. The $T H D$ and $S N R$ are shown as functions of the sampling frequency in Fig. 10.19(a), while a typical FFT spectral density plot is shown in Fig. 10.19(b) for a $200 \mathrm{kHz} 1 \mathrm{~V}_{\mathrm{pp}}$ input signal. The


Fig. 10.18 Measured static ADC linearity at 12-bit level with (a) DNL and (b) INL.
$T H D$ at $1 \mathrm{MS} / \mathrm{s}$ was measured to be 77 dB . The $S N R$ was 64.5 dB which is, in fact, what is expected for this design. Since the noise power of the $C+C$ concept is about half that of the standard $C \rightarrow C$ implementation, the required $C$ to achieve 12-bit noise performance of the algorithmic ADC is (see section 8.2.3.2):

$$
\begin{equation*}
C \geq \frac{\sqrt{R}}{2} \cdot 45 \cdot k T \cdot \frac{2^{2 N}}{F S^{2}}, \tag{10.11}
\end{equation*}
$$

where $R$ is the number of rotations. Here $R=11$, since the final bit is absolutely and instantly determined by a flash stage straight after the final bit trial. Based on noise considerations only, $C$ would be 5 pF for 12 -bit $S N R$. In our case, we chose $C=2 \mathrm{pF}$, to give an $S N R$ of over 64 dB which compares correctly with measurements. The T\&H, biasing circuits and clocking produce a small amount of noise which add a few tenths of a dB to the overall noise. In the embedded implementation, digital noise post-filtering is used to effectively increase the $S N R$. Capacitor area dominates the total die area, as can be seen from the die of Fig. 10.17. We know from capacitor matching considerations that using 2 pF capacitors yields about 14-bits linearity for the $C+C$ type ADC proposal of this thesis - see section 9.5 . Thus these capacitors are sufficient for this application. Fig. 10.22 and Fig. 10.23 show the output of Labview GUIs [115] written to acquire and process the ADC data.


Fig. 10.19 Measured ADC dynamic performance with (a) THD and SNR and (b) an FFT of digitized output.

At the time of writing, this 12-bit ADC has been embedded in a large scale digital VLSI application using the most modern 65 nm CMOS process. The block diagram of this application was discussed in section 10.1.2. The infra-red micrograph of a back-planed flip-chip die is shown in Fig. 10.20. It includes a SC reference circuit for generating $V_{\text {refp }}$ and $V_{\text {refn }}$ on chip and is accurate to 12 -bits across PVT. The circuits have been created using $0.25 \mu \mathrm{~m}$ thickoxide MOSTs which are required for chip I/O interfacing to the 65 nm 1 V digital VLSI. Here, the ADC area is considerably smaller than the $0.25 \mu \mathrm{~m}$ test-chip prototype at only $0.04 \mathrm{~mm}^{2}$, while the power is $1 / 3$ lower at 3.7 mW for the same dynamic performance. The reduction in area is achieved mainly due to the shrinkage of the capacitors and interconnect in going from 250 nm down to 65 nm , while the power reduction is achieved mainly due to the reduced parasitic capacitor loading. A SEM image of the back-milled cross-section of one of the capacitors is shown in Fig. 10.21. The layers of filamented metal used to compose the capacitor are clearly visible which create a very high specific capacitance in 65 nm . Finally, the main ADC performance parameters are summarized in Table 10.1.


Fig. 10.20 Micrograph of 65nm flip-chip showing ADC, T\&H and reference generator in an embedded VLSI application.


Fig. 10.21 Back-side SEM image of the milled cross-section of a metal finger capacitor revealing the filamented layers used.


Fig. 10.22 Graphical output of written LabView program to measure ADC Linearity.


Fig. 10.23 Graphical output of written LabView program for ADC dynamic testing.

Table 10.1 Cyclic ADC Measurements

| Technology | $0.25 \mu \mathrm{~m}$ baseline CMOS |
| :---: | :---: |
| Resolution ( $1 \mathrm{~V}_{\mathrm{p} \text {-p }}$ input) | 12-bits |
| Conversion Rate | $3.3 \mathrm{MS} / \mathrm{s}$ with 40 MHz clock |
| Clock cycles for 12 bits | 12 - no latency |
| Active area | $0.15 \mathrm{~mm}^{2}\left(0.04 \mathrm{~mm}^{2}\right.$ in 65 nm$)$ |
| Power | 5.5 mW ( 3.7 mW in 65 nm ) |
| DNL at 12-b | $<0.25$ LSBs |
| INL at 12-b | $<0.8$ LSBs |
| THD at 1MS/s | 77 dB |
| $S N R$ at 1MS/s | 64.5 dB |
| $S F D R$ at 1MS/s | 80 dB |
| $\mathrm{FOM}_{\text {power }}$ | $1.2 \mathrm{pJ} /$ conv $(0.8 \mathrm{pJ} /$ conv in 65 nm$)$ |
| $\mathrm{FOM}_{\text {area }}$ | $31 \mathrm{~nm}^{2} /$ conv $-\mathrm{Hz}\left(9 \mathrm{~nm}^{2} /\right.$ conv in 65 nm$)$ |

### 10.7 Pipelined ADC Design

The proposed $C+C$ concept of Chapter 9 has also been implemented as a fully differential pipelined ADC in a $0.25 \mu \mathrm{~m}$ baseline CMOS process, based on the circuit realization discussed for the cyclic ADC in section 10.3. The design is optimized according to the guiding principles espoused in section 8.3. Two versions of the pipeline have been implemented to test out the intrinsic performance of the new architecture in terms of speed and accuracy. The first pipeline is a high-speed, medium accuracy ADC (designed for 10 -bit resolution and $120 \mathrm{MS} / \mathrm{s}$ ), while the second pipeline is a high-resolution, medium speed ADC (14-bit resolution and $25 \mathrm{MS} / \mathrm{s}$ ). For the 10 -bit ADC, there is a fast acquisition T\&H followed by a first stage, each with 0.5 pF capacitors. The capacitors, switches and amplifiers of the first 4 stages are scaled with a scaling ratio of 0.58 after which no scaling is used. In the 14 -bit ADC , there is neither a $\mathrm{T} \& \mathrm{H}$ nor multi-bit front-end needed, since the intrinsic accuracy of the $C+C$ technique guarantees 14bits performance. The first and second stages has 2 pF capacitors. The first stage has been modified to ensure accurate acquisition of the analogue input signal. There is capacitor and amplifier scaling of 0.58 down to the sixth stage with the last 8 stages all being the same. The final stage is just a 1-bit flash. The 14-bit ADC also uses gate voltage boosted bootstrapped switches [114] in the first 4 stages in order to reduce distortion due to signal dependent switch resistance to below the 14-bit level. The progression of scaled stages can be clearly seen in the layout of the 14-bit ADC of Fig. 10.24.

Simulation results of the frequency response of the 10 -bit and 14-bit pipelined ADCs are shown in Fig. 10.25 and Fig. 10.26, respectively. Extracted values of all the important nets,


Fig. 10.24 Layout of intrinsic 14-bit pipelined $A D C$ based on $C+C$ concept.
including power supplies, are used in the circuit simulations. For the 10 -bit ADC, an input frequency just beyond the Nyquist interval of 60 MHz produces distortion of less than -72 dB with respect to the input level. On the other hand, the 14-bit ADC response for an input frequency just beyond its Nyquist interval of 12.5 MHz creates distortion of less than -86 dB .

The power consumption of the 14 -bit, $25 \mathrm{MS} / \mathrm{s}$ ADC is only 11 mW from a 2.5 V supply. It has an $S N R$ of 74 dB which is sufficient for 14-bit linearity signal-chain ADCs, as discussed in section 10.1.1. It occupies $1 \mathrm{~mm}^{2}$ in $0.25 \mu \mathrm{~m}$ CMOS. The definitions for the ADC FOMs were presented in section 7.7 .3 . For the 14 -bit design, $F O M_{\text {power }}=0.15 \mathrm{pJ} /$ conversion, while $F O M_{\text {area }}=8.5 \mathrm{~nm}^{2} /$ conversion -Hz , assuming 12 effective bits. The very low power and small die area are due to the fact that no power hungry, large area calibration is needed; instead, the achieved accuracy is intrinsic to the $C+C$ architecture and guaranteed by design. The efficiencies of the proposed ADCs based on the $C+C$ concept are benchmarked in the comparative FOM plot of Fig. 10.27 against key published ADC designs from 2000 onwards. The cyclic ADC power and area efficiency represents a big step forward for this type of ADC, while the pipelined ADC improves a lot on previous state of the art ADCs by exploiting the inherent power efficiency of pipelines and the intrinsic accuracy of the $C+C$ concept.

### 10.8 Conclusions

This chapter explored a number of novel circuits that were developed as part of this research into high-accuracy switched capacitor design. These include a T\&H, ADC and high-CMRR single-ended OTA. The T\&H is a key block for both high-accuracy measurement applications

SNEEM1, ADC10_test_ 120 MHz, Typ $T=40 \mathrm{C}, 63.75 \mathrm{MHz} / 120 \mathrm{Ms} / \mathrm{s}$, Single p/supply: Dec 62004


Fig. 10.25 DFT of post-layout simulated 10-bit pipelined ADC output: $f_{\text {sample }}=120 \mathrm{MHz}$ and $f_{\text {in }}=63.75 \mathrm{MHz}$.


Fig. 10.26 DFT of post-layout simulated 14-bit pipelined ADC output:
$f_{\text {sample }}=25 \mathrm{MHz}$ and $f_{\text {in }}=12.9 \mathrm{MHz}$.


Fig. 10.27 Performance comparison of ADCs based on recent key publications.
and high-speed communications applications. The design of a flexible and robust T\&H was demonstrated here which can process a number of different types of analogue input signals while always delivering a level shifted fully differential sampled data signal to the ADC. The ADC is kept oblivious to the type of analogue input signal received. The new ADC architecture based on the $C+C$ concept of Chapter 9 with floating-hold buffers has also been validated here. Essentially 4 properties of the new circuit have been demonstrated to a high level, namely accuracy, speed, small die area and robustness when integrated in digital VLSI. A new CMFB circuit was demonstrated which boosts the CMRR of single-ended amplifiers (needed for the implementation of the $\mathrm{T} \& \mathrm{H}$ and ADC ) to the extent that their performance become determined by other factors like transistor matching such as in fully differential amplifier structures.

Within the die area allocated to this work for an embedded measurement application, 12bit accuracy has been achieved for a cyclic ADC at 3.3MS/s using uncharacterized inter-digitated metal-metal capacitors and neither trimming nor calibration was needed. Similarly, based on the new circuit techniques, a 120MS/s 10-bit pipelined ADC and 25MS/s 14-bit pipelined ADC have been laid out and simulated for a $0.25 \mu \mathrm{~m}$ CMOS process. These ADCs are suitable for embedding in CMOS digital VLSI and will scale easily with the process without the need for special analogue characterization or process options. Power and Area FOMs are well below those of previously published ADCs.

## Chapter 11

## Main Conclusions

Switched capacitor (SC) techniques are well proven to be excellent candidates for implementing critical analogue functions with high accuracy, surpassing other analogue techniques when embedded in mixed-signal CMOS VLSI. The core structures for implementing SC functional blocks have not changed much down the years, with more emphasis being placed on achieving functionality at lower supply voltages (e.g. through using lower accuracy switched opamp techniques) than purely on achieving higher accuracy per se.

To this end, this thesis set out to explore and analyse novel SC techniques which are fundamentally more accurate than heretofore. The main theme of the thesis is the achievement of higher accuracy at circuit block level beyond the accuracy achievable due to component matching alone without having to resort to trimming or digital calibration. Two areas, which comprise the majority of SC applications, have been explored for exploitation of the proposed techniques, namely SC filters and algorithmic ADCs, both cyclic and pipelined. Furthermore, efficient system level procedures are explored in both these areas.

Practically all the power in SC circuits is dissipated in the amplifier. A strategy is proposed in Chapter 3 which is geared towards optimizing amplifier design specifically for sampled data applications. Single-stage amplifiers are especially suitable for use in SC circuits because they are genuinely high-bandwidth load-compensated amplifiers which have predictable settling performance across PVT with very high power efficiency. Unfortunately, their signal range is very limited, especially for those applications that require equal input and output common-mode reference levels. In Chapter 4, a suitable single-stage alternative is proposed based on the DITO which has dual inputs via complementary PMOS and NMOS differential pairs, high signal range for equal input and output reference levels and yet double the power efficiency of the standard telescopic OTA. It achieves this by exploiting the inherent level shift properties of the switching signal capacitors. These structures are applied successfully for the implementation of power efficient large signal range SC filters.

Standard SC charge transfer ( $Q T$ ) circuit techniques are primarily limited in accuracy by a) capacitor matching and b) the accuracy with which a differential amplifier can squeeze charge from signal capacitors connected to its input and the feedback capacitor. The proposed
delta-charge flow techniques $(\delta-Q)$ distinguish themselves as follows:

1) When needed (e.g. filter design, section 2.2.2), primary signal charge transport occurs via passive charge redistribution between signal capacitors without the aid of an active element, namely an amplifier;
2) Secondary charge transport $(\delta Q)$ via the amplifier virtual earth node is only to compensate for charge imbalance caused by the presence of unavoidable parasitic capacitors at the signal capacitors top and bottom plates and amplifier input terminals.
3) Amplifier is used primarily to provide a buffered output signal commensurate to the voltage spanning some combination of signal capacitors.
Methodologies based on orthogonal design procedures are proposed at system level for implementing SC circuits in such a way that circuit imperfections due to mismatch and noise neither affect the accuracy nor the integrity of the system transfer function. Applications are to be found using orthogonal-hardware-modulation in the context of high-selectivity SC filters in Chapter 5 and the $C+C$ concept to replace the popular "multiplying" DACs (MDACs) found in algorithmic type ADCs in Chapter 9.

With the theory developed for SC filters in Chapter 5, low power and very accurate integrated CMOS filters are developed in Chapter 6. For instance, a critical selectivity filter for full scale analogue video is created with a dynamic range of 79 dB for a supply voltage of 5 V but $6 V_{p p}$ signal range. A $6^{\text {th }}$ order CMOS bandpass filter, including gain control, for the purpose of replacing a ceramic filter in a 10.7 MHz FM radio, is implemented successfully. The achieved dynamic range of 61 dB for a 3 V supply is not yet good enough though for implementing a one-to-one replacement.

From Chapter 7 onwards, the focus of attention of the thesis shifts to how SC circuits can be used to implement algorithmic ADCs more accurately than previously possible without resorting to trimming and calibration. It is demonstrated that familiarity with the unique effects specific errors have on the ADC characteristics can be a useful means for debugging hardware issues after ADC fabrication. It is proven how the capacitor matching requirement can be reduced in high-resolution pipelined ADCs through judicious application of a multi-bit frontend with a scaled back-end. For instance, a multi-bit front-end should only be used if the accuracy can't be achieved with a 2-bit stage alone (1-bit effective). The function of the multi-bit front-end is to translate the ADC accuracy requirement down to the level of the achievable accuracy of the first 2-bit stage.

The floating-hold-buffer is proposed in Chapter 9 as the means for implementing the $C+C$ concept for algorithmic ADCs. With this novel structure, it is demonstrated that an extra 4 bits un-calibrated accuracy (linearity) is possible over previous MDAC conversion stages. The accuracies achieved through implementations on silicon are presented in Chapter 10, not just in 250 nm CMOS but in a mixed-signal 65 nm chip through use of the thick-oxide option. With the latter, the FOMpower ( $0.8 \mathrm{pJ} /$ conv) is better than previous algorithmic ADCs, while the FOMarea $\left(9 \mathrm{~nm}^{2} /\right.$ conv- Hz$)$ is orders of magnitude better than previously published.

## Original Contributions

- A black-box analysis of amplifier design is presented, which is geared specifically towards SC applications. The design procedure accounts for small-signal and large-signal effects to come to an optimal result.
- Dual-input telescopic OTAs are proposed for different applications in the video and radio domains which have improved $G B W$ and signal-handling compared to standard telescopic OTAs.
- Orthogonal hardware modulation is used in conjunction with $N$-path filtering as a means of preventing pattern noise while achieving very high accuracy in SC bandpass filters.
- SC delta-charge-redistribution $(\delta-Q R)$ stages are proposed as an alternative to the ubiquitous SC charge transfer stages for the more accurate implementation of SC filters. Three unique implementations of $\delta-Q R$ SC bandpass filter are critically analyzed.
- A methodology is presented for accurate and clear analysis of the SC biquad filter. It includes the effects of gain and phase errors caused by amplifier non-idealities and the presence of parasitic capacitors.
- A black-box model for ADC operation is presented which includes a more realistic quantization noise model, a simplified model for the spectral content of the quantized error signal, as well as minimum theoretical and practical power limits.
- A lumped error model is developed to account for static and dynamic errors arising from hardware imperfections in cyclic and pipelined ADCs.
- An error analysis is presented to aid the design of the multi-bit front-end stage of a pipelined ADC. It is demonstrated and quantified how the capacitor matching requirement can be reduced in a high-resolution pipelined ADC through the judicious application of a multi-bit front-end.
- A novel implementation of the 1.5 -bit ADC stage for use in cyclic and pipelined ADCs is presented. Voltage multiplication is replaced by accurate addition (the $C+C$ concept) and a floating-hold-buffer is proposed for its implementation. The accuracy of the ADC
employing the new circuitry is less sensitive to the matching accuracy and linearity of the sampling capacitors compared to previous circuit techniques presented in the literature.
- The design of a flexible and robust T\&H, based on the floating-hold-buffer, is demonstrated which can combine all the functions of a) single-ended to differential conversion, b) processing unipolar signals, c) processing bipolar signals, and d) processing fullydifferential signals. Irrespective of input signal type, it delivers a fully-differential sampleddata signal within the correct full scale range of the following algorithmic ADC block and which is set at the correct common-mode level for the ADC to operate optimally.
- A high CMRR single-ended current-mirror OTA employing a novel current CMFB is proposed. The current CMFB boosts the OTA CMRR by a factor of 30 while allowing integration of conventional OTA improvements. A unified approach relating the CMRR and transistor mismatches is presented.


## List of Publications and Patents

## Publications

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## Summary

In this thesis, switched-capacitor (SC) techniques are proposed which allow the attainment of higher intrinsic analogue accuracies than previously possible in such application areas as analogue filter and analogue-to-digital converter (ADC) design. The design philosophy is to create the required functionality without relying on trimming or digital calibration means but instead to develop methods which have reduced dependence on both component matching (especially capacitor matching) and parasitic effects (especially parasitic capacitance).

At a system level, orthogonal design procedures are employed which ensure that artefacts due to expected circuit imperfections are avoided in the system transfer function. For instance, in SC filter design, orthogonal-hardware-modulation helps alleviate the effects of N path mismatch through the introduction of an extra degree of freedom, where the number of hardware paths $N$ (hardware modulation) is decoupled from the functional modulation factor $n$, as introduced by the transformation $z \rightarrow z^{n}$. In algorithmic ADC design, both cyclic and pipelined, conventional techniques make use of multiplying digital-to-analogue converters (or MDACs) which require SC circuits with accurate capacitor ratios to implement accurate signal multiplication. On the other hand, in this thesis, the ADC function is decomposed into the simple sub-functions of signal addition and level shifting which can be implemented using SC techniques which don't rely on accurate capacitor ratios.

At circuit level, delta-charge flow $(\delta-Q)$ techniques are employed to realize SC circuits with more accurate transfers than their conventional charge-transfer $(Q T)$ counterparts. Unlike $Q T$ SC circuits, $\delta-Q$ SC circuits do not require signal charge transfer from capacitor to capacitor via the amplifier virtual earth node. Instead, only a delta charge $\delta Q$ flows in the virtual earth node due to the presence of parasitic capacitors at the amplifier input terminals. In SC filter design, delta-charge-redistribution $(\delta-Q R)$ is a means for the accurate implementation of filter transfer functions using passive charge redistribution between capacitors in the feedback path of an amplifier, instead of active charge transfer between capacitors through the active intervention of an amplifier in $Q T$ SC filters. In ADC design, a highly accurate method $(C+C)$ for the stacking of capacitor voltages is proposed which uses a floating-hold-buffer for implementation. The accuracy of signal addition is practically insensitive to the matching and linearity of the signal capacitors as well as the presence of parasitic terminal capacitance.

A number of other innovative circuit techniques have been included in the thesis, such as: a versatile accurate track-and-hold (T\&H) which is re-programmable for unipolar, bipolar
and differential modes; clock-skew insensitive sampling; a common-mode-feedback circuit which significantly boosts the common-mode rejection ratio of single-ended amplifiers; highefficiency dual-input transconductance amplifiers which make use of the level shift properties of switched capacitors; a low-reference dynamic comparator.

The validity of the concepts developed and analyzed in the thesis has been demonstrated in practice with the design of CMOS SC bandpass filters and algorithmic ADC stages (both cyclic and pipelined). The intrinsic accuracies achieved go beyond those achieved with previous state-of-the-art solutions with a consequent reduction in power consumption for the same speed applications. For example, a 10.7 MHz radio IF selectivity filter integrated in standard CMOS, employing the proposed methods, achieves an accuracy greater than ceramic filters. Another example is an ADC with better than 12-bit intrinsic performance, albeit capacitors with only 9-bits matching accuracy were used in the realization. The ADC architecture is also very robust and has proven itself in an embedded digital VLSI application in the very newest 65 nm CMOS. The power consumptions and silicon areas of the solutions proposed here are lower than other known solutions from the literature.

## SAMENVATting

In dit proefschrift, nieuwe methodes gebaseerd op switched-capacitor (SC) technieken zijn voorgesteld waarmee het mogelijk wordt om hoger intrinsieke nauwkeurigheden te bereiken dan voorheen (ooit tevoren) gericht op toepassingsgebieden zoals analoge filter ontwerp en analoog-naar-digitaal omzetter (ADC) ontwerp. Het ontwerpfilosofie is om de benodigde functionaliteit te creëren zonder te steunen op trimming of digitale calibratie maar, in plaats daarvan, nieuwe methodes te ontwikkelen die minder afhankelijk zijn van het matchen van circuit onderdelen (vooral het matchen van capaciteiten) en parasitaire effecten (vooral de invloed van parasitaire capaciteiten).

Op systeemniveau, worden orthogonale ontwerpprocedures ingezet (in gebruik genomen) om er voor te zorgen dat artefacten, die kunnen ontstaan door circuit imperfecties, in de systeemoverdracht worden vermeden. Bijvoorbeeld in SC filterontwerp, orthogonal-hard-ware-modulation helpt om de invloeden van $N$-path ongelijkheden te verleggen door een extra vrijheidsgraad in te voeren, waarbij het aantal hardware paden $N$ (hardware modulatie) wordt ontkoppeld van de functionele modulatie factor $n$, gekenmerkt door de $z$-domein transformatie $z \rightarrow z^{n}$. Voor het ontwerp van algoritmische ADCs, of cyclisch of gepipelined, conventionele technieken maken gebruik van vermenigvuldigende digitaal-naar-analoog omzetters (of wel MDACs) die hoge eisen stellen aan de nauwkeurigheid van capaciteitsverhoudingen om nauwkeurige signaalvermenigvuldiging te kunnen realiseren. Aan de andere kant, in dit proefschrift, de ADC functie wordt opgebroken tot de eenvoudige deel-functies van het opsommen en niveauverschuiving van signalen welke gerealiseerd kunnen worden met SC technieken die niet afhankelijk zijn van nauwkeurige capaciteitsverhoudingen.

Op circuitniveau, worden delta-charge flow $(\delta-Q)$ technieken gebruikt om SC circuits te realiseren met nauwkeuriger overdrachten dan de rechtdoorzee manier van charge-transfer ( $Q T$ ). Anders dan bij $Q T$ SC circuits, (is er geen behoefte aan) wordt geen signaalladingsverschuiving vereist van capaciteit naar capaciteit door middel van het virtuele aardpunt van de versterker. In plaats daarvan, vloeit alleen maar een delta-lading $\delta Q$ in het virtuele aardpunt van wege de aanwezigheid van parasitaire capaciteiten aan de ingangen van de versterker in een praktische realisatie. Voor het ontwerp van SC filters, is delta-charge-redistribution $(\delta-Q R)$ een manier om nauwkeurige filter overdrachten te implementeren door gebruik te maken van passieve ladingshervedeling tussen capaciteiten in de terugkoppellus van een versterker. Dit is anders dan bij $Q T$ SC filters, waarbij de versterker zorgt voor actieve ladingsver-
schuiving tussen capaciteiten om de filter overdracht te realiseren. Voor het ontwerp van ADCs, wordt een hoge nauwkeurigheidsmethode $(C+C)$ voorgesteld voor het opstapelen van capaciteitsspanningen die gebruik maakt van een floating-hold-buffer voor implementatie. De nauwkeurigheid waarmee signalen kunnen worden opgeteld is praktisch ongevoelig voor zowel het matchen en lineariteit van signaalcapaciteiten als de aanwezigheid van parasitaire capaciteiten aan de versterker knoopunten.

Tevens worden een aantal andere innovatieve circuit technieken beschreven in dit proefschrift zoals: een flexibele track-and-hold (T\&H) die herprogrameerbaar is voor unipolar, bipolar en differentiele modes; klok skew (scheefheid) ongevoelig samplen; een commonmode terugkoppel circuit die de common-mode onderdrukking van enkelzijdig versterkers sterk vebetert; dubbel-ingang enkeltrapsversterkers met een hoge efficiëntie en uituurbereik; een lage referentie comparator.

De concepten ontwikkeld en geanalyseerd zijn vervolgens gedemonstreerd in de praktijk met het ontwerpen van CMOS SC banddoorlaatfilters en algoritmische ADC trappen (zowel cyclisch als gepipelined). De gehaalde intrinsieke nauwkeurigheden zijn een sterke verbetering op voorafgaande state-of-the-art oplossingen. Bijvoorbeeld, door gebruik te maken van de voorgestelde methodes, een in standaard CMOS geïntegreerde 10.7 MHz radio IF selectiviteitsfilter haalt een hogere nauwkeurigheid dan keramische filters. Een andere voorbeeld is een ADC met meer dan 12-bit intrinsieke nauwkeurigheid, alhoewel capaciteiten met maar 9bit matching worden gebruikt in de implementatie. De ADC architectuur is zeer robuust en heeft zich bewezen in een embedded digital VLSI applicatie in het nieuwste 65 nm CMOS technologie. Het is aangetoond dat het vermogensverbruik en oppervlak van de oplossingen hier beschreven lager zijn dan andere bekende oplossingen uit de literatuur.

## Acknowledgments

The work conducted for this thesis was carried out partly in the Advanced Systems Laboratory of Philips Semiconductors in Eindhoven, The Netherlands, and more recently in the Xilinx Mixed-Signal Centre of Expertise in Dublin, Ireland, which is part of Xilinx's Advanced Products Division. I am grateful to the management of both companies in supporting my collaboration with universities, especially the Technical University Eindhoven (TU/e). In particular, I wish to thank Paul Hovens, Kees Karman and Stephan Borgers of Philips and John Jennings of Xilinx.

My promotor, Arthur van Roermund, has been instrumental in ensuring a successful completion of my thesis. In spite of having almost dropped the idea of completing my thesis after having left Philips, Arthur helped me to re-focus and helped me adapt the content of my Ph.D. to better fit with my current research pursuits. I did the bulk of my writing in the last couple of years and he has supported me with every last aspect of preparing this thesis. He has taught me about the structured presentation of ideas and how to impart the key message to the target audience. At a personal level, I have had a long association with Arthur, both when I was in Eindhoven and now in Dublin. I have always enjoyed his company, his personable nature and his genuine interest in me and my family. I look forward to continuing this for a long time to come.

I would also like to take the opportunity at this point to thank all the members of the promotion commision for their time and effort in proof-reading and critically examining this thesis.

My time at Philips was especially inspiring for me and I learned much from many colleagues. There is such a broad range of expertise at Philips at every technical level that it was always a pleasure to gain from this expertise. I benefitted enormously from the experience of Noud Boudewijns and Ton van Keeken and enjoyed our many intense discussions on all aspects of electronic engineering and daily life. Thanks also to ex-colleagues Paul Hovens, Ton Nillesen, Kees Jaspers, Dick de Greef, Henk ten Pierick and Ad van den Enden for sharing their technical expertise.

At Xilinx too I have been very lucky to have been able to explore new topics in integrated mixed-signal systems which have helped me broaden my experience. I am grateful for the valuable cooperation of all my colleagues in the Mixed-Signal group, especially John Jennings, Anthony Collins, and Maxim Pribytko. Thanks also to the FA lab in Xilinx Ireland,
especially Cathal McAuley for helping out with some photos.
I value my contacts and continuing cooperation with the Mixed-Signal Microelectronics Department of TU/e. Hans Hegt and the PhD candidates - especially Georgi Radulov, Athon Zanikopolous, and Pieter Harpe - in the data converter group have made me feel very welcome in the group. I have enjoyed both the friendship of Georgi as well as his enthusiastic interaction on current-steering DACs. I am also grateful to a number of previous Masters' students I had down the years, especially Koen van Hartingsveldt who did a sterling job working on the Radio IF filter.

Finally, I would like to give special thanks to my wife Orla who has supported me through thick and thin in getting this thesis finished. My parents too encouraged me and impressed on me the importance of achieving my Ph.D. Last but not least, although now only a few weeks old, Siobhán played an especially important role in focussing me on getting finished before arriving on the scene and taking up all the slack left after the thesis.

## Biography

Patrick John Quinn graduated in Electronic Engineering at University College Dublin with a B.E. degree in 1986 and a M.Sc.(Eng.) degree in 1989. The M.Sc. thesis was entitled "Design and investigation of a direct conversion FM receiver and its application in mobile radio". The research for the thesis was carried out in the Mobile Telephony group at Philips Semiconductors in Eindhoven.

From 1989 to 2000, he was employed at the Philips Semiconductors Advanced Systems Lab in Eindhoven. There he worked in various roles from IC design engineer to project leader in the areas of mobile telephony, video and radio systems and circuits. Most projects were based on analogue sampled-data processing, usually using switched capacitor circuit techniques for implementation.

At the end of 2000, he joined the mixed-signal centre-of-expertise of Xilinx at its European HQ in Dublin, Ireland. There he is team leader and technical lead of advanced mixed-signal IC design projects for Virtex FPGAs down to 65 nm CMOS. These are the first mixed-signal systems to enter into full 65 nm production of any company in the world.

The author has a range of professional publications and international patents. He has had a long association with the research activities of the Mixed-Signal Microelectronics department of the Technical University of Eindhoven under the chairmanship of Professor van Roermund. This relationship has contributed to the development of this thesis.

# STELLINGEN 

behorende bij het proefschrift

# High-Accuracy <br> Switched-Capacitor Techniques Applied To Filter And ADC Design 

Patrick John Quinn

13 September 2006

1. $\delta-Q \mathrm{SC}$ techniques are an example of disruptive innovation [1] for accuracy improvement in that they don't rely on the further refinement of existing $(Q T)$ techniques. [This thesis].
2. Tolerance to non-linear settling, while achieving an overall linear system response, makes SC techniques a powerful technology for accurate analogue circuit design. [Chapter 3].
3. By exploiting the inherent level shift properties of SC circuits, low power, and indeed low voltage, signal processing structures can be created which can simultaneously satisfy the demands of optimal DC biasing with optimized dynamic performance. [Chapter 4].
4. A multiplying DAC is best realized using additive means. [Chapter 9].
5. A data converter can only be as good as its auxiliary circuitry.
6. More for historical than for scientific reasons, switched capacitor technology has come to dominate ADC design, while switched current technology (current steering) has come to dominate DAC design.
7. The continually improving ecomonies of process scaling, as predicted by Moore's Law, do not translate to test. A paradigm shift in test methodology is needed. [Chapter 2, and [2]].
8. The key to good project management is the timely discovery of the unknown unknowns.
9. Those in power write the history; those who suffer write the songs. Ireland has a lot of songs. - After Frank Harte.
10. Nothing is impossible, the impossible just takes longer and costs more.
11. Experience always comes too late for when you need it.

## References

[1] C.M. Christensen, M.E. Raynor, The Innovator's Solution, Harvard Business School Press, ISBN 1578518520, 2003.
[2] International Roadmap for Semiconductors (ITRS) 2005 - http:// www.itrs.net/Common/2005ITRS/Home2005.htm, 2005.


[^0]:    1) Bottom-plate sampling is often used in SC design to reduce distortion from sampling. It is demonstrated in Fig. 2.2 as a part of a larger SC network, in which the bottom-plate (large parasitic capacitance) is shown thicker than the top-plate (small parasitic capacitance). The bottom-plate switch to $\operatorname{Vin}_{p}$ is of much larger size than the switches to the top plate in order to guarantee a low switch resistance across the full input signal range. Consequently it contains much larger channel charge which is signal dependent. At the point of sampling, the bot-tom-plate capacitance of $C_{1}$ is charged to $\operatorname{Vin}_{p}$, while the top-plate is charged to the common-mode reference voltage $V_{c m}$. The top-plate is firstly disconnected on $c l k 1 e$, then the bottom-plate on $c l k 1$. Hence, the signal capacitor $C_{1}$ is allowed to float while $\operatorname{Vin}_{p}$ is being disconnected. This prevents signal-dependent charge injection from the bottom-plate switch entering $C_{1}$. Thus, $\operatorname{Vin}_{p}$ is preserved on $C_{1}$ after sampling. Note that since on the following phase, the top plate of $C_{1}$ is connected to the high impedance gate of a differential-pair at the amplifier input, this gate should also be pre-charged to $V_{c m}$ on $c l k 1 e$ before the top-plate of $C_{1}$ connects to this gate on the following clock phase $c l k 2 e$.
[^1]:    1) Sometimes in the literature, an algorithmic $A D C$ refers to a cyclic $A D C$ only but since both the cyclic and pipelined ADCs rely on the same algorithm (section 8.1.1), then cyclic ADC is used here to distinguish it from the pipelined ADC.
[^2]:    2) The output of the sub-DAC is sometimes depicted as $D_{i} \cdot \frac{V_{r e f}}{G_{i}}$ (with $G_{i}$ following the summer) but should be $D_{i} \cdot V_{r e f}$, as depicted here, to be true to the SC realization.
