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Substrate Transfer for RF Technologies

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Invited Paper

Abstract—The constant pressure on performance improvement in RF processes is aimed at higher frequencies, less power consumption, and a higher integration level of high quality passives with digital active devices. Although excellent for the fabrication of active devices, it is the silicon substrate as a carrier that is blocking breakthroughs. Since all devices on a silicon wafer have a capacitive coupling to the resistive substrate, this results in a dissipation of RF energy, poor quality passives, cross-talk, and injection of thermal noise. We have developed a low-cost wafer-scale post-processing technology for transferring circuits, fabricated with standard IC processing, to an alternative substrate, e.g., glass. This technique comprises the gluing of a fully processed wafer, top down, to an alternative carrier followed by either partial or complete removal of the original silicon substrate. This effectively removes the drawbacks of silicon as a circuit carrier and enables the integration of high-quality passive components and eliminates cross-talk between circuit parts. A considerable development effort has brought this technology to a production-ready level of maturity. Batch-to-batch production equipment is now available and the technology and know-how are being licensed. In this paper, we present four examples to demonstrate the versatility of substrate transfer for RF applications.

Index Terms—Low power, RF technology, silicon-on-anything, silicon-on-insulator, substrate transfer.

I. INTRODUCTION

THE TREMENDOUS growth of mobile and wireless appliances during the past decade has accelerated the development of RF technologies to a breathtaking pace. Whereas ten years ago cut-off frequencies (f_T) of 15 GHz realized in 0.7-μm BICMOS processes were state of the art, at present SiGe bipolar transistors with cut-off frequencies in excess of 200 GHz fabricated in 0.12-μm BiCMOS technologies have been reported [1], [2]. These results clearly indicate the enormous potential of silicon for future wired and wireless wide-band communications. However, to fully access the performance of these powerful RF devices, it will also be necessary to address issues which are more related to the (passive) environment in which the active devices are embedded and which are hampering the realization of highly or even fully integrated transceivers.

Reducing Power Consumption: This immediately translates into prolonged battery lifetime, but also enables the use of more complex circuit topographies adding functionality (e.g., diversity). Proper transistor scaling is a first prerequisite for low-power consumption. But even for well-scaled active devices the rapid charging and decharging of capacitances contributes for a significant part to the total power consumption. These capacitances consist mainly of capacitances to ground, e.g., collector/drain to substrate, interconnect to substrate, or load to substrate [3], [4].

Integration of Better Passives: The RF section of modern wireless appliances is still swarmed with many expensive and bulky off-chip passive components like SAW filters, inductors, capacitors, and varicaps. As a first step, innovative design techniques can be used to minimize the number of required passives (e.g., zero/low IF, polyphase filtering) [5]–[7]. But even then it is attractive to integrate the remaining passive RF elements, not only because it will result in a better performance, a smaller form factor, lower cost, and higher added value, but also in a lower power consumption. If we define everything apart from the active transistors as a passive element, then the demand for better passives also encompasses interconnect, bond pads, and ESD devices with low parasitic capacitances and low thermal noise.

Reduction of Cross-Talk: The unavoidable leakage of RF energy between different circuit blocks is a constant nuisance to designers of mixed-signal ICs. The effect is often difficult to predict and heavily technology-dependent. The result is long design cycles, often involving one or more redesigns and/or an increase in silicon area due to an excessive use of guard rings. Even worse, problems solved for one technology node might turn up again at the next. Modern full duplex standards like W-CDMA even add to this problem because transceivers are receiving and transmitting at the same time.

Many of the above-mentioned problems are in one way or the other related to the silicon substrate. It is often not realized that the devices of an integrated circuit are confined to the top 2 μm or so of a silicon wafer and that the remaining 99.6% of the silicon only acts as a mechanical carrier to allow for wafer-scale processing. Indeed, from a processing point of view silicon is an excellent choice: state of-the-art IC technology has enabled the fabrication of integrated circuits with a mind-boggling device density and active device performance. As a mechanical carrier, however, silicon is not always an obvious choice, especially with regard to RF applications. Silicon unfortunately is neither an isolator nor a perfect conductor, and all devices

have a capacitive coupling to this resistive substrate. At RF frequencies, energy is dissipated in the silicon substrate resulting in passive devices with a poor quality factor. In return, thermal noise (kTR) is injected back into the circuit. Also, since all circuit elements are capacitively coupled to the distributed resistor network in the substrate, noise injection becomes a fundamental problem.

An obvious first step in tackling this problem is to modify the substrate resistance. Substrates with a resistivity in excess of 5 kΩ·cm have been used to fabricate passive elements with quality factors comparable to those processed on quartz [8]–[10]. However, the co-integration of active devices on these high-resistivity substrates is far from trivial. The main issue here, apart from availability, is to maintain the high specific resistance during (high-temperature) processing and to prevent punch through of wells or buried layers. A next step is the use of silicon-on-insulator (SOI) substrates. Although the use of SOI substrates significantly will add to the bill of materials, in return it may substantially improve performance. SOI enables a complete dielectric isolation of devices and, in particular, the class of bonded SOI substrates may be used to combine high-resistivity substrates with standard IC processing [11], [12]. Silicon-on-sapphire can be seen as the ultimate form of SOI offering silicon on a perfect isolator [13], [14]. However, issues concerning price, yield, availability, and increased process complexity have prevented its use other than for specific aerospace and military applications. An alternative way to produce true SOI material is proposed by SOITEC using the Smart Cut technology [15]. Here hydrogen ion implantation is used as an atomic scalpel to cut thin slices of monocrystalline film from a donor wafer, which are then transferred on the top of a receiving wafer by means of (high-temperature) van der Waals bonding. Using this technique silicon-on-quartz as well as silicon-on-glass wafers have been produced. However, the processing of these materials is not straightforward: clean-room equipment generally has a difficulty in handling fully isolating and/or (semi) transparent substrates. Finally, quartz is very expensive while glass may pose problems from a contamination point of view.

In this paper, we propose a substrate transfer technology (STT), which combines the advantages and ease of standard silicon processing with a complete freedom of substrate choice [16]–[18]. The technology is based on the gluing of a fully processed silicon wafer, top down, to an alternative substrate followed by a complete or partial removal of the original substrate (Fig. 1). Glass is an obvious choice for a replacement substrate because it combines excellent RF properties with a good availability and low price. The advantages of this approach are most obvious if it is used in combination with an SOI-based process. In this case, a perfect etch stop underneath the actual circuit layer allows for the complete removal of the original silicon substrate. It enables the integration of high-quality passives, a maximum reduction of cross-talk and parasitic capacitances. At the same time it opens the way to double-sided device processing [19], [20] and new wafer-scale device packaging concepts (this paper, [21], and [22]). Since it is a post-processing step, it is straightforwardly implemented on existing production lines. In this paper we will, in addition
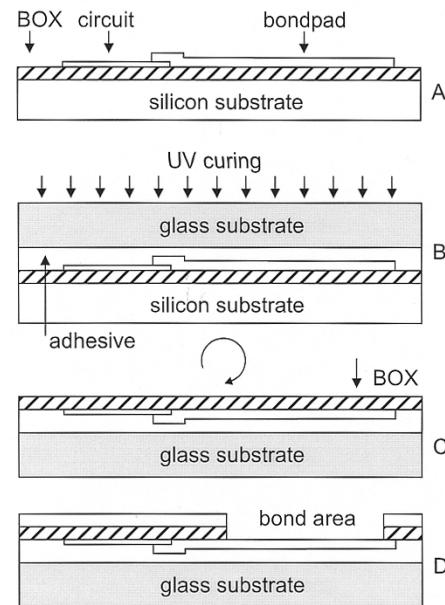

Fig. 1. Schematic cross section of the transfer of an SOI wafer to a glass substrate. (a) fully processed SOI wafer. (b) Curing of adhesive by UV exposure through the glass substrate. (c) Removal of the silicon substrate selective toward the buried oxide. (d) Optional deposition of a scratch protection layer and opening of bondpads.

to demonstrating two SOI-based applications, also demonstrate the significant advantages of STT for standard bulk processes.

Although substrate transfer techniques based on the use of adhesives have since long been proposed by the III–V community [20], [23], it has until now not found acceptance as a viable technique in the high-volume silicon industry, presumably due to the lack of suitable production equipment. A major development effort however, has brought STT to a production-ready level and has demonstrated itself to be a valuable new process step in IC fabrication technology. To stimulate proliferation of STT Philips has decided to license STT technology and know-how to third parties.[1] We will now first discuss the technological details concerning the STT process in general. Then four different applications of STT will be presented.

II. SUBSTRATE TRANSFER TECHNOLOGY (STT)

Vital in this technology is the gluing of a silicon wafer, top down, to an alternative substrate, e.g., glass. Crucial to the success of an adhesive bonding technique like this are the properties of the glue. The requirements for the glue can be summarized as follows.

Mechanical Stability: After transfer of the circuit layer to the new substrate, it has to comply with standard dicing, wire bond, packaging, and reliability testing procedures.

Thermal Stability: For certain applications, it may be necessary to continue with some additional processing after transfer of the circuit layer to the new substrate. For this reason, the transferred substrate should be able to withstand reasonable resist baking and PECVD/metal deposition temperatures.

[1][Online.] Available: www.emtechnologies.nl

Ease of Use: The use of the glue should be straightforward without the need for very complicated equipment or elaborate procedures. The glue layer itself should accommodate the topography in the wafer and result in a stress-free layer.

The adhesive we use largely fulfills these requirements. It is a monomer which after cross-linking forms a very hard acrylic. The absence of solvents is crucial since it would be impossible to diffuse any solvents in a layer of only a few micrometers from the center of a 6–8-in wafer to the edge. The monomer cross-links at temperatures of about 200 °C. Additionally, the cross-linking process may be promoted by the addition of either UV- or thermal-sensitive initiators. The UV-sensitive initiator that we use allows the adhesive to be cured in seconds at room temperature. This is very important: every curing process that needs an elevated temperature is troubled by differences in thermal expansion coefficients between the two substrates, which may result in unacceptable bowing or warping of the final substrate at room temperature. The gluing procedure described in detail below results in a uniform layer of glue with a thickness of 5 to 10 μm, accommodating the topography of the silicon wafer. Our experiments have shown that topography up to 4 μm poses no problem whatsoever. This is an advantage over some other techniques, like anodic wafer bonding, which require a fully planarized wafer surface. The adhesive is capable of withstanding corrosive chemicals such as the etchants used to remove the silicon substrate. Thermal stability is guaranteed to a temperature of 300 °C over a prolonged period of time. This is high enough for the deposition of high-quality PECVD layers. Extensive tests with circuits transferred to glass have shown that standard dicing and assembly equipment can be used to package devices. The relatively low glass transition temperature of the adhesive (below 100 °C) hampers wire bonding at elevated temperatures. However, the use of modern HF wire bonders has pushed the number of failing bonds back into to the ppm region as required for mass production. The glue has a low, water-like, viscosity that makes it easy to dispense. Finally, we should mention that the adhesive is highly transparent.

III. PROCESSING PROCEDURE

Almost all glasses can be used for substrate transfer. However, to remain more or less compatible with IC manufacturing procedures, we use an alkaline-free, high-barium-content glass like AF45 from Schott. This cheap process glass is also used for low-end LCD production and is available in sheets with a thickness of 400 μm. Round glass wafers including a flat (if required) are commercially available. Proper rounding of the glass edges to remove micro-crack damage virtually eliminates breakage of glass wafers during processing.

A modified Piranha clean is used to remove any metallic or organic surface contamination. After IC processing, the silicon wafer (SOI or bulk) and the glass substrate are primered. The primer promotes adhesion between the substrate and the glue. It consists of molecules that on one side react with hydroxyl groups at the wafer surface and on the other side react with the double-bonded carbon atoms of the glue molecules. The primer is applied solely by spinning followed by dry spinning, without additional baking or rinsing. Since hydroxyl groups are crucial

Fig. 2. ASiGS 625: a fully automatic batch-to-batch gluing machine. The machine accepts a batch of 6-in silicon wafers and a batch of 6-in glass wafers. After gluing and curing, it returns a batch of silicon-glass sandwiches.

for a perfect adhesion, the top layer of the silicon wafer preferably has to be a PECVD oxide layer. By correctly applying the primer procedure, the adhesion directly to the glass is perfect.

The next step is the actual gluing of the two wafers. During the research stage of process development, a simple manual procedure was used consisting of dispensing the glue, placement of the wafers, and pressing the wafer sandwich to remove the excess glue, resulting in a final glue thickness to 5 to 10 μm. Care should be taken to avoid the inclusion of air bubbles since they will result in a defect after silicon removal. The manual procedure works fine and is still used for all wafer diameters other than 6 and 8 in.

The manual procedure is of course not suitable for production. Therefore, to bring STT to an industrial level, fully automatic batch-to-batch equipment has been developed in cooperation with em technologies. Fig. 2 depicts the ASiGS 625 (Advanced Silicon-insulator Gluing System, 6-in, 25 wafers/h). The machine consists of a gluing stage, a curing stage, and a robot wafer manipulator. The central gluing stage consists of two opposing vacuum chucks that are rigidly coupled in the rotation direction, but can move independently in the vertical direction. The robot places the silicon wafer (face up) on the lower vacuum chuck and the glass substrate (face down) against the upper vacuum chuck. After a certain amount of glue has been dispensed in the center of the silicon wafer, the upper chuck moves down, thereby pressing the glue from the center to the edge. As it reaches the edge, the chucks start to rotate to remove the excess glue. The construction of the gluing stage directly produces the force to reduce the thickness of the glue to its final value of 5–10 μm. This procedure yields a uniform, air-bubble-free glue

layer. A similar apparatus as depicted in Fig. 2 has been built for 8-in wafers. The fact that only minor modifications in the process parameters were necessary when going from 6 to 8 in is indicative for a comfortable process window.

After gluing, the wafer sandwich is transferred to the curing stage. For UV curing, a simple 220-V/500-W halogen light source is used. Its UV spectrum is such that the cross-linking process proceeds relatively slow. Since the glue shrinks ca. 10% during curing, this allows for some redistribution of glue from areas with high topography to areas with low topography. A 30-s UV exposure under nitrogen ambient at room temperature is sufficient to cure the glue.

Depending on the type of silicon substrate, SOI or bulk, the silicon substrate can now be either completely or partially removed. In this section, the complete removal of the (SOI) substrate will be discussed. The partial removal of the silicon substrate will be discussed in one of the applications in the next section. At the production site, the removal of the silicon substrate is done by first grinding the silicon down to 50 μm on a standard DISCO grinder, followed by a 30-min 70 °C KOH etch to remove the remaining silicon using the buried oxide as an etch stop with a selectivity in excess of 1000. During the research stage of process development, the complete substrate was removed by wet etching because no grinding equipment was available. A two step etching process was used with the first step being a 3-h 100 °C KOH to etch the silicon down to ca. 30 μm, followed by a second step identical to the one mentioned above. The glue and the glass are able to withstand this etching inferno without any visible degradation. Two of the four substrate transfer applications presented in this paper require a partial removal of the silicon substrate. In this way also, non-SOI-based processes can be used in combination with STT. Partial removal of the silicon is achieved by deposition and patterning of a hard-etch mask layer after the first thinning step when the silicon has been thinned to 30–50 μm. The specific process details will be described in the discussion of the respective applications hereafter. After etching, the wafer is cleaned and ready for further processing.

In the simplest form of substrate transfer (application 1), the next step will be the deposition of a PECVD nitride dirt barrier layer, followed by opening of bond pad areas. During research, a simple contact aligner was used for photolithography after wafer transfer. At the production site, the wafers are exposed using a Canon stepper. Bond pad areas may be opened by either dry or wet etching. More elaborate forms of substrate transfer, which take advantage of the possibility to process the devices from the backside as well, have been developed by Nanver *et al.* [19]. Their process requires fine pitch lithography on the circuit layer after substrate transfer. To achieve an accurate front-to-back wafer alignment accuracy, mirror symmetric alignment markers for an ASML PAS5000 stepper have been developed by van Zeijl *et al.* [24], [25]. The mirror symmetric alignment markers were used in combination with standard overlay test procedures to characterize the front-to-back wafer overlay accuracy. The practical feature size that can be realized on the back wafer was found to be as small as 0.9–1.2 μm.

In addition to glass, many other materials can be used as a substrate depending on application requirements. Fig. 3 depicts
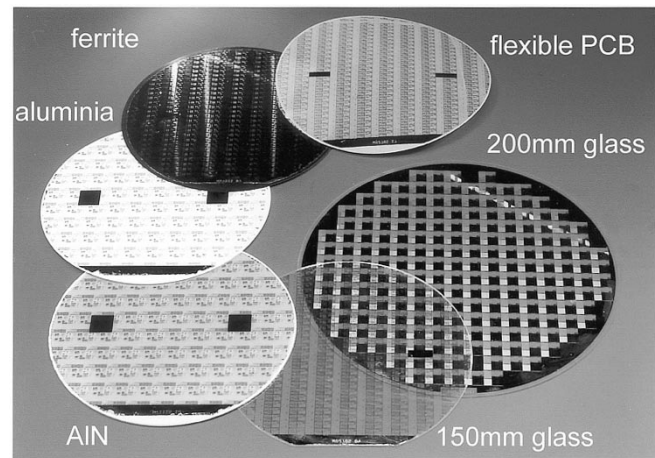

Fig. 3. Silicon circuits transferred to different types of substrates: glass (8 and 6 in), aluminum nitride, alumina, ferrite, and flexible glass-fiber epoxy.

circuit layers transferred to glass, alumina (Al_2O_3), aluminum nitride, NiZn ferrite, and flexible glass-fiber epoxy. To ensure optimum adhesion when using nonglass substrates, a PECVD oxide layer is deposited on the surface of the substrate prior to primering and gluing. For semitransparent substrates like alumina, aluminum nitride, and glass-fiber epoxy, UV curing can still be used by simply increasing the light intensity. In case of an opaque substrate like ferrite, the UV-sensitive initiator is replaced by a thermal sensitive initiator to reduce the curing temperature to 80 °C.

IV. APPLICATIONS

In this section, we present four RF applications of the proposed substrate transfer technology. The first example is the straightforward transfer of circuits fabricated on (thin-film) SOI substrates to glass with complete removal of the original silicon substrate. In this case, a dedicated lateral bipolar process is used to achieve ultralow-power operation. The second example uses a normal bulk IC process. In this case, the silicon is partly removed, leaving the active devices grouped in silicon mesas. The last two examples show how substrate transfer can additionally be used to realize new packaging concepts with strongly reduced parasitics and improved heat sinking.

A. A Low-Cost Lateral Bipolar Technology on Glass

Much of the efforts spent in the development of RF technologies are focused on the realization of transistors with extremely high cut-off frequencies. For most wireless applications in the 2–3-GHz range, however, a moderate f_T of 10–15 GHz is sufficient. For these battery-operated appliances, low power consumption is often of greater importance than extremely high f_T. Whereas frequency scaling involves profile optimization, scaling for low power primarily requires minimizing the emitter area combined with a proportional reduction of parasitic capacitances, especially to ground. The standard approach to achieve this is to use advanced lithography and isolation techniques like shallow and deep trenches.

Bipolar transistors on SOI are attractive as low-power RF devices [3], [16]. Fig. 4 depicts a schematic top view and
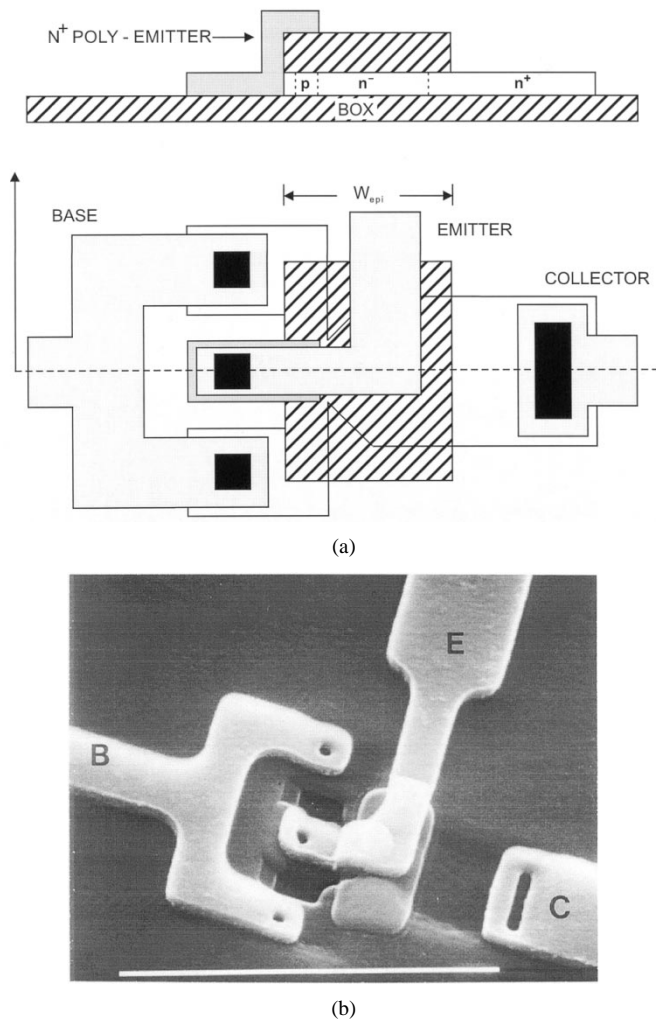
(a)

(b)

Fig. 4. (a) Schematic cross section and (b) SEM top view of the lateral bipolar transistor structure.
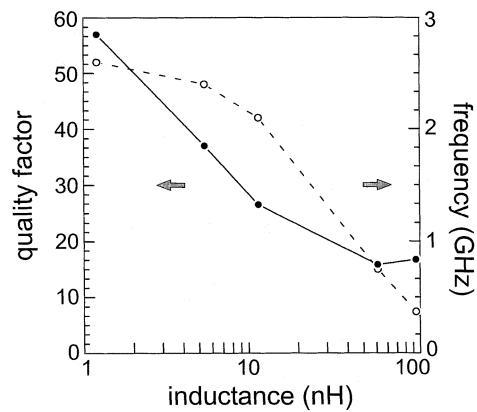

Fig. 5. Measured quality factor and frequency at which this maximum is reached versus inductance for a selection of available inductor structures in the lateral bipolar technology on glass.
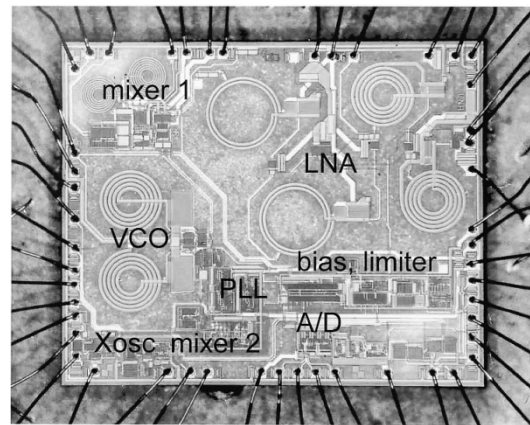

Fig. 6. Fully integrated GPS receiver frontend. The circuit was fabricated in the lateral bipolar SOI technology and after processing transferred to glass.

cross section of the lateral bipolar structure we proposed. The 0.1–0.2-μm-thin top silicon layer that is available in SIMOX or UNIBOND SOI material allows for emitter sizes as small as 0.05 μm^2 using half-micrometer lithography. Moreover, the semi-two-dimensional lateral transistor structure with oxide isolation on both sides allows junction capacitances to be scaled to values well below 1 fF. Despite a relatively low f_T of 10–15 GHz limited by the diffused base, this results in a gain of 24 dB at 2.6 GHz and a collector current as small as 15 μA. It is obvious that for such small devices it is very important to minimize stray capacitances, especially to ground. By transferring the circuits to glass, an ultimate reduction in substrate capacitances by a factor of 5 to 200 (depending on feature size) can be achieved [26]. Furthermore, it allows for the integration of high-quality passives like spiral inductors free of substrate parasitics. Fig. 5 depicts the maximum quality factor and the frequency at which this maximum quality factor is reached for a selection of inductors available in the device library. A quality factor as high as 57 is realized for a 1.2-nH inductor with a diameter of 400 μm using a 3-μm-thick top aluminum layer. The availability of these high-quality passive components helps for low-power since it reduces the need to go on-and-off chip with RF signals.

The process including transfer to glass has been industrialized by Philips Semiconductors, and the first parts will have been shipped to customers by the end of 2002. Naturally this means that the parts comply with all standard reliability and lifetime tests, demonstrating that substrate transfer is indeed a viable option for high-yield mass production.

Fig. 6 depicts one of the first products: a highly integrated GPS receiver frontend. The possibility to integrate spiral inductors enabled the integration of the antenna filter and VCO and eliminated an RF surface acoustic wave (SAW) filter. The integration of these RF functions greatly reduces the amount of RF knowledge needed by the set maker and made it possible to use a simple two-layer printed circuit board (PCB) in the application instead of an expensive six-layer PCB. These advantages/savings more than justify the integration of these large inductors. The 14–mask process additionally offers lateral pnp transistors, dense I^{2}L logic, varactors, 7-kΩ/sq resistors, 1.5-nF/mm^2 capacitors, and three layers of interconnect including a 3-μm-thick Al top layer for spiral inductors.

B. A Low-Cost Substrate Transfer Technology for Non-SOI Processes

The full benefits of STT are only obtained if it is used in conjunction with an SOI-based process since the buried oxide
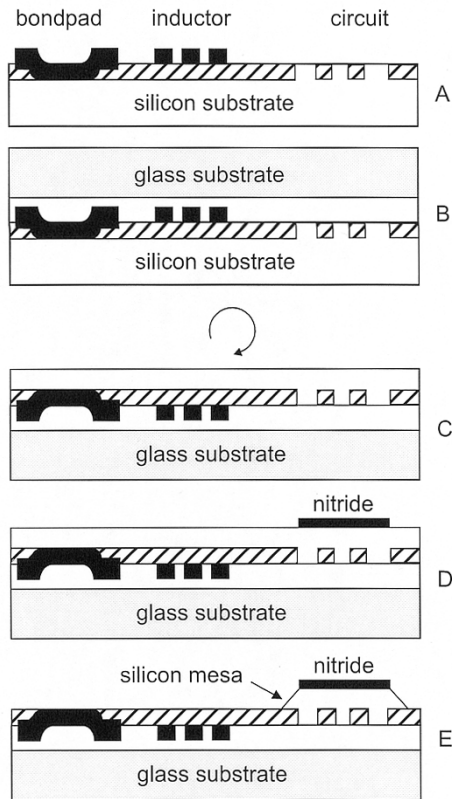
Fig. 7. Schematic processing sequence to transfer non-SOI wafers to glass. (a) A fully processed wafer with active devices grouped into functional units. (b) Gluing of wafer to a glass substrate. (c) Silicon thinned to 50 μm. (d) Deposition and patterning of PECVD nitride etch-mask. (e) Etching of the silicon using the field oxide as an etchstop.

layer allows for a complete removal of the silicon substrate underneath all circuit elements. In a standard non-SOI process (BICMOS, CMOS), it is difficult if not impossible to reliably remove the substrate by selectively stopping on n-/p-type buried layers or well diffusions. It is however possible to retain some of the most important advantages of STT in combination with a partial removal of the silicon substrate [17].

This procedure using a standard process in a conventional silicon bulk wafer is illustrated in Fig. 7. The fully processed wafers are again glued to a glass substrate following exactly the procedure as described previously [Fig. 7(a) and (b)]. The process deviates in that, after the silicon has been thinned to ca. 50 μm, a mask is applied to selectively etch silicon mesas. This is done by first grinding the silicon down to 60 μm using the glass as a mechanical support followed by polishing an HNO$_3$/HF etch to remove micro-crack damage [Fig. 7(c)]. Next a 0.5 μm thick PECVD nitride layer is deposited. A resist mask is applied by contact printing using an infrared alignment system. The nitride is patterned in a CF$_4$ barrel etch [Fig. 7(d)]. After resist removal, the silicon mesa is etched in a KOH-isopropanol etchant using the fieldoxide as an etch stop [Fig. 7(e)]. A small modification in the IC process makes the bondpads directly accessible after the silicon mesas have been etched. This is done at the stage when normally contacts to devices are etched before the first interconnect level is deposited, by wet etching the field oxide at the location of the bondpads [Fig. 7(a)]. Since KOH does not attack the Ti/TiN barrier layers
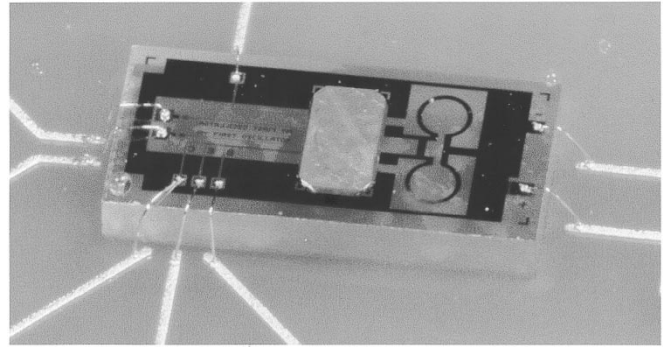

Fig. 8. VCO demonstrator circuit. The actual circuit resides underneath the silicon mesa. The resonator tank and bondpads are completely on glass. After dicing the circuit was directly mounted on a PCB to facilitate accurate measurement of phase noise.
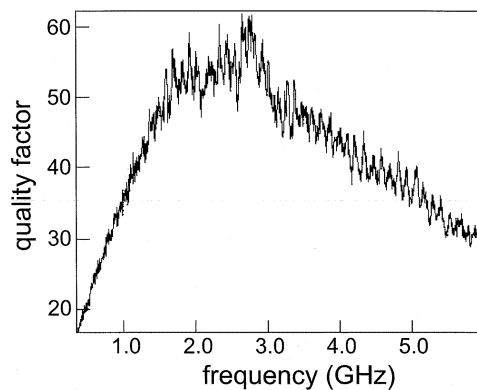

Fig. 9. Quality factor versus frequency for a single-loop inductor transferred to glass. The metal was 30-μm-thick Al with a width of 100 μm and an outer diameter of 500 μm.

underneath the first metal layer, this will immediately expose the backside of the bondpads after transfer.

Fig. 8 depicts a simple oscillator demonstrator circuit fabricated in a 30-GHz double-poly bipolar process available in our research FAB [29]. Clearly visible is the silicon mesa containing the active devices. Although in this example only one mesa is used, two or more of these mesas could be used to minimize cross-talk between critical circuit blocks. Besides the advantages of easy implementation using existing processes, the best possible passives like inductors, and a maximum reduction of cross-talk, this technique also has its limitations. First of all, despite the STT, it brings no benefit for the active devices. Second, the factor of one hundred higher thermal resistance of glass with respect to silicon severely limits the amount of power that can be dissipated. For example, the thermal resistance of the silicon mesa depicted in Fig. 8 (700 $\times$ 1300 μm^2) to the leadframe in air (worst case) was measured to be 300 K/W. In this example, the circuit dissipated 18 mW resulting in an acceptable temperature increase of 26 °C.

As mentioned, the circuit depicted in Fig. 8 merely served as a technology demonstrator and was by no means optimized for optimal performance. The inductors used have an inductance of 1 nH with a quality factor of 25 at 5 GHz. The circuit oscillated at 3.9 GHz on a supply voltage of 3 V and a power dissipation of 7 mW with an additional 11 mW for bias circuits and output
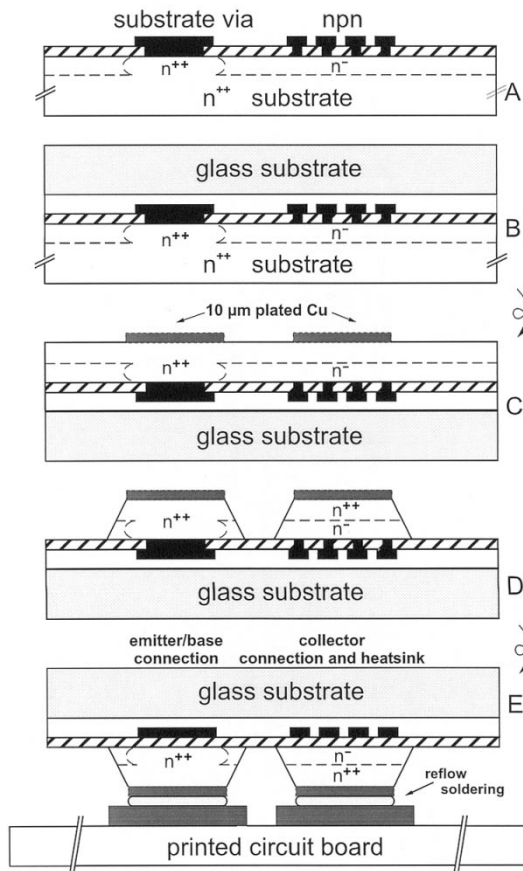
Fig. 10. Schematic processing sequence for the fabrication of surface mounted RF transistors on glass. (a) Fully processed wafer with via diffusions for frontside to backside wafer connection. (b) Wafer glued to a glass substrate. (c) Silicon thinned to 5 μm. (d) Formation of 10-μm-thick copper plated contacts. (e) Anisotropic KOH etching of the remain down toward the field oxide using the copper contacts as etching masks. (f) Soldering of the separated devices to the PCB.
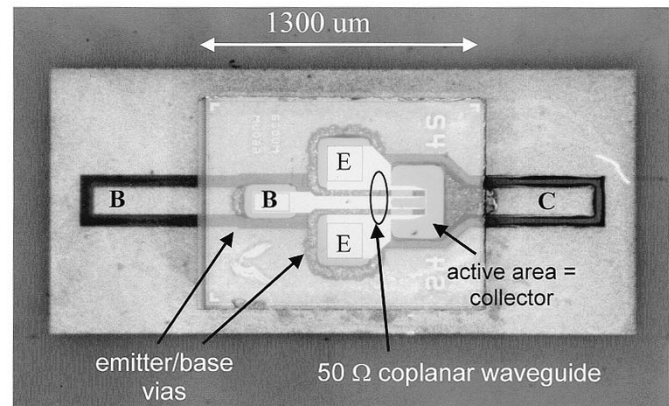

Fig. 11. A 0.5-W test transistor soldered to a test substrate viewed through the glass. The device consists of two blocks of 11 emitter fingers, each 0.4 $\times$ 30 μm^2.
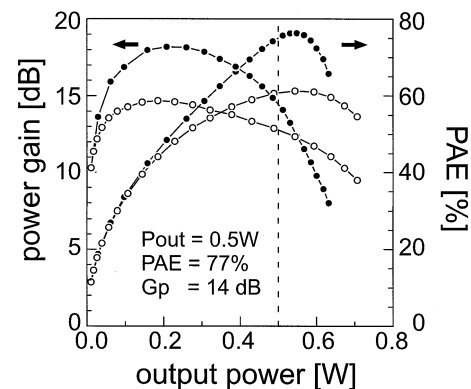

Fig. 12. Measured power gain (G_p) and PAE versus output power for a standard device ($\bigcirc$) and the SMD device ($\bullet$). The devices are tuned for maximum efficiency at 0.5 W, 1.8 GHz, 3-V bias, and class AB operation.

buffers. The phase noise was measured to be −108 dBc at a 1-MHz offset. In the meantime, inductors with a quality factor of 60 have been fabricated using wider metal (Fig. 9). This in combination with a more elaborate circuit design will substantially improve circuit performance.

So far we addressed only the IC process itself and not the package. For demanding applications, however, packaging parasitics like, e.g., bond-wire inductances can seriously deteriorate the overall circuit performance. The importance of the package will only increase with increasing frequencies. The next two examples show how substrate transfer can be used to introduce new packaging concepts.

C. Surface-Mounted Discrete Bipolar RF Power Transistors

The talk-time of cellular phones is to a large extent limited by the power gain (G_p) and power-added efficiency (PAE) of the power amplifier (PA) in particular of the final output transistor. It has been shown that these parameters are strongly affected by device and assembly parasitics [27], [28]. Any emitter series (bondwire) inductance will result in a negative feedback reducing G_p. At the output of the transistor, any (lossy) capacitance to ground will result in dissipative losses and an attenuation of higher harmonics resulting in a reduced PAE. Using

STT, we have demonstrated a device/packaging concept which offers maximum power gain through the elimination of bondwires, maximum efficiency by virtual elimination of output capacitance and losses, and wafer-scale fabrication of low-cost surface mounted devices (SMDs) [18].

The starting material for device fabrication are heavily arsenic doped 6-mΩ·cm n^{++} $\langle 100 \rangle$ silicon substrates. After a 0.9-μm-thick lightly doped epi layer is grown, phosphorus is diffused to make a low-resistivity connection between the frontside of the wafer and the substrate [Fig. 10(a)]. Next, npn devices are fabricated using a standard double poly-silicon technology [29]. The epilayer thickness and dope were chosen to optimize f_T versus ruggedness requirements resulting in an f_T of 25 GHz and BV$_{ceo}$ of 4.5 V. The substrate acts as the collector contact, so that a single layer of metal is sufficient to connect the interdigitated emitter and base fingers to the diffused vias. Total processing requires only six masks.

Exactly identical to the previous application, the processed wafers are glued, top-down, to a glass substrate and the silicon is thinned to 50 μm [Fig. 10(b)]. Next 10-μm-thick plated copper contacts are formed at the location of device contacts [Fig. 10(c)]. Using the copper as an etch mask, the silicon is anisotropically etched, stopping on the field oxide [Fig. 10(d)]. The silicon mesas with plated copper serve as device con-
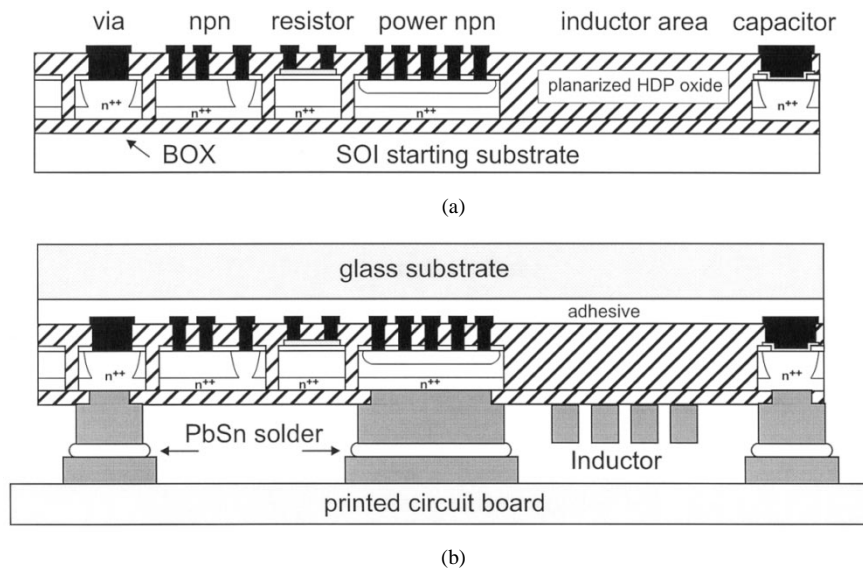
Fig. 13. Schematic cross section for the surface-mounted RF IC technology. (a) Fully processed SOI wafer with typical devices. (b) Final device soldered to a PCB after transfer-to-glass, etching of silicon, backside processing, and dicing.

tacts. After dicing, the devices are ready for surface mounted assembly [Fig. 10(e)].

To facilitate large-signal characterization, a 0.5-W transistor structure was fabricated. The devices were soldered to an Al_2O_3 test substrate with plated gold 50-Ω coplanar waveguides using commercially available reflow soldering equipment (Fig. 11). Note that the 50-Ω coplanar substrate waveguide is continued on-chip, effectively eliminating all interconnect and via inductances directly up to the active area itself. The devices are measured at 1.8 GHz, 3 V, and load-pull tuned for maximum efficiency at 0.5 W in class AB operation. Fig. 12 compares the measured G_p and PAE as a function of output power versus a standard wirebonded device without substrate transfer [28]. The fact that the measured PAE of 77% approaches the theoretical limit of 78% confirms the absence of substrate losses and output capacitance.

The concept is also very well suited for the fabrication of high-performance, small-scale integration monolithic microwave IC (MMIC) functions [18]. This example clearly demonstrates how a creative use of substrate transfer can be used to increase the lifetime of silicon processes just by tackling passive and packaging parasitics.

D. Surface-Mounted RF IC Technology

The same concept can be extended to full IC processes. The concept we propose is based on a combination of (thick-film) SOI substrates, a standard or only slightly modified front-end technology (CMOS/BiCMOS/bipolar), followed by substrate transfer and SMD assembly. In this work, a pure bipolar frontend was chosen because it was readily available in our research Fab and suited the demonstrator application. In this section, the first results are presented.

SOI substrates with 0.2-μm top silicon and 0.4-μm-thick buried oxide are used as starting material. The top silicon is doped n^{++} to 10^{20} cm^{-3} by diffusion from an arsenic doped glass to form a blanket buried layer. After epigrowth, a simple

bipolar frontend is fabricated based on a 25-GHz double poly-silicon technology. Unconventionally, device isolation is performed *after* the last high-temperature step (RTA emitter anneal). This is done by etching trenches down to the buried oxide, HDP oxide filling, and CMP. By designing the trenches well away from any p-type diffusions, junction leakage along trenches is avoided. Fig. 13(a) shows a schematic cross section of the finished wafer. The back-end trench procedure makes it possible to remove all the silicon in the areas reserved for inductors or micro-striplines and filling it with oxide while still retaining a fully planar surface. After transfer to glass, the wafers are flipped and processing continues on the former buried oxide layer. First, the oxide is (wet) etched at the locations where a contact to the backside of devices is needed (e.g., vias or power transistors). Next 10-μm-thick copper patterns are plated to form contacts and inductors. After dicing, the devices are directly reflow soldered to the PCB using the copper as contacts [Fig. 13(b)]. This concept offers the following advantages: 1) elimination of bondwire and package parasitics; 2) high-quality inductors/striplines; 3) effective heat transfer from power devices to PCB; 4) substrate-capacitance-free low-power RF devices; 5) extreme reduction of cross talk; 6) high-density MIM-like decoupling capacitors; and 7) possibility to fabricate sealed cavities. However, it is an entirely new packaging concept, implying that considerable development effort may be required to make it comply with normal reliability standards.

Fig. 14 depicts a balanced LC-VCO oscillator circuit included on the first test mask. The inset shows a circuit detail with backside illumination. Note that a fine grid of trenches is used for a maximum reduction of interconnect and inter-device capacitances. The oscillator starts at a tail current of 9 μA, indicating a resonator tank Q of 42 or better ($L = 0.7$ nH, $C = 300$ fF). By varying the tail current from 15 μA to 3.7 mA, the oscillation frequency can be tuned from 8.3 to 7.6 GHz. At the time of design, unfortunately only a rough estimate of device parameters for both active and passive devices was available.
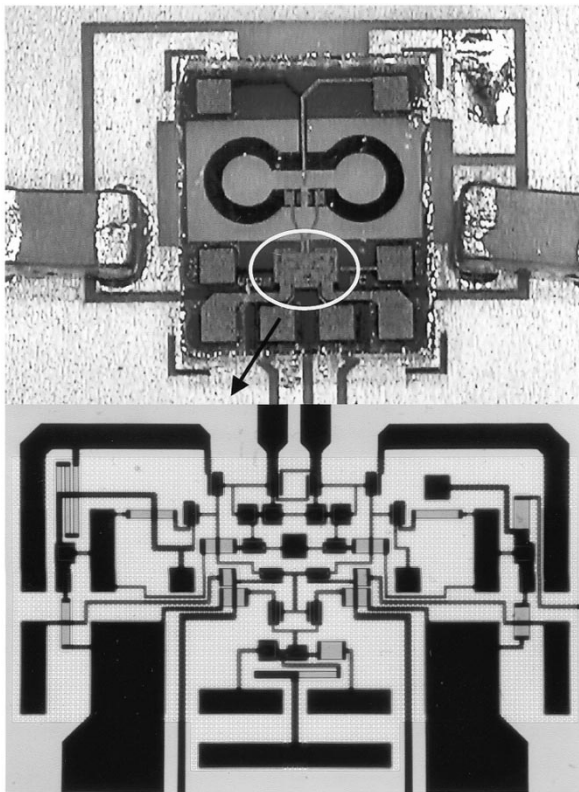
Fig. 14. VCO demonstrator circuit fabricated in the surface-mounted RF IC technology and soldered to a test substrate. The bottom picture shows a detail of the active circuit with backside illumination. The active devices are embedded in a grid of trenches to reduce interconnect and inter device capacitances.

Therefore, a robust and simple active oscillator core was designed, with a high open-loop gain to assure reliable start-up in case the actual Q would be significantly below first-order estimations. With a realized Q of about 42, the oscillator design enters the voltage-limited region for bias currents beyond 15 μA, which results in a phase-noise degradation compared to the maximum value of 100 dBc/Hz at a 1-MHz offset frequency. In a redesign with ac coupling or tapping of the tank, an improvement of more than 20 dB can be achieved. However, by normalizing for power consumption (P_{dc}), offset frequency (f_m), and oscillation frequency (f_{osc}) [30], we find $CNR_{norm} = CNR_{meas} - 20 \log(f_m/f_{osc}) - 10 \log(P_{dc}/1 \text{ mW})$ equal to 188 dBc/Hz. This value compares favorably with other reported values (173.4 dBc/Hz [31]) and (182.7 dBc/Hz [32]).

One of the most exciting applications of this technology is depicted in Fig. 15. It is a design for a fully integrated 1.8-GHz, 2-W PA including 50-Ω input and output match currently being investigated. Going from left to right, the input match, driver transistor, interstage match, output transistor, and output match are visible. The top and bottom regions contain ground vias, large decoupling capacitors, and bias circuits. At this moment, the complete PA does not yield any reasonable performance, presumably through mismatches in the interstage match circuit. The crucial output match, however, has been tested in a back-to-back configuration (see the inset of Fig. 16). Three variations were included on the testmask: 1) with the silicon film intact inderneath the inductor; 2) silicon completely removed; and 3) a fine grid of trenches underneath the inductor (width
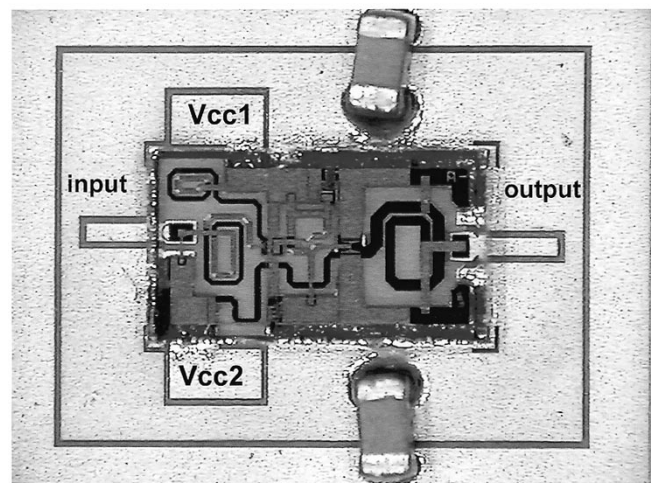

Fig. 15. Design study of a fully integrated 2-W, 3-V PA including input and output match circuits.
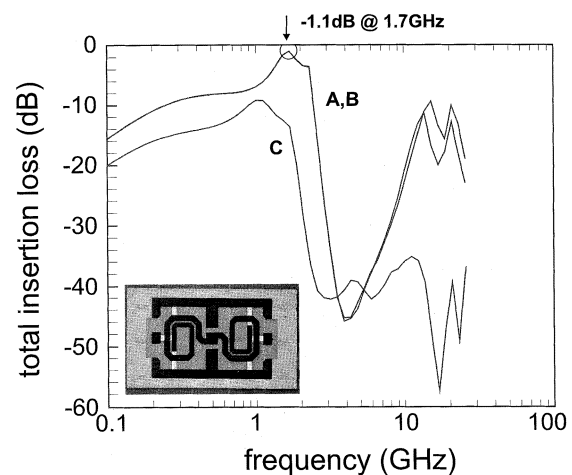

Fig. 16. Measured insertion loss versus frequency for the output match in a back-to-back configuration (inset, $3100 \times 1850 \ \mu\text{m}^2$). Three versions are fabricated. (A) Silicon completely removed underneath the inductor. (B) Silicon divided into a grid of isolated islands ($3.25 \times 3.25 \ \mu\text{m}^2$). (C) Silicon film intact.

1 μm and pitch 3.25 μm). The measured insertion loss versus frequency (Fig. 16) shows that the match is lightly out of band (1.7 GHz instead of 1.8 GHz). The insertion loss for the variant with the silicon film intact is obviously high. Surprisingly, the insertion loss for the other two variants is nearly identical and measured to be less than 0.5 dB. This value compares favorably to values achieved in much larger thick/thin film or laminate solutions.

V. CONCLUSION

For all semiconductor technologies (silicon, GaAs, InP), it usually holds that the actual devices are confined within the top few micrometers or so of the wafer, while the remaining part of the substrate only serves as a carrier. Frequently the substrate material, although it may yield excellent active devices, has properties that do not make it an obvious choice as a circuit carrier. Especially for RF applications, the substrate in many cases degrades the performance of the individual active devices

and the circuit as a whole. In the case of silicon, capacitive coupling to the resistive substrate causes a dissipation of RF energy resulting in poor passive components and cross talk. In (semi insulating) GaAs or InP, on the other hand, this is not an issue. Now it is the high thermal resistance that is troubling the integration of circuits with a high power density.

In this paper we presented a substrate transfer technology that involves the transfer of a thin layer from a fully processed wafer to a new substrate with properties better suited to the application, e.g., glass. This is done by gluing the processed wafer, top down, to the new substrate followed by removal of the original substrate. We have demonstrated the versatility of this substrate transfer process with four RF applications. Looking beyond the field of RF applications, one can foresee the advantage of substrate transfer for many other application, e.g., the possibility to use transparent substrates for optical applications, the use of substrates with a high dielectric permittivity or magnetic permeability, or the possibility to transfer circuits to flexible substrates.

The availability of fully automated 6- and 8-in gluing equipment and the licensing of process know-how and IP has reduced a seemingly exotic process step like STT to a powerful and viable new process module. STT will undoubtedly trigger many new and imaginative process ideas adding to the ever-expanding application area of silicon.

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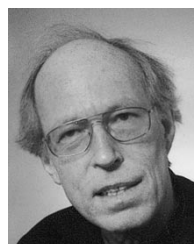
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