# Low temperature inorganic chemical vapor deposition of Ti-Si-N diffusion barrier liners for gigascale copper interconnect applications

RAPID COMMUNICATIONS

*This section is reserved for short submissions which contain important new results and are intended for accelerated publication.*

# Low temperature inorganic chemical vapor deposition of Ti–Si–N diffusion barrier liners for gigascale copper interconnect applications

Eric Eisenbraun,[a] Allan Upham, Raj Dash, Wanxue Zeng, Johann Hoefnagels, Sarah Lane, Dalaver Anjum, Katharine Dovidenko, and Alain Kaloyeros
*The New York State Center for Advanced Thin Film Technology and Department of Physics, The University at Albany–SUNY, Albany, New York 12203*

Barry Arkles
*Gelest Incorporated, Tullytown, Pennsylvania 19007*

John J. Sullivan
*MKS Instruments, Incorporated, Andover, Massachusetts 01810*

(Received 28 February 2000; accepted 26 May 2000)

A new low temperature inorganic thermal chemical vapor deposition process has been developed for the growth of titanium–silicon–nitride (Ti–Si–N) liners for diffusion barrier applications in ultralarge scale integration copper interconnect schemes. This process employs the thermal reaction of tetraiodotitanium ($TiI_4$), tetraiodosilane ($SiI_4$), and ammonia ($NH_3$) as, respectively, the individual Ti, Si, and N sources. Ti–Si–N films were successfully grown over a broad range of deposition conditions, including wafer temperature, process pressure, and $TiI_4$, $SiI_4$, and $NH_3$ flows ranging, respectively, from 350 to 430 °C, 0.1–1 Torr, and 2.5–8.0, 2.5–12.5, and 100–250 sccm. Film stoichiometry was tightly tailored through independent control of the Ti, Si, and N source flows. Film properties were characterized by x-ray photoelectron spectroscopy, Rutherford backscattering spectrometry, transmission electron microscopy, scanning electron microscopy, x-ray diffraction, and four-point resistivity probe. Resulting findings indicated that the texture and resistivity of the Ti–Si–N system were dependent on composition. In particular, films with a $Ti_{33}Si_{15}N_{51}$ stoichiometry exhibited a nanocrystalline TiN phase within an amorphous SiN matrix, highly dense morphology, resistivity of $\sim 800\ \mu\Omega$ cm for 25 nm thick films, and step coverage of $\sim 50\%$ in 130 nm wide, 10:1 aspect ratio trenches. Oxygen and iodine contaminant levels were below, respectively, 3 and 1.4 at. % each. Preliminary copper diffusion-barrier studies indicated that barrier failure for 25 nm thick $Ti_{34}Si_{23}N_{43}$ films did not occur until after annealing for 30 min at 700 °C. © *2000 American Vacuum Society.* [S0734-211X(00)07904-X]

Copper based interconnects have almost universally replaced aluminum in high-performance integrated circuitry applications. This transition was driven by copper's lower resistivity and improved electromigration resistance, which allow faster signal propagation speed and higher performance characteristics. However, the successful incorporation of copper into subquarter-micron device generations requires effective chemical, structural, mechanical, and electrical compatibility with the surrounding low dielectric constant insulators. Most of the resulting target specifications could be achieved through the identification of appropriate liners that prevent copper diffusion into the dielectric, and promote viable copper-dielectric interlayer adhesion.[1]

The need for a diffusion barrier and adhesion promoter is further mandated by the high diffusivity of Cu into silicon and its poor adhesion to silicon dioxide and low dielectric constant materials. The presence of copper in silicon results in the formation of deep level traps that cause device degradation and failure. Liner materials are also required to be thermodynamically stable with respect to the copper and dielectric layers, and preferably exhibit an amorphous structure to eliminate the high diffusion pathways typically provided by grain boundaries. More important, they must sustain their desirable properties at extremely reduced thicknesses to ensure that most of the effective volume of the trench and via structures is occupied by the actual copper conductor.[1]

In this respect, ternary refractory metal liners such as the titanium–silicon–nitrogen (Ti–Si–N), tantalum–silicon–nitrogen (Ta–Si–N), and tungsten–boron–nitrogen (W–B–N) systems could act as viable diffusion barriers in copper metallization due to their favorable chemical, structural, and thermal properties. In particular, the Ti–Si–N phase represents a highly desirable option due to the fact that Ti-based liners have already gained wide acceptance in semiconductor fabrication flows. In addition, the availability of Ti–Si–N in amorphous form provides an added incentive, in view of the

[a]Author to whom correspondence should be addressed; electronic mail: ee@cnsvax.albany.edu

TABLE I. Range of CVD TiSiN processing conditions investigated in this work.

| Parameter | Processing range investigated |
|---|---|
| Temperature | 350–430 °C |
| Pressure | 0.1–1 Torr |
| $NH_3$ flow | 100–250 sccm |
| $H_2$ flow | 100 sccm |
| $TiI_4$ vapor flow | 2.5–6 sccm |
| $SiI_4$ vapor flow | 0–12.5 sccm |

TABLE III. Optimized CVD TiSiN key processing parameters.

| Parameter | First-pass optimized process settings |
|---|---|
| Temperature | 430 °C |
| Pressure | 0.6 Torr |
| $NH_3$ flow | 250 sccm |
| $H_2$ flow | 100 sccm |
| $TiI_4$ vapor flow | 6 sccm |
| $SiI_4$ vapor flow | 10 sccm |

absence of grain boundaries that tend to act as fast diffusion paths for copper migration. In this respect, the amorphous Ti–Si–N phase has been shown to be stable against crystallization at temperatures as high as 1000 °C, with the latter being strongly dependent on film stoichiometry.[2] As a result, various research groups have investigated the formation of Ti–Si–N films by a variety of physical vapor deposition (PVD) and metalorganic chemical vapor deposition (MOCVD) techniques, and documented their resulting performance as copper diffusion barriers.

In the PVD case, most of the diffusion barrier studies employed liners with thicknesses larger than 100 nm, which made the resulting conclusions less applicable to subquarter-micron device structures.[3–5] The MOCVD route, on the other hand, exploited the reaction of tetrakis diethylamido titanium (TDEAT), silane ($SiH_4$), and $NH_3$ to deposit Ti–Si–N films over the temperature range from 300 to 450 °C.[6] Barrier thermal stress (BTS) testing was subsequently performed on 10 nm thick $Ti_{23}Si_{14}N_{45}O_3C_3H_{12}$ samples that were MOCVD grown at 400 °C. The samples were shown to possess a mean time to failure (MTTF) approximately 10–100 times that of PVD TiN.[7] More recently, metalorganic atomic layer deposition (MOALD) was employed to deposit conformal Ti–Si–N layers at low substrate temperatures (180 °C). However, no information was available with regard to film purity, resistivity, or barrier properties.[8]

The work presented herein has focused on the development of a low temperature thermal CVD process that employs the thermal reaction of tetraiodotitanium ($TiI_4$), tetraiodosilane ($SiI_4$), and ammonia ($NH_3$) as, respectively, the individual Ti, Si, and N sources. These source precursors are attractive because of their chemical simplicity, low dissociation energy, and reduced decomposition temperature as compared with other inorganic chemistries (such as $TiCl_4$). Additionally, $SiI_4$ was selected over $SiH_4$ in order to prevent the possible incorporation of hydrogen into the film as a result of incomplete decomposition of the $SiH_4$ molecule. The strategy espoused was to grow the Ti–Si–N phase *in situ* through the simultaneous reaction of appropriate mixtures of the Ti, Si, and N sources in the presence of hydrogen. Film stoichiometry was tightly tailored through independent control of the $TiI_4$, $SiI_4$, and $NH_3$ gaseous flows, with the reaction proceeding schematically as follows:

$$TiI_4 + SiI_4 + NH_3 + H_2 \rightarrow Ti_mSi_nN_p + NH_qI_r + HI.$$

Hydrogen was employed to ensure complete passivation and elimination of any free iodide reaction by-products from the reaction zone.

All Ti–SiN films were deposited in a customized, stainless steel, 200 mm wafer capable, warm-wall CVD system equipped with a high vacuum loadlock for wafer transport and handling without exposing the deposition chamber to air. This approach allowed tight control over the process stability and reproducibility. The chamber was also equipped with a parallel-plate-type, radio-frequency (rf) plasma capability for *in situ* wafer plasma cleaning. A Roots blower stack was used for process pumping. The $TiI_4$ and $SiI_4$ source precursors, which are solid at room temperature, were delivered to

TABLE II. Selected film properties.

| Property | Value |
|---|---|
| Optimized composition (RBS, XPS) | $Ti_{33}Si_{15}N_{51}$ |
| Iodine incorporation (XPS) | ~1.4 at. % |
| Oxygen incorporation (XPS) | Typical XPS background levels |
| Texture (XRD, TEM) | Nanocrystalline TiN phase within an amorphous $SiN_x$ matrix |
| Resistivity (25 nm thick film) | ~800 $\mu\Omega$ cm |
| Conformality (130 nm wide, 10:1 aspect ratio trenches) | 50% |

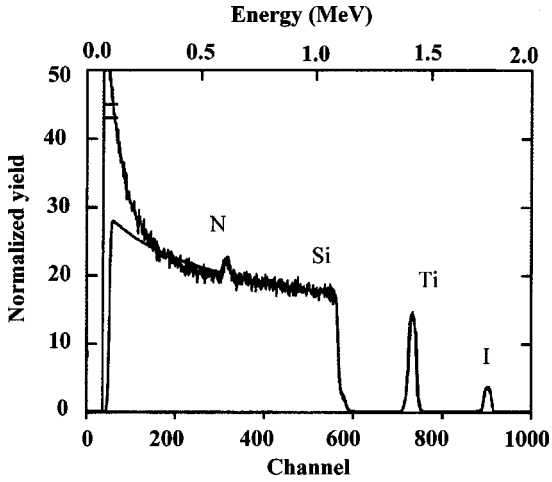


FIG. 1. Typical RBS plot of as-deposited CVD Ti–Si–N film.

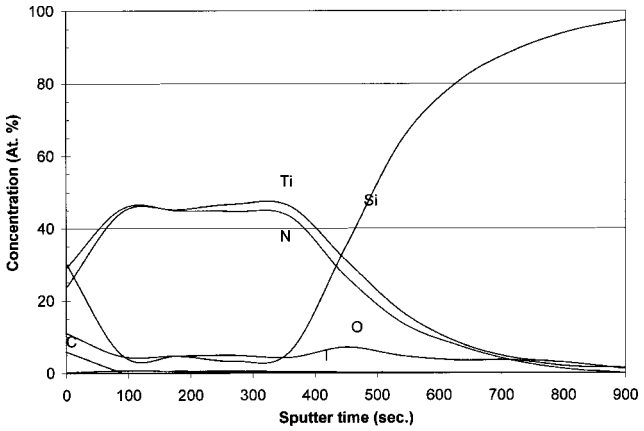


FIG. 2. XPS depth profile of as-deposited CVD $Ti_{36}Si_{12}N_{52}$ film.

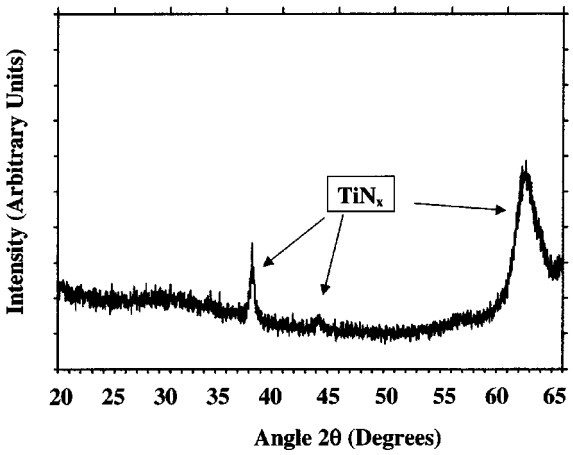


FIG. 3. XRD scan of an as-deposited, 25 nm thick, CVD $Ti_{36}Si_{12}N_{52}$ film.

the reaction chamber using individual MKS model 1153A vapor source delivery systems. Sufficient vapor pressure for delivery to the chamber was achieved by heating each source to ~160 °C, with the delivery systems and transport lines being kept at ~180 °C to prevent precursor recondensation. This delivery approach did not require carrier gas, and allowed repeatable and controllable control over reactant flows to the process chamber.

$NH_3$ and hydrogen ($H_2$) were used as coreactants. Undesirable gas phase reactions were eliminated through the use of a ''no-mix'' showerhead architecture, where the ammonia line was isolated from all other reactants until introduction into the reaction zone. For all depositions, three types of substrates were employed. Si(100) wafers were employed for thermal diffusion barrier testing, while 500 nm thick thermally grown $SiO_2$ on Si was applied for composition, resistivity, and texture measurements, and patterned oxide structures were used for assessment of film conformality. Table I summarizes pertinent deposition parameters and corresponding ranges explored in this work.

The composition, microstructure, surface morphology, conformality, and electrical properties of the CVD Ti–Si–N films were analyzed by x-ray photoelectron spectroscopy (XPS), Rutherford backscattering spectrometry (RBS), x-ray diffraction (XRD), transmission electron microscopy (TEM), and four-point resistivity probe. Relevant information regarding these characterization techniques is given elsewhere.[9] In this respect, selected film properties are summarized in Table II, and the corresponding optimized processing conditions are listed in Table III.

Additionally, a preliminary evaluation was carried out of

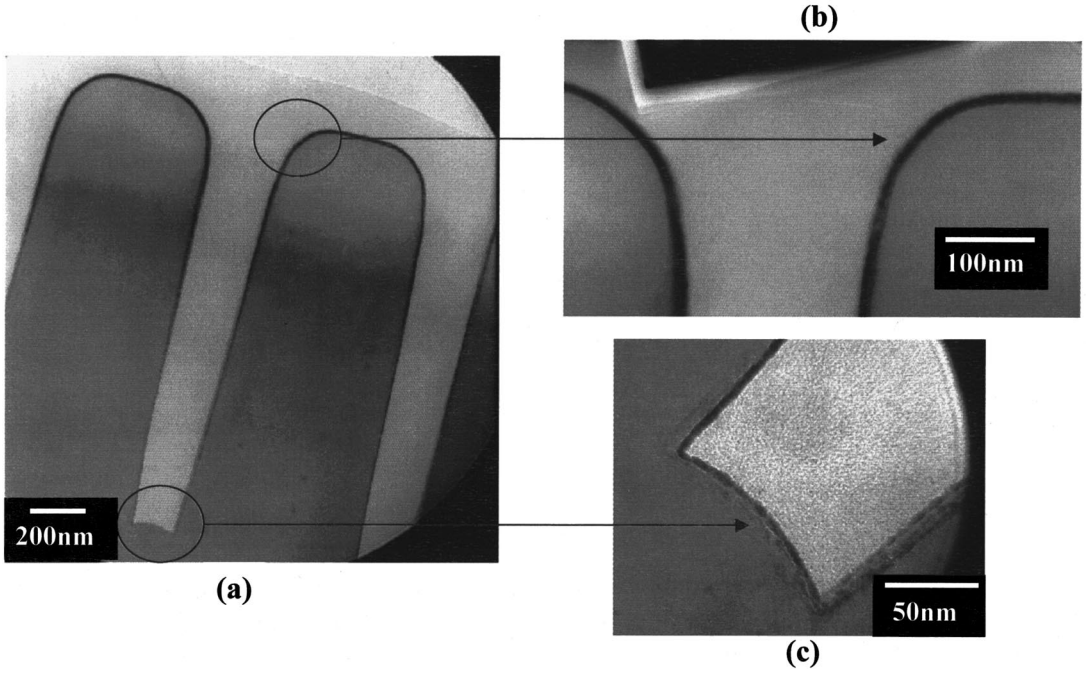


FIG. 4. TEM imaging studies of as-deposited, 10 nm thick, CVD Ti–Si–N film show (a) 50% step coverage in a nominally 130 nm wide, 10:1 aspect ratio, trench structure, (b) no loafing at the top corners of the structure, and (c) no thinning at the bottom corners of the trench structure.

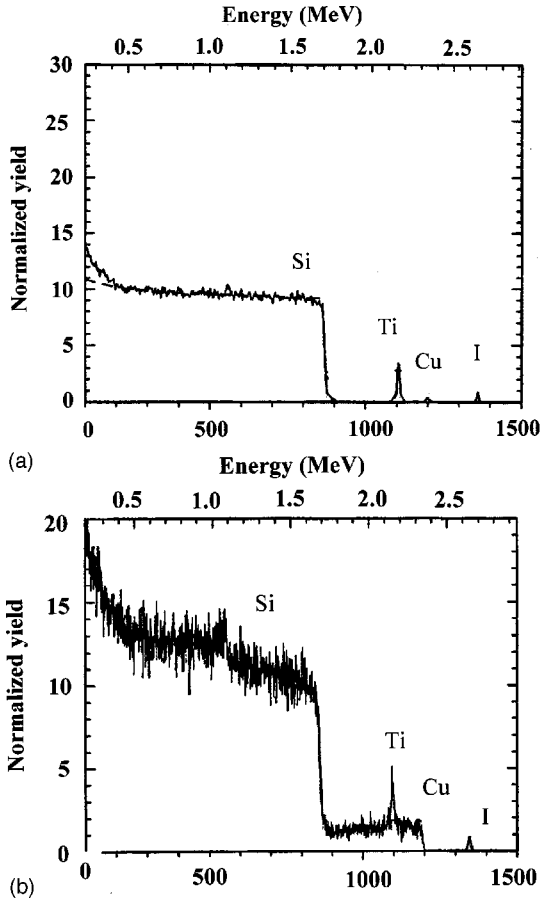


FIG. 5. Typical RBS spectra of sputtered Cu/CVD $Ti_{36}Si_{12}N_{52}$/Si stacks films after annealing at (a) 600 and (b) 700 °C. The data were collected after removal of the top copper layer.

the performance of the CVD Ti–Si–N as a diffusion barrier in copper metallization. For this, 100 nm thick Cu films were *ex situ* sputter deposited onto 25 nm thick CVD $Ti_{33}Si_{15}N_{51}$ films grown on Si. The resulting stacks were annealed in 1 atm argon at 450, 515, 600, and 700 °C for 30 min, along with sputter-deposited Cu/CVD TiN/Si stacks of identical thickness. The latter provided a comparative assessment of barrier performance. After annealing, the copper was stripped off in a diluted nitric acid solution, and the resulting samples were then analyzed by RBS to detect the presence of Cu, either in the liner material or in the underlying Si substrate.

Figure 1 presents a typical RBS spectrum of an 82 nm thick CVD Ti–Si–N film deposited on Si at a wafer temperature of 430 °C. RBS analysis indicated that the films were free of any heavy elemental contaminants, with the exception of ~1.4 at. % I. In this respect, higher $NH_3$ and $SiI_4$ flows at constant $TiI_4$ flow yielded, respectively, increased nitrogen and silicon incorporation into the resulting Ti–Si–N phase. For illustration purposes, Fig. 2 displays the XPS depth profile for the same type sample as that shown in Fig. 1. The XPS depth profile yielded a film composition of $Ti_{33}Si_{15}N_{51}$, and indicated the presence of oxygen levels of ~3 at. %, which was within the typical background levels of the XPS system.

Figure 3 presents a typical XRD spectrum of a 25 nm thick CVD TiSiN film grown on $SiO_2$. The only XRD peaks detected were ascribed to $TiN_x$ phases. It is believed that this finding indicates that film microstructure consisted of a nanocrystalline TiN phase within an amorphous SiN matrix, in agreement with prior results in the literature on sputter-deposited Ti–Si–N films.[10] It was suggested that this Ti–Si–N microstructure is desirable from a diffusion barrier performance perspective, especially in view of the absence of grain boundaries.[11] The latter tend to act as fast diffusion paths for copper migration.

TEM was used to determine the film conformality in aggressive device structures. In this respect, Fig. 4(a) exhibits the bright field TEM micrograph of 10 nm thick CVD-grown Ti–Si–N in a nominally 130 nm wide, 10:1 aspect ratio, trench structure. In addition, Figs. 4(b) and 4(c) display higher magnification TEM images of film profiles at, respectively, the top and bottom of the trench structure. TEM analysis yielded a film conformality of ~50%, and indicated the absence of thinning or loafing effects at the top and bottom corners of the trench structure. TEM imaging also confirmed the XRD results with respect to the existence of a nanocrystalline structural phase.

In terms of diffusion barrier performance, RBS results indicated the absence of any diffused copper in the CVD Ti–Si–N liner or underlying Si substrates after annealing at 600 °C, as shown in Fig. 5(a). In contrast, RBS detected the onset of copper diffusion for the same film after annealing at 700 °C, as shown in Fig. 5(b).

In summary, a new low temperature inorganic CVD Ti–Si–N process has been developed for applications as a diffusion barrier in copper metallization schemes. This process employs the thermal reaction of $TiI_4$, $SiI_4$, and $NH_3$ as, respectively, the individual Ti, Si, and N sources. Ti–Si–N films were successfully grown over a broad range of deposition conditions, including wafer temperature, process pressure, and $TiI_4$, $SiI_4$, and $NH_3$ flows ranging, respectively, from 350 to 430 °C, 0.1–1 Torr, and 2.5–8.0, 2.5–12.5, and 100–250 sccm. In particular, films with a $Ti_{33}Si_{15}N_{51}$ stoichiometry exhibited a nanocrystalline TiN phase within an amorphous SiN matrix, highly dense morphology, resistivity of ~800 $\mu\Omega$ cm for 25 nm thick films, and step coverage ~50% in 130 nm wide, 10:1 aspect ratio trenches. The oxygen and iodine contaminant levels were below, respectively, 3 and 1.4 at. % each. Preliminary copper diffusion-barrier studies indicated that barrier failure for 25 nm thick $Ti_{33}Si_{15}N_{51}$ films did not occur until after annealing for 30 min at 700 °C. Additional studies are presently underway to further optimize the film conformality through modeling of film profiles in aggressive device topographies using fast simulators and to fully document corresponding diffusion-barrier characteristics by employing barrier thermal stress measurements.

The work presented herein was supported in part by SEMATECH under Contract No. MLMA006, by MKS Instruments, and by the New York State Center for Advanced Thin Film Technology. This support is gratefully acknowledged.

[1]*The International Technology Roadmap for Semiconductors*, 1999 ed. (Semiconductor Industry Association, San Jose, CA, 1999), p. 165.
[2]X. Sun, J. Reid, E. Kolawa, and M. Nicolet, J. Appl. Phys. **81**, 656 (1997).
[3]J. Reid, E. Kolawa, R. Ruiz, and M. Nicolet, Thin Solid Films **236**, 319 (1993).
[4]P. Pokela, E. Kolawa, M. Nicolet, and R. Ruiz, J. Electrochem. Soc. **138**, 2125 (1991).
[5]J. Reid, E. Kolawa, C. Garland, M. Nicolet, F. Cardone, D. Gupta, and R. Ruiz, J. Appl. Phys. **79**, 1109 (1996).
[6]J. Custer, P. Smith, R. Jones, A. Maverick, D. Roberts, J. Norman, and A. Hochberg, *Advanced Metallization and Interconnect Systems for ULSI Applications in 1995* (Materials Research Society, Pittsburgh, PA, 1996), p. 343.
[7]P. Smith *et al.*, in Ref. 6, p. 249.
[8]J. Min, H. Park, and S. Kang, Appl. Phys. Lett. **75**, 1521 (1999).
[9]See, for example, J. Kelsey, C. Goldberg, G. Nuesca, G. Peterson, A. Kaloyeros, and B. Arkles, J. Vac. Sci. Technol. B **17**, 1101 (1999).
[10]X. Sun, E. Kolawa, S. Im, C. Garland, and M. Nicolet, Appl. Phys. A: Mater. Sci. Process. **65**, 43 (1997).
[11]X. Sun, J. Reid, E. Kolawa, M. Nicolet, and R. Ruiz, J. Appl. Phys. **81**, 664 (1997).