Sigma-Delta Modulators Operating at a Limit Cycle

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Sotir Ouzounov, Hans Hegt, and Arthur van Roermund

***Abstract*—A new type of sigma–delta modulator that operates in a special mode named limit-cycle mode (LCM) is proposed. In this mode, most of the SDM building blocks operate at a frequency that is an integer fraction of the applied sampling frequency. That brings several very attractive advantages: a reduction of the required power consumption per converted bandwidth, an immunity to excessive loop delays and to digital–analog converter waveform asymmetry and a higher tolerance to clock imperfections. The LCMs are studied via a graphical application of the describing function theory. A second-order continuous time SDM with 5 MHz conversion bandwidth, 1 GHz sampling frequency and 125 MHz limit-cycle frequency is used as a test case for the evaluation of the performance of the proposed type of modulators. High level and transistor simulations are presented and compared with the traditional SDM designs.**

***Index Terms*—Describing function (DF), limit cycles, sigma–delta modulation.**

I. Introduction

ONE of the unsolved problems in sigma–delta modulator's operation is the appearance of periodic modes that can lead to generation of spurious tones and unpredicted deterioration of the signal-to-noise-and-distortion ratio (SNDR) [1]. The existence of those periodic modes (generally defined as limit cycles) is due to the nonlinear nature of sigma–delta modulators. That is why, for the understanding and the description of those periodic modes, a "nonlinear look" at sigma–delta modulator operation is required. In the 1950's and 1960's, major developments in the treatment of closed-loop nonlinear systems were made in the context of automated control [2]–[4]. Those works led to a generalized approach for the treatment of nonlinear systems: the describing function (DF) representation of the nonlinear element [5]. So far, in the context of sigma–delta modulator, those theories have received little attention. In this work, the DF theory is used for the modeling of the quantizer function and the investigation of limit-cycles modes in SDMs.

The paper is structured as follows. Firstly, the LCMs in *asynchronous sigma–delta modulators* (ASDM) are discussed. A graphical determination of the limit cycles is demonstrated in the gain-phase plane. Secondly, the LCMs in *synchronous sigma–delta modulators* (SDMs) are studied (**here, the abbreviation SDM is used only for synchronous sigma–delta modulators**). Again, a graphical evaluation of the limit cycle's behavior is made. In Section IV, an SDM operating in an LCM is introduced. Its properties are illustrated with high level and transistor simulations. Finally, a comparison with the standard SDM design is made and the benefits of the new mode of operation are discussed.

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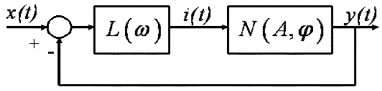

Fig. 1. ASDM.

II. Asynchronous Sigma–Delta Modulator

There are several reasons to start the study of limit-cycle behavior with a closer look at ASDM.

- ASDM [6], [7] can have a very similar structure to that of a typical continuous-time SDM. It is a closed-loop system (Fig. 1) built with a continuous-time linear filtering block $L(j\omega)$ and a quantizer with DF $N(A, \varphi)$.
- The ASDM transforms the information in the amplitude of their input signal into time information in a binary output signal, without an external sampling signal. The amplitude-time transformation in the ASDM is done using an inherent periodic self-oscillation: a limit cycle. The limit-cycle frequency ω_c can be regarded as counterpart of the clock frequency in SDM and is defined [8] as the main ASDM design parameter that determines the spectral properties of the output signal and the quality of the amplitude-time transformation.

Here, for the evaluation of the limit-cycle properties of the ASDM, a graphical application of the DF theory is used. For consistency, the amplitude A of the limit cycle is defined and observed at a fixed position in the system, for example, for the signal $i(t)$ in front of the nonlinear element. The observation point is concluded from the fact that this is the point from the signal propagation path that exhibits continuous variations in amplitude with respect to the system parameters and the input signal $x(t)$.

As an example, an ASDM built with a second-order low-pass filter and a binary quantizer with hysteresis is studied. The filter is described with the following expression:

$$L(j\omega) = \frac{(j\omega + \omega_z)\omega_{p1}\omega_{p2}}{(j\omega + \omega_{p1})(j\omega + \omega_{p2})\omega_z}. \tag{1}$$

The dc gain in (1) is normalized to 1 and for the second-order system two different poles and a zero are introduced.

Due to the hysteresis, the nonlinear function performed by this quantizer is dependent on both the sign and the phase of the input signal. At system level, the hysteresis is giving an additional degree of freedom for modification of the loop behavior. Furthermore, most asynchronous quantizers use regenerative circuitry (with a positive feedback) in order to achieve

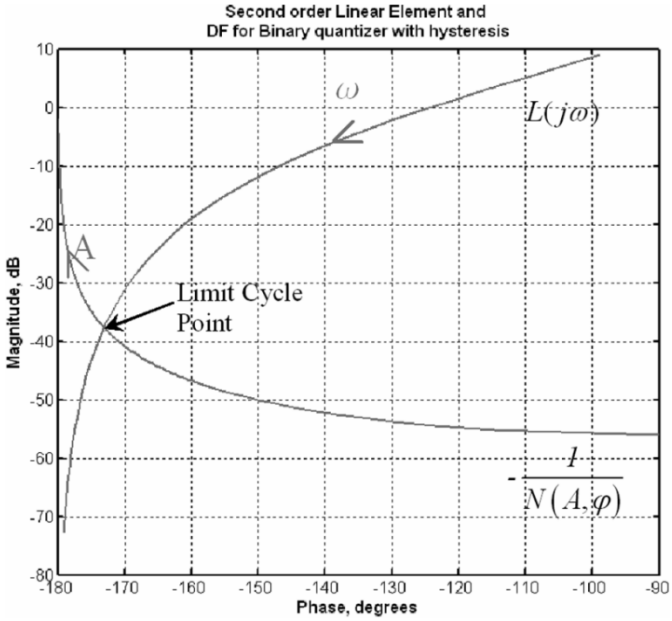

Fig. 2. Graphical determination of a limit cycle in ASDM.

high speeds. Such an implementation may have a hysteresis that has to be taken into account at system level.

A. DF Approach

The DF builds a linear approximation of the nonlinear element according to a certain linearization rule and with respect to preliminary defined input signals, for example sinusoids. The linearization rule implements a criterion for the evaluation of the approximation. The most common criterion used in practice is the minimum mean square difference between the approximated output and the actual output of the nonlinear element. The DF is derived under the assumption that there is a single harmonic component (pure sine) in front of the nonlinear element. That generally requires high-order filtering by $L(j\omega)$. However, for the following qualitative evaluations, a small inaccuracy of the DF result is of little consequence. The DF for a binary quantizer with hysteresis h and a sine input signal with amplitude A is given by [5]

$$N(A,\varphi)=\frac{4}{\pi A}\sqrt{1-\left(\frac{h}{A}\right)^2}-j\frac{4h}{\pi A^2}=\frac{4}{\pi A}e^{-j\sin^{-1}\left(\frac{h}{A}\right)}. \tag{2}$$

The quantizer output levels are normalized to $+/-1$ and φ accounts for the phase rotation of the complex function (2). Limit-cycle oscillations occur for set of A, φ and ω for which

$$L(j\omega)=-\frac{1}{N(A,\varphi)}. \tag{3}$$

This equation can be interpreted in analogy to the Barkhausen criterion. Namely, that a closed-loop system is prone to self-oscillation at a frequency for which an integer multiple of 360° of phase shift occurs and the gain is 1.

B. Graphical Prediction of Limit-Cycle Oscillations (ASDM)

After deriving the magnitude and the phase of (1), the solution of (3) is found graphically. A gain-phase plot (Fig. 2), parameterized with respect to frequency for $L(j\omega)$ and to amplitude A for $N(A,\varphi)$ is used. The solution of (3) is given by the crossing point of the linear and the nonlinear transfer characteristics, as indicated on the picture. For the chosen test case only one limit cycle is possible. The limit-cycle frequency can be altered via modifications of $L(j\omega)$ and/or the nonlinearity. For example, via changing the zero position in $L(j\omega)$ or via modification of the hysteresis value. If the initial values of A and ω_c are different from those determined from the crossing point, the loop mechanism would adjust them so that the limit-cycle point is reached. In the described case, the DF is giving a very good prediction for the existence, frequency and amplitude of the limit cycle.

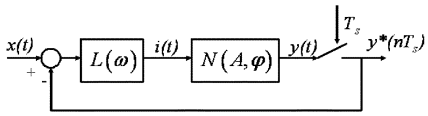

Fig. 3. SDM.

III. Limit Cycles in SDM

In this section, a clocked SDM is studied. The same $L(j\omega)$ and $N(A,\varphi)$ are used, with a sampling operation embedded within the loop, as shown in Fig. 3. The interaction between the sampling clock with frequency ω_s and the limit cycle as established in the previous section for the ASDM is investigated. In the general SDM treatment, the sampling operation is performed before or within the quantizer. Moreover, in practically all reported SDM implementations, the quantizer is an internally sampled circuit. The ideal quantizer is memoryless and its position with respect to the sampling operation is of no consequence for the loop operation. Here, to decouple the amplitude quantization from the sampling, the sampling is performed after the quantizer. This choice is interesting also from an implementation point of view, because in such a case, the sampling acts on a well-defined two-level signal. In this way, a possible metastability in the sampling can be significantly decreased because the time duration of the weak signal provided to the sampling switch is minimized. The sampling delay, the switching and the propagation times in the quantizer and the sampling switch are incorporated in the limit-cycle mechanism.

A. Graphical Prediction of Limit-Cycle Oscillations (SDM)

In a fully symmetric and unbiased system containing an integrator, only limit-cycle oscillations that are even integer multiples N of the sampling period T_s are possible ($N=2k+2,\ and\ k=0,1,2\ldots$) [9]. This follows from the fact that for zero input, the average value of the output should also be zero. This is only possible if the output consists of N ones followed by N zeros. The LCMs in an SDM can be established if the sampling operation is treated as a process that introduces phase delay in the loop. That results in a phase shift that is dependent on the clock frequency ω_s and can have any value in the range $(0-2p/N)$. In Fig. 4, the delay for each ω_s/N frequency is shown as a line originating from the discrete points $L(j\omega_s/N)$ and with length equal to $2p/N$. The frequencies for which the sampling operation can add enough delay into the loop (the sampling delay crosses $1/N(A,\varphi)$), correspond to LCMs. For our test case, two LCMs are possible with frequencies $\omega_s/2$ and

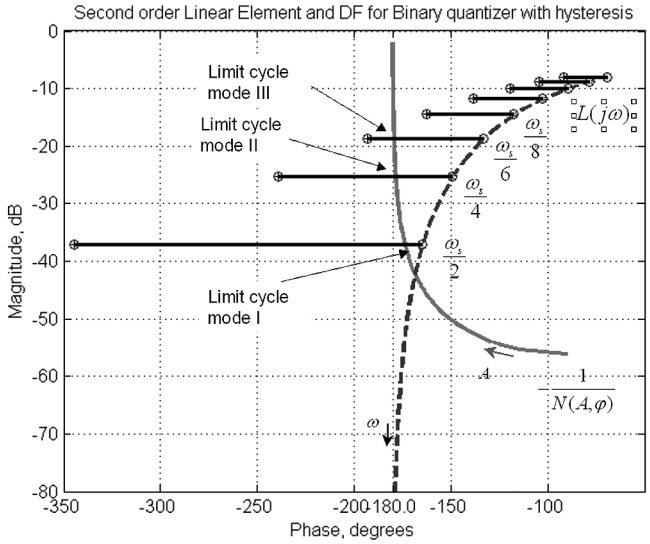

Fig. 4. Graphical determination of a limit cycle in SDM.

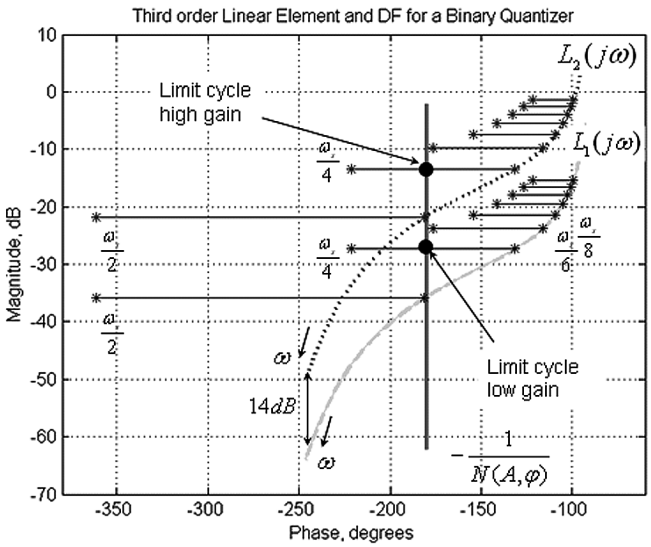

Fig. 5. Impact of the gain on the limit-cycle properties.

$\omega_s/4$. Limit cycles with lower frequency are not possible because the total phase delay in the loop does not provide 360° phase shift. The first limit cycle with frequency $\omega_s/2$ is the only mode used in practice for the design of SDMs. However, the second LCM that corresponds to $\omega_s/4$ should also be taken into account.

The DF approach can be easily applied for the study of arbitrary filter functions and the most common quantizers. In Fig. 5, an example is given for two third-order integrators and an ideal binary quantizer. The integrators' transfer characteristics $L_1(j\omega)$ and $L_2(j\omega)$ have a gain difference of 14 dB. The DF $N(A) = 4/\pi A$ for such a quantizer is dependent only on the sign of the driving signal and is a real function of the amplitude A, thus it is a straight line on the gain-phase plot. From Fig. 5, it can be concluded that if the clock speed is increased beyond a certain value, the SDM is not capable of operation at maximum clock speed due to insufficient phase margin in the loop and in both cases enters a limit cycle with a frequency of $\omega_s/4$. An increase of the loop gain results in a higher amplitude of the limit cycle; however, its frequency remains the same, because the phase characteristic of the filter remains the same. The loop can be forced to operate at full clock speed with proper phase compensation of the linear part of the loop.

B. Impact of the Input Signal

The establishment of the limit-cycle parameters A and ω_c was discussed for ASDM and SDM operating in an idle mode (without input signal). When those systems are driven with an input signal (harmonic or dc) several important aspects have to be pointed out.

- The amplitude and the frequency of the limit cycle are modulated by the input signal. That leads to the appearance of spectral component positioned around the limit-cycle frequency [8] and with energy that depends on the amplitude of the input signal. In order to prevent the appearance of these components in the baseband, the limit-cycle frequency has to be much higher than the desired conversion bandwidth. In the SDM case, the sampling operation de-correlates the limit-cycle tones from the input signal and spreads them in frequency. The tones are not distinguishable from the noise floor even for high input levels under the condition that the limit-cycle frequency is high enough. A qualitative evaluation is given in the next section.
- The input signal levels add to the amplitude of $i(t)$. When more than one limit cycle is possible (Fig. 4), with the increase of the input signal, the system can jump to the limit cycle with lower frequency. For the system shown in Fig. 4, that happens when the amplitude levels of $i(t)$ exceed with 12 dB the idle limit-cycle amplitude. Thus, the input signal forces the loop to jump from LCMI to LCMII. This jump does not alter the dynamic range of the system and the modulator overloads for the same input level.

IV. SDM Operating at a Limit Cycle

From the discussion so far, it is clear that every SDM is prone to entering one or more LCMs. The possible modes need to be carefully investigated and taken into account in the transistor level design of the building blocks. The design of $L(j\omega)$ (especially for higher order transfer functions) should be done with considerations for the possible limit cycles for the chosen sampling frequency.

The most common approach used in practice is to aim always for maximum loop speed equal to $\omega_s/2$. That requires a significant gain bandwidth (GBW) from the linear part. The requirement is becoming much more stringent when clock speeds, at the edge of the technology, are desired. Achieving gain that is high enough for those clock speeds can be very expensive, if possible at all. Even when the technology allows operation at $\omega_s/2$ that would leave very little room for extra processing inside the loop because of the very high sensitivity to extra loop delays [10]. An alternative approach is possible. The SDM loop can be deliberately designed to operate in a limit cycle i.e., with an integer fraction of the clock frequency. For example, one of

TABLE I
COMPARISON: STANDARD SDM AND LIMIT-CYCLE SDM

	Clock Frequency	Limit Cycle Frequency	P_N, dB penalty	Simulated $SNDR_{50\%,FS}$
Standard SDM 1	f_s	NA	reference	81.7dB
Standard SDM 2	$f_s/2$	NA	+15dB	66.5dB
Standard SDM 3	$f_s/4$	NA	+30dB	51.7dB
LCSDM 1	f_s	$f_c=f_s/4$	+9dB	72.5dB
LCSDM 2	f_s	$f_c=f_s/8$	+18dB	63.7dB

the systems shown in Fig. 5 can be used. In this case, only the sampling switches operate at the full clock speed. The rest of the loop operates at the limit-cycle frequency, thus with a significantly lower average speed.

A. Calculation of the Baseband Quantization Noise Power

For acquiring more insight in the consequences of working at a limit cycle, the quantization noise power P_N within bandwidth B is evaluated

$$P_N = \int_0^B E(f)\frac{2}{|1+L(f)|^2}df \tag{4}$$

where $E(f)$, is the quantization noise spectrum. Firstly, the white noise model [11] for a binary quantizer with a quantization step of 2 is used: $E(f) = 1/(3f_s)$. For a second-order system, (4) is evaluated as

$$P_N \approx \frac{\pi^4}{15}\left(\frac{2B}{f_s}\right)^5. \tag{5}$$

From (5), it follows that P_N decreases with 15 dB for each doubling of f_s. Secondly, the quantization noise spectrum $E_{\rm LC}(f)$ that arises from the sampling of a square wave with frequency f_c (the limit-cycle frequency) with clock frequency f_s, is evaluated [12], [13] as

$$E_{\rm LC}(f) = \frac{8}{3}f_c T_s^2. \tag{6}$$

When we take into account that the loop operates at a fraction $N = f_s/f_c$ of the clock frequency, from (4), $P_{\rm NLC}$ is

$$P_{NCL} = \frac{8}{3}f_c T_s^2 \frac{\pi^4}{5f_c^4}(2B)^5 = \frac{8\pi^4}{15}N^3\left(\frac{2B}{f_s}\right)^5. \tag{7}$$

From (7), it can be concluded that when the SDM operates at a limit cycle, a penalty of 9 dB is introduced for each reduction by two of the loop frequency. In Table I, several SDMs operating with different sampling frequencies are shown. Standard SDM1 operates with the highest f_s and is used as a reference. The reduction of the performance due to a decrease of the sampling speed is illustrated. A comparison between SDM2 and limit-cycle SDM1 (LCSDM1) shows that when the two loops operate at the same frequency ($f_s/4$ in this case), LCSDM shows 6 dB better performance. The improvement is 12 dB for LCSDM2 with respect to SDM3. The results show that it is far more advantageous to force the SDM to function at a low limit-cycle frequency than just decrease the clock f_s.

In the last column of Table I, Matlab simulation results are given for the SNDR in each case. A second-order system with a baseband of 5 MHz and clock frequency of 1 GHz is simulated for an input signal at 1 MHz with amplitude of 50% (−6 dB) of full scale (FS). The output spectrum of LCSDM2 operating at limit-cycle frequency $\omega_c = \omega_s/8$ is shown in Fig. 6. There, the LCM of operation can be recognized from the spectral bump at the limit-cycle frequency. The simulation results confirm the theoretical expectations.

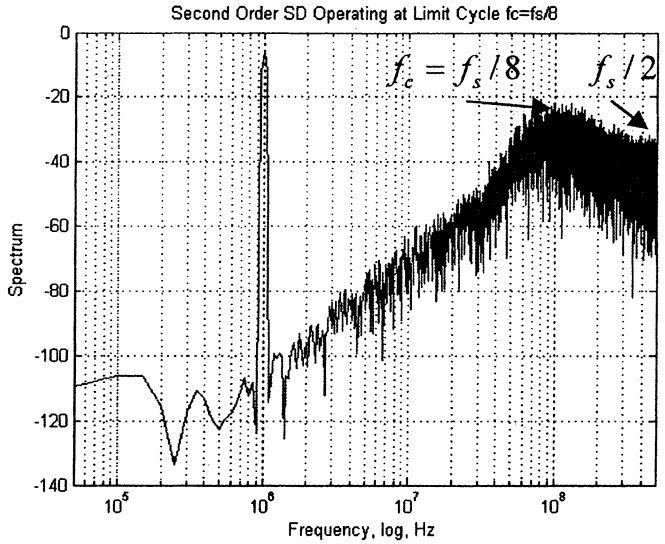

Fig. 6. SD operating on limit cycle with $\omega_c = \omega_s/8$.

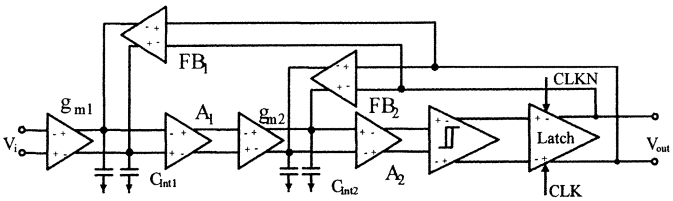

Fig. 7. Block diagram of a second-order LCSDM.

B. Block Diagram of the Hardware Implementation

A differential implementation of a second-order system is described with the block diagram shown in Fig. 7. The stages g_{m1} and g_{m2} are transconductors (voltage-to-current converters) that, together with the capacitances $C_{\rm int1}$ and $C_{\rm int2}$, implement continuous-time integrators. The blocks $\rm FB_1$ and $\rm FB_2$ represent the feedback transfer. In practice, they are implemented as switched-current sources that are controlled by the output signal. The blocks A_1 and A_2 are linear gain stages. Their purpose is to decrease the effective hysteresis value and reduce the design requirements for the quantizer with respect to speed and power consumption. A binary quantizer with hysteresis and a sampling latch complete the LCSDM loop.

The block diagram implements second-order LCSDM sampled with 1-GHz clock that operates at limit cycle of 125 MHz. In Fig. 8, the simulated output spectrum of the transistor implementation for 1-MHz sine input signal is shown. A SNDR of 64 dB is achieved in a bandwidth of 5 MHz.

The impact of the process variations on the limit cycle can be seen as modification of the phase-gain relation in the loop. The loop mechanism adjusts the limit-cycle amplitude to accommodate the deviation. However, in order to assure the desired mode, a safety margin for the GBW is recommended.

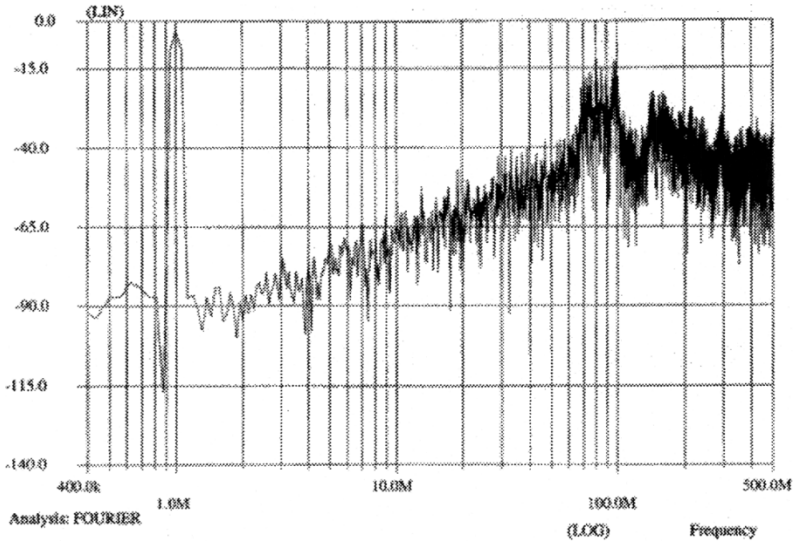

Fig. 8. Simulated output spectrum.

C. Advantages of the Lower Loop Frequency

It can be pointed out that the LCMs are not taking full advantage of the clock speed. However, in [13], it is shown that for high clock speeds it is very difficult to achieve the theoretically expected performance with real circuit implementations. Even some recent designs [14], [15], display performance well below the theoretically achievable one for the implemented filter order and the applied clock speed. One of the reasons for this is the susceptibility of higher order SDMs to enter unpredicted limit cycles that appear only for certain input amplitudes or clock speeds. On top of that, when the SDM operates at full clock speed it is very sensitive to excessive loop delays and clock imperfections.

In that respect, the proposed LCM of operation has several important advantages.

- The GBW that is required for the linear part of the loop corresponds to that required for a SDM operating at a fraction of the clock speed. This leads to a simpler implementation and a significant reduction of the power consumption.
- The loop delay is taken into account in the determination of the LCMs and is made a part of the loop mechanism. Higher extra delay can be tolerated.
- The proposed mode of operation introduces a tradeoff between conversion bandwidth, limit-cycle frequency and clock frequency and thus gives an additional degree of freedom in the design of SDM.

V. Conclusion

The existence of limit cycles in second-order ASDMs and SDMs was investigated via the DF method. The determination of the frequency and amplitude of the possible limit cycles was shown. An SDM that is forced to operate in a LCM was proposed. The expected performance was confirmed with simulations. It was pointed out that this mode of operation leads to a reduction of the total power consumption and significantly reduces the design complexity.

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