More effective Krylov subspace construction for smaller EM-based equivalent circuit models

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Pieter Heres [2], Jan Niehof [1], Wil Schilders [1,2]
[1]) Philips Research Laboratories
WAY, Prof. Holstlaan 4, Eindhoven, The Netherlands
[2]) Eindhoven University of Technology
PO Box 513, 5600 MB Eindhoven, The Netherlands
p.j.heres@tue.nl

Abstract

Although Krylov subspace methods have proved to be useful techniques to reduce the size of linear interconnect models, they suffer from the drawback of redundancy. The size of the models generated by the methods is larger than strictly needed. In this paper we propose a method to reduce this redundancy. The modification requires only minor extra computational effort and makes Krylov subspace methods significantly more efficient.

Two examples are given as a demonstration and validation of the proposed method. We show that with the new method models can be generated which are approximately 25% smaller in size and 50% faster in simulation time.

Introduction

In many industrial applications, model order reduction (MOR) techniques are of interest to overcome computational complexity. However, in the large variety of MOR methods that are available at the moment, only a few meet the requirements to be suitable for this area of application. In RF simulation applications there is a growing desire for stable time-domain simulations. The applications that are designed nowadays work with frequencies up to 60 GHz and have to be simulated in that range as well. All these requirements formulate a challenging task where MOR can play a vital role.

This article focuses on the application of an algorithm as implemented in a proprietary 2.5D EM simulator. This allows simulation on real-life electronic interconnect structures and functional RF layout components. Here a boundary element method is implemented to calculate the EM-properties of a layout. This is done in a way similar to the well-known PEEC method ([1],[5]). The equivalent circuit is reduced using a technique, which is available in the layout-simulator. However, this frequency domain based reduction method does not allow for time-domain simulations, because stability is not guaranteed.

The well-known methods PRIMA [7] and Laguerre-SVD [4] are implemented in this layout simulator as an alternative for the existing reduction method. The preservation of stability and passivity is shown in [2], where transient simulations using models generated by our initial implementation of the MOR algorithms were presented.

We have however observed that the reduced systems generated by applying Krylov subspace methods in a straightforward way are larger than really needed. The models contain redundant information, making the equivalent circuit models larger and the simulation times longer. The proposed modifications make the methods more efficient and demand only a minor extra computational effort.

Krylov subspace methods

An equivalent model for the layout can be formulated as a linear time-independent problem:

$$\mathbf{C}\frac{d}{dt}\mathbf{x}(t) + \mathbf{G}\mathbf{x}(t) = \mathbf{B}\mathbf{u}(t)$$
$$\mathbf{y} = \mathbf{L}^T\mathbf{x}(t)$$

The size of the model is dictated by the size of the state space vector. If the MNA formulation is applied the state space vector consists of voltage and current variables, associated with the circuit nodes and the branches that contain an inductor, respectively.

Laplace transforming these equations to the frequency domain and eliminating the state space vector **X**(s) gives the transfer function:

$$\mathbf{H}(s) = \mathbf{L}^T (s\mathbf{C} + \mathbf{G})^{-1} \mathbf{B}$$

The transfer function gives a description of the behavior of a system in the frequency domain. Given a moment expansion or Laguerre expansion [4] of the transfer function:

$$\mathbf{H}(s) = \mathbf{L}^T \sum_i s^i \mathbf{M}^i ,$$

in a Krylov space the coefficients (moments) of this expansion of the transfer function are collected in a space, the Krylov space. Normally this space has smaller dimensions than the dimensions of the system itself. If then the original system is projected onto this Krylov space, the size of the system is reduced and a certain number of coefficients in the expansion are preserved. Therefore, this smaller system gives an approximation of the original, large system.

For multiple input systems the matrix $\mathbf{B}_i$ has more than one column. Every port in the system corresponds with one column in this matrix. Hence, the Krylov space will be a Block Krylov space, consisting of blocks of size, say *p*, the number of ports.

There are some attributes of Krylov subspace methods that make them more interesting for this application than others. For a start, the methods are relatively cheap. Secondly, they converge to the exact system. Finally, they are more generally applicable than many truncation methods, like Balanced Truncation [6]. Krylov spaces methods can also be applied to DAE's, which are systems that have a singular matrix **C**.

A disadvantage of Krylov subspace methods is that they do not distinguish between important and negligible information. This can be seen from the fact that the reduced systems generated by Krylov subspace methods contain more information than really needed. For instance, some poles are approximated which are not needed in a good approximation. Besides, in many cases like PRIMA, there is no error bound known for the methods. Hence, it is not clear when to stop building a Krylov space. This is a second reason that an approximation can be generated, which is too large.

This is different from for instance truncation methods. In these methods, first the system is transformed into a form, which elucidates the difference between important states of the system and state that can be neglected in an approximation.

We have to remark here that the pictured problem is inherent to (Block) Krylov space methods. Therefore, an optimal choice of the expansion point in for instance PRIMA, cures part of this problem, but does not completely solve the problem.

Redundancy reduction

In our research we found a way to remedy part of this redundancy. Suppose a system has *p* ports. Then, every iteration of the Krylov space algorithm, adds *p* columns. However, not every column is adding an equal amount of information to the space. At a certain point there can be columns which are almost zero or which are already spanned by columns in the already existing Krylov space. This event can easily be detected during the construction of the block to be added. Hence, the method requires hardly any extra computational effort.

Two situations can arise: Firstly, a column in the block to be added is almost zero and secondly, a column might be completely spanned by columns, which are already in the Krylov space. When a Block Arnoldi procedure, as in for instance PRIMA, is applied, the second situation boils down to a column, which is almost zero just before the block is orthogonalized in itself by a QR step.

We therefore came up with an orthogonalisation procedure, comparable to modified Gramm-Schmidt, which removes columns that are zero or spanned by others and orthogonalizes the rest of the columns. In detail, suppose we have a three-column matrix **W** of which the second column is zero. The orthogonalisation comes up with an orthonormal basis **Q** of the two remaining columns, such that:

$$\mathbf{QR} = \mathbf{W} ,$$

where **Q** has two columns and **R** is a 2 by 3 upper triangular matrix. In this way we ensure that columns that do not really matter, are not added to the Krylov space. The remaining columns are added in such a way that the essential Krylov space properties are preserved. Exact details are given in [3].

The computational effort of this extra feature is comparable to the normal orthogonalization in a Block Arnoldi procedure, a QR decomposition.

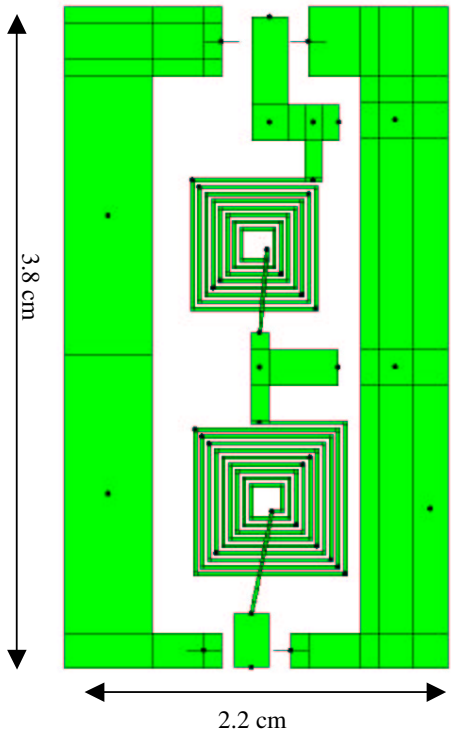
The main advantage of this method is obviously that, with a smaller system, the same level of approximation can be achieved.

Threshold for column removal

When the norm of a column vector is smaller than a certain specified threshold, it will be removed. With the introduction of this threshold an error is introduced. Removing columns, which are not exactly zero, is unavoidable, but may lead to errors in the Krylov space. More information on this topic can also be found in [3].

Demonstration

The advantages of the method can best be illustrated by some examples. Consider the following layout of a printed double LC-filter. The inductors of the layout are printed in metal. The two capacitors are added to the netlist to complete the circuit simulator input.

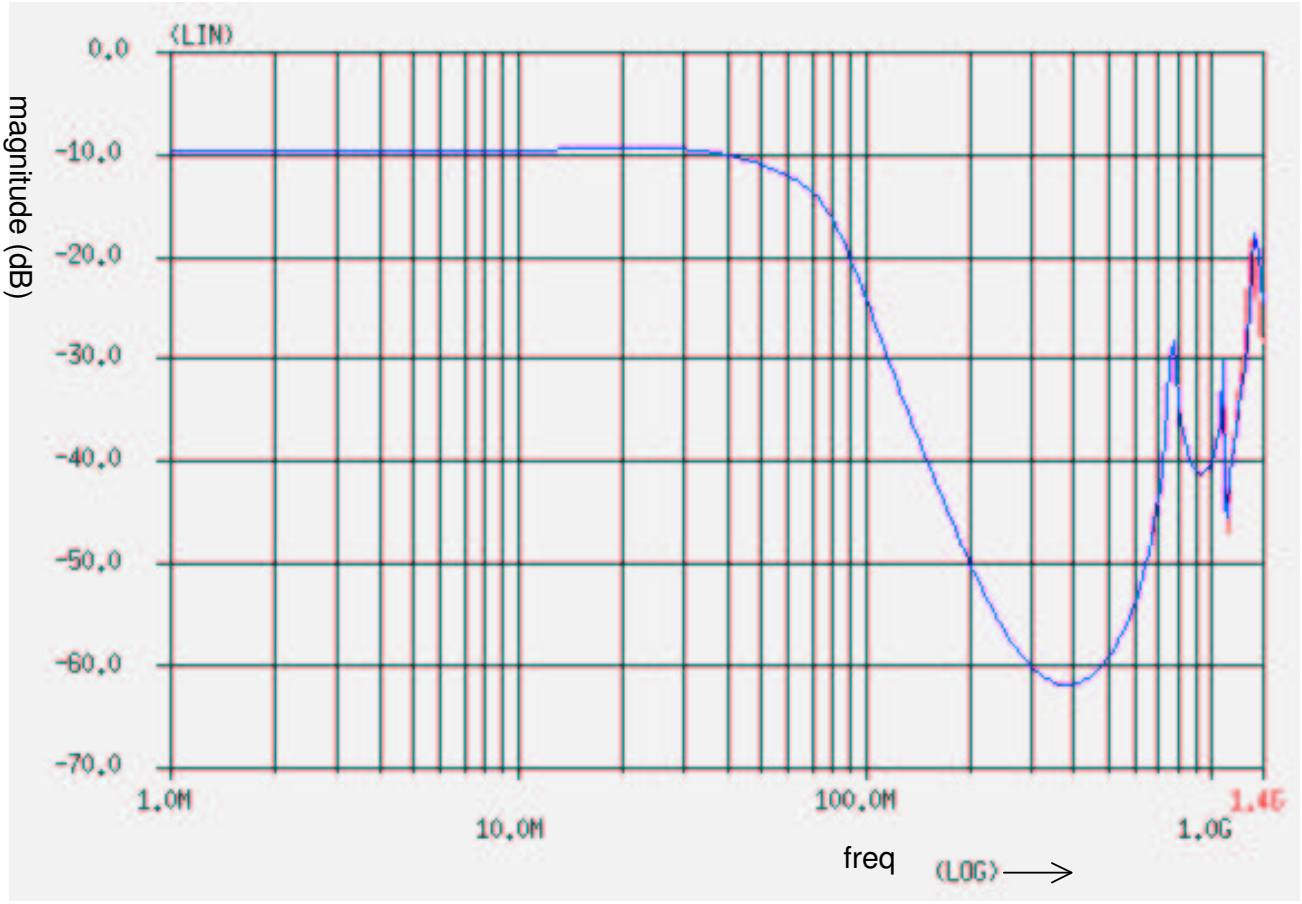


The layout simulator generates an equivalent model for this layout, which consists of an RLC-circuit with 223 circuit nodes and 236 branches with inductors in it. This comes down to a system of equations with 459 equations. For this given problem we consider 15 ports. So, in every iteration 15 columns will be added. Hence, after 6 iterations a Krylov space of 90 columns is constructed. The reduced system of size 90 gives an excellent approximation of the original system from frequency 0 to 1.2 GHz.

Now suppose columns smaller than the threshold of 1e-12 are removed. Then the following is seen:

In the first iteration all 15 columns are added, but in the third iteration 5 columns fall below the threshold and are therefore removed. So 10 columns are added. The 10 columns are taken into the fourth iteration and so on. Finally the construction of the Krylov space is completed with the 10 remaining columns.

The total number of columns in the Krylov space is therefore 70 (15+15+10+10+10+10). In the following picture the frequency response of the system is given. The red line is the PRIMA approximation of the model of size 90. The blue line is the 70-sized approximation of the proposed algorithm.

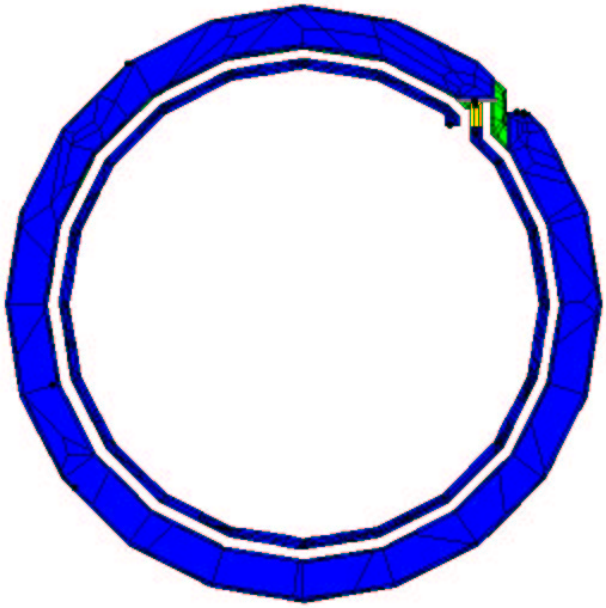


In the following table the time to generate the model and the time simulate the circuit in the frequency domain is given. It is seen that with a little extra effort in computational time, to compute the reduced models, a significant gain in simulation speed is achieved.

	Size	Time to generate	Simulation time
Standard PRIMA	90	0.92 sec	15.14 sec
New PRIMA with tol 1e-12	70	1.58 sec	6.57 sec

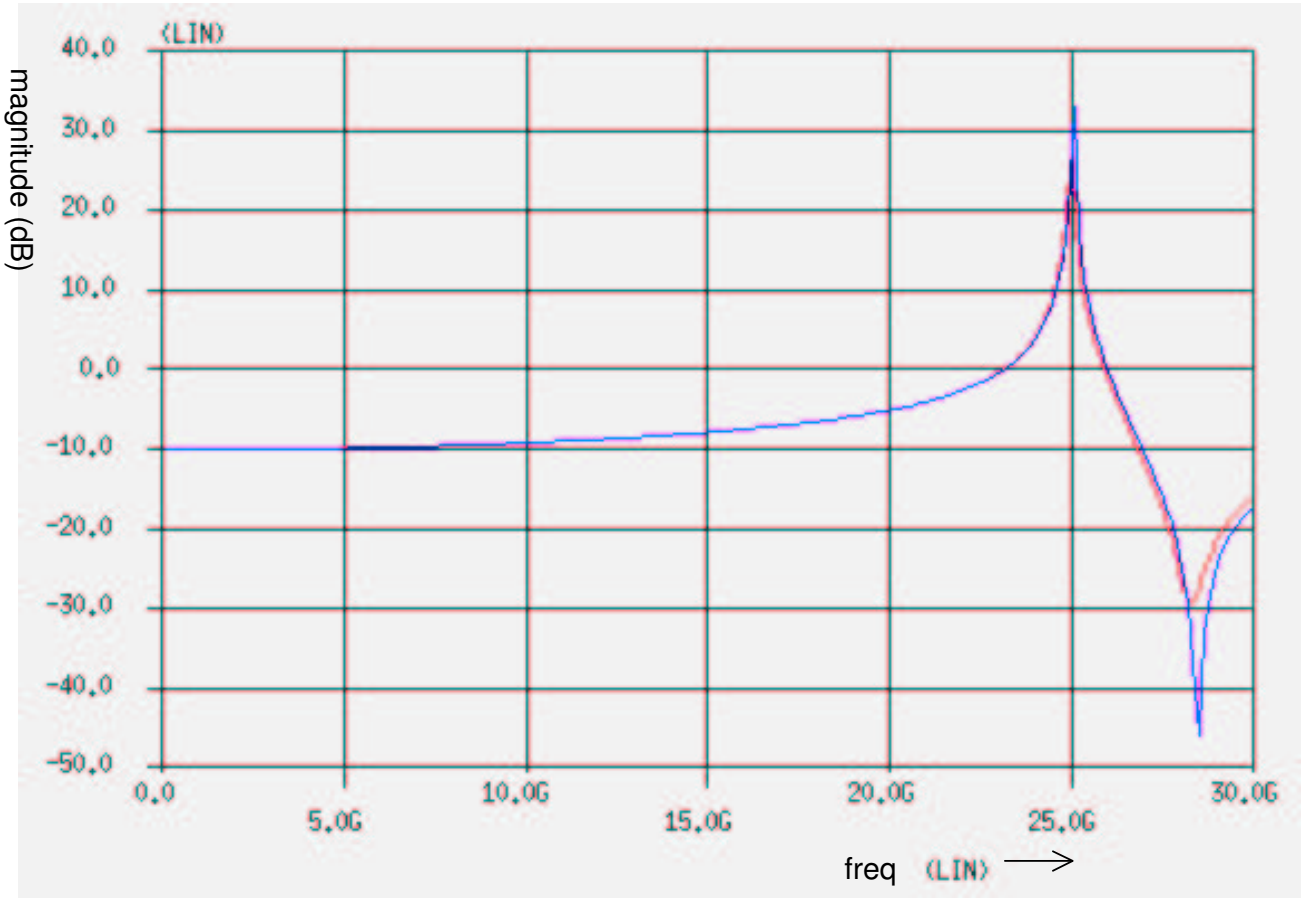
The second example is an RF transformer layout structure. The passive component has feature sizes of 340 by 340 micrometers. In the following picture the meshed layout is shown. Only the top layer can be seen, beneath it are two more narrow strips completing the second loop. The mesh consists of 1865 elements. The equivalent circuit generated by the layout simulator consists of 1865 circuit nodes and 3337

branches with inductors in it. This constitutes a system of 5202 equations.



The standard PRIMA approximated model with a 40-sized system. The red line in the next figure depicts the standard reduction result. The application of the proposed method (with threshold equal to 1e-13) gives the blue line. In the construction process immediately in the second iteration 1 of the four columns is removed, which gives a system of size 31, after 10 iterations.

As can be seen in the following picture the further reduced model still gives a good approximation of the behavior of the transformer.



A table can be drawn similar to the previous example:

	Size	Time to generate	Simulation time
Standard PRIMA	40	231 sec	0.85 sec
New PRIMA with tol 1e-13	31	239 sec	0.47 sec

Again a significant reduction in simulation time is seen, while the time to generate the reduced models is comparable.

Conclusions

This paper presents a new, very effective method to further reduce the size of reduced order equivalent models, while maintaining the level of accuracy.

Using real-life layout structures it is demonstrated that circuit simulation times for the structures can significantly be reduced, with a minor extra effort. This opens the possibility to include layout structure models in complete RF block simulations.

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