Compact modeling of high-voltage LDMOS devices including quasi-saturation

Compact Modeling of High-Voltage LDMOS Devices including Quasi-Saturation

Annemarie C.T. Aarts and Willy J. Kloosterman

***Abstract*— The surface-potential-based compact transistor model, MOS Model 20 (MM20), has been extended with quasi-saturation, an effect that is typical for LDMOS devices with a long drift region. As a result, MM20 extends its application range from low-voltage LDMOS devices up to high-voltage LDMOS devices of about 100V. In this paper, the new dc model of MM20 including quasi-saturation is presented. The addition of velocity saturation in the drift region ensures the current to be controlled by either the channel region or the drift region. A comparison with dc measurements on a 60V LDMOS device shows that the new model provides an accurate description in all regimes of operation, ranging from sub-threshold to super-threshold, in both the linear and saturation regime. Thus, owing to the inclusion of quasi-saturation also the regime of high gate and high drain bias conditions for high-voltage LDMOS devices is accurately described.**

***Index Terms*— LDMOS, Modeling, High-Voltage MOS, Quasi-Saturation, Integrated Circuit Design.**

I. Introduction

TODAY, high-voltage LDMOS devices are extensively used in all kinds of integrated power circuits for automotive and consumer applications. Optimal design of these power circuits requires high-voltage LDMOS models for circuit simulation, which describe the device characteristics accurately. Inclusion of specific LDMOS transistor aspects, like the quasi-saturation effect, is therefore necessary.

Recently, a new compact LDMOS transistor model called MOS Model 20 (MM20) has been developed [1]. This model describes the currents of an LDMOS device in surface-potential formulations, thereby including accumulation in the drift region. As a result, MM20 gives an accurate description in all regimes of operation, ranging from sub-threshold to super-threshold, in both the linear and saturation regime. The original MM20 model is aimed at *low-voltage* LDMOS devices (which consequently have a relatively short drift region). For such an LDMOS device, velocity saturation always occurs in the channel region of the device, the reason why velocity saturation occurring in the drift region has not been included in the original MM20 model. For *high-voltage* LDMOS devices (which consequently have a long drift region), however, velocity saturation can occur in the drift region of the device [2], an operating regime generally referred to as quasi-saturation. In that case, the saturation characteristics of the device are controlled by the drift region instead of by the channel region. The main limitation of the present MM20 model thus is that it is not applicable to these high-voltage devices.

So far, various LDMOS models have been developed which take quasi-saturation into account [3]-[11]. In the sub-circuit models [3]-[8] the internal potentials of the device are solved by the circuit-simulator, in which case no control can be executed on the convergence during circuit simulation. In the compact models [9]-[11], the internal potentials are solved by a numerical iteration procedure inside the model itself. The drawback of most models, however, is that accumulation in the drift region is neglected ([4], [9] and [10]), and that the sub-threshold regime is not included ([3], [4], [9] and [11]).

The aim of this paper is to present a new model for MM20 which includes the effect of quasi-saturation. To that end, velocity saturation in the drift region is included, which limits the dc-current at high gate and high drain bias conditions. Furthermore, in addition to accumulation occurring in the drift region, also pinch-off of the drift region through depletion has been included. The capacitances are described according to the original MM20 model [1]. Through the inclusion of quasi-saturation, however, in the new model the internal drain potential may obtain different values, affecting the capacitance values accordingly. Thus, the new model combines all the benefits of the original model with the ability to accurately describe quasi-saturation. As a result, a new MM20 model is obtained which can be used for both low-voltage and high-voltage LDMOS devices.

II. High-voltage LDMOS devices

In Fig. 1 a cross-section of a high-voltage LDMOS transistor is given. The p-well bulk (B) is diffused from the source-side under the gate (G), and thus forms a graded channel region (of length $L_{\rm ch}$). The internal drain Di represents the point where the graded channel turns into the lightly doped n^--drift region (of total length $L_{\rm dr}+L_{\rm LOCOS}$). To withstand the high voltages between source (S) and drain (D), the drift region is long and it comprises two different sections: the first section is the thin-gate-oxide drift region (of length $L_{\rm dr}$), and the second is the thick-field-oxide drift region (of length $L_{\rm LOCOS}$). The length of the gate on the thin gate oxide only, is denoted by $L_{\rm PSOD}$.

Above the threshold voltage of the channel region, electrons flow from the source through an inversion channel towards the drift region. With the gate extending over the drift region, subsequently an accumulation layer forms at the surface underneath the thin gate oxide of the drift region. At a certain

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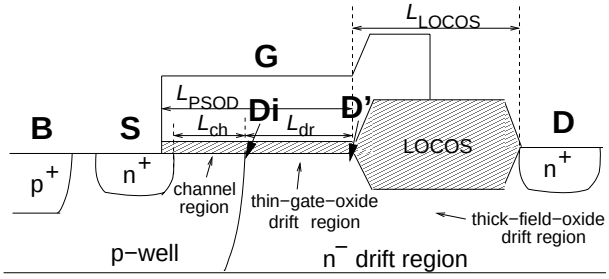

Fig. 1. A cross-section of a high-voltage LDMOS transistor, comprising two different drift region sections.

point in the thin-gate-oxide drift region, depletion occurs and the accumulation layer vanishes. Consequently, the electrons gradually flow into the bulk of the drift region (see [3]). Further towards the drain, in the thick-field-oxide drift region, the electrons are spread out across the whole body of the drift region. Since the LOCOS oxide is very thick compared to the thin gate oxide, the potential applied to the gate terminal has hardly any influence on the electrons in the drift region underneath this LOCOS oxide.

For simulation of the high-voltage LDMOS devices, the sub-circuit depicted in Fig. 2 is used. In this sub-circuit, MM20 describes the total region underneath the thin gate oxide. Since the gate voltage has hardly any influence on the electrons in the drift region underneath the LOCOS oxide, the current through the thick-field-oxide drift region is represented by a constant resistance $R_{\rm drift}$. The value of this resistance is given by

$$R_{\rm drift} = \frac{L_{\rm LOCOS}}{W} R_{\rm sheet}, \qquad (1)$$

where W is the width of the device, and $R_{\rm sheet}$ is the sheet-resistance of the thick-field-oxide drift region. The temperature rise due to self-heating is taken into account via a thermal network (not shown here) [7].

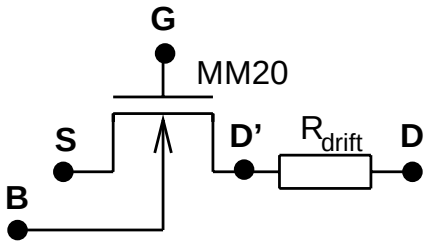

Fig. 2. Equivalent circuit for the high-voltage LDMOS device of Fig. 1. MM20 describes the total region underneath the thin gate oxide. The constant resistance $R_{\rm drift}$ represents the drift region underneath the thick LOCOS oxide.

Low-voltage LDMOS devices lack a thick-field-oxide drift region, and thus have a relatively short drift region; see [1]. In these devices the conductivity of the drift region is always larger than that of the channel region, so that saturation of the current is controlled by the channel region [8]. In high-voltage LDMOS devices, on the other hand, the current-voltage characteristics are affected at high gate-bias conditions; see Fig. 3. In this figure the measured drain-to-source current of a high-voltage (60V) LDMOS device is plotted versus drain voltage, over the whole gate-bias range. We observe that for high gate voltages the increase of saturation current with increasing gate voltage diminishes, which indicates the onset of quasi-saturation. The reason for the occurrence of quasi-saturation at high gate voltages is that the conductivity of the channel region is high, whereas that of the thin-gate-oxide drift region is low due to depletion in the drift region. For further increasing drain voltages the depletion layer widens, and the current through the drift region becomes confined to a limited effective cross-section [3], which leads to velocity saturation in the drift region.

Since velocity saturation occurring in the drift region has not been included in the present dc model of MM20, it is impossible to adequately describe quasi-saturation with this model. In Fig. 3 the simulated current obtained with MM20 without quasi-saturation is plotted in comparison to the measurements. We observe that for low gate voltages the model accurately describes the device characteristics. The reason is that for these low gate voltages saturation of the current is controlled by the channel region. For high gate voltages, however, the current is strongly over-estimated by the model, since in the present model the current can not be controlled by the drift region.

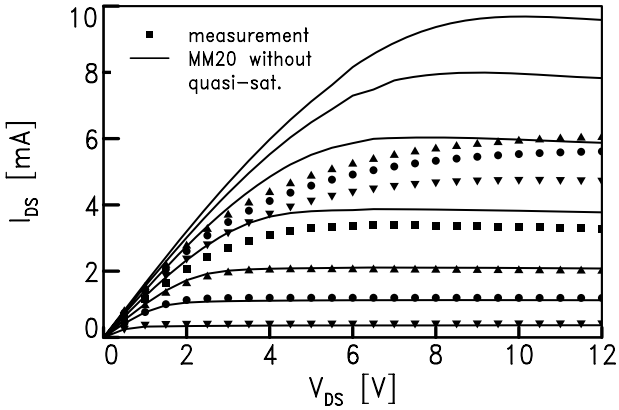

Fig. 3. Measured (symbols) drain-to-source current $I_{\rm DS}$ in comparison to MOS Model 20 (MM20) without quasi-saturation (solid lines), at $V_{\rm GS} = 2.4$, 3.4, 4.4, 6, 8 10 and 12 V and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm.

III. Model description including quasi-saturation

In our compact modeling approach, firstly expressions for the current $I_{\rm ch}$ through the inversion channel as well as for the current $I_{\rm dr}$ through the drift region are derived (see Sections III-A and III-B), both in terms of the known terminal drain-, gate-, source- and bulk voltages $V_{\rm D'}$, $V_{\rm G}$, $V_{\rm S}$ and $V_{\rm B}$, respectively, as well as of the unknown internal drain voltage $V_{\rm Di}$. Subsequently, the internal drain voltage $V_{\rm Di}$ is derived by equating $I_{\rm ch}$ to $I_{\rm dr}$. Since inclusion of velocity saturation in the drift region makes the current expression for $I_{\rm dr}$ more complex, an iteration procedure is included inside the model for the calculation of the internal drain potential. As the current difference $I_{\rm ch} - I_{\rm dr}$ is a monotonically increasing function of $V_{\rm Di}$, with exactly one zero between the source- and the external drain potential, the standard Newton-Raphson

scheme is used combined with a bisection procedure to speed up the iteration process and to ensure that the internal drain potential remains within its domain. In this way, a fast and robust iteration procedure is obtained for the calculation of the internal drain potential. Next, the internal drain voltage is used to calculate the surface potential ψ_{s_L} at the internal drain according to [12]. Finally, the drift- and diffusion component of the channel region current is calculated, both in terms of its surface potentials. Subsequently, second-order effects like channel length modulation, drain-induced barrier lowering and static feedback are added. Notice that expression of the final current in surface potential formulations yields an accurate current description, also in the sub-threshold regime.

A. Channel current

For the calculation of the internal drain quasi-Fermi potential $V_{\rm Di}$, the channel current $I_{\rm ch}$ is expressed as (see [1] with the surface-potential drop $\Delta\psi_{\rm s}$ replaced by $V_{\rm DiS}$)

$$I_{\rm ch} = \frac{W\mu_{\rm eff}^{\rm ch}C_{\rm ox}}{L_{\rm ch}}\frac{\left(V_{\rm inv_0} - \frac{1}{2}\,\xi\,V_{\rm DiS}\right)V_{\rm DiS}}{1+\theta_3\,V_{\rm DiS}}. \qquad (2)$$

Here, $\mu_{\rm eff}^{\rm ch}$ is the effective electron mobility in the channel region, $C_{\rm ox} = \epsilon_{\rm ox}/t_{\rm ox}$ is the thin-gate-oxide capacitance per unit area (with $t_{\rm ox}$ the thickness of the thin gate oxide, and $\epsilon_{\rm ox}$ its permittivity), $V_{\rm inv_0} = -Q_{\rm inv_0}/C_{\rm ox}$ represents the inversion charge $Q_{\rm inv}$ per unit area at the source side, and $\theta_3 = \mu_0^{\rm ch}/(L_{\rm ch}v_{\rm sat})$ represents velocity saturation in the channel region, with $\mu_0^{\rm ch}$ the zero-field electron mobility in the channel region and $v_{\rm sat}$ the saturated drift velocity of electrons. The factor $\xi = \left(\partial Q_{\rm inv}/\partial\psi_{\rm s}\right)/C_{\rm ox}$ reflects the variation of inversion charge with surface potential, and is taken as $\xi = 1+\frac{1}{2}\gamma_0/\sqrt{V_1+\psi_{\rm s_0}}$, where γ_0 is the body factor at the source, $V_1 = 1$ V, and $\psi_{\rm s_0}$ is the surface potential at the source. To account for mobility reduction due to the vertical electrical field, the effective electron mobility is taken as [1]

$$\mu_{\rm eff}^{\rm ch} = \frac{\mu_0^{\rm ch}}{1+\theta_1 V_{\rm inv_0}+\theta_2\left(\sqrt{\psi_{\rm s_0}}-\sqrt{\psi_{\rm s_0}|_{V_{\rm SB}=0}}\right)}, \qquad (3)$$

where θ_1 and θ_2 are model parameters.

Velocity saturation in the channel region occurs if

$$\left.\frac{\partial I_{\rm ch}}{\partial V_{\rm DiS}}\right|_{V_{\rm DiS}=V_{\rm sat,ch}} = 0. \qquad (4)$$

By use of (2) and (3), elaboration of (4) yields for the saturation potential of the channel region

$$V_{\rm sat,ch} = \frac{2\,V_{\rm inv_0}/\xi}{1+\sqrt{1+2\,\theta_3\,V_{\rm inv_0}/\xi}}. \qquad (5)$$

Subsequently, we incorporate saturation in the channel region current $I_{\rm ch}$ by taking an effective potential drop $V_{\rm DiS,eff}$ according to [13], which takes the minimum of $V_{\rm DiS}$ and $V_{\rm sat,ch}$ in a smooth manner.

B. Drift region current

To take velocity saturation into account in the drift region, its current is given in a continuous way as [14]

$$I_{\rm dr} = W\,\frac{\mu_{\rm eff}^{\rm dr}\left(-Q_{\rm n}^{\rm dr}\right)\dfrac{{\rm d}V_{\rm C}}{{\rm d}x}}{1+\dfrac{\mu_{\rm eff}^{\rm dr}}{v_{\rm sat}}\dfrac{{\rm d}V_{\rm C}}{{\rm d}x}}, \qquad V_{\rm Di} < V_{\rm C} < V_{\rm D'}, \qquad (6)$$

where $\mu_{\rm eff}^{\rm dr}$ is the effective electron mobility in the drift region, $Q_{\rm n}$ is the charge density per unit area, and $V_{\rm C}$ is the quasi-Fermi potential in the drift region. For the drift region we take both accumulation and depletion underneath the thin gate oxide into account, so that

$$-Q_{\rm n}^{\rm dr} = qN_{\rm D}t_{\rm Si_{eff}} - Q_{\rm acc}^{\rm dr} - Q_{\rm dep}^{\rm dr}, \qquad (7)$$

where q is the electron charge, $N_{\rm D}$ is the doping concentration of the drift region, $t_{\rm Si_{eff}}$ is the effective drift region thickness (taking into account the reduction due to depletion from the pn-junction), $Q_{\rm acc}^{\rm dr}$ is the accumulation charge per unit area at the surface of the drift region, and $Q_{\rm dep}^{\rm dr}$ is the depletion charge per unit area at the surface of the drift region. Both the accumulation- and depletion charge depend on the potential drop $V_{\rm GC}$ between gate and drift region, according to (see [15])

$$Q_{\rm acc}^{\rm dr} = -C_{\rm ox}\left(V_{\rm GC} - V_{\rm FB}^{\rm dr}\right), \qquad (8)$$

valid for $V_{\rm GC} > V_{\rm FB}^{\rm dr}$, and

$$Q_{\rm dep}^{\rm dr} = \gamma^{\rm dr}C_{\rm ox}\left(-\frac{\gamma^{\rm dr}}{2}+\sqrt{\left(\frac{\gamma^{\rm dr}}{2}\right)^2-\left(V_{\rm GC}-V_{\rm FB}^{\rm dr}\right)}\right), \qquad (9)$$

valid for $V_{\rm GC} < V_{\rm FB}^{\rm dr}$, respectively. Here, $\gamma^{\rm dr} = \sqrt{2q\epsilon_{\rm Si}N_D}/C_{\rm ox}$ is the body factor of the drift region, and $V_{\rm FB}^{\rm dr}$ is the flatband voltage of the drift region. Integration of (6) from $x = L_{\rm ch}$ to $x = L_{\rm ch}+L_{\rm dr}$ yields

$$I_{\rm dr} = \frac{W}{L_{\rm dr}}\,\frac{\mu_{\rm eff}^{\rm dr}}{1+\theta_3^{\rm dr}\,V_{\rm DDi}}\int_{V_{\rm Di}}^{V_{\rm D'}}\left(-Q_{\rm n}^{\rm dr}\right){\rm d}V_{\rm C}, \qquad (10)$$

where $\theta_3^{\rm dr} = \mu_{\rm eff}^{\rm dr}/(L_{\rm dr}v_{\rm sat})$. In the model, $\theta_3^{\rm dr}$ is taken as parameter, thus independent of the bias condition. In this way, a sufficiently large value for $\theta_3^{\rm dr}$ ensures the occurrence of velocity saturation in the drift region. Substitution of (7)-(9) into (10) yields, under the assumption that $t_{\rm Si_{eff}}$ is independent of $V_{\rm C}$,

$$I_{\rm dr} = \frac{W\mu_{\rm eff}^{\rm dr}C_{\rm ox}}{L_{\rm dr}}\,\frac{\left(V_{\rm n}^{\rm dr}\big|_{V_{\rm C}=V_{\rm Di}} - \frac{1}{2}\,\xi^{\rm dr}\,V_{\rm D'Di}\right)V_{\rm D'Di}}{1+\theta_3^{\rm dr}\,V_{\rm D'Di}} \qquad (11)$$

in which a Taylor expansion has been made around $V_{\rm C} = V_{\rm Di}$. Here, $V_{\rm n}^{\rm dr} = -\,Q_{\rm n}^{\rm dr}/\,C_{\rm ox}$, so that

$$V_{\rm n}^{\rm dr}\big|_{V_{\rm C}=V_{\rm Di}} = \begin{cases} \dfrac{qN_{\rm D}t_{\rm Si_{eff}} - Q_{\rm acc}^{\rm dr}\big|_{V_{\rm C}=V_{\rm Di}}}{C_{\rm ox}}, & V_{\rm GDi} > V_{\rm FB}^{\rm dr}, \\ \dfrac{qN_{\rm D}t_{\rm Si_{eff}} - Q_{\rm dep}^{\rm dr}\Big|_{V_{\rm C}=V_{\rm Di}}}{C_{\rm ox}}, & V_{\rm GDi} < V_{\rm FB}^{\rm dr}, \end{cases} \qquad (12)$$

while $\xi^{\rm dr} = \left(\partial V_{\rm n}^{\rm dr} / \partial V_{\rm C}\right)\big|_{V_{\rm C}=V_{\rm Di}}$. For simplicity, $\xi^{\rm dr}$ is taken equal to 1, which is the value in accumulation. Finally, to account for mobility reduction due to the vertical electrical field in accumulation, the effective electron mobility is taken as [1]

$$\mu_{\rm eff}^{\rm dr} = \frac{\mu_0^{\rm dr}}{1 + \theta_{\rm 1acc}\left(\frac{1}{2}\left(V_{\rm GS} + V_{\rm GD'}\right) - V_{\rm FB}^{\rm dr}\right)} \tag{13}$$

where $\mu_0^{\rm dr}$ is the zero-field electron mobility in the drift region.

Velocity saturation in the drift region occurs if

$$\left.\frac{\partial I_{\rm dr}}{\partial V_{\rm D'Di}}\right|_{V_{\rm D'Di}=V_{\rm sat,dr}} = 0. \tag{14}$$

By use of (11) and (13), elaboration of (13) yields for the saturation potential of the drift region

$$V_{\rm sat,dr} = \frac{2\ V_{\rm n}^{\rm dr}\big|_{V_{\rm C}=V_{\rm Di}}}{1 + \sqrt{1 + 2\,\theta_3^{\rm dr}\ V_{\rm n}^{\rm dr}\big|_{V_{\rm C}=V_{\rm Di}}}}. \tag{15}$$

Notice that, in contrast to the channel region, the saturation potential in the drift region depends on the internal drain potential $V_{\rm Di}$. Subsequently, we incorporate saturation in the drift region by taking an effective potential drop $V_{\rm D'Di,eff}$ according to [13], which takes the minimum of $V_{\rm D'Di}$ and $V_{\rm sat,dr}$ in a smooth manner.

IV. Results

We have characterized a 60V LDMOS device, with thin-gate-oxide thickness $t_{\rm ox} = 38$ nm, and a thick-field-oxide thickness of 0.7 μm. The device is processed in SOI-technology [16], and it has different mask widths $W_{\rm mask}$, and lengths $L_{\rm PSOD}$ and $L_{\rm LOCOS}$. For the reference device of $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm, the resistance $R_{\rm drift}$ is equal to 330 Ω. In the model, velocity saturation in the drift region is obtained by taking $\theta_3^{\rm dr} = 0.9$ V^{-1}.

In Fig. 4 we observe that the model describes the sub-threshold current accurately, also at the transition from the weak- to strong inversion regime. The reason for the accurate description in the sub-threshold regime is the formulation of the final drain-to-source current $I_{\rm DS}$ in surface potentials. Furthermore, the inclusion of drain-induced barrier lowering yields in this regime an accurate description of the increase in current for higher drain voltages.

In Fig. 5, we observe that also in the linear regime the model is accurate, even at high gate voltages where the effect of the gate extending over the drift region is significant. Thus, by inclusion of the potential drop across the accumulation layer in the thin-gate-oxide drift region, an accurate description is obtained.

In Fig. 6 the drain-to-source current and the output conductance are plotted versus drain voltage, for relatively low gate voltages. In this operating regime the current is controlled by the channel region, and saturation of the current occurs because the electrons in the *channel region* reach their saturated drift velocity (see Fig. 9). Notice that in Fig. 6 a negative output conductance is obtained, which clearly demonstrates the effect of self-heating. In the model, the effect of self-heating is

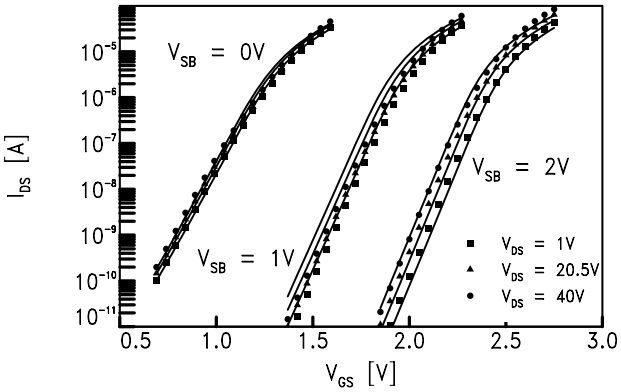

Fig. 4. Measured (symbols) and modeled (solid lines) drain-to-source current $I_{\rm DS}$ in the sub-threshold regime, for $V_{\rm SB} = 0$, 1 and 2 V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm.

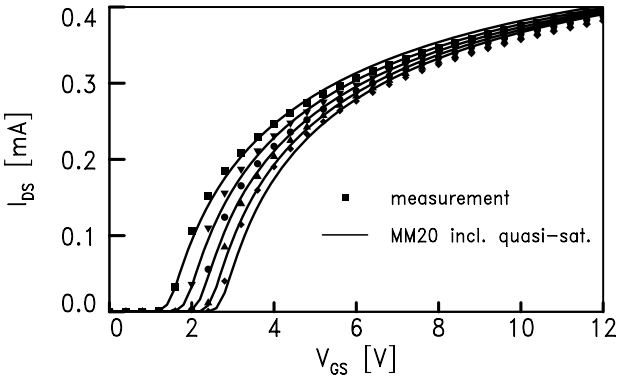

Fig. 5. Measured (symbols) and modeled (solid lines) drain-to-source current $I_{\rm DS}$ in the linear operating regime, for $V_{\rm DS} = 0.25$ V and $V_{\rm SB} = 0$, 0.5, 1, 1.5 and 2 V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm.

incorporated by the temperature dependent model parameters. By subsequent use of a thermal network [7], which calculates the temperature rise due to self-heating, the current through the device is affected accordingly.

In Fig. 7 the measured drain-to-source current is plotted versus drain voltage, over the whole gate-bias range; see also Fig. 3. For the high gate voltages, the current is controlled by the drift region, and saturation of the current occurs because the electrons in the *drift region* reach their saturated drift velocity (see Fig. 10). As we have seen in Fig. 3, MM20 without quasi-saturation is not capable of describing the current correctly at these high gate voltages. By inclusion of quasi-saturation in MM20, however, we observe in Fig. 7 that an accurate current description is obtained, also for the high gate voltages.

In Fig. 8 the drain-to-source current versus gate voltage is plotted. In this figure we clearly see that for high gate voltages the increase of current with increasing gate voltage diminishes, indicating again the onset of quasi-saturation. Thus, by inclusion of velocity saturation in the drift region of MM20, an accurate description is obtained for the whole range of bias conditions.

To demonstrate the effect of velocity saturation in the drift region, in Figs 9 and 10 the internal potentials of MM20

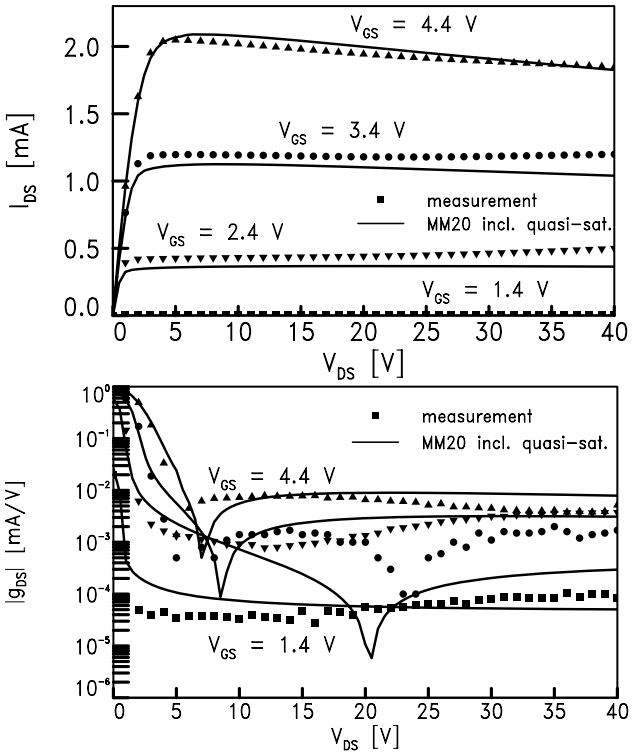

Fig. 6. Measured (symbols) and modeled (solid lines) drain-to-source current $I_{\rm DS}$ and output conductance $|g_{\rm DS}| = |\partial I_{\rm DS}/\partial V_{\rm DS}|$, for $V_{\rm GS} = 1.4$, 2.4, 3.4 and 4.4 V, and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm.

including quasi-saturation are plotted versus drain voltage. In Fig. 9 the internal potentials are given for the relatively low gate voltage $V_{\rm GS} = 3.4$ V. In this figure we observe that when the current saturates, the potential drop $V_{\rm Di} - V_{\rm S}$ over the channel region exceeds its saturation potential $V_{\rm sat,ch}$. At the onset of saturation the potential drop $V_{\rm D'} - V_{\rm Di}$ over the thin-gate-oxide drift region, on the other hand, is still below its saturation potential $V_{\rm sat,dr}$; only for higher drain voltages also the potential drop over the thin-gate-oxide drift region exceeds its saturation potential. Thus, for $V_{\rm GS} = 3.4$ V firstly the potential drop of the channel region exceeds its saturation potential, and the saturation current is controlled by the channel region.

In Fig. 10 the internal potentials of MM20 are given for the high gate voltage $V_{\rm GS} = 12$ V. In contrast to Fig. 9, we observe in Fig. 10 that when the current saturates, the potential drop $V_{\rm D'} - V_{\rm Di}$ over the thin gate-oxide drift region exceeds its saturation potential $V_{\rm sat,dr}$. The potential drop $V_{\rm Di} - V_{\rm S}$ over the channel region, on the other hand, is significantly decreased for $V_{\rm GS} = 12$ V compared to the one for the low gate voltage $V_{\rm GS} = 3.4$ V, and it remains below its saturation potential $V_{\rm sat,ch}$. Thus, for $V_{\rm GS} = 12$ V the saturation current is dictated by the thin-gate-oxide drift region, and quasi-saturation occurs in the device. Finally, we notice in both Figs 9 and 10 that in saturation most of the potential drop $V_{\rm DS}$ falls across the thin-gate-oxide drift region.

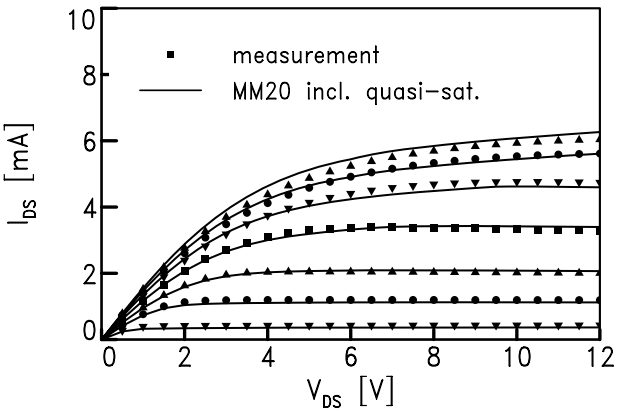

Fig. 7. Measured (symbols) drain-to-source current $I_{\rm DS}$ in comparison to MOS Model 20 (MM20) including quasi-saturation (solid lines), at $V_{\rm GS} = 2.4$, 3.4, 4.4, 6, 8, 10 and 12 V and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm; cf. Fig. 3. By inclusion of quasi-saturation into MM20, an accurate description is obtained, also for the high gate voltages applied.

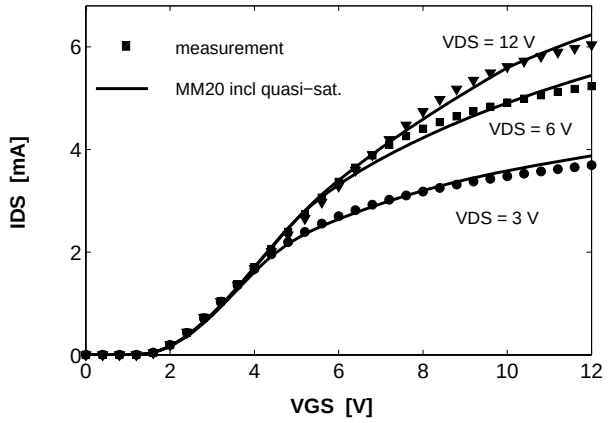

Fig. 8. Measured (symbols) drain-to-source current $I_{\rm DS}$ in comparison to MOS Model 20 (MM20) including quasi-saturation (solid lines), at $V_{\rm DS} = 3$, 6 and 12 V, and $V_{\rm SB} = 0$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm.

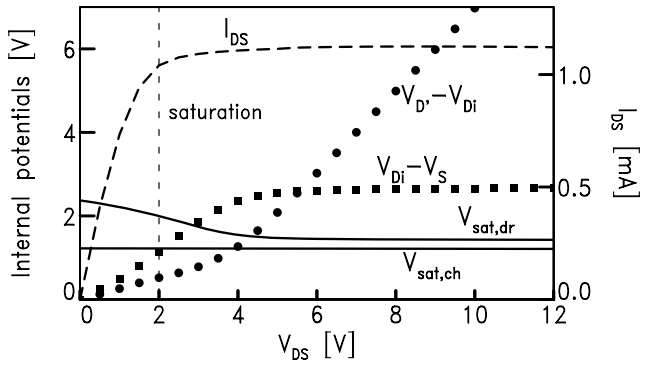

Fig. 9. Internal potentials of MOS Model 20 including quasi-saturation, for $V_{\rm GS} = 3.4$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm (see also Fig. 7)

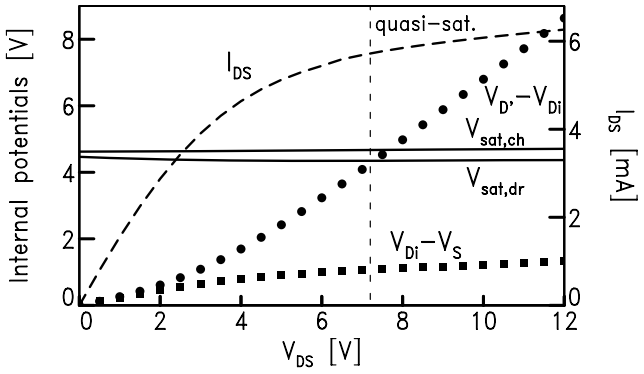

Fig. 10. Internal potentials of MOS Model 20 including quasi-saturation, for $V_{\rm GS} = 12$ V, for $W_{\rm mask} = 20$ μm, $L_{\rm PSOD} = 2.6$ μm and $L_{\rm LOCOS} = 3.5$ μm (see also Fig. 7).

V. Conclusions

A new model description of the surface-potential-based compact LDMOS transistor model, MOS Model 20, has been presented which includes the effect of quasi-saturation. By taking velocity saturation in the drift region into account, an adequate solution of the internal drain potential is obtained, which ensures the current to be controlled by either the channel region or the drift region. A comparison with dc measurements on a 60V LDMOS device shows a very good agreement, in all operating regimes ranging from sub-threshold to strong inversion, in both the linear and saturation regime. Thus, owing to the inclusion of quasi-saturation, the new model can be successfully used for high-voltage devices, also in the regime of high gate and high drain bias conditions. In this way, MM20 extends its application range from low-voltage LDMOS devices up to high-voltage LDMOS devices of about 100V. Successful use of the model in circuit simulations has proven that the iteration procedure inside the model, used for the calculation of the internal drain potential, is robust and sufficiently fast. Finally, it is mentioned that the source code and documentation of the model will become available in the public domain [17].

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