Current status and prospects of photonic IC technology

2007 International Conference on Indium Phosphide and Related Materials
Conference Proceedings
19th IPRM 14 - 18, May 2007 Matsue, Japan

CURRENT STATUS AND PROSPECTS OF PHOTONIC IC TECHNOLOGY

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Abstract

The most complex Photonic ICs today have been developed for WDM applications. An overview of the most important integration technologies will be given and recent developments towards broader applications and higher integration densities will be discussed.

I. Introduction

Photonics is a rapidly growing sector in the global economy. Optical communications, optical disks, digital cameras, lighting, lasers and optical sensors are just a few examples. In comparison to electronics, most photonic equipment is still large and ex-pensive. Just like in micro-electronics, many applications can be realized in a much more compact and cost-effective way by integrating the required functionality in a single chip.

So far the main drive for photonic integration has come from telecommunications, and especially WDM applications, and most of the integrations technologies reported today have been developed for application in the telecommunication wavelength window around 1.55 μm. More recently applications of this technology in other fields are emerging too.

In the present paper we will start with a short overview of the most important integration technologies reported today. Next we will give a sketch of current and future developments in photonic integration technologies and we will present some thoughts on the physical limits of Photonic Integration. Parts of this paper have also been presented at the European Conference on Integrated Optics ECIO '07 in Copenhagen on April 23-26.

II. Integration technologies

A major issue for Photonic Integration is the way in which active waveguide sections, used in laser and optical amplifier, are integrated with transparent waveguide sections, as they are used in a variety of passive devices like couplers, filters, wavelength (de)multiplexers, switches and modulators. In principle two different schemes can be distinguished, each with a number of variants. They are illustrated in Figure 1. In the first one active and transparent waveguides are in the same plane. In the second one the active and the passive layers are stacked vertically. The structures can be realised in several ways.

For the in-plane integration the most straightforward one is by first growing one stack on the full wafer, selectively removing that stack in the regions where the other stack is needed, by covering the wafer with a mask everywhere where the first stack is needed, and regrowing the second stack after etching away the first one while preventing regrowth on the region where the first stack is still present. This is called butt-joint integration because the active and the passive waveguides are coupled via a butt joint. This process offers a large flexibility to the designer, because both stacks can be chosen and optimised independently. In practical schemes the number of regrowths required is three [1] or even more [2]. The epitaxial regrowth process requires a tight control of process conditions in order to keep the yield sufficiently high

In-plane integration can also be realised by growing the active waveguide stack over the whole wafer and locally transforming the active layer into a transparent layer by shifting its absorption band edge by Quantum Well Intermixing [3]. This approach is simpler from an epitaxial point of view and it offers the opportunity to integrate more than two different stacks in a single growth step, with band edges optimised, for example. for use in optical amplifiers, electro-absorption modulators and passive waveguide devices. An important disadvantage is the reduced design freedom for the layer stack, which is the same through the whole wafer, including dopant level. As the requirements for the doping level in the cladding are conflicting for low-loss transparent waveguides and low resistance current injection devices like SOAs a compromise between waveguide loss and device resistance has to be accepted.

In the second scheme the active layer is applied on top of the transparent waveguide and it is removed afterwards everywhere where it is not needed. In this

1-4244-0875-X/07/$20.00 ©2007 IEEE.

approach each of the vertically stacked waveguide layers carries a waveguide mode, and light is vertically coupled from one waveguide to the other using am adiabatic taper. This approach [4] has the advantage that it requires only single step epitaxy and that the active and the passive waveguide stacks can be optimised independently. A disadvantage is the increased surface non-planarity which is inherent to this scheme and which complicates later processing, and the additional length of the tapers used for switching from the active to the passive waveguide layer. The latter point is important only if several active devices have to be cascaded, as it may occur in Large-Scale Integration.

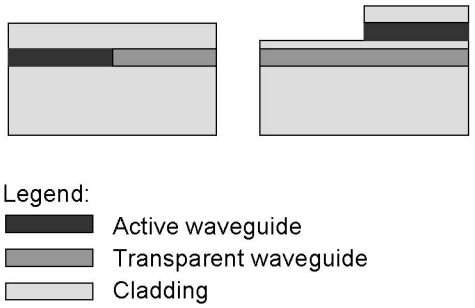

Figure. 2. Two different schemes for integration of active and passive waveguides.

In addition to the referenced technologies there are a number of other variants or mixed forms. Which one is best depends on the targeted application. On the longer term, we expect that the technology offering most design flexibility, i.e. butt-joint integration technology, will find the broadest application. Once these technologies are sufficiently mastered they open the way for integrating more complex Photonic ICs. In the next paragraph we will discuss the anticipated development with respect to complexity and integration density.

III. Moore's law in Photonics

The field of Information and Communication Technologies is showing a development speed which is unprecedented in history. Over a period of more than thirty years key features like processor speed and memory size are roughly doubling each 18 months. It is known as Moore's law [5] and enabled by the development of micro-electronic integration technology.

There have been several attempts to map the development of Photonic Integration on a Moore-like plot, with circuit complexity or integration density mapped logarithmically against time. However, due to the large variety in components and technologies, one ends up with a scattered cloud of data points that provide little insight.

If we restrict ourselves to devices realised in a similar technology, which is actually also the case in the famous Intel plot [6], a clear trend becomes visible as shown in Figure 2 for InP-based WDM-PICs [7]. This plot, of which we presented the first version in 1995 (IEEE/LEOS Annual Meeting), appears to be surprisingly valid today, more than ten years later and it is very useful for explaining trends in photonics. The plot shows an increase in integration density of around two orders per decade, which is roughly the slope of Moore's law. It should be noted that the vertical axis does not refer to circuit complexity, but to the number of (basic) components that fit on 1 cm^2, which is about the maximum size of a chip. So they are indicative for the maximum achievable circuit complexity, but practical circuits are usually smaller.

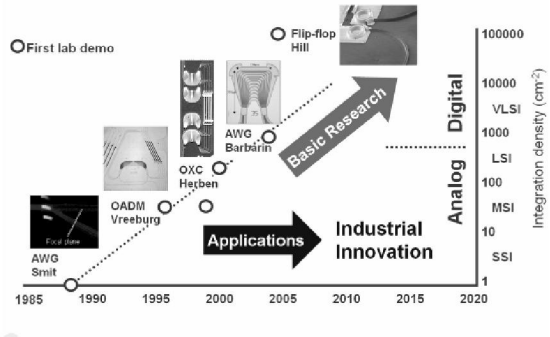

Figure 1 Moore's law in photonics for PICs developed at COBRA.

The data points shown are first laboratory demonstrators. Early commercial realisations follow the line with a delay in the order of 5 years. The most recent example is the 10-channel WDM transmitter chip with a capacity of 100 Gb/s (10x10 Gb/s), that is applied by Infinera in its WDM systems [8]. It integrates over 40 components in a single chip: 10 tunable DFB-lasers, 10 EA-modulators, 10 VOAs, 10 monitor-diodes and a 10-channel AWG. Although Infinera does not reveal the chip size the density is probably around 500 components per cm^2, which fits well into the metrics of Figure 2..

IV. Analog PICs

An interesting question is how long this increase in density and complexity will continue. Infinera announced already a chip with over 200 components per chip, by increasing the channel count of its device from 10 to 40 [8]. On a longer term even larger channel counts will appear, but it is unlikely that in this way, by increasing parallelism, the complexity will exceed a component count of 1000 per chip.

The alternative is serial integration, but also along this line it is improbable that the 1000 components/chip barrier will be broken. The main reason for this is that todays PICs, although they usually carry digital signals, operate essentially in an analog mode. As a result, errors generated by the components will cumulate and, after having passed a number of components, the signal will be degraded so strongly that it has to be regenerated. On-chip signal regeneration is possible, but full regenerators are complex and they also require a significant amount of chip space. Breaking the 1000 components/chip barrier by serial integration is, therefore, also unlikely. A combination of serial and parallel integration may bring us close, but we expect

that for analog PICs the increase in complexity will saturate around or below 1000 components/chip. But this is not the end of Moore's law for Photonics.

V. Towards Digital PICs

In the early days of micro-electronics analog circuits, such as operational amplifiers, formed an important market. Their complexity was typically limited to a few hundred components per circuit. Signal integrity was maintained by the application of feedback, but this limits the circuit complexity because feedback over too long distances reduces the speed and may cause instabilities.

A real breakthrough towards VLSI required, therefore, digital circuits that operate essentially with only two levels, so that the signal is inherently regenerated after each operation and cascading of hundreds of signal operations becomes possible with virtually no signal degradation.

In photonics digital signal processing is still in an embryonic stage. A number of papers on flip-flops or logical gates have been published, but their size, speed and power consumption is such that they allow only for very small integration levels and they are by far not competitive with modern electronics.

Recently a breakthrough in digital photonic signal processing has been reported by Hill [9]: a photonic flip-flop based on two coupled microring lasers with dimensions of 20x40 μm^2, a switching time of 18 ps and a switching energy of a few femtojoules. Although the device is still considerably larger than an electronic flip-flop, its dimensions allow for integrating hundred thousands of these components on a single chip, which is an integration complexity far beyond today's imagination. Its switching speed is comparable to that of high-speed electronic transistors, its switching energy is smaller by more than three orders. With some modifications (adding additional input waveguides) the device can also be used as a logical gate, so that the coupled microlasers form a basic building block for both digital photonic signal processing and storage.

From Figure 1 it is seen that this device does not fit into the Moore's law metrics, it is more than a decade ahead. This is due to the fact that, although it is realised in a similar technology as the other devices in the plot, the flip-flop element is much smaller than the basic elements (AWGs, switches) used in the other devices. This underlines the potential of this kind of technology for VLSI.

An important issue for digital photonics is the competition with electronics. Analog photonics brings a number of functionalities that are difficult to realise with electronics, especially for high speed signal processing. But as soon as we go to digital signal processing we will have to beat electronics in a field where it is extremely strong. Although the whole field is still very young a few applications where digital photonics will become competitive are already visible. An important one is header processing in all-optical packet switched networks, where huge electronic routers are required to switch the Terabit data streams that occur in high-level networks. In such networks digital photonic header processing may lead to a substantial reduction of the amount of high speed electronics that is required in the routers. But when the performance of digital photonics increases more applications can be envisaged and also operations like high-speed Optical Time Domain Demultiplexing, which are now performed by rather sensitive analog optical circuitry, may be performed by digital photonic circuits.

VI. Where are the limits?

It is clear that the device reported in [9] is only a first step into a new field of photonics, and it is an interesting question how far we can get before we encounter the fundamental limits of digital photonic signal processing.

An advantage of photonics over electronics is that it does not incur the charge displacements which form the speed bottleneck in electronic switching. Photonics can, therefore, operate at a higher speed than electronics, in principle, its switching speed is limited by the time that light needs for effective interaction in the switching structure. In nanocavities this time can be far into the subpicosecond domain. Electronics has the advantage that it can store information (charge) with virtually no power consumption. This is not possible in coupled lasers, they consume the same power in static and dynamic operation. We expect, therefore, that for ultrafast processing, including some short term memory functions, photonics may turn out to be superior to electronics, but for longer-term storage electronics will remain superior.

Whether photonics will really become an option for digital signal processing depends on how far features like component size and power consumption can be reduced. The microring lasers used in [9] had a ring diameter of 16 μm, and a threshold current of 30 mA. Much smaller lasers have been reported, such as the Photonic-Crystal micro-cavity lasers by Park [10], which have dimensions of a few micrometers and a threshold current of 260 μA. Logical gates based on such a laser will combine sub-ps switching times with sub-femtoJoule switching energies. Although the required injection currents are still prohibitive for integrating millions of such lasers, results reported on other microcavity lasers suggest that threshold currents can become so small (a few microamps) that integrating a million lasers on a chip may become reality. This is still much less than the transistor count in a modern pentium, but if the memory and other "slow" functions are provided by electronics it would allow for the design of powerful processors.

Research reported by Hill [11] indicates that by using metallic cavities the size of lasers can become comparable with that of modern transistors. Due to their small size, these lasers would operate at very low powers, and their predicted operation speeds are well into the THz domain. Research on nanostructuring of materials and components should make it possible for these devices to operate at room temperature. Such lasers would pave the way for VLSI digital photonic ICs,

containing millions of lasers, and operating at multi-TeraHz clock rates.

Such processors should be integrated in a compact and low-cost manner with the "slow" electronic functions that are required. The most promising way to do this seems to be heterogeneous integration of a InP photonic layer on top of a CMOS wafer, a technology which is has received increased attention in recent years.

VII. Conclusion

After a long time of development and struggling with market economics, photonic integration is becoming commercial reality. Costs are still high, however, because no large scale low-cost manufacturing facilities are available. For complex analog photonic circuits to penetrate mass markets, convergence in technologies will be mandatory, and here InP-based technology is a powerful candidate. Most probably in a hybrid technology platform that combines the power of InP-based technology with the power of CMOS. Such a technology is the subject of a number of research projects today.

For low-cost devices with a limited complexity silicon photonics will become a viable alternative, because of its compatibility with mature CMOS technology. For high complexity, involving light generation and amplification, and strong non-linear functionality, InP-based technology has a better potential and for large scale digital photonics it has no real competitor.

However, digital photonics is a dream so far. And so is much of what has been presented here. Many major issues have to be solved yet, such as thermal issues, developing a massive photonic interconnect layer, and finding proper ways of making the digital photonic circuits uni-directional, which is not trivial because of the strong preference of photonic circuits for reciprocal operation. But is a fascinating dream, and one that may come true.

Acknowledgments

The authors would like to acknowledge support form the Dutch Science foundation NWO (NRC Photonics), the Dutch Technology Foundation STW and the EU (several IST projects).

References

[1] Y. Barbarin, et al., "Butt-Joint Interfaces in InP/InGaAsP Waveguides with Very Low Reflectivity and Low Loss" in Proc. IEEE LEOS Benelux 2005.

[2] Y Suzuki et al., "Monolithically integrated eight-channel WDM modulator with narrow channel spacing and high throughput", IEEE J. of Sel. Topics in Quantum Electronics, Vol. 11, Jan/Feb 2005, pp. 43-49.

[3] E.J. Skogen et al., "Monolithically integrated active components: A Quantum-Well intermixing approach", IEEE J. of Sel. Topics in Quantum Electronics, Vol. 11, March/April, 2005, pp. 343-355.

[4] V.M. Menon et al., "Photonic integration using asymmetric twin-waveguide (ATG) technology: Part II – Devices", IEEE J. of Sel. Topics in Quantum Electronics, Vol. 11, Jan/feb 2005, pp. 30-42.

[5] G.E. Moore, "Cramming more components onto integrated circuits", Electronics, Vol. 38, pp. 114-117, Apr. 1965.

[6] www.intel.com/technology/mooreslaw

[7] Smit, M.K. et al., "Photonic integrated cir-cuits: where are the limits?", Proc. IPRA/NPIS 05, San Diego, CA, 11-13 April 2005, paper IWB1.

[8] R. Nagarajan et al., "Large-scale photonic in-tegrated circuits for long haul transmission and switching", J. of Opt. Networking, Vol. 6, No. 2, Feb. 2007, pp. 102-111.

[9] M.T. Hill et al., "A fast low-power optical memory based on coupled micro-ring lasers", Nature 432, nr. 7014, 2004, pp. 206-209.

[10] H.-G. Park et al., "Electrically Driven Single-Cell Photonic Crystal Laser", Science, Vol. 305. no. 5689, pp. 1444 – 1447, September 2004.

[11] M.T. Hill, "Micro and nanolasers for digital photonics", proc. Eur. Conf on Integr. Optics ECIO 2007, Copenhagen, Denmark, 25-27 April 2007, invited paper.