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design, technology, and characterization

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“Waat er veur haet, haet er noch neit achter.”

Aan Petra

mijn ouders en Ralf

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Chapter 1

Introduction

Since its reappearance in the early 1990s gallium nitride (GaN) has been regarded as a very interesting and highly promising material system for both optical and microwave high-power electronic applications. Over the last fifteen years researchers all around the world have made great efforts in order to redeem these promises. GaN-based optical applications have first reached the stage of commercialization while microwave high-power electronics are on the verge of their commercial breakthrough. The value of the worldwide GaN device market, which at present is about $3.5 billion, is estimated to be $7.2 billion by the year 2009.
This chapter will start with highlights of GaN research history. After this we will put GaN into perspective with conventional semiconductors and other wide-bandgap (WBG) materials. Among others we will give an overview of the application areas and the state-of-the-art of GaN-based microwave high-power electronics. Finally, we will discuss the objectives and organization of this thesis.

1.1 Highlights of Gallium Nitride research history

The material system of interest in this thesis is the wide-bandgap III-V compound semiconductor gallium nitride (GaN). GaN was first synthesized by Juza and Hahn in the 1930s by passing ammonia (NH_3) over liquid gallium (Ga) at elevated temperatures [74]. This method resulted in a powder consisting of small needles and platelets. Their purpose was to investigate the crystal structure and lattice constant of GaN. Due to the lack of a native GaN substrate no vapor phase epitaxial growth had ever been attempted.

In 1968, Maruska and Tietjen were the first to try the hydride vapor phase epitaxy (HVPE) approach to grow centimeter-sized GaN layers on sapphire substrates. In a traditional HVPE reactor the group III element such as Ga is transported as the monochloride. For example, gallium chloride (GaCl) is generated *in situ* by passing hydrochloric acid vapor (HCl(g)) over

liquid Ga. The group V element such as nitrogen (N) is transported as the hydride. Sapphire was chosen as substrate material because it is a robust material that is not reactive with ammonia. To date, sapphire has remained a very popular substrate for heteroepitaxial GaN growth. The early HVPE GaN films were grown at temperatures below 600 °C to prevent decomposition. However, these films were all polycrystalline. In 1969, Maruska realized that in an ammonia environment at temperatures above 600 °C GaN growth actually would occur instead of decomposition. He increased the growth temperature to 850 °C, the temperature typically used for gallium arsenide (GaAs), and obtained the first single crystalline GaN film [116]. The film quality could even be improved by increasing the temperature to 950 °C. All GaN films grown at that time showed very high electron concentrations (10^{20} cm^{-3}) even without intentional doping. The responsible n-type donors were believed to be nitrogen vacancies (V_N), a concept that has caused a lot of controversy over the years. Eventually oxygen (O_2) has been proposed as the responsible donor. Oxygen with its six valence electrons on an N site (N has five valence electrons) would be a single donor [148].

In order to create a pn junction a suitable p-type dopant had to be found. Zinc (Zn) seemed to be an appropriate acceptor as it worked for GaAs and gallium phosphide (GaP). Although heavy Zn concentrations rendered GaN films to be insulating, the films never became conducting p-type. Despite of this, Pankove *et al.* achieved the first GaN light emitting diode (LED) in 1971. This device consisted of an undoped n-type region, an insulating Zn-doped layer and an indium (In) surface contact. It could emit blue, green, yellow or red light depending on the Zn concentration in the light emitting region [134]. In 1972, Maruska was the first to propose magnesium (Mg) to be a better choice of p-type dopant than Zn. Using the same device structure as Pankove, Maruska grew the first HVPE GaN LED, emitting at a wavelength of 430 nm (violet) with Mg as the luminescent center [115]. Although Mg-doped devices (GaN:Mg) were much brighter than their Zn-doped equivalents, they were never very efficient (< 1 %) and no successful commercial product ever appeared. Nevertheless, Mg-doping has remained the basis for all commercial GaN-based LEDs and laser diodes (LDs) to date.

In the late 1970s, GaN research ceased virtually everywhere because of the continuing difficulties encountered with the growth of high quality films needed for device development. Remaining issues were the choice and availability of a suitable substrate, how to control the very high intrinsic n-type conductivity, and difficulties with obtaining conducting p-type GaN films. In 1982 only a handful of papers were published world-wide on this material system.

It was the perseverance of Isamu Akasaki that eventually resulted in obtaining conducting p-type GaN films in 1989. The conducting p-type films were discovered during cathodoluminescence (CL) observations of GaN:Mg in a scanning electron microscope (SEM). A photoluminescence (PL) study of the GaN:Mg material before and after low-energy electron beam irradiation (LEEBI) treatment showed that luminescence efficiency had increased by two orders of magnitude [4]. A Hall effect measurement indicated that the film had become p-type and conducting. The explanation for this phenomenon was given by Van Vechten *et al.* in 1992 who proposed that the shallow acceptor level of Mg was compensated by a hydrogen atom complexing with the Mg acceptor [160]. This Mg:H complex passivates the acceptor and prohibits p-type conduction. The energy of the electron beam breaks up this complex and enables Mg to be a shallow acceptor approximately 0.16 eV above the valence band [2]. In

1992, Nakamura *et al.* discovered that annealing GaN:Mg above 750 °C in nitrogen (N_2) ambient or vacuum also converted the material to conducting p-type. However, annealing in NH_3 reintroduced atomic hydrogen and rendered GaN:Mg insulating again [126].

In 1986, a milestone was achieved when Amano *et al.* reported highly improved surface morphology, and optical and electrical properties of GaN films grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrates through the use of a low-temperature (600 °C) aluminum nitride (AlN) nucleation layer. This layer is grown between the sapphire substrate and the bulk GaN film, which is typically grown at 1050 °C [5]. In 1991, Shuji Nakamura of the Japanese company Nichia Chemical Industries Ltd. (now Nichia Corp.) extended this concept with the introduction of a low-temperature ($450-600\,^{o}$C) GaN nucleation layer. The reason for this was that the large lattice mismatch between the low-temperature AlN nucleation layer and the following GaN film could cause defect generation and that the use of a low-temperature GaN nucleation layer would prevent this [125]. To date, MOCVD is the workhorse for the growth of GaN and related materials.

The breakthroughs achieved by Amano, Akasaki and Nakamura have lead to the revival of the GaN material system in the early 1990s. Researchers in the fields of optical and microelectronic applications showed renewed interest in GaN as most well-developed semiconductors, e.g. silicon (Si) and GaAs, approached their theoretical limits and the great potential of GaN predicted tremendous performance enhancement over these existing technologies. In 1991, Khan *et al.* reported first evidence for two-dimensional electron gas (2DEG) formation at an $Al_xGa_{1-x}N$/GaN heterojunction grown by MOCVD on sapphire [84]. The first GaN metal semiconductor field-effect transistor (MESFET) and heterostructure field-effect transistor (HFET) grown by MOCVD on sapphire substrates were reported in 1993 and 1994, respectively by Khan *et al*. [82, 83]. In 1993, Nakamura *et al.* demonstrated the first high-brightness (HB) blue double-heterostructure (DH) GaN LEDs [127]. In 1996, Nakamura *et al.* reported the first continuous wave (CW) blue GaN LD [128].

Since these giant steps in material and device development, both research and commercial GaN activities have gained enormous attention. GaN-based optical applications have first reached the stage of commercialization while microwave high-power electronics are on the verge of their commercial breakthrough. Producibility, reproducibility and reliability of the epitaxial material and process technologies are key issues that need to be addressed to redeem the great promises GaN-based devices hold.

1.2 GaN put into perspective

Relevant questions that have to be answered when choosing any particular semiconductor material system are:

- What are the advantages and disadvantages over existing material systems for the intended application?
- What are the application areas?
- What are the costs and the expected market-value?

We will answer these questions in the following subsections.

1.2.1 Advantages and disadvantages of GaN

In this subsection we will answer the question what are the advantages and disadvantages of GaN by comparing its basic material properties with those of conventional semiconductors like Si, GaAs, and InP and other wide-bandgap (WBG) materials such as SiC and diamond. Furthermore we will compare GaN devices to existing and competing alternatives.

Material properties

Table 1.1 shows the fundamental material properties of GaN, SiC, diamond, Si, GaAs, and InP that are most important to electronic device performance [78, 157, 158].

A large bandgap energy (E_g) results in high electric breakdown fields (E_c), which enable the application of high supply voltages. Furthermore, it allows the material to withstand high operating temperatures and provides for improved radiation hardness. GaN and SiC have bandgap energies about two to three times those of conventional semiconductors such as Si, GaAs, and InP. The electric breakdown fields for the WBG materials are excellent and very high, typically one order of magnitude larger than for the conventional semiconductors.

Generally, to achieve high currents and high frequency operation, high charge carrier mobility (μ) and high saturation velocity (v_{sat}) are desirable. The high value for electron mobility of GaAs (8500 cm^2/Vs) is the main reason that field-effect transistors (FETs) fabricated from this material have such excellent high-frequency performance. A primary disadvantage of fabricating transistors from bulk GaN and SiC is the relatively low values for the electron mobilities, which are 900 cm^2/Vs for GaN and depending on the polytype approximately 700 cm^2/Vs for SiC. However, these values are sufficient for transistors specifically designed for high-power operation. In general, WBG semiconductors have relatively low mobility but very high values for the saturation velocity, which is reached at high electric fields that can easily be supported. The mobility and saturation velocity of the 2DEG at the $Al_xGa_{1-x}N$/GaN heterojunction is very suitable for high-power, high-frequency device applications. The room temperature (RT) mobility of the 2DEG, which is typically between 1200 cm^2/Vs and 2000 cm^2/Vs, is significantly better than that of bulk GaN and SiC. The 2DEG sheet charge density (n_s) of the $Al_xGa_{1-x}N$/GaN structure is very high (experimental values up to 1 x 10^{13} cm^{-2}) due to piezoelectric and spontaneous polarization induced effects. The measured sheet charge density is about a factor of 10 better than those of $Al_xGa_{1-x}As/In_xGa_{1-x}As$ and $In_xAl_{1-x}As/In_xGa_{1-x}As$ heterostructures.

The thermal conductivity (κ) of a semiconductor material is extremely important since this parameter is a measure for the ease with which dissipated power can be extracted from the device. Poor thermal conductivity leads to degraded device operation at elevated temperatures. In general, conventional semiconductors are poor thermal conductors, particularly GaAs and InP. Conversely, SiC and especially diamond are excellent thermal conductors and GaN is comparable with Si, the best of the conventional semiconductors.

Table 1.1: Material properties of conventional and wide-bandgap semiconductors at 300 K [78, 157, 158].

Property	GaN AlGaN/GaN	SiC	Diamond	Si	GaAs AlGaAs/ InGaAs	InP InAlAs/ InGaAs
Bandgap energy, E_g (eV)	3.44	3.26	5.45	1.12	1.43	1.35
Electric breakdown field, E_c (MV/cm)	3	3	10	0.3	0.4	0.5
Saturated (peak) velocity electrons, v_{sat} (v_{peak}) ($\times 10^7$ cm/s)	2.5 (2.7)	2.0 (2.0)	2.7	1.0 (1.0)	1.0 (2.1)	1.0 (2.3)
Electron mobility, μ_n ($cm^2/V{\cdot}s$)	900 2000^{α}	700	4800	1500	8500 $10{,}000^{\beta}$	5400 $10{,}000^{\chi}$
2DEG density, n_s ($\times 10^{13}$ cm^{-2})	1.0	N.A.	N.A.	N.A.	< 0.2	< 0.2
Thermal conductivity, κ (W/cm·K)	1.3 – 2.1	3.7 – 4.5	22	1.5	0.5	0.7
Relative permittivity, ε_r	9.0	10.1	5.5	11.8	12.8	12.5

$^{\alpha, \beta, \chi}$ values for the corresponding heterostructures.

The relative permittivity (ε_r) is an indication of the capacitive loading of a transistor and affects the device terminal impedances. Table 1.1 shows that the values of ε_r for the WBG semiconductors are considerably lower than those for the conventional semiconductors. In the case of GaN and SiC the values of ε_r are about 20% lower whereas for diamond the value of ε_r is even about 55% lower. This permits for example a GaN device to be about 20% larger in area for a given impedance. As a consequence, this increased area enables the generation of larger currents and higher microwave output power.

For a better comparison of the possible high-power and high-frequency performance of different semiconductor materials, several figures of merit have been proposed. These figures of merit combine the most relevant material properties with respect to high-power and high-frequency applications into one number that represents a rough measure of the relative strengths of the alternative materials. Johnson's figure of merit (JFOM) [72] takes into account the breakdown voltage and saturated electron drift velocity in defining a value for the high-frequency handling capability of a certain semiconductor. For GaN, the JFOM is 728 times that of silicon, about 93 times that of GaAs, and about twice that of SiC. Baliga's figure of merit (BFOM) [13] is calculated based on the relative permittivity, electron mobility, and electric breakdown field and is a measure for the high-power handling capability. Based on its properties, the BFOM for GaN is about 133 times that of Si, 11 times that of GaAs and three times that of SiC [21]. Form these figures it is very clear that GaN offers much better high-power/high-frequency performance possibilities than GaAs and SiC.

GaN devices compared to existing and competing alternatives

Besides AlGaN/GaN HFETs a wide range of existing technologies for the generation of solid-state microwave power is available, including Si bipolar, Si laterally diffused metal oxide semiconductor (LDMOS), GaAs MESFET and pseudomorphic HFETs (pHFET), AlGaAs/InGaAs HFET, GaAs, InP, InGaP, and silicon germanium (SiGe) heterojunction bipolar transistors (HBT) as well as SiC MESFETs. SiC MESFETs and GaN HFETs offer superior microwave performance compared to similar components fabricated from Si or GaAs, particularly at elevated temperatures. Microwave output power densities on the order of 4 - 7 W/mm and 10 - 12 W/mm are achievable from SiC MESFETs and GaN HFETs, respectively. For high-power/high-frequency applications GaAs has several major drawbacks. Among them are high substrate costs and low thermal conductivity. The latter makes it very difficult to effectively remove heat when used in high-power applications. An additional drawback is its critical electric field which is much smaller than that of the WBG materials. This explains why GaN HFETs can provide output power densities 10 times higher than GaAs pHFETs.

SiC MESFETs benefit from the excellent thermal conductivity of the substrate. However, their electron mobility is significantly lower than that of GaN HFETs, which is related to the lack of heterojunction technology in this material system.

SiGe HBTs have found applications in many microwave and mixed-signal products where they offer high-performance, yet cost-effective, products previously unavailable on a Si platform. However, the SiGe HBT's device structure remains a relatively low-power configuration. The high-frequency performance exhibited by SiGe HBTs largely results from reduced

minority carrier transit time through the base layer and reduced base resistance. To render this structure suitable for high-power applications, the collector layer would have to be made thicker up to a point where most of the advantages of the reduced base transit time would be eliminated because of a much larger collector delay [21]. Therefore, SiGe HBTs are unlikely candidates for high-power/high-frequency applications.

Si LDMOS transistors are the workhorses of today's base-station power amplifiers (PAs) owing to their excellent price-to-performance ratio compared with other commercially available technologies such as GaAs HFETs and Si bipolar junction transistors (BJTs). Emerging third-generation (3G) wireless cellular networks are designed to provide high data rate services beyond traditional voice. To support these higher data rates, 3G air interfaces such as wide-band code-division multiple access (W-CDMA) place severe demands on the linearity of the base station power amplifiers and associated power transistors. The transistor linearity spec, which is commonly expressed in terms of the adjacent channel power ratio (ACPR), also known as the adjacent channel leakage ratio (ACLR), can be as stringent as -65 dBc [21]. ACPR is a measure for the amount of power spilling into the adjacent channels referenced to the power in the transmit channel. To achieve the required linearity W-CDMA transistors must operate with the power backed-off to well below their peak capability. For example, a state-of-the-art LDMOS transistor with a P_{1dB} rating of 180 W is capable of producing about 38 W (approximately 80 mW/mm) of linear power under W-CDMA modulation, at 28 V operation [22]. As GaN HFETs show much higher linearity than Si LDMOS, it may be possible on a system level to reduce the complexity of the linearization circuitry necessary for high-bandwidth wireless systems. As LDMOS technology is capable of providing only moderate power density, it is necessary to use devices with very large gate peripheries and correspondingly very low die impedances to realize the required large powers. As a consequence, the bandwidth of the matching circuit is reduced. GaAs HFET manufacturers face an even more challenging task than their Si counterparts as the operating voltages (12 - 15 V) are lower, operating currents are higher and thermal conductivity is lower than Si. All these issues can be circumvented by using a higher power density technology that enables higher total output power and increased bandwidth resulting from a more compact layout as in the case of GaN-based HFETs. In this way a same-sized device can handle higher power that results in lower costs per watt of power and lower system costs. The higher impedance levels of these smaller devices considerably ease input matching and high-bandwidth design.

1.2.2 Application areas

The direct bandgap of GaN and its alloys enables the material to be used for both optical and electronic applications. At 300 K the bandgap of GaN is 3.44 eV which corresponds to a wavelength in the near ultra violet (UV) region of the optical spectrum. Figure 1.1 shows a plot of the bandgap energy versus lattice constant in combination with the visible optical spectrum for various semiconductors including the wide-bandgap materials SiC, GaN and its alloys indium nitride (InN) and aluminum nitride (AlN). It can be seen that the $Al_xIn_yGa_{1-x-y}N$ alloys cover bandgap energies from 1.9 eV to 6.2 eV, which correspond to wavelengths ranging from red to deep UV.

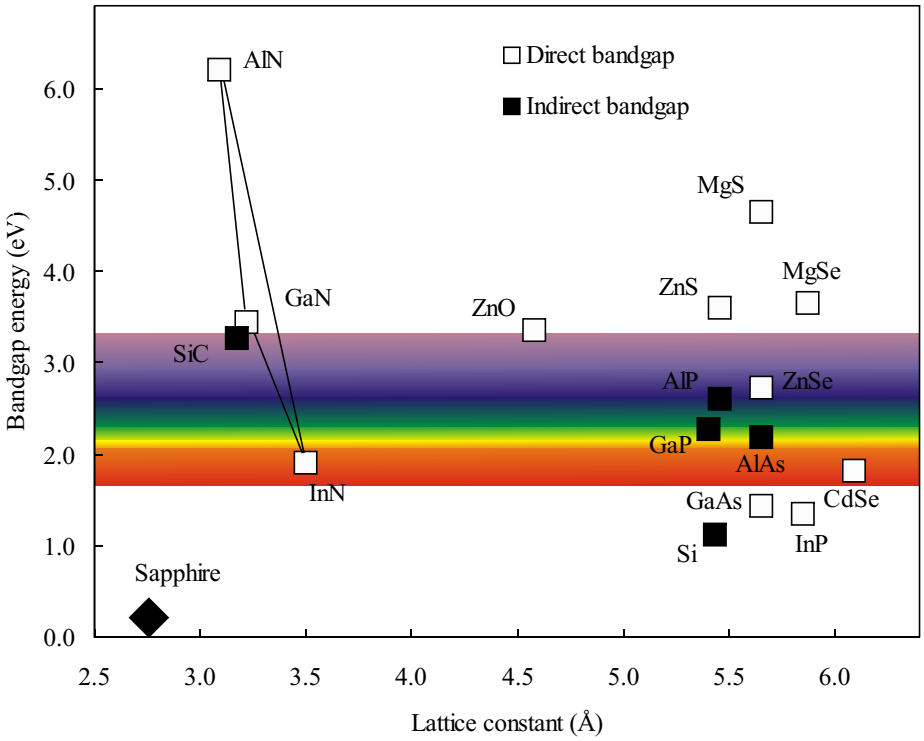

Figure 1.1: Bandgap energy versus lattice constant for various semiconductors including the wide-bandgap materials SiC and GaN with its alloys.

1.2.2.1 Optical applications

In 1968 James Tietjen, working at the Materials Research Division of the Radio Corporation of America (RCA), came up with the idea to develop a flat television that could be hung on the wall like a painting. A full color image can be created combining red, green, and blue pixels in the display. Red and green LEDs were available using gallium arsenide phosphide ($GaAs_{1-x}P_x$) and gallium phosphide nitride (GaP:N) materials, respectively. All that was missing to realise a flat LED-based television set was a bright blue LED. These devices became available using either SiC or II-VI compounds such as zinc oxide (ZnO). However, because of their indirect bandgap SiC LEDs were not very efficient. The devices based on II-VI compounds mainly suffered from much too short lifetimes for commercial applications. Hence these devices could not be used in the envisioned display application. As stated in Sect. 1.1 this void in solid-state

lighting was filled in 1993 by Nakamura *et al.*. By realizing high-brightness blue GaN-based LEDs that were about 100 times brighter than the previous blue SiC LEDs they made feasible the daylight visible full color display application.

LED applications

The main economical benefits of LED-based lighting are low power requirement, high efficiency, and long lifetime. In addition, solid-state design renders LEDs impervious to electrical and mechanical shock, vibration, frequent switching and environmental extremes. Several major markets are being addressed with these newly developed solid-state light sources. Automobile exterior lighting has been moving rapidly to incorporate transparent-substrate $Al_xIn_yGa_{1-x-y}P$ technology into high-mount braking lights and into the full amber and red-orange taillight assembly. Full-color, outdoor, changeable message signs and full-motion video displays have been adopting $Al_xIn_yGa_{1-x-y}N$ and $Al_xIn_yGa_{1-x-y}P$ technologies and will continue to proliferate as costs are reduced. Traffic-signal applications have begun to incorporate red AlInGaP and AlGaAs LEDs for traffic lights and are moving toward incorporating amber and blue-green LEDs to produce a completely LED-based signal head. All of these markets are rapidly expanding and will provide enormous growth opportunities in the future.

By using multiple LEDs, an LED cluster lamp continues to provide light even if one or more emitters fail unlike when the filament breaks in an incandescent bulb. Taking also into account an average life span of more than 100,000 hours (approximately 11 years), LEDs operate reliably year after year and are an excellent replacement for incandescent bulbs in hard-to-reach places and environments that depend on reliable lighting (e.g. hospitals, airports). Furthermore, colored lenses or filters are not needed since LEDs emit colored light that is determined by the composition of the semiconductor material comprising the diode. As LEDs are an energy-efficient light source and are virtually maintenance free, the cost savings are substantial. Other important GaN-based LED applications are backlighting (cell phones, PDAs), white light (flashlights, car head lights), general lighting (interior and exterior), water purification systems, and medical (sensors, surgical goggles).

Laser applications

Infra-red AlGaAs-based and red AlInGaP-based laser diodes (LDs), such as those in today's CD and DVD systems, have been around for decades. To increase the storage capacity on a CD, the pit size must be made smaller. A shorter wavelength LD is required to focus onto the smaller pit size. The current generation of DVD systems uses a LD with an emission wavelength of 650 nm. In the last few years the market for DVD systems has increased rapidly. However, the majority of these systems is read-only and is based on a 5 mW AlInGaP LD emitting at 650 nm. For further advances in the market recordable DVD was an obvious necessity. This required higher output power from the 650 nm LD (typically 30 - 40 mW). To also achieve faster read/write speeds even higher powers are required.

GaN-based blue-violet LDs with an emission wavelength of 405 nm will be the cornerstone of next-generation DVD player-recorders and optical high-density data-storage systems for

computers. Using these components it is already possible to write huge amounts of data (27 GB) on a single-layer 12 cm DVD disk which is almost six times the storage capacity possible with ordinary red LDs. This is enough to store more than two hours of high-definition (HD) video or 13 hours of standard-definition (SD) video.

In 2003, Tokyo-based Sony Corporation was the first consumer electronics company to begin offering next-generation DVD recorders. Sony leads a consortium called Blu-ray Disc, which is pushing one of two competing standards for the design of the discs, players, and recorders that use blue GaN-based LDs. The consortium further consists of the following major consumer electronics companies: Hitachi, LG Electronics, Matsushita Electric Industrial, Pioneer, Royal Philips Electronics, Samsung Electronics, Sharp, and Thomson. The other standard, high-density DVD (HD-DVD), has been proposed by Toshiba, Sanyo, and NEC [46]. At the time this thesis was written the first next-generation DVD systems, either Blu-ray Disc or HD-DVD, are expected mid 2006. Other GaN-based LD applications are laser printing, projection displays, and medical.

GaN-based blue LDs are used for the laser-induced fluorescence method (LIF) employing endogenous ("autofluorescence") and exogenous fluorophores. LIF is applied for clinical diagnosis in dermatology, gynecology, urology, lung tumors as well as for early dentin caries. The LIF method, which is fundamental for many medical applications, uses excitation radiation with a wavelength around 400 nm that could only be applied using tunable dye lasers or titanium lasers. This makes it only adequate for laboratory investigations. Development of GaN-based LDs provides the possibility to design portable, compact diagnostic devices as multi-channel analyzers of fluorescence spectra and surface imaging devoted to clinical applications. The designed systems used for spectra measurement and registration of fluorescence images include LDs with an output power of 5 - 30 mW at wavelengths of 405 - 407 nm. Dentistry diagnosis is a new field in which GaN-based LDs can be applied. After induction with blue light, decreased autofluorescence intensity can be observed when dentin caries occur [99].

1.2.2.2 Electronic applications

With respect to electronics, GaN is an excellent option for high-power/high-temperature microwave applications because of its high electric breakdown field (3 MV/cm) and high electron saturation velocity (1.5 x 10^7 cm/s). The former is a result of the wide bandgap (3.44 eV at RT) and enables the application of high supply voltages, which is one of the two requirements for high-power device performance. In addition, the wide bandgap allows the material to withstand high operating temperatures (300 °C - 500 °C). A big advantage of GaN over SiC is the possibility to grow heterostructures, e.g. AlGaN/GaN. The resulting two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction serves as the conductive channel. Large drain currents (> 1 A/mm), which are the second requirement for a power device, can be achieved because of the high electron sheet densities (1 x 10^{13} cm^{-2}) and mobilities (1500 - 2000 cm^2/Vs). These material properties clearly indicate why GaN is a serious candidate for next-generation microwave high-power/high-temperature applications. Figure 1.2 shows an overview of GaN-based micro-electronic applications.

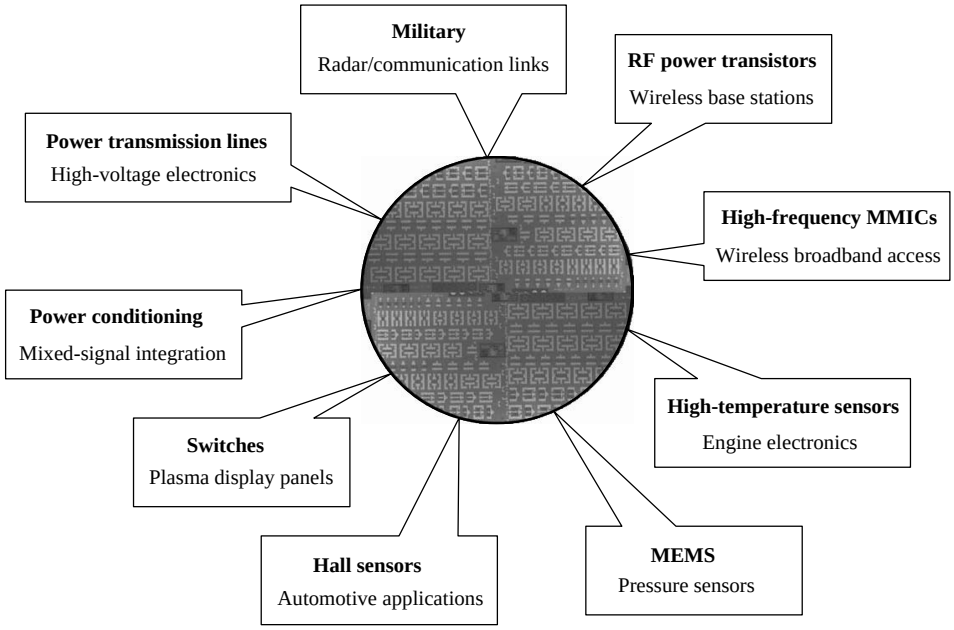

Figure 1.2: GaN-based micro-electronic applications.

Military applications

Despite the superior material properties and expected advances in device and system performance, the driving force behind research towards GaN-based microwave high-power/high-temperature electronics over the last decade has been almost exclusively military in nature. The main reason for this is the enormous costs that are involved with the early stages of GaN electronic device research. Several European countries, including France, Germany, United Kingdom, Italy, Spain, Sweden, and the Netherlands have defense oriented research programs, some of which are joint efforts such as the Swedish - Dutch SiC and GaN program (period: 2000 - 2005) and the new very big European GaN program KORRIGAN (Key Organization for Research on Integrated Circuits in GaN Technology) (period: 2005 - 2009). The frontiers of academic and military research and the commercialization of GaN-based electronics however are mainly in the US and to a lesser extent in Japan. US and Japanese research programs towards military microwave systems have been and continue to be heavily funded by the respective Departments of Defense (DoD). The US's Defense Advanced Research Projects Agency (DARPA) has granted a huge GaN program, total investment up to $144.5 million, with a triple-pronged approach to speed up the development of GaN-based microelectronics

and assure a rapid transition into military systems. Former research programs have focused on achieving hero values with respect to current densities and output power densities at microwave frequencies in order to prove the high expectations. The new programs however start for the basics (material growth, etching, contacts) and move through the stage of discrete devices to the eventual goal of GaN-based microwave monolithic integrated circuits (MMICs). The focus now is on understanding the physical reasons behind device failures and the development of physical models to predict performance in order to increase reproducibility and reliability. In general, defense research programs focus on the development of GaN technology for use in components such as surface radars, broadband seekers, jammers, battlefield communication, satellite communication links, transmit/receive modules, broadband high-power amplifiers (HPAs), and low noise amplifiers (LNAs). The frequencies of interest for these applications range from 2 GHz - 40 GHz.

Commercial applications

Commercial GaN-based applications are on the verge of their breakthrough. The first products will most probably be high-efficiency and high-linearity power amplifiers for base-stations, which power 3G wireless broadband cellular networks in the so-called S-band (2 GHz - 4 GHz). The US-based company RF Micro Devices (RFMD), the biggest player in this field, announced that it has sampled 100 W GaN amplifiers to customers early 2005. Competition can be expected from Japanese companies Fujitsu, Matsushita Electric, and OKI Electric [54]. Other high-volume commercial applications in which GaN-based electronics could lead to significant performance enhancement and cost reduction are high-frequency MMICs (wireless broadband communication links), hybrid electric vehicles (DC-AC conversion), high-temperature electronics (automotive, energy production), switches (plasma display panels, low-frequency high-power switching), high-voltage power rectifiers (inverter modules), micro-electro-mechanical systems, MEMS (pressure sensors), and Hall sensors (automotive applications).

Current hybrid electric vehicle (HEV) platforms, which use silicon-based power electronics, are faced with two major challenges: size and weight. In addition to traditional cars containing internal combustion engines (ICEs), HEVs must also accommodate power electronics, energy storage, and an electric motor in the predefined volume of the automobile platform. The HEV's motor drive, a power-electronics component that converts stored energy into an alternating-current (AC) source needed to operate the electric motor, is one of the main contributors to the system's size and weight. Typically, HEV motor drives use silicon insulated-gate bipolar transistors (IGBTs) for the primary switching element, with Si p-i-n diodes as the fly-back diode, configured in a module designed to control three-phase motors. The module is positioned inside the engine compartment as close to the electric motor as possible to minimize parasitic inductance and reduce cabling weight. However, like all silicon devices they are limited to junction temperatures of 150 °C - 175 °C. Controlling the junction temperature of the Si electronics in the engine compartment's harsh environment requires large heat sinks and liquid cooling, but both these solutions are costly and difficult to integrate into the volume available within the engine compartment. The temperature limitations inherent to Si technology mean

that state-of-the-art Si electronic components cannot meet the demands of HEV platforms to produce smaller, lighter, and cheaper electrical systems.

Besides the great opportunities that GaN-based high-temperature electronics present to HEVs, they also offer important capabilities to aerospace, energy production, and other industrial systems that will affect modern everyday life. The inherent ability of a GaN junction to properly rectify with low reverse leakage current at junction temperatures as high as 600 °C enables power-device operation at higher ambient temperatures. In addition, superior power switching properties of WBG devices are also present at room temperature ambient [118]. Therefore, if remaining technical challenges (e.g. material with low defect density, temperature stable contacts, and reliable packaging technologies) can be overcome, GaN is likely to play a critical role in realizing high-power electronics beyond the capability of Si at all temperatures. For low-power circuits, GaN-based electronics will likely be relegated to the temperature range beyond the reach of silicon-on-insulator (SOI) electronics, which appears to be above 300 °C [130].

High-voltage power rectifiers are key components of inverter modules, which are used in power flow control circuits. Lateral AlGaN-based Schottky rectifiers with spacings of 100 μm between the Schottky and ohmic metal contacts have shown reverse blocking voltages up to 9.7 kV. The figure of merit V_B^2 / R_{on}, where V_B is the reverse breakdown voltage and R_{on} is the on-state resistance, was as high as 270 MW/cm^2 for these devices [136].

1.2.3 Costs and market

The allowable costs depend to a great extent on the application area. For commercial applications it is eminent that cost reduction is the driving force for any material system to survive. To service the wide range of applications discussed in Subsect. 1.2.2, GaN technology must be cost-competitive throughout the range of frequencies presently addressed by Si LDMOS, GaAs MESFET, and InP pHFET. To meet strict cost requirements the technology must be based on a large diameter, low cost substrate material such as Si or HVPE grown bulk GaN. Cost reduction on a system level is feasible because of GaN's high-temperature operation that eliminates the need of bulky cooling units. In addition, GaN devices do not require as much off-chip circuit protection as GaAs transistors hence elimination of these circuits leads to weight and cost savings. Furthermore, the ability of GaN transistors to produce higher power densities not only allows the use of smaller and fewer transistors in total but also the reduction or even elimination of costly linearization circuitry necessary for high-bandwidth wireless systems. It should be noted that these cost requirements stand in strong contrast with military applications which are mainly performance driven.

In 2004, the worldwide GaN device market, which was overwhelmingly dominated by LED sales, was worth $3.2 billion. For the year 2009, Strategies Unlimited estimates this value to be $7.2 billion. It is expected that optical applications will still dominate sales and account for 83% of this amount, leaving 17% to electronic applications such as microwave high-power amplifiers (HPAs) [56].

1.3 State-of-the-art for GaN-based microwave high-power applications

The state-of-the-art values for GaN-based HFETs in literature are very scattered as they depend heavily on substrate type, epitaxial material quality, device layout, and mode of operation i.e. continuous wave (CW) or pulsed. Therefore, we will specify these numbers for the most commonly used substrates for GaN heteroepitaxial growth: sapphire, semi-insulating (s.i.) SiC, and Si. In addition, we will briefly consider single-crystal AlN substrates and provide state-of-the-art values from literature for hybrid and monolithic integrated GaN-based microwave high-power amplifiers.

Sapphire substrate

Traditionally, sapphire is the most commonly used substrate for GaN heteroepitaxy. Sapphire is an interesting choice because it is semi-insulating, it can withstand the required high growth temperatures, and it is relatively cheap ($ 100 for a 2 inch wafer). However, its very low thermal conductivity (0.47 W/cmK at 300 K), large lattice mismatch (13%), and large thermal expansion coefficient (TEC) mismatch (34%) with the GaN epilayers makes it the worst choice for high-power applications. Nevertheless, the power results for GaN HFETs on sapphire substrates are astonishing and are more than 10 times as high as can be achieved by GaAs HFETs. The state-of-the-art values for output power density of small gate periphery devices (typical total gate widths of 100 - 250 μm) with conventional T-shaped submicron gates are about 6.5 W/mm at 8 GHz and 3.3 W/mm at 18 GHz [161]. However, using a field-modulating plate (FP), which is an extension of the top of a conventional T-gate towards the drain contact, has overwhelmingly increased the power density of small devices to 12 W/mm at 4 GHz [30].

SiC substrate

The high thermal conductivity (3.7 - 4.5 W/cmK at 300 K), low lattice mismatch (3.4%), and relatively low TEC mismatch (25%) are the main reasons for the superior material quality of GaN epilayers grown on s.i. SiC compared to those grown on sapphire. As a consequence, the 2DEG transport properties of GaN epilayers on s.i. SiC are much better and it is very clear that at the moment s.i. SiC is the substrate of choice for GaN microwave high-power applications. For small periphery devices with conventional gates state-of-the-art values for output power density are 10 - 12 W/mm at X-band (8.0 - 12.4 GHz) [156, 172]. For small devices with a FP gate, record output power densities of over 30 W/mm at C- (4 GHz - 8 GHz) and X-band have been reported [174].

Si substrate

Despite the very large lattice mismatch (17%) and enormous TEC mismatch (56%), the advantages of low substrate cost, excellent availability of large substrate diameters, acceptable

Table 1.2: Detailed overview of reported state-of-the-art results for small and large gate periphery GaN-based HFETs on sapphire, SiC, and Si substrates and for hybrid and monolithic integrated microwave power amplifiers.

Mat/Amp	f	$L_g \times W_g$	P_{out}	P_D	PAE	G_p	V_{DS}	mode	class	ref.
	(GHz)	(μm)	(W)	(W/mm)	(%)	(dB)	(V)			
sapphire	1.95	0.9 x 32,000	113	3.5	–	6.8	40	pulsed	–	[9]
sapphire	2.0	0.9 x 1,000	2.1	2.1	37.1	16.7	35	CW	–	[9]
sapphire	4.0	0.25 x 150 (FP)	1.8	12.0	58.0	15.0	26	CW	–	[30]
sapphire	8.0	0.15 x 100	0.65	6.5	47.0	15.0	26	CW	–	[161]
sapphire	18.0	0.15 x 100	0.33	3.3	–	–	26	CW	–	[161]
SiC	2.0	1.0 x 1,000	12.0	12.0	48.8	21.2	66	CW	–	[8]
SiC	2.0	0.5 x 4,000	28.4	7.1	76.0	16.1	48	CW	–	[132]
SiC	2.0	0.5 x 48,000	230.0	4.8	67.0	9.5	53	CW	–	[132]
SiC	3.5	0.4 x 250	3.0	12.0	34.0	16.0	90	pulsed	A	[140]
SiC	4.0	0.55 x 246 (FP)	7.9	32.2	54.8	–	120	CW	–	[174]
SiC	8.0	0.55 x 246 (FP)	7.5	30.6	49.6	–	120	CW	–	[174]
SiC	10.0	0.35 x 150 (FP)	2.5	16.5	47.0	16.0	60	CW	AB	[155]
SiC	10.0	0.25 x 1,500	13.8	9.2	33.0	10.0	55	pulsed	–	[179]
SiC	18.0	0.25 x 100	0.67	6.7	26.6	–	35	CW	–	[95]
SiC	26.0	0.25 x 200	1.0	5.0	30.1	5.24	25	CW	–	[102]
SiC	30.0	0.25 x 1,000	5.8	5.8	43.2	9.2	30	CW	–	[65]
SiC	35.0	0.25 x 200	0.83	4.13	23	7.54	30	CW	AB	[101]
Si	2.14	0.7 x 100	1.2	12.0	52.7	15.3	50	CW	AB	[73]
Si	2.14	0.5 x 36,000	55	1.53	–	13.4	28	CW	–	[24]
Si	4.0	0.5 x 100	0.18	1.8	32.0	16.0	30	CW	A	[161]
Si	10.0	0.3 x 200	1.4	7.0	52.0	12.0	40	CW	AB	[43]
Amp	2.0	0.4 x 24,000	102	4.25	54.0	8.0	37	CW	AB	[140]
Amp	10.0	0.4 x 12,000	38	3.2	29.0	8.0	37	CW	AB	[140]
Amp	16.0	0.4 x 6,000	24.2	4.0	22.0	12.8	31	pulsed	AB	[140]

thermal conductivity (1.5 W/cmK at 300 K), and integration possibilities with Si electronics make Si substrates interesting candidates for GaN hetero-epitaxy. Although the epitaxial growth process of GaN on Si differs considerably from the ones on sapphire and s.i. SiC, the current state-of-the-art transistor results level those obtained on sapphire and even those on s.i. SiC. For small gate periphery devices with conventional gates the best reported output power densities are 12 W/mm at 2.14 GHz [73] and 7.0 W/mm at 10 GHz [43], respectively.

AlN substrate

Single-crystal aluminum nitride (AlN) substrates are possibly the best candidates for the heteroepitaxial growth of GaN epilayers because they have the same structure (wurtzite), high thermal conductivity (2.85 - 3.2 W/cmK at 300 K), high electrical resistivity (10^7 - 10^{13} Ωcm) [106], and their lattice mismatch (2.4 %) and TEC mismatch (approximately 5.2 % from RT up to 1000 °C) are very low. As a result of the last two properties, the defect density of GaN epilayers on AlN substrates is on the order of 10^3 - 10^4 cm^{-2} for 2 inch substrates [55], which is about four to five orders of magnitude lower than that of layers grown on 2 inch s.i. SiC substrates. It should be noted that the growth of high-quality large diameter bulk AlN substrates has proven to be very complicated. Only since early 2006, the US-based company Crystal IS has made 2 inch single-crystal AlN substrates available for the first time [55]. First AlGaN/GaN HFETs fabricated on small AlN substrates have shown DC current-voltage characteristics comparable to those fabricated on s.i. SiC [62].

Hybrid and monolithic integrated microwave high-power amplifiers

The majority of GaN-based high-power amplifiers that has been shown up to now is hybrid in nature. This means that the passive circuits needed for matching, biasing, and stabilization of the transistors are fabricated on a different substrate, which is connected to the active substrate by e.g. wire/ribbon bonding or flip-chip technology. It has to be noted that the GaN-based microwave monolithic integrated circuits (MMICs) are exclusively fabricated on SiC as substrate material. Table 1.2 provides a more detailed overview of reported state-of-the-art power results for small and large gate periphery GaN-based HFETs on sapphire, SiC, and Si substrates and for hybrid and monolithic integrated microwave power amplifiers.

1.4 Objectives of this research

The research described in this thesis has been carried out within a joint project between the Radboud Universiteit Nijmegen (RU) and the Technische Universiteit Eindhoven (TU/e) with the title: “Performance enhancement of GaN-based microwave power amplifiers: material, device and design issues”. This project has been granted by the Dutch Technology Foundation STW under projectnumber NAF5040. As pointed out in Sect. 1.3 a lot of research is ongoing in the development of GaN-based device technology. Publications in literature however very rarely reveal technological details with respect to material growth and device processing. Instead they are mainly concerned with general concepts regarding these issues and reporting

of device results. Therefore, the aims of this project have been to develop the technology required to grow state-of-the-art AlGaN/GaN epilayers on sapphire and s.i. SiC substrates by using metal organic chemical vapor deposition (MOCVD) and to fabricate microwave high-power heterostructure field-effect transistors (HFETs) on these epitaxial films.

AlGaN/GaN HFETs have been chosen over GaN MESFETs because of the superior transport properties (high values for μ_n and v_{sat}) of electrons in a potential well at the heterojunction compared to those in bulk GaN material. As a result, HFETs show much higher saturated drain currents and transconductance, which makes them the preferred choice for microwave high-power device applications. A difference between AlGaN/GaN HBTs and AlGaN/GaN HFETs is the fact that HBTs are vertical devices and HFETs are lateral devices. Because of the extremely high dislocation densities in GaN-based epilayers (typically 10^8 cm^{-2}), which are in the vertical direction, it is very hard to achieve high breakdown voltages. Furthermore, as HBTs are bipolar devices they require p-type doped GaN base layers. Both efficient p-type doping of GaN epilayers and the fabrication of high-quality ohmic contacts on these layers are still quite challenging.

MOCVD growth of AlGaN/GaN epilayers and material characterization has been done within the group Applied Materials Science (AMS) of RU. Research at the Opto-Electronic Devices group (OED) of TU/e has focused on electrical characterization of AlGaN/GaN epilayers and design, process technology development, and characterization of GaN-based HFETs and CPW passive components. Although a considerable amount of work has been done during this research with respect to processing of CPW passive components on s.i. SiC substrates, this thesis will focus on active AlGaN/GaN devices only. In the following paragraphs we will give a summary of our work on CPW passive components and provide references for further details.

To realize a microwave high-power amplifier (HPA), passive components are required for impedance matching and stabilization of the transistors used and to provide the bias voltages to fix their operating points. The implementation, i.e. surface mounted device (SMD), microstrip, or coplanar waveguide (CPW), of these passive components depends among others on the frequency at which the application has to operate, and substrate material used. For operation frequencies at X-band, SMD components cannot be used as their dimensions are larger or comparable to the signal wavelength and hence cannot be considered as lumped components. For a microstrip implementation a through-substrate via hole technique is required to connect the ground planes on the top and bottom of the carrier substrate. If a through-substrate via hole cannot be realized, and if an SMD solution is not an option, CPW is the only way to implement passive components.

AlGaN/GaN epilayers on s.i. SiC are an excellent candidate for implementation of a monolithic integrated HPA, i.e. active and passive components are realized on the same carrier substrate. However, this material was not available in the early stages of this project and the choice was made to first concentrate on a hybrid integration scheme consisting of AlGaN/GaN HFETs on sapphire substrates and CPW passive components on ceramic AlN. The latter substrate material has been chosen for its excellent thermal and electric properties. Within a collaboration between TNO Defence, Security and Safety, and TU/e a significant research effort has been made towards the process development and the extraction of scalable models for a CPW com-

ponent library consisting of transmission lines (TLs), discontinuities (e.g. 90^{o} bends, tees, crosses), metal-insulator-metal (MIM) capacitors, and thin-film nickel chromium (NiCr) resistors [67]. After establishing the CPW technology on ceramic AlN, we have transferred it onto s.i. SiC substrates. The process flow for CPW passive components on these substrates is described in Appendix B. TNO has created a component model library based on measurements of components on s.i. SiC using this process flow. As a detailed description of these measurement and modeling results is beyond the scope of this thesis, we refer to project reports for additional information on these matters [145].

1.5 Thesis organization

This thesis is organized in the following way. Chapter 2 describes the GaN material system and focuses on several key topics concerning GaN-based HFETs. Chapter 3 deals with design aspects of microwave high-power AlGaN/GaN HFETs on both sapphire and s.i. SiC substrates. Chapter 4 is concerned with the development of the process technology required for the fabrication of microwave high-power transistors. Chapter 5 focuses on the optimization of the silicon nitride (SiN) film used for device passivation. Chapter 6 discusses the characterization of small and large periphery transistors and presents microwave power results of HFETs fabricated on n.i.d. AlGaN/GaN:Fe epilayers on s.i. SiC. Finally, Chapter 7 provides a review of the main conclusions that can be drawn from the work described in this thesis and provides recommendations for future research.

Chapter 2

GaN-based heterostructure field-effect transistors

The invention of the idea of the heterostructure field-effect transistor (HFET) in 1979 is claimed by Takashi Mimura of the Japanese Fujitsu Laboratories. This device utilizes the enhanced mobility of electrons that move parallel to a heterojunction in a so-called two-dimensional electron gas (2DEG). The physics of this kind of carrier transport was first considered in 1969 by Esaki and Tsu at IBM Research [44]. The enhanced mobility effect was first demonstrated in $Al_xGa_{1-x}As$/GaAs heterojunctions in 1979 by Dingle at Bell Laboratories [42] and applied to demonstrate a HFET in 1980 by Mimura and Delagebeaudeuf [40, 121]. Enhanced electron mobility at an $Al_xGa_{1-x}N$/GaN heterojunction was first reported by M. Asif Khan in 1991 [84]. In 1994, Khan et al. demonstrated the excellent potential of $Al_xGa_{1-x}N$/GaN HFETs for microwave electronics [82].

2.1 Introduction

GaN-based heterojunction field-effect transistors (HFETs) on sapphire and SiC substrates for microwave high-power applications are the subject of interest in this chapter. HFETs are also known as high electron mobility transistors (HEMTs), modulation-doped field-effect transistors (MODFETs), two-dimensional electron gas field-effect transistors (TEGFETs), and selectively doped heterostructure transistors (SDHTs). All these names have in common that they refer to the unique channel formation and resulting enhanced electron transport properties observed in this kind of field-effect transistors.

The basic layer stack of these devices consists of a highly doped wider bandgap material grown on top of a non-intentionally doped (n.i.d.) narrower bandgap material. Figure 2.1

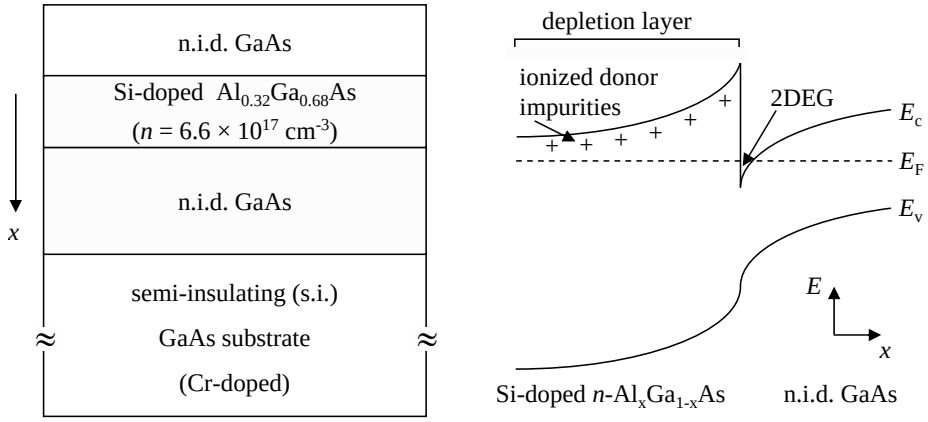

Figure 2.1: Schematic cross section of the original $Al_xGa_{1-x}As$/GaAs HFET and the corresponding energy band diagram [121].

shows a schematic cross section of the original $Al_xGa_{1-x}As$/GaAs, hereafter indicated as AlGaAs/GaAs, HFET and the corresponding energy band diagram after Mimura [121]. The always present conducting channel in these devices, which are referred to as normally-on, consists of electrons from the highly doped wider bandgap material that have accumulated in the quantum well, which resides in the narrower bandgap material near the heterojunction. As this quantum well is confined in the direction perpendicular to the heterojunction, quantum mechanics dictates that the energy levels in this spatial direction are discrete. However, the electrons are still allowed to move freely in the plane parallel to the heterojunction. Hence, the electrons in the quantum well are usually referred to as a two-dimensional electron gas (2DEG). These electrons show enhanced mobility due to significantly reduced Coulomb scattering as they are separated from the ionized donor atoms in the highly doped material from which they stem. In addition, mobility is further enhanced because of strongly reduced impurity scattering as the quantum well resides in the n.i.d. material. Enhanced electron mobility is the key feature that differentiates HFETs from ordinary FETs.

This chapter starts with a description of the GaN material system. We will give an overview of the crystal structure and the unique polarization effects in III-nitride crystals. Next, we will discuss some key topics concerning GaN-based HFETs. We will start with the most important material growth techniques followed by different HFET layer structures. After describing the theory of 2DEG formation we will end this chapter with an explanation of two major charge trapping effects in GaN-based HFETs that severely deteriorate their microwave high-power performance.

2.2 GaN material system

2.2.1 Crystal structure

The group III-nitrides AlN, GaN, and InN can crystallize in the following three crystal structures: wurtzite, zinc-blende, and rock-salt. However, at ambient conditions the wurtzite structure is the thermodynamically stable phase consisting of two interpenetrating hexagonal close-packed lattices, which are shifted with respect to each other ideally by $3/8 \cdot c_0$ [135], where c_0 is the height of the hexagonal lattice cell as shown in Fig. 2.2. The chemical bonds of III-nitride compounds such as GaN are predominantly covalent, which means that each atom is tetrahedrally bonded to four atoms of the other type. Because of the large difference in electronegativity of Ga and N atoms, there is a significant ionic contribution to the bond which determines the stability of the respective structural phase. The unit cell of the wurtzite lattice is hexagonal with a basis of four atoms, two of each kind. There is no inversion symmetry in this lattice along the [0001] direction or c-axis, which by convention is the direction shown by a vector pointing from a Ga atom to the nearest neighbor N atom. Lack of inversion symmetry means that, when defining an atom position on a close-packed plane with coordinates (x, y, z) it is not invariant to the position $(-x, -y, -z)$ since inversion results in replacement of group III atoms by nitrogen atoms and vice versa. As a result of the lack of inversion symmetry all atoms on the same plane at each side of a bond are the same. Hence, wurtzite GaN crystals have two distinct faces, commonly known as Ga-face and N-face, which correspond to the (0001) and $(000\bar{1})$ crystalline faces. Figure 2.2 shows the atomic arrangement in Ga-face GaN crystals. For N-face material this can be obtained by flipping the Ga-face material upside-down. It has to be noted that for Ga-face material the N atom is stacked directly over the Ga atom and vice versa for N-face.

Figure 2.2 also shows the three parameters that define the wurtzite lattice. These are the edge length of the basal hexagon (a_0), the height of the hexagonal lattice cell (c_0), and the cation-anion bond length ratio (u_0) along the [0001] direction in units of c_0. The subscript "0" indicates that these values are those of the equilibrium lattice. In an ideal wurtzite crystal the c_0/a_0 ratio equals $\sqrt{\frac{8}{3}} = 1.633$ and the value for u_0 is 0.375 [135]. Because of the different metal cations, the bond lengths and the resultant c_0/a_0 ratios of AlN, GaN, and InN are different. Table 2.1 shows an overview of these lattice parameters of wurtzite III-nitrides at 300 K [16].

From Tab. 2.1 it is clear that GaN is closest to the ideal wurtzite structure, followed by InN and AlN. This fact is very important because the degree of non-ideality is a significant factor in determining the strength of polarization in III-nitrides.

2.2.2 Polarization effects in III-nitrides

The involvement of nitrogen, which is the smallest and the most electronegative Group V element, makes the III-nitrides special among the other III-V compounds as this has a strong effect on their properties. Because of the $1s^2 2s^2 2p^3$ electronic configuration of the N atom, or rather the lack of electrons occupying the outer orbitals, the electrons involved in the metal-nitrogen covalent bond will be strongly attracted by the Coulomb potential of the N atomic

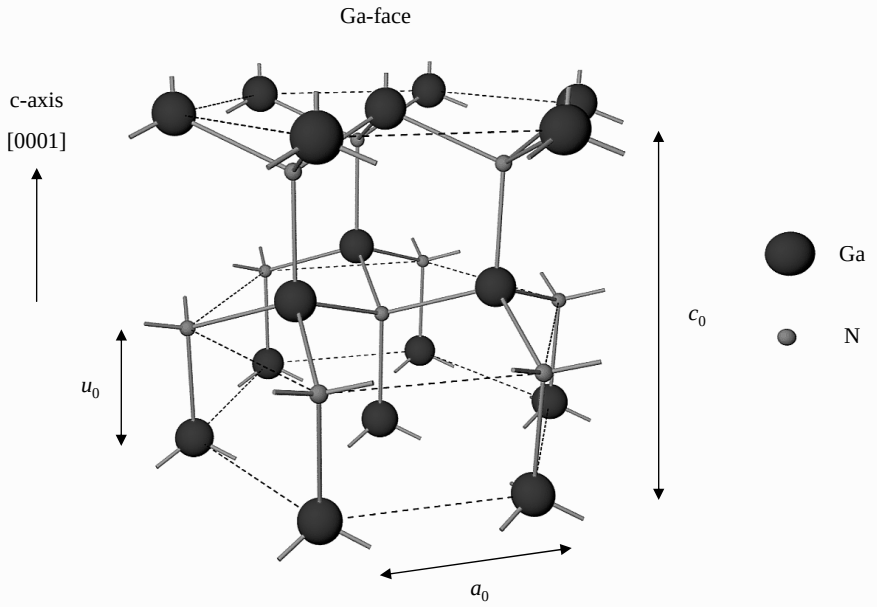

Figure 2.2: Atomic arrangement in Ga-face GaN crystals.

Table 2.1: Lattice parameters of wurtzite III-nitrides at 300 K [16].

parameter	ideal	AlN	GaN	InN
a_0 (Å)	–	3.112	3.189	3.54
c_0 (Å)	–	4.982	5.185	5.705
c_0/a_0 (exp.)	–	1.6010	1.6259	1.6116
c_0/a_0 (cal.)	1.633	1.6190	1.6336	1.6270
u_0	0.375	0.380	0.376	0.377

Table 2.2: Influence of lattice non-ideality on the value of spontaneous polarization in III-nitrides [16]

parameter	ideal	AlN	GaN	InN
c_0/a_0	1.633	1.6010	1.6259	1.6116
P_{SP} (C/m^2)	–	-0.081	-0.029	-0.032

nucleus. This means that this covalent bond will have stronger ionicity compared to other III-V covalent bonds. This ionicity, which is a microscopic polarization, will result in a macroscopic polarization if the crystal lacks inversion symmetry.

As mentioned in Sect. 2.2.1, the wurtzite III-nitrides do not have inversion symmetry along the [0001] direction. This fact in combination with the strong ionicity of the metal-nitrogen bond results in a strong macroscopic polarization along the [0001] direction. Although this effect also exists in the [111] direction of zinc-blende crystals such as GaAs and InP, it is much less pronounced because of the smaller ionicity of the covalent bond. Since this polarization effect occurs in the equilibrium lattice of III-nitrides at zero strain, it is called spontaneous polarization [16].

In addition to the ionicity of the covalent bond, the degree of non-ideality of the crystal lattice also affects the strength of spontaneous polarization. In III-nitrides, although the covalent bond parallel to the c-axis is strongly ionic and is primarily responsible for the spontaneous polarization, the other three covalent bonds in the tetrahedral structure are also equally ionic. The resultant polarization from these other three bonds is actually aligned in the opposite direction and serves to counteract the polarization of the other bond. As the c_0/a_0 ratio decreases, c_0 decreases and a_0 increases, these three covalent bonds will be at a wider angle from the c-axis and their resultant compensation polarization will decrease. As a result the macroscopic spontaneous polarization will increase. Table 2.2 shows the c_0/a_0 ratio and the spontaneous polarization for AlN, GaN, and InN. It can be seen that as the lattice non-ideality increases, c_0/a_0 ratio moves away from 1.633 of the ideal lattice, the value of spontaneous polarization (P_{SP}) increases from GaN to InN to AlN [16].

If the ideality of the III-nitride lattices is changed externally, then due to the strong ionicity of the metal-nitrogen covalent bond there will be large changes in the polarization of the crystal. One way to change the ideality of the crystal lattice is through strain. If stress is applied to the III-nitride lattice, the ideal lattice parameters c_0 and a_0 of the crystal structure will change to accommodate the stress. Hence, the polarization strength will be changed. This additional polarization in strained III-nitride crystals is called piezoelectric polarization [16]. For example, if the nitride crystal is under biaxial compressive stress, the in-plane lattice constant a_0 will decrease and the vertical lattice constant c_0 will increase. Hence, the c_0/a_0 ratio will increase towards 1.633 of the ideal lattice and the total polarization strength of the crystal will decrease because the piezoelectric and spontaneous polarizations will act in the opposite directions. It is clear that if tensile stress is applied to the crystal, the total polarization will increase because

the piezoelectric and spontaneous polarizations in that case act in the same direction.

According to Bernardini *et al.* [16], the strength of piezoelectric polarization (P_{PE}) can be calculated with the piezoelectric coefficients e_{33} and e_{31} as

$$P_{\mathrm{PE}} = e_{33} \cdot \varepsilon_{\mathrm{z}} + e_{31} \cdot (\varepsilon_{\mathrm{x}} + \varepsilon_{\mathrm{y}}), \tag{2.1}$$

where $\varepsilon_{\mathrm{z}} = (c - c_0)/c_0$ is the strain along the c-axis, and the in-plane strain $\varepsilon_{\mathrm{x}} = \varepsilon_{\mathrm{y}} = (a - a_0)/a_0$ is assumed to be isotropic, with a_0 and c_0 being the equilibrium lattice constants. The different strains in the lattice are related as in [16]

$$\varepsilon_{\mathrm{z}} = -2 \cdot \frac{C_{13}}{C_{33}} \cdot \varepsilon_{\mathrm{x}}, \tag{2.2}$$

where C_{13} and C_{33} are elastic constants. Equations (2.1) and (2.2) can be combined to obtain the following equation

$$P_{\mathrm{PE}} = 2 \cdot \frac{a - a_0}{a_0} \cdot \left[e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}} \right]. \tag{2.3}$$

Since in the wurtzite III-nitrides the piezoelectric coefficient e_{31} is always negative while e_{33}, C_{13}, and C_{33} are always positive, it turns out that $(e_{31} - e_{33} \cdot C_{13}/C_{33})$ will always be negative [16, 135]. As a consequence, the value of piezoelectric polarization (P_{PE}) in III-nitrides is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). As spontaneous polarization in III-nitrides is always negative, it can be concluded that for layers under tensile stress, spontaneous and piezoelectric polarizations are parallel to each other, and for layers under compressive stress the two polarizations are anti-parallel. Figure 2.3 shows the directions of the spontaneous and piezoelectric polarization vectors for an undoped Ga-face $\mathrm{Al_xGa_{1-x}N/GaN}$, hereafter indicated as AlGaN/GaN, heterostructure where the AlGaN layer is under tensile stress. We will consider this heterostructure in more detail in Sect. 2.3.2. Furthermore, it has to be noted that we only consider the heterojunction at which the 2DEG is formed.

2.3 Key topics concerning GaN-based HFETs

This section starts with a brief summary of the most important techniques for GaN epitaxy. This is followed by a discussion of HFET layer structures and the theory of 2DEG formation in GaN-based HFETs. Finally, we will give an overview of trapping effects in these devices that severely deteriorate their microwave high-power performance.

2.3.1 Growth techniques

As mentioned in Sect 1.3, the lack of a lattice and thermally matched substrate forces to use heteroepitaxy on lattice and thermally mismatched substrates such as sapphire, SiC, or Si. We will briefly discuss the most commonly used growth techniques: hydride vapor phase epitaxy

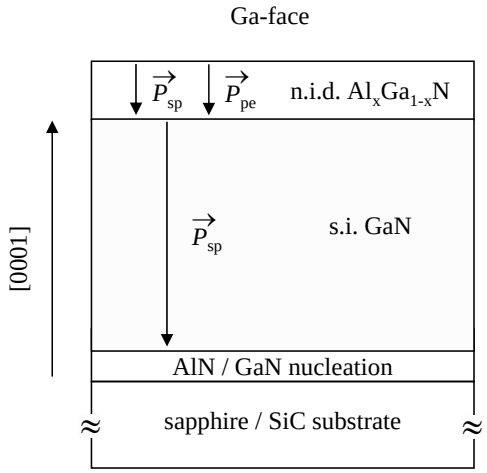

Figure 2.3: Directions of the spontaneous and piezoelectric polarization vectors for an undoped Ga-face AlGaN/GaN heterostructure where the AlGaN layer is under tensile stress.

(HVPE), metal organic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE).

HVPE

Historically, hydride vapor phase epitaxy (HVPE) and its closely related technique, halide vapor phase epitaxy, have played an important role in the development of semiconductor material systems. It was the first [116] and until the early 1980s the most popular method to grow epitaxial GaN layers [182]. This technique is a chemical vapor phase deposition method, which is usually carried out in a hot wall reactor. The gallium monochloride (GaCl) precursor is synthesized within the reactor by the reaction of hydrochloric acid (HCl) with liquid Ga at temperatures between 750 °C and 900 °C. The GaCl is then transported to the usually foreign substrate, e.g. sapphire, Si, GaAs, or SiC, where it reacts with ammonia (NH_3) at 900 °C-1100 °C to form GaN. After the growth process the foreign substrate can be removed by techniques such as laser ablation. The GaN growth process can be described by the following two-step reactions [14]

$$2\mathrm{Ga(l)} + 2\mathrm{HCl(g)} \rightarrow 2\mathrm{GaCl(g)} + \mathrm{H_2(g)}, \text{ and} \tag{2.4}$$

$$\mathrm{GaCl(g)} + \mathrm{NH_3(g)} \rightarrow \mathrm{GaN(s)} + \mathrm{HCl(g)} + \mathrm{H_2(g)}. \tag{2.5}$$

HVPE is a high-growth-rate technique (typically 100 μm/hr), which has the potential to facilitate large area, thick, and low defect density GaN quasi-substrates for subsequent growth by

MOCVD or MBE.

MOCVD

To date, metal organic chemical vapor deposition (MOCVD) is the workhorse for the growth of GaN and related materials. Manasevit *et al.* applied this technique for the deposition of GaN and AlN in 1971 [112]. Using trimethylgallium (TMG) and NH_3 as source gases for Groups III and V species, respectively, they obtained *c*-axis oriented films on sapphire (0001) and on 6H-SiC (0001) substrates. In the MOCVD process, substrate temperatures well in excess of 900 °C are required to obtain single crystalline high-quality GaN layers. GaN films with the best electrical and optical properties are grown at 1050 °C or even higher [142]. These high growth temperatures require that the used substrates do not decompose. Sapphire, SiC, Si, and AlN are among those that meet this criterion. In addition, metalalkyls must be kept below pyrolysis temperature and should be kept separate from NH_3 until just before the reaction zone to minimize predeposition reactions. The MOCVD process is also characterized by a low growth rate (typically 1-2 μm/hr) and a high N/Ga (V/III) flux ratio. The former enables the controllable growth of abrupt junctions whereas the latter is used to minimize nitrogen loss. The high growth temperatures have a contradictory effect on the crystal quality. On the one hand, because of the higher surface mobility of the atoms the grown films are of better quality. On the other hand, high vapor pressure of N over Ga brings the growth process very close to the dissociation temperature. Also, post-growth cooling introduces more strain and thus more structural defects may be introduced during cooling.

It is well established that two pretreatment steps are essential to obtain high-quality MOCVD GaN films on sapphire substrates: a high temperature nitridation of the sapphire surface [77, 122, 159] and the deposition of a low-temperature buffer layer [5, 125, 166]. The nitridation of sapphire was found to result in the formation of a relaxed AlN layer [159], which acts subsequently as a buffer layer. The mechanism of this layer was studied by Amano *et al.* [5]. The essential role of the low-temperature buffer layer is to supply nucleation centers having the same orientations as the substrate and to promote lateral growth of the GaN film due to the decrease in the interfacial free energy between the film and the substrate [182]. In the case of a SiC substrate, efficient surface wetting can only be achieved by using an AlN layer. To avoid confusion later on with the high-temperature GaN buffer layer in HFET layer stacks, we will from now on refer to the former AlN and the latter low-temperature layers as nucleation layers.

In Sect. 2.2.1 we have seen that III-nitrides have either Ga-face or N-face structure. It has been observed that III-nitride films grown by MOCVD are almost always Ga-face irrespective of the growth conditions or the nature of the intervening layers [142].

MBE

Molecular beam epitaxy (MBE) of GaN layers is slow (typically 1 μm/hr, or slightly more than one monolayer per second) and tedious due to a variety of reasons such as finding a suitable nitrogen source since NH_3 is very stable at the lower temperatures (500 °C-900 °C) that are common for MBE growth. To avoid this problem, reactive species of nitrogen, generated by

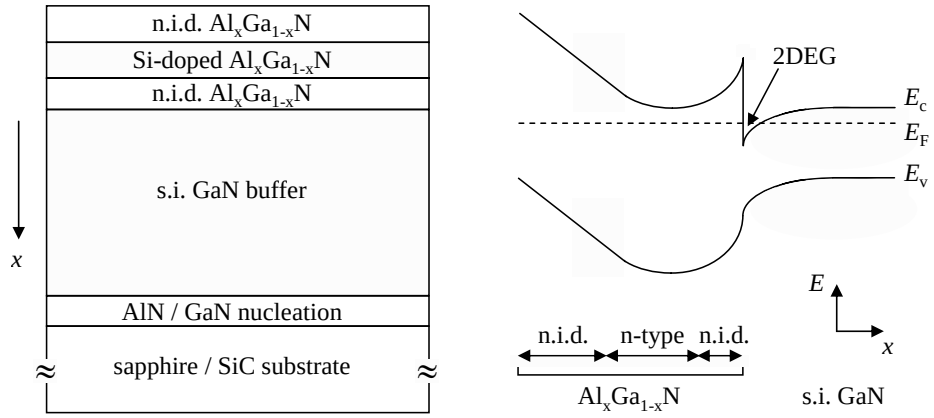

Figure 2.4: Schematic cross section of a basic Ga-face doped AlGaN/GaN HFET structure and the corresponding energy band diagram.

electron cyclotron resonance (ECR) or radio frequency (RF) plasmas with low energy, are generally used. In addition to the problem of the nitrogen source, the intrinsic problem of MBE growth is that it is carried out far from thermodynamic equilibrium. Hence it is primarily governed by the kinetics of the surface processes that occur when the impinging beam reacts with the outermost layer of the substrate crystal [142]. This is in contrast with the other epitaxial growth techniques HVPE and MOCVD, which proceed at conditions near thermodynamic equilibrium and are therefore most frequently controlled by diffusion processes occurring in the crystallizing phase near the substrate. Despite of these difficulties, MBE grown GaN layers of comparable material quality to those grown by MOCVD have been shown. This is especially true if MOCVD or HVPE grown GaN templates are used for further MBE growth.

Contrary to what has been observed for MOCVD grown GaN-based films, growth by MBE can result in either Ga-face or N-face material depending on the nature of the nucleation layer. For growth on sapphire it has been shown that a low-temperature GaN nucleation layer will result in an N-face crystal and the use of a high-temperature AlN nucleation layer yields Ga-face epilayers.

2.3.2 GaN-based HFET layer structures

The first AlGaN/GaN HFET structures consisted of an identical layer sequence as the original AlGaAs/GaAs HFET structures described in Sect. 6.1. Figure 2.4 shows a schematic cross section of a basic Ga-face doped AlGaN/GaN HFET structure and the corresponding energy band diagram.

The most pronounced differences in the case of GaN-based epitaxy are of course the for-

eign substrates and the use of a nucleation layer. As in the case of AlGaAs/GaAs the GaN buffer layer should be semi-insulating (s.i.) to provide good electrical isolation between active devices when used in an integrated circuit (IC). Without the application of advanced growth steps such as lateral epitaxial overgrowth (LEO) the dislocation densities of GaN buffer layers on sapphire and SiC substrates are very high, typically 10^8 - 10^{10} cm^{-2} [3, 142]. These very high dislocation densities can act as recombination and trapping centers which cause a serious threat to device performance and reliability. Nevertheless, s.i. GaN buffers can for example be achieved by compensation doping using e.g. iron (Fe) atoms. Reported resistivity values of such buffer layers are in excess of 10^8 Ωcm [142]. The highly Si-doped (typically, n = 1.0 x 10^{19} cm^{-3}) AlGaN layer is used to supply sufficient electrons to the 2DEG. Between this supply layer and the s.i. GaN buffer layer a thin (typically 3 nm) n.i.d. AlGaN layer usually with the same Al alloy composition as the supply layer is inserted. This so-called spacer layer strongly decreases Coulomb scattering between the 2DEG electrons and their ionized parent atoms in the supply layer. Hence the mobility of the 2DEG electrons is significantly increased to typical values ranging from 1200 - 2000 cm^2/Vs at room temperature (RT). The n.i.d. AlGaN capping layer is used to improve the performance of the Schottky gate contact as it is impossible to realize a properly rectifying control electrode on highly doped semiconductor material.

In Sect. 2.2.2 we mentioned the much stronger spontaneous polarization in III-nitrides compared to other III-V semiconductors because of the involvement of nitrogen as the Group V element. If we consider a Ga-face AlGaN/GaN HFET structure in which the AlGaN layer is under tensile stress, the polarization fields in the AlGaN and GaN layers are parallel and pointing towards the substrate as shown in Fig. 2.3. As we will see in Sect. 2.3.3, a gradient in the polarization field ($\vec{P}$) at the AlGaN/GaN heterojunction induces a bound sheet charge. To maintain charge neutrality, this induced bound sheet charge has to be compensated by mobile charge. We will see that in the case of a Ga-face AlGaN/GaN HFET structure the induced bound charge is positive. Hence, free electrons accumulate in the quantum well on the GaN side of the heterojunction forming a 2DEG. Figure 2.5 shows a schematic cross section of a basic Ga-face undoped AlGaN/GaN HFET structure and the corresponding energy band diagram.

It has been shown that even in the case of un undoped AlGaN layer, 2DEG sheet charge densities in excess of 10^{13} cm^{-2} can be achieved [6]. These values are ten times higher than the sheet charge densities obtained in impurity doped AlGaAs/GaAs HFETs. The so-called piezoelectric induced 2DEG formation in undoped AlGaN/GaN heterostructures is typical for the III-nitrides. The omission of impurity doping has several advantages such as increased breakdown voltage due to reduced gate leakage currents. However, some serious disadvantages arise in these structures as they are very sensitive for trapping and de-trapping phenomena at the AlGaN barrier layer as the donor resides on this surface. We will elaborate on this matter in Sect. 2.3.4.

In Sect. 2.2.1 we have explained the Ga- and N-faces of wurtzite GaN crystals. These different polarities have different properties that affect both device technology and performance. Although N-face crystals have lower dislocation density and are chemically active, which enables wet-chemical etching of the material, these layers suffer from a very rough

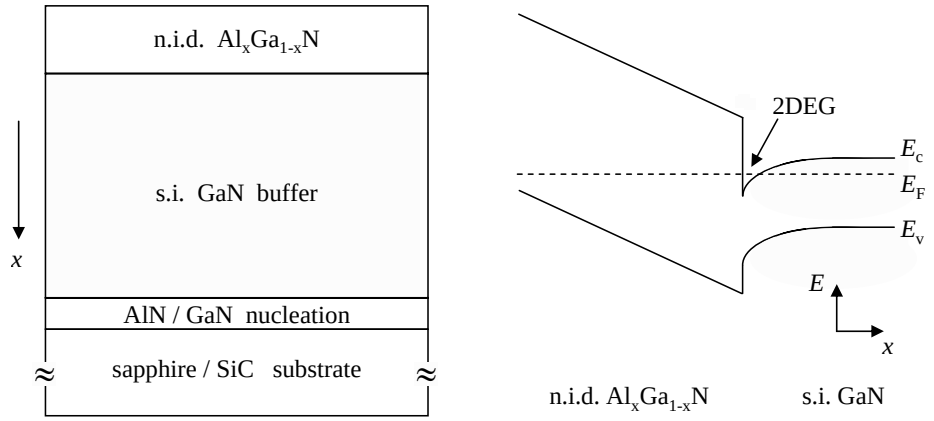

Figure 2.5: Schematic cross section of a basic Ga-face undoped AlGaN/GaN HFET structure and the corresponding energy band diagram.

surface morphology and high background doping concentration. Ga-face crystals have much smoother surface morphology and lower background doping concentration, which is beneficial for buffer resistivity and electrical isolation of integrated devices, but this material is almost chemically inert. Consequently, with respect to device processing it can only be etched conveniently using plasma etching techniques such as reactive ion etching (RIE), inductively coupled plasma etching (ICP), chemically assisted ion beam etching (CAIBE), or electron cyclotron resonance etching (ECR). Despite this difficulty with respect to processing technology, Ga-face crystals have superior electron transport properties and are therefore almost exclusively used for device work [7]. The experimental work described in this thesis is based on Ga-face AlGaN/GaN HFET structures only and we will therefore constrict the discussion to Ga-face crystals after Sect. 2.3.3 in which the 2DEG formation in both Ga- and N-face crystals will be explained.

2.3.3 Theory of 2DEG formation in GaN-based HFETs

We will use the polarization effects in III-nitrides as described in Sect. 2.2.2 to explain the formation of the 2DEG and the difference in its position for Ga-face and N-face materials. We have seen that nitride epilayers under stress exhibit both spontaneous and piezoelectric polarization fields. In general, if the polarization field ($\vec{P}$) changes in space, there will be a bound charge density (ρ) associated with it which is given by

$$\rho = -\vec{\nabla} \cdot \vec{P}. \tag{2.6}$$

For wurtzite III-nitrides polarization is always directed along the *c*-axis, perpendicular to the

Table 2.3: Values for lattice parameters, piezoelectric constants, elasticity constants, and spontaneous polarization for GaN and AlN [6, 16]

parameter	AlN	GaN
a_0 (Å)	3.112	3.189
e_{31} (C/m^2)	-0.60	-0.49
e_{33} (C/m^2)	1.46	0.73
C_{13} (GPa)	108	103
C_{33} (GPa)	373	405
P_{SP} (C/m^2)	-0.081	-0.029

heterostructure interface. Hence, at the heterojunction, which is assumed to be planar and abrupt a bound sheet charge (σ_{int}) will be formed that is given by [7]

$$\sigma_{int} = P_{tot,layer1} - P_{tot,layer2} = (P_{SP} + P_{PE})_{layer1} - (P_{SP} + P_{PE})_{layer2}. \tag{2.7}$$

In reality, heterojunctions are rarely totally abrupt due to interface roughness or an unintentional composition gradient. However, as long as the gradient of the heterojunction is not over a large distance (e.g. > 20 Å), a sheet density (σ) given by equation 2.7 is a quite good approximation. This bound charge, which is induced by a change in polarization of the two layers, will attract compensating mobile charge at the interface. If the bound charge is positive it will cause a negative mobile sheet charge and vice versa. Baring this in mind we will focus on the calculation of bound charge and the corresponding 2DEG density in a Ga-face undoped AlGaN/GaN heterojunction as shown in Fig. 2.5.

To calculate the amount of bound sheet charge at an abrupt undoped AlGaN/GaN heterojunction we need to know the physical properties of the AlGaN barrier layer as a function of its aluminum (Al) mole fraction (x). Table 2.3 gives the values for the lattice parameters, piezoelectric constants, elasticity constants, and spontaneous polarization for GaN and AlN [6, 16].

It has to be noted that the GaN buffer layer in the structure shown in Fig. 2.5 is relaxed and therefore only has spontaneous polarization. The AlGaN barrier layer however is tensile strained and therefore has both spontaneous and piezoelectric polarization. Using equations (2.1) - (2.3), and (2.7) the bound sheet charge at the AlGaN/GaN interface is given by

$$\begin{aligned} \sigma_{int} &= (P_{SP})_{GaN} - (P_{SP} + P_{PE})_{AlGaN} \\ &= P_{SP}(0) - P_{SP}(x) - 2 \cdot \tfrac{a(0)-a(x)}{a(x)} \cdot \left[e_{31}(x) - e_{33}(x) \cdot \tfrac{C_{13}(x)}{C_{33}(x)} \right]. \end{aligned} \tag{2.8}$$

Using Vegard's law for interpolation between the values of the parameters of AlN and GaN given in table 2.3, σ_{int} can be calculated for any Al alloy composition. Figure 2.6 shows the total polarization induced bound sheet charge, which equals the sum of the charge densities induced by the spontaneous and piezoelectric polarization components, as a function of the

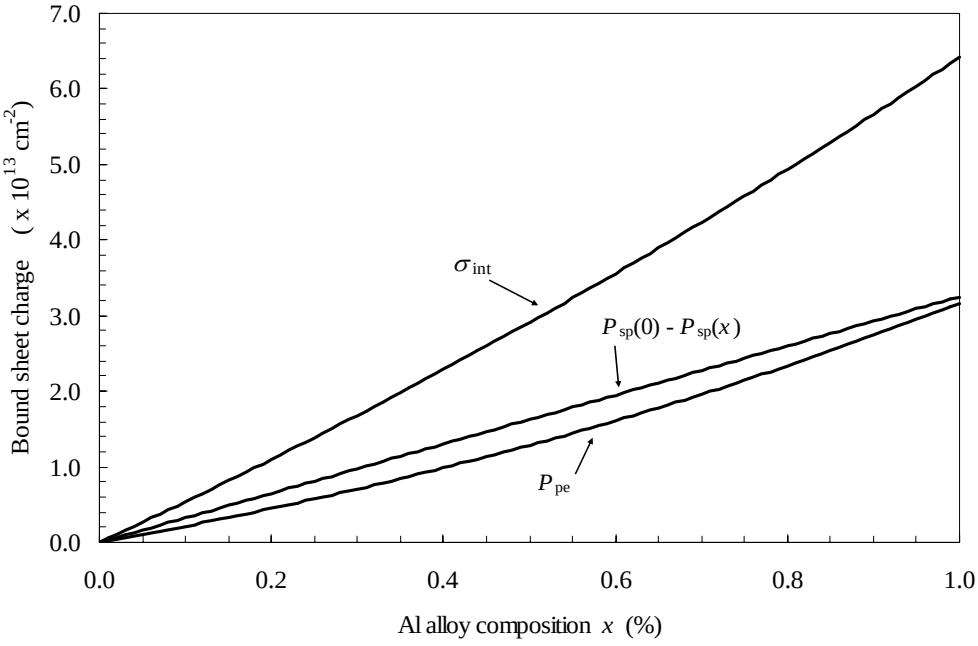

Figure 2.6: Polarization induced bound sheet charge at AlGaN/GaN interface as a function of Al alloy composition of the AlGaN barrier layer for Ga-face undoped material.

Al alloy composition of the undoped AlGaN barrier layer. It can clearly be seen that both polarizations significantly contribute to the total sheet charge over the entire range of Al alloy composition.

The positive polarization induced bound sheet charge shown in Fig. 2.6 is characteristic for an AlGaN layer grown on top of a Ga-face GaN buffer. If another GaN layer is grown on top of the AlGaN barrier layer, this top GaN/AlGaN interface will have exactly opposite change in polarization in relation to the bottom interface. Hence, the polarization induced bound sheet charge at this upper heterojunction will be negative. For N-face material the polarization vectors will be pointing in the reverse direction (along the [0001] direction, away from the substrate), which means that the sign of the bound charge at the AlGaN/GaN and GaN/AlGaN interfaces will be reversed compared to the Ga-face material. The formation of bound charge at the heterointerfaces for both Ga-face and N-face materials is summarized in Fig. 2.7.

For the calculation of the 2DEG density we will again focus on the Ga-face undoped AlGaN/GaN structure shown in Fig. 2.5. To calculate the 2DEG density it is important to know the value of the surface barrier height. In the case of a bare surface this value can be determined using sophisticated measurements such as the Kelvin probe technique. In GaN-based HFETs however, the gate metal forms a Schottky barrier with the AlGaN barrier layer, which

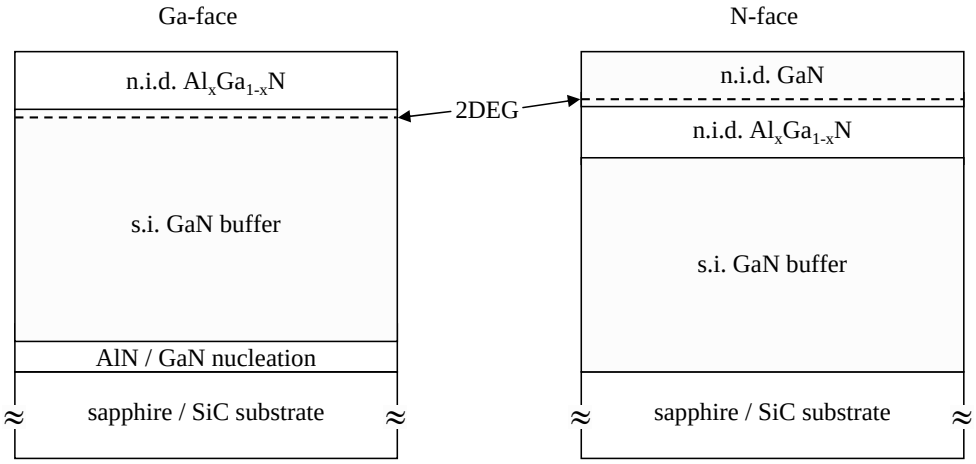

Figure 2.7: Formation of bound sheet charge at AlGaN/GaN and GaN/AlGaN interfaces for Ga-face and N-face materials.

can be measured easily by a variety of techniques such as capacitance-voltage measurements. Figure 2.8 again shows the energy band diagram of a Ga-face undoped AlGaN/GaN heterostructure. In addition, the polarization induced bound sheet charge densities at the AlGaN/GaN and air/AlGaN interfaces, σ_{int}, σ_{surf}, and σ_{comp} , and the compensating mobile sheet charge density σ_{2DEG} are shown. As the material is Ga-face, the sign of the charge densities σ_{int} and σ_{surf} is positive and negative, respectively. To satisfy charge neutrality across the AlGaN barrier the net charge at the surface must be positive and therefore a positive compensating charge (σ_{comp}) is required. Furthermore, it has to be noted that as the considered AlGaN/GaN structures are undoped, the compensating mobile sheet charge density (σ_{2DEG}) consists of electrons that must originate from the surface of the AlGaN barrier [64].

Although an accurate calculation of the 2DEG density in this structure would require a sophisticated simulation tool, a simple semi-classical electrostatic analysis assuming charge neutrality to hold between the sheet charge densities at the surface and the interface, leads to the following analytical expression for the 2DEG sheet charge density (n_s) as a function of the Al alloy composition (x) of the Al$_x$Ga$_{1-x}$N barrier layer [176]

$$n_s = \frac{\sigma_{int}}{q} - \left[\frac{\varepsilon_0 \varepsilon(x)}{dq^2}\right] [q\phi_b(x) + E_F(x) - \Delta E_c(x)], \tag{2.9}$$

where σ_{int} is the polarization induced bound sheet charge density at the AlGaN/GaN heterojunction, q the electron charge, ε_0 the permittivity of free space, ε, d, x, are the relative dielectric constant, thickness, and Al mole fraction of the Al$_x$Ga$_{1-x}$N barrier layer, ϕ_b is the Schottky barrier height, E_F is the Fermi level at the heterojunction with respect to the GaN conduction

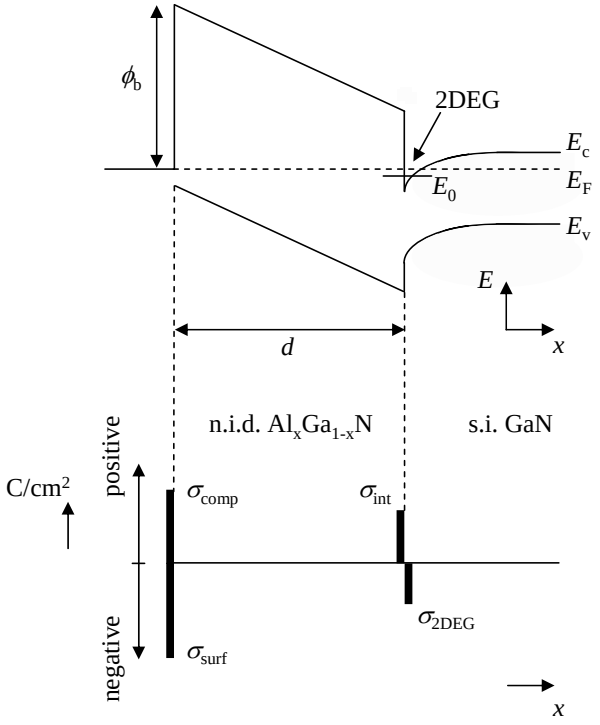

Figure 2.8: Energy band diagram of a Ga-face undoped AlGaN/GaN heterostructure and the polarization induced bound and compensating mobile sheet charge densities.

band edge, and finally ΔE_c is the conduction band offset at the AlGaN/GaN interface. The values for $\varepsilon(x)$ and $\phi_b(x)$ can be calculated by interpolation again using Vegard's law as [178]

$$\varepsilon(x) = 9.0 - 0.5x, \text{ and} \tag{2.10}$$

$$\phi_b(x) = 0.84 + 1.3x. \tag{2.11}$$

The value for E_F as a function of Al mole fraction can be approximated by [7]

$$E_F(x) = E_0(x) + \frac{\pi\hbar^2}{m^\star(x)} \cdot n_s(x), \tag{2.12}$$

with the ground state level (E_0) of the 2DEG being equal to

$$E_0(x) = \left[\frac{9\pi\hbar q^2}{8\varepsilon_0\sqrt{8m^\star(x)}} \cdot \frac{n_s(x)}{\varepsilon(x)} \right]^{\frac{2}{3}}, \tag{2.13}$$

and the effective electron mass as $m^\star(x) \approx 0.22 \cdot m_0$. $\triangle E_c(x)$ can be approximated by [113, 114]

$$\triangle E_c(x) = 0.7 \cdot \left[E_g(x) - E_g(0) \right], \tag{2.14}$$

where the bandgap energy of $Al_xGa_{1-x}N$ from experiments is known to be [25]

$$E_g(x) = 6.13 \cdot x + 3.42 \cdot (1-x) - x(1-x). \tag{2.15}$$

Using equations (2.9) - (2.15), the 2DEG sheet charge density can be calculated as a function of Al alloy composition or the thickness of the barrier layer assuming the surface barrier to be constant. Figure 2.9 shows the calculated 2DEG density as a function of the Al alloy composition with the AlGaN barrier thickness as a parameter. In addition, the bound polarization induced sheet charge (σ_{int}) is plotted as a reference. Three AlGaN barrier layer thicknesses, 100 Å, 200 Å, and 300 Å are plotted to illustrate the effect of barrier thickness variation. It can clearly been seen that for decreasing AlGaN barrier thickness the 2DEG density drops, which is due to increased Schottky barrier depletion. If we assume an Al content of 30%, the 2DEG densities for the 100 Å, 200 Å, and 300 Å barrier layers are 1.08 x 10^{13} cm^{-2}, 1.38 x 10^{13} cm^{-2},and 1.48 x 10^{13} cm^{-2}, respectively.

From Fig. 2.9 it can be seen that the 2DEG density approaches the bound polarization induced sheet charge for increasing AlGaN barrier thickness. This can be understood since the dipolar charge ($\sigma_{int} + n_s$) across the AlGaN barrier required to produce a fixed surface barrier decreases as the thickness increases, as the gate Schottky barrier is assumed to be constant for a particular Al composition irrespective of the AlGaN barrier thickness. It has to be noted that as a consequence of the constant barrier height (ϕ_b) there is a lower bound of the Al composition of the AlGaN layer for the formation of the 2DEG at the heterojunction. For the 100 Å, 200 Å, and 300 Å layers this lower bound turns out to be 9%, 5%, and 3%, respectively.

To understand the effect of the AlGaN thickness on the 2DEG density more clearly, it is plotted against the barrier layer thickness for 30% alloy composition in Fig. 2.10.

It can be seen that the 2DEG density increases monotonically with the AlGaN barrier thickness and asymptotically approaches a sheet carrier concentration of 1.68 x 10^{13} cm^{-2}, which equals the value for the bound polarization induced sheet charge for a layer with 30% Al content. In addition, there exists a minimum AlGaN barrier thickness of 35 Å below which no 2DEG exists at the heterojunction. This is due to the presence of a constant Schottky barrier height and is quite similar to the existence of a lower bound for Al composition in the case of a constant AlGaN barrier thickness. Furthermore, the surface barrier height controls the charge dipole across the AlGaN barrier, which in turn controls the magnitude of the 2DEG. Consequently, any change in surface barrier height is reflected as a change in the 2DEG.

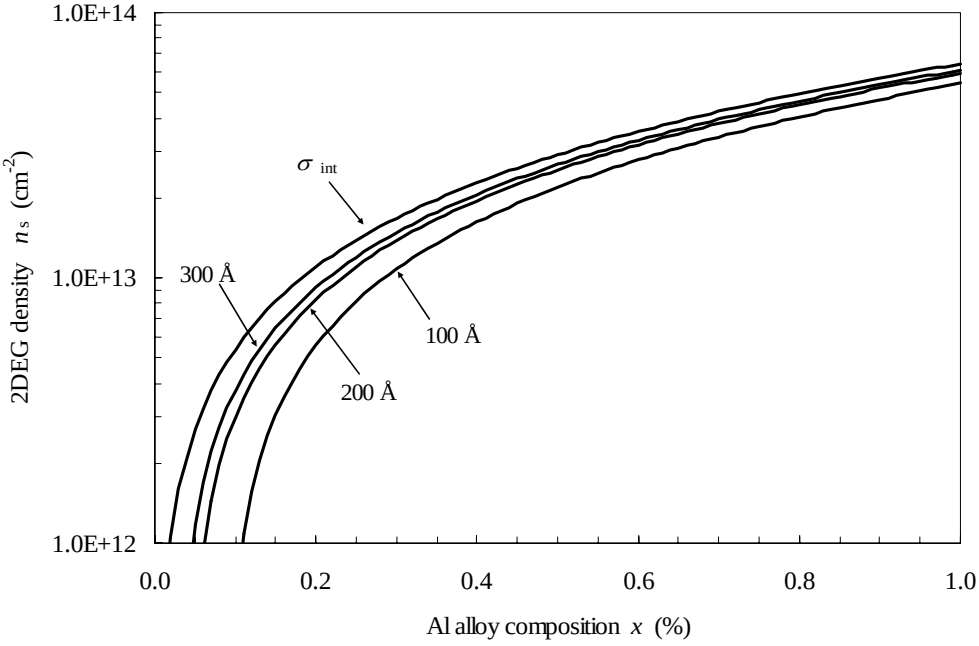

Figure 2.9: Calculated 2DEG density as a function of the Al alloy composition of the $Al_xGa_{1-x}N$ barrier layer for three different thicknesses. The bound polarization induced sheet charge (σ_{int}) is plotted as a reference.

2.3.4 Trapping effects in AlGaN/GaN HFETs

The previous discussions have clearly pointed out why AlGaN/GaN HFETs are the ultimate choice for high-power applications at microwave frequencies. However, these structures suffer from trapping and de-trapping of 2DEG electrons both inside the layer structure and at the semiconductor surface. These trapping effects give rise to the formation of quasi-static charge distributions that cause the current-voltage (*I-V*) characteristics at microwave frequencies to be considerably lower than under direct-current (DC) conditions. Consequently the microwave output power capability of the devices is significantly lower than expected from the DC output (*I-V*) characteristics and the chosen operation class.

Research activities towards identifying, understanding, and eliminating trapping effects in GaN-based HFETs in many ways parallel those conducted during the development of GaAs-based technology. Much of the knowledge obtained and techniques utilized for the GaAs case can and have been applied to GaN as well.

In this subsection, we will give an overview of two electrical characterization techniques used to investigate the various trapping effects in AlGaN/GaN HFETs. These techniques,

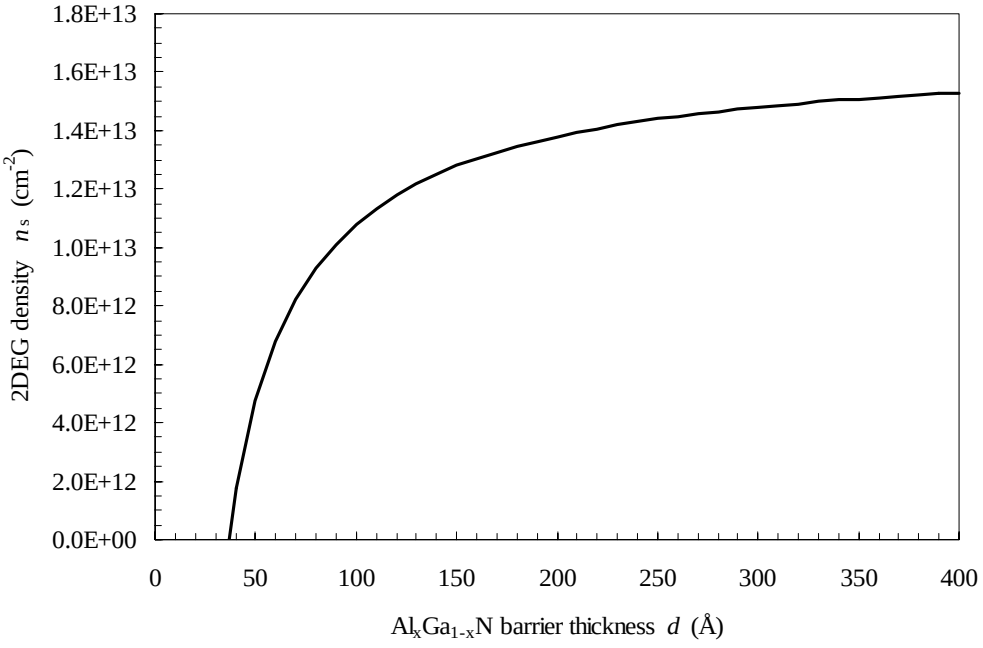

Figure 2.10: Calculated 2DEG density as a function of the AlGaN barrier thickness for an Al alloy composition of 30%.

which try to discriminate between lateral and vertical trapping phenomena, are commonly known as drain lag and gate lag respectively. Although the underlying physical mechanisms are completely different, the various trapping effects cause a reduction in drain current and consequently in output power. It has to be noted that in literature these reductions in drain current and output power are often referred to by a variety of terms such as current collapse, current slump, drain dispersion, DC-to-RF current dispersion, power drift, and power slump [19, 49, 168]. These terms sometimes cause some ambiguity regarding the responsible trapping mechanism as collapse, dispersion, and drift refer to a recoverable reduction whereas slump indicates a permanent degradation.

Drain lag

A significant but recoverable reduction in drain current resulting from the application of high drain-source bias voltages (typically $V_{DS} > 20$ V) is known as drain lag. This current collapse in GaN-based HFETs can be caused by instabilities in the positive compensation charge density at the AlGaN surface (σ_{comp}) that needs to be present to maintain the 2DEG channel. These instabilities in σ_{comp} can be caused by oxidation of the AlGaN barrier layer due to the high

current densities and elevated temperatures at the source contacts. Any reduction of σ_{comp} leads to a reduction of σ_{2DEG} and hence a decreased drain current and lower output power. However, initially the current collapse observed during a drain lag measurement has been related mainly to trapping of hot 2DEG electrons inside the layer stack because of the analogy observed in GaN-based MESFETs. Possible trapping locations inside the AlGaN/GaN layer stack, first reported by Khan *et al.* [81], are:

- the semi-insulating (s.i.) substrate (in the case of growth on SiC),
- at the interface between GaN and the substrate (either sapphire or SiC),
- in the n.i.d. high-resistivity (HR) GaN buffer,
- at the AlGaN/GaN interface, or
- in the AlGaN barrier layer.

Binari *et al.* [20] were the first to correlate drain current collapse in GaN-based MESFETs with hot electron trapping by deep traps in the n.i.d. HR GaN buffer layer. In addition, they showed the dependence of drain current recovery on illumination and temperature. These findings were confirmed by Zhang *et al.* and Kuliev *et al.* [94, 180]. A continuous transition from partial to complete drain current recovery was observed upon decreasing the wavelength of the light used from 720 nm to 366 nm (corresponding to the GaN bandgap energy at RT), respectively. The same behavior can be observed if the ambient temperature is increased up to temperatures over 150°C, which is consistent with thermal emission of trapped electrons from deep traps. For both dependencies no threshold in the amount of current recovery is observed which is indicative for a distribution of trap energy levels rather than a single trap with a well-defined level [20]. Further studies by Binari *et al.* [17, 18] revealed that the degree of drain lag is related to the conductivity of the GaN buffer layer, which can be significantly influenced by the growth pressure used. It has been shown that at low pressures (typically < 50 Torr) trap formation is strongly enhanced. As these traps compensate shallow donors this enables the growth of HR GaN buffer layers but also results in increased drain lag. At higher pressures trap formation decreases which results in more conductive GaN buffers and reduced drain lag either because of the lower trap density or the filling of these traps by shallow donors.

By studying the wavelength dependence of the drain current recovery in more detail, Klein *et al.* [88] have succeeded in providing spectroscopic signatures of the traps responsible for drain lag in GaN MESFETs and to estimate the energy levels of these traps with respect to the conduction band. They observed two broad absorptions below the GaN bandgap corresponding to the photoionization of carriers from two distinct traps that are located approximately 1.8 eV and 2.85 eV below the conduction band, respectively. The trap at 1.8 eV is suggested to be related to dislocations and grain boundaries [19] and the trap at 2.85 eV is related to carbon (C) incorporation which increases as growth pressure decreases [86]. Photoionization measurements on AlGaN/GaN HFETs have shown the same broad trap-related absorptions and a rapid increase at the GaN bandgap [87]. As no enhancement of the optically induced drain current recovery was observed for photon energies at or above the AlGaN bandgap it seems

obvious that drain lag in AlGaN/GaN HFETs is caused by the same traps in the HR GaN buffer layer that also caused drain lag in the GaN MESFETs.

It is well known that AlGaAs/GaAs HFETs suffer from trapping by so-called DX centers in the AlGaAs barrier layer [76]. In the nitrides a DX-like center associated with oxygen in the AlGaN barrier layer has been observed [119]. This trap, like the DX center in AlGaAs, is effective only at low temperatures. However, in the nitrides current collapse is observed at RT. Therefore it is unlikely that current collapse in AlGaN/GaN HFETs is due to a DX-like trap in the AlGaN barrier layer.

Recovery from current collapse by thermal emission of the trapped carriers has a characteristic time dependence which can be investigated by measuring the drain current at a low drain-source voltage (typically $V_{DS} < 1$ V) before and after applying a large drain-source voltage (typically $V_{DS} > 20$ V) while keeping the gate-source voltage at 0 V (open channel). Exposure to the high drain-source voltage induces current collapse and the recovery of the drain current to its low-field value is monitored as a function of time. Dang *et al.* [35] have determined three time constants, designated as fast ($\sim$1 s), intermediate ($\sim$10 s), and slow ($>$ 100 s), which they assigned to traps at the semiconductor surface, deep levels in the AlGaN barrier layer, and traps at the AlGaN/GaN interface, respectively.

Gate lag

For an ideal HFET an estimate of the maximum obtainable output power under large-signal operation at microwave frequencies can be calculated using the DC output (*I*-*V*) characteristics and the chosen operation class. If biased in class A, i.e. $I_D = 0.5 \cdot I_{D,max}$, the maximum output power is given by [67]

$$P_{out,max} = \frac{(V_{BD} - V_{knee}) \cdot I_{D,max}}{8}, \tag{2.16}$$

where V_{BD} is the drain-source breakdown voltage, V_{knee} is the knee voltage of the curve representing the maximum drain current ($I_{D,max}$). It has been observed that the maximum output power under large-signal operation at microwave frequencies, even for AlGaN/GaN HFETs hardly suffering from any drain lag, is much less than calculated using equation 2.16 [90, 173]. Figure 2.11-(a) shows a schematic representation of the $(I_D - V_{DS})$ characteristics of an ideal HFET under DC operation with the location of the quiescent bias point (Q) for class A operation on the load line for maximum output power. It should be noted that this representation shows the (*I*-*V*) curves for a given maximum power dissipated in the device. Figure 2.11-(b) shows a schematic representation of the $(I_D - V_{DS})$ characteristics under large-signal operation at microwave frequencies. Note that the (*I*-*V*) curves are shown for the same maximum power dissipated in the device as under DC operation.

Comparing Figs. 2.11-(*left*) and (*right*) it can clearly be concluded that although the big discrepancy between expected and measured microwave output power is caused by both reduced voltage and current swings, the reduction of the latter is dominant. Reduced voltage swing is due to an increased knee voltage, also known as knee voltage walk-out, which is generally related to surface oxidation but has also been attributed to trapping of electrons in the s.i. GaN buffer layer [17].

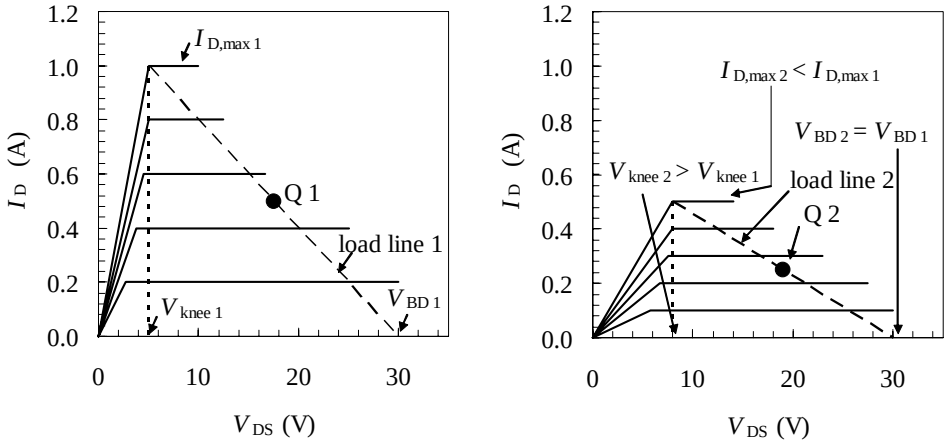

Figure 2.11: Schematic representation of the output (*I*-*V*) curves for an ideal HFET under DC operation (*left*), and under large-signal operation at microwave frequencies (*right*).

Nguyen *et al.* [131] showed that drain current compression during large-signal operation at microwave frequencies has been observed even when the load impedance was near zero. As the voltage swing in this case is minimal, they concluded that the trapping of electrons occurs either in the AlGaN barrier layer or at the AlGaN surface and not in the GaN buffer layer. Despite the fact that this effect has been observed over a wide range of time and frequency, which makes it very difficult to unambiguously determine the location of the responsible trapping mechanism, various research groups have confirmed that drain current reduction during large-signal operation at microwave frequencies is mainly caused by trapping of electrons at the free AlGaN surface [17, 48, 64, 141, 162, 164].

To understand how electrons that get trapped at the free AlGaN surface can influence the magnitude of the drain current we have to recall the discussion about the formation of the 2DEG at the AlGaN/GaN heterojunction. As described in Subsect. 2.3.3, the existence of the polarization dipole in the AlGaN barrier layer alone is not enough for a 2DEG to form in the potential well at the AlGaN/GaN interface. For this to happen, a positive sheet charge (σ_{comp}) must exist at the free AlGaN surface to compensate the negative sheet charge (σ_{2DEG}) due to electrons in the channel. Such positive sheet charge can arise from surface states created by dangling bonds, threading dislocations accessible at the surface, ionized donor states, and ions absorbed from the ambient environment [48, 64]. Neutralizing the positive surface charge, either by the capture of electrons in trap states, the emission of holes, or by the adsorption of charged ions, leads to depletion of the 2DEG density and hence reduction of the drain current.

The effect of surface states was measured for the first time by Vetury *et al.* [163]. They used floating gates as potential probes to directly measure the surface potential along the gate-drain access region. It was found that the lateral extension of the gate depletion region was

inconsistent with the ionized positive donor density, suggesting the presence of negative charge on the surface. This negative charge causes the surface potential to become more negative leading to a rapid extension of the gate depletion region. The observation that negative surface charge acts like a negatively biased metal gate has led to the virtual gate concept [37, 164].

According to this concept, there now exist two gates, the actual metal gate and the so-called virtual gate on the AlGaN surface in the gate-drain access region, the depletion regions of which being in series. The potential on the metal gate is controlled by the applied gate bias while the potential on the virtual gate is determined by the total amount of trapped charge in the gate-drain access region. As a consequence, the drain current is now a function of the potential on the metal gate, on the virtual gate, and on the gate-drain voltage (V_{GD}). The potential on the virtual gate is zero as long as no bias is or has been applied to the device. Upon biasing the device the potential on the virtual gate starts changing. The general trend is that the virtual gate becomes reverse biased when the metal gate is (negatively) biased towards pinch-off and the drain bias is increased. In any dynamic measurement, e.g. a load-pull power measurement, the current available at any point during the cycle depends on the instantaneous trap occupancy, i.e. the instantaneous value of the potential on the virtual gate at that specific point. It is obvious that the ability of the metal gate to decrease the drain current is never impaired as to decrease the drain current the trap occupancy must either remain unchanged or increase. However, the ability of the metal gate to open up the channel is in fact impaired as that requires the trap occupancy to decrease. Because of this dependency of drain current reduction on the (virtual) gate, the term gate lag is now obvious.

It has become clear that the potential of the virtual gate depends on the instantaneous trap occupancy and hence is a complex function of the spatial distribution of the total charge trapped and on the charging path. Charging and discharging of the virtual gate are processes with time constants that not only depend on the spatial location of the surface traps involved but also on their capture and emission constants, the charging and discharging paths, and the surface mobility of mobile charges, either electrons or holes. The latter is a function of the location dependent electric field. As charging of the virtual gate proceeds, the depletion region extends from the edge of the metal gate towards the drain. As a result the electric field at the gate edge is decreased, thereby reducing the surface gate leakage current. Because unoccupied surface states are located continuously further away from the metal gate, the reduced electric field reduces the rate at which the depletion region extends.

It is obvious that in order to restore the drain current the net positive charge (σ_{comp}) on the AlGaN surface has to be restored, i.e. eliminating the virtual gate. This can be done either by forward biasing the metal gate with respect to the source and drain or by illumination using photons with energy larger than the bandgap of the GaN buffer. In the latter process the photons create electron-hole pairs in the GaN buffer layer. Due to the strong electric field in the AlGaN barrier layer these holes get swept towards the AlGaN surface. The accumulation of holes at the surface forward biases the surface and thereby eliminates the virtual gate.

It has been reported that the formation of a virtual gate and the resulting drain current reduction can effectively be eliminated by passivation of the free AlGaN surface [17, 48, 109, 141, 162, 164]. Traditionally a silicon nitride film (a-SiN_x:H), hereafter indicated as SiN, deposited by plasma enhanced chemical vapor deposition (PECVD) has been used as surface

passivation layer. However other passivation layers, e.g. silicon dioxide (SiO_2), scandium oxide (Sc_2O_3), and magnesium oxide (MgO), have also been reported [110]. Although the exact mechanism by which surface passivation prevents the formation of the virtual gate is still unclear, several possible mechanisms can be found in literature. Green *et al.* [48] suggest that upon passivation with SiN the properties of the surface traps are changed leading to an unchanged or even slightly increased amount of positive charge at the SiN/AlGaN interface preventing drain current reduction. Vetury *et al.* [164] and Kohn *et al.* [89] suggest that the SiN film buries the positively charged surface donors and makes them inaccessible to electrons leaking from the metal gate. The total amount of positive surface charge remains unchanged, at least, and drain current reduction is prevented. In addition to this mechanism, the SiN film or the deposition process is assumed to change the energy level of the surface donor. This mechanism seems likely since it has been observed that deposition of a SiN film results in an increase of the 2DEG density. Such an increase indicates that the electric field in the AlGaN barrier layer must have decreased since the deposition cannot change the energy band diagram in the GaN buffer layer. This change of the electric field implies that the level of surface pinning has decreased [89, 164]. It has to be remarked that the passivation layers being amorphous materials can also contain electronic or ionic charge states, e.g. the K_0-center in SiN films which has been identified in power slump measurements in passivated AlGaAs/GaAs power HEMTs [63]. This could negatively impact long time stability and reliability of the device characteristics and performance.

2.4 Conclusions

This chapter started with a description of the GaN material system. We have given an overview of the wurtzite crystal structure and the unique polarization effects in III-nitride crystals, which are mainly caused by the involvement of nitrogen (N), which is the smallest and most electronegative Group V element. We have also discussed some key topics concerning GaN-based HFETs such as the most important material growth techniques, different AlGaN/GaN HFET layer structures, and the theory of 2DEG formation in these structures. The chapter ended with a discussion about charge trapping effects in GaN-based HFETs that severely deteriorate their microwave high-power performance. A priori, the surface of AlGaN/GaN HFETs needs to be and remain positively charged.

Chapter 3

Design of GaN-based HFETs

In this chapter we will focus on design aspects of microwave high-power AlGaN/GaN HFETs on both sapphire and s.i. SiC substrates. The chapter starts with epitaxial device design. We will describe the requirements that the epitaxial AlGaN/GaN layers on sapphire and s.i. SiC have to meet for application in microwave high-power devices. This is followed by the development of the growth processes and the electrical characterization of the different epitaxial layers. This subject ends with an overview of the optimized AlGaN/GaN epitaxial heterostructures that have been used for the fabrication of large gate periphery microwave high-power HFETs the results of which will be shown in Chapter 6.

Next, we will discuss several device layouts that have been designed to fabricate both small and large gate periphery devices. We will explain key aspects that have to be taken into account in the design of microwave high-power devices. Finally, schematic overviews of the process flows of the different mask sets will be given. Detailed descriptions of these process flows are provided in Appendix A.

3.1 Epitaxial device design

This section describes the design, development and electrical characterization of epitaxial AlGaN/GaN layer stacks on sapphire and s.i. SiC substrates using metal organic chemical vapor deposition (MOCVD) suited for the fabrication of microwave high-power HFETs. The MOCVD hetero-epitaxial growth has been carried out by Andrzej Grzegorczyk (sapphire) [50] and Mariusz Rudzinski (s.i. SiC) [146], PhD students with the group Applied Materials Science (AMS) of the Radboud University Nijmegen (RU). At TU/e we have defined the epitaxial layer stack and electrically characterized the epilayers using current-voltage (I-V) and capacitance-voltage (C-V) measurements.

First we will consider the requirements which AlGaN/GaN epilayers have to meet from a device perspective in order to be used in microwave high-power applications. Baring these

requirements in mind and taking into account the boundary conditions determined by our resources we will explain our choice for the initial AlGaN/GaN layer stack. Next we will discuss the optimization of the different layers, i.e. GaN buffer layer and AlGaN barrier layer. Finally we will present the optimized layer stack that has been processed into large periphery microwave high-power HFETs the results of which will be presented in Chapter 6.

3.1.1 Requirements for AlGaN/GaN epilayers from a device perspective

From a device perspective there are several requirements the GaN-based layer stack must meet in order to be used in microwave high-power applications. As mentioned in Sect. 1.3, GaN is hetero-epitaxially grown on both lattice and thermally mismatched substrates such as sapphire and s.i. SiC. As pointed out in Sect. 1.3, at the moment s.i. SiC is the substrate of choice for application in microwave high-power HFETs because of its relatively low lattice mismatch (3.4%), and relatively low thermal expansion coefficient mismatch (25%), which lead to relatively low dislocation densities on the order of 10^8 - 10^9 cm^{-2}. In addition, its high thermal conductivity (3.7 - 4.5 W/cmK at 300 K) provides good heat-sinking capabilities. However, a considerable drawback of these substrates is that they were and still are very expensive (at the time of writing this thesis about $ 4,000 for a single 2 inch wafer). Besides the fact that high quality s.i. SiC substrates were not available to us at the start of the project the decision was made to develop both the MOCVD material growth and device technology on cheap ($ 100 for a single 2 inch wafer) sapphire substrates.

To achieve optimal device performance it is of utmost importance that the GaN buffer layer is of a very high quality, i.e. low defect density and high resistivity (semi-insulating behavior) to avoid both charge trapping of 2DEG electrons, which causes drain current collapse and hence output power reduction, and high buffer leakage, which makes it very difficult or even impossible to pinch-off a device and achieve a high breakdown voltage. The inability to effectively pinching-off a device also reduces the available current swing and therefore the achievable microwave output power. In addition, buffer leakage can cause interaction between active devices on the same chip even if they are isolated by mesa structures. Furthermore the surface of the GaN buffer layer should be smooth to render a good interface between itself and the AlGaN barrier layer. A smooth and sharp interface is required to obtain a high mobility and good confinement of the 2DEG electrons. Good carrier confinement also enables effective device pinch-off.

To obtain a high drain current, as a partial requirement for high output power, not only a high density of the 2DEG electrons (n_s) but also a high saturation velocity (v_{sat}) is required as the drain current is proportional to the product of n_s and v_{sat}. In addition to a high value of n_s, a high electron mobility (μ_n) is required to achieve a low series resistance (R_s) and consequently a low knee voltage (V_{knee}). In Sect. 2.3.3 it has been shown that n_s is a function of the aluminum content and to a lesser extent of the thickness of the tensile strained AlGaN barrier layer. Therefore, to achieve a high 2DEG density it should be tried to incorporate as much aluminum as possible without causing relaxation of the AlGaN layer. An additional restriction on the maximum thickness of the AlGaN layer is imposed by a very important device structural design concept described by Das [36], which is also known as the high-aspect-ratio design

concept, that puts a limit on the maximum AlGaN thickness. For microwave high-power applications the most important device figures of merit are the unity current gain frequency or cut-off frequency (f_T), and the unity power gain frequency or maximum oscillation frequency, (f_{max}). The aspect ratio in the aforementioned design concept is the ratio of the effective gate length, i.e. including lateral depletion between the gate and drain regions, and the distance between the Schottky gate metal and the 2DEG. It has been shown that for good microwave device performance this ratio should not drop below 10 [36]. If the frequency of operation is targeted at the center of the X-band, i.e. 10 GHz, a rule of thumb tells that the minimum value for f_T would have to be 40 GHz. Under the assumptions that all electrons in the 2DEG travel at the saturation velocity and that any intrinsic feedback due to the gate-drain capacitance (C_{gd}) can be neglected, a first order approximation of f_T is given by

$$f_T = \frac{v_{sat}}{2\pi L_g}, \tag{3.1}$$

where v_{sat} is the saturation velocity of the electrons (2.7 x 10^7 cm/s), and L_g is the gate length. Using Eqn. 3.1 the allowed gate length is 1 μm at maximum. However, if parasitic capacitances are taken into account the required gate lengths are in the range of 0.25 μm - 0.5 μm. Hence the maximum thickness of the AlGaN barrier layer is about 25 nm. A possibility to use thicker AlGaN layers without disobeying the high-aspect-ratio concept would be to use a gate recess.

3.1.2 Initial AlGaN/GaN layer stack

To develop an epitaxial MOCVD growth process for AlGaN/GaN layer stacks that can meet the requirements described in Sect. 3.1.1 from scratch is very complex. In order not to obscure the development process too much, we have chosen to keep the initial epitaxial layer stack as simple as possible. Figure 3.1 shows a schematic representation of the initial stack consisting of a c-plane (0001) sapphire substrate, GaN nucleation layer (NL), non-intentionally doped (n.i.d.) GaN buffer layer, and n.i.d. AlGaN barrier layer. In addition, the idea was to develop the epitaxial MOCVD growth process on cheap sapphire substrates and after obtaining good results start transferring the growth technology onto s.i. SiC substrates.

As a first step the growth process for obtaining high quality s.i. GaN buffer layers has been investigated. Section 3.1.3 will describe the approach used and the results obtained on both c-plane sapphire and s.i. 4H-SiC substrates.

3.1.3 GaN buffer layer

In this section we will briefly touch upon the developed growth strategy for high quality GaN buffer layers on both c-plane sapphire and s.i. 4H-SiC substrates using MOCVD. For a detailed explanation of all process details and the involved growth mechanisms we refer to the PhD theses of Andrzej Grzegorczyk (sapphire) [50] and Mariusz Rudzinski (s.i. SiC) [146]. Furthermore, we will present and discuss electrical characterization results of these layers that have been obtained by current-voltage (I-V) and capacitance-voltage (C-V) measurements.

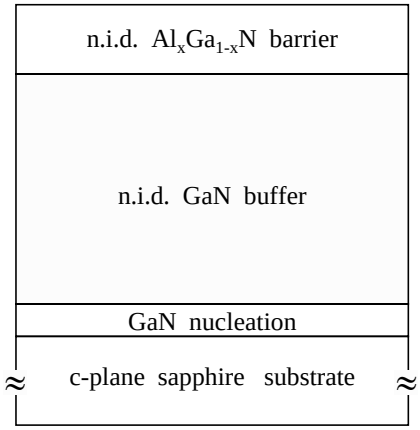

Figure 3.1: Schematic representation of the initial n.i.d. AlGaN/GaN layer stack on a c-plane sapphire substrate.

The GaN layers have been grown on commercially available 2 inch c-plane sapphire substrates in a radio frequency (RF) heated, AIXTRON AIX-200, low-pressure horizontal MOCVD reactor. Trimethylgallium ($Ga(CH_3)_3$) and ammonia (NH_3) are used as Ga and N precursors, respectively. A growth method generally known as the two-step growth method has been chosen. In this method, which has first been introduced by Amano *et al.* [5], a low-temperature GaN nucleation layer is grown before the high-temperature GaN buffer layer. It was shown that the low-temperature GaN nucleation layer strongly determines the quality of the high-temperature GaN buffer layer. In 1996, Keller *et al.* [77] demonstrated that a short nitridation of the sapphire substrate before deposition of the low-temperature GaN nucleation layer strongly improves the structural properties of this layer thereby reducing the density of threading dislocations in the GaN buffer layer.

To calculate the resistivity of GaN buffer layers the mobility and the concentration of the residual free carriers have to be determined. The mobility has been determined by Hall measurements and the residual free carrier concentration has been calculated from capcacitance-voltage (C-V) measurements using circular nickel/gold (Ni/Au) Schottky contacts with an area of 9.2 x 10^{-5} cm^2. The Schottky contacts are surrounded by titanium/aluminum/nickel/gold (Ti/Al/Ni/Au) ohmic contacts as can be seen in Fig. 3.2.

In thermal equilibrium a depletion region exists in the GaN buffer layer due to the Schottky contact. The width of this depletion region depends to a large extent on the residual doping concentration of the GaN buffer layer, i.e. for high residual carrier concentration the depletion region will be narrow and for low concentration it will be wide. Using the depletion approximation [143] the system, Schottky metal - depletion region - bulk GaN buffer layer, can be considered as a parallel plate capacitor with the depletion region acting as the insulator. The capacitance (C) is then approximated by

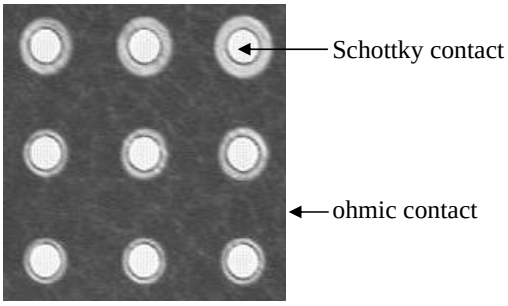

Figure 3.2: Circular Ni/Au Schottky contacts with an area of 9.2 x 10^{-5} cm^2 used for (*C-V*) measurements. The Schottky contacts are surrounded by (Ti/Al/Ni/Au) ohmic contacts.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{W}, \tag{3.2}$$

where ε_0 is the permittivity of free space, ε_r is the relative permittivity of the GaN buffer layer, A is the area of the Schottky contact, and W is the width of the depletion region. The latter is given by

$$W = \sqrt{\frac{2\varepsilon_0 \varepsilon_r}{qN_D}(V_{bi} - V_R)}, \tag{3.3}$$

where q is the elementary charge, N_D is the concentration of completely ionized donor atoms, V_{bi} is the built-in voltage, and V_R is the applied reverse bias. Combining Eqns. 3.2 and 3.3 yields

$$C = \frac{A}{\sqrt{\frac{2(V_{bi}-V_R)}{qN_D\varepsilon_0\varepsilon_r}}}. \tag{3.4}$$

This equation can be inverted and squared to obtain

$$\frac{1}{C^2} = \frac{2(V_{bi} - V_R)}{qN_D\varepsilon_0\varepsilon_r A^2}, \tag{3.5}$$

which describes the dependency of the capacitance (C) on the applied reverse bias (V_R). A plot of $1/C^2$ versus V_R yields a straight line with a slope that is inversely proportional to N_D. After a derivation of Eq. 3.5 with respect to V_R, N_D is given by

$$N_D = \frac{-2}{q\varepsilon_0\varepsilon_r A^2 \frac{d\left(\frac{1}{C^2}\right)}{dV_R}}. \tag{3.6}$$

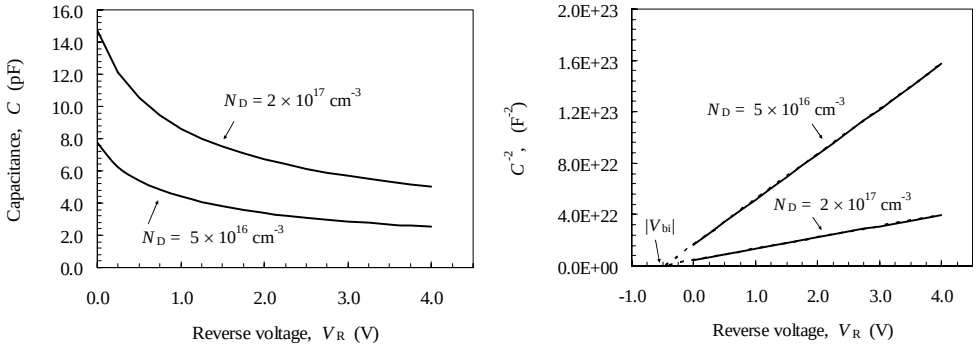

Figure 3.3: Typical (C-V) profiles of our first GaN buffer layers on sapphire (*left*) and the corresponding ($1/C^2$-V_R) plots (*right*).

Using this equation we can calculate the residual free carrier concentration in the GaN buffer layer once we have measured the (C-V) profile. To do this an alternating current (ac) capacitance bridge can be used. The amplitude of the ac test signal used must be much smaller than the applied DC bias voltage in order not to significantly influence the width of the depletion layer and the corresponding capacitance value. A difficulty in obtaining the (C-V) profile can be caused by the presence of electron traps in the GaN buffer layer. These traps may be filled and depleted in response to the ac signal which influences the measurement results. To minimize these effects (C-V) measurements must be performed at a frequency, typically larger than 100 kHz, where the traps cannot follow the ac signal [143]. We have performed (C-V) measurements using a HP4275A multi-frequency LCR meter at a frequency of 1 MHz. Figure 3.3-(*left*) shows typical (C-V) profiles of our first GaN buffer layers that were grown using a GaN nucleation layer deposited at 525 °C followed by a thick (1 μm) GaN layer deposited at 1170 °C using hydrogen as carrier gas throughout the process. Figure 3.3-(*right*) shows the corresponding ($1/C^2$-V_R) plots from which the residual free carrier concentrations have been calculated.

Hall measurement results of these GaN buffer layers showed mobility values ranging from 300 - 500 cm^2/Vs. Together with the residual free carrier concentrations in the range of 5 x 10^{16} cm^{-3} - 2 x 10^{17} cm^{-3} this results in resistivity values ranging from 0.06 Ωcm - 0.4 Ωcm. It is obvious that these low resistivity values make these buffer layers unsuitable for application in an actual device.

In an attempt to decrease the residual electron concentration and thereby increasing the resistivity of the high-temperature GaN buffer layer, the growth procedure has been changed in the following way. The low-temperature GaN nucleation layer has been replaced by a layer consisting of selectively grown GaN islands realized by an in-situ grown Si_xN_y, hereafter SiN, mask [52]. The in-situ deposition of the SiN mask starts directly after nitridation of the sapphire substrate at 1170 °C by mixing silane (SiH_4) to the ammonia (NH_3) flow. After cooling down to 525 °C a 30 nm standard low-temperature GaN layer is deposited on the SiN layer. During heating up the SiN/GaN layers to the growth temperature of the high-temperature

GaN buffer layer (1170 °C) the 30 nm GaN layer transforms from a smooth layer into GaN islands with a diameter of approximately 100 nm. These islands will act as centers from where lateral epitaxial overgrowth starts. Despite considerably improved optical properties of the GaN epilayers grown using this approach, the residual free carrier concentration of the GaN buffer layers remained the same, i.e. 5 x 10^{16} cm^{-3} - 2 x 10^{17} cm^{-3}.

In general two possible methods can be used to decrease the residual free carrier concentration of the GaN buffer layers. The first is to grow compensated GaN buffer layers using acceptor impurity atoms like magnesium (Mg), iron (Fe), or zinc (Zn) [58, 98]. Using the growth process described above, Mg-doped GaN buffer layers have been grown. Although this approach resulted in reduced residual free carrier concentrations of about 9 x 10^{15} cm^{-3} and correspondingly increased resistivity values of 26 Ωcm we have abandoned Mg-compensation since the Mg content of the layers is difficult to control and Mg starts diffusing through the complete layer stack due to high-temperature steps during device processing. In addition, the introduction of additional scattering centers that reduce the mobility of the 2DEG electrons in an HFET is not desired. Instead at RU they have chosen to concentrate on the second method which states that highly resistive GaN buffer layers can be achieved by optimizing the growth conditions. By decreasing the temperature at which the high-temperature GaN buffer layer is grown from 1170 °C to 1130 °C they were able to reduce the residual free carrier concentration to about 1 x 10^{13} cm^{-3} and correspondingly increase the resistivity up to 3000 Ωcm. The reason for these results is attributed to the introduction of dislocations in the high-temperature GaN buffer layer that compensate the free carrier concentration. However, it must be kept in mind that there is a trade-off between the resistivity of the layers and the concentration of deep traps which can cause considerable drain lag and hence reduction of output power as we have seen in Sect. 2.3.4. Although a resistivity of 3000 Ωcm is high enough for application in an HFET, this result could not be obtained reproducibly.

To understand the mechanism behind the high-resistivity of the GaN buffer layers enabling them to grow such layers in a reproducible way, Grzegorczyk *et al.* [50, 51] have investigated the influence of the morphology and epilayer structure of the low-temperature GaN nucleation layer on the resistivity of the high-temperature GaN buffer layer. They found that the type of carrier gas used during the deposition of the low-temperature GaN nucleation layer strongly affected its surface morphology and structure. They showed that changing of carrier gas from hydrogen to nitrogen before deposition of the GaN nucleation layer the resistivity of the GaN buffer layer could very reproducibly be increased from typically 0.5 Ωcm to more than 3 x 10^4 Ωcm. Furthermore, they showed evidence that this result is due to changes of the ratio of edge to screw and mixed-type threading dislocations. Figure 3.4-(*left*) shows typical (C-V) profiles of the GaN buffer layers that were grown using the lower growth temperature of 1130 °C and of buffer layers that were grown on GaN nucleation layers which have been deposited using nitrogen as carrier gas. Figure 3.4-(*right*) shows the corresponding ($1/C^2$-V_R) plots from which the residual free carrier concentrations have been calculated.

The optimized growth procedure developed at RU to achieve these resistivity values starts by annealing the sapphire substrate at 1150 °C in a hydrogen ambient at a total reactor pressure of 50 mbar. After that the carrier gas is changed to nitrogen keeping all other parameters constant. Next, a short nitridation step of the substrate is carried out at 1125 °C using ammonia.

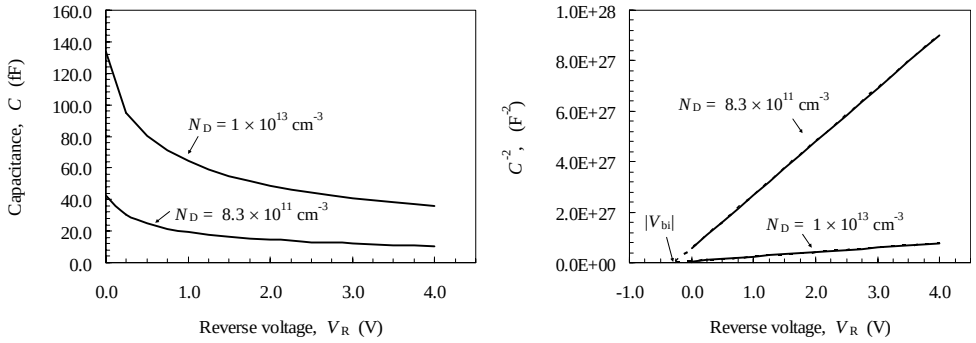

Figure 3.4: Typical (*C*-*V*) profiles of the GaN buffer layers that were grown using the lower growth temperature of 1130 °C and of buffer layers that were grown on GaN nucleation layers which have been deposited using nitrogen as carrier gas (*left*) and the corresponding ($1/C^2$-V_R) plots (*right*).

After this step the temperature is decreased to 560 °C, the pressure raised to 500 mbar, and a thin GaN nucleation layer is deposited. Next, the temperature is raised to 1130 °C and a short annealing of the GaN nucleation layer takes place due to which the crystallites in the nucleation layer recrystallize and form small-diameter islands [66]. A high density of these islands leads to a smoother surface and more grain boundaries in the nucleation layer. Weimann *et al.* [167] have shown that the boundaries between these islands contain arrays of dislocations along the interface between two islands. Cho *et al.* [32] have shown that these edge dislocations work as acceptor-like traps levels. Since screw dislocations have been identified as a path of electrical conductivity [32] and mixed dislocations are electrically inactive [32, 149], or at least not highly conductive, it is clear that by increasing the edge and decreasing the screw dislocation densities it is possible to grow highly resistive GaN buffer layers. Finally, the GaN buffer layer is grown at a total reactor pressure of 50 mbar with a V/III ratio of 1400 and hydrogen as carrier gas. The thickness of our first GaN buffer layers was chosen to be 1 μm. For application in HFETs we have decided to grow buffer layers with a thickness of 2 μm. Problems with respect to thermal issues are alleviated by increasing the distance between the channel, which can get really hot during operation (typically around 300 °C), and the sapphire substrate with its poor thermal conductivity (0.47 W/cmK at 300 K).

Having obtained these good results on sapphire substrates the growth process has been transferred onto commercially available 2 inch s.i. 4H-SiC substrates. The same low-pressure horizontal MOCVD reactor has been used but now using trimethylgallium ($Ga(CH_3)_3$), ammonia (NH_3), trimethylaluminum ($Al(CH_3)_3$), and ferrocene ($Fe(C_5H_5)_2$) as precursors for Ga, N, Al, and Fe, respectively. Trimethylaluminum has been used because wetting problems with GaN nucleation layers on SiC required the use of AlN or $Al_xGa_{1-x}N$ nucleation layers. The standard non-intentionally doped GaN buffer layers on s.i. 4H-SiC showed n-type conductivity with resistivity values ranging from 0.5 to 3 Ωcm. To increase the resistivity of the GaN buffer layers the same approaches, i.e. compensation doping and optimization of growth

conditions, have been used as for the GaN buffer layers grown on sapphire. Pyrolyzation of the metalorganic ferrocene has been used to investigate compensation doping of the GaN buffer layers with Fe as this has been proposed to be an effective way to control their resistivity [23, 57]. Rudzinski *et al.* [146] have been able to show that both the compensation doping and non-compensation doping approaches can be used to grow highly resistive GaN buffer layers on s.i. SiC substrates. Typical resistivity values for GaN buffer layers on Fe-doped and non-compensation doped GaN buffer layers on s.i. 4H-SiC exceed 10^4 Ωcm. Due to the excellent thermal conductivity of SiC substrates (3.7 - 4.5 W/cmK at 300 K) it is not necessary to grow buffer layers with a thickness of 2 μm as in the case of sapphire substrates. Therefore, in the case of SiC substrates the choice has been made to grow GaN buffer layers with a thickness of 1 μm in order to keep the active part of the device at a safe distance from the higher-defect-density material near the substrate interface.

3.1.4 AlGaN barrier layer

The final step towards the realization of the initial AlGaN/GaN layer stack as proposed in Sect. 3.1.2 is the development of the n.i.d. AlGaN barrier layer. In Sect. 2.3.3 it has been shown that the growth of a tensile strained AlGaN barrier layer with an aluminum content higher than 20% is required to achieve a 2DEG with a sheet carrier density (n_s) larger than 1 x 10^{13} cm^{-2} without any additional doping of the AlGaN layer. The optimization described in this section is done baring in mind the requirements for achieving optimal device performance mentioned in Sect. 3.1.1. For detailed information on the actual growth procedure we refer to the PhD theses of Andrzej Grzegorczyk (sapphire) [50] and Mariusz Rudzinski (s.i. SiC) [146]. Furthermore, we will discuss electrical characterization results of the first and optimized n.i.d. AlGaN/GaN layers obtained by reverse *I-V* and *C-V* measurements.

As starting point for the optimization of the AlGaN barrier we have used the optimized GaN buffer layers grown on commercially available 2 inch c-plane sapphire substrates. We started with AlGaN barrier layers with a thickness of 20 nm and a targeted aluminum content of about 30%. Experiments have been done with different growth temperatures, different aluminum flows and different total reactor pressures during the growth of the AlGaN layer. As mentioned in Sect. 3.1.3 the optimized growth conditions for our high-resistivity GaN layers include a total reactor pressure of 50 mbar so it has been tried to grow the AlGaN layer at the same pressure in order to facilitate a simple transition during growth from GaN to AlGaN. Grzegorczyk *et al.* [50] noticed a very strong dependence of the aluminum content of the AlGaN layers on the pressure in the reactor. At 50 mbar, a maximum aluminum content of about 19% can be achieved. By decreasing the pressure to 35 mbar, they managed to grow layers with an aluminum content higher then 60%. Additionally, the growth rate of the AlGaN layer increased from less than 0.1 μm/h to 0.6 μm/h. The reproducibility of the aluminum content in AlGaN layers is a very important aspect in device development. To accurately determine the aluminum content of thin (20 - 30 nm) AlGaN layers photoluminescence should be used since Raman spectroscopy and X-ray measurements require layer thicknesses of at least 0.3 μm. As we have seen in Sect. 2.3.3, the thickness of the tensile strained AlGaN barrier layer also influences the magnitude of the sheet carrier concentration. Furthermore, the sharpness

Table 3.1: Summary of the intended thicknesses of the AlGaN barriers and aluminum contents of structures S_1 to S_4.

Structure	S_1	S_2	S_3	S_4
AlGaN thickness (nm)	15	20	20	20
Aluminum content (%)	20	25	20	25

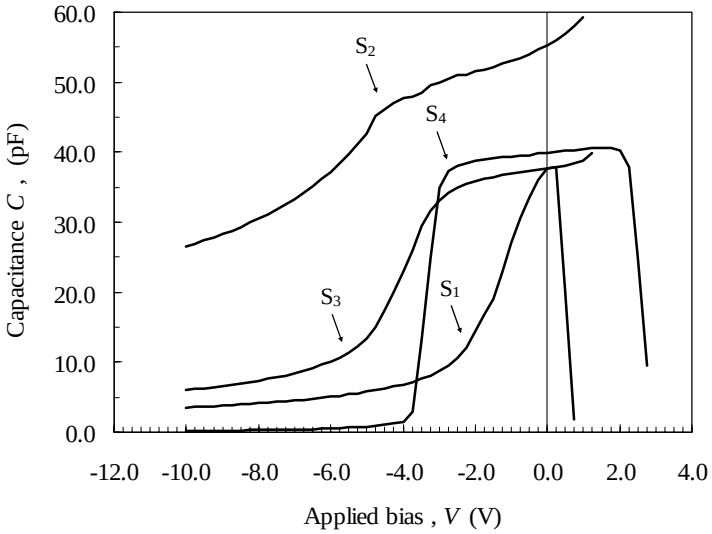

Figure 3.5: Typical (*C-V*) profiles of our first (S_1 and S_2), nearly optimized (S_3), and optimized (S_4) n.i.d. AlGaN/GaN layers on sapphire substrates.

and smoothness of the interface between the AlGaN barrier and GaN buffer layers is critical for the mobility and confinement of the 2DEG electrons.

(*C-V*) measurements using the Schottky contacts mentioned before have been done to determine the thickness of the AlGaN barrier, the 2DEG sheet carrier density (n_s) , and the residual carrier concentration of the GaN buffer layer. Reverse (*I-V*) measurements using these contacts have been done to determine the leakage currents of the different layer stacks. Figure 3.5 shows typical (*C-V*) profiles of our first (S_1 and S_2), nearly optimized (S_3), and optimized (S_4) AlGaN/GaN layers on sapphire substrates. Table 3.1 shows a summary of the intended thicknesses of the AlGaN barriers and aluminum contents of structures S_1 to S_4.

Looking at Fig. 3.5 it can be concluded that the 2DEG concentration of structure S_1 must

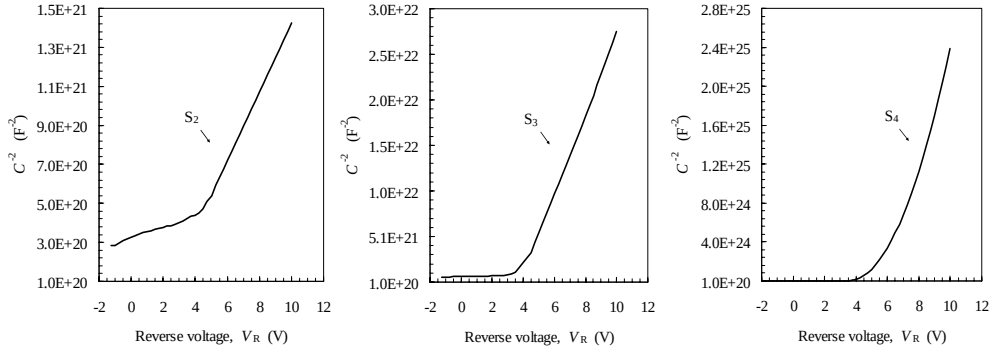

Figure 3.6: Typical ($1/C^2$-V_R) plots of our first (S_2), nearly optimized (S_3), and optimized (S_4) AlGaN/GaN layers on sapphire substrates.

be low as the area under the (C-V) profile is a measure of the total charge in the 2DEG. The low sheet charge density is due to the facts that the barrier layer is too thin and the actual aluminum content is lower than expected. Photoluminescence and Raman spectroscopy showed that the actual aluminum content of the AlGaN barrier of structure S_1 was about 10% which is significantly lower than the intended content of 20%. In addition it should be mentioned that the surface morphology of the AlGaN barrier layer of this structure was quite rough. This large surface roughness was reflected in the rather low mobility of the 2DEG electrons of about 1100 cm^2/Vs that has been determined by Hall measurements.

In an attempt to improve the surface morphology Grzegorczyk *et al.* [50] annealed the top GaN layer before deposition of the AlGaN layer. Unfortunately, this method significantly increased the leakage current in the HFET structure. The (C-V) profile of structure S_2 clearly shows that the channel can not be depleted by the applied reverse bias voltage. This is due to the high residual free carrier concentration of the GaN buffer layer as can be calculated from the slope of the ($1/C^2$-V_R) plot of structure S_2 which is shown in Fig. 3.6. The residual free carrier concentration in the GaN buffer layer of structure S_2 equals 10^{19} cm^{-3}, which obviously is unsuitable for application in a device. Figure 3.7 shows the measured free carrier concentration as a function of the depletion depth (x_d) for structures S_1 to S_4. Despite Debye length smearing that occurs during (C-V) profiling of heterojunctions using a Schottky contact, Kroemer *et al.* [92] have shown that in such a process the number of the charge carriers is conserved. Hence, (C-V) profiling can be used to calculate the sheet charge density of the 2DEG (n_s) by

$$n_s = \int_0^\infty \hat{n}(x)\,dx, \tag{3.7}$$

where $\hat{n}(x)$ is the measured free carrier concentration. Using Eq. 3.7 the sheet carrier density of structure S_2 is calculated to be 1.2 x 10^{13} cm^{-2}. Grzegorczyk *et al.* [50] have improved the

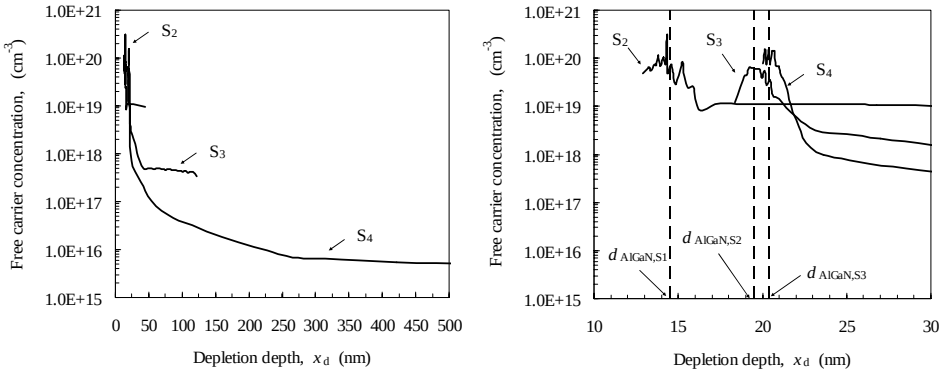

Figure 3.7: Typical profiles of the doping concentration as a function of the depletion depth of our first (S_2), nearly optimized (S_3), and optimized (S_4) AlGaN/GaN layers on sapphire substrates (*left*), and close-up of 2DEG region for determination of the thickness of the AlGaN barrier layer.

surface morphology of the AlGaN layer by optimization of the growth conditions. Structure S_3 represents a nearly optimized AlGaN/GaN HFET structure. Figure 3.5 shows that the sheet carrier density of the 2DEG is expected to have a reasonable value. Furthermore channel depletion has been improved but the GaN buffer layer seems still not to be resistive enough. Figures 3.6 and 3.7 confirm the latter as the free carrier concentration in the GaN buffer layer is calculated to be 2.7 x 10^{17} cm^{-3}. The sheet carrier density of this structure has been calculated using Fig. 3.7 and equals 8.3 x 10^{12} cm^{-2}.

Structure S_4 represents the optimized AlGaN/GaN HFET structure as the (*C-V*) profile shows excellent channel depletion which implies that the resistivity of the GaN buffer layer is high enough. Figures 3.6 and 3.7 confirm the latter as the residual free carrier concentration in the GaN buffer layer is calculated to be 6 x 10^{15} cm^{-3}. The sheet carrier density of structure S_4 equals 9.5 x 10^{12} cm^{-2}. The Hall carrier mobilities of structures S_3 and S_4 are 1350 cm^2/Vs and 1400 cm^2/Vs, respectively. These values confirm that the surface roughness at the AlGaN/GaN interface has been reduced. Comparison of the thicknesses of the AlGaN barrier layers listed in Table 3.1 and the thicknesses determined in Fig. 3.7 shows that these values are in good agreement.

Fig. 3.8 shows reverse (*I-V*) measurement results of structures S_2, S_3, and S_4. These curves clearly show that the leakage currents of the Schottky diodes on the different structures strongly depend on the resistivity of the GaN buffer layer. It has to be noted that the residual free carrier concentration of the GaN buffer layers in the complete AlGaN/GaN layer stacks is higher than in single GaN buffer layers. The exact mechanism for this increase is still under investigation by Rudzinski *et al.*

After developing the growth of the AlGaN barrier layer on sapphire substrates the researchers at RUN have transferred this growth process onto s.i. 4H-SiC substrates. The

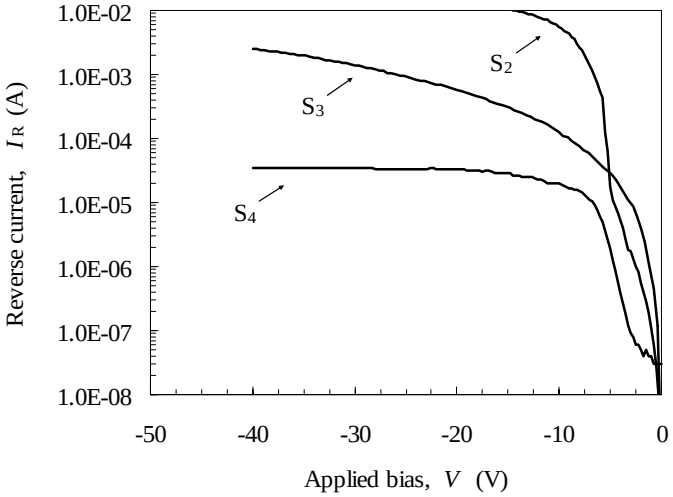

Figure 3.8: Typical reverse (*I-V*) characteristics of Schottky diodes on our first (S_2), nearly optimized (S_3), and optimized (S_4) AlGaN/GaN layers on sapphire substrates.

same development sequence of growth and characterization has been carried out. Rudzinski *et al.* [146] managed to grow n.i.d. AlGaN barrier layers with a thickness of 30 nm, an aluminum content between 25% and 30%, and a very smooth surface morphology. The resulting Hall mobility of the 2DEG electrons varied between 1300 cm^2/Vs and 1500 cm^2/Vs. By inserting a very thin, typically 1 nm AlN layer between the GaN buffer layer and AlGaN barrier layer they succeeded in improving the Hall mobility to values between 1700 cm^2/Vs and 1900 cm^2/Vs at room temperature. The very thin AlN layer not only improved the carrier mobility due to reduced alloy scattering at the heterojunction but also improved the confinement of the 2DEG as a result of the increased discontinuity in the conduction band. The residual free carrier concentration of the GaN buffer layers was low, typically 3.5 x 10^{13} cm^{-3}, which resulted in very low leakage currents, typically 1 x 10^{-7} A. The latter enables a high breakdown voltage (V_{BD}) which is one of the necessary conditions to realize high output powers as has been discussed in Sect. 2.3.4.

3.1.5 Complete AlGaN/GaN epitaxial layer stack

For the fabrication of small and large gate periphery microwave high-power HFETs we have used n.i.d. AlGaN/GaN epilayers on s.i. 4H-SiC substrates. Table 3.2 provides an overview of the thicknesses of the GaN and AlGaN layers, the aluminum content of the latter, the sheet resistance (R_{sheet}), the 2DEG sheet carrier density, and the Hall mobility of the 2DEG electrons for the different layer stacks. Wafer 1203 is the only structure with an Fe-doped GaN buffer layer. The Fe doping concentration in the first 0.3 μm of this layer is 5 x 10^{18} cm^{-3}. In

Table 3.2: Overview of the n.i.d. AlGaN/GaN epilayers on s.i. 4H-SiC substrates.

Wafer	Layer stack	d_{GaN} (μm)	Fe	d_{AlGaN} (nm)	Al (%)	R_{sheet} (Ω/sq.)	n_s (cm^{-2})	μ (cm^2/Vs)
1200	AlGaN/AlN/GaN	1.2	no	30	26	350	9.5 x 10^{12}	1875
1201	AlGaN/GaN	1.2	no	30	26	440	9.3 x 10^{12}	1515
1203	AlGaN/GaN:Fe	1.4	yes	30	26	530	8.8 x 10^{12}	1352

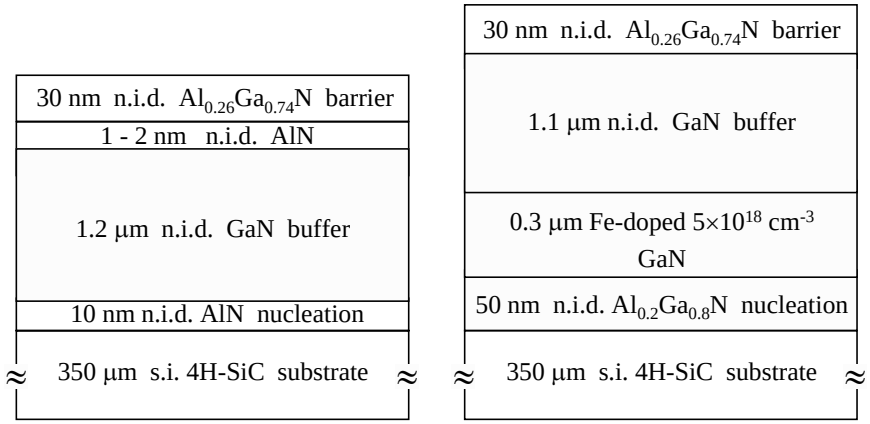

Figure 3.9: Schematic overviews of the completely n.i.d. AlGaN/GaN epilayers on s.i. 4H-SiC (*left*) and of the structure with the Fe compensation doped GaN buffer layer (*right*).

addition, the nucleation layer of this structure is a 50 nm AlGaN layer with an aluminum content of 20%. In the case of the completely n.i.d. structures the nucleation layer is a 10 nm AlN layer. Figure 3.9 shows schematic overviews of the completely n.i.d. AlGaN/GaN epilayers (*left*) and the structure with the Fe compensation doped GaN buffer layer (*right*).

3.2 Device layout and process flows

The next step towards the realization of microwave high-power AlGaN/GaN HFETs is the design of a suitable device layout. We will describe the key aspects that have led to the design of mask sets for both small and large periphery devices. Furthermore we will present schematic overviews of the process flows whose detailed descriptions are given in Appendix A.

3.2.1 Mask layout

We have designed layouts for both small and large gate periphery devices. For short loop experiments where fast feedback is very desirable as they are performed for process development and optimization, we have used small gate periphery devices. The gates of these devices have a total width (W_g) of 80 μm and consist of two parallel gate fingers with a unit gate width (W_{gu}) of 40 μm. The mask set for these small devices consists of the following steps:

1. device isolation by mesa etching,
2. formation of ohmic contacts,
3. formation of Schottky contacts and ground-signal-ground (GSG) probe pads, and
4. etching of openings in the silicon nitride passivation layer (optional).

The gates of these devices are defined using optical contact lithography and have a gate length (L_g) of 2 μm. In the remainder of this thesis, devices with such long gates are referred to as "*fat gate*" devices. Usually, device isolation is done after ohmic contact formation. We have investigated the influence of mesa etching on leakage currents of AlGaN/GaN devices and found that the leakage current levels can significantly be reduced if mesa etching is done as the first step in the process flow. The details of this investigation have been described in the thesis of B. Jacobs [67]. As our process flow starts with mesa isolation, the mask set used for processing small fat gate devices is called the "*Inverse Mesa*" mask.

Using the Inverse Mesa mask set, devices can be made with a drain-source spacing (L_{ds}) of 10 μm. As the fat gates are placed in the middle of this gap the gate-source (L_{gs}) and gate-drain (L_{gd}) spacings are equal, i.e. 4 μm. Figure 3.10-(*left*) shows an optical microscope picture of a small fat gate device. The dimensions of the GSG probe pads contacting the gate, drain, and source regions of the device are indicated. The gate-to-gate pitch (L_{gg}) of these devices is 60 μm. Figure 3.10-(*right*) shows a SEM image of the active region of the same device. The unit width (W_{gu}) and L_g of the fat gates are indicated.

As we want to fabricate HFETs that can operate at microwave frequencies, e.g. X-band, we have seen that the gate length has to be reduced to sub-micrometer values in the range of 0.25 μm - 0.5 μm. To fabricate these gate lengths we have switched from optical contact lithography to electron beam lithography (EBL), which will be discussed in more detail in Sect. 4.3. For quick development of this process step and to suppress the influence of heating effects on the device results as much as possible we have designed a mask set based on the Inverse Mesa principle. This mask set is called "*Submu*" referring to the sub-micrometer length of the gate contacts. In this layout the source-drain spacing is reduced to lower the drain-source resistance (R_{ds}) and the sub-micrometer gates are placed closer to the source than to the drain contact. The latter has been done for two reasons. First to increase the speed of the device as the electrons sooner start drifting through the channel at the saturated velocity (v_{sat}) and second to maintain a high breakdown voltage, typically 80 V - 100 V, as the largest electric field exists across the drift region in the gate-drain spacing. The internal device dimensions of the Submu mask set are: L_g = 0.25 μm, W_g = 80 μm, W_{gu} = 40 μm, L_{gg} = 60 μm, L_{gs} = 1 μm , L_{gd} = 2 μm ,and

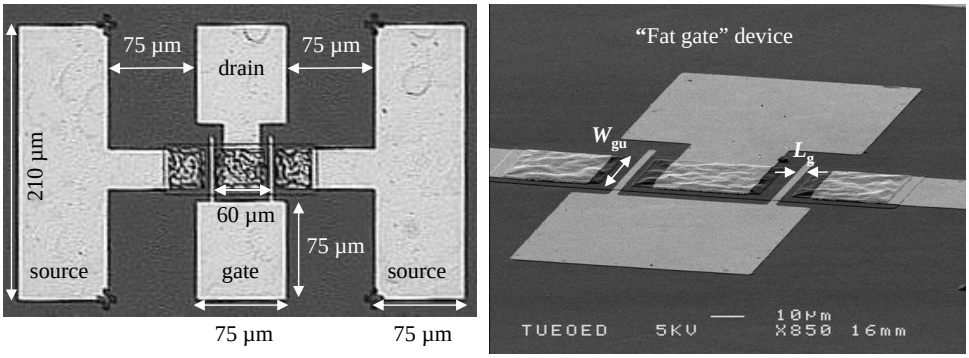

Figure 3.10: Optical microscope picture of a small fat gate device showing dimensions of GSG probe pads and gate-to-gate pitch (*left*) and SEM image of active region of the same device indicating unit width (W_{gu}) and length (L_g) of the fat gates (*right*).

L_{ds} = 3.25 μm. Figure 3.11 shows a SEM image of the active region of a small submicron gate device. The strongly reduced L_{ds} and L_g can clearly be seen. It has to be noted that the Submu mask set for reference purposes contains devices, which have the same internal dimensions as those of the Inverse Mesa mask set.

With the previously described mask sets it was only possible to fabricate small gate periphery (80 μm) devices. As we want to realize actual high-power devices the total gate width of the devices has to be increased to eventually 1 mm and beyond. To achieve this, we have designed a mask set named "mmTor" which refers to the fact that the design contains devices with gate peripheries of 1 mm and more. Key aspects that need to be considered in the design of microwave large gate periphery devices are the following:

- gate length (L_g),
- total gate width (W_g),
- unit gate width (W_{gu}),
- gate-to-gate pitch (L_{gg}),
- layout of the gate fingers,
- gate-source spacing (L_{gs}), and
- gate-drain spacing (L_{gd}).

As mentioned before, the gate length of HFETs that have to operate at X-band frequencies (8 GHz - 12.4 GHz) has to be in the range of 0.25 μm - 0.5 μm to achieve values for f_T higher than 40 GHz. In addition, a shorter gate length contributes to the increase of the drain

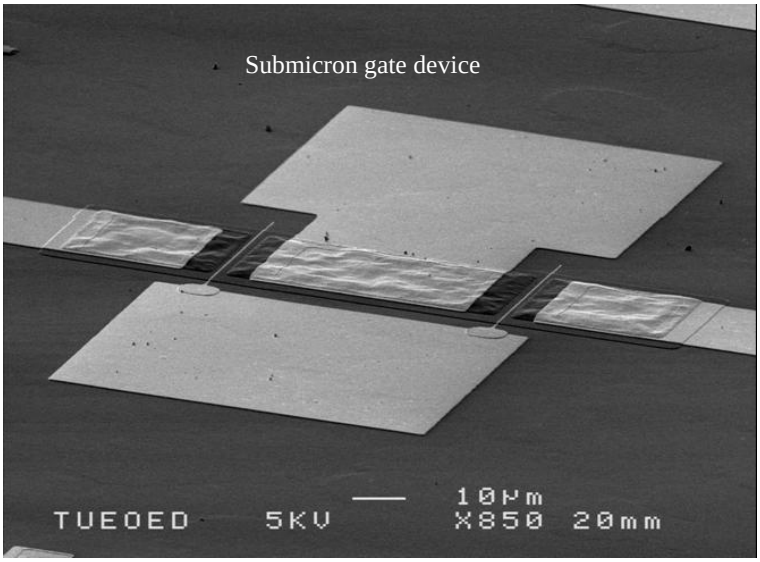

Figure 3.11: SEM image of the active region of a small submicron gate device. The strongly reduced drain-source spacing (L_{ds}) and gate length (L_g) can clearly be seen.

current of the device as the latter is proportional to the gate width over gate length (W / L) ratio. According to this ratio, W_g has also to be increased to achieve higher output powers. For microwave HFETs this cannot be done by simply increasing the gate width of only one or two gate fingers as the power gain of the devices significantly decreases with gate width. This decrease is caused by increased attenuation and phase shift of the ac signal along the gate fingers. Therefore the total gate width of the transistor has to be increased by placing several gate fingers in parallel. However, the maximum width of one such finger, W_{gu}, decreases with frequency. In practice it has been shown that the value of W_{gu} for GaAs HFETs operating at X-band is limited to approximately 125 μm [39]. Knowing this boundary condition the number of gate fingers that have to be placed in parallel to obtain a certain total gate width can easily be calculated. However, it has to be noted that the maximum number of gate fingers is determined by the maximum phase shift allowed to the outer gate fingers of the device, the distance between the parallel gate fingers, which is referred to as the gate-to-gate pitch (L_{gg}), and the input impedance of the HFET which decreases with the number of gate fingers. From literature [165] it is known that to still consider the transistor as a lumped element, the maximum distance allowed between the outer gate fingers should not exceed one sixteenth of the wavelength of the ac signal. At 10 GHz this distance for GaN HFETs corresponds to 625 μm. From an electrical point of view the gate-to-gate pitch should be as small as possible to reduce phase shift of the ac gate signal and the corresponding power gain reduction. However,

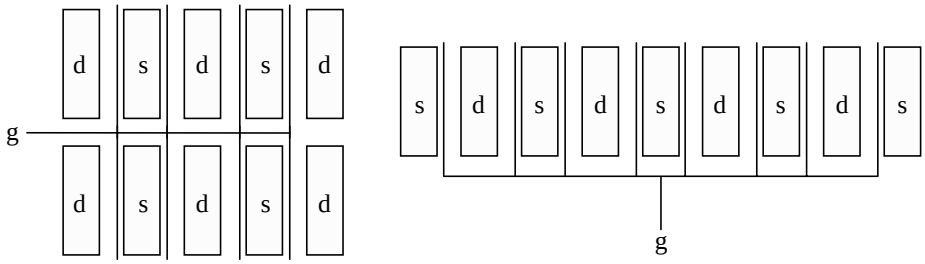

Figure 3.12: Schematic representation of the fishbone layout (*left*) and interdigitated or comb layout (*right*). The gate, source, and drain electrodes are indicated.

from a thermal point of view L_{gg} should be maximized to avoid device degradation due to too high channel temperatures in the vicinity of the gates, which cause significantly compressed output power and strongly reduced power gain. In addition, reliability of the devices is a strong function of temperature as most failure mechanisms are due to diffusion of atoms, which is a process that is accelerated at high temperatures. Channel temperatures for GaN-based HFETs depend on the substrate used, the power dissipated, and the power added efficiency (PAE). For increasing dissipated power at a constant PAE, channel temperature increases. For increasing PAE at a constant dissipated power, channel temperature decreases. For sapphire and SiC substrates at a dissipated power density of 6 W/mm the channel temperatures range between 300 °C - 400 °C, and 180 °C - 240 °C, respectively [45].

The next important design aspect is the layout of the parallel gate fingers. Figure 3.12 shows a schematic representation of the two most commonly used layouts used for microwave high-power devices, which are known as the fishbone layout (*left*) and the interdigitated or comb layout (*right*).

Using the fishbone layout the highest output power per chip area can be obtained because this layout results in the most square transistor layout [39]. Figure 3.12 clearly shows that if the number of gate fingers is increased the comb layout will quickly become very long. If a number of these transistors are combined in a high-power amplifier, the dimensions of the matching networks also become very large. As a result the losses of the matching networks increase. This is not the case for fishbone transistors because they can be designed in such a way that the matching networks remain as small as possible. In addition, a fishbone transistor has highest power gain because more gate fingers with a smaller unit gate width are placed in parallel than for a comb transistor with the same total gate width. Finally, we have already mentioned that L_{gs} and L_{gd} are very important design parameters influencing the speed and breakdown voltage of the devices, respectively.

The mmTor mask set comprises of small and large gate periphery multi-finger devices in both the fishbone and comb layouts. Both layouts have been implemented with or without

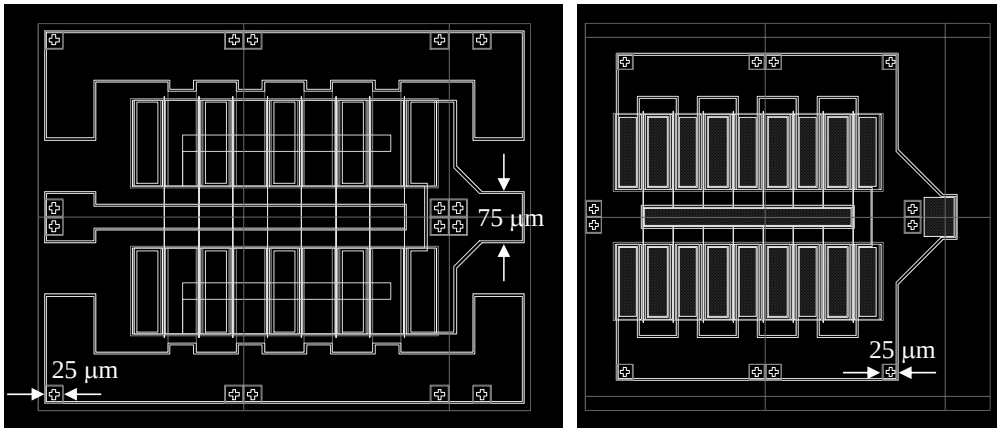

Figure 3.13: Fishbone layout with (*left*) and without GSG probe pads (*right*).

GSG probe pads. Devices with GSG probe pads require air bridges to connect the drain or source contacts in the device in the case of a fishbone or comb layout, respectively. Devices without GSG probe pads can be used in a hybrid implementation of a high-power amplifier. This requires flip-chip technology to connect the active and passive components which are fabricated on different substrates. Figures 3.13 and 3.14 show examples of the fishbone and comb layouts with (*left*) and without GSG probe pads (*right*).

The mask set contains a variety of device dimensions, alignment marks for optical and electron beam lithography, and test structures for process monitoring, e.g. circular TLM to determine ohmic contact resistance, Schottky contacts, single gates to determine the gate resistance (R_g), and Vernier structures to check the overlay accuracy of the EBL process. Figure 3.15 shows an overview of the complete mmTor mask layout.

The central part of the layout, which contains all transistor types and measures 11.3 x 11.3 mm^2, is highlighted. Inside this part four units can be distinguished. Unit 1 consists of transistors with relatively small total gate widths of 0.25 mm and 0.5 mm. Unit 2 consists of devices with a total gate periphery of 1.0 mm. In unit 3 transistors with total gate peripheries of 1.2 mm and 2.0 mm are located. Finally, unit 4 comprises really large devices with gate widths of 3.0 mm, 3.2 mm, 4.0 mm and 6.4 mm. Units 1 and 2 have been copied above the central part and units 3 and 4 have been copied below it. Hence we can choose to process mainly small periphery devices, small and large periphery devices and mainly large periphery devices. We have used values for W_{gu} of 62.5 μm, 100 μm, 125 μm, and 200 μm. The latter unit gate width obviously is too large for devices that have to operate at X-band. However, we have incorporated this unit gate width because we are also interested in the power capability of the GaN-based HFETs at S-band (2GHz - 4 GHz). The internal dimensions of all devices in the central part are: L_{gs} = 1.2 μm, L_{gd} = 3.0 μm, L_g = 0.7 μm, L_{gg} = 50 μm. On the left hand

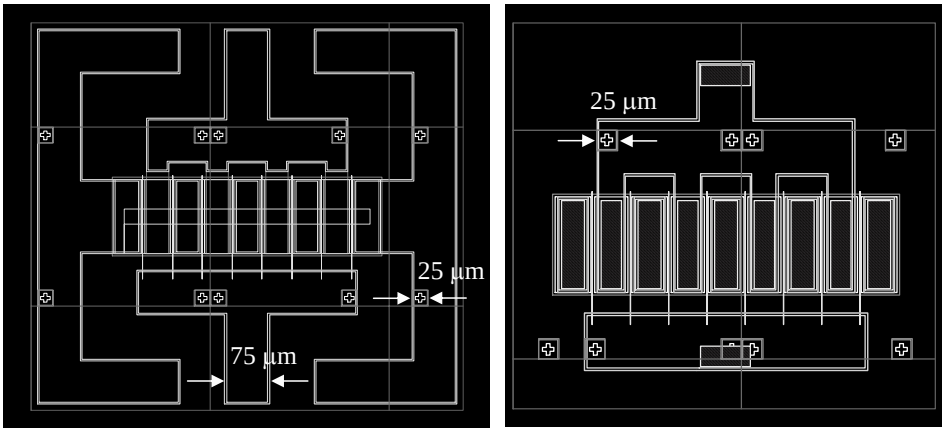

Figure 3.14: Comb layout with (*left*) and without GSG probe pads (*right*).

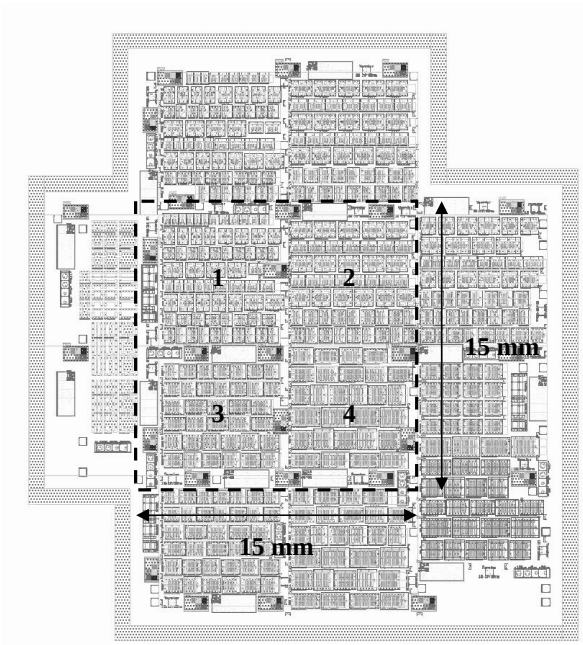

Figure 3.15: Overview of the complete mmTor mask layout. Highlighted is the central part showing the four basic units.

side of the central part we have incorporated test structures to characterize the GSG probe pads that are used in the devices with air bridges. On the right hand side of the central part we placed transistors with a total gate width W_g of 1.0 mm in which the value for L_{gg} is varied, i.e. 30 μm, 40μm, 50μm, and 60 μm, to determine the trade-off between the thermal and electrical behavior of the transistors. In this part we also incorporated devices with a total gate width of 1.0 mm in which the value for L_{gd} is varied, i.e. 1.0 μm, 2.0 μm, 3.0 μm, 4.0 μm, and 5.0 μm, to investigate the breakdown behavior of the HFETs. In addition, we want to mention that the mask is suitable for processing either using only positive resists or a combination of positive and negative resists.

3.2.2 Process flows

Figures 3.16 and 3.17 show schematic overviews of the main steps in the process flows of the Inverse Mesa and mmTor mask sets, respectively. Detailed descriptions of the process flows for all mask sets can be found in Appendix A.

3.3 Conclusions

In this chapter we have focused on design aspects of microwave high-power AlGaN/GaN HFETs on both sapphire and s.i. SiC substrates. With respect to the development of the MOCVD growth process the following conclusions can be drawn:

- Optimization of the growth process of the GaN buffer layer on sapphire substrates has shown that buffer layers with resistivities exceeding 10^4 Ωcm can be achieved in a controlled and reproducible manner if nitrogen is used as carrier gas during the deposition of the low-temperature GaN nucleation layer [50].

- GaN buffer layers on commercially available 2 inch s.i. 4H-SiC substrates with resistivities also exceeding 10^4 Ωcm can be obtained by both compensation doping with Fe and non-intentionally doping as has been done on sapphire substrates [146].

- The residual free carrier concentration of the GaN buffer layers was low, typically 3.5 x 10^{13} cm^{-3}, which resulted in very low leakage currents, typically 1 x 10^{-7} A. The latter are required to enable a high value for V_{BD}, which is one of the necessary conditions to realize high microwave output power.

- Non-intentionally doped AlGaN barrier layers with a thickness of 30 nm, an aluminum content between 25% and 30%, and a very smooth surface morphology have been grown on s.i. 4H-SiC substrates. The sheet carrier density and Hall mobility of the 2DEG electrons varied between 8.8 x 10^{12} cm^{-2} - 9.3 x 10^{12} cm^{-2}, and 1300 cm^2/Vs - 1500 cm^2/Vs at room temperature, respectively. By inserting a very thin, typically 1 nm, AlN layer between the GaN buffer layer and AlGaN barrier layer these values have been increased to 9.5 x 10^{12} cm^{-2} - 1.0 x 10^{13} cm^{-2}, and 1700 cm^2/Vs - 1900 cm^2/Vs.

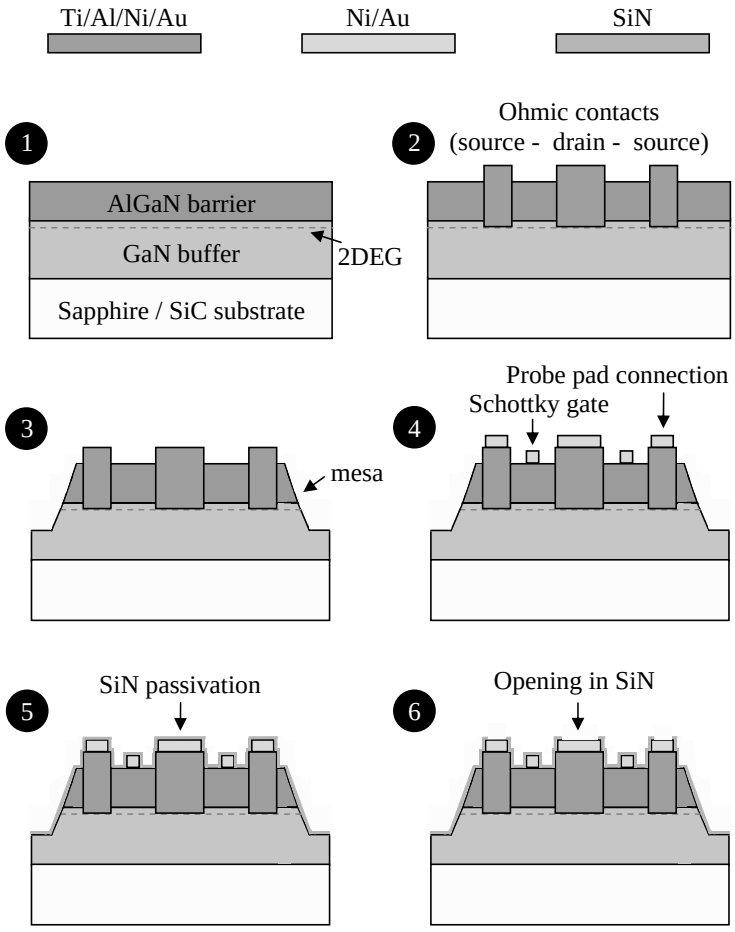

Figure 3.16: Schematic overview of the main steps in the process flow of the Inverse Mesa mask set.

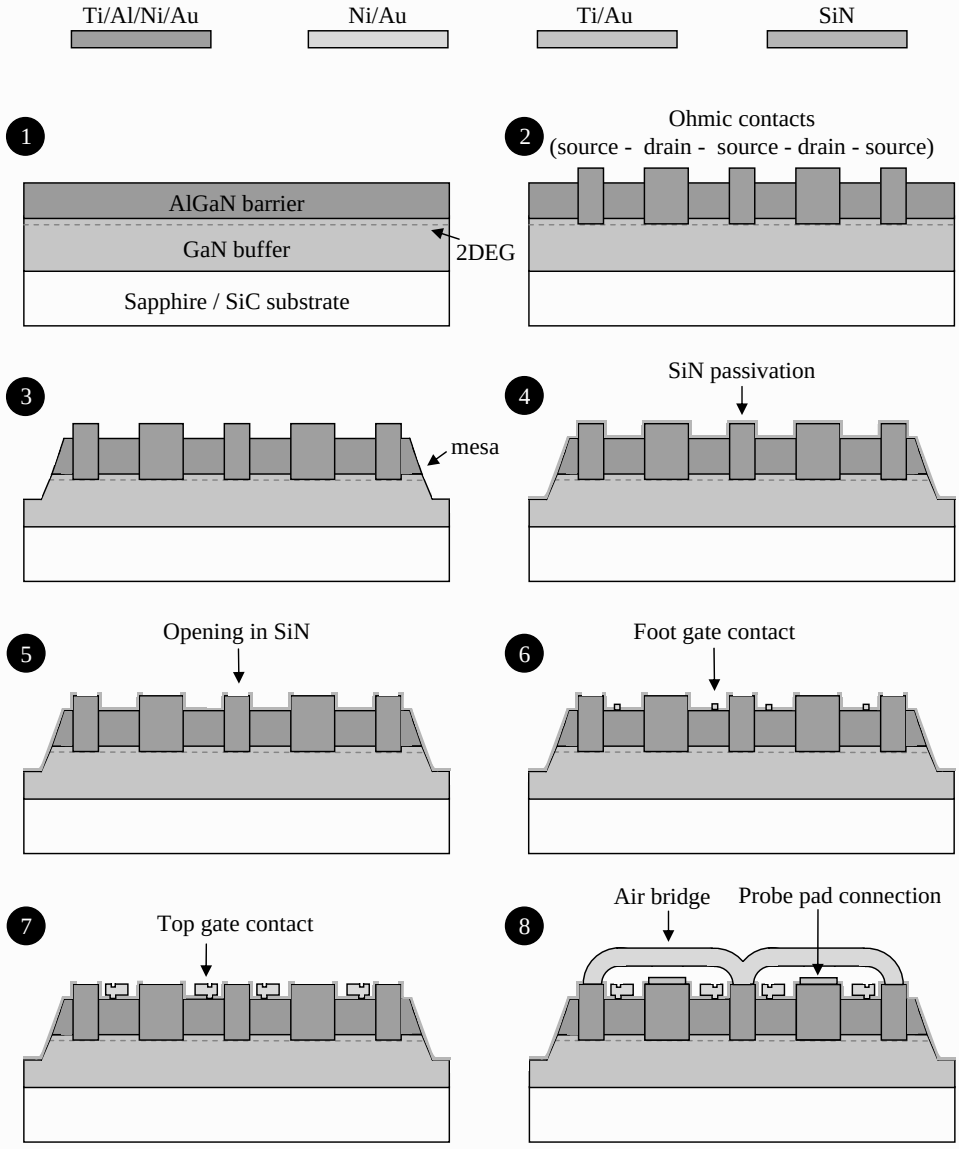

Figure 3.17: Schematic overview of the main steps in the process flow of the mmTor mask set.

For the fabrication of large periphery devices we have used an AlGaN/GaN structure on s.i. 4H-SiC consisting of a 1.4 μm Fe-doped GaN buffer layer, a 30 nm n.i.d. AlGaN barrier layer with an aluminum content of 26%. The residual free carrier concentration in the GaN buffer layer is 3.5 x 10^{13} cm^{-3}, the sheet carrier density in the 2DEG equals 8.8 x 10^{12} cm^{-2}, and the Hall mobility is 1350 cm^2/Vs. Device results from this material will be presented in Chapter 6.

Regarding device layout the following remarks can be made:

- The "Inverse Mesa" and "Submu" mask sets were very useful to fabricate small devices with W_g = 80 μm and values for L_g of 0.25 μm and 2 μm, respectively. These devices have been used in short loop experiments, which are performed for process development and optimization.

- The "mmTor" mask set enables the fabrication of large devices with sub-micrometer gate lengths and total gate widths ranging from 0.25 mm to 6.4 mm. These devices can be used at frequencies ranging from S-band (2 GHz - 4 GHz) to X-band (8.0 GHz - 12.4 GHz) have shown to achieve microwave high-power operation. We have discussed key aspects that need to be considered in the design of these devices, i.e. gate length, total gate width, unit gate width, gate-to-gate pitch, layout of the gate fingers, gate-source spacing, and gate-drain spacing.

- Finally, we presented schematic overviews of the main steps in the process flows of the Inverse Mesa and mmTor mask sets, respectively. Detailed descriptions of the process flows for all mask sets can be found in Appendix A.

Chapter 4

Fabrication technology

Having defined the epitaxial layer stack and the device layout, the next step is to develop the process technology needed to fabricate microwave high-power AlGaN/GaN HFETs. In this chapter we will describe key process steps of the fabrication process in the order of their appearance in the process flow of the mmTor mask set, which has been presented in Sect. 3.2.2. The chapter starts with contact technology, followed by device isolation, electron beam lithography, surface passivation, and ends with air bridge formation. Detailed descriptions of the different process steps can be found in Appendix A.

4.1 Contact technology

In this section we will describe the contact technology that has been used in our n.i.d. AlGaN/GaN HFETs. The fabrication of high-quality contacts is very important to achieve any high-performance device. In Sect. 2.3.4 it has been shown that maximum microwave output power is obtained if both the drain current swing and drain-source voltage swing are maximized. The former can be achieved by a high maximum drain current ($I_{\mathrm{D,max}}$) and low drain leakage current ($I_{\mathrm{D,leak}}$), and the latter can be realized by a high breakdown voltage (V_{BD}) and a low knee voltage (V_{knee}). First we will focus on ohmic contacts which should enable maximum drain current and low knee voltage. We will discuss the main requirements on these contacts for application in microwave high-power devices, provide a brief overview of reported contact technologies, and present our optimized contact scheme, which has been used in the large periphery devices whose performance will be presented in Chapter 6. The same approach will be followed for the Schottky contacts, which among others have to realize low gate and drain leakage currents and a high breakdown voltage.

4.1.1 Ohmic contacts

The first key process step, after preparing and cleaning of the sample and defining alignment marks for both optical and electron beam lithography (EBL), is the formation of ohmic contacts, which form the drain and source contacts of the HFETs. To enable high performance of the microwave high-power devices they have to meet the following requirements:

- lowest possible ohmic contact resistance (R_c),
- excellent line definition,
- smooth surface morphology, and
- high mechanical and thermal stability.

The lowest possible value for R_c is required to obtain $I_{D,max}$, reduce the on-resistance, which determines the slope of the linear region of the *I-V* output characteristics and hence the value of V_{knee}, and to minimize the power dissipated in the ohmic contacts because of the high current densities in power devices, typically 1.0 A/mm - 1.5 A/mm [8, 85, 174] for state-of-the-art AlGaN/GaN HFETs. Furthermore, to achieve high values for f_T and f_{max} the extrinsic transconductance ($g_{m,ext}$), which is given by Eqn. 4.1, should be maximized.

$$g_{m,ext} = \frac{g_m}{1 + g_m R_s} \tag{4.1}$$

In Eqn. 4.1, g_m is the intrinsic transconductance, and R_s is the source resistance, which is the sum of the sheet resistance between the gate and source contacts ($R_{sh,gs}$) and R_c. From Eqn. 4.1 it is obvious that R_s should be minimized. This has to be done by decreasing the sheet and contact resistances. The latter can be minimized by choosing an appropriate metallization scheme and optimization of the process technology used. The sheet resistance can be decreased through epitaxy and design, i.e. by reducing the gate-source spacing (L_{gs}). It is clear that the contacts need to have excellent line definition to position the gate very close to the source contact. In addition, good line definition is required to achieve a high breakdown voltage.

Smooth surface morphology and limited thickness of the ohmic contacts is very important to avoid alignment problems in optical contact lithography due to too much topography. Finally, the contacts should be mechanically stable, i.e. they should not be scratched away during testing or bonding, and they should not degrade due to the high temperatures that can arise during device operation. In Sect. 3.2.1 it has been mentioned that the channel temperature can be between 180 °C and 400 °C depending on the substrate used.

Most ohmic contacts on AlGaN/GaN heterostructures are based on titanium / aluminum (Ti / Al) based metallization schemes. The most frequently reported are the Ti/Al/Ti/Au, Ti/Al/Ni/Au, and Ti/Al/Pt/Au schemes [27, 108, 147]. The various metals in these schemes have their own specific role. Titanium is the first metal layer deposited on the AlGaN material and is believed to:

- serve as an adhesion layer to provide good mechanical stability [147],

- dissolve the native oxide on the AlGaN surface [107, 147], and
- create nitrogen vacancies (V_N) by reacting with nitrogen atoms in the AlGaN barrier layer. Hence, the AlGaN material underneath the contact becomes highly doped enabling electrons to tunnel through the remaining thin potential barrier which separates them from the 2DEG [108, 147].

Aluminum is supposed to:

- react with Ti to form an Al_3Ti layer that prevents oxidation of the underlying Ti layer [108, 147], and
- serves as a diffusion barrier for the Ni and Au layers as they form high Schottky barriers with the AlGaN barrier layer [107].

Nickel (Ni) and platinum (Pt) layers are used to form a diffusion barrier for the gold (Au) top layer. If this Au layer, which has been added to improve the conductivity of the metal stack, reacts with Al a highly resistive alloy is formed, which generally is called "purple plague". One of the most important reasons to add metals on top of Al is to prevent this layer from smearing out. Usually the ohmic contacts are annealed at high temperatures, typically $\geq 800\,^{\circ}$C, which is far above the melting point of Al ($660\,^{\circ}$C at atmospheric pressure). Without the additional Ni/(Pt)/Au layers the line definition of the contacts cannot be controlled.

Instead of the formation of tunnel contacts with one of the metallization schemes mentioned above, other techniques such as ion implantation using Si have been tried to realize ohmic contacts with low contact resistance. Yu *et al.* [177] have succeeded in fabricating n.i.d. AlGaN/GaN HFETs with ion implanted nonalloyed Ti/Al/Ni/Au ohmic contacts that show comparable contact resistance and device performance as HFETs fabricated using conventional tunnel contacts. Device fabrication starts with ion implantation in the source and drain regions because of the extremely high thermal budget of this process needed for activation of the Si dopants and damage recovery of the implanted AlGaN/GaN regions. The Si ions are implanted at a temperature of $200\,^{\circ}$C with doses of 1.5 x 10^{15} cm^{-2} at energies of 30 keV and 60 keV, with the dopant concentration peak overlapping with the 2DEG. In order to avoid ion channeling and non-intentional doping in areas outside the source and drain regions, the Si ion beam is tilted by 7° relative to the normal of the sample surface. After implantation, the activation and damage removal anneal was done at $1500\,^{\circ}$C with 100-bar N_2 overpressure for 1 minute. As deposited Ti/Al/Ni/Au contacts showed ohmic behavior and a contact resistance of 0.4 Ωmm. Very important advantages of the nonalloyed ion implanted ohmic contacts are the superior line definition and surface morphology, which can strongly improve yield, reproducibility, and reliability in AlGaN/GaN HFETs [177].

Initially, we have chosen to optimize the Ti/Al/Ni/Au tunnel contact for lowest contact resistance. Detailed descriptions of this optimization process can be found in [67, 91]. The optimized metal stack consisting of Ti/Al/Ni/Au = 30/180/40/150 nm yielded contact resistances of 0.2 Ωmm and 0.35 Ωmm on doped and undoped AlGaN/GaN layers, respectively [68]. However, these contacts show very rough surface morphology and poor line definition. These

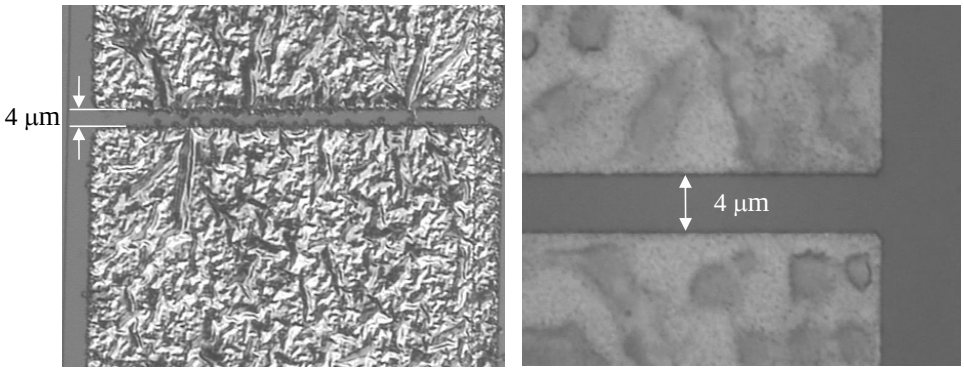

Figure 4.1: Line definition and surface morphology of the standard Ti/Al/Ni/Au (30/180/40/150 nm) contact (*left*), and for the modified (30/180/40/100 nm) contact (*right*) after RTA (800 °C, 2 min., N_2).

phenomena cause problems with alignment accuracy and early breakdown which are detrimental for the performance of microwave high-power devices.

Hilsenbeck et al. [59] reported that the Au/Al thickness ratio plays an important role in decreasing surface roughness and enhancing line definition of Ti/Al/Ni/Au ohmic contacts. They reported that an Au/Al thickness ratio of 0.55 yields the best line definition. In our contact the Au/Al thickness ratio is 0.83. From our work on optimizing contact resistance [67, 91] it becomes clear that the thickness of the Al layer cannot be changed as it is linked to the thickness of the Ti layer which should be 30 nm to achieve lowest contact resistance. Hence, the only possibility to decrease the Au/Al ratio is to decrease the Au layer thickness.

We have investigated the line definition, surface morphology, and contact resistance of Ti/Al/Ni/Au = 30/180/40/100 nm contacts on n.i.d. AlGaN (25 nm) / GaN (2 μm) heterostructures on sapphire substrates. Figure 4.1 shows the line definition and surface morphology of the standard Ti/Al/Ni/Au (30/180/40/150 nm) contact (*left*), and of the modified contact (*right*) after rapid thermal annealing (RTA) at 800 °C for 2 minutes in nitrogen (N_2) ambient.

Figure 4.1 clearly shows the significantly improved line definition and better surface morphology of the modified ohmic contact. The contact resistance of the improved ohmic contact using the standard RTA treatment with a ramp up time of only 15 seconds was 0.55 Ωmm. Upon increasing the ramp up time to 45 seconds, the contact resistance decreased to 0.15 Ωmm. In conclusion, the Ti/Al/Ni/Au = 30/180/40/100 nm ohmic contacts show enhanced line definition and surface morphology in combination with low contact resistance. These contacts have been used in the large periphery devices the performance of which will be presented in Chapter 6.

Table 4.1: Reported values of the work functions and barrier heights of the most commonly used Schottky metals to n-type bulk GaN [138, 143].

Metal	Work function (eV)	Barrier height (eV)
Pt	5.65	1.0 - 1.2
Ir	5.20	0.9 - 1.1
Ni	5.15	0.66 - 0.97
Pd	5.12	0.7 - 0.94
Au	5.10	0.8 - 0.93

4.1.2 Schottky contacts

Schottky contacts are very suitable gate electrodes for microwave devices because of their fast switching speed, typically in the picoseconds range, between forward and reverse current transport. This is due to the fact that they are mainly majority carrier devices and therefore hardly suffer from time delays caused by minority carrier storage effects. For application in microwave high-power devices Schottky gates are required to realize:

- low gate and drain leakage currents ($I_{\mathrm{G,leak}}$ and $I_{\mathrm{D,leak}}$),
- high breakdown voltage (V_{BD}),
- good adhesion,
- good thermal stability, and
- low gate resistance (R_{g}).

To ensure low gate and drain leakage currents and a high breakdown voltage, the barrier height between the gate metal and the AlGaN barrier layer should be as high as possible. Wide bandgap materials like AlGaN and GaN suffer much less from Fermi level pinning than semiconductors with small bandgaps like Si and GaAs. As a result, the work function of the metal applied has a stronger influence on the Schottky barrier height. In the case of n.i.d. or n-type bulk or relaxed material, metals with high work functions are used to realize high-performance Schottky contacts. Table 4.1 gives an overview of reported values of the work functions and barrier heights of the most commonly used Schottky metals to n-type bulk GaN [138, 143].

The spread on the reported values of the barrier height in Table 4.1 is believed to result from both the presence of several transport mechanisms and to material and process details such as the defect density of the films used, local stoichiometry variations, differences in surface roughness, and the effectiveness of surface cleans prior to metal deposition. Table 4.1 shows that the Schottky barrier height on n-type bulk GaN tends to increase with the work

function. However, Lin *et al.* [105] reported that the barrier height of Schottky contacts fabricated on strained AlGaN/GaN heterostructures shows the complete opposite behavior. In that case the barrier height is lower for metals with a higher work function. They explain this in the following way. The 2DEG electrons in strained AlGaN/GaN heterostructures originate from donor states at the surface of the AlGaN barrier layer. As electrons in metals with lower work functions have higher energy, they have larger moving spaces. As a result, their electron wave functions overlap more with those of the 2DEG electrons. This stronger coupling influences characteristics of the AlGaN surface states such as their density and energy levels and thereby directly affects the 2DEG sheet carrier concentration. This is shown by the difference between the calculated 2DEG sheet carrier concentrations using different Schottky metals and the 2DEG sheet carrier concentration determined using Hall measurements, i.e. without a Schottky contact, which increases as the metal work function decreases. At the same polarization sheet charge density, barrier heights of Schottky contacts are higher because of the decreased 2DEG sheet carrier concentration. Therefore, due to the significant influence on the characteristics of AlGaN surface states, the barrier heights of Schottky contacts on strained AlGaN/GaN heterostructures are higher for lower metal work functions [105].

From the metals listed in Table 4.1 Ir and Ni have the best adhesion to AlGaN and GaN epilayers, which is very important to avoid metal breaking off the surface during device processing, e.g. during lift-off. Good thermal stability of the Schottky contacts is required as the channel temperature of AlGaN/GaN HFETs can get very high, typically between 180 °C and 400 °C depending on the substrate used, the bias conditions and the power dissipated [45, 93, 97]. The resistance of the Schottky gates (R_g) should be low as it not only determines the input impedance but also strongly influences the values of f_{max}, maximum available gain (MAG), and minimum noise figure (NF_{min}) of the HFETs. The gate resistance can be decreased if T-shaped or so-called mushroom gates are used. We will discuss this topic into more detail in Sect. 4.3. Further reduction of the gate resistance can be achieved using copper (Cu) as contact metal. Ao *et al.* [11] have reported Cu gates on strained AlGaN/GaN heterostructures whose gate resistance is 40% lower than that of comparable Ni/Au Schottky gates. In addition, these Cu gates show much lower leakage currents than Ni/Au contacts processed on the same material, which is attributed to the fact that the barrier height of the Cu gates is higher than that of the Ni/Au gates as the work function of Cu (4.65 eV) is lower than that of Ni (5.15 eV). This is in complete agreement with the work of Lin et al. [105].

Based on our previous studies with respect to Schottky contacts on AlGaN/GaN heterostructures [67, 91, 170] we have chosen to use Ni/Au = 20/200 nm gates in our HFETs. The thickness of the Au layer, which has been used to enhance conductivity and prevent the oxidation of Ni, is arbitrary. Because of our choice to use AlGaN/GaN heterostructures it is difficult to apply conventional characterization techniques such as (*I-V*) and (*C-V*) to determine Schottky contact characteristics like barrier height and ideality factor. This is due to the fact that this system consists of two back-to-back series diodes, i.e. the Schottky diode and a diode as a result of the bandgap discontinuity at the heterojunction. Therefore we have optimized the Ni/Au contacts for lowest reverse current and highest breakdown voltage.

The main focus of these studies was to develop a suitable pre-metallization surface clean to improve the performance, stability and reliability of the Ni/Au Schottky contacts. We have

found that for high-power applications a surface clean with ammonium hydroxide (NH_4OH) for 15 minutes just before electron beam evaporation of the Ni/Au layers yielded the lowest reverse currents, typically 6 x 10^{-5} A at a reverse bias of 100V. However, in the mmTor process flow this pre-metallization surface clean caused severe adhesion problems with the copolymer (MMA(8.5)MAA EL13). As the AlGaN surface is cleaned using an ammonia dip for 1 minute before passivation with silicon nitride (SiN), see Appendix A, the surface clean just before Ni/Au evaporation has been omitted. Reverse (*I-V*) measurements of Schottky test structures showed leakage currents of 400 μA/mm and breakdown voltages around 150 V. These results indicate that our Ni/Au Schottky contacts are perfectly suitable for application in high-power HFETs.

4.2 Device isolation

Electrical isolation of active devices on the same chip can be achieved by significantly increasing the resistivity of the conductive material between them using ion implantation or by completely removing the conductive material. The latter can be realized by etching mesa structures using either wet chemical etching or dry etching techniques such as reactive ion etching (RIE), inductively coupled plasma etching (ICP), chemically assisted ion beam etching (CAIBE), or electron cyclotron resonance etching (ECR). As described in Sect. 2.2.1 wurtzite GaN crystals have either a N- or Ga-face with different properties affecting among others device technology. N-face crystals are chemically active, which enables wet-chemical etching of the material. However, Ga-face crystals, which are preferred for application in devices because of their superior electrical properties, are almost chemically inert. Ga-face material can only be etched wet chemically either by using acids or bases at elevated temperatures (up to 75 °C), which is known as orthodox etching [169], or by using a potassium hydroxide (KOH) solution at room temperature in combination with ultraviolet (UV) light, known as photo enhanced chemical etching (PEC) [175]. Due to the rather poor uniformity and rough surface morphology of the etch results these techniques are not suitable for device processing leaving dry etching as the only viable option to fabricate mesa structures for device isolation.

4.2.1 RIE

In the past we have fabricated mesas by RIE using an Oxford Plasma System 100 equipped with a load-lock. The plasma chemistry used consisted of argon - silicontetrachloride (Ar:$SiCl_4$ = 10 sccm : 10 sccm) at a pressure of 40 mTorr, RF (13.56 MHz) power of 70 W, DC bias of -288 V, and a temperature of 20 °C. Using this process we achieved etch rates for AlGaN and GaN of 5 nm/min and 6 nm/min, respectively and a very nice surface morphology of the etched GaN material. This can clearly be seen by comparing the surface morphologies of the unetched AlGaN (mesa) and RIE etched GaN buffer layers in the SEM image shown in Fig. 4.2. To pattern the mesas we have used photoresist (AZ4533) instead of a silicon nitride hard mask. By appropriate baking of the photoresist a profile can be obtained that upon RIE etching renders sloped side walls. This has been done to minimize the risk of breaking of the

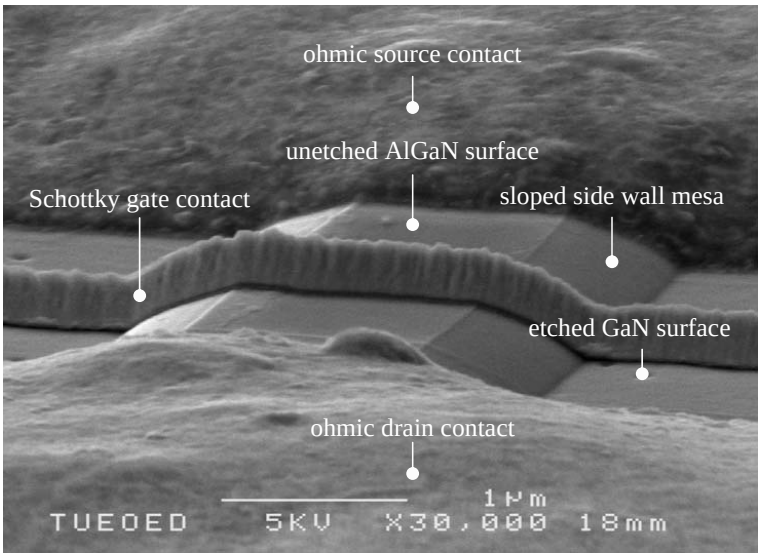

Figure 4.2: SEM image showing the surface morphologies of unetched AlGaN (mesa) and etched GaN layers using an Ar:$SiCl_4$-based RIE process (RF = 70 W, DC bias = -288 V, 40 mTorr, 20 ^oC). Furthermore the sloped side wall of the mesa can be seen and the gate running over the mesa.

Schottky gates due to too steep side walls.

The RIE process became obsolete for mesa etching as chlorine contamination of the chamber caused problems with the ohmic contacts that were exposed to a very low-power RIE argon plasma before rapid thermal annealing. Despite thorough chamber conditioning before this Ar plasma, residual chlorine caused aluminum from the ohmic metal stack to be dissolved and redeposited across the sample. This attack of the ohmic contacts resulted in dirt across the sample, in the source-drain region, and very rough contact edges which made positioning of the gate contact very difficult or even impossible. Figure 4.3 shows the results of chlorine attack on the ohmic contacts.

4.2.2 ICP

As the very low-power Ar plasma could only be carried out in the RIE system we had to develop the AlGaN/GaN mesa etch in the ICP system. This is also an Oxford Plasma System 100 equipped with an ICP source, load-lock and wafer clamp system. The carrier wafer used during the etch process is a 4 inch Si wafer. Wafer cooling is established by passing liquid nitrogen (LN2) through the etch table and by passing a helium (He) flow at the backside of the carrier wafer. Due to the high-power ICP source the plasma density in an ICP system is much higher than in a RIE system resulting in much higher etch rates and process temperatures.

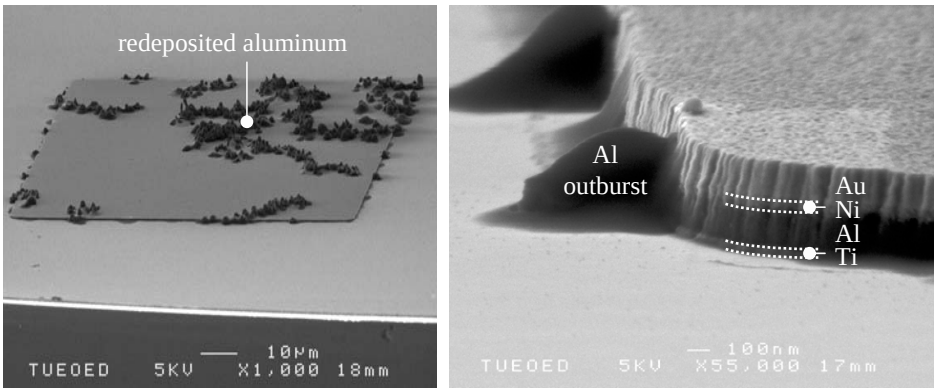

Figure 4.3: SEM images showing the redeposition of aluminum across the sample due to residual chlorine in the RIE process chamber (*left*), and aluminum outbursts at the edges of the ohmic contacts causing difficulties with respect to the positioning of the gate contact (*right*).

From literature it is known that the etch rate in an ICP process is mainly determined by the ICP power whereas the RF power mainly determines the surface morphology of the etched layers [103]. Typical power settings for ICP systems of ICP/RF = 2000/200 W, enable etch rates of several micrometers per minute which are suitable for through wafer via-hole etching but are completely impractical for etching AlGaN/GaN mesas with heights of 100-200 nm. In addition, the high process temperature renders photoresist useless as masking material. As we intend to use photoresist (AZ4533) as an etch mask to obtain sloped side walls, we had to considerably downscale the ICP etching rate and process temperature. As a starting point for our experiments we have chosen the two most commonly used plasma chemistries for AlGaN/GaN ICP etching known from literature, i.e. chlorine-argon (Cl_2/Ar) and chlorine-hydrogen (Cl_2/H_2), respectively [103, 137]. Our first experiments were carried out using Cl_2 : Ar = 30 sccm : 10 sccm at a pressure of 10 mTor at T = 20 °C with ICP/RF powers ranging from 500/50 W to 200/20 W, the latter being at the lowest power limit for obtaining a stable plasma. The resulting AlGaN/GaN etch rates ranged from 250 nm/min to 140 nm/min. It has to be noted that we have not considered selectivity between AlGaN and GaN as we have not used a recess etch in which selectivity of AlGaN with respect to GaN is critical. The SEM image in Fig. 4.4 shows a typical example of the surface morphology of the etched GaN buffer layer obtained using the Cl_2 /Ar chemistry.

For better process control and to achieve a smoother surface of the etched GaN layer we wanted to further decrease the etch rate. Therefore we tried the Cl_2/H_2 chemistry using the same ICP/RF power sweep as mentioned before. The resulting AlGaN/GaN etch rate ranged from 170 nm/min to 40 nm/min. SEM images of the etched samples showed that the smoothest GaN surface is obtained using ICP/RF powers of 200/50 W (etch rate of 110 nm/min). Lower ICP/RF power combinations, leading to lower etch rates (e.g. ICP/RF = 150/30 W, 40 nm/min),

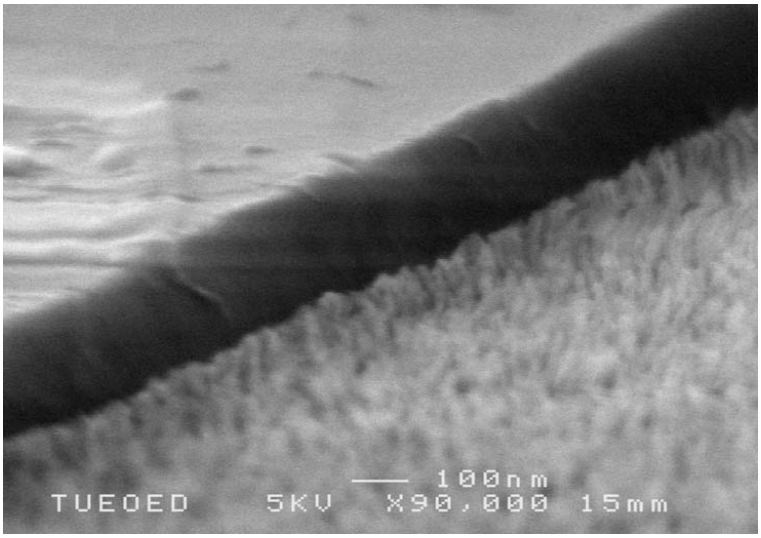

Figure 4.4: SEM image showing the surface morphologies of the AlGaN/GaN mesa and the etched GaN buffer layer using Cl_2 : Ar = 30 sccm : 10 sccm, ICP/RF = 200/20 W, p = 10 mTor, T = 20 °C.

result in rougher etched GaN surfaces. Figure 4.5-(*left*) shows the AlGaN/GaN mesa and the surface morphology of the etched GaN layer using Cl_2/H_2 = 30 sccm : 10 sccm with ICP/RF = 150/30 W, p = 10 mTor, at T = 20 °C. Figure 4.5-(*right*) shows a typical example of the very smooth surface morphology of the etched GaN layer using Cl_2/H_2 = 30 sccm : 10 sccm with ICP/RF = 200/50 W, p = 10 mTor at T = 20 °C. This process is very suitable for mesa etching and has been used in the transistor processing (see Appendix A).

Our ICP etching tool is used to etch several different materials using different gas chemistries. Hence, it was very important to isolate the AlGaN/GaN mesa etch process from these other processes by creating a process window in order to achieve reproducible etch results from run to run. To achieve this, we have embedded the actual mesa etch step in a process sequence consisting of the following steps: chamber cleaning, chamber conditioning, mesa etching, and again chamber cleaning. For chamber cleaning we have used an oxygen plasma (see Appendix A). To obtain a stable and reproducible AlGaN/GaN etch rate it is very important to carefully condition the process chamber as it is significantly affected by residual oxygen from the cleaning process. The residual oxygen enhances the ionization of chlorine and hence increases the etch rate. Chamber conditioning has been done using the process settings of the actual mesa etch process. We found out that for a stable etch rate of 110 nm/min, the chamber needs to be conditioned for more than 1 hour. As chlorine significantly etches the Si carrier wafer, which has to be used during this long conditioning step to protect the etch table, we have used a cyclic conditioning process to suppress excessive Si etching (see Appendix A).

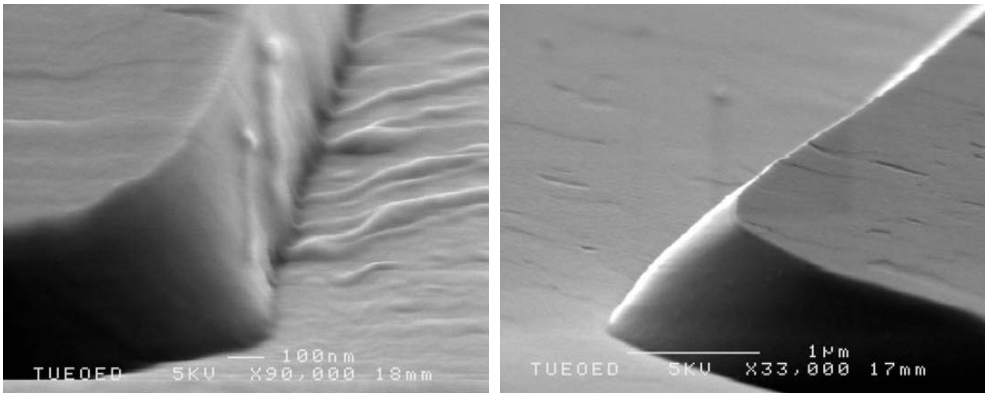

Figure 4.5: SEM images showing the surface morphologies of the AlGaN/GaN mesas and the etched GaN buffers layer using $Cl_2 : H_2$ = 30 sccm : 10 sccm, p = 10 mTor, T = 20 °C, for ICP/RF = 150/30 W (*left*) and ICP/RF = 200/50 W (*right*).

4.3 Electron beam lithography

To increase the operation frequency of devices, the internal device dimensions have to be scaled down to minimize the influence of parasitic geometrical capacitances and inductances. As mentioned in Sect. 3.1.1 for devices operating at X-band (8 GHz - 12.4 GHz) the gate length (L_g) has to be decreased to submicrometer dimensions, e.g. 0.25 μm - 0.5 μm, to achieve values for f_T larger than 40 GHz. The reasons to decrease the gate length in the case of a microwave high-power device are manifold because L_g has a significant effect on I_D, f_T, f_{max}, MAG, and NF_{min}, as is clearly indicated by Eqns. 4.2 - 4.6 [139].

$$I_D \propto \frac{W_g}{L_g} \tag{4.2}$$

$$f_T = \frac{v_{sat}}{2\pi L_g} = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \tag{4.3}$$

$$f_{max} = \frac{f_T}{2\sqrt{2\pi f_T R_g C_{gd} + G_{ds} R_{in}}} \tag{4.4}$$

$$\mathrm{MAG} = \frac{(f_T/f)^2}{4G_{ds}(R_{in}+\frac{\omega_T L_s}{2}) + 2\omega_T C_{gd}(R_{in}+R_g+\omega_T L_s)} \tag{4.5}$$

$$NF_{min} = 1 + K\frac{f}{f_T}\sqrt{g_m(R_g+R_s)} \tag{4.6}$$

In these formulas C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, G_{ds} is the output conductance, R_g is the gate resistance, R_{in} is the input resistance consisting of gate,

source, and channel components, $\omega_T = 2\pi f_T$, L_s is the source inductance, and K is a fitting parameter. From these equations it is clear that gate length reduction yields higher values for I_D, f_T, f_{max}, and MAG, and a lower value for NF_{min}. The minimum gate length that can be achieved depends on several issues, e.g. thickness of epitaxial layers to obey the high-aspect-ratio concept, suppression of short channel effects, and gate resistance. From Eqns. 4.4 - 4.6 it is clear that R_g has to be minimized to achieve maximum values for f_{max} and G_{max}, and a minimum value for NF_{min}. The microwave gate resistance, which has to be considered as the HFETs have to operate at microwave frequencies, is given by

$$R_g = \frac{\rho W_{gu}}{3mhL_g}, \tag{4.7}$$

where ρ is the resistivity of the gate metal used, W_{gu} is the unit gate width, m is the number of parallel gate fingers, h is the height of the gate metal, L_g is the gate length, and the factor of three in the denominator accounts for the distributed nature of the intrinsic gate region. A rigorous derivation of Eqn. 4.7 can be found in [1]. From Eqn. 4.7 it is clear that R_g increases as L_g is decreased. This can be prevented by increasing the number of parallel gate fingers (m), using a highly conductive metal, e.g. Cu, and increasing the height of the gate metal. The latter approach is not very practical as the aspect ratio of the gate, which is defined as h/L_g becomes very large making the gates very fragile during processing. In addition, the number of parallel gate fingers is limited by the rules discussed in Sect. 3.2.1.

4.3.1 T-gates

An approach commonly used to maintain low gate resistance upon shrinking the gate length is the fabrication of T-shaped or so-called mushroom gates. Figure 4.6 shows a SEM image of such a structure. The submicrometer footprint of these structures provides the short gate length and the bulky wide head maintains low gate resistance. Since optical contact lithography is not suitable to fabricate T-gates with submicrometer footprints other lithography techniques such as electron beam lithography (EBL) or nanoimprint lithography (NIL) have to be used. We have used EBL as this technique is most mature and commonly used in research environments. EBL in brief consists of scanning a beam of highly energetic electrons according to a desired pattern across a surface covered with a resist film. This resist consists of long organic polymer chains that are being cut (positive tone) or cross linked (negative tone) due to the energy of secondary and backscattered electrons. The changed structure of the resist in the exposed areas causes the dissolution rate to be different from that in unexposed areas upon putting it in a developer. The critical dimension (cd) is mainly determined by the spot size of the electron beam, the field size, and the bit size of the pattern generator used. The spot size of the electron beam depends on the acceleration voltage, thickness of the resist film, and semiconductor properties such as the atomic weight of the substrate constituents.

Usually T-gates are defined in a one-step electron beam writing process using a bi-layer PMMA/copolymer stack. Because of its high resolution polymethyl methacrylate (PMMA) is used to pattern the narrow footprint. For the wide top a mixture of PMMA and 8.5 % methacrylic acid (MMA8.5MAA), usually referred to as copolymer, is used because of its

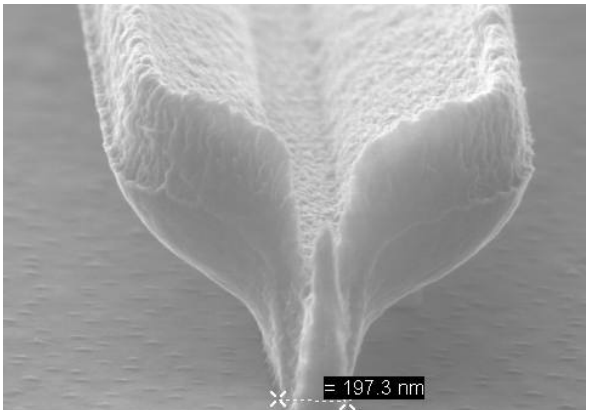

Figure 4.6: SEM image of a T-gate structure. Note the narrow footprint (197 nm) and the wide top. Courtesy of Dr. G. Schmidt, Universität Würzburg, Germany.

higher sensitivity to the electron beam. This difference in sensitivity is required for the one-step process in which the top is written with a much lower electron dose than the footprint, which has been written first. Also the step size used to write the footprint is much smaller, typically 1 pixel, to achieve best line width control. The minimum step size or single pixel size is defined as the ratio of the field size and the bit size of the pattern generator. In our case where we have used a field size of 300 μm and a 16 bit digital-to-analog converter (DAC), the single pixel size equals 5 nm (300 μm / 2^{16}). Figure 4.7 shows a SEM image of a T-gate that we have fabricated on AlGaN/GaN using a one-step process with a PMMA950K / MMA(8.5)MAA EL13 = 250/650 nm stack and the following settings: acceleration voltage = 20 kV, aperture size = 10 μm, field size = 300 μm, step sizes for the footprint and top of 5 nm and 15 nm, respectively, doses footprint and top are 80 μC/cm^2 and 60 μC/cm^2, respectively.

The EBL process on nonconducting substrates such as AlGaN/GaN on sapphire and s.i. SiC suffers from electrostatic charge-up of the sample surface due to the scanning electron beam. As a result of the negative charge buildup the electron beam is deflected and the writing process is disrupted. This problem can be solved by evaporating a transparent Au layer with a thickness of 12.5 nm on top of the PMMA/copolymer stack, which enables the electrons to be drained away to ground. However, it should be noted that this Au layer should be applied by thermal evaporation instead of e-beam evaporation. Some electrons from the e-gun, which are used to heat up the metal, escape the electric field that directs them into the metal crucible and completely expose the PMMA/copolymer during the evaporation. As a result the EBL process will fail because the structure of the PMMA/copolymer cannot be changed locally anymore.

4.3.2 Field plates

As mentioned in Sect. 2.3.4, AlGaN/GaN HFETs suffer from gate lag if the AlGaN surface has not been passivated properly using e.g. SiN. However, SiN passivated devices hardly suffering

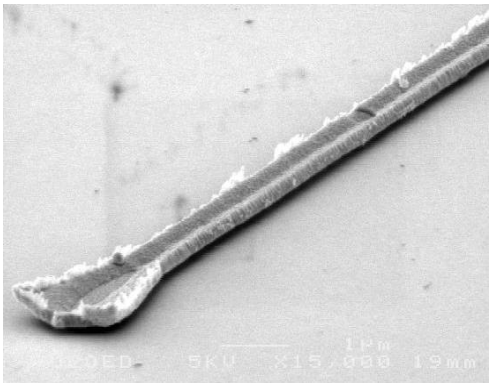

Figure 4.7: SEM image of a T-gate on AlGaN/GaN using a one-step process with a PMMA950K / MMA(8.5)MAA EL13 = 250/650 nm stack and the following settings: acceleration voltage = 20 kV, aperture size = 10 μm, field size = 300 μm, step sizes for the footprint and top of 5 nm and 15 nm, respectively, doses footprint and top are 80 μC/cm^2 and 60 μC/cm^2, respectively.

from gate lag have been reported to exhibit significant degradation of gate-drain breakdown voltage [181]. Hence, the trade-off between current collapse and breakdown voltage is a major difficulty for realizing the high-power capability of AlGaN/GaN HFETs. A similar problem has been encountered in Si and AlGaAs/GaAs power devices. In these devices the introduction of a field-modulating plate connected with the gate and extending towards the drain contact has not only shown to increase the breakdown voltage but also to suppress surface trapping effects [12, 28, 29, 34]. Zhang *et al.* [181] have used the field plate (FP) concept in AlGaN/GaN HFETs for the first time showing strongly improved breakdown voltages. In the original implementation the FP is directly connected to the gate finger and supported by a dielectric film. Chini *et al.* [30] were the first to introduce a different implementation in which the FP is separated from the gate finger by a dielectric film and connected to the gate finger only by the gate bus outside the intrinsic device. Although the maximum output power that can be achieved by the modified implementation is less, the value of C_{gd} has significantly been reduced. Reduced C_{gd} yields higher gain and efficiency as Miller feedback, which is a negative current feedback for which C_{gd} provides a path, has been decreased. Figure 4.8 shows schematic representations of the original (*left*) and modified (*right*) FP implementation.

The function of the field plate is to reduce the peak value of the electric field which occurs at the drain-edge of the Schottky gate and to redistribute the electric field along the 2DEG channel in the gate-drain spacing (L_{gd}). It should be noted that in AlGaN/GaN HFETs the highest electric field occurs at the AlGaN/GaN interface instead of the depletion region as is the case for GaAs MESFETs [104]. Specific for AlGaN/GaN HFETs is the role of the positive compensating charge (σ_{comp}) at the AlGaN surface, which helps to reduce and redistribute the electric field on the drain-edge of the Schottky gate. As discussed in Sect. 2.3.4, in the

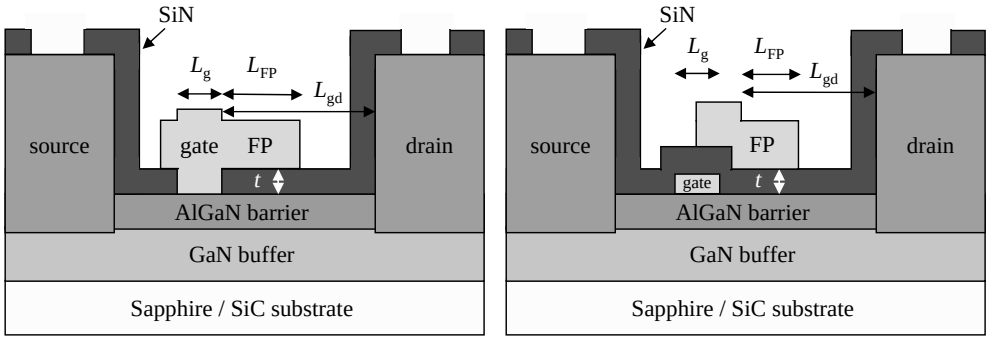

Figure 4.8: Schematic representations of the original (*left*) and modified (*right*) FP implementation.

case of unpassivated devices this positive charge is neutralized mainly by electron trapping. As a result both the 2DEG becomes depleted thereby reducing the drain current swing and the breakdown voltage is decreased. SiN surface passivation prevents neutralization of the positive compensating charge and the FP reduces and reshapes the electric field. Hence, output power is significantly increased because both the current and voltage swings have been increased. For AlGaN/GaN HFETs on sapphire tremendous increase in output power density from 5 - 6 W/mm to 12 W/mm has been reported [30]. For AlGaN/GaN HFETs on s.i. SiC the increase is even more spectacular as the output power density has been increased from 10 - 12 W/mm to over 30 W/mm [174].

Karmalkar *et al.* [75] show that the field distribution for devices without a FP will be confined to a small distance from the gate edge. Hence, a high field is reached even for small values of the drain-source voltage and the breakdown voltage will be low. Incorporation of a FP reduces the peak value of the electric field and the reshaped field distribution along the 2DEG shows two triangular lobes with peaks at the gate and FP edges. Figure 4.9 shows a schematic representation of the electric field distributions in the gate-drain spacing for devices with and without FPs.

Karmalkar *et al.* [75] also show that the critical variables associated with the FP are the following geometrical and material parameters, which have been indicated in Fig. 4.8:

- FP length (L_{FP}),
- thickness of the dielectric film (t),
- gate-drain spacing (L_{gd}),
- 2DEG sheet carrier concentration (n_s), and
- the relative permittivity of the dielectric film ($\varepsilon_{r,diel}$).

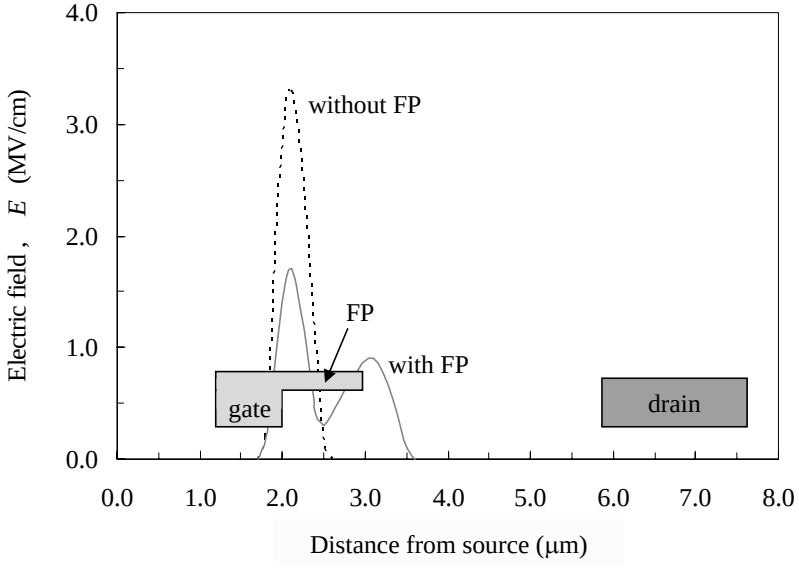

Figure 4.9: Schematic representation of the electric field distributions in the gate-drain spacing for devices with and without FPs [75].

They show that the maximum breakdown voltage will be obtained for an optimum thickness of the dielectric film as for $t = 0$ and $t \rightarrow \infty$ the breakdown voltage will be equal to that of a device without FP. The optimum value for t will increase with $\varepsilon_{r,diel}$ as the FP influences the electric field along the 2DEG channel by capacitive action. However, the optimum thickness will decrease for increasing 2DEG sheet carrier concentration on account of this capacitive action and the fact that a stronger influence by the FP is required to manage a higher n_s. As a result the breakdown voltage will decrease with increasing n_s. Karmalkar *et al.* [75] also show that the breakdown voltage stops increasing with L_{FP} beyond a certain point because the field distribution along the 2DEG consists of two lobes as is shown in Fig. 4.9. As the breakdown voltage equals the total area under these lobes, for a given peak breakdown field, enlarging this area will saturate as the overlap between the lobes decreases with increasing L_{FP}. Finally, the breakdown voltage will stop increasing with L_{gd} beyond a certain point because the field distribution decays beyond the FP edge. Instead, the drain series resistance increases too much thereby degrading the power performance of the device.

4.3.3 Implementation of T- and FP-gates

As maximum microwave output power is our primary goal we have decided to fabricate AlGaN/GaN HFETs with the original FP implementation as shown in Fig. 4.8 -(*left*). The development of the required profile for a one-step EBL process has two very important disadvan-

tages:

- the FP will not be completely parallel to the AlGaN surface as can be seen in Fig. 4.6, and
- complete coverage of the AlGaN layer with SiN up to the footprint of the gate can not be guaranteed.

To solve these problems we have decided to use a two-step EBL process, which offers two additional advantages:

- excellent control over the width of the footprint, the actual gate length, because it can be defined using a very thin (typically 250 nm) high resolution PMMA layer, and
- SiN passivation layer is deposited early on in the fabrication process protecting the AlGaN barrier layer from getting damaged or contaminated.

After defining the footprint, the SiN passivation layer is opened using a RIE sulfurhexafluoride (SF_6) plasma. To prevent the AlGaN barrier layer from excessive plasma damage, which gives rise to high gate leakage currents, an etch process with very low RF power and DC bias of 10 W and -10 V, respectively has been developed. Furthermore, the etch time is accurately determined using dummy samples to avoid excessive overetching. After opening the SiN layer the footprint is evaporated and the wide top of a T- or FP-gate is defined using a thick (typically 900 nm) copolymer layer. Although fabrication is slowed down as it takes two writing steps, the process is much less critical as only a good overlay accuracy between the top and the footprint is required as this determines L_{FP}. Figure 4.10 shows a schematic overview of the two-step EBL process. More detailed information can be found in Appendix A.

Figure 4.11 shows a SEM image of the cross-section of a submicron T-gate fabricated using the two-step process. The footprint of this gate is 0.4 μm and the top is 1.0 μm wide. The image also shows the excellent coverage of the semiconductor surface with SiN up to the footprint of the gate. Furthermore, it can be seen that the top part of the gate is parallel to the semiconductor surface. Figure 4.12 shows photographs using an optical microscope of a T-gate (*left*), and two FP-gates with FP lengths of 0.5 μm (*middle*) and 1.0 μm (*right*), respectively. The footprint of these gates is 0.7 μm and the extension of the top part towards the source contact is 0.25 μm in all cases.

4.4 Surface passivation

Surface passivation is a very important topic in any device technology. As the periodic structure of the crystal lattice abruptly stops at the surface many defect or trap states can be present due to e.g. dangling bonds. Surface passivation is used to terminate these bonds with elements assuring chemical stability of the surface. If there is no suitable native oxide, e.g. SiO_2 in the case of Si, this can be done using hydrogen or a dielectric film such as SiN. In addition, passivation is used to prevent the surface from mechanical and chemical damage during assembly and packaging and environmental influences such as moisture, which is one of the main catalysts for corrosion, and highly mobile impurities like sodium (Na).

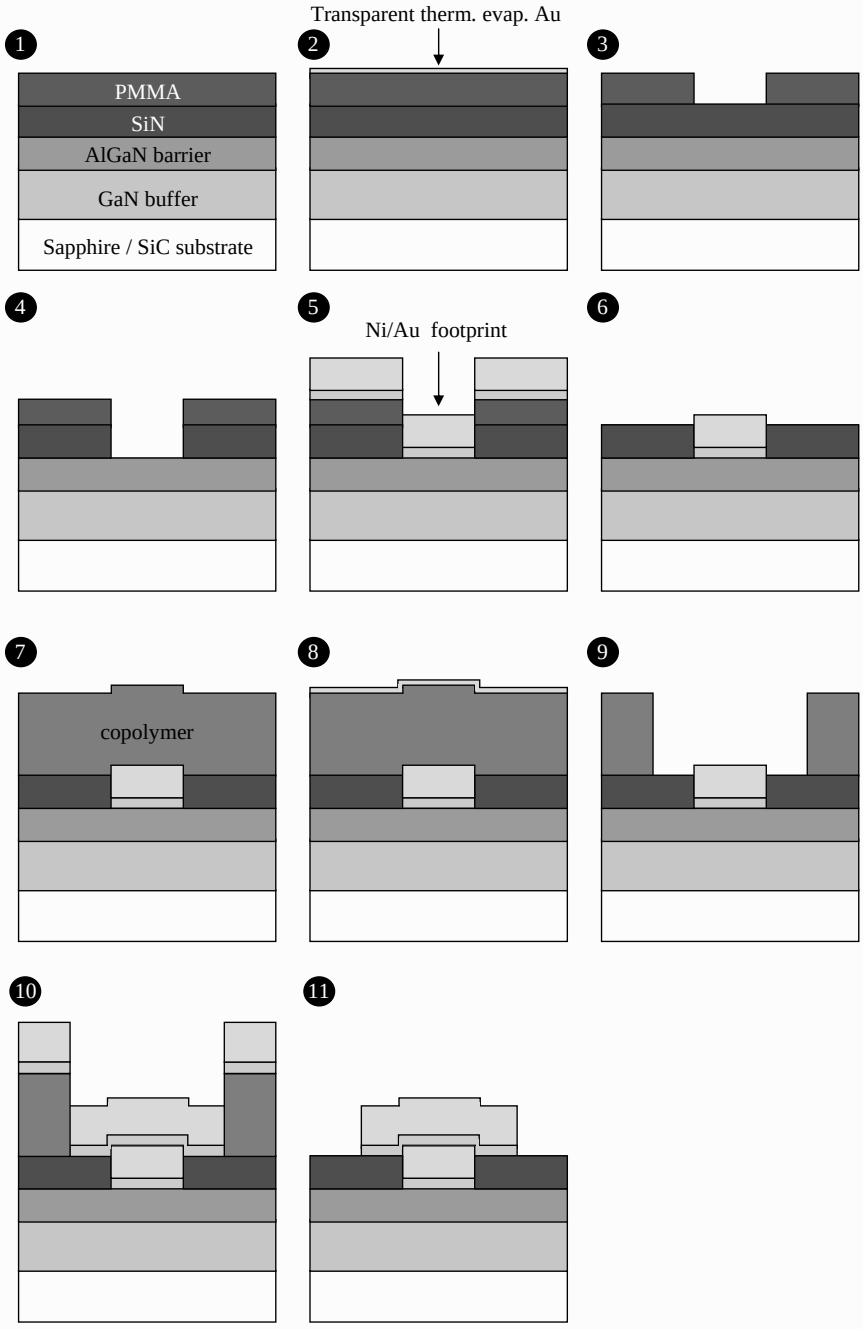

Figure 4.10: Schematic overview of the two-step EBL process.

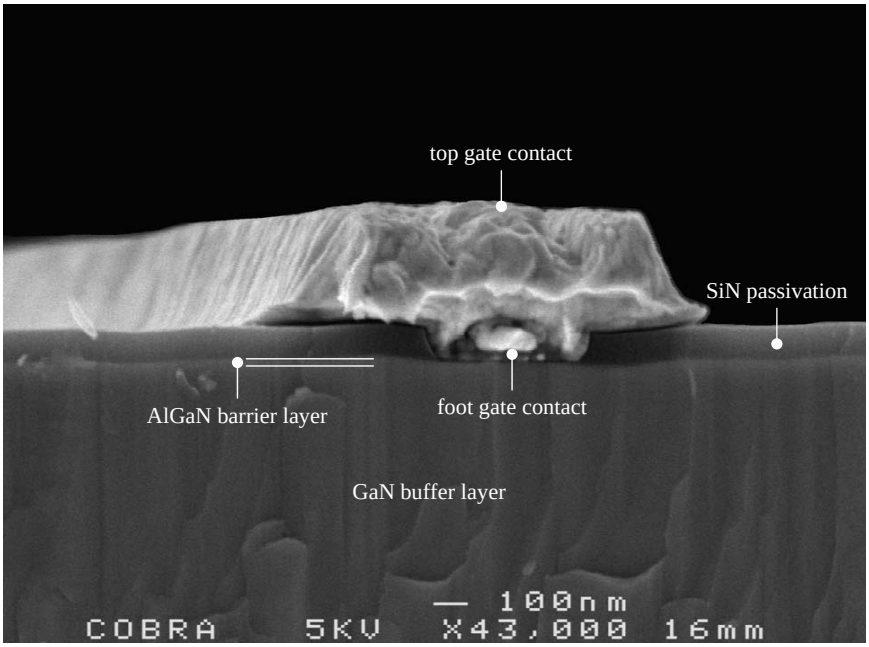

Figure 4.11: Cross-section of a submicron T-gate fabricated using the two step process. The footprint of this gate is 0.4 μm and the top is 1 μm wide.

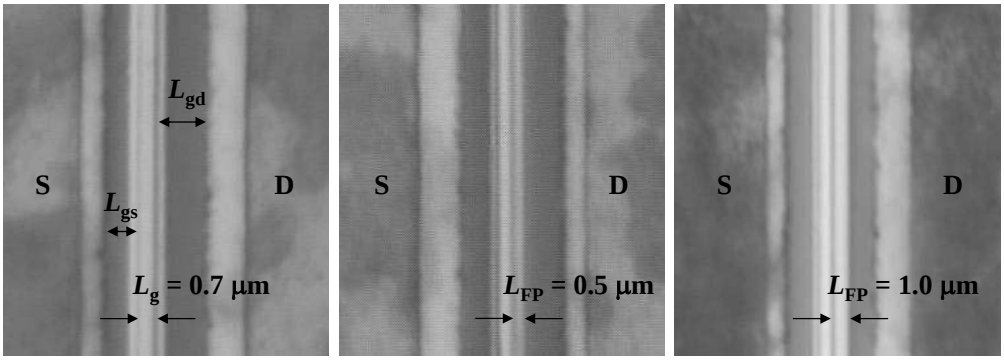

Figure 4.12: Photographs using an optical microscope of a T-gate (*left*), and two FP-gates with FP lengths (L_{FP}) of 0.5 μm (*middle*) and 1.0 μm (*right*).

4.4.1 PECVD SiN

Especially in the case of AlGaN/GaN heterostructures effective surface passivation is required because the AlGaN surface and in particular the amount of positive compensating charge (σ_{comp}) plays a crucial role with respect to device operation and microwave power performance as has been explained in Sect. 2.3.4. In that Section we also mentioned that according to literature [17, 48, 109, 141, 162, 164] effective passivation of the free AlGaN surface, which prevents the formation of a virtual gate and thereby eliminates gate lag, can be achieved by a plasma enhanced chemical vapor deposited (PECVD) SiN film.

We have investigated the efficiency of gate lag reduction and the uniformity of microwave device performance using PECVD SiN on both n.i.d. and doped AlGaN/GaN heterostructures. Undoped HFETs on sapphire have been fabricated on samples, typical size 10 x 10 mm^2, from 2 inch wafers with comparable material characteristics grown by RU, RF Nitro, and QinetiQ. Si-doped HFETs on s.i. SiC have been processed on identical samples from 2 inch wafers grown by the Fraunhofer Institute for Applied Solid-State Physics (IAF). All epitaxial material has been grown using MOCVD. We have investigated "fat gate" and "submicron gate" devices processed using the Inverse Mesa and Submu mask sets respectively, as described in Sect. 3.2.1.

Our experiments confirm that passivation with SiN indeed achieves increased drain current swing because of reduced gate lag but the observed uniformity of the microwave device performance was very poor. This was quite surprising as microwave device performance before passivation showed to be poor but very uniform. The uniformity of the DC *I-V* characteristics before and after passivation remained good.

4.4.2 Surface treatments

To improve uniformity of microwave device performance after SiN deposition, thereby improving process yield, we* have investigated surface treatments before passivation. Although GaN is well known to withstand harsh environmental conditions we have found that gate lag reduction is very sensitive to proper surface preparation before passivation and device processing. The idea to apply surface treatments to the AlGaN barrier layer is based on the hypothesis that contaminants, processing remnants or crystal irregularities residing at the AlGaN-SiN interface prevent effective and reproducible gate lag reduction, which leads to poor uniformity of microwave device performance even on samples as small as 10 x 10 mm^2. We assumed that cleaning and reorganization of the AlGaN surface before SiN passivation would strongly improve reproducible gate lag minimization. We have investigated the influence of a wet etch using buffered hydrofluoric acid (BHF) and a low-power RIE Ar plasma (10 sccm, 40 mTorr, 30 W, 30", DC bias = -86 V, 20 ^oC) in combination with SiN passivation on the amount of gate lag and the uniformity of microwave device performance. The wet etch with BHF (1'30") was performed at the start of device processing whereas the Ar plasma was applied just before the RTA step (800 ^oC, 2 minutes, N_2 ambient) of the Ti/Al/Ni/Au ohmic contacts. The RTA step is

*This work was a joint effort between this author and B. Jacobs, at that time Ph.D. student at the same institute [67].

done at 800 °C to avoid degradation of the crystallinity of the AlGaN material [183]. Annealing for 2 minutes yields good ohmic contacts (R_c = 0.15 Ωmm) and enables reorganization of the AlGaN surface.

To make a good comparison between the four possible surface treatments and to exclude sample to sample spread, we have combined them all on the same 10 x 10 mm^2 sample. For these experiments we have used the Inverse Mesa mask set, which consists of four identical transistor modules consisting of 91 fat gate HFETs each. Module 1 has not been exposed to any surface treatment before passivation with a 100 nm PECVD SiN film (300 °C, refractive index between 1.97 - 2.01 at 2 eV) and served as a reference. Module 2 has only been etched in BHF. Module 3 has only been exposed to the Ar plasma, and module 4 has received both treatments before SiN passivation. The modules that have not been exposed to the Ar plasma have been covered by a piece of sapphire during the plasma treatment. Masking with a piece of sapphire has been used instead of masking with photoresist to prevent the AlGaN surface from being contaminated with resist residues after resist removal. Figure 4.13 shows a schematic representation of this experimental approach.

4.4.3 Pulsed DC current-voltage measurements

To examine the amount of gate lag in our devices, we have built a measurement setup to perform on-wafer pulsed DC (*I*-*V*) measurements. This setup consists of a HP214B voltage pulse generator, DC bias sources and a HP54120A digital sampling oscilloscope. Figure 4.14 shows the equivalent circuit of the pulsed DC (*I*-*V*) setup used for analyzing gate lag in AlGaN/GaN HFETs. At the gate side, the voltage pulse generator is used to switch the device from off-state to on-state by applying voltage pulses (V_p) to the gate. The negative DC voltage needed to bias the device in the off-state is provided by $V_{DC,gate}$. A bias tee, consisting of $C_{bias\ tee}$ and $L_{bias\ tee}$, has to be used to provide the DC bias and voltage pulses to the gate electrode. At the drain side, a capacitor (C_{buf}) is required to supply the current during switching of the device while maintaining a nearly constant drain-source bias voltage. The DC voltage needed to drive the device is provided by $V_{DC,drain}$. The drain current is determined by measuring the voltage drop over the resistor (R_{meas}) using the digital sampling oscilloscope.

Pulsed measurements start by biasing the device in the saturation region ($V_{DC,drain} > V_{knee}$ = 7 V) and just into pinch-off ($V_{DC,gate} < V_{pinch\text{-}off}$ = -5.5 V). The values used for $V_{DC,drain}$ and $V_{DC,gate}$ were 10 V and -6 V, respectively. Voltage pulses with a width of 100 ns (9 ns rise time, 0.2 % duty cycle) were used to drive the device from pinch-off (-6 V) to open channel (0 V) and back. In response to this, the drain current should show transitions from channel leakage current, to open channel current, and back to channel leakage current. The value of the pulsed drain current ($I_{D,p}$) has been determined 15 ns after the leading edge of the voltage pulse. Figure 4.15 shows typical pulse shapes of the drain current in response to a gate pulse for SiN passivated undoped fat gate devices on sapphire that severely suffer from gate lag (*left*), and for devices, on the same sample, for which gate lag has effectively been eliminated (*right*).

We have defined the amount of gate lag elimination (GL_{elim}) as

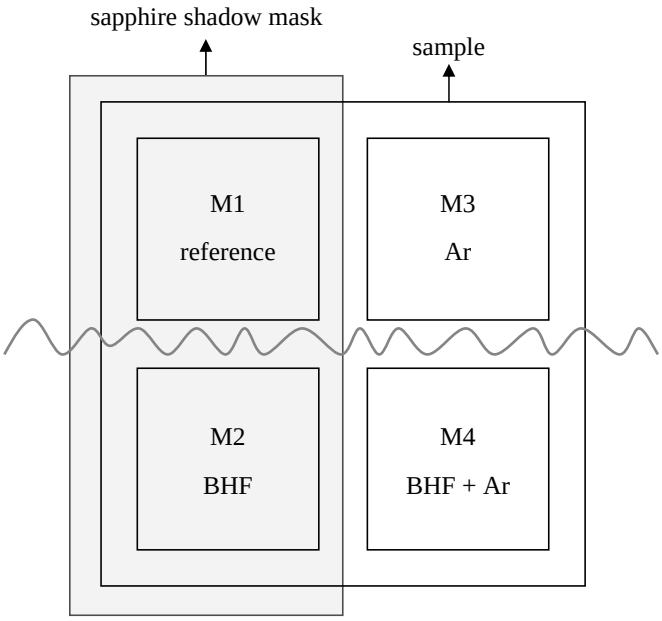

Figure 4.13: Module 1 has not been exposed to any surface treatment before SiN passivation and serves as a reference. Module 2 has only been etched in BHF. Module 3 has only been exposed to the Ar plasma, and module 4 has received both treatments before SiN passivation.

$$GL_{\text{elim}} = \frac{I_{\text{D,p}}}{I_{\text{D,CW}}}, \tag{4.8}$$

where $I_{\text{D,p}}$ is the pulsed DC drain current and $I_{\text{D,CW}}$ is the continuous wave (CW) DC drain current at V_{gs} = 0 V. Figure 4.16 shows typical results of pulsed and CW drain current measurements from the four differently treated modules before and after passivation with 100 nm SiN. It has to be noted that these results apply to both fat gate and submicron gate devices regardless of the substrate used and the material source.

The clear bars represent average values of $I_{\text{D,CW}}$ (white) and $I_{\text{D,p}}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values. In each module 15 devices have been measured. The relatively moderate values of $I_{\text{D,CW}}$ are mainly caused by the dimensions of the fat gate devices, which give rise to considerable parasitic source and drain resistances.

Figure 4.16 clearly shows that the devices from all modules show a very large amount of

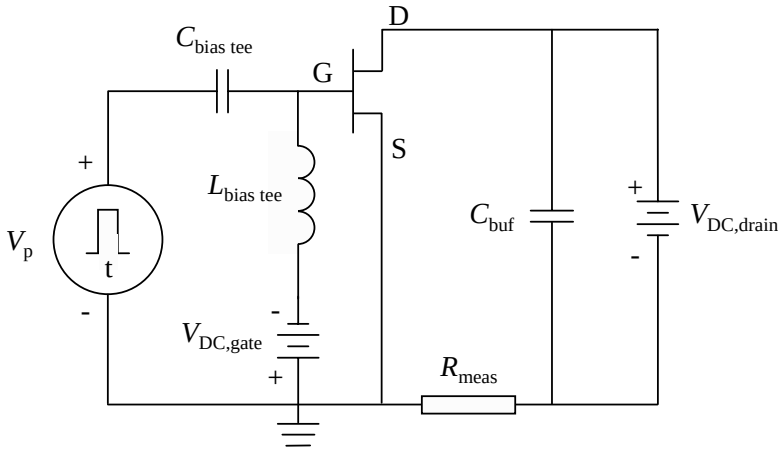

Figure 4.14: Equivalent circuit of the pulsed DC (*I-V*) measurement setup for analyzing gate lag.

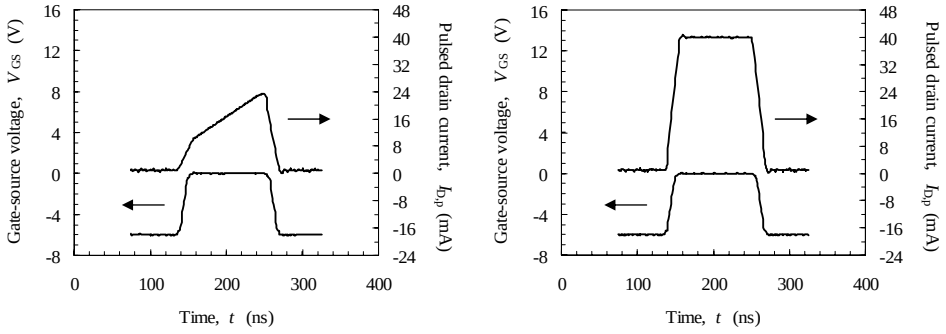

Figure 4.15: Typical pulse shapes of the drain current in response to a gate pulse for SiN passivated undoped fat gate devices on sapphire that severely suffer from gate lag (*left*), and for devices, on the same sample, for which gate lag has effectively been eliminated (*right*).

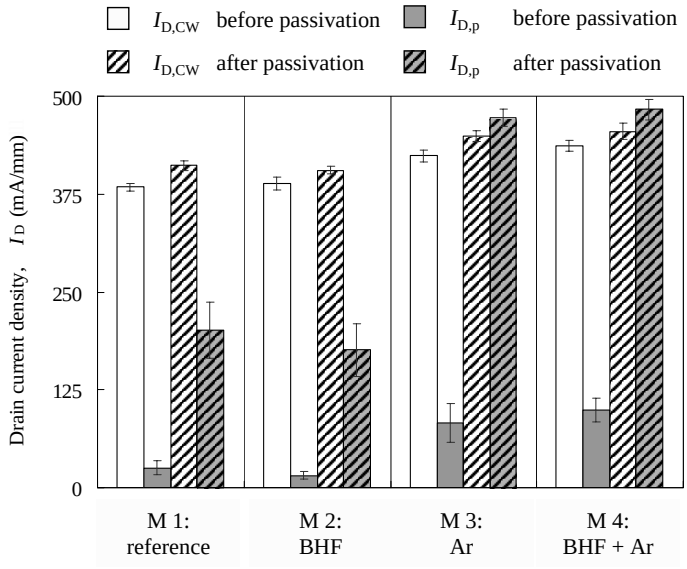

Figure 4.16: Typical results of pulsed and CW drain current measurements from the four differently treated modules before and after passivation with the standard SiN film (100 nm, 300 ^{o}C, refractive index between 1.97 - 2.01 at 2 eV). It has to be noted that these results apply to both fat gate and submicron gate devices regardless of the substrate used and the material source. The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

gate lag before passivation. This is especially true for the modules that have not been exposed to the Ar plasma (modules 1 and 2, respectively). After SiN passivation, the amount of gate lag in devices from modules 1 and 2 has been decreased significantly but it still is unacceptably large. This is in sharp contrast with devices from the modules that have been exposed to the Ar plasma (modules 3 and 4, respectively) as in that case gate lag has completely disappeared. It should be noted that the strong reduction of self-heating under pulsed measurement conditions causes $I_{D,p}$ to be higher than the corresponding $I_{D,CW}$. Looking at the error bars it should also be noted that the Ar plasma treatment has significantly improved the uniformity of the pulsed *I-V* results after passivation. The observed increase in the values for $I_{D,CW}$ and $I_{D,p}$ after passivation is in accordance with literature [48, 71]. Although the best results after passivation are achieved using the combination of the BHF wet etch and the Ar RIE etch (module 4), it has to be concluded that the Ar plasma treatment is the key processing step leading to the strongly minimized gat lag and the significantly improved uniformity of the measurement results.

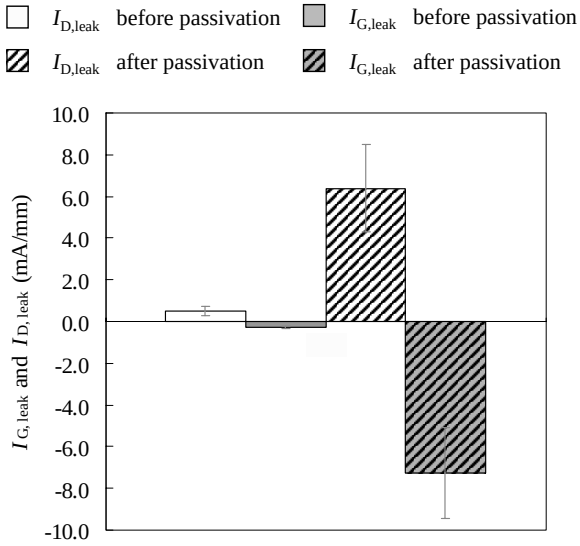

Figure 4.17: Typical gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$) of undoped fat gate devices on sapphire substrates before and after passivation using the standard SiN film (100 nm, 300 ^{o}C, refractive index between 1.97 - 2.01 at 2 eV), respectively.

A serious drawback of our standard PECVD SiN film (100 nm, 300 ^{o}C, refractive index between 1.97 - 2.01 at 2 eV) is the strongly increased gate leakage current ($I_{G,leak}$) after passivation of the AlGaN surface. Figure 4.17 shows typical gate and drain leakage current densities of undoped fat gate devices on sapphire substrates before and after passivation, respectively. Although the increased drain leakage current density after SiN deposition is undesired, it does not have a very big influence on the drain current swing. However, the increased gate leakage current density significantly reduces the maximum breakdown voltage and hence the drain-source voltage swing. It is obvious that this is detrimental for high-power device operation. In chapter 5 we will investigate the influence of several process settings, i.e. gas flow, RF power, total gas pressure, and substrate temperature, on the material properties of PECVD SiN films and their influence on the surface passivation of AlGaN/GaN HFETs on sapphire and s.i. SiC substrates. The main goals of these investigations have been to minimize gate and drain leakage currents while maintaining the passivation properties of the standard SiN film.

4.5 Air bridges

Air bridges, which in fact are lifted metal lines, are required to connect the multiple drain or source contacts in multi-finger devices as can be seen in Fig. 3.17. In the case of a comb layout

the internal sources are connected through air bridges whereas for a fishbone layout this is the case for the drain contacts.

4.5.1 Electroplating

A typical air bridge is defined using a double-layer photoresist pattern and Au electroplating. The first photoresist layer is used to define the posts of the air bridges and to support them. This resist layer should be thick, typically thicker than 3 μm, to ensure that the bridges are high enough and to reduce parasitic capacitances. After definition of the posts a seed layer, typically Ti/Au, is deposited, which serves as cathode electrode in the Au electroplating process. This seed layer should be continuous over the complete sample surface otherwise no plating will occur due to a break in the cathode electrode. Therefore, the side walls of the thick support resist should not be too steep. This can be achieved by a two-step backing step, in which the resist is hardened first and then rounded by controlled flowing of the resist. After the deposition of the seed layer the second resist layer is used to define the areas where the air bridges will be realized. In the next step the actual air bridges are fabricated by electroplating of a thick Au layer. After the plating process, the top resist layer is removed first. Then first the Au part of the seed layer is removed by wet etching using a potassium cyanide (KCN) based solution (DEGUSSA) followed by an etch with oxalic acid (mixture of $C_2H_2O_4.2H_2O$, H_2O_2, and KOH) to remove the Ti part of the seed layer. Finally, the thick support resist is removed.

Electroplating of thick Au layers on small samples, typically 10 mm x 10 mm, is very troublesome as a clamp has to be used to attach them to a sample holder. Such construction severely affects the flow in the Au bath which results in strongly non-uniform plating results with respect to the thickness of the plated metal across the sample. In addition, huge topography on the small samples also significantly deteriorates the uniformity of the thickness of the plated Au layer.

4.5.2 Electron beam evaporation

To circumvent these problems we have chosen to use e-beam evaporation to fabricate air bridges with a 1.5 μm thick Au layer. As a consequence, we had to use a resist with a lift-off profile, i.e. negatively sloped side walls, to define the areas where the air bridges will be realized. For this purpose we have used ma-N440, which is a 4 μm thick negative resist with an excellent lift-off profile. To prevent the support resist from being attacked during development of the top resist we have evaporated a 12.5 nm transparent Au layer on top of the support resist before starting the bridge litho process. This Au layer has to be transparent to allow alignment of the bridge litho to the litho of the posts. After the bridge litho we have evaporated Ti/Au = 20/1500 nm. The Au layer has been evaporated in three consecutive runs of 500 nm each to avoid excessive heating of the sample, which can cause flowing and hardening of the resist during the metallization process that is long as the evaporation rate is as low as 0.6 nm/s to avoid sputtering of Au. After lift-off of the bridge metallization, the transparent Au layer is removed using the DEGUSSA solution, and finally the support resist is removed.

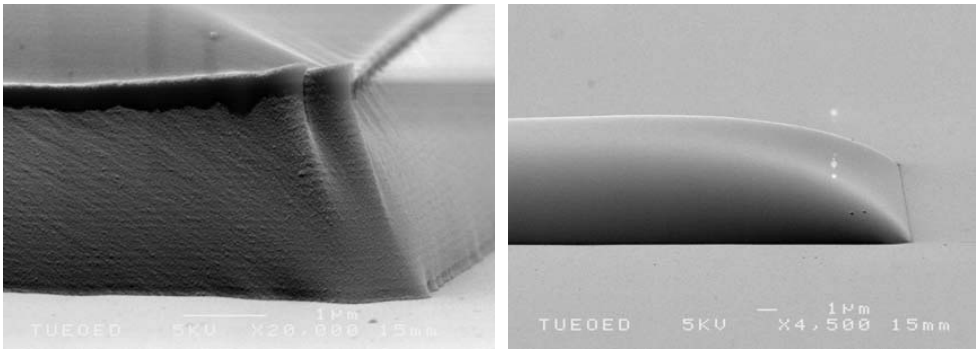

Figure 4.18: Steep (*left*) and strongly rounded or lens-shaped AZ4533 profiles (*right*).

The reliability of air bridges depends on the metal thickness used, the size of the posts, the height of the bridge, and its width-to-length ratio. These aspects should be well considered to prevent the bridge from sagging. Foundries use a width-to-length ratio of 1 : 4. In our mmTor design the maximum distance the air bridges have to span is about 100 μm. As the minimum width of the air bridges is 62.5 μm, implying a span width of 250μm, this design criterion has perfectly been obeyed. However, we have encountered problems with respect to breaking of bridges during removal of the thick support resist, in our case 3.3 μm thick AZ4533 (positive tone). We found out that this problem was caused by the side walls of the AZ4533 profile that were too steep and had a notch at the top edge causing a weak spot in the connection between the bridge and the posts. We have solved this problem by significantly improving the rounding of the AZ4533 profile by increasing the temperature of the second bake step from105 ^{o}C to 160 ^{o}C. Figure 4.18 shows SEM images of the steep (*left*) and strongly rounded or lens-shaped AZ4533 profiles (*right*).

Furthermore, we have introduced slits that split up wide air bridges into several narrower parts in parallel because it is difficult to efficiently remove the thick support resist underneath very wide air bridges without destroying them. Figure 4.19-(*left*) shows a photograph of an AlGaN/GaN HFET with a total gate width (W_{g}) of 1 mm in which the drain contacts have been connected using air bridges including the aforementioned slits. Figure 4.19-(*right*) is a close up showing two source-drain regions through the split in an air bridge connecting two drain contacts.

4.6 Conclusions

In this chapter we have described key steps of the process technology that we have developed to fabricate microwave high-power AlGaN/GaN HFETs on sapphire and s.i. SiC substrates. The following conclusions can be drawn:

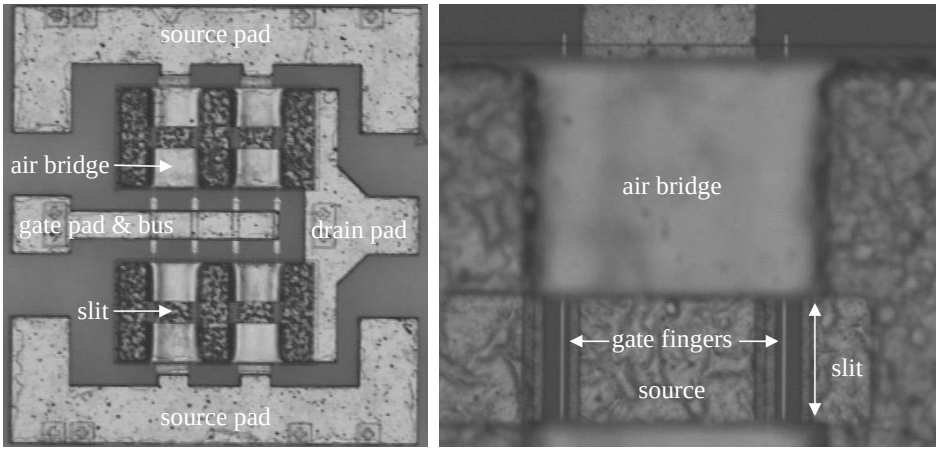

Figure 4.19: Photograph of an AlGaN/GaN HFET with a total gate width (W_g) of 1 mm in which the drain contacts have been connected using air bridges including slits (*left*) and close up showing two source-drain regions through the split in an air bridge connecting two drain contacts (*right*).

- The line definition and surface morphology of the Ti/Al/Ni/Au (30/180/40/100 nm) ohmic contacts has significantly been improved using an Au/Al ratio of 0.55, and a ramp-up time of the RTA process of 45 seconds. The contact resistance on n.i.d. AlGaN (25 nm) / GaN (2 μm) heterostructures using this metallization scheme is as low as 0.15 Ωmm.

- We have pointed out that our choice to investigate Ni/Au Schottky contacts on strained AlGaN/GaN heterostructures instead of relaxed bulk AlGaN layers proves to be the approach to follow despite difficulties with respect to characterization. Our studies towards the optimization of these contacts have focused on the development of a suitable pre-metallization surface clean to achieve lowest reverse current and highest breakdown voltage. The most suitable surface clean for high-power applications consisting of a wet etch using NH_4OH for 15 minutes cannot be used in the process flow of the large periphery HFETs (mmTor) as it causes severe adhesion problems with the copolymer that is used to define the footprint of the Schottky gates. However, as the AlGaN surface is cleaned using an ammonia dip for 1 minute before passivation with silicon nitride, the surface clean just before Ni/Au evaporation has been omitted. Reverse (I-V) measurements of Schottky test structures showed leakage currents of 400 μA/mm and breakdown voltages around 150 V. These results indicate that our Ni/Au Schottky contacts are perfectly suitable for application in high-power HFETs.

- For device isolation using a dry etch, we have shown the development of a low power

ICP process using a Cl_2/H_2 chemistry that enables the use of photoresist as masking material to obtain mesa structures with sloped side walls. This process etches AlGaN/GaN unselectively at a rate of 110 nm/min and yields a very smooth surface morphology of the etched GaN buffer layer. Furthermore, we have discussed the importance of creating a process window for the etch process to assure a constant etch rate and reproducible etch results from run to run.

- A two-step EBL process has been developed to fabricate T-shaped and FP-gates with sub-micrometer footprints, which define the actual gate length. The top parts of these gates are parallel to the semiconductor surface, which is completely covered with SiN up to the footprint of the gate. Additional advantages of this process are the excellent line width control of the footprint and the protection of the AlGaN layer due to the deposition of the SiN passivation layer early in the fabrication process.

- We have investigated the efficiency of gate lag reduction and the uniformity of microwave device performance using PECVD SiN on both n.i.d. and doped AlGaN/GaN heterostructures. Our experiments confirm that passivation with SiN indeed achieves increased drain current swing because of reduced gate lag but the observed uniformity of the microwave device performance showed to be very poor. We have shown that the application of a low power dry etch using Ar (10 sccm, 40 mTorr, 30 W, 30", DC bias = -86 V, 20 ^{o}C) just before the RTA step (800 ^{o}C, 2 minutes, N_2 ambient) of the Ti/Al/Ni/Au ohmic contacts is the key processing step leading to strongly minimized gat lag and the significantly improved uniformity of microwave device performance upon surface passivation with SiN. The observed increase in gate and drain leakage currents after SiN deposition will be investigated into more detail in Chapter 5.

- We have developed a process that uses e-beam evaporation to fabricate air bridges with a 1.5 μm thick Au layer. To improve the stability and reliability of the air bridges a lens-shaped support resist has been used to avoid the posts of the bridges to be too steep which causes easy breaking. Furthermore, we have introduced slits that split up wide air bridges into several narrower parts in parallel because it is difficult to efficiently remove the thick support resist underneath very wide air bridges without destroying them.

Chapter 5

PECVD silicon nitride passivation films

Insulating amorphous silicon nitride (SiN) films are widely used both as an element of microelectronic solid-state device structures, and in device process technology. A few examples of the former are the use of SiN as a gate dielectric of nonvolatile memories, it is one of the dielectric materials in the stacked oxide-nitride-oxide layers in DRAM capacitors, and it is used as sidewall spacers in MOSFETs. In process technology it is for example used as masking material, as stop-layer for chemical mechanical polishing and etching processes, and as surface passivation layer.

In 1964 researchers at IBM started working on amorphous SiN films to develop an improved substitute or supplement for silicon dioxide (SiO_2) as a passivation layer of Si surfaces. They discovered that SiN is extremely impervious to e.g. moisture, oxygen, and ions of different metals, first of all sodium (Na), which is a very important requirement for the use as passivation layer [61]. Additional properties making SiN suitable for surface passivation are the facts that it can be synthesized by plasma enhanced chemical vapor deposition (PECVD) to have low compressive stress, which allows it to be exposed to severe environmental stress with less likelihood of delamination or cracking. Furthermore, its coverage of underlying metal is conformal, and finally it can be deposited with an acceptably low pinhole density [171].

In this chapter we will investigate the influence of several process settings, i.e. gas flow, RF power, total gas pressure, and substrate temperature, on the material properties of PECVD amorphous SiN films and their influence on both leakage currents and surface passivation of AlGaN/GaN HFETs on sapphire and s.i. SiC substrates.

5.1 Introduction

In Sect. 4.4 it has clearly been shown that the AlGaN barrier of HFETs on sapphire and s.i. SiC substrates can effectively be passivated using the combination of a BHF wet etch, an Ar RIE etch, and a PECVD SiN film (100 nm, 300 ^{o}C, refractive index between 1.97 - 2.01 at 2 eV). However, after passivation with this standard SiN film a significant increase in the gate and drain leakage currents has been observed. Although the increased drain leakage current density after SiN deposition is undesired, it does not severely reduce the drain current swing. However, the increased gate leakage current density significantly reduces the maximum breakdown voltage and hence the drain-source voltage swing, which obviously is detrimental for high-power device operation.

We assumed that the cause for the increased gate leakage current was related to the SiN-AlGaN interface. This assumption is supported by Ansell *et al*. [10] and Tan *et al.* [154] who have shown that hopping conduction, which they suggest to be the dominant gate leakage mechanism in the case that the device is pinched-off and drain-source voltages above the knee voltage are applied, increased after SiN passivation as the average activation energy decreased from 200 meV to 50 - 70 meV. We have investigated if changing the composition of the PECVD SiN film or preparation of the AlGaN barrier layer before SiN deposition, or both, results in decreased leakage currents after SiN deposition. It should be noted that the surface passivation capability should remain equal to that of the standard film.

The composition of SiN films can be changed by altering the settings of the PECVD process, e.g. gas flow, RF power (P_{RF}), total gas pressure (p), and substrate temperature ($T_{\mathrm{substrate}}$). To investigate the material properties and compositions of differently synthesized SiN films using spectral ellipsometry (SE), Fourier transform infrared spectroscopy (FTIR), effective minority carrier lifetime measurements, and stress measurements, the films have been deposited on monocrystalline Si wafers. Characterization and analysis of the results obtained by SE, FTIR, and effective minority carrier lifetime measurements have been performed by Bram Hoex and Erwin Kessels, researchers with the group Equilibrium and Transport in Plasmas (ETP) from the faculty of Applied Physics at TU/e. Stress measurements have been performed by Eugene Timmering and Johan Klootwijk from Philips Research Laboratories Eindhoven.

Preparation of the AlGaN barrier layer before SiN deposition can be done by a combination of organic cleaning, using acetone and iso-propyl alcohol (IPA), and wet etching either using dilute hydrofluoric acid (HF), buffered HF (BHF), or dilute ammonia (NH_4OH) [48, 109]. Regarding the mmTor process flow we have chosen to use NH_4OH to avoid degradation of the Ti/Al/Ni/Au ohmic contacts as Ti is attacked by HF and BHF.

CW and pulsed DC *I*-*V* measurements have been performed to determine the influence of the film properties of different PECVD SiN films as well as the preparation of the AlGaN barrier layer before SiN deposition on the surface passivation and the amount of gate and drain leakage currents of n.i.d. AlGaN/GaN HFETs on sapphire substrates.

5.2 Deposition of silicon nitride by PECVD

When used as a passivation layer, the deposition process of amorphous SiN is preferably done at relatively low substrate temperatures, typically 200 °C - 400 °C, for example to be compatible with metals that have low melting points like aluminum (660 °C at atmospheric pressure) or to prevent outgassing of volatile elements like phosphorus (P). In those cases, PECVD is the method of choice as it enables deposition of SiN films in the aforementioned low-temperature range because the major part of the energy required to initiate and sustain the chemical reaction is supplied by an RF plasma. Hence, the high temperature that is generated within the gaseous molecules facilitates their reaction and results in deposition at relatively low substrate temperatures.

Already in 1965, Sterling and Swann described SiN deposition by PECVD [153]. However, in 1990 Smith *et al.* [151] provided a thorough explanation of this technique for the first time. Stoichiometric amorphous SiN films have a nitrogen to silicon ratio (x) of 1.33 [15] and a refractive index (n) of 1.95 at 2eV [80]. However, PECVD SiN films tend to be non-stoichiometric and commonly contain substantial quantities of atomic hydrogen, typically 10 at% - 30 at% [171]. For this reason the chemical representation sometimes used for these films is a-SiN_x:H. In this thesis we will just use the representation SiN.

The two main reactions for synthesizing SiN films from the gas phase are the interactions of silane (SiH_4) and silicon tetrachloride ($SiCl_4$) with ammonia (NH_3) as is given by reaction equations 5.1 and 5.2, respectively. An alternative for using pure silane is the use of dilute silane, i.e. diluted in an inert gas such as argon (Ar) or nitrogen (N_2), which does not spontaneously combust when exposed to air.

$$3SiH_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12H_2(g) \tag{5.1}$$

$$3SiCl_4(g) + 4NH_3(g) \rightarrow Si_3N_4(s) + 12HCl(g) \tag{5.2}$$

5.2.1 Equipment

The deposition of our SiN films has been done in a load-locked Oxford Plasmalab 100 system using ammonia (NH_3), pure silane (SiH_4) and nitrogen (N_2) as process gases. The samples are placed on a 4 inch Si carrier wafer, which is transferred by a robot arm into the parallel plate deposition chamber and placed on a grounded and heated lower electrode with a diameter of 205 mm. The process gases are mixed and injected into the deposition chamber at the desired flow rates through a showerhead-type upper electrode. Gas is continuously pumped out of the chamber, underneath the lower electrode, to maintain a constant total gas pressure (p) during the deposition. An RF field with a frequency of 13.56 MHz is applied between the upper and lower electrodes to initiate and sustain a plasma that contains the ionized gas species from which the SiN film is synthesized. A high excitation frequency is used to minimize plasma damage of the sample surface during the deposition process [80].

5.2.2 Characterization techniques

To investigate the material properties and composition of the SiN films we have chosen to deposit them on monocrystalline Si wafers as this enables the use of the following standard characterization techniques:

- spectroscopic ellipsometry (SE),
- Fourier transform infrared spectroscopy (FTIR), and
- effective minority carrier lifetime measurements.

SE measurements have been performed on SiN films deposited on 2 inch monocrystalline Si wafers using a Woolam M2000 system in the energy range from 0.7 eV - 5 eV. Using the Tauc-Lorentz formalism, the SE measurement results are used to extract the following material properties of the films: thickness (d_{SiN}), surface roughness (d_{s}), refractive index (n), and extinction coefficient (k) [69]. From the extinction coefficient, the absorption coefficient (α) can be calculated using $\alpha = 4\pi k/\lambda$. In addition, the photon energy at which the absorption coefficient equals 10^4 cm^{-1} is often referred to as the optical band gap (E_{04}).

FTIR measurements using a Bruker Vector 22 system have been performed on relatively thick SiN films, typically > 300 nm, which are also deposited on 2 inch monocrystalline Si wafers. In these measurements, which are performed at normal incidence to the substrate, transmittance spectra of the bare Si substrate and of the same Si substrate covered with a SiN film are recorded on the same spot. This differential measurement approach enables the extraction of the absorbance of the SiN film. FTIR measurements provide information about the configuration and amount of bonded hydrogen in SiN films. Therefore, they can be used to determine the regime in which the SiN films have been deposited. The so-called simple radical deposition regime, i.e. plasma deposition from SiH_3 and NH_2 radicals, yields SiN films containing Si-H and N-H bonds. In the case of aminosilane SiN deposition, gas phase reactions cause all SiH_4 to be incorporated into $Si(NH_2)_3$ molecules and radicals before SiN deposition. These films can contain N-H and N-H_2 bonds but no Si-H bonds [124]. In addition it should be noted that films which only contain N-H bonds are dense and highly stable, whereas films containing N-H_2 bonds are highly unstable because they get oxidized due to the reaction with water vapor from the air [123].

To measure the effective minority carrier lifetime (τ_{eff}) SiN films have been deposited on 3 inch double polished float zone (FZ) monocrystalline Si wafers. The resistivity of the p-type and n-type substrates used was 8.4 Ωcm and 1.3 Ωcm, respectively. Before SiN deposition the Si wafers have been cleaned using the standard RCA clean [79] followed by an HF dip. The effective minority carrier lifetime is a measure for the surface passivation capability of the deposited SiN film. The higher the effective lifetime, the better the Si surface has been passivated. We have determined the effective minority carrier lifetime using a Sinton lifetime tester. This system, first introduced by Sinton *et al.* [150], is a contactless implementation of the steady-state photoconductance technique in which the photoconductance of a Si substrate is measured in a quasi-steady-state mode during a long, slowly varying light pulse. Contrary to conventional techniques, which are based on the analysis of photoconductance decay transients

Table 5.1: Process settings for our standard SiN deposition process using an Oxford Plasmalab 100 PECVD system.

N_2 (sccm)	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	p (mTorr)	$T_{substrate}$ (^oC)
980	16.6	13.4	20	650	300

to determine the effective minority carrier lifetime, the quasi-steady-state approach allows the use of simple electronics and light sources. Despite its simplicity it is capable of determining very low effective lifetimes. Even when measuring lifetimes below 1 μs the data acquired is from a ms-range slowly varying wave form, eliminating the requirement for fast electronics. The quasi-steady-state technique operates at frequencies between 8 MHz - 10 MHz and uses a coil in a bridge circuit to couple to the wafer conductivity. A signal proportional to this conductivity is observed on a digital oscilloscope and transferred to a computer for analysis. The range of measurable lifetimes is only limited by signal strength, e.g. if the light intensity is increased to 100 W/cm^2 the detection limit becomes as low as 3 ns [150].

5.3 Influence of PECVD process settings on SiN film properties

The starting point of these investigations has been to determine the material properties of the standard PECVD SiN film used for surface passivation of the AlGaN barrier layer. The process settings for our standard SiN deposition process are listed in Table 5.1.

Table 5.2 shows the values for the material properties, i.e. thickness (d_{SiN}), surface roughness (d_s), refractive index (n) at 2 eV, and extinction coefficient (k) at 3.44 eV, which have been determined from the SE measurement data using the Tauc-Lorentz formalism, of a SiN film with a target thickness of 200 nm that has been deposited using the standard deposition process. In addition, the values for E_{04} of this film, the deposition rate (R_{dep}) of the standard process, and the Tauc-Lorentz parameters (A, E_0, Γ, and E_g) are given.

Table 5.2 shows that the refractive index at 2 eV of the standard film is higher than that of stoichiometric amorphous SiN films, which is 1.95 at 2 eV [80]. This implication of the fact that the standard SiN film is Si-rich is confirmed by the non-zero value of the extinction coefficient at 3.44 eV, which is a measure for the amount of Si-Si bonds present in SiN films. The value of 2.85 eV for the optical bandgap, which is associated with the isolating properties of SiN films, is rather low as for good isolating behavior its value should preferably be larger than 5 eV.

Having determined the material properties of the standard film we started investigating their dependence on gas flow, RF power, substrate temperature, and total gas pressure, as will be described in Sects. 5.3.1 - 5.3.4.

Table 5.2: Material properties of the standard SiN film determined from SE measurement data using the Tauc-Lorentz formalism. In addition, the values for the optical band gap (E_{04}) and the deposition rate (R_{dep}) are given.

d_{SiN} (nm)	d_s (nm)	n (2 eV)	k (3.44 eV)	E_{04} (eV)	R_{dep} (nm/min)	A (eV)	E_0 (eV)	Γ (eV)	E_g (eV)
204	1.5	2.01	0.030	2.85	12.7	79.25	9.07	7.32	2.76

Table 5.3: Gas flows and Tauc-Lorentz parameters for the SiN films deposited in the SiH_4 flow series.

Sample	SiH_4 (sccm)	N_2 (sccm)	NH_3 (sccm)	t (min)	A (eV)	E_0 (eV)	Γ (eV)	E_g (eV)
A	4	980	13.4	18	107.87	9.98	4.94	4.72
B	7	980	13.4	16	102.96	9.91	5.03	4.47
C	10	980	13.4	20	78.29	9.81	3.89	3.73
D	11	980	13.4	16	77.29	9.64	4.12	3.54
E	13	980	13.4	18	73.75	9.56	5.04	3.15
F	15	980	13.4	8.5	71.15	8.68	5.38	2.83
G	16.6	980	13.4	16	79.25	9.07	7.32	2.76
H	20	980	13.4	7	90.94	8.27	9.43	2.59

5.3.1 Gas flow

First we have determined which ranges of values for the refractive index and optical bandgap could be achieved by changing the gas flow. Based on the process settings for the standard deposition process, which have been given in Table 5.1, the SiH_4 flow has been varied from 4 sccm - 20 sccm while keeping the NH_3 and N_2 flows constant at 13.4 sccm and 980 sccm, respectively. All films have a target thickness of 200 nm. Table 5.3 gives an overview of the variations in the SiH_4 flow and the Tauc-Lorentz parameters following from SE analysis. It has to be noted that these values for the Tauc-Lorentz parameters are in good agreement with values obtained by Jellison *et al.* [70].

Table 5.4 gives an overview of the material properties and the values for E_{04} of the SiN films from the SiH_4 flow series. In addition, the values for the deposition rate (R_{dep}) of the different processes are given. Figure 5.1-(*left*) shows that the refractive index of the SiN film, as expected, increases with the SiH_4 flow and that the optical bandgap decreases with the SiH_4 flow. Figure 5.1-(*right*) shows that the extinction coefficient becomes unequal to zero for SiH_4

Table 5.4: Material properties and optical bandgaps (E_{04}) of the 200 nm thick SiN films from the SiH_4 flow series that have been determined from SE measurement data using the Tauc-Lorentz formalism. In addition, the values for the deposition rate (R_{dep}) of the different processes are given.

Sample	SiH_4 (sccm)	n (2 eV)	k (3.44 eV)	E_{04} (eV)	R_{dep} (nm/min)
A	4	1.82	0	4.38	11.1
B	7	1.84	0	3.63	12.5
C	10	1.88	0	4.15	12.9
D	11	1.91	0	3.64	12.9
E	13	1.94	0.003	3.27	12.8
F	15	1.97	0.020	2.93	11.5
G	16.6	2.01	0.030	2.85	12.7
H	20	2.07	0.078	2.68	11.5

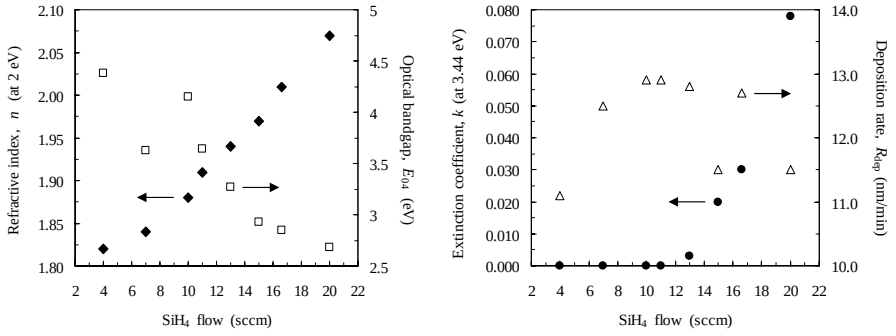

Figure 5.1: Refractive index (n), optical bandgap (E_{04}) (*left*), extinction coefficient (k), and deposition rate (R_{dep}) (*right*) as a function of SiH_4 flow. The other process settings are listed in Table 5.1.

flows of 13 sccm and larger. The observed increase in extinction coefficient with SiH_4 flow is expected as the films get increasingly Si-rich. Figure 5.1-(*right*) also shows the deposition rate as a function of SiH_4 flow.

Table 5.5: Settings for the deposition process of the SiN films from the RF power series.

N_2 (sccm)	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	p (mTorr)	$T_{substrate}$ (^oC)
980	4	13.4	20 - 150	650	300

Table 5.6: Tauc-Lorentz parameters for the SiN films deposited in the RF power series.

Sample	P_{RF} (W)	A (eV)	E_0 (eV)	Γ (eV)	E_g (eV)
I	20	107.9	9.98	4.94	4.72
J	40	140.2	9.0	5.0	5.0
K	70	169.7	8.80	6.48	5.13
L	110	181.9	8.63	6.01	5.22
M	150	217.9	8.03	6.64	5.28

5.3.2 RF power

From literature [80] it is known that the RF power (P_{RF}) has an impact on both the surface passivation and the density of the SiN films. We have varied the RF power using the process settings summarized in Table 5.5. An SiH_4 flow of 4 sccm has been chosen as for this value the optical bandgap is largest. It has to be noted that also in this case all films have a target thickness of 200 nm. The Tauc-Lorentz parameters for the SiN films deposited in the RF power series are summarized in Table 5.6. The values for the resulting material properties and the deposition rates are summarized in Table 5.7. It has to be noted that in this study it was not possible to directly determine values for E_{04} above 5 eV. As this is the case for samples J - M, the values for E_{04} have not been specified. To give an indication of the influence of RF power on the bandgap E_g has been listed instead.

Figure 5.2 shows the influence of RF power on the refractive index (*left*) and on the deposition rate (*right*). It can clearly be seen that the refractive index only marginally increases as a function of RF power while the deposition rate significantly increases up to an RF power of 110 W. However, if the RF power is increased beyond this value it starts decreasing. The cause for this phenomenon might be related to the simultaneous etching of the growing SiN film, which depends on the energy of the ions in the plasma and consequently on the RF power.

Figure 5.3 shows E_g, as determined by SE, as a function of RF power. It can be seen that E_g continuously increases with RF power and that this increase is more pronounced for RF powers in the range of 20 W - 80 W than in that of 80 W - 150 W. From the RF power sweep it becomes

Table 5.7: Material properties of the 200 nm SiN films from the RF power series that have been determined from SE measurement data using the Tauc-Lorentz formalism. In addition, the values for E_g and R_{dep} are given.

Sample	P_{RF} (W)	n (2 eV)	k (3.44 eV)	E_g (eV)	R_{dep} (nm/min)
I	20	1.82	0	4.72	11.1
J	40	1.83	0	5.0	16.4
K	70	1.84	0	5.13	21.6
L	110	1.86	0	5.22	24.0
M	150	1.86	0	5.28	20.9

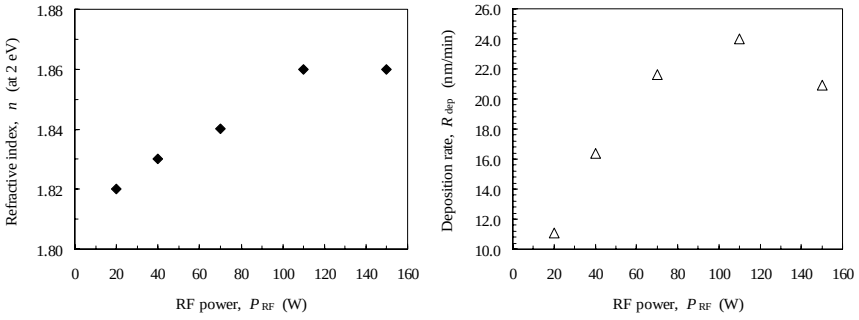

Figure 5.2: Influence of RF power on the refractive index (*left*) and on the deposition rate (*right*) of the SiN films from the RF power series.

clear that the (optical) bandgap of SiN films can be increased using a higher RF power while the refractive index only shows a minor increase. This is a clear indication for densification of the SiN films, which could be beneficial for the level of surface passivation [60]. However, too high RF power must be avoided to prevent the semiconductor surface form excessive plasma damage.

5.3.3 Total gas pressure

As a next step we have investigated the influence of the total gas pressure (p) on the material properties of the SiN films. The total gas pressure has been varied using the process settings summarized in Table 5.8. It has to be noted that the target thickness for all films is again 200 nm. The Tauc-Lorentz parameters for the SiN films deposited in the total gas pressure series

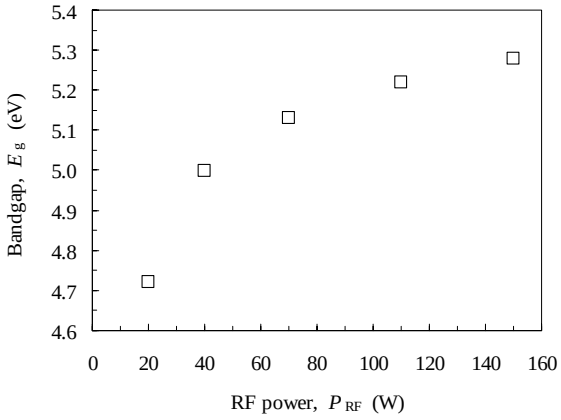

Figure 5.3: Bandgap (E_g), as determined by SE, as a function of RF power.

Table 5.8: Settings for the deposition process of the SiN films from the total gas pressure series.

N_2 (sccm)	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	p (mTorr)	$T_{substrate}$ (^oC)
980	10	13.4	110	150 - 650	300

are summarized in Table 5.9. The values for the resulting material properties, E_{04}, and R_{dep} are summarized in Table 5.10.

Figure 5.4 shows the influence of the total gas pressure on the refractive index (*left*) and on the deposition rate (*right*) of the SiN films. It can clearly be seen that the refractive index increases with total gas pressure and that the deposition rate also significantly increases with total gas pressure.

Figure 5.5 shows the influence of the total gas pressure on the value of E_{04}. It can be seen that E_{04} significantly decreases for increasing total gas pressure. From the total gas pressure sweep it can be concluded that the optical bandgap and the deposition rate are strong functions of the total gas pressure. Furthermore, it can be observed that the influence on the refractive index is reasonably large.

Table 5.9: Tauc-Lorentz parameters for the SiN films deposited in the total gas pressure series.

Sample	p (mTorr)	A (eV)	E_0 (eV)	Γ (eV)	E_g (eV)
N	150	196.4	8.3	9.8	4.95
O	400	103.1	10.2	6.7	4.10
P	650	79.1	9.9	9.9	3.67

Table 5.10: Material properties of the 200 nm SiN films from the total gas pressure series that have been determined from SE measurement data using the Tauc-Lorentz formalism. In addition, the values for E_{04} and R_{dep} are given.

Sample	p (mTorr)	n (2 eV)	k (3.44 eV)	E_{04} (eV)	R_{dep} (nm/min)
N	150	1.84	0	5.10	19.8
O	400	1.89	0	4.24	26.9
P	650	1.91	0	3.79	37.3

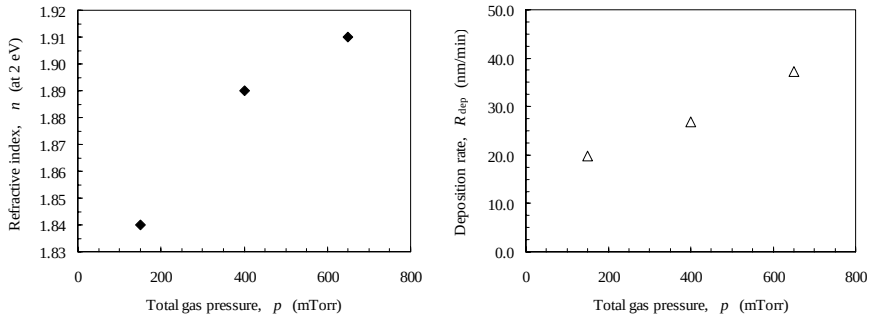

Figure 5.4: Influence of the total gas pressure on the refractive index (*left*) and on the deposition rate (*right*) of the SiN films from the total gas pressure series.

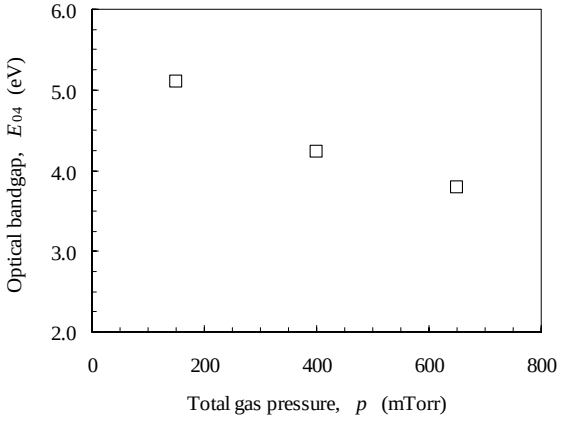

Figure 5.5: Influence of the total gas pressure on the optical bandgap (E_{04}) of the SiN films from the total gas pressure series.

5.3.4 Substrate temperature

Finally, we have investigated the influence of the substrate temperature ($T_{\text{substrate}}$) on the material properties of the SiN films and on both the configuration and amount of bonded hydrogen in these films. We have made a temperature series, i.e. 100 °C, 175 °C, 250 °C, 300 °C, and 350 °C, of the standard film, whose process settings have been listed in Table 5.1.

Influence on material properties

For these experiments, the deposited films have a target thickness of 100 nm. The Tauc-Lorentz parameters for the SiN films deposited in the temperature series are summarized in Table 5.11. The values for the resulting material properties, E_{04}, and R_{dep} are summarized in Table 5.12.

Figure 5.6-(*left*) shows the influence of the substrate temperature on the refractive index and optical bandgap. Figure 5.6-(*right*) shows the same for the extinction coefficient and deposition rate. It can clearly be seen that both the refractive index and extinction coefficient increase with the substrate temperature and that both the optical bandgap and deposition rate decrease if the substrate temperature is increased. Higher substrate temperatures lead to a densification of the SiN films deposited, which explains the increase of the refractive index and the decrease of the deposition rate. In addition, the increasing extinction coefficient indicates a larger incorporation of Si into the SiN layer which also contributes to the increase of the refractive index. From the temperature sweep it can be concluded that all properties, i.e. refractive index, extinction coefficient, optical bandgap, and deposition rate are strong functions of the substrate temperature.

Table 5.11: Tauc-Lorentz parameters for the SiN films deposited in the temperature series.

Sample	T (°C)	A (eV)	E_0 (eV)	Γ (eV)	E_g (eV)
Q	100	63.6	8.75	5.6	2.99
R	175	64.5	8.63	5.4	2.82
S	250	74.0	9.04	6.78	2.78
T	300	79.3	9.07	7.32	2.76
U	350	77.5	8.49	6.40	2.65

Table 5.12: Material properties of the 100 nm SiN films from the temperature series that have been determined from SE measurement data using the Tauc-Lorentz formalism. In addition, the values for E_{04} and R_{dep} are given.

Sample	T (°C)	n (2 eV)	k (3.44 eV)	E_{04} (eV)	R_{dep} (nm/min)
Q	100	1.84	0.010	3.10	15.8
R	175	1.90	0.020	2.92	13.8
S	250	1.95	0.025	2.87	13.0
T	300	2.01	0.030	2.85	12.7
U	350	2.04	0.042	2.74	11.3

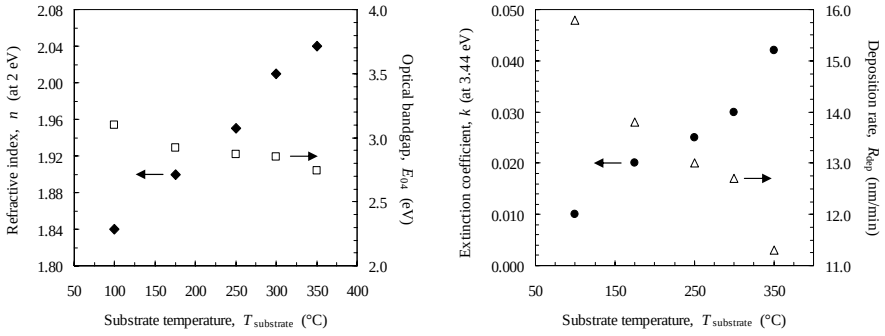

Figure 5.6: Influence of the substrate temperature on the refractive index and optical bandgap (*left*) and on the extinction coefficient and deposition rate (*right*) of the SiN films from the temperature series.

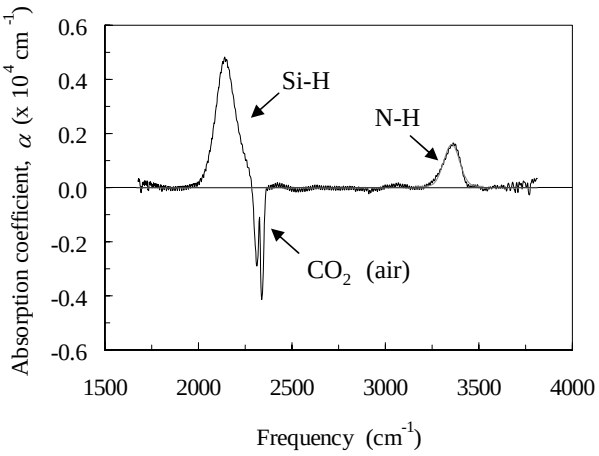

Figure 5.7: Typical FTIR spectrum of the standard SiN film deposited in the Oxford Plasmalab 100 PECVD system.

Influence on the configuration and amount of bonded hydrogen

FTIR measurements provide information about the configuration and amount of bonded hydrogen in the different SiN films from the temperature series. Figure 5.7 shows a typical FTIR spectrum of the standard SiN film whose process settings are listed in Table 5.1. Using the absorption peak positions proposed by Bustaret *et al*. [26], Fig. 5.7 clearly shows the presence of Si-H and N-H bonds and the absence of $N\text{-}H_2$ bonds. Figure 5.7 also points out that the standard film is deposited in the so-called simple radical deposition regime, which was mentioned in Sect. 5.2.2, as the film contains both Si-H and N-H bonds.

The hydrogen content of the SiN films can be determined by the integrated absorption of both Si-H and N-H stretching modes. The peak positions of the several Si-H and N-H configurations are well known [26] and their relative intensities can be determined. From the total Si-H and N-H absorption intensities, the amount of bonded hydrogen can be calculated using the proportionality constants proposed by Lanford *et al*. [100]. Figure 5.8 shows the integrated intensities as a function of the substrate temperature for the various Si-H (*left*) and N-H (*right*) stretching modes, respectively. Figure 5.9 shows the individual Si-H and N-H concentrations, and the total bonded hydrogen (H) concentration in the SiN films as a function of the substrate temperature.

Figures 5.8 and 5.9 show that the hydrogen content decreases with increasing substrate temperature. This behavior is observed for any PECVD SiN film, independent of the deposition method [15, 80]. Assuming an atomic hydrogen concentration of typically 8 - 10 x 10^{22} cm^{-3} [53], the total amount of bonded hydrogen is about 50 at% and 35 at% for substrate temperatures of 100 ^{o}C and 250 ^{o}C, respectively. These values are relatively high as values

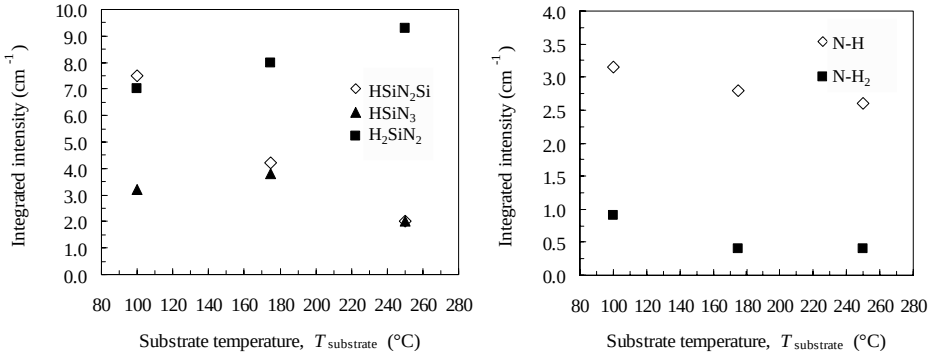

Figure 5.8: Integrated intensities as a function of the substrate temperature for the various Si-H (*left*) and N-H (*right*) stretching modes, respectively.

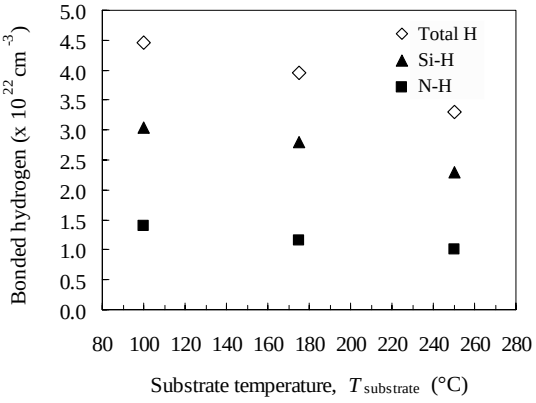

Figure 5.9: Individual Si-H and N-H concentrations, and the total bonded hydrogen (H) concentration in the SiN films as a function of the substrate temperature.

Table 5.13: Process settings and material properties of the SiN films whose passivation capability has been determined using effective minority lifetime measurements.

Sample	N_2 (sccm)	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	p (mTorr)	T (^oC)	n (2 eV)	E_{04} (eV)
V	980	4	13.4	110	650	300	1.86	5.22
W	980	10	13.4	110	650	300	1.91	3.78
X	980	16.6	13.4	20	650	300	2.01	2.85

between 10 at% and 30 at% are commonly reported [171].

5.3.5 Effective lifetime measurements

To investigate the influence of the material properties of the SiN films on their capability to passivate the surface of monocrystalline Si we have performed effective minority carrier lifetime measurements using a Sinton lifetime tester. The wafers used were p-type (resistivity of 8.4 Ωcm) 3 inch double sided polished float zone (FZ) monocrystalline Si wafers. Before SiN deposition the wafers have been cleaned using the standard RCA clean [79] followed by an HF dip. Table 5.13 gives an overview of the process settings and the material properties of the three SiN films whose passivation capability has been measured. We have chosen these films to investigate the effect of the refractive index and the optical bandgap on the passivation capability. It has to be noted that sample "X" is covered with the standard SiN film.

Figure 5.10 shows the effective minority carrier lifetimes of the three samples measured as a function of the carrier injection level. As mentioned in Sect. 5.2.2, the higher the effective minority carrier lifetime, the better the Si surface has been passivated. It can clearly be seen that the standard SiN film, sample "X", shows only a very moderate level of surface passivation as the effective minority carrier lifetime for an unpassivated wafer is about 2 μs. Sample "W" shows a reasonably good level of surface passivation as it is well over one order of magnitude higher than that of the standard film. The level of surface passivation of sample "V" is even worse than that of the standard film and is only slightly higher than that of an unpassivated wafer. This result can possibly be explained by the relatively low refractive index of this film.

During the measurements it has been observed that the level of surface passivation, especially for sample "W", was not stable over time. Therefore, the surface passivation induced by this SiN film has further been investigated on n-type monocrystalline Si wafers which have a resistivity of 1.3 Ωcm. Figure 5.11 shows the time-evolution of the effective minority carrier lifetime as a function of the injection level for a SiN film deposited with the same process settings as has been done for sample "W" on such an n-type wafer. It can be seen that the effective minority carrier lifetime increases with time. Further investigations are required to explain this behavior.

Finally, the influence of an anneal process on the surface passivation capability of this film,

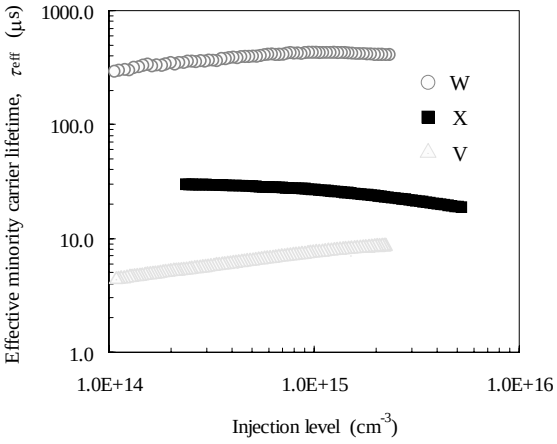

Figure 5.10: Measurement of the effective minority carrier lifetime on 8.4 Ωcm p-type double polished float zone (FZ) monocrystalline Si wafers as a function of the injection level for the SiN films whose process settings and material properties are summarized in Table 5.13.

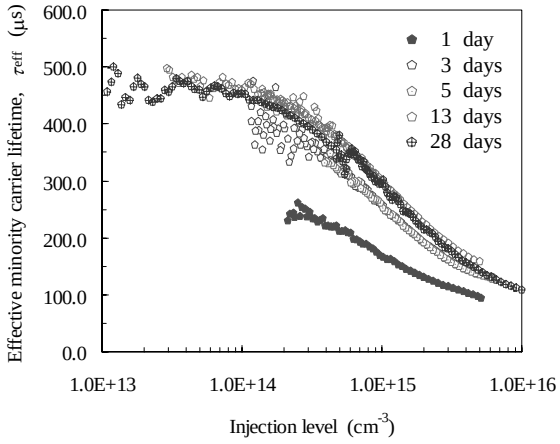

Figure 5.11: Time-evolution of the effective minority carrier lifetime as a function of the injection level for a SiN film deposited with the same process settings as has been done for sample "W" on 1.3 Ωcm n-type monocrystalline Si.

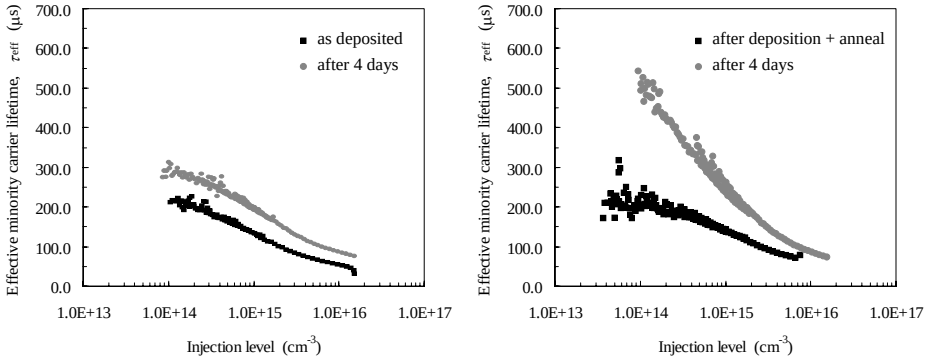

Figure 5.12: Effective minority carrier lifetimes as a function of the injection level directly after deposition and after 4 days for an as-deposited SiN film (*left*), and for a SiN film that has been annealed for 20 minutes in air at 400 °C directly after deposition (*right*).

i.e. similar process settings as for sample "W", has been investigated. This has been done for an as-deposited film and a film that was annealed for 20 minutes in air at 400 °C. Figure 5.12-(*left*) shows the passivation capabilities of the as-deposited film directly after deposition and 4 days after. Figure 5.12-(*right*) shows the same for the film that after deposition has been annealed for 20 minutes in air at 400 °C. It can be concluded that the anneal process does not have any effect on the surface passivation capability directly after deposition. However, over time the anneal process clearly has a big impact on the surface passivation capability.

5.3.6 Stress in PECVD SiN films

In Sect. 2.3.3, it has been discussed that the sheet carrier density confined at the heterojunction in AlGaN/GaN HFETs is a strong function of the piezoelectric polarization in the tensile strained AlGaN barrier layer. In Sect. 4.4 we have observed an increase of the value of the CW DC drain current ($I_{D,CW}$) after passivation of the AlGaN surface with the standard SiN film. This increase could be caused by increased sheet carrier density, increased electron mobility, or a combination of these two. Jeon *et al.* [71] have shown that the increase in drain current is caused by an increase in sheet carrier density, which is caused by an increase in the piezoelectric polarization in the tensile strained AlGaN layer due to additional external tensile stress induced by the SiN passivation film. Hence, from the (*I*-*V*) results shown in Fig. 4.16, Sect. 4.4, we can conclude that the type of stress induced by our standard SiN film on the AlGaN/GaN epilayers is tensile.

Knowing that the standard SiN film induces tensile stress on the AlGaN/GaN epilayers, we have first determined the amount (σ) and type of stress, tensile or compressive, induced by this

film on a Si substrate. Independent of the absolute result, this information serves as a reference that can be used to correlate the changes in the amount and type of stress of different SiN films deposited on Si substrates to changes in the stress induced by these films on AlGaN/GaN epilayers. The different films have been deposited on 4 inch monocrystalline Si substrates and the measurements have been performed by Eugene Timmering and Johan Klootwijk from Philips Research Laboratories Eindhoven.

From the range of SiN films that have been deposited on Si substrates using different process settings, we have selected a set of films for which we will investigate both the ability to passivate the AlGaN barrier layer of AlGaN/GaN HFETs and the amount of gate and drain leakage currents in these devices after deposition. The process settings and material properties of these films are listed in Table 5.14. We have chosen this set for the following reasons:

- sample "A" versus sample "G" (standard film), indicates the influence of the optical bandgap (E_{04}),
- sample "L" versus samples "A" and "G", separates the influence of the optical bandgap and RF power (P_{RF}),
- sample "W" versus sample "N", shows the influence of total gas pressure (p), and
- samples "G", "L", and "W", enable the correlation of the effective minority lifetime measurements on Si to the surface passivation of AlGaN.

To investigate the influence of the hydrogen content of SiN films on their capability of passivating the AlGaN barrier layer, we have also tested the films from the substrate temperature series on AlGaN/GaN HFETs. The process settings and material properties of these films have also been listed in Table 5.14.

The amount (σ) and type of stress, tensile or compressive, induced by the films listed in Table 5.14 on 4 inch monocrystalline Si substrates have been determined. The results for the films deposited at 300 $^{\mathrm{o}}$C are listed in Table 5.15. The results for the films from the temperature series are shown in Fig. 5.13. It has to be noted that the target thickness of all films is 100 nm.

From Table 5.15 it becomes clear that all SiN films induce tensile stress on the Si substrates which is the same type of stress induced by the standard film on the AlGaN/GaN epilayers. Hence, we assume that deposition of films "G", "A", "L", and "N" on AlGaN/GaN HFETs will result in an increased DC drain current. The influence on the electrical device results will be described in Sect. 5.4. Figure 5.13 shows that all films but the one deposited at 100 $^{\mathrm{o}}$C induce tensile stress on the Si substrates. In addition, it can be observed that the amount of stress is a strong function of the substrate temperature.

5.4 Influence of SiN properties and surface preparation on passivation and leakage

In this section we will describe the influence of the film properties of the different PECVD SiN films listed in Table 5.14 and the preparation of the AlGaN barrier layer before SiN deposition

Table 5.14: Process settings and material properties of the SiN films that have been selected to investigate both the ability to passivate the AlGaN barrier layer of AlGaN/GaN HFETs and the amount of gate and drain leakage currents in these devices after deposition.

Sample	SiH_4 (sccm)	NH_3 (sccm)	P_{RF} (W)	p (mTorr)	T (^oC)	n (2 eV)	k (3.44 eV)	E_{04} (eV)
H	20	13.4	20	650	300	2.07	0.078	2.68
G	16.6	13.4	20	650	300	2.01	0.030	2.85
C	10	13.4	20	650	300	1.88	0	4.15
A	4	13.4	20	650	300	1.82	0	4.38
L	4	13.4	110	650	300	1.86	0	5.22
W	10	13.4	110	650	300	1.91	0	3.78
N	12	13.4	110	150	300	1.86	0	4.99
Q	16.6	13.4	20	650	100	1.84	0.010	3.10
R	16.6	13.4	20	650	175	1.90	0.020	2.92
S	16.6	13.4	20	650	250	1.95	0.025	2.87
U	16.6	13.4	20	650	350	2.04	0.042	2.74

Table 5.15: Amount and type of stress induced by selected films on 4 inch monocrystalline Si substrates. The target thickness of all films is 100 nm.

Sample	σ (MPa)	type
G	390	tensile
A	540	tensile
L	350	tensile
N	450	tensile

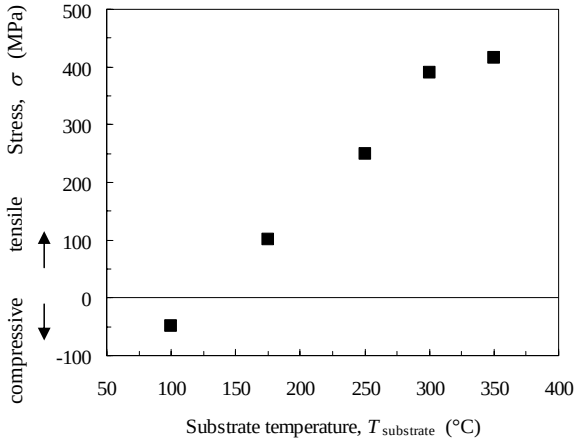

Figure 5.13: Amount and type of stress induced by SiN films from substrate temperature series on 4 inch monocrystalline Si substrates. The target thickness of all films is 100 nm.

Table 5.16: Overview of the n.i.d. AlGaN/GaN epilayers on sapphire grown by RU.

$d_{GaN,nucl.\ layer}$ (nm)	$d_{GaN,\ buffer}$ (μm)	$d_{AlGaN,\ barrier}$ (nm)	Al (%)	R_{sheet} (Ω/sq.)	n_s (cm^{-2})	μ (cm^2/Vs)
30	2	23	25	450	8.0 x 10^{12}	1200

on the surface passivation and amount of gate and drain leakage currents of n.i.d. AlGaN/GaN HFETs on sapphire substrates using CW and pulsed DC (*I-V*), and microwave CW active load pull measurements. Details of the n.i.d. epitaxial layer stack, which has been grown by RU, are listed in Table 5.16.

5.4.1 Influence of SiN film properties on passivation of AlGaN layer and leakage currents

The influence of the different SiN films on the surface passivation has been determined by pulsed DC *I-V* measurements, as described in Sect. 4.4, on small periphery fat gate devices (W_g = 2 x 40 μm, L_g = 2 μm) fabricated with the "Inverse Mesa" mask set. It has to be noted that all devices have been fabricated in the same way up to the point of surface passivation, i.e. BHF dip at the start of the processing and RIE Ar treatment before the ohmic contact anneal. We have used CW DC (*I-V*) measurements to determine the gate and drain leakage currents at

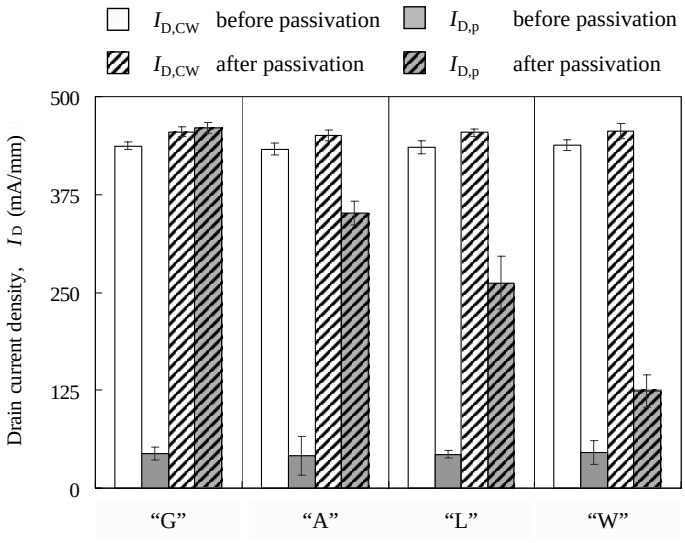

Figure 5.14: Pulsed and CW drain current measurements before and after passivation with 100 nm of films "G", "A", "L", and "W", respectively on fat gate n.i.d. AlGaN/GaN devices on sapphire substrates. The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

pinch-off before and after SiN passivation.

Figure 5.14 shows pulsed and CW drain current measurements before and after passivation with 100 nm of films "G", "A", "L", and "W", respectively. The clear bars represent average values of the CW DC drain current density ($I_{D,CW}$) (white) and the pulsed DC drain current density ($I_{D,p}$) (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

Figure 5.15 shows the gate and drain leakage current densities at pinch-off before and after passivation with 100 nm of films "G", "A", "L", and "W", respectively. The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

Figure 5.14 suggests that film "G" is the best choice to achieve good surface passivation as it is the only film capable of completely eliminating gate lag. It should be noted that the strong

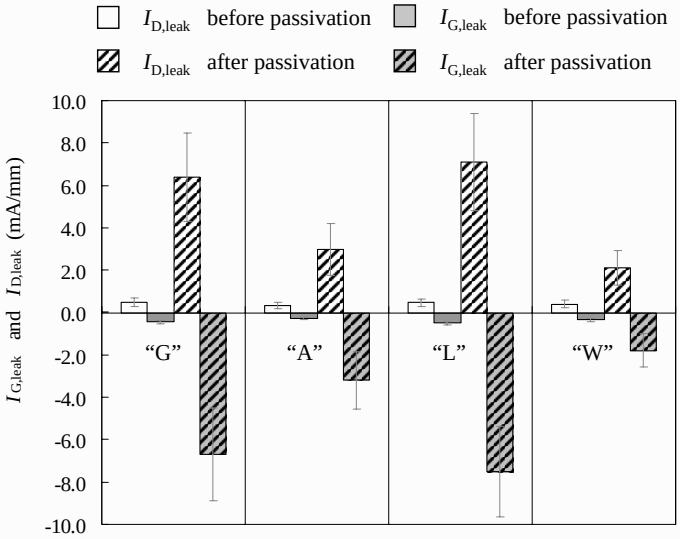

Figure 5.15: Gate and drain leakage current densities at pinch-off before and after passivation with 100 nm of films "G", "A", "L", and "W", respectively. The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

reduction of self-heating under pulsed measurement conditions causes $I_{D,p}$ to be higher than the corresponding $I_{D,CW}$ for this film. The result for film "W" clearly indicates that there is no correlation between the level of surface passivation of monocrystalline Si substrates and the amount of gate lag elimination after deposition on AlGaN/GaN epilayers. Furthermore, it can be seen that the value of $I_{D,CW}$ after passivation for all films is higher than before passivation. This confirms that all SiN films induce tensile stress on the AlGaN/GaN epilayers as described in Sect. 5.3.6.

Figure 5.15 shows that films "A" and "W" show the smallest gate and drain leakage current densities at pinch-off. The behavior of film "L" is quite surprising as it has the largest optical bandgap. This results indicates that there is no clear correlation between the value of the optical bandgap and the amount of gate and drain leakage currents after surface passivation.

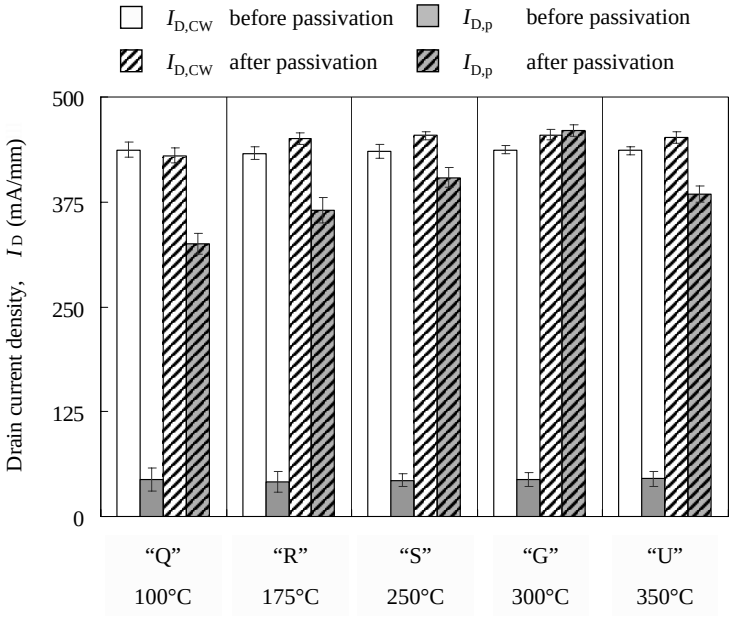

Figure 5.16: Pulsed and CW drain current measurements before and after passivation with 100 nm of films "Q", "R", "S", "G", and "U", from the temperature series on fat gate n.i.d. AlGaN/GaN devices on sapphire substrates. The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

Temperature series

To determine the influence of the hydrogen content of SiN films on the surface passivation and amount of gate and drain leakage currents we have deposited 100 nm of films "Q", "R", "S", "G", and "U", see Table 5.14, on the n.i.d. AlGaN/GaN devices. Figures 5.16 and 5.17 show pulsed and CW drain current measurements before and after passivation, and gate and drain leakage current densities for the different films from the temperature series, respectively.

Figure 5.16 shows that film "G" achieves the best surface passivation. This clearly points out that the hydrogen content does not play the same role in surface passivation of AlGaN/GaN HFETs as it does in surface passivation of monocrystalline Si substrates. In addition, it should be noted that only for film "Q", the CW drain current ($I_{D,CW}$) after passivation is slightly lower that before passivation. This could be caused by the fact that this film induces compressive stress on the AlGaN/GaN epilayers whereas the films deposited at higher temperatures induce tensile stress. This result correlates with the measurements of the amount and type of

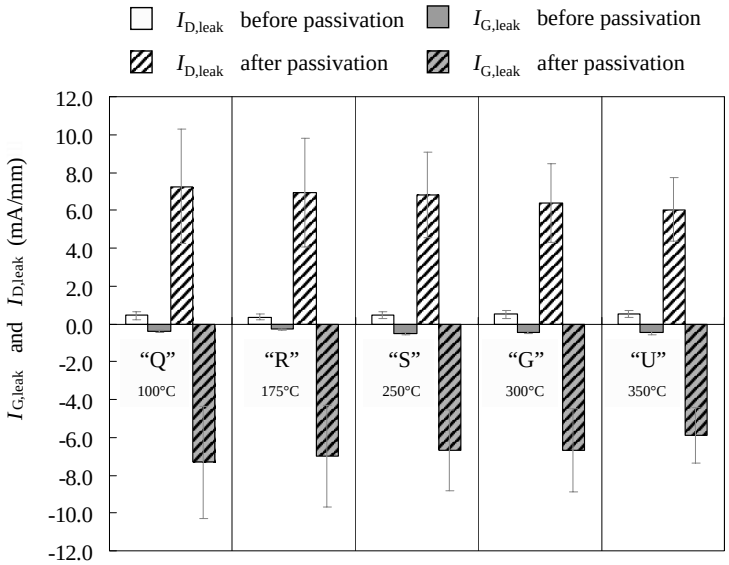

Figure 5.17: Gate and drain leakage current densities at pinch-off before and after passivation with 100 nm of films "Q", "R", "S", "G", and "U", from the temperature series. The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

stress as a function of substrate temperature on monocrystalline Si substrates as described in Sect. 5.3.6. Figure 5.16 clearly shows that the hydrogen content hardly influences the gate and drain leakage current densities at pinch-off. The increase of these leakage current densities, and especially that of the gate leakage current, after SiN deposition remains unacceptably large to establish high-power device operation.

SiH_4 flow

Although the gate and drain leakage current densities after SiN deposition are too high, up to this point in our investigation, film "G" seems to be the best choice to achieve good passivation of the AlGaN barrier layer. In Sect. 5.3.1, we have seen that the extinction coefficient (k) at 3.44 eV, whose value is a measure for the amount and presence of Si-Si bonds, can be decreased by lowering the silane (SiH_4) flow. To investigate the influence of the SiH_4 flow on the surface passivation, and gate and drain leakage current densities, we have deposited 100 nm of films "A", "C", "G", and "H", see Table 5.14. Figures 5.18 and 5.19 show pulsed and CW drain

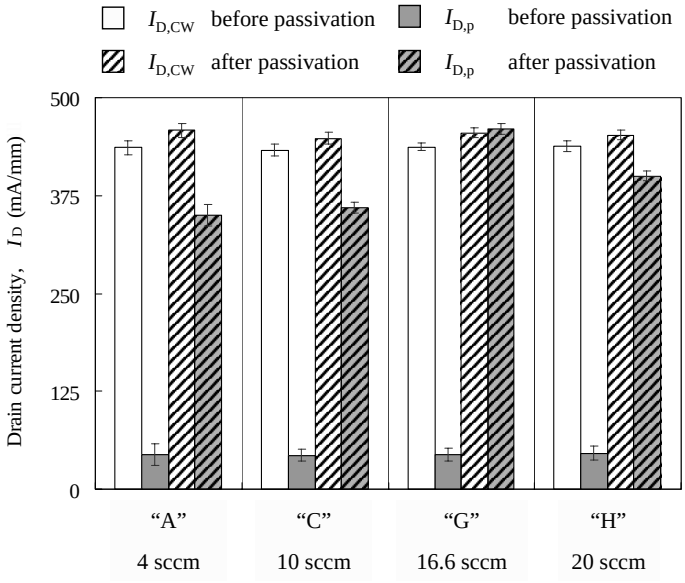

Figure 5.18: Pulsed and CW drain current measurements before and after passivation with 100 nm of films "A", "C", "G", and "H", see Table 5.14, from the SiH_4 flow series on fat gate n.i.d. AlGaN/GaN devices on sapphire substrates. The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

current measurements before and after passivation, and gate and drain leakage current densities for the different films from the SiH_4 flow series, respectively.

Although Fig. 5.19 shows that the gate and drain leakage current densities can be decreased by lowering the SiH_4 flow, Fig. 5.18 clearly shows that film "G" should be used to achieve the best AlGaN surface passivation.

Thickness series

Finally, we have deposited SiN films, using the process settings for film "G", with thicknesses of 50 nm, 100 nm, 200 nm, and 400 nm, to investigate the influence of the amount of induced stress on AlGaN surface passivation and gate and drain leakage currents. Figures 5.20 and 5.21 show pulsed and CW drain current measurements before and after passivation, and gate and drain leakage current densities for the different films from the thickness series, respectively.

Figure 5.20 shows that 100 nm is the optimum thickness for film "G" to achieve optimum passivation of the AlGaN barrier layer. Figure 5.21 shows that the gate and drain leakage

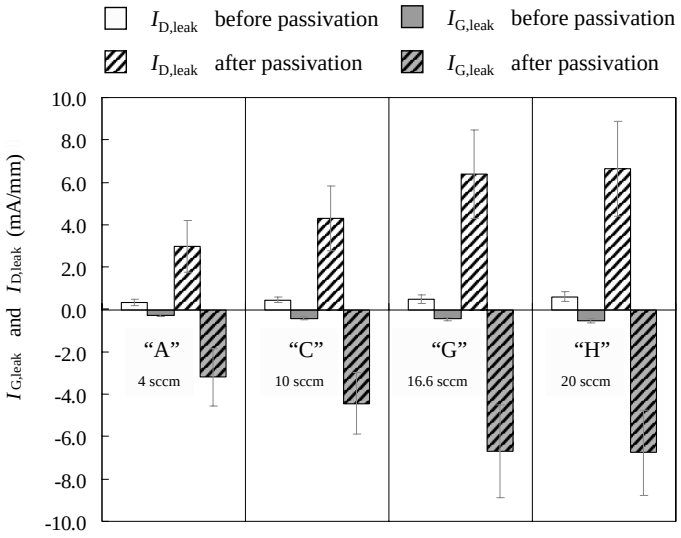

Figure 5.19: Gate and drain leakage current densities at pinch-off before and after passivation with 100 nm of films "A", "C", "G", and "H", see Table 5.14, from the SiH_4 flow series. The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

current densities are still unacceptably high. It is clear that we have to investigate treatments to prepare the AlGaN barrier layer before SiN deposition. This will be the subject of Sect. 5.4.2.

5.4.2 Influence of surface preparation on passivation of AlGaN layer and leakage currents

Although the observed increase of the drain leakage current density after SiN deposition is undesired, it does not have a very big influence on the drain current swing. However, the increased gate leakage current density significantly reduces the maximum breakdown voltage and hence the drain-source voltage swing. It is obvious that this is detrimental for high-power operation of the AlGaN/GaN HFETs.

It has been reported that the gate leakage current is very sensitive to surface preparation and is therefore attributed to surface leakage [48, 109, 154]. In addition, it is shown that the increase of the gate leakage current is not caused by the PECVD process as it returns to its

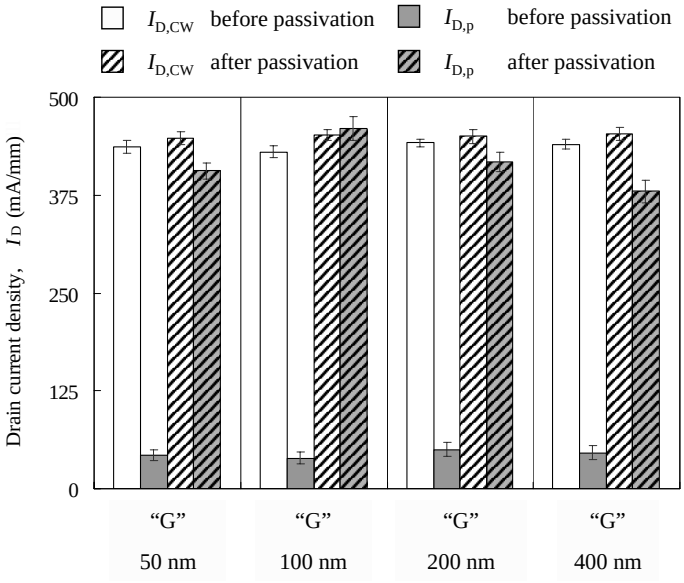

Figure 5.20: Pulsed and CW drain current measurements before and after passivation with film "G" using thicknesses of 50 nm, 100 nm, 200 nm , and 400 nm, respectively. The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

original level upon removal of the deposited SiN film. We have observed the same reversible behavior of the gate leakage current and therefore conclude that our PECVD process does not cause damage to the AlGaN surface such that it is responsible for the increase of the gate leakage observed after SiN deposition.

Preparation of the AlGaN barrier layer before SiN deposition can be done by a combination of organic cleaning, using acetone and iso-propyl alcohol (IPA), and wet etching either using dilute hydrofluoric acid (HF), buffered HF (BHF), or dilute ammonia (NH_4OH) [48, 109, 154]. Regarding the mmTor process flow we have chosen to use NH_4OH to avoid degradation of the Ti/Al/Ni/Au ohmic contacts as Ti is attacked by HF and BHF. We have applied a short NH_4OH dip for 1 minute to avoid adhesion problems with the gold (Au) optical alignment marks. Figures 5.22 and 5.23 show the influence of the NH_4OH dip on the pulsed and CW drain current measurements, and the gate and drain leakage current densities, respectively before and after passivation with 100 nm of film "G".

Figure 5.22 shows that the NH_4OH dip does not influence the AlGaN surface passivation capability of film "G". However, Fig. 5.23 shows that the NH_4OH dip causes an enormous reduction of both the gate and drain leakage current densities. This result confirms that proper

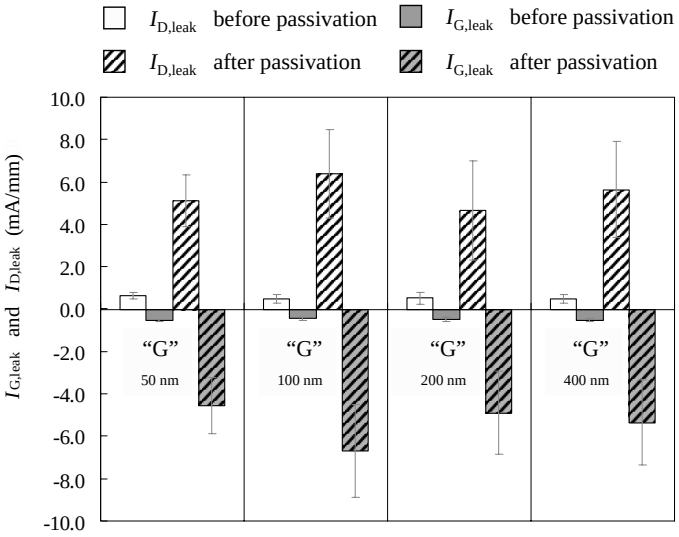

Figure 5.21: Gate and drain leakage current densities at pinch-off before and after passivation with film "G" using thicknesses of 50 nm, 100 nm, 200 nm , and 400 nm, respectively. The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

preparation of the AlGaN surface directly before SiN deposition is very important to achieve leakage current levels required for high-power device operation.

5.5 Conclusions

In Sect. 4.4 it has clearly been shown that the AlGaN barrier of HFETs on sapphire and s.i. SiC substrates can effectively be passivated using the combination of a BHF wet etch, an Ar RIE etch, and a PECVD SiN film (100 nm, 300 °C, refractive index between 1.97 - 2.01 at 2 eV). However, after passivation with this standard SiN film a significant increase in the gate and drain leakage currents has been observed. Although the increased drain leakage current density after SiN deposition is undesired, it does not severely reduce the drain current swing. However, the increased gate leakage current significantly reduces the maximum breakdown voltage and hence the drain-source voltage swing, which obviously is detrimental for high-power device operation.

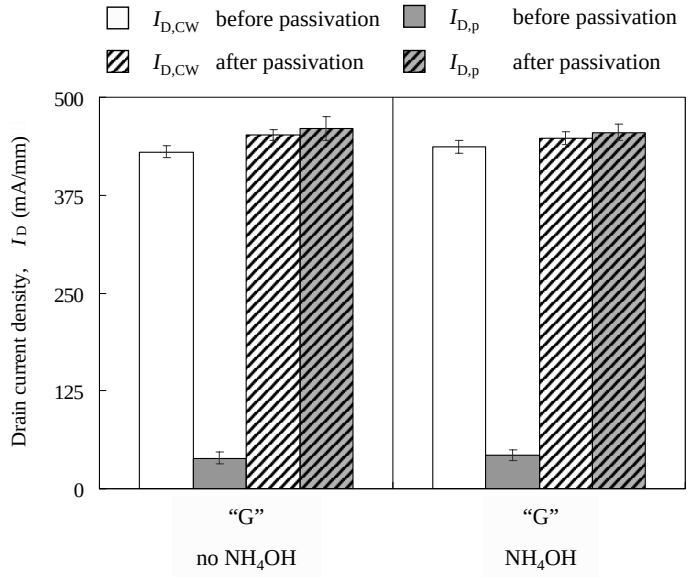

Figure 5.22: Influence of the NH_4OH dip on the pulsed and CW drain current measurements before and after passivation with 100 nm of film "G". The clear bars represent average values of $I_{D,CW}$ (white) and $I_{D,p}$ (grey) before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

As we assumed that the cause for the increased gate leakage current was related to the SiN-AlGaN interface, we have investigated if changing the composition of the PECVD SiN film or preparation of the AlGaN barrier layer before SiN deposition, or both, results in decreased leakage currents after SiN deposition. It should be noted that the surface passivation capability should remain equal to that of the standard film.

This chapter started with a description of our investigations of the influence of the process settings of an Oxford Plasmalab 100 PECVD system on the SiN film properties. It has to be noted that this work, as it has been done on monocrystalline Si substrates, can only be used as an indirect reference for the investigations of the surface passivation and amount of gate and drain leakage currents of AlGaN/GaN HFETs after passivation. Nevertheless, we have established an overview of the capabilities of the Oxford Plasmalab 100 PECVD system and gained an understanding about how film properties such as refractive index, extinction coefficient, optical bandgap, and stress can be influenced by the process settings, i.e. gas flow, RF power, substrate temperature, and total gas pressure.

From the range of SiN films that have been deposited on Si substrates using different process settings, we have selected a set of films, see Table 5.14, for which we have investigated

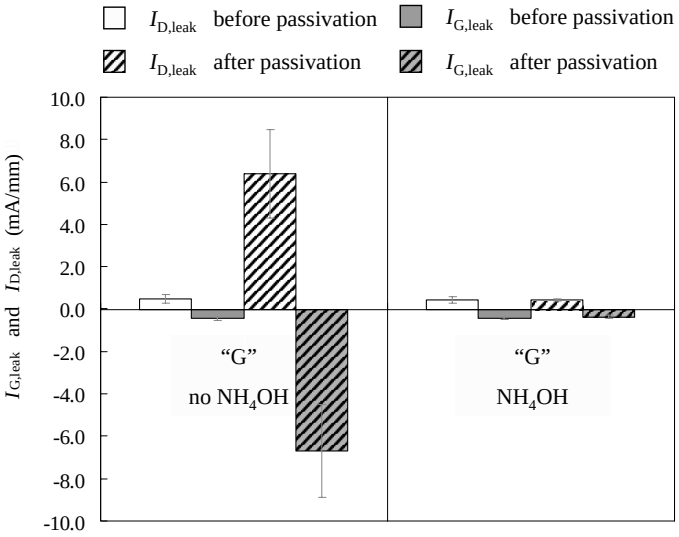

Figure 5.23: Influence of the NH_4OH dip on the gate and drain leakage current densities at pinch-off before and after passivation with 100 nm of film "G". The white and grey clear bars represent average values of the CW DC gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$), respectively before SiN passivation. The corresponding dashed bars represent average values of these quantities after passivation. The error bars indicate the standard deviation of the measured values.

both the ability to passivate the AlGaN barrier layer of AlGaN/GaN HFETs and the amount of gate and drain leakage currents in these devices after deposition. It has to be noted that all devices have been fabricated in the same way up to the point of surface passivation, i.e. BHF wet etch at the start of the processing and RIE Ar etch before the ohmic contact anneal. Comparing the results for gate lag elimination, and the level of gate and drain leakage current densities after passivation with 100 nm of films, "G", "A", "L", and "W", which have been deposited using different process settings with respect to SiH_4 flow, RF power (P_{RF}), and total gas pressure (p), see Table 5.14, the following conclusions can be drawn:

- film "G" (SiH_4 = 16.6 sccm, N_2 = 980 sccm, NH_3 = 13.4 sccm, P_{RF} = 20 W, p = 650 mTorr, T = 300 °C) is the best choice to achieve good surface passivation as it is the only film capable of completely eliminating gate lag,

- these films induce tensile stress on the AlGaN/GaN epilayers as the value of the CW DC drain current ($I_{D,CW}$) after passivation is higher than before passivation,

- there is no correlation between the level of surface passivation of monocrystalline Si substrates and the amount of gate lag elimination after deposition on AlGaN/GaN epilayers, and

- there is no clear correlation between the value of the optical bandgap (E_{04}) and the amount of gate and drain leakage currents after surface passivation.

From the temperature series, films "Q", "R", "S", "G", and "U" (Table 5.14) respectively, we can conclude that the hydrogen content of the SiN films does not play the same role in surface passivation of AlGaN/GaN HFETs as it does in surface passivation of monocrystalline Si substrates.

From the SiH_4 flow series, films "A", "C", "G", and "H" (Table 5.14) respectively, it can be concluded that the value of the extinction coefficient (k) at 3.44 eV, which is a measure for the amount and presence of Si-Si bonds, should be minimized to reduce the gate and drain leakage currents after SiN deposition. However, the best passivation of the AlGaN surface is achieved by film "G" for which the value of the extinction coefficient equals 0.030.

From the results of the thickness series, 50 nm, 100 nm, 200 nm , and 400 nm of film "G" respectively, it can be concluded that 100 nm is the optimum thickness for this film to achieve good passivation of the AlGaN barrier layer.

Finally, as the gate and drain leakage current densities remained unacceptably high for high-power device operation, we have investigated the influence of the preparation of the AlGaN barrier layer directly before SiN deposition on both gate lag elimination and the gate and drain leakage current densities after passivation with 100 nm of film "G". It has been reported that the gate leakage current is very sensitive to surface preparation and is therefore attributed to surface leakage [48, 109, 154]. In addition, it is shown that the increase of the gate leakage current is not caused by the PECVD process as it returns to its original level upon removal of the deposited SiN film. We have observed the same reversible behavior of the gate leakage current and therefore conclude that our PECVD process does not cause damage to the AlGaN surface such that it is responsible for the increase of the gate leakage observed after SiN deposition. Preparation of the AlGaN surface can be done by a combination of organic cleaning, using acetone and iso-propyl alcohol (IPA), and wet etching either using dilute hydrofluoric acid (HF), buffered HF (BHF), or dilute ammonia (NH_4OH) [48, 109]. Regarding the mmTor process flow we have chosen to use NH_4OH to avoid degradation of the Ti/Al/Ni/Au ohmic contacts as Ti is attacked by HF and BHF. We have applied a short NH_4OH dip for 1 minute to avoid adhesion problems with the gold (Au) optical alignment marks. Although the NH_4OH dip does not influence the AlGaN surface passivation capability of film "G", it causes an enormous reduction of both the gate and drain leakage current densities from about 6.7 mA/mm to 400 μA/mm. This result confirms that proper preparation of the AlGaN surface directly before SiN deposition is very important to achieve leakage current levels required for high-power device operation.

To conclude, passivation of the AlGaN barrier layer of the large periphery microwave high-power AlGaN/GaN HFETs, whose performance will be presented in Chapter 6, has been done using an NH_4OH dip for 1 minute, which is immediately followed by the deposition of 100

nm SiN according to the PECVD process settings for film "G" (SiH_4 = 16.6 sccm, N_2 = 980 sccm, NH_3 = 13.4 sccm, P_{RF} = 20 W, p = 650 mTorr, T = 300 ^{o}C).

Chapter 6

Device results

In this chapter we will present measurement results of small and large gate periphery HFETs fabricated by TU/e using MOCVD n.i.d. AlGaN/GaN epilayers on s.i. 4H-SiC substrates grown by RU [146]. The development of both the epitaxial growth process, and the process technology required to fabricate microwave high-power HFETs have proven to be major challenges and therefore are the main topics of this thesis. The measurement results presented in this chapter, will illustrate the successful integration of process modules such as ohmic and Schottky contact technology, device isolation, electron beam lithography, surface passivation, and air bridge technology, into a process flow that enables the fabrication of large n.i.d. AlGaN/GaN HFETs that are capable of producing an output power density of 11.9 W/mm at S-band (2 GHz - 4 GHz).

6.1 Introduction

We will start with a brief description of the measurement techniques used to determine the DC (*I*-*V*) characteristics, the small-signal *S*-parameters, and the microwave power performance of both small and large gate periphery n.i.d. AlGaN/GaN HFETs on s.i. 4H-SiC substrates. Next, we will present the measurement results of the small devices which have a total gate width (W_g) of 80 μm and a gate length (L_g) of 0.25 μm. These devices, which have been fabricated using the "*Submu*" mask set described in Sect. 3.2.1, have been used for short loop experiments to tune the fabrication process before fabricating the large devices with values for W_g of 0.25 mm, 0.5 mm, and 1.0 mm, respectively. After this, we will present the measurement results of these large AlGaN/GaN HFETs, which have values for L_g of 0.7 μm and have been fabricated using the "*mmTor*" mask set that has also been described in Sect. 3.2.1. Finally, we will present the conclusions that can be drawn from the measurement results.

6.2 Measurement techniques

In this section, we will give a brief description of the measurement techniques used to determine the DC (*I*-*V*) characteristics, the small-signal *S*-parameters, and the microwave power performance of both small and large gate periphery n.i.d. AlGaN/GaN HFETs on s.i. 4H-SiC substrates. All measurements have been performed on-wafer using ground-signal-ground (GSG) RF probes and without any active chip cooling. The measurements have been performed in cooperation with Thieu Kwaspen from TU/e, Erwin Suijker from TNO Defence, Security and Safety, Thomas Rödle from Philips Semiconductors, and Iouri Volokhine from Philips Research Eindhoven. The scope of the measurements has been to monitor the influence of device design, both epitaxial design and layout, and processing on device performance. Figures of merit used to evaluate the latter are the minimum value of the knee voltage (V_{knee}) and the maximum values of the:

- drain current (I_{D}),
- gate and drain leakage currents at pinch-off ($I_{\mathrm{G,leak}}$ and $I_{\mathrm{D,leak}}$),
- breakdown voltage (V_{BD}),
- extrinsic transconductance ($g_{\mathrm{m,ext}}$),
- extrinsic unity current gain frequency (f_{T}),
- extrinsic unity power gain frequency (f_{max}),
- output power (P_{out}) and output power density (P_{D}),
- associated power gain (G_{p}), and
- power added efficiency (PAE).

6.2.1 DC current-voltage measurements

The DC (*I*-*V*) output characteristics, i.e. $(I_{\mathrm{D}} - V_{\mathrm{DS}})$, and the transfer characteristics, i.e. $(I_{\mathrm{D}} - V_{\mathrm{GS}})$, of the AlGaN/GaN HFETs have been obtained either by continuous wave (CW) or pulsed on-wafer measurements using an HP4142B DC supply at TNO Defence, Security and Safety. As no active cooling of the devices under test (DUTs) has been applied, we have done pulsed measurements for devices with total gate peripheries larger than 250 μm to avoid excessive self-heating and the resulting decrease of the drain current for increasing drain-source (V_{DS}) bias voltages. This decrease of the drain current can be observed in the output characteristics as a negative slope of the $(I_{\mathrm{D}} - V_{\mathrm{DS}})$ curves in the saturation region, i.e. $V_{\mathrm{DS}} > V_{\mathrm{knee}}$. The pulsed *I*-*V* measurements were performed using a pulse width (PW) of 10 μs, and a duty cycle (dc) of 10 %.

From the DC *I*-*V* measurements we have determined values for $I_{\mathrm{D,max}}$, $I_{\mathrm{G,leak}}$, $I_{\mathrm{D,leak}}$, V_{BD}, V_{knee}, and $g_{\mathrm{m,ext}}$. To estimate the microwave output power that can be achieved if the device is

biased in class A, i.e. I_D= 0.5·$I_{D,max}$, we can use Eqn. 2.16. However, as the processed devices suffer from a certain amount of drain leakage current at pinch-off ($I_{D,leak}$), the term $I_{D,max}$ in Eqn. 2.16 has to be replaced by $(I_{D,max} - I_{D,leak})$, yielding

$$P_{out,max} = \frac{(V_{BD} - V_{knee}) \cdot (I_{D,max} - I_{D,leak})}{8}. \tag{6.1}$$

The maximum drain current densities of state-of-the-art AlGaN/GaN HFETs range from 1.0 A/mm to 1.5 A/mm [8, 85, 174]. Hence, from Eqn. 6.1 it is obvious that breakdown voltages over 160 V are required to achieve record output power densities larger than 30 W/mm [174] for class A operation. For breakdown voltages the distinction between off-state and on-state breakdown voltages ($V_{BD,off}$ and $V_{BD,on}$, respectively) is often made due to the difference in breakdown mechanism. In general, $V_{BD,off}$ is dominated by a combination of thermionic field emission (TFE) and tunneling of electrons from the gate into the channel, whereas impact ionization in the channel, when a considerable amount of current is flowing through the device, dominates $V_{BD,on}$ [120, 152]. The operation class used obviously determines whether $V_{BD,off}$ or $V_{BD,on}$ is mostly relevant when choosing the drain-source bias voltage.

The extrinsic transconductance (g_m) can be determined from the transfer characteristics using

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=\text{constant}}. \tag{6.2}$$

Together with the value for the extrinsic unity current gain frequency (f_T), which can be determined from small-signal *S*-parameter measurements as will be discussed in Sect. 6.2.2, the gate-source capacitance (C_{gs}) can be calculated using Eqn. 4.3.

6.2.2 Small-signal *S*-parameter measurements

Linear components, or nonlinear components, e.g. transistors, operating with signals sufficiently small to cause them to respond in a linear manner, can be completely characterized by parameters measured at their input and output terminals (ports) while considering the actual component as a "black box". Among the many representations available, e.g. *Z*-, *Y*-, and *h*-parameters, scattering or *S*-parameters [96] are the most convenient to use for the characterization of components at microwave frequencies because *S*-parameters can easily be determined from the measured ratios of the incident (a_i) and reflected (b_i) power waves using a network analyzer. The small-signal *S*-parameter measurements have been performed by Thieu Kwaspen from TU/e, Erwin Suijker from TNO Defence, Security and Safety, and Thomas Rödle from Philips Semiconductors using an HP8510C network analyzer in combination with an HP85110A pulsed test-set. Figure 6.1 shows these power waves and the individual *S*-parameters in the case of a two-port component, e.g. a transistor where the gate-source and the drain-source terminals are considered as the input and output ports, respectively.

From Fig. 6.1, it becomes clear that the relations between the input and the output of the two-port can be represented as

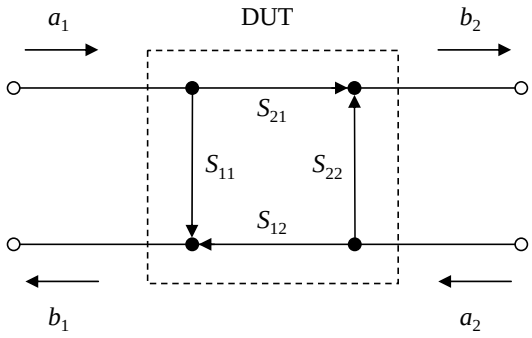

Figure 6.1: Graph representation of a two-port component showing the relations between the incident (a_i) and reflected (b_i) power waves and the individual *S*-parameters.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{6.3}$$

where the *S*-parameters S_{11}, S_{12}, S_{21}, and S_{22}, represent reflection and transmission coefficients. The measurement of these coefficients only requires termination of the DUT with the characteristic impedance of the measurement system, which for our measurements equals 50 Ω. The additional advantage of terminating the DUTs with this characteristic impedance is that they are stable at microwave frequencies [39]. These are major advantages compared to the measurement of *Z*- and *Y*-parameters for which good open and short terminations are required. These standards are not only difficult to realize at microwave frequencies, especially for on-wafer measurements, but can also cause active devices, e.g. transistors, to start oscillating [39, 47].

In a certain bias point and under small-signal conditions, the magnitude and phase of the *S*-parameters of a transistor are measured as a function of frequency. With this data, values for f_T, and the extrinsic unity power gain frequency (f_{max}) can be determined. The frequency at which the magnitude of the current gain (h_{21}), which expressed in *S*-parameters is given by Eqn. 6.4 [111], equals one is defined as f_T, and the frequency at which Mason's unilateral power gain (U), which expressed in *S*-parameters is given by Eqn. 6.5 [117], equals one is defined as f_{max}.

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \tag{6.4}$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[K\left|\frac{S_{21}}{S_{12}}\right| - \mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)\right]} \tag{6.5}$$

In Eqn. 6.5, K is the Rollet stability factor, which expressed in S-parameters, is given by [144]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}. \tag{6.6}$$

The value of K determines whether a transistor operates stable at the frequency of interest or has a tendency to start oscillating. For $K > 1$, and $|S_{11}S_{22} - S_{12}S_{21}| < 1$, the transistor operates unconditionally stable whereas for $K \leq 1$, the stability of the transistor depends on the source and load terminations and hence is called conditionally stable. For $K < 0$, transistor operation is unstable. It has to be noted that the validity of K is rather limited. Actually, it can only be applied to discrete devices without any external feedback. In practice, the use of K is valid for a maximum of two amplifier stages. Furthermore, it cannot be used for devices that are connected in parallel, which however is very common practice in the case of high-power amplifiers.

Figure 6.2 shows the theoretical determination of the values for f_T and f_{max} from plots of the magnitudes of the current gain and the unilateral power gain, $|h_{12}|^2$ and $|U|$ respectively, in decibels (dB) on a linear scale, versus frequency (f) on a logarithmic scale. It has to be noted that the magnitude of both gains rolls off at a theoretical rate of 6 dB/octave or 20 dB/decade. Hence, extrapolation of measurement results to determine the values for f_T and f_{max} in practical situations have to be done in those regions where the gain roll-off equals 6 dB/octave.

Besides the determination of the high-frequency response of the HFETs from the measured small-signal S-parameters, a start value for the load reflection coefficient (Γ_L), which is used in the active load-pull measurements that will be discussed in Sect. 6.2.3, is found by using the complex conjugated value of the measured output reflection coefficient S_{22}, i.e. S_{22}^*, of the HFET [39]. It is well known that, under small-signal conditions, this approach will give the maximum gain and hence maximum output power for a given input power. In addition, this approach provides good starting values for parameters like PAE. The use of S_{22}^* as a starting value for Γ_L is the first step of a very fast search algorithm, developed by De Hek [38, 39], for finding the optimum load impedance (Z_L), which must be presented to the output of the HFET to achieve maximum power transfer between the source (HFET) and the load.

6.2.3 Active load-pull measurements

Active load-pull measurements, both CW and pulsed, have been performed to determine the maximum output power (P_{out}), the associated maximum power gain (G_p), and power added efficiency (PAE) of the AlGaN/GaN HFETs at fundamental frequencies (f_0) of 2 GHz and 4 GHz, which are the lower and upper frequency limits, respectively of the so-called S-band. It

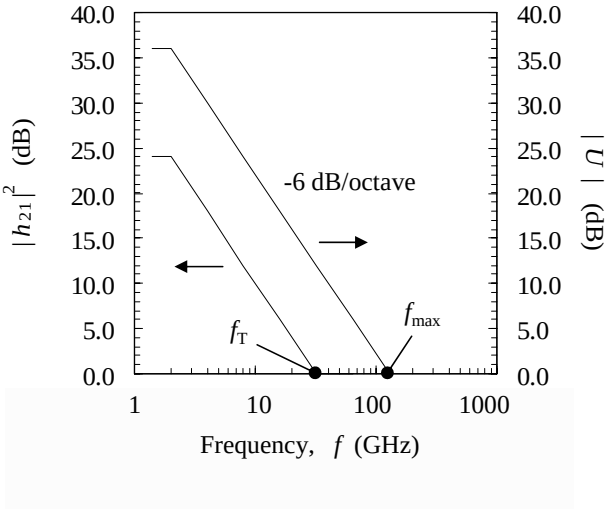

Figure 6.2: Theoretical determination of f_T and f_{max}.

has to be noted that no tuning of the higher order harmonics, i.e. $2f_0$, $3f_0$ etc., has been done. The measurements at 2 GHz and 4 GHz have been performed by Iouri Volokhine from Philips Research Eindhoven and Erwin Suijker from TNO Defence, Security and Safety, respectively. At TNO the large-signal measurement setup, which is schematically shown in Fig. 6.3 [39], has been used.

Figure 6.3 shows that this measurement setup consists of an HP8510C network analyzer, an HP85110A pulsed test-set, a traveling wave tube amplifier (TWTA), an active load, and of course the DUT. The input power required is generated by the TWTA, which can supply a maximum power of 3 W at the probe tip of this on-wafer measurement system [39]. For the load-pull measurements the output of the DUT is terminated with an active load, which is used instead of a passive load because it enables us to correct for the losses that occur between the load and the on-wafer measurement reference plane. This is essential as it must be possible to present large load reflection coefficients ($\Gamma_L > 0.8$) to the output of the DUT. To achieve such high values for Γ_L with a passive load, the loss between the load and the measurement reference plane must be less than 0.5 dB, which is difficult to achieve at microwave frequencies [39].

The choice of operating class, i.e. the position of the quiescent bias point (Q) in the $(I_D - V_{DS})$ plane, should be carefully selected as it influences the maximum values for P_{out}, G_p, and PAE of the AlGaN/GaN HFETs. Figure 6.4 shows the different positions of the quiescent bias points for operating classes A ($I_D = 0.5 \cdot I_{D,max}$), B ($V_{GS} = V_{pinch\text{-}off}$ hence ideally $I_D = 0$), and AB, respectively.

A measure of how much DC power (P_{DC}) is converted into microwave output power (P_{out}) is given by the drain efficiency (η_D), which is defined as [39]

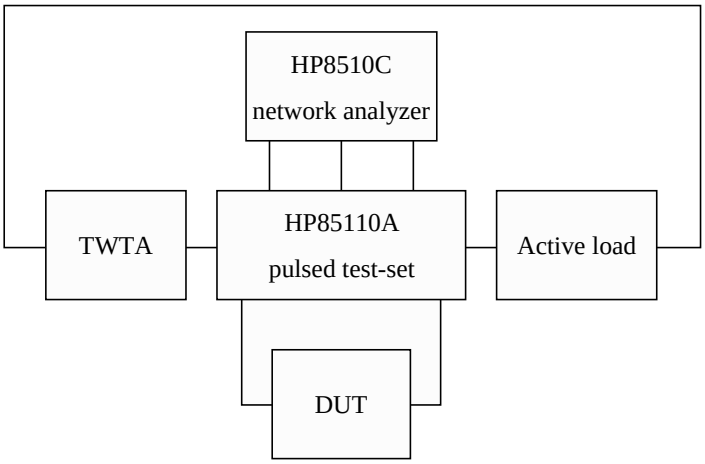

Figure 6.3: Schematic representation of the large-signal measurement setup used to perform the active load-pull measurements [39].

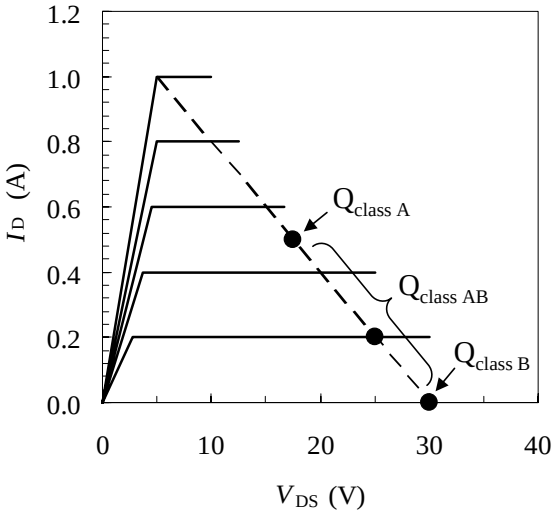

Figure 6.4: Different positions of the quiescent bias point (Q) in the $(I_D - V_{DS})$ plane for operating classes A, B, and AB, respectively.

$$\eta_D = \frac{P_{out}}{P_{DC}}. \tag{6.7}$$

However, the drain efficiency is the maximum achievable efficiency assuming an infinite G_p. Furthermore, it does not take into account the incident microwave power (P_{in}) that is provided to the device. Therefore, a more relevant measure for transistor efficiency is provided by PAE, because it takes into account the influence of both a finite power gain and the incident microwave power provided to the device. An expression for PAE is given by Eqn. 6.8 [139]

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left[1 - \frac{1}{G_p}\right]. \tag{6.8}$$

Equation 6.8 shows that PAE is directly related to the drain efficiency and that G_p should be as high as possible to obtain maximum PAE. In practice, a value for G_p less than 10 dB is unacceptable in terms of PAE reduction [39]. Especially for high-power HFETs, as high as possible values for PAE, i.e. > 50 %, are desirable to avoid excessive heat generation, which causes the drain current to drop as the mobility of the 2DEG electrons decreases with increasing temperature. Consequently, the output power of the devices also decreases.

Investigations by De Hek [39] have shown that P_{out} is almost equal for operating classes A, B, and AB. However, maximum PAE is obtained if the devices are biased in class AB. Hence, active load-pull measurements of our AlGaN/GaN HFETs on s.i. 4H-SiC substrates have been performed using bias conditions that correspond to an AB operating class.

6.3 Small periphery devices

The small periphery devices have been processed using the "*Submu*" mask set, which has been described in Sect. 3.2.1. The internal device dimensions using this mask set are: L_g = 0.25 μm, W_g = 80 μm, W_{gu} = 40 μm, L_{gg} = 60 μm, L_{gs} = 1 μm , L_{gd} = 2 μm ,and L_{ds} = 3.25 μm. For the sub-micrometer gate contacts we have used T-gates. The top of these gates is 0.75 μm wide and the extensions towards the source and drain contacts are both 0.25 μm long. The devices have been fabricated on 10 mm x 10 mm samples from wafers 1200, 1201, and 1203, whose layer stack and material properties are listed in Table 6.1.

Figure 6.5 shows continuous wave (CW) DC (I-V) measurement results for the devices processed on structures 1200, 1201, and 1203, respectively. The output characteristics ($I_D - V_{DS}$) show maximum drain current densities at V_{GS} = +2 V of 1.0 A/mm, 1.1 A/mm, and 1.2 A/mm for structures 1203, 1201, and 1200, respectively. These current densities are in perfect agreement with the values that can be calculated using the material properties listed in Table 6.1. In addition, it can be concluded that the very thin (1 - 2 nm) AlN layer between the AlGaN barrier and GaN buffer layers in structure 1200 indeed enhances both the density and mobility of the 2DEG electrons as this structure shows the highest drain current density. Furthermore, Fig. 6.5 shows that these structures have knee voltages (V_{knee}) as low as 4 V, which is excellent for achieving a large drain-source voltage swing provided that the breakdown voltage is high.

Table 6.1: Overview of the n.i.d. AlGaN/GaN epilayers on s.i. 4H-SiC substrates, grown by RU [146], which have been used for the fabrication of small periphery devices using the "*Submu*" mask set.

Wafer	Layer stack	d_{GaN} (μm)	d_{AlGaN} (nm)	Al (%)	R_{sheet} (Ω/sq.)	n_s (cm^{-2})	μ (cm^2/Vs)
1200	AlGaN/AlN/GaN	1.2	30	26	350	9.5 x 10^{12}	1875
1201	AlGaN/GaN	1.2	30	26	440	9.3 x 10^{12}	1515
1203	AlGaN/GaN:Fe	1.4	30	26	530	8.8 x 10^{12}	1352

A serious drawback of these devices is the fact that the gate and drain leakage current densities ($I_{G,leak}$ and $I_{D,leak}$) at V_{DS} = 26 V and V_{GS} = -6 V are very high. The value of $I_{G,leak}$ is 11 mA/mm for all structures, and the values of $I_{D,leak}$ are 120 mA/mm, 100 mA/mm, and 80 mA/mm for structures 1200, 1201, and 1203, respectively. It has to be noted that structure 1203, whose GaN buffer layer has been intentionally doped with iron (Fe), shows the smallest drain leakage current. Although the large drain leakage currents reduce the drain current swing, the microwave output power of these devices will be limited mostly by the breakdown voltage, which is strongly reduced because of the huge leakage currents of the 0.25 μm Schottky gates. The off-state breakdown voltages of the devices on all structures were approximately as low as 35 V.

From the transfer characteristics ($I_D - V_{GS}$) it can be seen that the devices on all structures are pinched-off at gate-source voltages (V_{GS}) of -6 V, and that the values of the maximum transconductance (g_m) are 220 mS/mm, 195 mS/mm, and 175 mS/mm for structures 1200, 1201, and 1203, respectively. Small-signal *S*-parameter measurements have been performed between 8 GHz and 12 GHz to determine values for S_{22}^*, which can be used as a starting value for Γ_L in the active load-pull measurements at 10 GHz. Figure 6.6 shows the extrapolation of the values for f_T and f_{max} from the magnitudes in decibels of the current gain and the unilateral power gain, $|h_{12}|^2$ and $|U|$ respectively, versus frequency. It can be seen that the values for f_T and f_{max} are 35 GHz and 75 GHz, respectively.

Pulsed DC (*I*-*V*) measurements, using the measurement setup whose equivalent circuit has been shown in Fig. 4.14, showed that gate lag has successfully been eliminated for all devices on structures 1200, 1201, and 1203. This has been confirmed by CW active load-pull measurements using low drain-source bias voltages and small input powers (P_{in}). Figure 6.7 shows single tone CW active load-pull results of a device on structure 1203, at 10 GHz with V_{DS} = 10 V, V_{GS} = -4 V, and a load reflection coefficient (Γ_L) of 0.7 + j 0.45. The maximum output power (P_{out}) of 17.4 dBm corresponds to 55.2 mW. Using the DC output characteristics of this structure, which are shown in Fig. 6.5-(3), we can calculate that the output power expected using the given bias conditions, which is (36.8 mA x 12 V) / 8 = 55.2 mW, exactly equals the output power that has been measured at 10 GHz.

Finally, we have performed single tone CW active load-pull measurements at 10 GHz

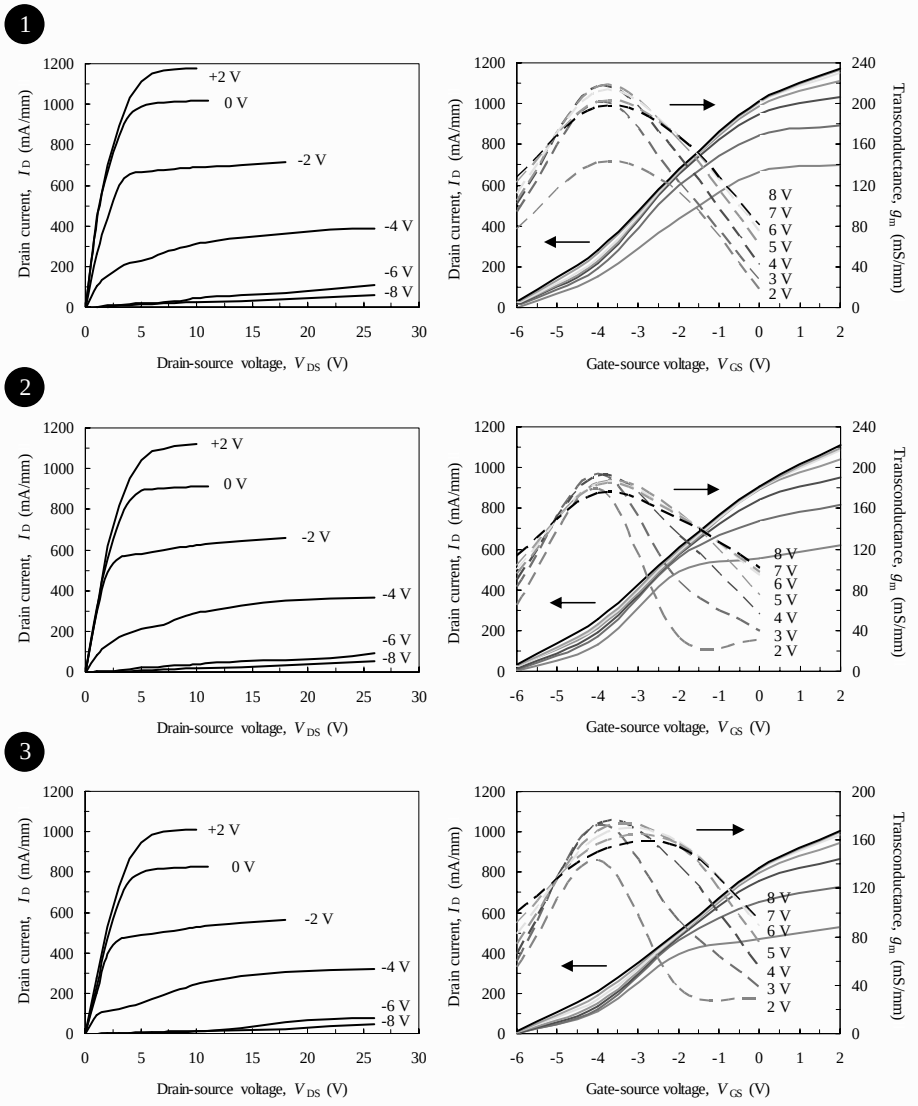

Figure 6.5: Continuous wave (CW) DC (*I-V*) measurement results of small (W_g = 80 μm) AlGaN/GaN HFETs with sub-micrometer T-gates (L_g = 0.25 μm) on structures 1200 (1), 1201 (2), and 1203 (3), respectively. The maximum DC power dissipated (P_{DC}) has been limited to 10 W.

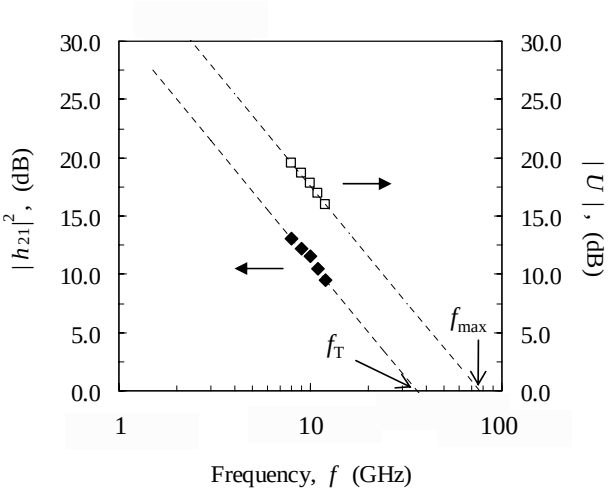

Figure 6.6: Extrapolation of the values for f_T and f_{max} for small (W_g = 80 μm) AlGaN/GaN HFETs with sub-micrometer T-gates (L_g = 0.25 μm) on structures 1200, 1201, and 1203, respectively. The small-signal *S*-parameter measurements have been performed between 8 GHz and 12 GHz at V_{DS} = 26 V and V_{GS} = -3.5 V.

using class AB bias conditions (V_{DS} = 26 V and V_{GS} = - 4 V) on all structures to determine values for the maximum output power (P_{out}), associated power gain (G_p), and PAE of the small gate periphery AlGaN/GaN HFETs. Figure 6.8 shows the results for structures 1200 (*left*), 1201 (*middle*), and 1203 (*right*), respectively. Using Γ_L = 0.75 + j 0.30, a maximum output power density (P_D) of 1.0 W/mm, power gain of 3.5 dB, and PAE of 4.3 % are obtained for structure 1200. For structure 1201 values for P_D, G_p, and PAE of 2.7 W/mm, 6 dB, and 13 %, respectively have been obtained using the same load reflection coefficient as for structure 1200. Finally, for structure 1203 using Γ_L = 0.80 + j 0.25, values for P_D, G_p, and PAE of 3.5 W/mm, 8 dB, and 26 %, respectively have been measured.

Considering the facts that the devices on all structures show dispersion free behavior at 10 GHz and have high maximum drain current densities of on average 1 A/mm, these load-pull results are very disappointing. The reason for these poor results obviously is the very low breakdown voltage caused by the excessively high gate and drain leakage currents. Comparison of the gate and drain leakage currents of the submicron T-gate devices and the fat gate (L_g = 2 μm) reference devices, which are also present on the Submu mask set as described in Sect. 3.2.1, shows that the huge leakage currents are not introduced by the SiN deposition process as the fat gate devices show values for $I_{G,leak}$ and $I_{D,leak}$ of 150 μA/mm and 400 μA/mm, respectively.

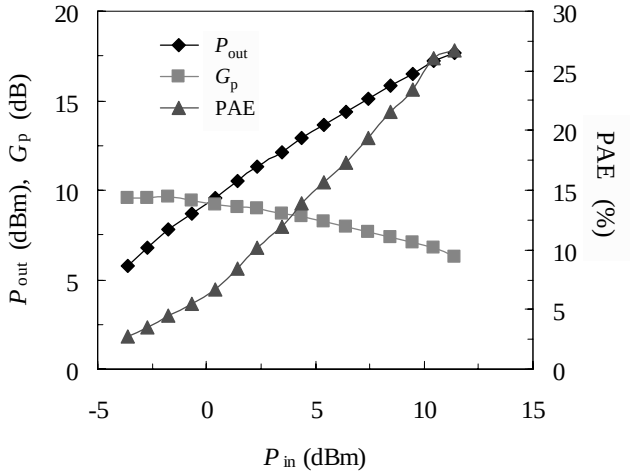

Figure 6.7: Single tone CW active load-pull results of a device on structure 1203, at 10 GHz with V_{DS} = 10 V, V_{GS} = -4 V, and a load reflection coefficient (Γ_L) of 0.7 + j 0.45.

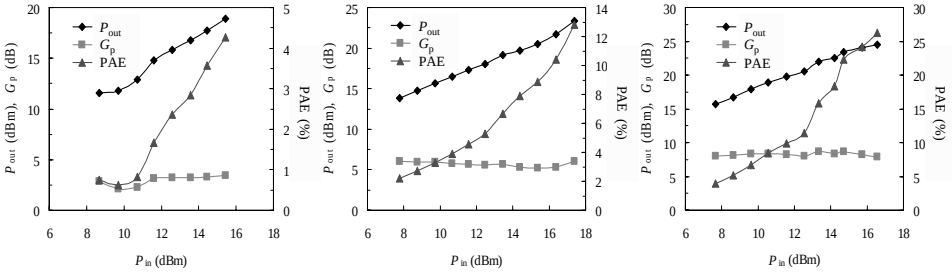

Figure 6.8: Single tone CW active load-pull results at 10 GHz using class AB bias conditions (V_{DS} = 26 V and V_{GS} = - 4 V) for devices on structures 1200 (*left*), 1201 (*middle*), and 1203 (*right*), respectively.

The reason for the high leakage currents most likely is the use of titanium (Ti) in the top part of the T-gates. The T-gate consists of a Ni/Au = 20/40 nm foot and a Ti/Au = 20/380 nm top. Titanium has been chosen to achieve a good mechanical stability of the top part of the gates due to the good adhesion between Ti and the SiN passivation film. However, as the temperatures in the channel underneath the Schottky gates can get as high as 240 °C [45], it is possible that Ti diffuses towards the AlGaN surface and causes the Schottky barrier height to be lowered. As a consequence, the gate leakage current increases and the breakdown voltage decreases. To circumvent this problem we have used Ni/Au for both the foot and top parts of the T- and FP-gates of the large gate periphery devices the results of which will be described in the next section.

6.4 Large periphery devices

The large periphery devices have been processed using the "*mmTor*" mask set, which has been described in Sect. 3.2.1. Devices with air bridges in both comb and fishbone layouts, which have total gate widths (W_g) of 0.25 mm, 0.5 mm, and 1.0 mm have been fabricated. The unit gate widths (W_{gu}) used are 62.5 μm, 100 μm, and 125 μm, respectively. For the fabrication of the sub-micrometer gate contacts we have used T-gates and gates with a field plate (FP) towards the drain contact using the original implementation, which has been shown in Fig. 4.8-(*left*), Sect. 4.3. The gate length (L_g), which defines the footprint of the T- and FP-gates, is 0.7 μm. The top of the T-gates is 1.2 μm wide and its extensions towards the source and drain contacts are 0.25 μm long. For the FP-gates we have used two FP lengths (L_{FP}) of 0.5 μm and 1.0 μm, which will be indicated as "FP0.5" and "FP1.0", respectively. According to the definition of the FP length, see Fig. 4.8, the T-gate can also be considered as a FP-gate. Hence, we actually have three FP lengths of 0.25 μm, 0.5 μm, and 1.0 μm. It has to be noted that the extension of the FP-gate towards the source contact is also 0.25 μm. The remaining internal dimensions for all large periphery devices are: L_{gs} = 1.2 μm, L_{gd} = 3.0 μm, L_{ds} = 4.9 μm, and L_{gg} = 50 μm, respectively. Table 6.2 shows an overview of the different device layouts and gate configurations, i.e. unit gate width (W_{gu}) and number of gate fingers (N_g), that have been fabricated. It has to be noted that each of these device types has been implemented with a T-, FP0.5, and FP1.0 gate.

All devices have been fabricated on a 15 mm x 15 mm sample from structure 1203 because this material showed the lowest gate and drain leakage currents as we have seen in Sect. 6.3. Figure 6.9 shows CW DC (*I*-*V*) results for 0.25 mm, and pulsed DC (*I*-*V*) results for 0.5 mm and 1.0 mm T-gate devices. The output characteristics $(I_D - V_{DS})$ show drain current densities of 1.0 A/mm and 840 mA/mm at V_{GS} = +2 V and V_{GS} = 0 V, respectively. These current densities are in perfect agreement with the values that can be calculated using the material properties listed in Table 6.1 and with the results for the small periphery devices shown in Sect. 6.3. From Fig. 6.9 we can see that the knee voltages (V_{knee}) for the output characteristics at V_{GS} = 0 V are 5 V. From the transfer characteristics $(I_D - V_{GS})$ it can be seen that all devices are pinched-off at V_{GS} = -6 V, and that the values of the maximum g_m range from 180 mS/mm to 190 mS/mm.

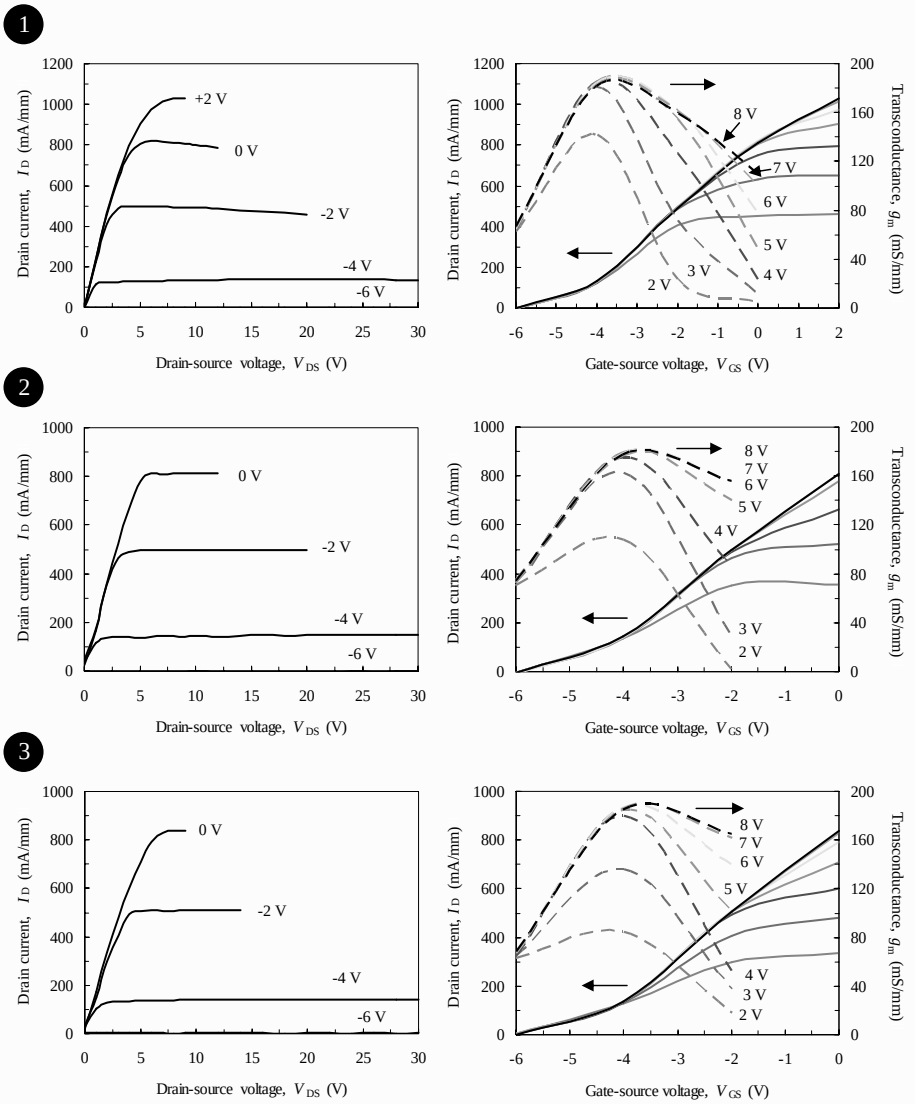

Figure 6.9: CW DC (*I-V*) results for 0.25 mm (1), and pulsed DC (*I-V*) results for 0.5 mm (2) and 1.0 mm (3) T-gate devices (L_g = 0.7 μm) with a comb layout on structure 1203. The maximum DC power dissipated (P_{DC}) has been limited to 10 W.

Table 6.2: Overview of the different device layouts and gate configurations used for the fabrication of the large periphery AlGaN/GaN HFETs.

Layout	W_{gu} (μm)	N_g	W_g (mm)
comb/fishbone	62.5	4	0.25
comb/fishbone	125	2	0.25
comb/fishbone	62.5	8	0.5
comb/fishbone	125	4	0.5
comb/fishbone	100	10	1.0
comb/fishbone	125	8	1.0

The off-state breakdown voltage ($V_{BD,off}$), which is defined as the drain-source voltage at which the gate leakage current reaches 1.0 mA/mm [33, 152] for a completely pinched-off device, has been determined for a 1.0 mm T-gate HFET with 10 gate fingers in a comb layout. Figure 6.10 shows that the device broke down at a drain-source voltage of 155 V, before the gate leakage current reached the 1.0 mA/mm level. This high breakdown voltage allows biasing of the devices at high drain-source voltages, e.g. V_{DS} = 60 V, to achieve a large voltage swing and a high microwave output power. Furthermore, from Fig. 6.10 it has to be concluded that the implementation of the top parts of the T- and FP-gates with Ni/Au instead of Ti/Au has solved the problems of the huge gate and drain leakage currents and the reduced breakdown voltage. For comparison with the small periphery devices, the values of $I_{G,leak}$ and $I_{D,leak}$ at V_{DS} = 30 V and V_{GS} = -7 V are 200 μA/mm and 2 mA/mm, respectively.

Small-signal *S*-parameter measurements have been performed between 2 GHz and 4 GHz to determine values for S_{22}^*, which can be used as a starting value for Γ_L in the active load-pull measurements that have been performed at 2 GHz and 4 GHz, which are the lower and upper frequency limits, respectively of the S-band. Figure 6.11 shows the extrapolation of the values for f_T (12 GHz) and f_{max} (34 GHz) for a T-gate device in a comb layout with a total gate periphery of 0.25 mm. It should be noted that the extrapolated value for f_{max} is an underestimate of its actual value as the slope of the measurement data (solid line) obviously is less than -6 dB/octave.

Figure 6.12 shows the values for f_T and f_{max} as a function of the gate length (L_g), the total gate width (W_g), V_{GS}, and the field plate length (L_{FP}), respectively. Figure 6.12-(1) shows values for f_T and f_{max} of devices with a total gate width of 80 μm and gate lengths of 0.25 μm, 0.7 μm, and 2.0 μm, respectively. Figure 6.12-(2) shows that f_T increases with W_g as it is directly proportional to the transconductance. However, f_{max} does not scale linearly with W_g because of the parasitic effect of the increasing gate-drain capacitance (C_{gd}). Figure 6.12-(3) shows the influence of V_{GS} on the values for f_T and f_{max}. From Fig. 6.12-(4) it can be concluded that the increasing value of C_{gd} starts influencing the values for f_T and f_{max} for

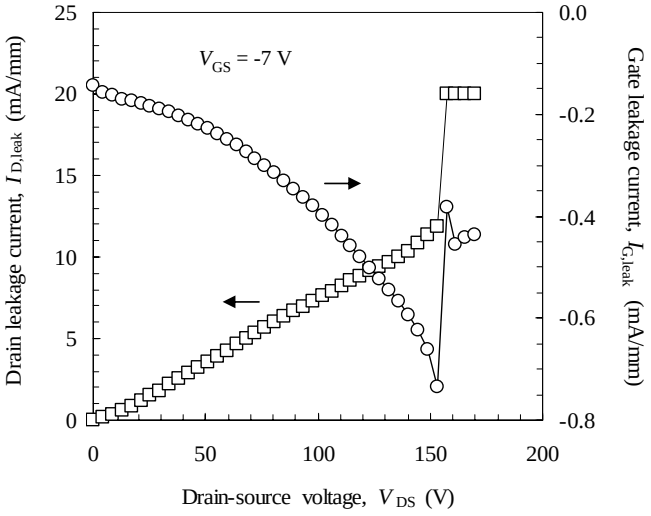

Figure 6.10: Measurement of the off-state breakdown voltage ($V_{BD,off}$) of a 1.0 mm T-gate HFET with 10 gate fingers arranged in a comb layout. The applied gate-source voltage is -7 V.

values of L_{FP} larger than 0.5 μm.

Figure 6.13 shows active load-pull results for 0.25 mm (CW) (*left*), 0.5 mm (pulsed) (*middle*), and 1.0 mm (pulsed) (*right*) T-gate devices with a comb layout. The single tone measurements have been performed at 2 GHz under class AB bias conditions (V_{DS} = 50 V, V_{GS} = -4.65 V). It has to be noted that in the case of pulsed measurements the values for PAE could not be determined due to limitations of the measurement setup. Using Γ_L = 0.67 + j 0.21, values of 34.5 dBm (2.8 W), 15 dB, and 54 % have been measured for P_{out}, G_p, and PAE, respectively of the 0.25 mm devices. For the 0.5 mm devices, values of 37.7 dBm (5.9 W) and 10.4 dB have been obtained for P_{out} and G_p using Γ_L = 0.35 + j 0.18. Finally, for the 1.0 mm devices values of 40.75 dBm (11.9 W) and 11 dB have been achieved for P_{out} and G_p using Γ_L = 0.06 + j 0.24. From these results it has to be concluded that the maximum output power excellently scales as a function of W_g.

Figure 6.14 shows the influence of the drain-source bias voltage on the values for P_{out} (*left*), G_p (*middle*), and PAE (*right*) at 2 GHz for a 0.25 mm T-gate device. In all cases the applied gate-source voltage is -4.65 V and the load reflection coefficients (Γ_L) used are 0.63 + j 0.27, 0.70 + j 0.29, and 0.67 + j 0.29 for V_{DS} = 30 V, 40 V, and 50 V, respectively. It can clearly be seen that P_{out} and G_p increase with drain-source voltage whereas PAE decreases.

Table 6.3 gives a summary of the active load-pull results at 2 GHz under class AB bias conditions for T- and FP-gate devices on structure 1203. It can clearly be seen that the output

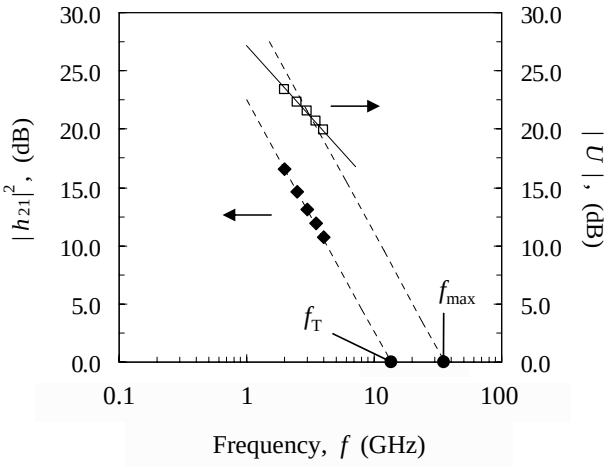

Figure 6.11: Extrapolation of the values for f_T and f_{max} for a T-gate device with a comb layout with a total gate periphery of 0.25 mm and a gate length of 0.7 μm. The small-signal *S*-parameter measurements have been performed between 2 GHz and 4 GHz at V_{DS} = 30 V and V_{GS} = -3.5 V.

power density (P_D) scales very well with W_g, i.e. within 5 %, for devices with the same type of gate and biased at the same drain-source voltage. Although L_{FP} does not seem to influence the value for P_D, it can be observed that G_p decreases for increasing L_{FP} because C_{gd} increases with L_{FP}. Furthermore, the values for G_p and PAE clearly show that devices fabricated on structure 1203 using the *mmTor* mask set and the process flow that is described in Appendix A, are very well suited for application in high-power amplifiers (HPA) at 2 GHz.

Figure 6.15 shows single tone pulsed active load-pull results for 0.25 mm (*left*), 0.5 mm (*middle*), and 1.0 mm (*right*) T-gate devices with a comb layout at 4 GHz under class AB bias conditions (V_{DS} = 40 V, V_{GS} = -4.0 V). Using Γ_L = 0.45 + j 0.45, values of 33.1 dBm (2.05 W), 14 dB, and 47 % have been measured for P_{out}, G_p, and PAE of the 0.25 mm devices. For the 0.5 mm devices, values of 36.1 dBm (4.07 W), 14.5 dB, and 52 % have been obtained for P_{out}, G_p, and PAE using Γ_L = 0.20 + j 0.50. Finally, for the 1.0 mm devices values of 37.7 dBm (5.9 W), 19.8 dB, and 46 % have been achieved for P_{out}, G_p, and PAE using Γ_L = 0.10 + j 0.40. It has to be noted that P_{out} of the 1.0 mm devices is less than can be expected from the scaling with W_g, which can clearly be observed for the 0.25 mm and 0.5 mm devices, because of the limited power available from the TWTA used. However, based on the scaling of P_{out} with W_g observed at 2 GHz and the scaling of the 0.25 mm and 0.5 mm devices at 4 GHz, it is reasonable to assume that the 1.0 mm devices can show an output power of 8 W at 4 GHz

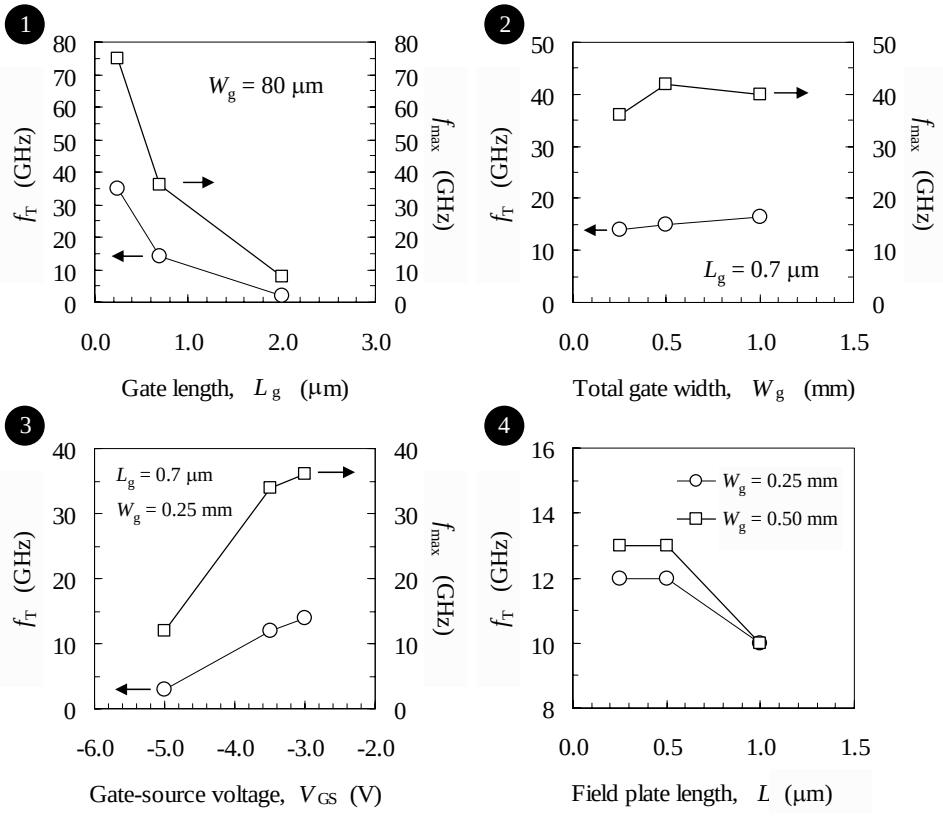

Figure 6.12: Values for f_T and f_{max} as a function of the gate length (L_g) (1), the total gate width (W_g) (2), the gate-source voltage (V_{GS}) (3), and the field plate length (L_{FP}) (4), respectively. Note that V_{DS} = 30 V for all cases and that V_{GS} = -3.5 V for (1), (2), and (4).

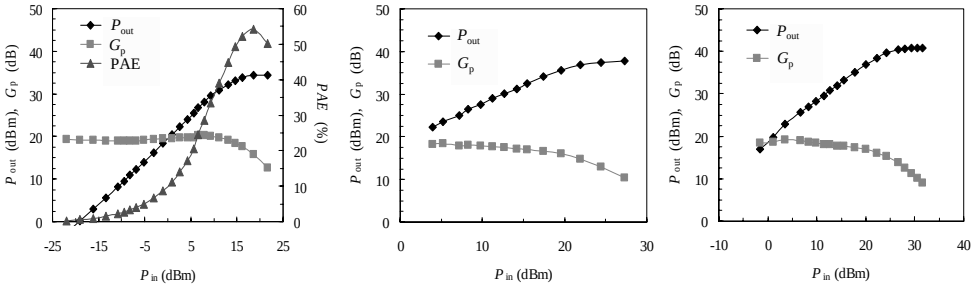

Figure 6.13: Single tone active load-pull results of 0.25 mm devices (CW, Γ_L = 0.67 + j 0.21) (*left*), 0.5 mm devices (pulsed, Γ_L = 0.35 + j 0.18) (*middle*), and 1.0 mm devices (pulsed, Γ_L = 0.06 + j 0.24) (*right*) at 2 GHz with V_{DS} = 50 V and V_{GS} = -4.65 V. All devices have T-gates that are arranged in a comb layout.

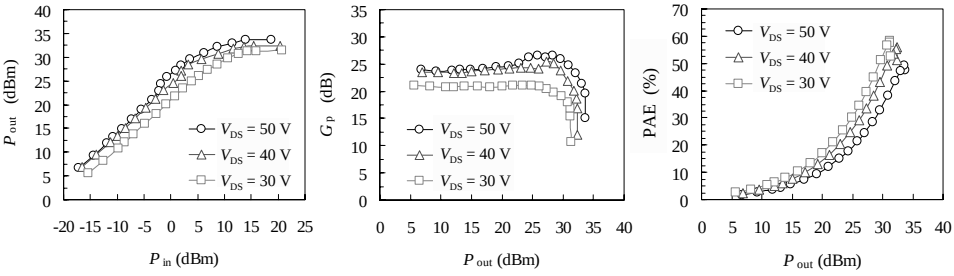

Figure 6.14: Influence of the drain-source bias voltage on the values for P_{out} (*left*), G_p (*middle*), and PAE (*right*) at 2 GHz for a 0.25 mm T-gate device. In all cases the applied gate-source voltage is -4.65 V and the load reflection coefficients (Γ_L) used are 0.63 + j 0.27, 0.70 + j 0.29, and 0.67 + j 0.29 for V_{DS} = 30 V, 40 V, and 50 V, respectively.

Table 6.3: Summary of single tone active load-pull results at 2 GHz under class AB bias conditions for T- and FP-gate devices on structure 1203. The total gate peripheries (W_g) of the devices are 0.25 mm, 0.5 mm, and 1.0 mm, respectively, and all gates are arranged in a comb layout.

W_g (mm)	type	W_{gu} x N_g	mode	V_{DS} (V)	V_{GS} (V)	P_{out} (W)	P_D (W/mm)	G_p (dB)	PAE (%)
0.25	T	62.5 x 4	CW	30	-4.65	1.6	6.4	> 20	60
0.25	T	62.5 x 4	CW	40	-4.65	2.2	8.8	> 20	60
0.25	T	62.5 x 4	CW	50	-4.65	2.8	11.2	> 20	54
0.25	FP0.5	62.5 x 4	CW	30	-4.65	1.5	6.0	> 17	57
0.25	FP0.5	62.5 x 4	CW	40	-4.65	2.0	8.0	> 17	57
0.25	FP0.5	62.5 x 4	CW	50	-4.65	2.7	10.8	> 17	-
0.25	FP1.0	62.5 x 4	CW	30	-4.65	1.6	6.4	15	70
0.25	FP1.0	62.5 x 4	CW	40	-4.65	2.4	9.6	> 15	-
0.25	FP1.0	62.5 x 4	CW	50	-4.65	3.0	12.0	> 17	-
0.5	T	125 x 4	pulsed	30	-4.65	3.2	6.4	> 16	-
0.5	T	125 x 4	pulsed	40	-4.65	4.6	9.2	> 17	-
0.5	T	125 x 4	pulsed	50	-4.65	5.9	11.8	> 20	-
0.5	T	62.5 x 8	pulsed	30	-4.65	3.1	6.2	> 15	-
0.5	T	62.5 x 8	pulsed	40	-4.65	4.3	8.6	> 17	-
0.5	T	62.5 x 8	pulsed	50	-4.65	5.7	11.4	> 18	-
1.0	T	125 x 8	pulsed	30	-4.65	6.5	6.5	> 15	-
1.0	T	125 x 8	pulsed	40	-4.65	9.3	9.3	> 18	-
1.0	T	125 x 8	pulsed	50	-4.65	11.9	11.9	> 19	-

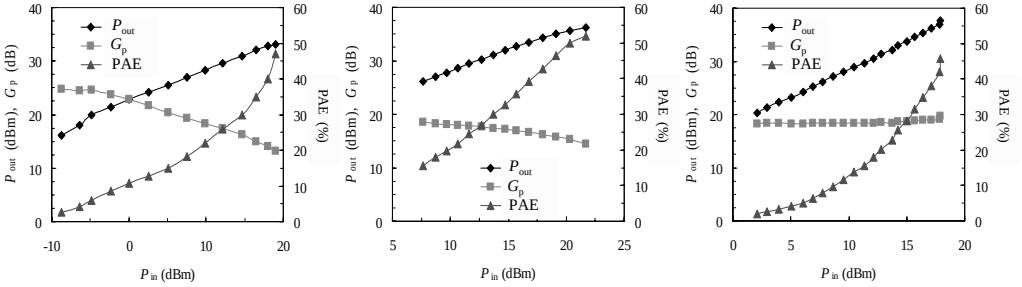

Figure 6.15: Single tone pulsed active load-pull results for 0.25 mm (*left*), 0.5 mm (*middle*), and 1.0 mm (*right*) T-gate devices with a comb layout at 4 GHz under class AB bias conditions (V_{DS} = 40 V, V_{GS} = -4.0 V).

using V_{DS} = 40 V and V_{GS} = -4.0 V.

Figure 6.16 shows the influence of the drain-source bias voltage on the values for P_{out} (*left*), G_p (*middle*), and PAE (*right*) at 4 GHz for a 0.25 mm T-gate device. In all cases the applied V_{GS} = -3.5 V and the values for Γ_L used are 0.32 + j 0.32, 0.45 + j 0.45, and 0.60 + j 0.40 for V_{DS} = 30 V, 40 V, and 50 V, respectively. It can be seen that P_{out} and G_p increase with drain-source voltage whereas PAE decreases, which is the same behavior as has been observed at 2 GHz.

Table 6.4 gives a summary of the active load-pull results at 4 GHz under class AB bias conditions for T- and FP-gate devices on structure 1203. It can clearly be seen that P_D of the 0.25 mm and 0.5 mm devices scales very well with W_g, i.e. within 5 %, for devices with the same type of gate and biased at the same drain-source voltage. Table 6.4 also shows that L_{FP} does not influence the value for P_D. However, it can be seen that G_p and PAE decrease for increasing L_{FP} because the value of C_{gd} increases with L_{FP}. Furthermore, the values for G_p and PAE clearly indicate that devices fabricated on structure 1203 using the *mmTor* mask set and the process flow that is described in Appendix A, are also very well suited for application in HPAs at 4 GHz.

Figure 6.17 shows a comparison of P_D versus W_g for T-gate devices at 2 GHz and 4 GHz for drain-source bias voltages of 30 V, 40 V, and 50 V, respectively. It has to be noted that the results have been obtained using different measurement setups, different load reflection coefficients and slightly different gate-source voltages, i.e. V_{GS} = -4.65 V at 2 GHz, and V_{GS} = -4.0 V at 4 GHz. Nevertheless, it can be concluded that the scaling of the output power with total gate width is excellent, especially at 2 GHz.

Figure 6.18 provides a comparison of the maximum values of P_D at S-band as a function of W_g of n.i.d. AlGaN/GaN HFETs on s.i. SiC substrates that we have shown in this section

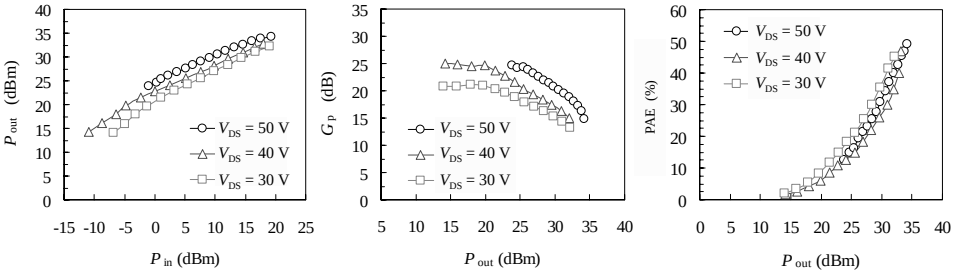

Figure 6.16: Influence of the drain-source bias voltage on the values for P_{out} (*left*), G_p (*middle*), and PAE (*right*) at 4 GHz for a 0.25 mm T-gate device. In all cases the applied gate-source voltage is -3.5 V and the load reflection coefficients (Γ_L) used are 0.32 + j 0.32, 0.45 + j 0.45, and 0.60 + j 0.40 for V_{DS} = 30 V, 40 V, and 50 V, respectively.

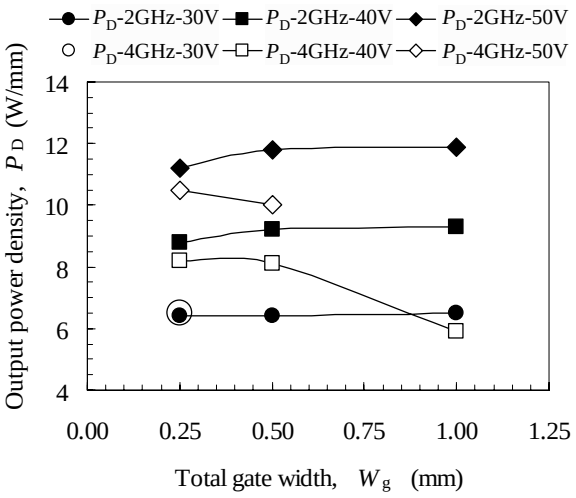

Figure 6.17: Comparison of P_D versus W_g for T-gate devices at 2 GHz and 4 GHz for V_{GS} = -4.65 V and V_{DS} is 30 V, 40 V, and 50 V, respectively.

Table 6.4: Summary of single tone active load-pull results at 4 GHz under class AB bias conditions for T- and FP-gate devices on structure 1203. The total gate peripheries (W_g) of the devices are 0.25 mm, 0.5 mm, and 1.0 mm, respectively, and all gates are arranged in a comb layout.

W_g (mm)	type	V_{DS} (V)	V_{GS} (V)	P_{out} (W)	P_D (W/mm)	G_p (dB)	PAE (%)
0.25	T	30	-3.5	1.64	6.5	14.0	42
0.25	T	40	-3.5	2.05	8.2	14.0	47
0.25	T	50	-3.5	2.63	10.5	12.9	49
0.25	FP0.5	30	-3.5	1.66	6.6	12.4	45
0.25	FP0.5	40	-3.5	2.09	8.4	12.8	40
0.25	FP0.5	50	-3.5	2.75	11.0	13.8	44
0.25	FP0.5	60	-3.5	2.95	11.8	14.0	44
0.25	FP1.0	50	-3.5	2.40	9.6	11.0	38
0.5	T	40	-4.0	4.07	8.1	14.5	52
0.5	T	50	-4.0	5.01	10.0	15.9	48
0.5	FP0.5	30	-4.0	3.27	6.5	10.0	59
0.5	FP0.5	40	-4.0	4.17	8.3	14.2	52
0.5	FP1.0	40	-4.0	3.39	6.8	13.6	44
1.0	T	40	-4.0	5.89	5.9	19.8	46
1.0	FP0.5	30	-4.0	4.61	4.6	14.0	43
1.0	FP0.5	40	-4.0	5.89	5.9	19.8	46
1.0	FP1.0	40	-4.0	4.27	4.3	17.3	36

(diamonds) and that have been reported in literature (squares) [8, 41, 73, 132, 140, 174]. It can be concluded that we have achieved state-of-the-art results with respect to the generation of large, i.e. 11.9 W, microwave output power for devices with large total gate widths, e.g. 1.0 mm.

6.5 Conclusions

In this chapter we have presented DC (*I*-*V*), small signal *S*-parameter and active load-pull results for both small (W_g = 80 μm) and large (W_g = 0.25 mm, 0.5 mm, and 1.0 mm) gate periphery n.i.d. AlGaN/GaN HFETs on s.i. 4H-SiC substrates. These devices are the product of a joint research effort between TU/e and RU and demonstrate the successful development

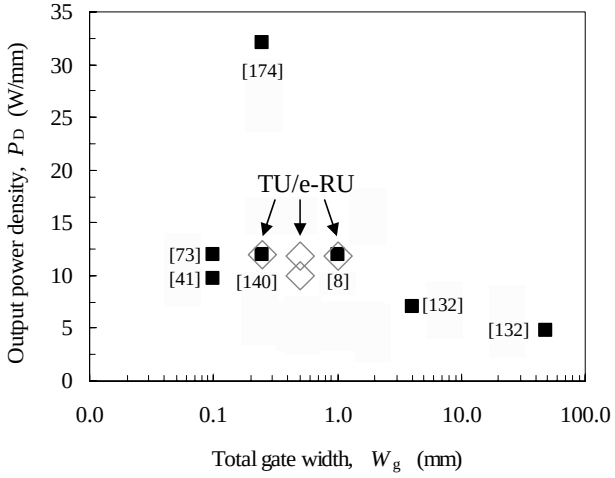

Figure 6.18: Comparison of the maximum output power densities (P_D) at S-band as a function of the total gate width (W_g) of n.i.d. AlGaN/GaN HFETs on s.i. SiC substrates that we have shown in this section (diamonds) and that have been reported in literature (squares) [8, 41, 73, 132, 140, 174].

and integration of both MOCVD epitaxial growth processes and device process technology.

DC (*I-V*) data of the presented HFETs show the potential for high-power performance of these devices as they enable both large drain current and drain-source voltage swings. The former can be realized because of the high maximum drain current densities, typically 1.0 A/mm, and the low values of $I_{G,leak}$ and $I_{D,leak}$ at pinch-off, which are typically 200 μA/mm and 2 mA/mm, respectively for large gate periphery devices. The large voltage swing is enabled by the low value of V_{knee}, typically 4 V - 6 V, and the high value of $V_{BD,off}$, typically larger than 150 V, which is enabled by the incorporation of T-gates with a field plate length of 0.25 μm. It has to be noted that the lowest values for $I_{G,leak}$ and $I_{D,leak}$ have been obtained on structure 1203, which incorporates an iron (Fe) compensation doped GaN buffer layer. Hence, only this structure has been used to fabricate large gate periphery devices whose microwave power performance as a function of W_g has been investigated.

For devices with an L_g of 0.7 μm the values for f_T and f_{max}, which have been extrapolated from small-signal *S*-parameter measurements, were 12 GHz and 34 GHz, respectively. These values indicate that devices with these gate lengths are suitable for S-band (2 GHz - 4 GHz) applications.

Single tone CW active load-pull results of small gate periphery (W_g = 80 μm) devices with a gate length of 0.25 μm at 10 GHz have demonstrated the successful elimination of gate lag from devices on all epitaxial layer structures used. This result proved the successful integration of the developed surface passivation modules, i.e. the plasma surface treatment (Sect. 4.4) and

SiN surface passivation (Chapter 5), into the process flow described in Appendix A.

Single tone CW and pulsed active load-pull results at 2 GHz under class AB bias conditions, e.g. V_{DS} = 50 V and V_{GS} = -4.65 V, have shown excellent values for P_{out} of large gate periphery AlGaN/GaN HFETs on the Fe-doped epistructure (1203), i.e. 11.9 W for a 1.0 mm T-gate device. Moreover, excellent scaling of P_{out} with W_g has been demonstrated for equally biased devices with the same type of gate, i.e. T- or FP-gate. Although L_{FP} does not seem to influence the value for P_D, it can be observed that G_p decreases for increasing L_{FP} because the value of C_{gd} increases with L_{FP}. In addition, the values for G_p, typically 15 dB, and PAE, typically larger than 54 %, clearly show that devices fabricated on structure 1203 using the *mmTor* mask set and the process flow described in Appendix A, are very well suited for application in HPAs. Single tone pulsed active load-pull measurements at 4 GHz under class AB bias conditions, e.g. V_{DS} = 50 V and V_{GS} = -4 V, have shown similar results, which has clearly been shown in Fig. 6.17. We want to mention that the results of comparable measurements on these devices performed by TU/e, TNO, and Philips were in excellent agreement. In addition, as the devices have been measured over a period of 5 months, it has clearly been shown that their behavior is stable over time.

Comparison of the maximum output power densities at S-band as a function of total gate width of n.i.d. AlGaN/GaN HFETs on s.i. SiC substrates that we have shown in Sect. 6.4 and that have been reported in literature, clearly shows that we have achieved state-of-the-art results with respect to the generation of large, i.e. 11.9 W, microwave output power for devices with large total gate widths, e.g. 1.0 mm. Furthermore, it can be concluded that GaN:Fe buffer layers are perfectly suitable for high-power applications at S-band.

Chapter 7

Conclusions and recommendations

This chapter provides a review of the main conclusions that can be drawn from the work described in this thesis and provides recommendations for future research.

7.1 Main conclusions

The objectives of the research described in this thesis were to develop the technology required to grow state-of-the-art AlGaN/GaN epilayers on sapphire and s.i. SiC substrates by MOCVD and to fabricate microwave high-power HFETs on these epitaxial films. The large periphery HFETs consisting of n.i.d. AlGaN/GaN:Fe epilayers on s.i. SiC substrates have sub-micrometer T- or FP-gates with a gate length (L_g) of 0.7 μm and total gate widths (W_g) of 0.25 mm, 0.5 mm, and 1.0 mm, respectively. The 1.0 mm devices are capable of producing a maximum microwave output power (P_{out}) of 11.9 W at S-band (2 GHz - 4 GHz) using class AB bias conditions of V_{DS} = 50 V and V_{GS} = -4.65 V. Moreover, excellent scaling of P_{out} with W_g has been demonstrated as has been shown in Fig. 6.17. In addition, the associated power gain (G_p) ranges between 15 dB and 20 dB, and for the power added efficiency (*PAE*) values from 54 % up to 70 % have been obtained.

Figure 6.18 provided a comparison of the maximum output power densities (P_D) at S-band as a function of the total gate width (W_g) of n.i.d. AlGaN/GaN HFETs on s.i. SiC substrates that we have shown in Sect. 6.4 (diamonds) and that have been reported in literature (squares) [8, 41, 73, 132, 140, 174]. It is clear that we have achieved state-of-the-art results with respect to the generation of large, i.e. 11.9 W, microwave output power for devices with large total gate widths, e.g. 1.0 mm.

The device results presented, illustrate both the successful development of the MOCVD growth process, and the successful integration of process modules such as ohmic and Schottky contact technology, device isolation, electron beam lithography, surface passivation, and

air bridge technology, into a process flow that enables the fabrication of state-of-the-art large periphery n.i.d. AlGaN/GaN:Fe HFETs on s.i. SiC substrates. These devices are perfectly suitable for application in e.g. high-power amplifiers at S-band (2 GHz - 4 GHz).

With respect to the development of the MOCVD growth process (Chapter 3), which is required for the fabrication of state-of-the-art n.i.d. AlGaN/GaN epilayers, the following main conclusions can be drawn:

- Optimization of the growth process of the GaN buffer layer on sapphire substrates has shown that buffer layers with resistivities exceeding 10^4 Ωcm can be achieved in a controlled and reproducible manner if nitrogen is used as carrier gas during the deposition of the low-temperature GaN nucleation layer [50].

- GaN buffer layers on commercially available 2 inch s.i. 4H-SiC substrates with resistivities also exceeding 10^4 Ωcm can be obtained by both compensation doping with iron (Fe) and non-intentionally doping as has been done on sapphire substrates [146].

- The residual free carrier concentration of the GaN buffer layers was low, typically 3.5 x 10^{13} cm^{-3}, which resulted in very low leakage currents, typically 1 x 10^{-7} A. The latter is required to enable a high breakdown voltage (V_{BD}) which is one of the necessary conditions to realize high output power.

- Non-intentionally doped AlGaN barrier layers with a thickness of 30 nm, an aluminum content between 25% and 30%, and a very smooth surface morphology have been grown on s.i. 4H-SiC substrates. The sheet carrier density and Hall mobility of the 2DEG electrons varied between 8.8 x 10^{12} cm^{-2} - 9.3 x 10^{12} cm^{-2}, and 1300 cm^2/Vs - 1500 cm^2/Vs at room temperature, respectively. By inserting a very thin, typically 1 nm, AlN layer between the GaN buffer layer and AlGaN barrier layer these values have been increased to 9.5 x 10^{12} cm^{-2} - 1.0 x 10^{13} cm^{-2}, and 1700 cm^2/Vs - 1900 cm^2/Vs.

Regarding device layout (Chapter 3) we make the following remarks:

- The “Inverse Mesa” and “Submu” mask sets were very useful to fabricate small devices with a total gate width (W_g) of 80 μm and gate lengths (L_g) of 0.25 μm and 2 μm, respectively. These devices have been used in short loop experiments, which are performed for process development and optimization.

- The “mmTor” mask set enables the fabrication of large devices with sub-micrometer gate lengths and total gate widths ranging from 0.25 mm to 6.4 mm. These devices can be used at frequencies ranging from S-band (2 GHz - 4 GHz) to X-band (8 GHz - 12.4 GHz) have shown to achieve microwave high-power operation. We have discussed key aspects that need to be considered in the design of these devices, i.e. gate length, total gate width, unit gate width, gate-to-gate pitch, layout of the gate fingers, gate-source spacing, gate-drain spacing, and the pitch of the ground-signal-ground probe pads.

- Finally, we presented schematic overviews of the main steps in the process flows of the Inverse Mesa and mmTor mask sets, respectively. Detailed descriptions of the process flows for all mask sets can be found in Appendix A.

With respect to the individual process modules (Chapter 4), which have been integrated into the process flow that enables the fabrication of state-of-the-art large periphery n.i.d. AlGaN/GaN HFETs on s.i. SiC substrates, the following conclusions can be drawn:

- The line definition and surface morphology of the Ti/Al/Ni/Au (30/180/40/100 nm) ohmic contacts has significantly been improved using an Au/Al ratio of 0.55, and a ramp-up time of the RTA process of 45 seconds. The contact resistance on n.i.d. AlGaN (25 nm) / GaN (2 μm) heterostructures using this metallization scheme is as low as 0.15 Ωmm.

- We have pointed out that our choice to investigate Ni/Au Schottky contacts on strained AlGaN/GaN heterostructures instead of relaxed bulk AlGaN layers proves to be the approach to follow despite difficulties with respect to characterization. Our studies towards the optimization of these contacts have focused on the development of a suitable pre-metallization surface clean to achieve lowest reverse current and highest breakdown voltage. The most suitable surface clean for high-power applications consisting of a wet etch using ammonia (NH_4OH) for 15 minutes cannot be used in the process flow of the large periphery HFETs (mmTor) as it causes severe adhesion problems with the copolymer that is used to define the footprint of the Schottky gates. However, as the AlGaN surface is cleaned using an ammonia dip for 1 minute before passivation with silicon nitride, the surface clean just before Ni/Au evaporation has been omitted. Reverse (*I-V*) measurements of Schottky test structures showed leakage currents of 400 μA/mm and breakdown voltages around 150 V. These results indicate that our Ni/Au Schottky contacts are perfectly suitable for application in high-power HFETs.

- For device isolation using a dry etch, we have shown the development of a low power ICP process using a chlorine-hydrogen (Cl_2/H_2) chemistry that enables the use of photoresist as masking material to obtain mesa structures with sloped side walls. This process etches AlGaN/GaN unselectively at a rate of 110 nm/min and yields a very smooth surface morphology of the etched GaN buffer layer. Furthermore, we have discussed the importance of creating a process window for the etch process to assure a constant etch rate and reproducible etch results from run to run.

- A two-step electron beam lithography (EBL) process has been developed to fabricate T-shaped and field-plated (FP) gates with sub-micrometer footprints, which define the actual gate length. The top parts of these gates are parallel to the semiconductor surface, which is completely covered with SiN up to the footprint of the gate. Additional advantages of this process are the excellent line width control of the footprint and the protection of the AlGaN layer due to the deposition of the SiN passivation layer early in the fabrication process.

- We have investigated the efficiency of gate lag reduction and the uniformity of microwave device performance using PECVD silicon nitride (SiN) on both n.i.d. and doped AlGaN/GaN heterostructures. Our experiments confirm that passivation with SiN indeed achieves increased drain current swing because of reduced gate lag but the observed uniformity of the microwave device performance showed to be very poor. We have shown that the application of a low power dry etch using Ar (10 sccm, 40 mTorr, 30 W, 30", DC bias = -86 V, 20 ^{o}C) just before the RTA step (800 ^{o}C, 2 minutes, N_2 ambient) of the Ti/Al/Ni/Au ohmic contacts is the key processing step leading to strongly minimized gat lag and the significantly improved uniformity of microwave device performance upon surface passivation with SiN.

- We have developed a process that uses e-beam evaporation to fabricate air bridges with a 1.5 μm thick Au layer. To improve the stability and reliability of the air bridges a lens-shaped support resist has been used to avoid the posts of the bridges to be too steep which causes easy breaking. Furthermore, we have introduced slits that split up wide air bridges into several narrower parts in parallel because it is difficult to efficiently remove the thick support resist underneath very wide air bridges without destroying them.

- After passivation of the AlGaN surface using a PECVD SiN film a huge increase in drain and gate leakage currents has been observed. Especially the latter is detrimental for the high-power performance of the devices as it severely reduces the maximum breakdown voltage. As we assumed that the cause for the increased gate leakage current was related to the SiN-AlGaN interface, we have investigated if changing the composition of the PECVD SiN film or preparation of the AlGaN barrier layer before SiN deposition, or both, results in decreased leakage currents after SiN deposition (Chapter 5). It should be noted that the surface passivation capability should remain equal to that of the standard film (SiH_4 = 16.6 sccm, N_2 = 980 sccm, NH_3 = 13.4 sccm, P_{RF} = 20 W, p = 650 mTorr, T = 300 ^{o}C) deposited using an Oxford Plasmalab 100 PECVD system. From our investigations it can be concluded that proper preparation of the AlGaN surface directly before SiN deposition is very important to achieve leakage current levels (typically 400 μA/mm) that enable high-power device operation. Passivation of the AlGaN barrier layer of the large periphery microwave high-power AlGaN/GaN HFETs has been done using an NH_4OH dip for 1 minute, which is immediately followed by the deposition of 100 nm SiN according to the PECVD process settings of the standard SiN film.

7.2 Recommendations for future research

The research described in this thesis was concerned with the developments of both MOCVD epitaxial growth processes and device technologies for the fabrication of n.i.d. AlGaN/GaN HFETs on c-plane sapphire and s.i. 4H-SiC substrates. Future research topics concerning material growth, process technology, and device characterization will be discussed.

Material growth

Physical models should be developed to optimize material growth and enable the evaluation of new device structures by simulations. Furthermore, MOCVD growth of AlGaN/GaN epilayers on high-resistivity, e.g. 10^4 Ωcm, Si (111) substrates should be developed as this substrate provides the best chances for successful commercialization of GaN-based electronics [73]. Also free-standing GaN substrates grown by hydride vapor phase epitaxy (HVPE) are very interesting as this material can be used as starting material to achieve MOCVD grown AlGaN/GaN epilayers with reduced defect densities, i.e. lower than 10^8 cm^{-2}.

Device concepts

Another interesting topic that should be considered is the investigation of new device concepts such as an indium gallium nitride (InGaN) channel structure sandwiched between two GaN barrier layers and the double barrier AlGaN/GaN structure [129]. Both concepts aim at the elimination of polarization related surface charge instabilities by burying these surface charges inside the heterostructure. The latter allows charge accumulation due to the polarization field to be substituted by ionized doping. This technique of screening the polarization field by doping in fact substitutes mobile polarization induced interface charges by immobile donors or acceptors [16, 129].

Process technology

To improve device performance and reliability, we recommend the development of drain and source contacts that show ohmic behavior either as deposited or after rapid thermal annealing at low temperatures, i.e. $T < 660$ °C, which is the melting point of aluminum.

To increase the operating frequency of the devices it is obvious that L_g has to be decreased. As a result, recessing of the gate contact becomes important to satisfy the high-aspect-ratio design concept discussed in Sect. 3.1.1. A gate recess also leads to higher values of V_{BD} as the highest electric field strength at the drain side of the gate is reduced. Hence, the output power is increased [133].

The influence of the implementation of the FP-gate on device performance should be investigated into more detail. The original implementation after Zhang *et al.* [181] suffers from increased values of C_{gd} which reduces power gain and PAE as described in Sect. 4.3. Reduction of C_{gd} can be achieved using the implementation first introduced by Chini *et al.* [30] in which the FP is separated from the gate finger by a dielectric film and connected to the gate finger only by the gate bus outside the intrinsic device. A different field plate configuration, which could be considered if frequency does not have the highest priority, is the so-called source-terminated field plate (SFP) which is reported to achieve improved output power, linearity and PAE compared to gate-terminated field plates [31]. The SFP reduces current crowding at the source contacts. As a result, it decreases oxidation and possible morphology degradation of the AlGaN barrier layer, which give rise to surface charge instabilities that contribute to drain current and consequently microwave output power reduction.

Device characterization

We have used device characterization to investigate the influence of process technology on device performance. However, accurate measurements should be done to enable the development of small- and large-signal transistor models that can be used to simulate device performance as a function of device layout. In addition, thermal simulations should be available to optimize device layout. Finally, reliability testing of GaN-based devices is an important topic to be addressed with respect to commercialization of this technology.

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Appendix A

Process flows for GaN-based HFETs

We have developed process flows for GaN-based HFETs that can be used for the fabrication on sapphire and s.i. SiC substrates. This appendix starts with descriptions of process steps that form the building blocks for the process flows of both small and large gate periphery devices. Section A.2 describes the process settings for resists used for optical contact lithography and polymers used for electron beam lithography. Section A.3 provides process settings for different plasma processes used. Finally, sections A.3 to A.6 provide the complete process flows for small and large periphery devices, respectively.

A.1 Building blocks

A.1.1 Cleaning

Cleaning	**Comments**
Spray with acetone (CH_3COCH_3)	- in quartz basket with teflon insert - above waste container
Spray with iso-propyl alcohol ($CH_3CHOHCH_3$)	- in quartz basket with teflon insert - above waste container
Blow dry with nitrogen (N_2)	

A.1.2 Rinsing

Rinsing	**Comments**
Rinse in ultra pure water (UPW)	- for *positive* resists time > 1 minute - for *negative* resists time > 3 minutes - for both resist types resistance water > 5MΩ - place sample in quartz basket with teflon insert
Blow dry with nitrogen (N_2)	

A.1.3 Exposure

Exposure	Comments
UV 300	- Karl Süss MJB3 mask aligner - λ = 300 nm - optical power density: 3.4 mW/cm^2 (range 20)
UV 400	- Karl Süss MJB3 mask aligner - λ = 400 nm - optical power density: 21.7 mW/cm^2 (range 200)
UV 430	- Karl Süss MA6 mask aligner - λ = 430 nm - optical power density: 7.5 mW/cm^2 (range 20) - vacuum mode

A.1.4 Metal lift-off

Lift-off	Comments
Soak in aceton	time > 3 minutes
Spray with acetone	- in quartz basket with teflon insert - above waste container
Ultrasonically stirring in acetone	- time > 1 minute - place quartz basket with teflon holder on bottom of beaker glass
Cleaning	see A.1.1

A.1.5 Oxygen plasmas

Oxygen plasmas	T (^{o}C)	time (m:s)	Comments
Descum	20	0:30	- Tepla - process power 50 W - Faraday cage to prevent surface damage due to ion bombardment
Stripping	20	5:00	- Tepla - process power 150 W - Faraday cage
Ashing	20	15:00	- Tepla - process power 300 W - Faraday cage

A.1.6 Resist removal after plasma etching

Resist removal	**T** (^{o}C)	**time (m:s)**	**Comments**
Stripping	20	5:00	see A.1.5
Spray with acetone			- in quartz basket with teflon insert - above waste container
Ultrasonically stirring in acetone		2:00	place quartz basket with teflon holder on bottom of beaker glass
Cleaning			see A.1.1

A.2 Resists and polymers

A.2.1 Microchemicals AZ5214e

AZ5214e	T (^{o}C)	time (m:s)	Comments
			- optical lithography - positive radiation sensitive
Spinning		0:30	- open air spinner - 5000 rpm
Soft bake	95	5:00	hotplate
Flood exposure		0:00.8	- UV 300, see A.1.3 - required for lift-off profile
Bake	105	5:00	hotplate
Mask exposure		0:30	UV 300, see A.1.3
Develop		1:30	AZ developer : UPW = 1 : 1 (volume)
Rinsing			see A.1.2

A.2.2 Microchemicals AZ4533

AZ4533	T (^{o}C)	time (m:s)	Comments
			- optical lithography - positive radiation sensitive
Spinning		0:30	- open air spinner - 5000 rpm
Soft bake	95	20:00	hotplate
Mask exposure: UV 400		0:15	UV 400, see A.1.3
Mask exposure: UV 430		0:32	UV 430, see A.1.3
Develop		1:20	AZ developer : UPW = 1 : 1 (volume)
Rinsing			see A.1.2
Hard bake	105	30:00	hotplate

A.2.3 Micro resist ma-N415

ma-N415	**T** (^{o}C)	**time (m:s)**	**Comments**
			- optical lithography - negative radiation sensitive
Spinning		0:30	- CONVAC open air spinner - 5000 rpm
Bake	95	5:00	hotplate
Mask exposure		0:24	UV 300, see A.1.3
Develop		1:50	ma-D332S (concentrated)
Rinsing			see A.1.2

A.2.4 Micro resist ma-N440

ma-N440	**T** (^{o}C)	**time (m:s)**	**Comments**
			- optical lithography - negative radiation sensitive
Spinning		0:30	- CONVAC open air spinner - 3000 rpm
Bake	95	5:00	hotplate
Mask exposure		8:20	- UV 430, see A.1.3 - Vacuum mode - 5 x 100 seconds
Develop		1:30	ma-D332S (concentrated)
Rinsing			see A.1.2

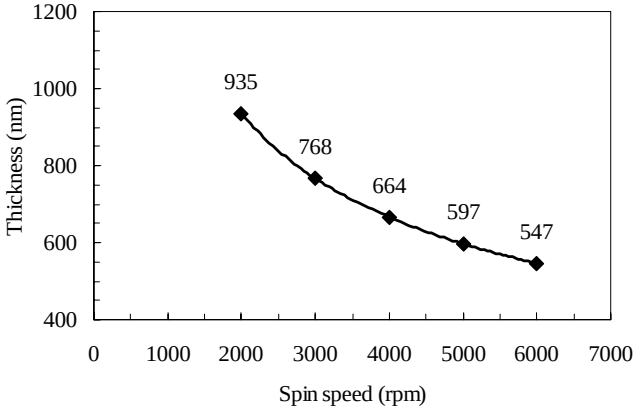

Figure 7.1: Spin curve copolymer for MMA(8.5)MAA EL13 using CONVAC open air spinner.

A.2.5 Microchemicals MMA(8.5)MAA EL13

MMA(8.5)MAA EL 13	T (^oC)	time (m:s)	Comments
			- electron beam lithography - Methyl Meth Acrylate - Meth Acrylate Acid (MMA-MAA) - Ethyl Lactate (EL) - positive radiation sensitive
Spinning foot		1:15	- CONVAC open air spinner - 5000 rpm
Spinning top		1:15	- CONVAC open air spinner - 2500 rpm
Bake	175	95:00	- HERAEUS hot air oven in yellow room - samples in glass cups with glass cover
Electron beam exposure			- RAITH 150 - see Appendix B
Develop		1:30	methyl isobutyl ketone (MIBK) : iso-propyl alcohol (IPA) = 1 : 3 (volume)
Stop		1:00	VLSI IPA
Blow dry with nitrogen (N_2)			no rinsing in UPW

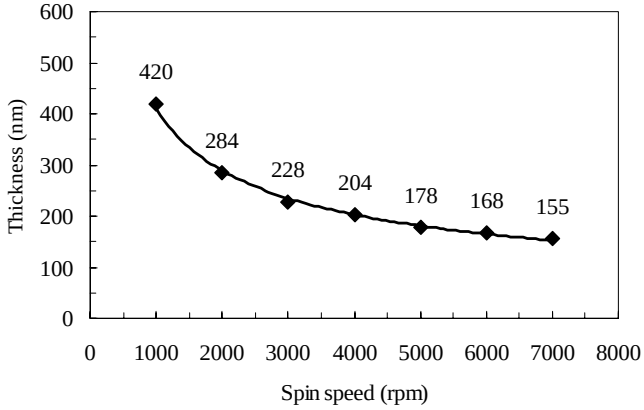

Figure 7.2: Spin curve for PMMA 950K A4 using CONVAC open air spinner.

A.2.6 Microchemicals PMMA 950K A4

PMMA 950K A4	**T** (^oC)	**time (m:s)**	**Comments**
			- electron beam lithography - Poly Methyl Meth Acrylat (PMMA) - positive radiation sensitive
Spinning SPL		1:00	- CONVAC open air spinner - 5000 rpm - single pixel lines
Bake	175	95:00	- HERAEUS hot air oven in yellow room - samples in glass cups with glass cover
Electron beam exposure			- RAITH 150 - see Appendix B
Develop		1:30	methyl isobutyl ketone (MIBK): iso-propyl alcohol (IPA) = 1 : 3 (volume)
Stop		1:00	VLSI IPA
Blow dry with nitrogen (N_2)			no rinsing in UPW

A.3 Plasma processes

A.3.1 Reactive ion etching (RIE): dispersion

RIE: dispersion	T (^{o}C)	time (m:s)	Comments
			Oxford instruments Plasmalab system 100
Chamber and quartz plate cleaning	20	30:00	- O_2 = 20 sccm, Ar = 10 sccm - P_{RF} = 100 W, DC_{bias} = -141 V - p = 100 mmTor - heater-chiller on, cooling on
Chamber and quartz plate conditioning	20	10:00	- no sample - 3B mode, C_1 = 86, C_2 = 21 - Ar = 10 sccm - P_{RF} = 30 W, DC_{bias} = -86 V - p = 40 mmTor - heater-chiller on, cooling on
Dummy run	20	0:30	- one dummy sample - 1F mode, C_1 = 86, C_2 = 21 - t_{set} = 33 seconds - Ar = 10 sccm - P_{RF} = 30 W, DC_{bias} = -86 V - p = 40 mmTor - heater-chiller on, cooling on
Dispersion etch	20	0:30	- one sample at a time - 1F mode, C_1 = 86, C_2 = 21 - t_{set} = 33 seconds - Ar = 10 sccm - P_{RF} = 30 W, DC_{bias} = -86 V - p = 40 mmTor - heater-chiller on, cooling on

A.3.2 RIE: open silicon nitride passivation layer

RIE: SF_6	**T (^oC)**	**time (m:s)**	**Comments**
			Oxford instruments Plasmalab system 100
Chamber and quartz plate cleaning	20	30:00	- O_2 = 20 sccm, Ar = 10 sccm - P_{RF} = 100 W, DC_{bias} = -141 V - p = 100 mmTor - heater-chiller on, cooling on
Chamber conditioning	20	10:00	- no sample - 3B mode C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on
Dummy run	20	3:00	- one dummy sample - 1F mode, C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on - determined etch rate SiN: 50 - 60 nm/min
Open SiN on ohmic contacts	20	4:00	- one sample at a time - 1F mode, C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on - considerably over-etched to avoid SiN remaining between probe pad connections and ohmic contacts
Open SiN underneath foot T/FP gate	20	2:50	- one sample at a time - 1F mode, C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on - avoid over-etching too much because of damage to AlGaN underneath gate (leakage currents)

A.3.3 Inductively coupled plasma etching (ICP): mesa

ICP: mesa	T (^{o}C)	time (m:s)	Comments
			Oxford instruments Plasmalab system 100
Chamber cleaning	40	60:00	- C_1 = 4.06, C_2 = 4.92 - O_2 = 40 sccm - P_{ICP} = 1500 W, P_{RF} = 150 W - DC_{bias} = -260 V - p = 20 mmTor - LN2 cooling on
Chamber conditioning	40	105:00	- with Si carrier wafer, no sample - cyclic etching process, $t_{etch\ cycle}$ = 5 minutes - C_1 = 6.85, C_2 = 4.06 - Cl_2 = 30 sccm, H_2 = 10 sccm - P_{ICP} = 200 W, P_{RF} = 50 W - DC_{bias} = -210 V - p = 10 mmTor, p_{He} = 16 Torr (8 sccm) - LN2 cooling on
Dummy run	40	2:00	- one dummy sample - C_1 = 6.85, C_2 = 4.06 - Cl_2 = 30 sccm, H_2 = 10 sccm - P_{ICP} = 200 W, P_{RF} = 50 W - DC_{bias} = -210 V - p = 10 mmTor, p_{He} = 16 Torr (8 sccm) - LN2 cooling on - determined etch rate AlGaN/GaN: 110 nm/min
Mesa etch	40	1:35	- one sample at a time - C_1 = 6.85, C_2 = 4.06 - Cl_2 = 30 sccm, H_2 = 10 sccm - P_{ICP} = 200 W, P_{RF} = 50 W - DC_{bias} = -210 V - p = 10 mmTor, p_{He} = 16 Torr (8 sccm) - LN2 cooling on - targeted mesa height: 175 nm

A.3.4 Plasma enhanced chemical vapor deposition (PECVD)

PECVD	**T** (^{o}C)	**time** (m:s)	**Comments**
			Oxford instruments Plasmalab system 100
SiN deposition	300		- SiH_4 = 16.6 sccm, NH_3 = 13.4 sccm - N_2 = 980 sccm - P_{RF} = 20 W - p = 650 mmTor - deposition rate: 12 nm/min

A.4 Small gate periphery devices (*inverse mesa*)

Small periphery devices consist of two parallel gate fingers in a U-shape layout with total gate width (W_g) of $80\,\mu m$*. The gates have been defined either using optical contact lithography or electron beam lithography. The optically defined gates are called "long" or "fat" as their gate length (L_g) is* $2\,\mu m$*. The e-beam defined gates are called "sub-micron" gates and the gate length used for small periphery devices is* $0.25\,\mu m$*.*

We have processed small periphery devices using two different mask sets. The first set ("inverse mesa") consists of devices with optically defined gates only. The process flow for this set is described in this section. The second mask set ("submu") consists of devices with both optically and e-beam defined gates. The process flow for this set will be described in Sect. A.5.

A.4.1 Sample preparation

Preparation	**T** (^{o}C)	**time (m:s)**	**Comments**
Spin coat epi-side 2" wafer with AZ5214e			protect epilayers during saw/dice process
Bake AZ5214e	95	5:00	hotplate
Paste 2" wafer with resist coated epi-side on blue tape			if sawn with disco
Sawing of 2" wafer			- sample size at least 10 x 10 mm^2 - diamond coated saw blade - water cooled
Dicing of 2" wafer			- sample size at least 10 x 10 mm^2 - Manually with diamond scratch pen
Mark substrate side			scratch "Z" on substrate (sapphire/SiC) side to identify epi-side during processing

A.4.2 Sample cleaning

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
Remove surface oxides		1:30	- sample completely dipped - BHF
Rinsing			see A.1.2
Optical inspection			polyvar

A.4.3 Ohmic contact lithography

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
AZ5214e			see A.2.1
Optical inspection			- polyvar - check development and lift-off profile

A.4.4 Ohmic contact metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Al/Ni/Au = 30/180/40/100 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.4.5 Lift-off after ohmic contact metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.4.6 Dispersion etch

	T (^{o}C)	**time (m:s)**	**Comments**
RIE: dispersion			see A.3.1

A.4.7 Rapid thermal annealing of ohmic contacts

	T (^{o}C)	time (m:s)	Comments
RTA process	800	2:00	- AST RTA: 800n-m02.2 - N_2ambient - ramp-up 100 ^{o}C - 800 ^{o}C in 45 seconds
Dummy run	800	2:00	- no samples - AST RTA: 800n-m02.2
RTA ohmic contacts	800	2:00	- all samples at once - AST RTA: 800n-m02.2

A.4.8 Mesa lithography

	T (^{o}C)	time (m:s)	Comments
Cleaning			see A.1.1
AZ4533			see A.2.2
Measure resist height			Tencor Alpha Step

A.4.9 Mesa formation

	T (^{o}C)	time (m:s)	Comments
ICP: mesa			see A.3.3
Measurement step height after ICP etch			Tencor Alpha Step
Remove AZ4533			see A.1.6
Optical inspection			polyvar
Measurement mesa height			Tencor Alpha Step

A.4.10 Schottky gate and probe pad lithography

	T (^{o}C)	time (m:s)	Comments
Cleaning			see A.1.1
AZ5214e			see A.2.2
Optical inspection			- polyvar - check development and lift-off profile

A.4.11 Schottky gate and probe pad metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ni/Au = 20/250 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.4.12 Lift-off after Schottky gate and probe pad metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.4.13 Surface passivation

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
SiN deposition	300	8:36	- see A.3.4 - 100 nm

A.5 Small gate periphery devices (*submu*)

This section describes the process flow for small periphery devices using the submu mask set. The gate length for these devices is $0.25\,\mu m$.

A.5.1 Sample preparation

Preparation	**T** (^oC)	**time (m:s)**	**Comments**
Spin coat epi-side 2” wafer with AZ5214e			protect epilayers during saw/dice process
Bake AZ5214e	95	5:00	hotplate
Paste 2” wafer with resist coated epi-side on blue tape			if sawn with disco
Sawing of 2” wafer			- sample size 10 x 10 mm^2 - diamond coated saw blade - water cooled
Dicing of 2” wafer			- sample size 10 x 10 mm^2 - Manually with diamond scratch pen
Mark substrate side			- scratch “Z” on substrate (sapphire/SiC) side to identify epi-side during processing

A.5.2 Sample cleaning

	T (^oC)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
Remove surface oxides		1:30	- sample completely dipped - BHF
Rinsing			see A.1.2
Optical inspection			polyvar

A.5.3 Mesa lithography

	T (^oC)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
AZ4533			see A.2.2
Measure resist height			Tencor Alpha Step

A.5.4 Mesa formation

	T (^{o}C)	**time (m:s)**	**Comments**
ICP: mesa			see A.3.3
Measurement step height after ICP etch			Tencor Alpha Step
Remove AZ4533			see A.1.6
Optical inspection			polyvar
Measurement mesa height			Tencor Alpha Step

A.5.5 Ohmic contact lithography

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
AZ5214e			see A.2.1
Optical inspection			- polyvar - check development and lift-off profile

A.5.6 Ohmic contact metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Al/Ni/Au = 30/180/40/100 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.5.7 Lift-off after ohmic contact metallization

	T (^{o}C)	**time (m:s)**	**Comments**
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.5.8 Oxygen plasma

	T (^{o}C)	**time (m:s)**	**Comments**
Stripping	20	5:00	see A.1.5

A.5.9 Dispersion etch

	T (^oC)	time (m:s)	Comments
RIE: dispersion			see A.3.1

A.5.10 Rapid thermal annealing of ohmic contacts

	T (^oC)	time (m:s)	Comments
RTA process	800	2:00	- AST RTA: 800n-m02.2 - N_2ambient - ramp-up 100 ^{o}C - 800 ^{o}C in 45 seconds
Dummy run	800	2:00	- no samples - STS RTA: 800n-m02.2
RTA ohmic contacts	800	2:00	- all samples at once - STS RTA: 800n-m02.2

A.5.11 Surface passivation

	T (^oC)	time (m:s)	Comments
Surface preparation	20	1:00	NH_4OH (25%) : UPW = 1 : 10 (volume)
Rinsing			see A.1.2
SiN deposition	300	8:36	- see A.3.4 - 100 nm

A.5.12 Lithography for definition of fat gates and RF probe pads

	T (^oC)	time (m:s)	Comments
			- define RF probe pads on fat gate modules - use this pattern to open SiN
Cleaning			see A.1.1
AZ5214e			see A.2.1
Optical inspection			- polyvar - check development

A.5.13 Open SiN passivation layer on fat gate modules

	T (^{o}C)	time (m:s)	Comments
RIE: SF_6	20	4:00	- see A.3.2 - open SiN on ohmic contacts and underneath gates and RF probe pads
Optical inspection			polyvar

A.5.14 Metallization of fat gates and RF probe pads

	T (^{o}C)	time (m:s)	Comments
Evaporation			- Ni/Au = 20/250 nm - evaporation rate Au: 3 Å/s - Airco electron beam evaporator

A.5.15 Lift-off after metallization of fat gates and RF probe pads

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			see A.1.4, but now soak in acetone for 10 minutes
Optical inspection			polyvar

A.5.16 Lithography for foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
Cleaning			see A.1.1
PMMA 950K A4			see A.2.6
Thermal evaporation			- Edwards, tooling factor 1.4 - Au = 12.5 nm

A.5.17 Electron beam writing of foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
EBL: foot			- RAITH 150 - EHT = 20 kV - aperture = 10 μm - write field = 300 x 300 μm^2 - line step size = 5 nm - line dose = 500 pC/cm - dose factor SPL = 14.4
Remove thermal Au layer	20	0:45	- KI solution - etch rate = 500 nm/min - Au layer has to be removed before developing MMA(8.5)MAA EL13
Rinsing			see A.1.2
Develop PMMA 950K A4			see A.2.6
Optical inspection			
Oxygen descum		0:30	see A.1.5

A.5.18 Open SiN passivation layer underneath foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
			open SiN passivation layer underneath foot T/FP gates
RIE: SF_6		2:50	- see A.3.2 - avoid over-etching too much because of damage to AlGaN underneath gate (leakage currents)

A.5.19 Metallization of foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
Evaporation			- Ni/Au = 20/40 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.5.20 Lift-off after metallization of foot T/FP gates

	T (^oC)	time (m:s)	Comments
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.5.21 Lithography for top T/FP gates

	T (^oC)	time (m:s)	Comments
Cleaning			see A.1.1
MMA(8.5)MAA EL13			see A.2.5 (use spinning top)
Thermal evaporation			- Edwards, tooling factor 1.4 - Au = 12.5 nm

A.5.22 Electron beam writing of top T/FP gates

	T (^oC)	time (m:s)	Comments
EBL: top			- RAITH 150 - EHT = 20 kV - aperture = 10 μm - write field = 300 x 300 μm^2 - area step size = 15 nm - area dose = 100 $\mu C/cm^2$ - dose factor T = 3.0
Remove thermal Au layer	20	0:45	- KI solution - etch rate = 500 nm/min - Au layer has to be removed before developing MMA(8.5)MAA EL13
Rinsing			see A.1.2
Develop MMA(8.5)MAA EL13			see A.2.5
Optical inspection			
Oxygen descum		0:30	see A.1.5

A.5.23 Metallization of top T/FP gates

	T (^oC)	time (m:s)	Comments
Evaporation			- Ni/Au = 20/380 nm - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

A.5.24 Lift-off after metallization of top T/FP gates

	T (^oC)	time (m:s)	Comments
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.5.25 Lithography to open SiN on ohmic contacts of submu modules

	T (^oC)	time (m:s)	Comments
			open SiN on ohmic contacts of submu modules
Cleaning			see A.1.1
AZ5214e			see A.2.1
Optical inspection			polyvar

A.5.26 Open SiN passivation layer on ohmic contacts

	T (^oC)	time (m:s)	Comments
RIE: SF_6	20	4:00	- see A.3.2 - open SiN on ohmic contacts and open regions where gate flaps will be defined
Remove AZ5214e	20	1:00	- stripping see A.1.5 but now 1 minute
Soak in acetone		2:00	
Cleaning			see A.1.1
Optical inspection			polyvar

A.5.27 Lithography for definition of RF probe pads

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
AZ5214e			see A.2.1
Optical inspection			- polyvar - check development and lift-off profile

A.5.28 Metallization of RF probe pads

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Au = 20/250 nm - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

A.5.29 Lift-off after metallization of RF probe pads

	T (^{o}C)	**time (m:s)**	**Comments**
Metal lift-off			see A.1.4, but now soak in acetone for 10 minutes
Optical inspection			polyvar

A.6 Large gate periphery devices (*mmTor*)

The large periphery devices have total gate widths that vary from 0.25 *mm to* 6.4 *mm. To achieve these device widths multiple parallel gate fingers are needed that are arranged in either "comb" or "fishbone" layouts. The unit gate widths* (W_{gu}) *are* 62.5 μm, 100 μm, 125 μm, *and* 200 μm *respectively. The gates are defined using electron beam lithography to obtain a gate length of* 0.7 μm. *T-shaped and field-plated (FP) sub-micron gates have been fabricated to prevent high gate resistance at microwave frequencies due to the skin effect, reduce charge trapping at the edge of the gate nearest to the drain contact, and increase the breakdown voltage of the HFETs.*

A.6.1 Sample preparation

Preparation	**T** (^{o}C)	**time (m:s)**	**Comments**
Spin coat epi-side 2" wafer with AZ5214e			protect epilayers during saw/dice process
Bake AZ5214e	95	5:00	hotplate
Paste 2" wafer with resist coated epi-side on blue tape			if sawn with disco
Sawing of 2" wafer			- sample size 10 x 10 mm^2 - diamond coated saw blade - water cooled
Dicing of 2" wafer			- sample size 10 x 10 mm^2 - Manually with diamond scratch pen
Mark substrate side			scratch "Z" on substrate (sapphire/SiC) side to identify epi-side during processing

A.6.2 Sample cleaning

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
Remove surface oxides		1:30	- sample completely dipped - BHF
Rinsing			see A.1.2
Optical inspection			polyvar

A.6.3 Optical alignment marks lithography

	T (^{o}C)	**time** (m:s)	**Comments**
Cleaning			see A.1.1
ma-N415			see A.2.3
Optical inspection			- polyvar - check development and lift-off profile

A.6.4 Optical alignment marks metallization

	T (^{o}C)	**time** (m:s)	**Comments**
Evaporation			- Au = 100 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.6.5 Lift-off after optical alignment marks metallization

	T (^{o}C)	**time** (m:s)	**Comments**
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.6.6 Ohmic contact lithography

	T (^{o}C)	**time** (m:s)	**Comments**
Cleaning			see A.1.1
ma-N415			see A.2.3
Optical inspection			- polyvar - check development and lift-off profile

A.6.7 Ohmic contact metallization

	T (^{o}C)	**time** (m:s)	**Comments**
Evaporation			- Ti/Al/Ni/Au = 30/180/40/100 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.6.8 Lift-off after ohmic contact metallization

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.6.9 Oxygen plasma

	T (^{o}C)	time (m:s)	Comments
Stripping	20	5:00	see A.1.5

A.6.10 Dispersion etch

	T (^{o}C)	time (m:s)	Comments
RIE: dispersion			see A.3.1

A.6.11 Rapid thermal annealing of ohmic contacts

	T (^{o}C)	time (m:s)	Comments
RTA process	800	2:00	- AST RTA: 800n-m02.2 - N_2ambient - ramp-up 100 ^{o}C - 800 ^{o}C in 45 seconds
Dummy run	800	2:00	- no samples - AST RTA: 800n-m02.2
RTA ohmic contacts	800	2:00	- all samples at once - AST RTA: 800n-m02.2

A.6.12 Mesa lithography

	T (^{o}C)	time (m:s)	Comments
Cleaning			see A.1.1
AZ4533			see A.2.2
Measure resist height			Tencor Alpha Step

A.6.13 Mesa formation

	T (^{o}C)	time (m:s)	Comments
ICP: mesa			see A.3.3
Measurement step height after ICP etch			Tencor Alpha Step
Remove AZ4533			see A.1.6
Optical inspection			polyvar
Measurement mesa height			Tencor Alpha Step

A.6.14 Surface passivation

	T (^{o}C)	time (m:s)	Comments
Surface preparation	20	1:00	NH_4OH (25%) : UPW = 1 : 10 (volume)
Rinsing			see A.1.2
SiN deposition	300	8:36	- see A.3.4 - 100 nm

A.6.15 Lithography to open SiN

	T (^{o}C)	time (m:s)	Comments
			open SiN on ohmic contacts and open regions where gate flaps will be defined
Cleaning			see A.1.1
AZ5214e			see A.2.2
Optical inspection			polyvar

A.6.16 Open SiN passivation layer on ohmic contacts

	T (^oC)	time (m:s)	Comments
RIE: SF_6	20	4:00	- see A.3.2 - open SiN on ohmic contacts and open regions where gate flaps will be defined
Remove AZ5214e	20	1:00	stripping see A.1.5 but now 1 minute
Soak in acetone		2:00	
Cleaning			see A.1.1
Optical inspection			polyvar

A.6.17 Lithography for foot T/FP gates

	T (^oC)	time (m:s)	Comments
Cleaning			see A.1.1
MMA(8.5)MAA EL13			see A.2.5 (use spinning foot)
Thermal evaporation			- Edwards, tooling factor 1.4 - Au = 12.5 nm

A.6.18 Electron beam writing of foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
EBL: foot			- RAITH 150 - EHT = 20 kV - aperture = 10 μm - write field = 300 x 300 μm^2 - area step size = 15 nm - area dose = 100 μC/cm^2 - dose factor = 3.0
Remove thermal Au layer	20	0:45	- KI solution - etch rate = 500 nm/min - Au layer has to be removed before developing MMA(8.5)MAA EL13
Rinsing			see A.1.2
Develop MMA(8.5)MAA EL13			see A.2.5
Optical inspection			
Oxygen descum		0:30	see A.1.5

A.6.19 Open SiN passivation layer underneath foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
			open SiN passivation layer underneath foot T/FP gates
RIE: SF_6		2:50	- see A.3.2 - avoid over-etching too much because of damage to AlGaN underneath gate (leakage currents)

A.6.20 Metallization of foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
Evaporation			- Ni/Au = 20/150 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

A.6.21 Lift-off after metallization of foot T/FP gates

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.6.22 Lithography for top T/FP gates

	T (^{o}C)	time (m:s)	Comments
Cleaning			see A.1.1
MMA(8.5)MAA EL13			see A.2.5 (use spinning top)
Thermal evaporation			- Edwards, tooling factor 1.4 - Au = 12.5 nm

A.6.23 Electron beam writing of top T/FP gates

	T (^{o}C)	time (m:s)	Comments
EBL: top			- RAITH 150 - EHT = 20 kV - aperture = 10 μm - write field = 300 x 300 μm^2 - area step size = 15 nm - area dose = 100 μC/cm^2 - dose factor T = 3.0 - dose factor FP0.5 = 1.0 - dose factor FP1.0 = 1.1
Remove thermal Au layer	20	0:45	- KI solution - etch rate = 500 nm/min - Au layer has to be removed before developing MMA(8.5)MAA EL13
Rinsing			see A.1.2
Develop MMA(8.5)MAA EL13			see A.2.5
Optical inspection			
Oxygen descum		0:30	see A.1.5

A.6.24 Metallization of top T/FP gates

	T (°C)	**time (m:s)**	**Comments**
Evaporation			- Ni/Au = 20/250 nm - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

A.6.25 Lift-off after metallization of top T/FP gates

	T (°C)	**time (m:s)**	**Comments**
Metal lift-off			see A.1.4
Optical inspection			polyvar

A.6.26 Lithography for definition of RF probe pads

	T (°C)	**time (m:s)**	**Comments**
Cleaning			see A.1.1
ma-N415			see A.2.3
Optical inspection			- polyvar - check development and lift-off profile

A.6.27 Oxygen plasma

	T (°C)	**time (m:s)**	**Comments**
Stripping	20	1:00	see A.1.5, but now 1 minute

A.6.28 Metallization of RF probe pads

	T (°C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Au = 20/250 nm - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

A.6.29 Lift-off after metallization of RF probe pads

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			see A.1.4, but now soak in acetone for 10 minutes
Optical inspection			polyvar

A.6.30 Lithography for definition of via openings

	T (^{o}C)	time (m:s)	Comments
			definition of via openings and air bridge support
Cleaning			see A.1.1
AZ4533			- see A.2.2 (use in this case Mask exposure: UV 430) - hard bake this time at 160 ^{o}C for 20 minutes in HERAEUS hot air oven in yellow room
Optical inspection			polyvar

A.6.31 Oxygen plasma

	T (^{o}C)	time (m:s)	Comments
Stripping	20	1:00	see A.1.5, but now 1 minute
Optical inspection			polyvar

A.6.32 Evaporation transparent Au separation layer

	T (^{o}C)	time (m:s)	Comments
			Evaporation of transparent Au layer to separate via litho (see A.5.30) and bridge litho (see A.5.33)
Evaporation			- Au = 12.5 nm - evaporation rate Au: 3 Å/s - Airco electron beam evaporator

A.6.33 Lithography for definition of air bridges

	T (^{o}C)	**time (m:s)**	**Comments**
			NO cleaning with acetone and iso-propyl alcohol!
ma-N440			see A.2.4
Optical inspection			- polyvar - check development and lift-off profile

A.6.34 Oxygen plasma

	T (^{o}C)	**time (m:s)**	**Comments**
Stripping	20	1:00	see A.1.5, but now 1 minute

A.6.35 Metallization of air bridges

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Au = 20/1500 nm - evaporate Au in three steps of 500 nm each with cool down intervals of 30 minutes - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

A.6.36 Lift-off after metallization of air bridges

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			- see A.1.4, but now soak in acetone for 10 minutes - spray with acetone on sample while it is still underneath acetone surface - metallization comes off as one thick film
Optical inspection			- polyvar - all slits between air bridges have been removed
Removal transparent Au layer		1:00	- KCN solution (DEGUSSA) - use the old solution with an etch rate of about 20 nm/min - don't use KI solution because the etch rate is too high (500 nm/min). This high etch rate causes a very rough Au surface
Optical inspection			polyvar

A.6.37 Removal of air bridge support resist

	T (^{o}C)	time (m:s)	Comments
			Remove AZ4533
Soak in aceton		30:00	
Spray with acetone			- in quartz basket with teflon insert - above waste container
Cleaning			see A.1.1
Ashing	20	15:00	see A.1.5
Optical inspection			polyvar

Appendix B

Process flow for CPW passive components on s.i. SiC

We have developed a process flow for coplanar waveguide (CPW) passive components on s.i. SiC substrates. This appendix starts with descriptions of process steps that form the building blocks for the complete process flow. Section B.2 describes the process settings for resists used for optical contact lithography. Section B.3 provides process settings for different plasma processes used. Finally, section B.4 provides the complete process flow for the CPW components.

B.1 Building blocks

B.1.1 Cleaning

Cleaning	**Comments**
Spray with acetone (CH_3COCH_3)	- in quartz basket with teflon insert - above waste container
Spray with iso-propyl alcohol ($CH_3CHOHCH_3$)	- in quartz basket with teflon insert - above waste container
Blow dry with nitrogen (N_2)	

B.1.2 Rinsing

Rinsing	**Comments**
Rinse in ultra pure water (UPW)	- for *positive* resists time > 1 minute - for *negative* resists time > 3 minutes - for both resist types resistance water > 5MΩ - place sample in quartz basket with teflon insert
Blow dry with nitrogen (N_2)	

B.1.3 Exposure

Exposure	Comments
UV 300	- Karl Süss MJB3 mask aligner - λ = 300 nm - optical power density: 3.4 mW/cm^2 (range 20)
UV 430	- Karl Süss MA6 mask aligner - λ = 430 nm - optical power density: 7.5 mW/cm^2 (range 20) - vacuum mode

B.1.4 Metal lift-off

Lift-off	Comments
Soak in aceton	time > 3 minutes
Spray with acetone	- in quartz basket with teflon insert - above waste container
Ultrasonically stirring in acetone	- time > 1 minute - place quartz basket with teflon holder on bottom of beaker glass
Cleaning	see C.1.1

B.1.5 Oxygen plasmas

Oxygen plasmas	T (^{o}C)	time (m:s)	Comments
Stripping_CPW	20	1:00	- Tepla - process power 150 W - Faraday cage
Ashing_CPW	20	5:00	- Tepla - process power 300 W - Faraday cage

B.1.6 Resist removal after plasma etching

Resist removal	**T** (^{o}C)	**time (m:s)**	**Comments**
Stripping_CPW	20	5:00	see C.1.5
Spray with acetone			- in quartz basket with teflon insert - above waste container
Ultrasonically stirring in acetone		2:00	place quartz basket with teflon holder on bottom of beaker glass
Cleaning			see C.1.1

B.1.7 Adhesion promotion

Adhesion promotion	**T** (^{o}C)	**time (m:s)**	**Comments**
Ashing_CPW	20	5:00	see C.1.5
Rinsing			see C.1.2
HMDS deposition	20	3:00	old Delft vapour cylinder

B.2 Resists for optical contact lithography

B.2.1 Microchemicals AZ5214e

AZ5214e	T (^{o}C)	time (m:s)	Comments
			- optical lithography - positive radiation sensitive
Spinning		0:30	- open air spinner - 5000 rpm
Soft bake	95	5:00	hotplate
Flood exposure		0:00.8	- UV 300, see C.1.3 - required for lift-off profile
Bake	105	5:00	hotplate
Mask exposure		0:30	UV 300, see C.1.3
Develop		1:35	AZ developer : UPW = 1 : 1 (volume)
Rinsing			see C.1.2

B.2.2 Microchemicals AZ4533

AZ4533	T (^{o}C)	time (m:s)	Comments
			- optical lithography - positive radiation sensitive
Spinning		0:30	- open air spinner - 5000 rpm
Soft bake	95	20:00	hotplate
Mask exposure: UV 430		0:32	UV 430, see C.1.3
Develop		1:50	AZ developer : UPW = 1 : 1 (volume)
Rinsing			see C.1.2
Hard bake	160	20:00	HERAEUS hot air oven in yellow room

B.2.3 Micro resist ma-N440

ma-N440	**T** (^{o}C)	**time (m:s)**	**Comments**
			- optical lithography - negative radiation sensitive
Spinning_top plate		0:30	- CONVAC open air spinner - 3000 rpm
Spinning_air bridge		0:30	- CONVAC open air spinner - 2500 rpm
Bake_top plate	90	4:00	hotplate
Bake_air bridge	95	5:00	hotplate
Mask exposure_top plate		3:20	- UV 430, see C.1.3 - Vacuum mode
Mask exposure_air bridge		8:20	- UV 430, see C.1.3 - Vacuum mode - 5 x 100 seconds
Develop_top plate		1:00	ma-D332S (concentrated)
Develop_air bridge		1:30	ma-D332S (concentrated)
Rinsing			see C.1.2

B.3 Plasma processes

B.3.1 RIE: open silicon nitride layer

RIE: SF_6	**T (^oC)**	**time (m:s)**	**Comments**
			Oxford instruments Plasmalab system 100
Chamber and quartz plate cleaning	20	30:00	- O_2 = 20 sccm, Ar = 10 sccm - P_{RF} = 100 W, DC_{bias} = -141 V - p = 100 mmTor - heater-chiller on, cooling on
Chamber conditioning	20	10:00	- no sample - 3B mode C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on
Dummy run	20	3:00	- one dummy sample - 1F mode, C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on - determined etch rate SiN: 50 - 60 nm/min
Open SiN	20	6:00	- one sample at a time - 1F mode, C_1 = 52, C_2 = 47 - SF_6 = 10 sccm, - P_{RF} = 10 W, DC_{bias} = -10 V - p = 40 mmTor - heater-chiller on, cooling on - considerably over-etched to avoid SiN remainings

B.3.2 Plasma enhanced chemical vapor deposition (PECVD)

PECVD	**T** (^{o}C)	**time (m:s)**	**Comments**
			Oxford instruments Plasmalab system 100
SiN deposition	300		- SiH_4 = 16.6 sccm, NH_3 = 13.4 sccm - N_2 = 980 sccm - P_{RF} = 20 W - p = 650 mmTor - deposition rate: 12 nm/min

B.4 Complete process flow for CPW components on s.i. SiC

This section describes the complete process flow for CPW passive components on s.i. SiC using the process steps described in the previous sections.

B.4.1 Sample preparation

Preparation	**T** (^{o}C)	**time (m:s)**	**Comments**
Spin coat epi-ready side of 2" wafer with AZ5214e			protection during saw process
Bake AZ5214e	95	5:00	hotplate
Paste 2" wafer with resist coated side on blue tape			
Sawing of 2" wafer			- sample size at least 15 x 15 mm^2 - diamond coated saw blade - water cooled

B.4.2 Sample cleaning

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see C.1.1
Rinsing			see C.1.2
Optical inspection			polyvar

B.4.3 Deposition SiN base layer

	T (^{o}C)	**time (m:s)**	**Comments**
Cleaning			see C.1.1
SiN deposition	300	4:18	- see C.3.2 - 50 nm

B.4.4 Lithography of bottom plate

	T (^{o}C)	**time (m:s)**	**Comments**
Adhesion promotion			see C.1.7
AZ5214e			see C.2.1
Optical inspection			- polyvar - check development and lift-off profile

B.4.5 Oxygen plasma

	T (^{o}C)	**time (m:s)**	**Comments**
Stripping_CPW	20	1:00	see C.1.5

B.4.6 Metallization of bottom plate

	T (^{o}C)	**time (m:s)**	**Comments**
Evaporation			- Ti/Au = 50/200 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

B.4.7 Lift-off after metallization of bottom plate

	T (^{o}C)	**time (m:s)**	**Comments**
Metal lift-off			see C.1.4
Optical inspection			polyvar

B.4.8 Oxygen plasma

	T (^{o}C)	**time (m:s)**	**Comments**
Ashing_CPW	20	5:00	see C.1.5

B.4.9 Deposition SiN dielectric layer

	T (^{o}C)	time (m:s)	Comments
			SiN film is used as dielectric layer for MIM capacitors
Cleaning			see C.1.1
SiN deposition	300	17:12	- see C.3.2 - 200 nm

B.4.10 Lithography of top plate

	T (^{o}C)	time (m:s)	Comments
ma-N440			- see C.2.3 - use settings for top plate
Optical inspection			- polyvar - check development and lift-off profile

B.4.11 Oxygen plasma

	T (^{o}C)	time (m:s)	Comments
Stripping_CPW	20	1:00	see C.1.5

B.4.12 Metallization of top plate

	T (^{o}C)	time (m:s)	Comments
Evaporation			- Ti/Au = 50/200 nm - evaporation rate: 3 Å/s - Airco electron beam evaporator

B.4.13 Lift-off after metallization of top plate

	T (^{o}C)	time (m:s)	Comments
Metal lift-off			see C.1.4
Optical inspection			polyvar

B.4.14 Oxygen plasma

	T (^oC)	time (m:s)	Comments
Ashing_CPW	20	5:00	see C.1.5

B.4.15 Lithography for via openings

	T (^oC)	time (m:s)	Comments
Cleaning			see C.1.1
Adhesion promotion			see C.1.7
AZ5214e			see C.2.1
Optical inspection			polyvar

B.4.16 Oxygen plasma

	T (^oC)	time (m:s)	Comments
Stripping_CPW	20	1:00	see C.1.5

B.4.17 Open SiN dielectric layer

	T (^oC)	time (m:s)	Comments
RIE: SF_6	20	6:00	- see C.3.1 - etch rate: 50 - 60 nm/min - deliberately over etch to avoid SiN remainings
Remove AZ5214e			see C.1.6
Optical inspection			polyvar

B.4.18 Oxygen plasma

	T (^oC)	time (m:s)	Comments
Ashing_CPW	20	5:00	see C.1.5

B.4.19 Lithography of air bridge support layer

	T (^{o}C)	time (m:s)	Comments
Cleaning			see C.1.1
Adhesion promotion			see C.1.7
AZ4533			see C.2.2
Optical inspection			polyvar

B.4.20 Evaporation transparent Au separation layer

	T (^{o}C)	time (m:s)	Comments
			Evaporation of transparent Au layer to separate bridge support litho (see C.4.19) and bridge litho (see C.4.21)
Evaporation			- Au = 12.5 nm - evaporation rate Au: 3 Å/s - Airco electron beam evaporator

B.4.21 Lithography for definition of air bridges

	T (^{o}C)	time (m:s)	Comments
			NO cleaning with acetone and iso-propyl alcohol!
ma-N440			- see C.2.3 - use settings for air bridge
Optical inspection			- polyvar - check development and lift-off profile

B.4.22 Oxygen plasma

	T (^{o}C)	time (m:s)	Comments
Stripping_CPW	20	1:00	see C.1.5

B.4.23 Metallization of air bridges and thick gold on TLs

	T (^oC)	time (m:s)	Comments
			Metallization of air bridges and thick gold layer on transmission lines (TLs)
Evaporation			- Ti/Au = 12.5/2000 nm - evaporate Au in four steps of 500 nm each with cool down intervals of 30 minutes - evaporation rate Au: 6 Å/s - Airco electron beam evaporator

B.4.24 Lift-off after metallization of air bridges and TLs

	T (^oC)	time (m:s)	Comments
Metal lift-off			- see C.1.4, but now soak in acetone for 10 minutes
Optical inspection			polyvar
Ashing_CPW	20	5:00	see C.1.5
Removal transparent Au layer		1:00	- KCN solution (DEGUSSA) - use the old solution with an etch rate of about 20 nm/min - don't use KI solution because the etch rate is too high (500 nm/min). This high etch rate causes a very rough Au surface
Optical inspection			polyvar

B.4.25 Removal of air bridge support resist

	T (^{o}C)	time (m:s)	Comments
			Remove AZ4533
Soak in aceton		20:00	
Spray with acetone			- in quartz basket with teflon insert - above waste container
Cleaning			see C.1.1
Ashing_CPW	20	15:00	see C.1.5
Optical inspection			polyvar

List of contstants and acronyms

List of constants

q	elementary charge	$1.60 \cdot 10^{-19}$	C
ε_0	permittivity of vacuum	$8.85 \cdot 10^{-12}$	F/m
h	Planck's constant	$6.63 \cdot 10^{-34}$	Js
$\hbar$	Dirac's constant ($h/2\pi$)	$1.05 \cdot 10^{-34}$	Js
k	Bolzmann's constant	$1.38 \cdot 10^{-23}$	J/K
μ_0	permeability of vacuum	$4\pi \cdot 10^{-7}$	H/m

List of acronyms

2DEG	two-dimensional electron gas
3G	third generation
AC	alternating-current
ACLR	adjacent channel leakage ratio
ACPR	adjacent channel power ratio
Al	aluminum
AlGaAs	aluminum gallium arsenide
AlGaN	aluminum gallium nitride
AlInGaN	aluminum indium gallium nitride
AlInGaP	aluminum indium gallium phosphide
AlN	aluminum nitride
AMS	Applied Materials Science group
Ar	argon
Au	gold

BFOM	Baliga's figure of merit
BHF	buffered hydrofluoric acid
BJT	bipolar junction transistor
CAIBE	chemically assisted ion beam etching
cd	critical dimension
CD	compact disc
CL	cathodoluminescence
Cl_2	chlorine
CPW	coplanar waveguide
Cu	copper
CW	continuous wave
DAC	digital-to-analog converter
DARPA	Defense Advanced Research Projects Agency
dc	duty cycle
DC	direct-current
DH	double-heterostructure
DoD	department of defense
DRAM	dynamic random access memory
DUT	device under test
DVD	digital versatile disc
EBL	electron beam lithography
ECR	electron cyclotron resonance
ETP	Equilibrium and Transport in Plasmas group
FET	field-effect transistor
FP	field plate
FTIR	Fourier transform infrared spectroscopy
FZ	float zone
Ga	gallium
GaAs	gallium arsenide
GaAsP	gallium arsenide phosphide
GaCl	gallium monochloride
GaN	gallium nitride
GaP:N	gallium phosphide nitride
GB	giga byte
GSG	ground-signal-ground
H_2	hydrogen
HB	high-brightness

HBT	heterojunction bipolar transistor
HCl	hydrochloric acid
HD-DVD	high-density digital versatile disc
HEMT	high electron mobility transistor
HEV	hybrid electric vehicle
HF	hydrofluoric acid
HFET	heterostructure field-effect transistor
HPA	high-power amplifier
HR	high-resistivity
HVPE	hydride vapor phase epitaxy
IC	integrated circuit
ICE	internal combustion engine
ICP	inductively coupled plasma
IGBT	insulated-gate bipolar transistor
InGaAs	indium gallium arsenide
InGaP	indium gallium phosphide
InN	indium nitride
InP	indium phosphide
JFOM	Johnson's figure of merit
KCN	potassium cyanide
LD	laser diode
LDMOS	laterally diffused metal oxide semiconductor
LED	light emitting diode
LEEBI	low-energy electron beam irradiation
LEO	lateral epitaxial overgrowth
LIF	laser-induced fluorescence
LNA	low-noise amplifier
MAG	maximum available gain
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical system
MESFET	metal semiconductor field-effect transistor
Mg	magnesium
MMA	methacrylic acid
MMIC	microwave monolithic integrated circuit
MOCVD	metal organic chemical vapor deposition
MoD	ministry of defense

MODFET	modulation-doped field-effect transistor
MOSFET	metal oxide semiconductor field-effect transistor
Na	sodium
N_2	nitrogen
NH_3	ammonia
NH_4OH	ammonium hydroxide
Ni	nickel
NiCr	nickel chromium
n.i.d.	non-intentionally doped
NIL	nano-imprint lithography
NL	nucleation layer
OED	Opto-Electronic Devices group
P	phosphorus
PA	power amplifier
PAE	power added efficiency
PDA	personal digital assistant
PECVD	plasma enhanced chemical vapor deposition
pHEMT	pseudomorphic high electron mobility transistor
PL	photoluminescence
PMMA	polymethyl methacrylate
Pt	platinum
PW	pulse width
RF	radio frequency
RIE	reactive ion etching
RT	room temperature
RTA	rapid thermal annealing
RU	Radboud Universiteit Nijmegen
s.i.	semi-insulating
SDHT	selectively-doped heterostructure transistor
SE	spectroscopic ellipsometry
SEM	scanning electron microscopy
SF_6	sulfurhexafluoride
SFP	source-terminated field plate
Si	silicon
SiC	silicon carbide
$SiCl_4$	silicon tetrachloride
SiGe	silicon germanium
SiH_4	silane

SiN	silicon nitride
SiO_2	silicon dioxide
SOI	silicon-on-insulator
STW	Stichting voor Technische Wetenschappen
TEC	thermal expansion coefficient
TEGFET	two-dimensional electron gas field-effect transistor
TFE	thermionic field emission
Ti	titanium
TL	transmission line
TLM	transmission line method
TMG	trimethyl gallium
TU/e	Technische Universiteit Eindhoven
TWTA	traveling wave tube amplifier
UV	ultra violet
WBG	wide-bandgap
W-CDMA	wide-band code-division multiple access

Summary

Gallium Nitride-based Microwave High-Power Heterostructure Field-Effect Transistors

design, technology, and characterization

The research described in this thesis has been carried out within a joint project between the Radboud Universiteit Nijmegen (RU) and the Technische Universiteit Eindhoven (TU/e) with the title: "Performance enhancement of GaN-based microwave power amplifiers: material, device and design issues". This project has been granted by the Dutch Technology Foundation STW under project number NAF 5040. The aims of this project have been to develop the technology required to grow state-of-the-art AlGaN/GaN epilayers on sapphire and semi-insulating (s.i.) SiC substrates using metal organic chemical vapor deposition (MOCVD) and to fabricate microwave (f > 1 GHz) high-power (P_{out} > 10 W) heterostructure field-effect transistors (HFETs) on these epitaxial films. MOCVD growth of AlGaN/GaN epilayers and material characterization has been done within the group Applied Materials Science (AMS) of RU. Research at the Opto-Electronic Devices group (OED) of TU/e has focused on both electrical characterization of AlGaN/GaN epilayers and design, process technology development, and characterization of GaN-based HFETs and CPW passive components. Although a considerable amount of work has been done during this research with respect to processing of CPW passive components on s.i. SiC substrates, this thesis focused on active AlGaN/GaN devices only.

GaN is an excellent option for high-power/high-temperature microwave applications because of its high electric breakdown field (3 MV/cm) and high electron saturation velocity (1.5 x 10^7 cm/s). The former is a result of the wide bandgap (3.44 eV at RT) and enables the application of high supply voltages (> 50 V), which is one of the two requirements for high-power device performance. In addition, the wide bandgap allows the material to withstand much higher operating temperatures (300 °C - 500 °C) than can the conventional semiconductor materials such as Si, GaAs, and InP. A big advantage of GaN over SiC is the possibility to grow heterostructures, e.g. AlGaN/GaN. The resulting two-dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction serves as the conductive channel. Large drain currents (> 1 A/mm), which are the second requirement for a power device, can be achieved because of the

high electron sheet densities (> 1 x 10^{13} cm^{-2}) and high electron saturation velocity. These material properties clearly indicate why GaN is a very suitable candidate for next-generation microwave high-power/high-temperature applications such as high-power amplifiers (HPAs) for GSM base stations, and microwave monolithic integrated circuits (MMICs) for radar systems.

In this thesis we have presented the design, technology, and measurement results of n.i.d. AlGaN/GaN:Fe HFETs grown on s.i. 4H-SiC substrates by MOCVD. These devices have submicrometer T- or FP-gates with a gate length (L_g) of 0.7 μm and total gate widths (W_g) of 0.25 mm, 0.5 mm, and 1.0 mm, respectively. The 1.0 mm devices are capable of producing a maximum microwave output power (P_{out}) of 11.9 W at S-band (2 GHz - 4 GHz) using class AB bias conditions of V_{DS} = 50 V and V_{GS} = -4.65 V. It has to be noted that excellent scaling of P_{out} with W_g has been demonstrated. In addition, the associated power gain (G_p) ranges between 15 dB and 20 dB, and for the power added efficiency (PAE) values from 54 % up to 70 % have been obtained. These results clearly illustrate both the successful development of the MOCVD growth process, and the successful development and integration of process modules such as ohmic and Schottky contact technology, device isolation, electron beam lithography, surface passivation, and air bridge technology, into a process flow that enables the fabrication of state-of-the-art large periphery n.i.d. AlGaN/GaN:Fe HFETs on s.i. SiC substrates, which are perfectly suitable for application in e.g. HPAs at S-band.

Mark Krämer

Samenvatting

Gallium Nitride Gebaseerde Microgolf Hoogvermogen Heterostructuur Veldeffect Transistoren

ontwerp, technologie en karakterisatie

Het onderzoek dat in dit proefschrift beschreven wordt, is uitgevoerd binnen een gezamenlijk project van de Radboud Universiteit Nijmegen (RU) en de Technische Universiteit Eindhoven (TU/e) met als titel: "Performance enhancement of GaN-based microwave power amplifiers: material, device and design issues". De beoogde doelen van dit project, dat gehonoreerd en financieel ondersteund is door de Stichting voor Technische Wetenschappen (STW) onder projectnummer NAF 5040, waren het ontwikkelen van de vereiste technologie ten behoeve van de epitaxiale groei van hoogwaardige AlGaN/GaN lagen op saffier en halfisolerende SiC substraten en de fabricage van heterostructuur veldeffect transistoren welke in staat zijn een hoog uitgangsvermogen ($P_{\text{out}} > 10$ W) te leveren op microgolf frequenties ($f > 1$ GHz). De toegepaste epitaxiale groeitechniek, die bekend staat als metaal-organische chemische gas fase depositie (MOCVD), en de benodigde materiaalkarakterisatie is uitgevoerd binnen de leerstoel Applied Material Science (AMS) van RU. Het onderzoek binnen de leerstoel Opto-Electronic Devices (OED) van de TU/e heeft zich toegespitst op zowel de elektrische karakterisatie van de epitaxiale AlGaN/GaN lagen als op het ontwerpen van transistorstructuren, het ontwikkelen van procestechnologie en het elektrisch karakteriseren van AlGaN/GaN HFETs en coplanaire passieve componenten. Hoewel een aanzienlijke hoeveelheid werk is verricht met betrekking tot de procesontwikkeling en karakterisatie van coplanaire passieve componenten op halfisolerende SiC substraten, wordt in dit proefschrift uitsluitend ingegaan op actieve AlGaN/GaN HFETs.

GaN is een uitstekende optie voor hoogvermogen en hoge temperatuur microgolf toepassingen vanwege zijn hoge elektrische doorslag veldsterkte (3 MV/cm) en hoge verzadigingssnelheid van de elektronen (1.5 x 10^7 cm/s). Het gebruik van hoge voedingsspanningen (> 50 V), hetgeen een van de voorwaarden is om hoge uitgangsvermogens te genereren, wordt mogelijk gemaakt door de hoge doorslag veldsterkte, die het gevolg is van de grote bandafstand van GaN (3.44 eV bij kamer temperatuur). Een bijkomend voordeel van deze grote bandafstand is dat GaN transistoren nog steeds goed kunnen functioneren bij bedrijfstemperaturen, die tussen de

300 °C en 500 °C liggen, hetgeen niet mogelijk is voor Si en andere III-V halfgeleidermaterialen. Een groot voordeel van GaN ten opzichte van SiC is de mogelijkheid om heterostructuren zoals AlGaN/GaN te groeien. Het tweedimensionale elektronen gas (2DEG) dat zich aan de heterojunctie bevindt, vormt het geleidende kanaal van de transistoren. Een nodige voorwaarde voor het genereren van hoge uitgangsvermogens zijn ook grote drain stromen (> 1 A/mm), welke tot stand komen door de hoge dichtheid (>1 x 10^{13} cm^{-2}) en verzadigingssnelheid van de elektronen die het tweedimensionale elektronen gas vormen. Deze materiaaleigenschappen tonen duidelijk aan dat GaN een zeer geschikte kandidaat is voor toekomstige generaties van microgolf hoogvermogen en hoge temperatuur toepassingen zoals versterkers voor GSM basis stations en microgolf monolithisch geïntegreerde circuits (MMICs) voor radarsystemen.

In dit proefschrift zijn we uitvoering ingegaan op het ontwerp, de technologie en de meetresultaten van ongedoteerde AlGaN/GaN:Fe HFETs die met behulp van MOCVD gegroeid zijn op halfisolerende 4H-SiC substraten. Deze transistoren hebben T- en FP-gate contacten met een lengte (L_g) van 0.7 μm en totale breedten (W_g) van 0.25 mm, 0.5 mm, en 1.0 mm, respectievelijk. Wanneer de transistoren met een totale gate breedte van 1.0 mm ingesteld worden in een klasse AB werkpunt (V_{DS} = 50 V en V_{GS} = -4.65 V), kunnen ze een maximaal uitgangsvermogen (P_{out}) leveren van 11.9 W op S-band (2 GHz - 4 GHz). Tevens dient vermeld te worden dat P_{out} perfect schaalt met de totale gate breedte. Daarnaast laten de vermogensversterking (G_p) en de power added efficiency (PAE) waarden zien van 15 dB - 20 dB en 54 % - 70 %, respectievelijk. Uit deze resultaten kan duidelijk geconcludeerd worden dat we erin geslaagd zijn om zowel een geschikt MOCVD groeiproces als een solide procestechnologie te ontwikkelen. De laatste, welke bestaat uit een integratie van afzonderlijke procesmodules zoals ohmse en Schottky contacten, transistor isolatie, elektronen bundel lithografie, oppervlakte passivatie en luchtbrugtechnologie, maakt het mogelijk om hoogwaardige AlGaN/GaN:Fe HFETs op SiC met een grote totale gate breedte te vervaardigen. Deze transistoren zijn uitstekend geschikt om toegepast te worden in bijvoorbeeld HPAs op S-band.

Mark Krämer

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Mark

Curriculum Vitae

Mark Krämer was born in Sittard, The Netherlands, on the 10th of October 1975. He studied Electrical Engineering at the Eindhoven University of Technology, The Netherlands. After obtaining the ir. (M.Sc.) degree, *cum laude*, in 2000, he started a Ph.D. research on the design, technology, and characterization of gallium nitride-based microwave high-power heterostructure field-effect transistors. This research was carried out within the Opto-Electronic Devices group at the Eindhoven University of Technology. In March 2006, he started working within the RF Devices & Technology group of the Silicon Process Options division at Philips Research Laboratories in Leuven, Belgium.