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DEEP ETCHED DBR GRATINGS IN InP FOR PHOTONIC INTEGRATED CIRCUITS

B. Docter, E.J. Geluk, M.J.H. Sander-Jochem, F. Karouta and M.K. Smit

COBRA Inter-University Research Institute on Communication Technology
Eindhoven University of Technology
Faculty of Electrical Engineering, Opto-Electronic Devices Group
P.O.Box 513, 5600 MB Eindhoven, The Netherlands
Email: b.docter@tue.nl

Abstract

A novel fabrication process was developed to realize high quality SiO_x masks for Cl_2 based ICP etching of InP. First order DBR mirrors, 3 μm deep, were realized that can be used in photonic circuits. The process can be used in combination with conventional optical lithography, reducing production cost.

I. Introduction

Deep etched distributed Bragg reflector (DBR) gratings are very promising devices for InP/InGaAsP-based photonic integrated circuits (PICs). In theory, a first order deep etched grating can achieve reflectivity of more than 97%, within only a few grating periods [1]. The small size and high reflectivity makes the DBR grating an ideal building block for high-Q cavities [2]. These can be used to make ultra small, in-plane lasers that can be easily integrated in photonic logical circuits.

The realization of these sub-micrometer scale structures is very challenging. Being able to integrate the DBR mirrors with other photonic components adds additional restrictions to the fabrication process. We present a fabrication technique which is able to produce high quality 3 μm deep DBR gratings, using electron beam lithography and inductively coupled plasma (ICP) etching. The process is completely compatible with the conventional fabrication flow of both active and passive PICs [3].

II. Grating design

The first order DBR gratings are schematically shown in fig. 1. The air gaps in the DBR sections are about 390 nm wide and the lines are about 120 nm wide. This corresponds to ¼ of the wavelength in each medium. The p-InP cladding layer is sufficiently thick to avoid optical loss from the InGaAsP contact layer, which is necessary to integrate semiconductor optical amplifiers (SOAs) and optical phase shifters in the same chip. Because the gratings should be etched through the waveguide layer, an etch depth of at least 3 μm is required. Furthermore, the sidewalls should be smooth and vertical.

III. Etching process

To meet these requirements a Cl_2:Ar:H_2 ICP process was used. This process has a high etch rate (~2.5 μm/min) and the addition of H_2 results in good passivation of the sidewalls. The selectivity towards a PECVD deposited SiO_x mask layer is about 20:1. However, because of faceting effects on the mask,

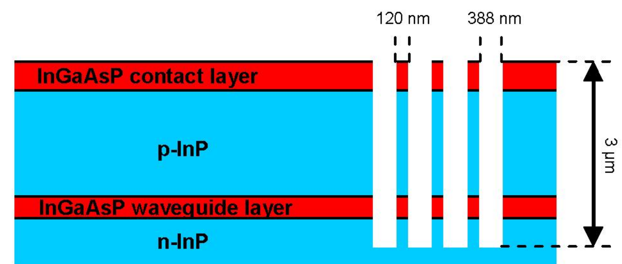

Fig 1: Schematic drawing of deep-etched DBR grating

which play a major role in the small DBR structures, this SiO_x layer needs to be at least 400 nm thick.

The grating structures are written using a Raith-150 electron beam lithography system. The typical thickness of common ZEP resist is 320 nm in this 30 kV system, which is not sufficient to accurately transfer a detailed pattern to the thick SiO_x layer, and therefore a metal inter-layer was introduced. In the next sections we will describe the use of aluminum in a lift-off process and chromium in an etching process.

VI. Aluminum lift-off

The aluminum process flow is shown in fig. 2. First a 200 nm PMMA layer is patterned using 20 kV e-beam lithography. The lower acceleration voltage increases the amount of forward scattering of the electrons while passing through the PMMA layer, providing a good profile for a lift-off process. 70 nm of aluminum is e-beam evaporated followed by a lift-off. Subsequently the aluminum is used as an etching mask to open the SiO_x layer. The selectivity between aluminum and SiO_x is approximately 1:13. This allows the thickness of the SiO_x layer to be well over 500 nm.

The high quality SiO_x pattern is used as a mask in a high power ICP etching process. The resulting DBR grating is shown in fig. 3. The ICP power was 1000W and the RF power was 120W. This gives very straight sidewalls. The roughness that is still visible on the waveguide is not caused by the etching process, but results from the aluminum lift-off

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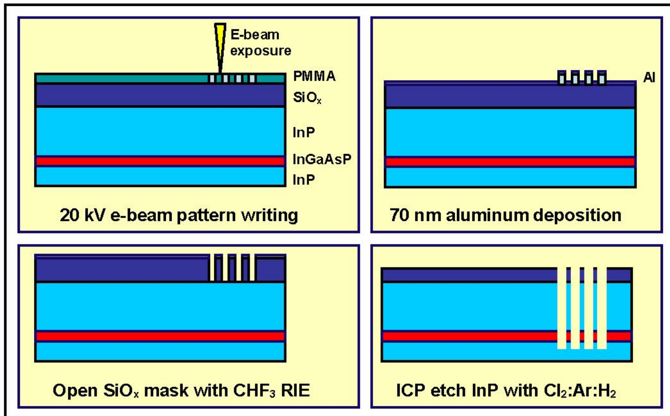

Fig 2: Aluminum lift-off process flow

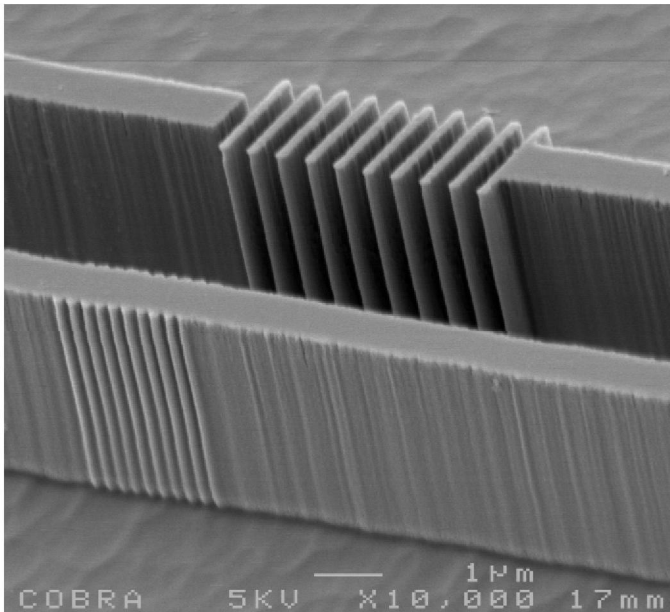

Fig 3: 4 μm deep DBR gratings in InP

process. It is expected that by using optical lithography for the waveguides this roughness will be reduced drastically.

V. Chromium etching process

We also investigated using chromium as an inter-layer material. Chromium is a well known material used in photo-lithography mask fabrication, because it has a smaller grain size than aluminum. It also has a high resistance towards the CHF_3 plasma that is used to open the SiO_x mask.

We also wanted to investigate whether an etching process gives better results than a lift-off process to define our metal mask. The process flow is shown in figure 4. First a 50 nm thick Cr layer was evaporated on the SiO_x mask and was covered by ZEP e-beam resist. Then the waveguide and grating pattern was written using a 30 kV e-beam. After development of the ZEP resist, the Cr layer was etched in an ICP system using a Cl_2:O_2 chemistry. This is a process that is also used in photo-mask fabrication and is known to etch Cr and CrO_x layers at about the same etch speed [4].

The Cr layer then serves as an etching mask for the opening of the SiO_x layer in a CHF_3 RIE process. The

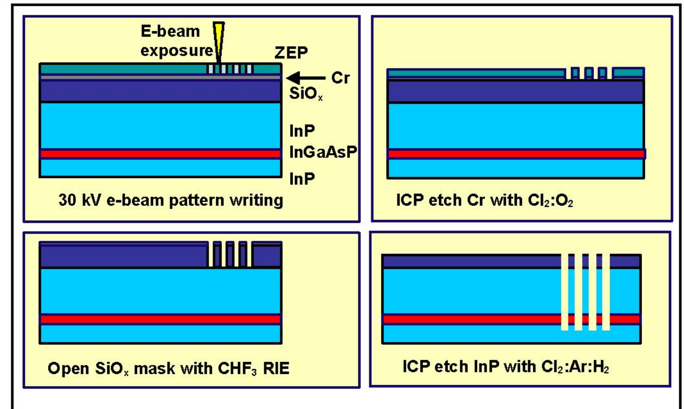

Fig 4: Process flow

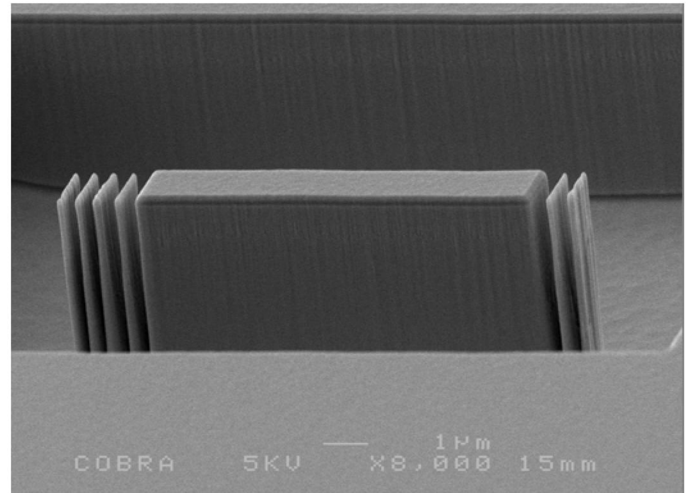

Fig 5: 6 μm deep DBR gratings in InP

selectivity is about 1:17. After removing the Cr mask, the pattern is then transferred into the InP by the same ICP process as described before.

A SEM image of the resulting structure is shown in fig 5. The waveguide has very smooth sidewalls and the roughness that was present in the aluminum lift-off process is not visible. The DBR sections however are still a little bit rough. This is caused by the fact that the ZEP is a positive e-beam resist, and therefore we have to write around the waveguide and DBR sections. This gives additional difficulties in applying the proximity effect correction, which was originally developed for photonic crystal structures, and is necessary when working with these relatively low acceleration voltage e-beam exposures.

Another problem with this e-beam system is that it uses small writing fields. The maximum write field size is 200 x 200 μm. Multiple write fields can be joined together, but between the written fields there are always stitching errors, which can cause unwanted reflections and losses.

To overcome both the proximity effect problem and the stitching errors, we developed a process that combines e-beam lithography with conventional optical lithography to fabricate high quality deep etched DBR gratings.

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VI. EBL – optical lithography combination

A top view of the process flow for the combined e-beam- and optical lithography process is given in fig. 6. First a 400 nm SiO_x mask is deposited by PECVD followed by a 50 nm e-beam evaporated Cr layer. The grating patterns are defined together with some alignment markers in a 320 nm thick ZEP layer by 30 kV e-beam writing (fig. 6a). This pattern is then transferred into the Cr layer by Cl_2:O_2 ICP etching.

Next the waveguides are defined in HPR504 optical photoresist, using the e-beam written alignment markers (fig. 6b). This pattern is then also etched into the Cr layer by the second Cl_2:O_2 etch step (fig. 6c). Note that with this type of gratings, the alignment of the optical mask is not very critical, since the grating pattern can be much wider than the waveguide. Also, the written pattern resembles much more a photonic crystal like structure and therefore the proximity effect correction algorithm works much better.

The rest of the processing is the same as mentioned in the previous section. The resulting structure is shown in figure 7.

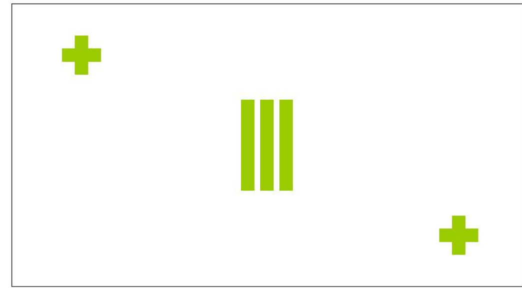

Fig. 6a: EBL pattern

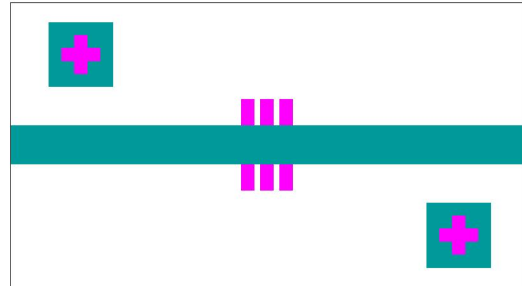

Fig. 6b: Waveguide pattern aligned to EBL pattern

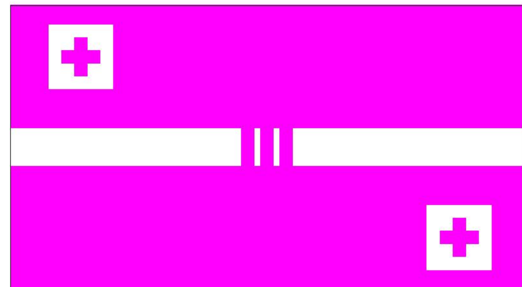

Fig. 6c: Final chrome mask

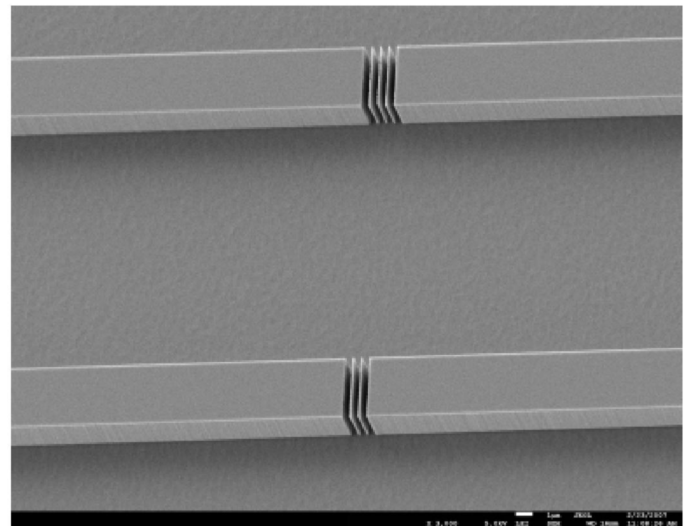

Fig.7: 3 and 4 section DBR mirrors in 4 µm wide waveguides.

VII. Conlcusion

We presented a novel fabrication method for high quality, deep etched DBR mirrors. It was shown that the addition of a metal inter-layer to the SiO_x hard mask provides an extremely high selectivity process. It was found that chromium is most suitable for this purpose.

The use of a thin chromium layer also enables us to use a combination of e-beam lithography and optical lithography. This does not only decrease writing time, it also avoids stiching errors and increases the accuracy of the proximity effect correction algorithm.

Furthermore the technology is fully compatible with other processing steps and therefore enables the use of deep etched DBR gratings as building blocks in future advanced photonic integrated circuits.

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