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Abstract

In this paper a physically based compact model is presented which includes the specific aspects of an SOI-LDMOS transistor, like the lateral doping gradient in the channel and the effect of the gate extending over the drift region. To have an accurate description at all bias conditions, the model is formulated in terms of surface potentials. In contrast to circuit-level models, the so-called internal drain voltage is solved analytically in terms of the terminal voltages. The resulting compact model thus combines the benefits of short computation times and robustness of explicitly formulated models with accuracy.

A comparison with data measured on transistors of different dimensions and operating temperatures shows that the model provides an accurate, well scaled description in all regimes of operation. Since all model expressions and their derivatives are continuous, the use of this compact model demonstrates improved convergence in circuit simulation.

1. Introduction

The use of high-voltage thin-film SOI devices provides a new and attractive technology for smart power integrated circuits in consumer and automotive applications [1]. Optimal design of these power circuits requires high-voltage device models for circuit simulation, which describe the device characteristics accurately over a wide range of biases and temperatures. With the LDMOS transistor being a frequently used component in these power circuits, inclusion of the specific SOI-LDMOS transistor aspects, like the lateral doping gradient in the channel, the effect of the extension of the gate over the drift region and the temperature behaviour, is essential.

A frequently followed approach in high-voltage modelling is to describe the LDMOS transistor on circuit level, by either a sub-circuit model [2-5] or a semi-numerical model [6-8]. In this approach internal nodes are solved *numerically*, either by the circuit simulator in case of a sub-circuit model, or in the model itself in case of a semi-numerical model. The disadvantage of this approach is that during circuit simulation these models give rise to an increase of computation time, or may have difficulty to reach convergence at all.

Furthermore, most of these models lack an accurate description of one or more specific device characteristics. For instance, in the models of [2,3,6] a conventional low-power MOS model with uniform doping has been taken for the graded channel, while in the sub-circuit model of [4] the drift region is only described by a linear resistor. The drawback of the models [7,8] is that the sub-threshold regime is not included, and that the potential drop over the channel varies only linearly with position.

Thus, most of the LDMOS models do not take into account the complete specific SOI-LDMOS behaviour. Combined with an enormous increase in computation time when a circuit-level model is used in circuit simulations, the need for the development of a *compact* model for an SOI-LDMOS transistor appears.

So far, only one compact model, that takes into account all the specific SOI-LDMOS aspects, has been developed [9]. The use of this compact model, however, has been found to be limited due to the occurrence of non-convergence in circuit simulation, as a result of discontinuities in the model expressions and their derivatives. Thus, even more important for successful IC-design is a compact model that is robust by having all its expressions and derivatives continuous, allowing fast, converging circuit simulations.

In order to combine accuracy with robustness, we have developed a new compact SOI-LDMOS model, for which the model developed in [9] served as starting point. Analogous to [9,5], the model is surface potential based, providing a precise current description at the so-called moderate inversion region. In addition to [9], we have further incorporated static feedback, and improved the description of drain-induced barrier lowering and the sub-threshold regime. Also the analytical solution of the internal drain voltage as well as the surface potential is obtained more consistently.

2. Model methodology

In Fig. 1 a cross-section of the LDMOS transistor is given for which the compact model is developed. The p-well is diffused under the gate and forms a graded inversion channel region. With the gate extending over the drift region, in the linear operating regime an accumulation layer forms in the drift region underneath the gate oxide. The internal drain Di represents the point

where the graded channel (of length L) turns into the lightly doped n$^-$ drift region (of length L_{dr}).

In our compact modelling approach, firstly the current I_{ch} through the inversion channel as well as the current I_{dr} through the drift region are derived, both in terms of the unknown internal drain voltage V_{Di}. In contrast to a circuit-level model, this internal drain voltage is solved *analytically* by equating I_{ch} to I_{dr}. In this way, the internal drain voltage, and subsequently the drain-to-source current $I_{DS} = I_{ch}$, are expressed explicitly in terms of the terminal voltages V_D, V_G, V_S and V_B.

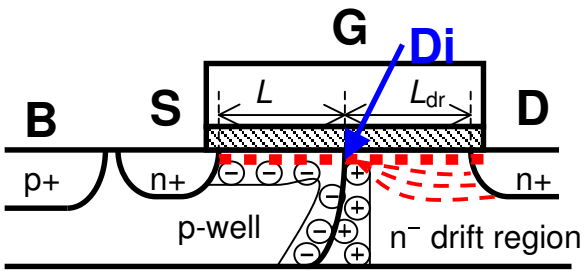

Figure 1. The SOI-LDMOS transistor

2.1. The graded channel current

To obtain an accurate and continuous description of the channel current and its derivatives in all operation regimes, a charge sheet MOSFET model approach based on surface potential formulations is taken. In order to reduce computation time, the explicit yet accurate relation between the surface potential and the terminal voltages according to [10] is used. In this way, the surface potentials ψ_{s0} at the source $x = 0$ and ψ_{sL} at the internal drain $x = L$ are respectively given by

$$\psi_{s0} = \Psi(V_{SB}, V_{GB,eff}), \quad \psi_{sL} = \Psi(V_{DiB}, V_{GB,eff}), \quad (1)$$

in which the explicit function Ψ is valid in all operating regimes ranging from weak to strong inversion. In contrast to the explicit relation used in [9], the function Ψ and all its first- and higher order derivatives are continuous. The effective gate-to-backgate potential is given by $V_{GB,eff} = V_{GB} - V_{FB}$, where V_{FB} denotes the flatband voltage.

To describe the effect of the decrease of doping along lateral position x, the p-well doping N_A is taken as [8]

$$N_A = N_{A0} \exp(-kx/L), \qquad 0 < x < L, \qquad (2)$$

where N_{A0} is the doping level at the source and k is the doping gradient model parameter. Hence, the body factor $\gamma = \sqrt{(2q\varepsilon_{Si}N_A)}/C_{ox}$ (with q the electronic charge, ε_{Si} the permitivity of silicon and C_{ox} the gate oxide capacitance per unit area) decreases from $\gamma_0 = \sqrt{(2q\varepsilon_{Si}N_{A0})}/C_{ox}$ at the source to $\gamma_L = \gamma_0 \exp(-k/2)$ at the internal drain. The surface potentials in (1) depend on the body factor γ.

With the device width denoted by W and the electron mobility by μ, the channel current is given by

$$I_{ch} = \frac{W\mu}{L}\left[\int_{\psi_{s0}}^{\psi_{sL}} (-Q_{inv})\,d\psi_s + \phi_T\,(Q_{invL} - Q_{inv0})\right], \quad (3)$$

where ϕ_T is the thermal voltage. Since the drift current contributes only significantly once the source is in strong inversion, the surface potentials ψ_{s0} and ψ_{sL} are calculated with $\gamma = \gamma_0$. With the strong inversion charge Q_{inv} per unit area given by

$$Q_{inv} = -C_{ox}\left(V_{GB,eff} - \psi_s - \gamma\sqrt{\psi_s}\right), \quad (4)$$

this charge also depends on the lateral position via the body factor γ. By taking in (4) the body factor linearly dependent on ψ_s following [9], and subsequently substituting (4) into the drift current term of (3), we arrive, by use of various Taylor expansions, at

$$I_{ch} = \frac{W\mu C_{ox}}{L}\left(\overline{V_{inv0}} - \tfrac{1}{2}(1+\delta)\Delta\psi_s\right)\Delta\psi_s, \quad (5)$$

where

$$\overline{V_{inv0}} = V_{GB,eff} - \psi_{s0} - \bar{\gamma}\sqrt{\psi_{s0}},$$
$$\bar{\gamma} = (\gamma_0 + \gamma_L)/2, \qquad \Delta\psi_s = \psi_{sL} - \psi_{s0}, \quad (6)$$
$$\delta = \frac{\gamma_0}{2\sqrt{V_1 + \psi_{s0}}}, \qquad V_1 = 1.$$

Inclusion of mobility reduction due to the vertical as well as the lateral electrical field according to

$$\mu = \frac{\mu_0}{F_{mob\perp}\,F_{mob//}}, \qquad F_{mob//} = 1 + \theta_3\,\Delta\psi_s,$$
$$F_{mob\perp} = 1 + \theta_1\left(V_{inv0} + \eta_{mob}V_{dep0}\right), \quad (7)$$
$$V_{inv0} = V_{GB,eff} - \psi_{s0} - \gamma_0\sqrt{\psi_{s0}}, \quad V_{dep0} = \gamma_0\sqrt{\psi_{s0}},$$

with θ_1, θ_3 and η_{mob} being model parameters, yields the graded channel current in terms of the surface potentials. In the model, $\beta = W\mu_0C_{ox}/L$ is taken as a parameter.

In strong inversion the potential drop $\Delta\psi_s$ approximately equals V_{DiS}. Hence, in saturation, where $\partial I_{ch}/\partial\Delta\psi_s = 0$ holds, the potential drop $V_{DiS} = V_{DiS,sat}$ is given by

$$V_{DiS,sat} = \frac{2\,\overline{V_{inv0}}/(1+\delta)}{1 + \sqrt{1 + 2\theta_3\,\overline{V_{inv0}}/(1+\delta)}}. \quad (8)\,\mathrm{I}$$

In the linear regime, on the other hand, the potential drop $\Delta\psi_s \cong V_{DiS}$ will be solved by equating I_{dr} to I_{ch}, in which the mobility reduction term $F_{mob//}$ is neglected. In this way, we obtain a second order polynomial for the channel current in terms of the unknown potential drop V_{DiS}. Subsequently, after V_{DiS} in the linear regime is solved, we incorporate saturation by taking an effective potential drop $V_{DiS,eff}$ according to [11]

$$V_{DiS,eff} = \frac{V_{DiS}V_{DiS,sat}}{\left(V_{DiS}^4 + V_{DiS,sat}^4\right)^{1/4}}. \quad (9)$$

In this way, $V_{DiS,eff}$ results smoothly in the minimum of V_{DiS} and $V_{DiS,sat}$. Finally, the surface potential ψ_{sL} is calculated by using $V_{DiB} = V_{SB} + V_{DiS,eff}$ in (1). To obtain an accurate expression for the sub-threshold current, the term $(Q_{invL} - Q_{inv0})$ in (3) is taken according to [10].

2.2. The drift region current

For devices with the drift region length L_{dr} of the same order of magnitude as the inversion channel length L, the

channel current saturates before the onset of depletion in the drift region [9]. In the linear operating regime, the drift region current I_{dr}, under neglect of the diffusion current, is thus given by

$$I_{dr} = \frac{W\mu_{dr}}{L_{dr}} \int_{V_{Di}}^{V_D} Q_b \mathrm{d}V - \frac{W\mu_{acc}}{L_{dr}} \int_{V_{Di}}^{V_D} Q_{acc} \mathrm{d}V, \qquad (10)$$

in which the first term is the current through the bulk of the drift region and the second one the current through the accumulation layer. Here, μ_{dr} is the electron mobility through the bulk, while μ_{acc} is that through the accumulation layer. Furthermore, Q_b represents the amount of dopants per unit area in the bulk of the drift region and Q_{acc} the charge per unit area in the accumulation layer, respectively given by

$$Q_b = qN_D t_{Si} - Q_{depB},$$
$$Q_{acc} = -C_{ox}\left(V_G - V - V_{FB}^{dr}\right). \qquad (11)$$

Here, N_D is the doping level of the drift region, while t_{Si} is its thickness. In contrast to [9], we take the effect of depletion at the pn-junction between p-well and n$^-$ drift region into account, via the charge per unit area Q_{depB}. For small V_{DiS} this charge reads

$$Q_{depB} = \gamma_{dr} C_{ox} \sqrt{\frac{\gamma_0^2}{\gamma_0^2 + \gamma_{dr}^2}} \sqrt{V_{SB} + \phi_0}, \qquad (12)$$

in which $\gamma_{dr} = \sqrt{(2q\varepsilon_{Si}N_D)}/C_{ox}$ is the body factor of the drift region, and ϕ_0 denotes the built-in potential of the pn-junction. Substitution of (11) and (12) into (10) yields

$$I_{dr} = \frac{1 - f_{dep}}{R_{on}} V_{DDi} + \frac{\beta_{acc}}{2F_{mob,acc}} \left[\left(V_{GDi} - V_{FB}^{dr}\right)^2 - \left(V_{GD} - V_{FB}^{dr}\right)^2 \right], \qquad (13)$$

in which the electron mobility in the accumulation layer is taken according to

$$\mu_{acc} = \frac{\mu_{acc0}}{F_{mob,acc}},$$
$$F_{mob,acc} = 1 + \theta_{1,acc}\left(\frac{V_{GS} + V_{GD}}{2} - V_{FB}^{dr}\right). \qquad (14)$$

Here, $\beta_{acc} = W\mu_{acc0}C_{ox}/L_{dr}$, $R_{on} = L_{dr}/[W\mu_{dr}(qN_D t_{Si} - Q_{depB0})]$ and θ_{1acc} are model parameters, while the function f_{dep} is given by

$$f_{dep} = \frac{Q_{depB} - Q_{depB0}}{qN_D t_{Si} - Q_{depB0}},$$
$$Q_{depB0} = Q_{depB}\big|_{V_{SB}=0}. \qquad (15)$$

Thus, we have derived a second-order polynomial of the drift region current I_{dr} in terms of V_{Di}, valid in the linear operating regime, provided that V_{GD}-$V_{FB}^{dr} > 0$.

2.3 Additional effects

In the final current calculation of I_{ch}, second order effects like channel length modulation, drain-induced barrier lowering and static feedback are incorporated. Also, the effect on drain and bulk current of avalanche occurring in the MOSFET region is taken into account. Finally, the temperature dependence of the relevant model parameters is included.

3. Results

We have characterized a 12V SOI-LDMOS transistor using our compact model. In addition, a thermal sub-circuit is used in which the temperature rise due to this self-heating is calculated [3]. In the figures, symbols correspond to the measurement data, while the solid lines represent our compact model.

In Fig. 2 the drain current is plotted in the sub-threshold regime at various backgate and drain voltages. As a result of the surface potential formulations, the model describes the current adequately and in a smooth manner also at the transition from the weak- to strong inversion regime. In Fig. 3 the accurateness at this transition is again observed in the current and transconductance. In this figure we observe that the model is also accurate at the high gate voltages, where the effect of the gate extending over the drift region is significant. In Fig. 4 the drain current and output conductance at various gate voltages are plotted. We observe that also the saturation regime is well described by our SOI-LDMOS model.

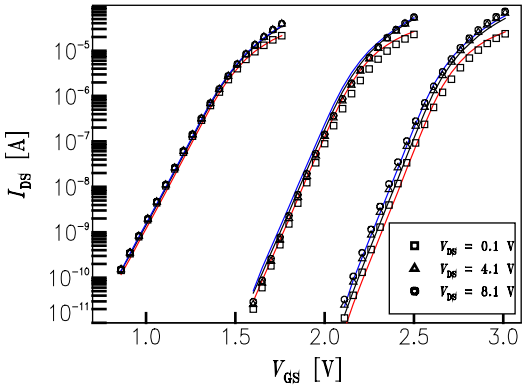

Figure 2. Drain current I_{DS} for V_{SB} = 0, 1 and 2 V.

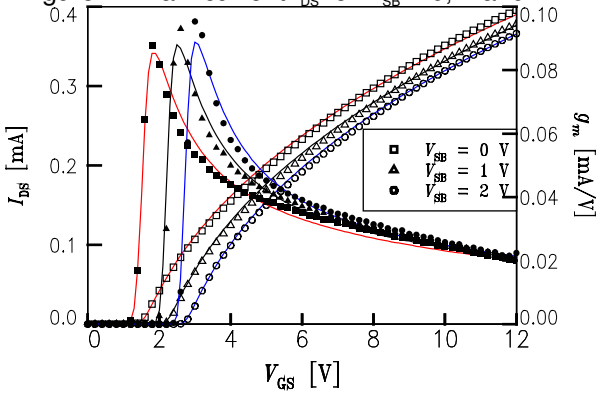

Figure 3. Drain current I_{DS} (open symbols) and transconductance g_m (solid symbols) in the linear operating regime, at V_{DS} = 0.1 V.

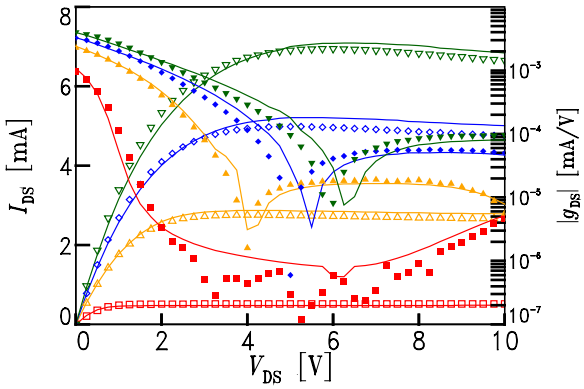

Figure 4. Drain current I_{DS} (open symbols) and output conductance g_{DS} (solid symbols) for V_{GS} = 3, 6, 9 and 12 V, and V_{SB} = 0 V.

Also important is the fact that the model predicts the behaviour over a whole range of device widths, lengths and temperatures. In Fig. 5 the model parameters β, β_{acc}, R_{on} and θ_3 are plotted versus temperature T on a logarithmic scale. We observe that these parameters indeed exhibit the power-law behaviour as expected from the physics. In Fig. 6 the scaling of parameters β, β_{acc}, and R_{on} with drawn mask width W_{drawn} is demonstrated.

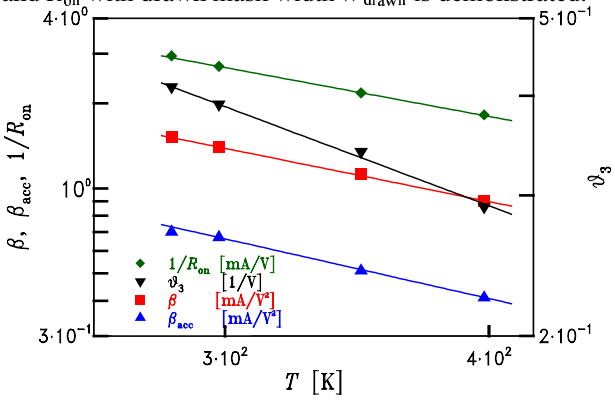

Figure 5. Parameter scaling with temperature T

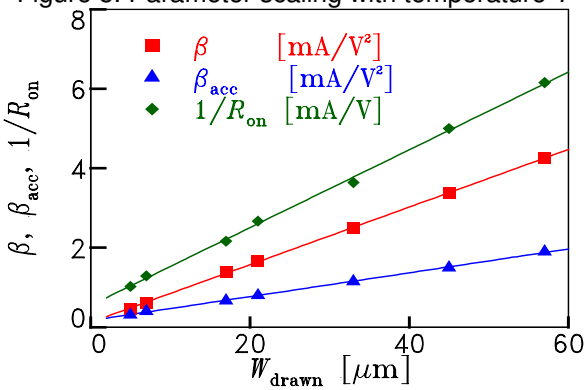

Figure 6. Parameter scaling with width W_{drawn}.

4. Conclusions and discussion

A surface-potential-based compact SOI-LDMOS transistor model, based on an analytical solution of the internal drain voltage in terms of the terminal voltages, has been presented. By the use of the explicit relation according to [10] between surface potentials and terminal voltages, an accurate current description has been obtained, valid in all operating regimes ranging from sub-threshold to strong inversion, in both the linear and saturation regime. By having all expressions and their derivatives continuous at all bias conditions, our compact model has shown an improved convergence behaviour during circuit simulations. Also the use of this compact model in a sub-circuit model to describe higher voltage LDMOS devices has been proven to be successful.

5. Acknowledgements

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