Timing recovery techniques for digital recording systems

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to my parents
and my family

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abstract — This thesis is devoted to the development of timing recovery techniques for digital recording systems. The thesis begins with a detailed review and discussion of timing recovery structures, requirements, performance measures, timing error detector (TED) algorithms, and timing acquisition issues. The main contributions include five parts. The first part examines the timing sensitivity of read channel detectors, and develops a new analytical approach for evaluating the performance under static and random timing errors. The second part examines the TED efficiencies, develops an improved TED for jitter minimization, and studies optimality issues for timing acquisition. The third part investigates false lock and hang up problems, and develops two novel acquisition techniques. The fourth part presents the timing recovery loop design and implementation for an experimental read channel detector. The fifth part develops a new asynchronous equalizer adaptation structure with fully digital interpolative timing recovery (ITR) for digital optical recording systems.

SUMMARY

A critical part of data storage systems is the read-write channel, which consists of the electronic circuits needed for writing the user-supplied data into the storage medium and for reliably recovering the written data. A properly designed read-write channel has the potential to enhance the recording density and data rate capabilities of a given head-medium combination. Equalizer, data-detector and timing recovery circuitry are among the most important blocks of a read-write channel. Usually, the tasks of equalization and detection receive considerable attention from researchers. As recording channels become more efficient in terms of modulation code, bandwidth and storage density, the task of timing recovery becomes more difficult and, at the same time, increasingly critical for reliable data recovery. The problem of timing recovery is concerned with the determination of the optimum sampling instants for the readback signal. The research work that has been undertaken in the thesis deals with the timing recovery issues in read-write channels.

This thesis is devoted to the study and development of timing recovery techniques for digital recording systems. It investigates the structure and performance of timing recovery schemes, and develops new timing recovery schemes for magnetic and optical recording applications. The thesis contains eight chapters. Chapter 1 gives a brief introduction to digital recording technology and a review of read-write channel techniques. It concludes with the motivation, contributions and organization of the thesis. Chapter 2 gives a detailed review of timing recovery, highlighting the different possible structures, requirements, and performance measures. It also discusses the generic timing error detector (TED) algorithms and the main issues that arise during timing acquisition. Analyses and simulation results support the discussions, wherever possible. Chapters 3 to 7 describe the main new research contributions made during the course of this Ph.D. work. Chapter 8 concludes the thesis with some remarks on directions for further work.

Chapter 3 investigates the timing sensitivity of partial response (PR) Viterbi detectors and decision feedback equalization (DFE) detectors, and develops an analytical approach to evaluate the performance in the presence of static and random timing errors. Chapter 4 examines the efficiencies of existing and proposed TED algorithms for partial response and DFE recording systems. It also develops a marginal detection based TED for minimizing jitter in the multi-level DFE (MDFE) detector and analyzes its phase noise performance. Further, it examines the optimality of the preamble and TED used for timing acquisition in MDFE. Chapter 5 investigates the problem of timing acquisition in DFE detectors. It develops two novel fast acquisition techniques that do not suffer from hang up and false lock problems, even in the presence of large initial errors in timing, gain and DC offset. Chapter 6 describes the design and implementation of a practical timing recovery system, which is designed and prototyped in ECL (emitter-coupled logic) discrete-components, for a 100 Mb/s experimental MDFE read channel (channel data rate is 150 Mb/s). Performance evaluations of the system based on bench and spinstand tests are also presented.

The focus of the development of the algorithms and systems presented in Chapters 3 to 6 is on magnetic recording, even though these are also applicable with minor modifications to optical recording. In contrast, the focus of Chapter 7 is on optical recording. In Chapter 7, a new and attractive architecture for fully digital zero-forcing based equalizer adaptation and interpolative timing recovery (ITR) is developed. The development of algorithms and systems in Chapters 3 to 7 is supplemented with computer simulation results. These simulation results are used for demonstrating the effectiveness of the proposed algorithms and for corroborating the analytical developments.

CONTENTS

GLOSSARY

Abbreviations

A/D :	Analog-to-Digital converter.
AGC :	Automatic Gain Control.
AWG :	Arbitrary Waveform Generator.
AWGN :	Additive White Gaussian Noise.
BECM :	Band-Edge Component Maximization.
BER :	Bit Error Rate.
CAD :	Computer Aided Design.
CD :	Compact Disc.
D/A :	Digital-to-Analog Converter.
DA :	Data-Aided.
DC :	Direct Current.
DD :	Decision-Directed.
DDFE:	Dual Decision Feedback Equalization.
DFE :	Decision Feedback Equalization.
DFT :	Discrete-time Fourier Transform.
DPO :	Digital Phosphor Oscilloscope.
DVR:	Digital Video Recording
DSP :	Digital Signal Processor.
DVD :	Digital Versatile Disc.
ECC :	Error Control Coding.
ECL :	Emitter-Coupled Logic.
EER :	Error Event Rate.
EPR4 :	Extended class IV Partial Response.
E^2PR4 :	Extended order-2 class IV Partial Response.
FBF :	Feedback Filter.
FDTS/DF :	Fixed Delay Tree Search with Decision Feedback.
FEQ :	Forward Equalizer.
FIR :	Finite Impulse Response.
HDD :	Hard Disk Drive.
IC :	Integrated Circuit.
IIR :	Infinite Impulse Response.
ISI :	Intersymbol Interference.
ITP :	Interpolation.
ITR :	Interpolative Timing Recovery.

LF :	Loop Filter.
LPF :	Low-Pass Filter.
LMS :	Least-Mean-Square.
MAP :	Maximum A Posteriori.
MDFE :	Multi-level Decision Feedback Equalization.
MLSD :	Maximum Likelihood Sequence Detector.
ML :	Maximum-Likelihood.
MMSE :	Minimum Mean-Square Error.
MR:	Magneto-Resistive.
MSE :	Mean-Square Error.
MSB :	Most Significant Bit.
MT :	Modified Threshold.
NCO :	Numerically Controlled Oscillator.
NDA :	Non-Data-Aided.
NDD :	Non-Decision-Directed.
NRZ :	Non-Return to Zero.
NRZI :	Non-Return to Zero Inverse.
PAM :	Pulse-Amplitude modulation.
PCB :	Printed Circuit Board.
PDF :	Probability Density Function.
PLL :	Phase-Locked Loop.
PR :	Partial Response.
PR4 :	class IV Partial Response.
PR4-VD :	class-IV Partial-Response with Viterbi Detection.
PRML :	Partial Response with Maximum Likelihood.
PSD :	Power Spectral Density.
RC :	Resistor-Capacitor.
RF :	Radio Frequency.
RLL :	Run-Length-Limited.
RMS :	Root-Mean-Square.
SNR :	Signal-to-Noise Ratio.
SRC :	Sample Rate Conversion.
STI :	Spatio-Temporal Interpolation.
TA :	Thermal Asperity.
TED :	Timing Error Detector.
VCO :	Voltage Controlled Oscillator.
VD :	Viterbi Detector.
VGA :	Variable Gain Amplifier.
ZCD :	Zero-Crossing Detection.
ZF :	Zero-Forcing.

Often Used Symbols

a_k : RLL coded data bit sequence in alphabet $a_k \in \{-1, 1\}$.

$A(e^{j2\pi\Omega})$: PSD of data a_k .

b_k : RLL encoder output in alphabet $b_k \in \{0, 1\}$.

B_l : PLL equivalent noise bandwidth.

(d, k) : two constraint-parameters of RLL codes.

d_k : desired (reference) sequence.

D_{ch} : channel bit density.

D_u : user bit density.

e_k : error sequence.

f : frequency variable in units Hz.

$h(t)$: channel bit response.

$\tilde{h}(t)$: isolated transition response.

k : discrete-time index in units T.

K_d : TED gain, i.e., slope of $\rho(\tau)$ at the origin $\tau = 0$.

$n(t)$: channel additive noise.

$N_o / 2$: PSD of two-sided 'white' noise.

pw_{50} : pulse width (in seconds) at 50% base-to-peak amplitude of $\tilde{h}(t)$.

$r(t)$: readback (replay) signal at the channel output.

R : RLL modulation encoder rate, $0 < R \le 1$.

SNR_{loop} : PLL loop signal-to-noise ratio.

SNR_m : signal-to-noise ratio in the matched filter bound sense.

$S_u(e^{j2\pi\Omega})$: PSD of noise component u_k at the TED output.

t : continuous-time index in seconds.

t_k : k^{th} sampling instant in seconds.

T : duration of one bit in seconds.

u_k : noise component at the TED output.

y_k : discrete-time detector input.

y_k' : sampled derivative of signal $y(t)$ with respect to t at instants t_k .

γ : TED efficiency.

Γ : time-constant of the first-order PLL in units T .

$\rho(\tau)$: timing function, i.e. TED characteristics.

ς : damping factor of the continuous-time second-order PLL.

ς^d : damping factor of the discrete-time second-order PLL.

θ_k : input-referred phase noise of the PLL.

σ_θ^2 : variance of θ_k .
τ : timing phase error in units *T*.
ϕ : unknown channel delay in units T .
χ_k : TED output.
ψ : sampling phase in units T .
ω_n : natural frequency of the continuous-time second-order PLL.
ω_n^d : natural frequency of the discrete-time second-order PLL.
Ω : normalized frequency variable in units 1/*T*, i.e. $\Omega = fT$.

Notational Conventions

D : one-bit interval delay operator.
$E[x]$: expected value of x .
$\mathrm{Im}[x]$: imaginary part of a complex number x .
P : matrices or vectors are boldfaced.
$\mathbf{P}^{-1}$: matrix inverse.
$\mathbf{P}^{\mathrm{T}}$: matrix or vector transpose.
$Q(x)$: *Q*-function, i.e., $Q(x) = \left(\sqrt{2\pi}\right)^{-1} \int_x^\infty \exp\left(-u^2/2\right) du$.
$r_x(l)$: autocorrelation function of x for lag l .
$\mathrm{Re}[x]$: real part of a complex number x .
s_k : sample element of sequence $\{s_k\}$ at instant k .
$\{s_k\}$: discrete-time sequence.
$|x|$: absolute value (magnitude) of x .
$\lfloor x \rfloor$: biggest integer not exceeding x .
x^* : conjugate of a complex number x .
$\otimes$: convolution operator.
$\oplus$: modulo-2 addition operator.
$\delta(t)$: Dirac's delta function.
δ_k : discrete-time delta function.

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CHAPTER 1

INTRODUCTION

In this chapter, we first give a brief introduction to digital recording systems such as magnetic and optical systems. Following this, we present an overview of the key techniques used for data recovery in magnetic recording systems[1]. Our emphasis in this overview is on the role of coding and signal processing techniques in digital recording systems. Thereafter, we present the motivation for the work reported in this thesis. The chapter concludes with a brief description of the contributions in each chapter of the thesis.

1.1 Introduction to Digital Recording Technology

The advent of the information era and the fast growth of information technology have resulted in an enormous demand for the storage of digital data, along with demands for processing and transmission in huge volumes and/or at high speeds. The recording density and transfer rate of storage devices have had to increase at dramatically fast rates to accommodate this growing demand. For instance, the areal density and transfer rate of magnetic hard disk drives were about 20 Mb/in^2 and 24 Mb/s, respectively, in 1986 [1]. By the beginning of 2001, these had become 50 Gb/in^2 and 700 Mb/s, respectively [2] [3]. Although this explosive growth has been mainly due to the technological improvements made in the design of heads and disk-media, sophisticated coding and signal processing techniques, as well as accurate servo control algorithms, have also played a significant role [4] [5]. The potential of coding and signal processing techniques to significantly enhance the storage capacity has been proved repeatedly in the past. For a given head-medium combination, the use of better coding and signal processing techniques allows more bits to be packed into a given area in the medium, resulting in an increase in storage density from the improved reliability. A classic example of this is the increase in density that resulted from substituting partial response detection for peak detection in hard disk drives in the early 1990s [6] [4] [5]. As the developments in integrated circuits (IC) technology allow ever more complex functions to be implemented at affordable costs, signal processing techniques are going to play an increasingly important role in data storage systems.

[1] The review in Chapters 1 and 2 is aimed at magnetic recording systems. This is because the developments in Chapters 3 to 6, which constitute the bulk of the thesis, assume magnetic recording systems. Chapter 7, which deals with optical systems, will also include the required review on optical recording.

A digital recording system very much resembles a synchronous digital baseband communication system. Whereas communication systems transport information from one location to another, recording systems do it from one time to another. The common goal of both systems is to eventually retrieve the transmitted or stored information as accurately as possible [7]. The information is in the form of binary data. In baseband systems, no carrier modulation is used for matching the channel and data characteristics. Instead, these systems typically use modulation codes to adapt the data to the channel characteristics [8]. The received signal is processed using equalization, detection and timing recovery techniques for recovering the original digital data. Because of the operational and system level similarities between digital storage systems and digital baseband communication systems, the techniques developed for transmission and reception in communications have been widely exploited in storage systems.

The principles of digital magnetic recording and digital optical recording form the basis of most of the data storage systems that are in use currently. Magnetic recording systems, in particular hard disk drives (HDD), prevail for high volume and high-speed storage applications. On the other hand, optical recording systems, such as compact disc (CD), digital versatile disc (DVD), and their advanced generations, prevail for removable storage applications. Because of the continuous demand from customers for storage systems capable of high densities and/or high data rates, the research efforts in the last decade on improving the storage technology have been very aggressive. As a result, for example, areal densities of 100 Gb/in^2 and data rates of more than 1 Gb/s will be realized very soon in magnetic recording [9] [10]. In fact, researchers are being forced to make revolutionary changes in technology to sustain the advancements in storage capabilities, since the existing technologies are fast approaching their physical limits [11].

A critical part of data storage systems is the read-write channel, which consists of the circuits and techniques needed for writing the user-supplied data into the storage medium and for reliable recovery of the written data. A properly designed read-write channel has the potential to enhance the recording density and data rate capabilities. The research work that has been undertaken in this thesis deals with timing recovery issues in read-write channels. To motivate the work, we first present a system-level overview of the read-write channel and the various key techniques developed for implementing each of its subsystems. For the sake of convenience, we present this review in the context of digital magnetic recording systems.

1.2 Overview of Read-Write Channel Techniques for Digital Magnetic Recording Systems

Fig.1-1 shows the block schematic of a magnetic recording system, highlighting the read-write channel part of the whole system. As shown, the read-write channel involves a write channel and read channel. These are similar in functionality to the transmitter and receiver, respectively, in a communication system. The write channel accepts the input binary data and converts it into a form suitable for writing into the storage medium. The read channel recovers the original data by processing the output of the read head in accordance with certain algorithms. Throughout the thesis, the phrase ‘recording channel’ refers to the cascade of write circuits, write head, storage medium, and the read head.

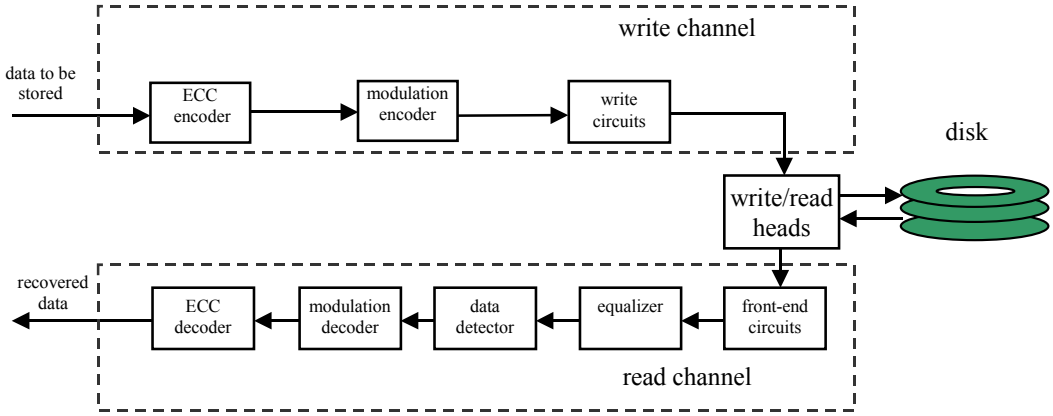

Fig.1-1: Block schematic of a magnetic recording system. The blocks enclosed by the dashed boxes constitute the read-write channel of the recording system.

We now briefly describe the functions of each block shown in Fig.1-1. The ECC (error control coding) encoder uses special coding schemes to introduce error detection and correction capability into the input binary data. The ECC decoder uses this capability for detection and correction of errors during data recovery [12] [13]. The modulation encoder, on the other hand, is used for matching the data to the recording channel characteristics, and to help in the operation of the various control-loops (e.g. timing/gain recovery) in the read-channel [14] [15] [16]. The write circuits convert the binary output data of the modulation encoder to a write-current waveform. Each current pulse is properly shaped and positioned (through pulse shaping and write precompensation) to counteract the nonlinear distortions in the recording process. These distortions arise from the bandwidth limitations of the write path and the demagnetization fields in the medium [17] [8] [18]. The write-current waveform causes the write-head to produce magnetic flux which magnetizes the storage medium in one of the two directions, thereby recording the data.

The electrical signal generated by the read-head, in response to the magnetization pattern in the medium, is processed by the frond-end circuits which condition the replay signal (e.g., amplify, limit noise bandwidth, regulate dynamic range, etc) prior to equalization [19]. The equalizer shapes the signal according to certain pre-chosen criteria [20] [21] [22] [23] [8] so that the data detector is able to recover the binary data from the equalized signal with as few errors as possible [24] [6] [25] [26]. The modulation and ECC decoders operate on the output bits of the data detector to give the estimate of the original data that was input to the storage system. Not shown explicitly in Fig.1-1 are the control loops required for doing timing recovery [27] [28], gain control [19] [29], DC offset cancellation and adaptive equalization [30] [26].

In the rest of this section, we further elaborate on selected parts of the read-write channel, namely, modulation codes, equalization, and detection, since these will be used extensively in this thesis. The problem of timing recovery, which is the main subject of the thesis, is briefly introduced in Section 1.3. A detailed review on timing recovery will be given in Chapter 2.

1.2.1 Modulation codes

As mentioned above, modulation codes are used for matching the characteristics of the data to those of the recording channel [8] [31]. Run-length-limited (RLL) codes are the most popularly used modulation codes in digital magnetic and optical recording systems [32].

In this thesis, the output sequence $\{b_k\}$, $b_k \in \{0,1\}$, of the RLL (modulation) encoder is assumed to be in the NRZI (non-return to zero inverse) representation [33]. That is, $b_k = 1$ implies a transition in the medium magnetization at the k^{th} bit instant, whereas $b_k = 0$ implies no transition. To generate the write current from the transition sequence $\{b_k\}$, a precoder is used to convert the NRZI bits $\{b_k\}$ into NRZ (non-return to zero) representation $\{b'_k\}$, where $b'_k = 1$ and $b'_k = 0$ imply the two directions of magnetization (i.e., write current polarities) instead of the presence and absence of transitions [33] [15]. This precoding is done as

$$b'_k = b'_{k-1} \oplus b_k \tag{1.1}$$

where ' $\oplus$ ' indicates modulo-2 addition. The write current polarity is given by

$$a_k = 2b'_k - 1 \tag{1.2}$$

so that $a_k \in \{-1, 1\}$.

RLL codes are also known as (d, k) codes. The parameters d and k specify the constraints on the minimum and maximum runs of consecutive zeros between two ones in the coded sequence b_k. The d-constraint, when $d > 0$, helps to increase the minimum spacing between transitions in the medium. This, in turn, helps to reduce the linear as well as nonlinear interactions (called intersymbol interference) among the data bits recorded in the medium [34]. The k-constraint limits the maximum transition spacing and ensures that the control loops (e.g. timing, gain and equalization) are updated frequently enough to maintain the loops in good condition. The k-constraint also helps to reduce the path memory requirement as well as to avoid certain catastrophic error events in Viterbi-algorithm-based data detectors [24] [25]. The benefits provided by the d and k constraints carry a price tag in the form of redundancy added to the coded data stream. This redundancy is characterized by a parameter called code-rate that is defined as $R=p/q$, $0 < R < 1$, specifying that groups of p data bits at the encoder input are coded into groups of q bits at its output. Clearly, the code-rate decreases with increase in d or decrease in k. An important disadvantage of coding is that it decreases the signal-to-noise ratio (SNR) in the readback signal. The lower the code-rate is, the greater will be the reduction in SNR [35] [36]. Hence, it is important to design the data detector to minimize any further reduction of SNR.

In practical recording systems, the d-constraint is restricted to 0, 1 or 2, and the k-constraint ranges between 2 and 10. The most popular RLL codes are the rate 1/2 (1, 3) code used in floppy disk drives [15], rate 8/17 (2, 10) code used in CD [32], rate 8/16 (2, 10) code used in DVD [37], rate 1/2 (2, 7) and 2/3 (1, 7) codes used in earlier hard disk drives [15] [32], and several d=0 codes such as rate 8/9 (0,4/4) [25], 16/17 (0, 6/6) [38], and 8/9 (0,11) codes [39] used in hard disk drives. The rate 16/17 (0, 6/6) and 8/9 (0, 4/4) codes belong to the class of RLL codes whose constraints are specified as (d, G/I), where d and G have the same meaning as d and k discussed above. The I-parameter describes an additional constraint on the maximum run-length of zeros in the odd and even interleaved sequences [16]. More recently, high-rate codes combined with parity bits in conjunction with parity-based post-processing schemes have been widely used for improving error performance and densities [40] [41] [42]. These codes have the advantage of minimizing performance degradation due to rate loss and error propagation at the modulation decoder. For example, in the disk-drive industry, to enhance density and performance, the rates of d=0 modulation codes have steadily been increasing over the years, from initially, rate 8/9 and 16/17 codes to currently 19/20 [43], 32/33, 64/65 [42], and

96/100 [42]. These codes keep the *d*-constraint to zero and allow the *k*-constraint to vary between 4 and 8, thus providing the benefits of (*d*, *k*) codes while largely reducing the code redundancy.

1.2.2 Equalization and detection techniques

A mathematical model for the readback signal at the read head output can be given as [44] [6]

$$r(t) = \sum_{k=-\infty}^{\infty} a_k h(t - kT) + n(t) \tag{1.3}$$

where $\{a_k\}$, $a_k \in \{-1, 1\}$, is the sequence of RLL coded bits in NRZ format, $h(t)$ is the response of the combination of write-head, medium and read-head to the NRZ input bit '+1', and $n(t)$ is the noise due to read-head and electronics. The noise $n(t)$ is modeled as white Gaussian with power spectral density $N_o / 2$ Watts/Hz. Here, '*t*' denotes time and '*T*' denotes the duration of one bit a_k. The dispersion of each bit a_k, which is caused by the bit response $h(t)$, normally results in linear intersymbol interference (ISI) in the readback signal since the duration of $h(t)$ is much larger than *T*. The problem of ISI worsens with increase in recording density. Recording density may be characterized by the user bit density D_u, defined as the ratio pw_{50} / T_u, where pw_{50} is the pulse-width at 50% of the peak amplitude of $\tilde{h}(t)$, the isolated transition response, and T_u is the duration of one user bit[2]. Clearly, $T_u = T / R$, where R is the code-rate of the RLL encoder. The bit response and transition response are related by [6]

$$h(t) = \left(\tilde{h}(t) - \tilde{h}(t - T)\right) \Big/ 2 . \tag{1.4}$$

The readback signal can also be expressed in terms of $\tilde{h}(t)$ as [6]

$$r(t) = \sum_{k=-\infty}^{\infty} a'_k \tilde{h}(t - kT) + n(t) \tag{1.5}$$

where $a'_k = (a_k - a_{k-1}) / 2$ and $a'_k \in \{-1, 0, 1\}$. For instance, in longitudinal magnetic recording, a commonly used model for the transition response $\tilde{h}(t)$ is the Lorentzian pulse given by [33] [44] [45]

[2] In this thesis, we do not include ECC encoder and decoder. Hence, the raw data appears directly at the input of the RLL encoder. Following existing practices, we call the data bits at the input and output of the RLL encoder user bits and channel bits, respectively [6] [33]. Further, the transition response $\tilde{h}(t)$ is the response of the recording channel when the NRZ data pattern $\{a_k\}$ is of the form $\{\cdots, -1, -1, -1, +1, +1, +1, \cdots\}$.

$$\tilde{h}(t) = \frac{V_{op}}{1 + \left(\frac{2t}{pw_{50}} \right)^2} \tag{1.6}$$

where V_{op} is the base-to-peak amplitude of $\tilde{h}(t)$. The readback signal will be a series of such pulses corresponding to the transitions a'_k in the magnetization pattern. The peak detector, which was the first data detector for digital magnetic recording systems, detects the data bits by identifying the locations of the peaks of these pulses [46]. When recording density increases, pulses increasingly overlap, and it becomes increasingly difficult to reliably detect the pulse positions. This problem has been circumvented to a certain extent by encoding the user data using an RLL code with d=1 or d=2 constraint and by applying 'pulse slimming' to the readback signal [47] [46] [15]. Pulse slimming is a form of equalization whereby the interaction between adjacent pulses is minimized by filtering the readback signal for trimming the pulses to be narrow.

At high recording densities, the peak detector breaks down due to the presence of severe ISI in the readback signal. This necessitates the use of more sophisticated equalization and detection techniques to ensure reliable data recovery. The purpose of equalization is to shape the characteristics (e.g. spectrum) of signal and noise according to certain specifications. A straightforward approach would be to design the equalizer transfer function to be the reciprocal of the channel transfer function, so that the ISI is completely eliminated. This, however, is not a practical approach since the resulting equalizer would result in extremely large noise enhancement at frequencies close to zero and 1/(2T). This is because the channel has almost no transfer at these frequencies [48]. Yet another straightforward approach would be to use an optimum maximum likelihood sequence detector (MLSD) [49], implemented using the cost efficient Viterbi algorithm [24], on the 1/T-sampled readback signal. This, however, is not practical either, since the complexity of Viterbi detector (VD) increases exponentially with the number of ISI components. As a result, two of the most commonly considered approaches for detection are based on the principles of partial response (PR) equalization [21] and decision feedback equalization (DFE) [22].

The basic idea of partial-response equalization is to use a linear filter, called equalizer, to shape the long channel response $h(t)$, which causes severe ISI, into a known partial response $p(t)$. That response is chosen such that i) the ISI components due to $p(t)$ are limited to a specified small number, and ii) the spectra of $h(t)$ and $p(t)$ are as similar as possible. Such a choice ensures that the complexity of Viterbi detector is practically affordable and the resulting noise enhancement is minimum. A widely used family of PR polynomials is of the form [50]

$$P(D) = (1 - D)(1 + D)^n, \quad n = 0, 1, 2, \cdots, \tag{1.7}$$

where D denotes the 'one bit delay' operator and $P(D)$ relates to a sampled version $p_k = p(t)|_{t=kT}$ of $p(t)$ according to $P(D) = \sum_k p_k D^k$. Some examples are PR4 (class IV partial response), EPR4 and E^{2}PR4 (extended PR4) for n=1, 2, and 3, respectively [25] [51] [52] [53]. Fig.1-2 shows the schematic of a read channel with PR equalization and Viterbi detector.

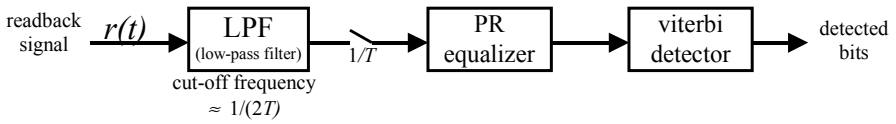

Fig.1-2: Read channel with PR equalizer and Viterbi detector.

At high densities, PR detection results in significant improvement over peak detection [6]. However, the mismatch between the recording channel and the target responses causes the noise at the PR equalizer output to be correlated. In the presence of correlated noise, the Viterbi detector becomes a sub-optimal detector. To improve the performance of PR-based detectors, several modifications have been proposed. An important contribution has been the 'noise-predictive PR scheme' [54]. This scheme uses a noise predictor to effectively whiten the noise at the equalizer output. Another key proposal has been the 'modified-target PR' scheme [55]. In this scheme, instead of choosing a standard PR target, the PR target shape is optimized for the given head-media combination to result in better detection performance. Yet another approach, which is currently being pursued intensively, is the combination of distance-enhancing codes and/or parity codes with PR equalization to improve the overall detection performance [56] [42].

The decision feedback based approaches use a two-step procedure for ISI removal [22]. Fig.1-3 shows the schematic of a read channel with DFE detector.

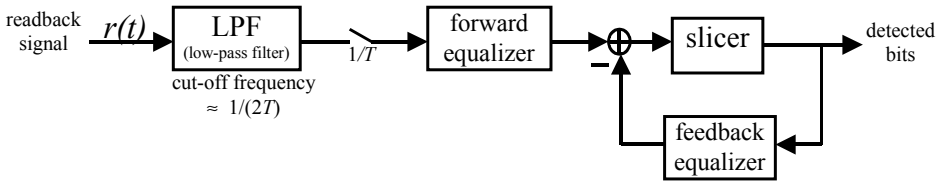

Fig.1-3: Read channel with DFE detector.

The DFE detector consists of a forward equalizer, a feedback equalizer, and a slicer. The forward equalizer suppresses pre-cursive ISI (i.e. ISI from bits yet to be detected, or $a_{k+l}, l \geq 1$) and minimizes noise. The feedback equalizer removes post-cursive ISI (i.e. ISI from already detected bits, or $a_{k-l}, l \geq 1$). Thus, the joint action of the forward and feedback equalizers results in complete absence of the ISI at slicer input. Then, the detected bit (also called, decision) is equal to the sign of the slicer input. One of the major advantages of DFE, because of its 2-step ISI removal structure, is that it does not suffer from noise enhancement [23] [48]. On the other hand, a weakness of DFE is the phenomenon of error propagation, which arises because of the use of past decisions to cancel the post-cursive ISI [23]. In other words, errors in past decisions tend to cause further decision errors. Over all, the DFE offers a good compromise between complexity and performance [26] [23] [33] [48].

There have been several modifications to the basic DFE to improve detection performance. One key proposal has been to use multiple DFE detectors connected in parallel in a single structure for making more accurate decisions on those samples which are not suitable for making direct hard decisions [57] [58] [34]. This structure also helps in minimizing error propagation. Examples of such detectors are parallel DFE [57], Dual DFE [34] [59], and multi-level DFE family [58] [60]. Another key proposal has been to use a combination of decision

feedback and a fixed-depth tree-search based detector, called fixed delay tree search with decision feedback (FDTS/DF) [6] [61] [62]. There have also been proposals where the principle of decision feedback is used to reduce the complexity of the Viterbi detector [63] [64].

We can conclude from the above paragraphs that equalization is an effective technique to provide the signal shaping suitable for detection while mitigating the effects of ISI and noise. Adaptation techniques have also been widely used to compensate in real time for variations in the recording system parameters. These techniques may involve the adaptation of equalizer coefficients, timing phase, gain, and DC [25] [26]. Our focus in this thesis is on timing recovery, which deals with the acquisition and tracking of timing phase in the read channel. Timing recovery is regarded as one of the most important and also difficult tasks at the receiver end, especially for high-density and high data-rate recording [8]. In the next two sections, we summarize the topics of timing recovery, which are undertaken for investigation in this thesis, and the contributions that resulted from this research work.

1.3 Motivation for the Present Study

For the present study, we choose 'timing recovery' as the broad area, and identify several topics for in-depth investigation. We leave a broad review and detailed discussions on timing recovery issues in Chapter 2. In this section, we elaborate on the motivations that underlie the selection of these topics.

The data detector in the read channel operates on samples of the filtered readback signal for detecting the recorded data bits. The problem of timing recovery is concerned with the determination of the time instants at which these samples should be taken. Clearly, timing recovery is very important since errors in the choice of sampling instants will directly translate to poor detection performance. This is because the minimization or cancellation of ISI is guaranteed only at the correct sampling instants. Further, with the steady increase in recording densities and data rates, the resulting decreased bandwidth and deteriorated SNR reflect a decreased amount of timing information, and at the same time, requirements on the accuracy of timing recovery tend to become increasingly severe. As a result, timing recovery becomes increasingly critical for reliable data recovery and, at the same time, more difficult to accomplish. Hence, studying and developing reliable timing recovery techniques become necessary and important.

An example of the timing recovery system in a read channel is depicted in Fig.1-4.

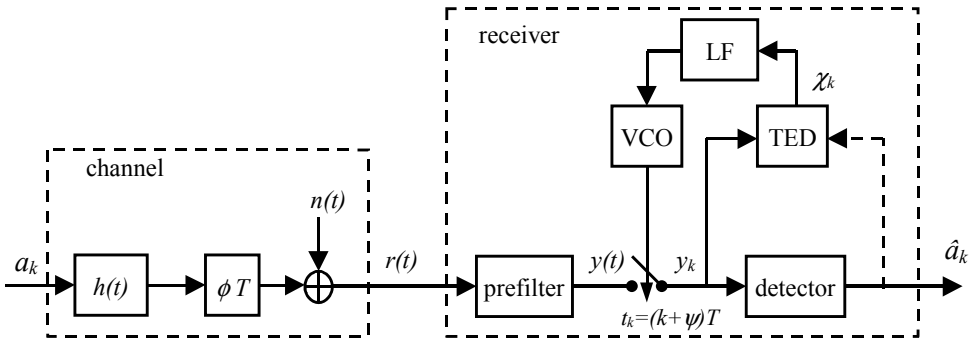

Fig.1-4: Example of a timing recovery system.

The input data sequence a_k of data rate $1/T$ is applied to the channel with bit response *h(t),* additive noise *n(t),* and an unknown delay ϕ (normalized in units T). The receiver operates on the received signal *r(t)* to produce decisions $\hat{a}_k$ with respect to a_k based on the recovered clock signal that indicates the sampling instants $t_k = (k + \psi)T$. Here, ψ is the normalized sampling phase of the recovered clock signal that must closely approach ϕ in order for the detector to function properly. To achieve this, a timing recovery subsystem has to be developed in order to demarcate the instants t_k that make the magnitude of the sampling phase error $\tau = \psi - \phi$ (normalized in units T) as small as possible. Obviously, the desired sampling instants are $\tilde{t}_k = (k + \phi)T$. Then, the actual sampling instants t_k can be interpreted as $t_k = \tilde{t}_k + \tau T$ that exhibit a sampling phase error τ . For the sake of convenience, throughout this thesis, we set $\phi = 0$, i.e. we denote by kT the desired sampling instants in the presence of the unknown channel delay, which is ϕ in the present case. Therefore, the actual sampling instants t_k are expressed as $t_k = (k + \tau)T$, thus indicating the presence of the sampling phase error τ .

As illustrated in Fig.1-4, the heart of the timing recovery subsystem is a phase-locked loop (PLL) that tracks the clock phase and frequency from the incoming signal [8] [65]. The PLL consists of a timing-error detector (TED), a loop filter (LF), and a voltage-controlled oscillator (VCO). The TED serves to generate a timing error output χ_k , which is an indication of the sampling phase error τ . The LF and the VCO serve to filter and average the timing error. As a result, the frequency and phase of the VCO are adjusted by the filtered timing error. The output of the VCO is the sampling clock signal that controls a sampling device, which is often an analog-to-digital (A/D) converter. Clearly, the timing recovery system depends largely on the TED. The loop properties also depend on the LF and VCO.

Typically, the timing recovery process takes place as follows. Initially, the read clock is running freely at a frequency close to the specified channel bit rate $1/T$. However, the timing phase of the clock bears no relation to the timing of the incoming signal (filtered readback signal). By ‘timing phase’ we mean the phase shift of the read channel clock with respect to the ideal sampling instants at the frequency $1/T$. The actual timing of the incoming signal depends on the timing of the clock used in the write channel as well as the delays caused by the physical or electrical systems from the write-head to the sampling point in the read channel. The system needs to be brought into synchronism in both phase and frequency. Usually, a known training sequence, which is called preamble, is recorded prior to the actual data sequence. To facilitate acquisition, specially developed TED algorithms make use of this preamble to compensate for initial errors in phase and frequency [66]. This is called the ‘acquisition mode’ of timing recovery. Once the acquisition has been accomplished, small corrections are necessary for tracking the slow variations in the actual timing. This is called the ‘tracking mode’.

The thesis work focuses on timing recovery techniques that ensure reliable acquisition and tracking for recording channels. With a limited period of preamble, the objective of timing acquisition is to select the sampling phase ψ to match the channel delay ϕ as rapidly and accurately as possible. With the specific recording density and data rate, the objective of tracking is to track the clock signal with a minimum phase error variance while maintaining the averaged sampling phase error τ to zero. This is essential for the read channel to provide a reliable detection performance.

There are several issues that should be addressed while developing a timing acquisition system. The first and foremost requirement is that the acquisition should be fast and accurate. The preamble pattern and the TED have significant roles in achieving this goal. The preamble

should be chosen to maximize the amount of timing information available at the TED input in the face of noise. Further, a shorter length of the preamble is desirable to allow more storage area for the user data. For a given preamble pattern, the TED should be chosen to result in a performance that is as close to optimum as possible, with a practically affordable complexity [67].

False lock and hang up are two serious problems that can arise during timing acquisition. False lock means that the timing loop locks to a wrong phase and/or frequency. Hang up means that the timing loop dwells at a wrong phase for a prolonged interval and therefore takes a very long time to reach the correct phase [68]. Thus, false lock and hang up are disastrous for timing acquisition in magnetic recording systems where fast and reliable timing acquisition is required with a short preamble sequence. The preamble pattern and the acquisition mechanism must be chosen appropriately in view of this requirement. In addition, a concern that deserves significant attention during the development of acquisition techniques for timing recovery is the feasibility of their implementation in a practical system. In other words, the techniques should be simple as well as reliable. Hence, it is of interest to explore the practical implementation of the fast acquisition schemes under consideration.

An important concern during the tracking mode of timing recovery is the steady-state jitter, which tends to increase with increase in recording density and data rate. Steady-state jitter is the timing jitter that is present in the phase when the timing loop is operating in the tracking mode. Even though the timing jitter can be made small enough by careful choice of the timing loop parameters, timing fluctuations can arise due to various reasons, such as variations in spindle speed or flying height, fluctuations in the read head position, occurrence of magneto-resistive (MR) thermal asperity, etc.. Because timing jitter causes a performance degradation, it is useful to calibrate or evaluate the sensitivity of detectors to timing jitter. It is also of interest to develop techniques that can help to minimize the timing jitter.

Recently, fully digital adaptive equalization and interpolative timing recovery techniques for asynchronously sampled recording channels have appeared in the literature and they show attractive advantages in terms of complexity, cost and stability [69] [70]. Development of these techniques, from the point of view of real-time implementation, is a topic that is of much interest in read-write channel research.

All of the above mentioned aspects have motivated the research work reported in this thesis. In the next section, we summarize the contributions in each of the chapters.

1.4 Contributions and Organization of the Thesis

As recording systems become more efficient in terms of modulation code, bandwidth and storage density, the task of timing recovery becomes more difficult and, at the same time, increasingly critical to reliable data recovery. This thesis is devoted to the investigation and development of timing recovery techniques for digital recording channels. It investigates the structure and performance of timing recovery schemes, and develops new timing recovery schemes for magnetic and optical recording applications.

The thesis contains eight chapters. Chapter 1 gives a brief introduction to digital recording technology, and a quick review of read-write channel techniques. It concludes with the motivation, contributions and organization of the thesis. Chapter 2 gives a detailed review of timing recovery, highlighting the different possible structures, requirements, and performance measures. It also discusses generic timing-error detector (TED) algorithms, and the main issues

that arise during timing acquisition. Analyses and simulation results are provided to support the discussions, wherever possible. Chapters 3 to 7 describe the main new research contributions made during the course of this Ph.D. work. Chapter 8 concludes the thesis with some remarks on directions for further work.

Chapter 3 investigates the timing sensitivity of partial response and decision feedback detectors, and develops an analytical approach to evaluate the performance in the presence of static and random timing phase errors. Chapter 4 examines the efficiencies of existing and proposed TED algorithms for partial response and DFE recording channels. It also develops a marginal detection based TED for minimizing jitter in multi-level DFE (MDFE) detector and analyzes its phase noise performance. Further, it examines the optimality of the preamble and TED used for the timing acquisition in MDFE. Chapter 5 investigates the problem of timing acquisition in DFE detectors. It develops two novel fast acquisition techniques that do not suffer from hang up and false lock problems, even in the presence of large initial errors in timing, gain and DC offset. Chapter 6 describes the implementation of a practical timing recovery system, which is designed and prototyped in emitter-coupled logic (ECL) discrete-components, for a 100 Mb/s experimental MDFE read channel (channel data rate is 150 Mb/s). Performance evaluation of the system based on bench tests and spinstand tests are also presented.

The focus of the development of the algorithms and systems in Chapters 3 to 6 is on magnetic recording, even though these are also applicable with minor modifications to optical recording. In contrast, our focus in Chapter 7 is on optical recording. In Chapter 7, an asynchronously sampled optical DVR (digital video recording) channel is studied. It develops a new, attractive and practicable architecture for fully digital zero-forcing (ZF) based equalizer adaptation and interpolative timing recovery (ITR).

The development of new algorithms and systems presented in Chapters 3 to 7 is supplemented with computer simulation results. These simulation results are used for demonstrating the effectiveness of the proposed algorithms and for corroborating the analytical developments.

1.4.1 About the publications by the author

Based on the research work carried out during the course of the Ph.D. work, the author published thirteen papers, coauthoring with his supervisors and other project partners (see the list of the publications by the author). The author's contributions to timing recovery, as reported in these publications, consist of four parts. The first part develops effective analytical approaches with simulations to corroborate the analytical results in [1~5] and [8]. The second part proposes improved or simple TED algorithms in [2], [4], [10] and [12]. The third part develops novel DFE acquisition structures in [3], [5], [10] and [12]. The fourth part performs the design, implementation and verification of a timing recovery system in [6~7], [9], [11] and [13]. The contents of these publications are reorganized and reflected in the following chapters of this thesis.

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CHAPTER 2

REVIEW OF TIMING RECOVERY

In digital communication systems, synchronization is one of the most crucial tasks to be performed at the receiver for ensuring reliable data recovery. In general, the problem of synchronization involves carrier synchronization, timing recovery and word/block synchronization. The objective of carrier synchronization is to generate a reference carrier whose phase matches that of the received signal in carrier modulated systems. Since digital recording systems are equivalent to digital baseband communication systems, the synchronization tasks in these systems are limited to timing recovery and block synchronization. The objective of timing recovery, which is also called clock recovery or bit synchronization, is to recover a clock at the channel rate that is phase-locked to the readback signal. The objective of block synchronization is to look for the start of a message in the detected data or to divide the detected data sequence into smaller blocks. Our focus in this thesis is on timing recovery techniques for digital recording systems. The goal is to ensure that the samples of the readback signal taken at the set of sampling instants provided by the timing recovery technique should result in reliable data recovery.

In this chapter, we present a reasonably broad review on timing recovery. This review relates to different possible structures, requirements, and performance measures. It also discusses generic timing error detector algorithms and the main issues that arise during timing acquisition. Wherever possible, analyses and simulation results are presented for supporting the discussion.

2.1 Introduction to Timing Recovery

Timing recovery, being a critical task at the receiver for reliable data recovery, has been a subject under investigation for many decades (see [1] [2] and the references therein). Several books are available (e.g. [3], [4], [5], and [6]) that deal with timing recovery issues in detail. The key problem in timing recovery is the determination of time instants at which the received (or, readback) signal should be sampled for doing reliable data recovery. A straightforward solution to this problem is to send the clock signal to the receiver as side information. Since this approach requires additional power and/or bandwidth, another approach, called self-timing, has been widely adopted for implementing timing recovery. The timing-recovery schemes based on self-timing recover the clock from the received signal itself [7] [8], thus they do not have the additional requirements mentioned above. For this reason, the self-timing approach has been utilized extensively in data transmission systems. The earliest large-scale application was in regenerative repeaters [9] [10]. A key step in the development of a self-timing scheme is the determination of an objective function that can be constructed using the received signal samples

such that the information on the correct timing can be obtained from the salient features of this function such as minimizers, maximizers, or roots, without any ambiguity [11] [7] [1]. In this chapter, we restrict the review to self-timing based timing recovery schemes, since read channels in recording systems are based on this approach.

Fig. 2-1 shows the schematic of a read-write channel (i.e., transmitter and receiver) for recording systems emphasizing the timing recovery part.

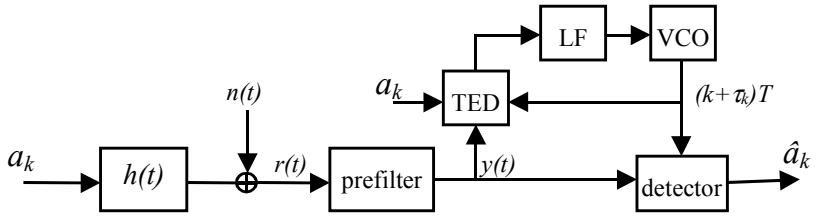


Fig. 2-1: Schematic of a read-write channel with timing recovery.

As explained already in Section 1.2.2, the recording channel is modeled using the bit response *h(t)* with input data bits $a_k \in \{-1,1\}$ at rate $1/T$ bits/s and additive noise *n(t)*. The prefilter and detector form part of the read channel. The prefilter conditions the readback signal *r(t)* by doing noise limiting, equalization, or any such filtering functions. The detector operates on the prefilter output *y(t)* to produce the decisions $\hat{a}_k$ on the data bits a_k. The detector, as shown here, uses a phase-locked loop (PLL) [12], which consists of a timing error detector (TED), loop filter (LF), and voltage-controlled oscillator (VCO), for generating the timing instants at which the prefilter output should be sampled. It is assumed that the readback signal *r(t)* may suffer from timing fluctuations arising from several undesired phenomena that occur in the recording channel (e.g. variations in spindle speed and flying height, clock drift, etc.). In addition to these, while sampling the signal *y(t),* the detector also needs to take into account the delay caused by the physical or electrical elements in the recording system. The resulting sampling instants are denoted by $(k+\tau_k)T$ where kT specifies the k^{th} ideal sampling instant and τ_k (normalized in units T) is the estimate of the timing discrepancy with respect to this reference. Clearly, τ_k, which we call 'timing phase error', accounts for unknown timing fluctuations and delays in the recording channel.

It can be said that the TED is the most important block in the PLL, since the task of the TED is to extract timing information from the incoming signal. The TED shown Fig. 2-1 is of the data-aided type since it makes use of the data bits a_k. There are also non-data aided TEDs where the data a_k is not used in the TED. The filtered TED output by the loop filter (LF) is used to control the frequency and phase of the VCO. The PLL effectively performs an averaging operation on the TED output, thereby suppressing the dynamic variations caused by noise and other effects in the system. The loop filter has a significant role in deciding the various properties (e.g. bandwidth, noise suppression gain, etc) of the overall PLL. Therefore, what is of utmost importance to the PLL performance is the average output of the TED. The TED output, in time or phase domain, can be modeled as [3]

$$\chi_k = \rho(\tau_k) + u_k \tag{2.1}$$

$$\tau_k = \phi_k - \psi_k \tag{2.2}$$

where ϕ_k and ψ_k (all normalized in units *T*) are the ideal timing phase and its estimate from the PLL, respectively, and u_k is the noise component of the TED output that is converted into phase noise by the PLL. For obvious reasons, τ_k is the timing phase error. The function $\rho(\tau)$, which is deterministic in nature, describes the average output of the TED over the ensemble of possible data sequences, and is called the timing function. Since the TED output is meant to be proportional to the timing phase error, it is clear that the function $\rho(\tau)$ should have a zero crossing only at $\tau = 0$ and the sign of $\rho(\tau)$ for $\tau > 0$ should be opposite to that for $\tau < 0$. Strictly speaking, the zero crossings in $\rho(\tau)$ may also occur at integer values of τ. Sampling with $\tau_k = l$ for integers $l \neq 0$ implies a shift of *l* samples in the original sequence of samples obtained for $\tau_k = 0$.

For small timing phase errors, we may linearize $\rho(\tau)$ as

$$\rho(\tau) \simeq K_d \tau \tag{2.3}$$

where K_d is the slope of the timing function $\rho(\tau)$ at origin $\tau = 0$, and is called the 'TED gain'. To conclude our discussion on the TED, we may say that a properly designed TED should have zeros crossing only at $\tau = 0$ and a large TED gain K_d. The resulting linearized discrete-time TED model is shown in Fig. 2-2.

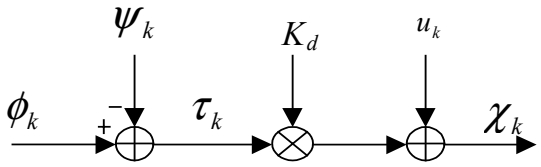


Fig. 2-2: Linearized discrete-time phase-domain TED model.

Fig. 2-3 shows two structures that are used for the loop filter. Fig. 2-3(a) corresponds to a simple proportional filter type with coefficient K_p and Fig. 2-3(b) corresponds to proportional-plus-integral filter type with coefficients K_p and K_f. The PLLs that use these loop filters are called 'first-order PLL' and 'second-order PLL', respectively. Because of these loop filter configurations, the first-order PLL is able to handle only phase errors whereas the second-order PLL can handle both phase and frequency errors.

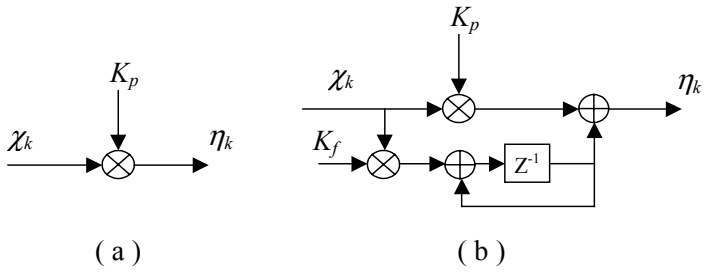


Fig. 2-3: Structures of discrete-time loop filters: (a) proportional type, (b) proportional-plus-integral type.

Fig. 2-4 shows a discrete-time phase-domain model of the VCO [3]. The gain factor K_o determines the sensitivity of the VCO. The error between the VCO frequency and the frequency of the signal at PLL input (i.e. bit rate $1/T$) is modeled by the offset parameter λ. The integrator performs the frequency-to-phase conversion within the VCO. Finally, υ_k represents the VCO phase noise.

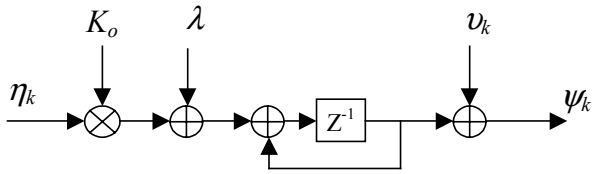


Fig. 2-4: Discrete-time phase-domain model of VCO.

Let us look at an example of a first-order PLL . Combining Fig. 2-2, Fig. 2-3 and Fig. 2-4, we get the discrete-time model of a first-order PLL as shown in Fig. 2-5. Here, the VCO phase noise and frequency errors are ignored. The quantity θ_k is the input-referred phase noise and is given by (using Fig. 2-2)

$$\theta_k = u_k / K_d \,. \tag{2.4}$$

The overall loop gain K_t is given by $K_t = K_d K_p K_o$.

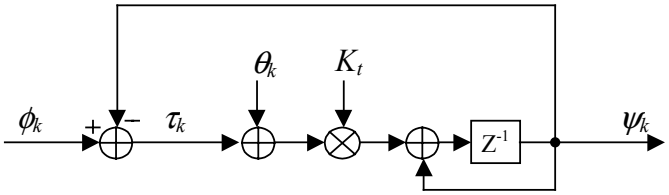


Fig. 2-5: Discrete-time phase-domain model of first-order PLL ignoring VCO phase noise and frequency error.

For a given channel, the most important part of work in the design of timing recovery is the design of the TED. In the past fifty years, a vast array of techniques has been reported for implementing self-timing based timing recovery in various applications. An excellent review as well as summary of the key contributions can be found in [3, Chapter 10]. Based on how the timing information is derived from the received signal (i.e. how the TED is designed), timing recovery techniques can be classified as: maximum-likelihood (ML) schemes, minimum mean-square error (MMSE) schemes, zero-forcing (ZF) schemes, threshold-crossing schemes, early-late schemes, and nonlinear spectral line schemes, or a combination of these.

2.2 Structures, Requirements and Performance Measures

In this section, we discuss the different ways in which the timing recovery schemes can be configured, the various requirements that should be taken into account to ensure proper operation of the timing loop, and the various measures that can be used to assess the performance of timing recovery schemes.

2.2.1 Timing recovery structures

In Fig. 2-1 we did not explicitly show the position of the sampler. We did this to keep the discussion in Section 2.1 as general as possible. Depending upon whether the timing information is extracted before or after this sampler, the timing recovery systems can be classified as deductive or inductive [3]. Fig. 2-6 depicts receivers incorporating these two configurations of timing recovery schemes.

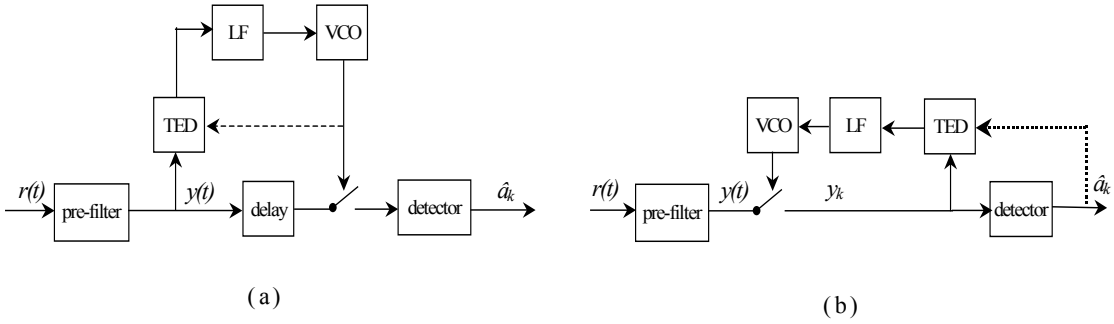


Fig. 2-6: Receivers incorporating (a) deductive and (b) inductive timing recovery schemes.

As shown, the sampler is assumed to be located between the prefilter and the detector. In the deductive scheme, the timing information is extracted before the sampler, whereas in the inductive scheme this is done after the sampler. Clearly, the deductive structure favors analog implementation whereas the inductive structure favors digital implementation. Further, the inductive structure can operate in a data-aided (DA) mode, in contrast to the deductive structure that operates in a non-data-aided (NDA) mode. However, practical implementation of data-aided inductive schemes often makes use of the decisions $\hat{a}_k$ from the detector, rather than the actual data a_k, thereby resulting in the so-called 'decision-directed' (DD) mode of operation [18].

The decision-directed inductive schemes tend to perform poorly during acquisition because of decision errors. Clearly, the effect of decision errors is nonexistent in the deductive structure. Thus, the deductive structure has the potential for fast and reliable timing acquisition. To mitigate the effects of decision errors during acquisition, the inductive schemes usually use a fixed training sequence, called preamble, which precedes the actual user data. The preamble is usually a known periodic pattern. By using the knowledge of this preamble, acquisition speeds in inductive schemes can be significantly improved.

Deductive and inductive timing recovery schemes may yield different performances in the tracking mode, especially for low signal-to-noise ratio (SNR) channels. The key advantage of the deductive scheme is that it is independent of the detection performance. However, the deductive scheme has a big disadvantage in that it requires the received signal to have reasonable excess bandwidth. This makes this scheme not practical for high-density recording applications, where the readback signal has minimal or nil excess bandwidth. For this reason, the inductive scheme attracts more interest and attention than the deductive scheme for timing recovery in recording systems.

Currently, the trend in the industry is towards fully digital implementation of read channels. Therefore, it is of utmost priority to ensure that the overall circuit complexity is within limits so as to permit operation at high speeds and low power. Since cost and complexity of digital circuits increase with data rate, timing recovery operating at as low as the symbol rate, also

called baud-rate, is most desirable. Symbol-rate timing recovery techniques were first proposed in the classical paper of Mueller and Müller [1]. This paper is widely acknowledged as the basis for most of the current algorithms for symbol-rate timing recovery [13]-[21]. In these schemes, the timing loop is driven by samples at symbol-rate, thereby favoring digital implementation. This is unlike the non-symbol-rate schemes, which usually have unsampled signals at the TED input and may need additional samplers within the timing loop to generate the sampling phase updates.

2.2.2 Timing recovery requirements

Since self-timing techniques extract timing information from the received signal, additional requirements should be imposed on the signal to ensure that the timing loop performs satisfactorily. For example, if the data sequence $\{a_k\}$ contains long runs of +1 or -1, then the received waveform contains very minimal timing information. Consequently, the timing loop cannot be updated frequently enough. As a result, the PLL may loose lock. Therefore, it is required that the transmitted data have significant high frequency content and not be DC-like for prolonged periods of time. For this reason, it is customary to encode the user data using proper modulation codes to ensure that there is sufficient timing information embedded in the received signal. Modulation codes can be used to limit the maximum run-lengths of data bits [22]-[25]. Examples of such codes are DC-free and run-length-limited (RLL) codes. Such codes are widely applied in digital recording systems. As we discussed in Section 1.2.1, the price paid for the use of these codes is the reduced SNR in the received signal. An alternative approach to the use of modulation codes is to randomize the data by means of a scrambler [22][26][27], which lowers the probability of a long run length. This approach does not add redundancy into the data sequence and has found widespread application in data modems.

For fast and reliable timing acquisition, a preamble is usually used to precede the actual user data. The preamble often contains a known periodic pattern that can be used to acquire clock rapidly before the user data begins. Therefore, it is desirable that the preamble contains as many transitions as possible so as to convey sufficient timing information to enable fast acquisition. We postpone further discussion on the issue of optimality of the preamble pattern to Chapter 4, in which the impact of recording data on timing recovery is investigated in detail.

In addition to the items mentioned above, there are also several other issues and requirements that must be taken into account for developing a reliable and efficient timing recovery algorithm. Possibly the most important of these is that the timing function $\rho(\tau)$ must not have multiple zero crossings or a zero crossing at $\tau \neq 0$. Such undesired zero-crossings could make the timing loop converge to a wrong phase, thereby resulting in significantly inferior detection performance. In case $\rho(\tau)=0$ for $\tau \neq 0$, special precautions should be taken to avoid wrong phases. Additional requirements are fast initial acquisition of the correct phase, faithful tracking of the timing fluctuations in the steady state, good noise suppression, minimum phase jitter etc. From the point of view of practical implementation, the algorithm should be simple enough, while not compromising on reliability.

2.2.3 Timing recovery performance measures

In this section, we discuss various measures that can be used to evaluate the effectiveness of timing recovery schemes. Our discussion includes measures that can be computed based on theoretical analyses, as well as numerical measures that can be obtained by doing simulations. Therefore, in cases where it is difficult to evaluate the analytical measures, one can resort to the numerical measures for performance evaluation.

A. Timing sensitivity

For any system, the performance is dependent on the available timing phase margins. The timing phase margin specifies the maximum error in the timing phase that the receiver can tolerate before the performance becomes unacceptable. Clearly, the timing phase margin depends on the characteristics of the channel and the timing loop. The timing sensitivity is a measure of how fast the performance degrades with timing phase error. The sensitivity to timing phase can be gauged by examining the eye pattern of the signal at the input of the decision block within the receiver [52]. The decision block is, for example, the slicer in the DFE detector [28] and the Viterbi algorithm in the partial response detector [16]. The eye pattern, sometimes also called eye diagram, is obtained by overlaying segments of the signal in a phase-aligned manner. That is, if the i^{th} segment is given by $y(t)$ for $t_i \leq t < t_i+t_s$ and i=1,2,3,…, then the i^{th} and j^{th} segments are related by $t_j=t_i+nT$ where n is an integer and T is the bit interval. Here, $t_s \geq T$ is the duration of each segment. The overlaid plots resemble a human eye. The shape and size of the 'eye' indicate the margins of the system against various disturbances, such as timing phase error, intersymbol interference (ISI) and noise.

Fig. 2-7 shows the eye pattern for a noiseless channel that has raised-cosine characteristics with 25% and 100% excess bandwidth [52].

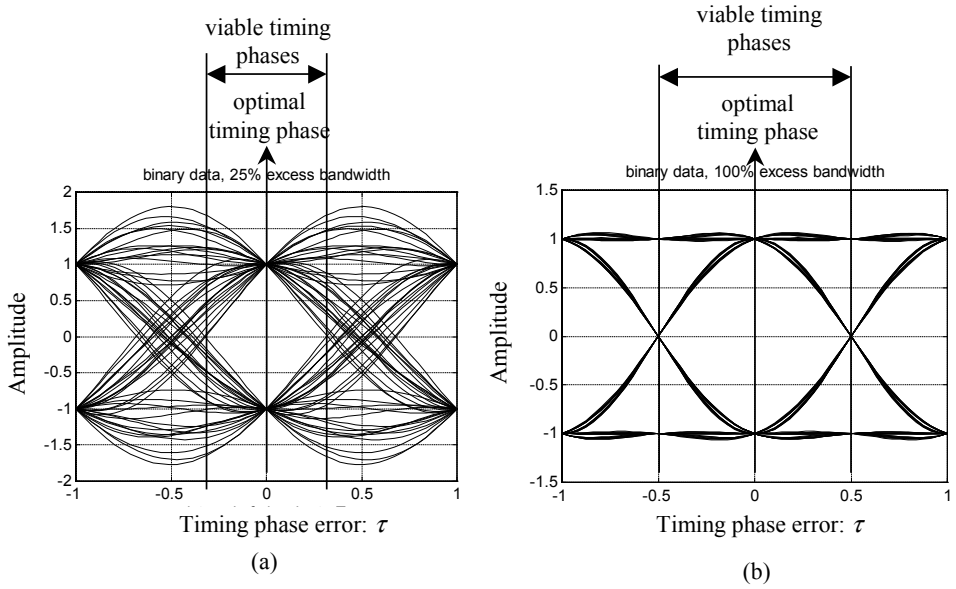
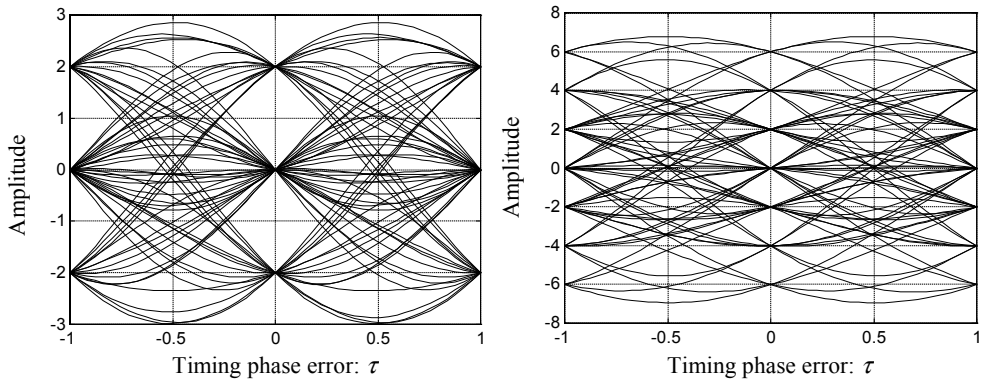


Fig. 2-7: Eye patterns for a raised-cosine channel with (a) 25% and (b) 100% excess bandwidth.

The optimal timing phase corresponds to τ=0 (τ is normalized in units T) where the eye opening is the greatest. The eye opening decreases as the timing phase error moves away from τ=0 in either direction. This is because the ISI, which is zero at τ=0, increases as τ deviates from the optimum value. Clearly, as τ or ISI increases, the noise margin decreases. The width of the interval around the optimal phase over which the eye is not closed is defined as the eye width. In the absence of noise, the data bits can be correctly detected as long as the timing phase is within the open eye region. Fig. 2-7 shows that compared to the case of 100% excess bandwidth, the case of 25% excess bandwidth is more sensitive to timing phase error because the eye closes more rapidly in the latter. For example, the eye width is T for 100% excess bandwidth and 0.638T for 25% excess bandwidth. With zero excess bandwidth, the eye width approaches zero. Thus, the eye width is a straightforward measure of timing sensitivity.

It should not be inferred, however, that all signals without excess bandwidth have zero eye width. For example, consider the partial responses PR4 ($P(D)=1-D^2$) and E^{2}PR4 ($P(D)=1+2D-2D^3-D^4$) which are widely used as equalization targets in magnetic recording systems. These responses have no excess bandwidth and yet result in eye-patterns with open eyes, as illustrated in Fig. 2-8. In particular, the eye width is $0.449T$ for PR4 and $0.345T$ for E^{2}PR4.



(a) (b)

Fig. 2-8: Eye patterns of (a) PR4 and (b) E^{2}PR4 partial response channels that have no excess bandwidth.

Timing sensitivity can be examined using different approaches. Several researchers have reported theoretical and simulation studies on timing sensitivity of detectors [29] [30] [31] [32] [33]. In Chapter 3, we propose a novel analytical approach to evaluate timing sensitivity of decision feedback and partial response detectors in magnetic recording systems [34].

B. Tracking performance

Practical timing recovery circuits in the receiver cannot perfectly duplicate the clock of transmitter. Although the average frequency and phase of the derived clock may be correct, it will inevitably exhibit phase jitter because of noise. Fig. 2-9 shows a typical situation of phase jitter in the recovered clock. Statistical properties of the timing phase error (or, phase jitter) are of much interest in the tracking mode since they determine the accuracy of the recovered timing signal. In practice, a convenient performance measure is the root-mean-square (RMS) value of the timing phase error.

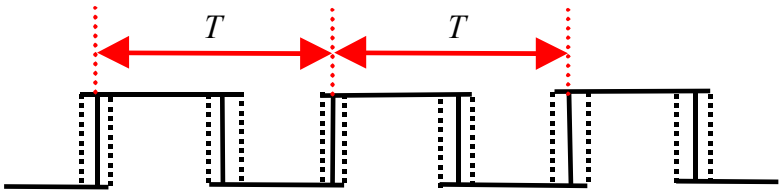


Fig. 2-9: Recovered clock with phase jitter.

Timing jitter causes mainly two degradations. First, it results in increased ISI because of suboptimal sampling instants, thereby reducing the noise immunity of the receiver and increasing the bit error rate. Second, the data signal emerging from the detector will generally have similar timing jitter as in the recovered clock. This could cause degradation in the performance of the systems that follow the receiver. Timing jitter has two principal

components, namely, pattern-dependent jitter and noise-induced jitter. In the tracking mode where timing phase errors are small, it is possible to ensure that pattern-dependent jitter is very small [35]. Therefore, noise-induced jitter is generally the main disturbance to be dealt with in timing recovery systems. In principle, jitter can be minimized by appropriate design of the timing recovery circuits, for example through a proper choice for the bandwidth of the timing-recovery loop. Reduction of jitter via a reduction of the bandwidth of the loop, will adversely affect the ability of the loop to track the phase fluctuations in the system. Because of this trade-off, phase jitter remains a serious problem that deserves careful attention in the design of the receiver.

Another key problem in practical timing recovery circuits is static timing phase error (also called steady state phase bias), which may arise from unexpected errors at the TED input due to channel variations and misequalization, or DC offsets within the timing loop. The static timing phase error must remain very small with respect to the clock period to ensure a satisfactory detection performance. For this reason, the steady state phase bias is an important parameter that cannot be ignored when evaluating the tracking performance.

The PLL may lose lock when timing phase errors become too large. This can happen due to noise as well as changes in the phase and frequency of the PLL input. For the PLL to lose lock due to fluctuations in phase, the underlying fluctuations should be sudden and large. Two key parameters that are used to specify the frequency range in which the PLL can track satisfactorily are the 'hold range' and 'pull-out range' [36, Chap. 2] [3, Chap. 11]. The hold range, which is also called hold-in range or static operating range, is the range of frequency over which the loop will remain locked when the input frequency changes very slowly. The pull-out range is the dynamic limit for stable operations, i.e. the loop will lose lock if the frequency step exceeds the pull-out range.

Large noise peaks, which occur when the noise power is significant, may cause loss of lock or cycle slips. A cycle slip is said to occur when the recovered clock drops or adds one or more cycles of oscillations relative to the incoming signal. If there are cycle slips, the loop is considered to have lost lock. This depends strongly on the loop signal-to-noise ratio defined as

$$SNR_{loop} \triangleq \frac{1}{2\sigma_\theta^2 B_l} = \frac{K_d^2}{2\sigma_u^2 B_l} \tag{2.5}$$

where σ_θ^2 is the variance of the phase noise θ_k at the PLL input (see Fig. 2-5) and B_l is the equivalent noise bandwidth of the loop, which is given by

$$B_l \triangleq \int_{-0.5}^{0.5} |\, G_\psi(e^{j2\pi\Omega})\,|^2 \, d\Omega \tag{2.6}$$

where $G_\psi(e^{j2\pi\Omega})$ is the transfer function of the PLL from the TED input to VCO output [3, Chap. 11], and Ω is a normalized frequency variable defined as $\Omega = fT$. (Note that Ω is a dimensionless frequency variable that is normalized with respect to the rate $1/T$ while f is a frequency variable that has dimension 'Hz'. For the sake of convenience, throughout the thesis we will use Ω instead of f to describe frequency-domain notations.) The averaged elapsed time between cycle slips grows exponentially with the loop SNR [12]. In practice, the tracking failure rate is required to be much smaller than the bit or symbol error rate.

C. Timing error detector (TED) efficiency

The capability of the timing loop to track the timing clock depends heavily on how much timing information the TED can extract from the incoming signal, while rejecting the noise as much as possible. To retain the signal component $K_d\tau_k$ while suppressing the noise u_k (see Fig. 2-2), the timing loop (i.e., PLL) must have a bandwidth that is much smaller than the symbol rate 1/*T*. Therefore, all the noise will be rejected except for components near DC (i.e., zero frequency). If $S_u(e^{j2\pi\Omega})$ denotes the power spectral density of u_k, we see from the above argument that $S_u(1)$ will largely determine the amount of noise-induced jitter. Thus, the timing jitter at the TED input is proportional to $S_u(1)/K_d^2$. Using this, the efficiency of the TED is formally defined as [18]

$$\gamma = \frac{1}{SNR_m}\frac{K_d^2}{S_u(1)} \tag{2.7}$$

where SNR_m is the signal-to-noise ratio (SNR) in the matched filter bound sense, given as

$$SNR_m = \frac{\int_{-\infty}^{\infty} h^2(t)dt}{N_o/2} \tag{2.8}$$

where *h(t)* is the channel bit response and $N_0/2$ is the power spectral density of the channel noise. In (2.7), the division by SNR_m removes the dependence of $S_u(1)$ on the noise level in the channel. The TED efficiency, therefore, is a measure of the relative ease of accurate clock recovery. Using this measure, it is possible to quantitatively evaluate the timing recovery performance and compare various timing recovery schemes.

D. Acquisition performance measures

As mentioned already, the most desirable features during the acquisition mode are fast and accurate acquisition of the timing phase. There are certain key parameters that are usually used to describe the acquisition properties [3, Chap. 9], [36, Chap. 2]. The ‘pull-in time’ is the time that the PLL takes in the beginning of the acquisition mode to adjust the VCO frequency to approach that of the incoming signal. The ‘pull-in range’ is the frequency range over which the loop can acquire lock. Acquisition of phase follows acquisition of frequency. The ‘lock time’ is the time taken to acquire the phase, and is usually much smaller than the ‘pull-in time’.

The total acquisition time depends on initial errors in the frequency and phase, the loop bandwidth, the TED used, and the type of preamble pattern used etc.. A large loop bandwidth helps to speed up acquisition but increases phase jitter, and vice versa. Further, the preamble pattern should be chosen optimally, so as to maximize the extracted timing information within a given time duration.

The probability distribution function of the acquisition time for a particular timing loop configuration is of much interest. When this distribution is combined with the false lock probability and acquisition-end characteristics such as phase bias and phase jitter variance before entering the tracking mode of operation, then comprehensive knowledge concerning the acquisition performance is obtained. In practical systems, the acquisition failure rate is a critical parameter, and stringent requirements are imposed on this rate to ensure a reliable timing acquisition. The phenomena of false lock and hang up, mentioned earlier, are the major obstacles to keeping the acquisition failure rate several orders below the symbol error rate. It is

noted that no theory presently exists that can be used to analytically predict the acquisition failure rate. This is because the acquisition process is highly complicated when aspects such as TED non-linearity and noise sources are taken into account. However, one can use Monte-Carlo simulations to study the acquisition performance in specific applications. A detailed discussion on the various aspects of timing acquisition is given in Section 2.4.

2.3 Timing Recovery Schemes and TED Algorithms

As mentioned in Section 2.1, the past several years of research on timing recovery have resulted in a wide variety of techniques. This includes the maximum likelihood (ML) based optimum timing recovery approach and several suboptimal approaches. Even though the ML approach may be expensive to implement in practice, it serves as a reference as well as motivation to develop practical schemes that are simple to implement while being near optimal. Typical examples of suboptimal approaches are the threshold crossing based timing recovery technique (e.g. [37] [38]), the nonlinear spectral line based technique (e.g. [39] [40]), and the early-late timing recovery technique. In general, for these techniques to work well, the excess bandwidth should be significant. Therefore, these techniques are not suitable for digital recording systems, which have almost no excess bandwidth.

Most of the currently used timing recovery schemes in digital magnetic recording are based on the minimum mean-square error (MMSE) and zero-forcing (ZF) principles [21] [41] [3, Chap. 10]. These schemes can work well at sampling rates as low as the baud rate even when systems have little excess bandwidth, and at the same time, yield near-optimal timing recovery performance. They use inductive structures with data-aided (DA) or decision-directed (DD) operation to extract timing information from an error signal. The error signal represents the difference between the actual detector input and the desired one, and can be generated in various simplified ways that lead to different implementation structures. The MMSE and ZF timing recovery schemes suit a broad category of channels, modulation codes and detection schemes. This section restricts the review and discussion to baud-rate data-aided timing recovery techniques based on ML, MMSE and ZF schemes [3], and studies their underlying TED algorithms and the resulting performances for magnetic read channels. In the following subsections, the readback signal $r(t)$ is modeled as shown in Fig. 2-1, and is assumed to contain a delay that is unknown to the read channel. We use [3, Chap. 10] as the source for the ML, MMSE and ZF based TED structures.

2.3.1 Data aided Maximum-Likelihood (ML) timing recovery

Denote the ideal sampling instants by kT and the actual sampling instants by $t_k = (k+\tau)T$ where τ is the timing phase error normalized in units T. Because the channel noise $n(t)$ is white and Gaussian, the ML estimate of the timing phase error τ can be obtained by finding the minimum over all τ of the cost function

$$\Lambda(\tau) \triangleq \int_{-\infty}^{\infty} e^2(t)dt \tag{2.9}$$

where

$$e(t) = \sum_k a_k h(t-(k+\tau)T) - r(t)\,. \tag{2.10}$$

Here, a_k is the input data such that

$$r(t) = \sum_k a_k h(t - kT) + n(t). \tag{2.11}$$

Minimization of $\Lambda(\tau)$ with respect to τ results in the TED structure shown in Fig. 2-10 [3]. The algorithm of the DA ML TED reveals that the optimum TED output χ_k is the product of the data sequence a_k with the samples of the differentiated output of the matched filter with impulse response $h(-t)$. As a result, the TED output can be written as

$$\chi_k(\tau) = a_k \int_{-\infty}^{\infty} r(u) h'(u - (k+\tau)T) du \tag{2.12}$$

where $h'(t) = T\dfrac{dh(t)}{dt}$. The TED transfer characteristic, i.e. timing function, is given by [3, chapter 10]

$$\rho_{ML}(\tau) = \frac{2}{TN_0} \int_{-\infty}^{\infty} 2\pi\Omega A(e^{j2\pi\Omega}) \,|\, H(\Omega) \,|^2 \sin(2\pi\Omega\tau) d\Omega \tag{2.13}$$

where $A(e^{j2\pi\Omega})$ denotes the power spectral density (PSD) of a_k, $H(\Omega)$ is the Fourier transform of $h(t)$, and $N_0/2$ is the PSD of noise $n(t)$. Recall that Ω is the normalized frequency variable defined as $\Omega = fT$.

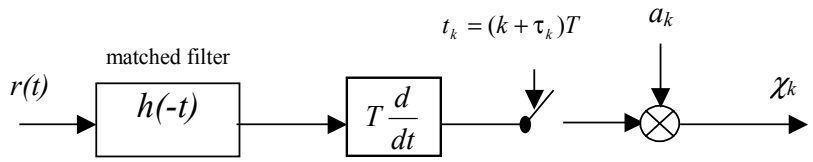


Fig. 2-10: Data-aided ML TED scheme based on the matched filter.

Consider the digital magnetic recording channel with bit response $h(t)$ given by (1.4) and (1.6). We define the normalized user density D_u, as

$$D_u = \frac{pw_{50}}{T_u} = \frac{pw_{50}R}{T} = D_{ch}R \tag{2.14}$$

where $D_{ch} = \dfrac{pw_{50}}{T}$ is called the channel density, R is the code rate and T_u is the bit duration before the modulation encoder. We get the unit step response of Lorentzian channel model as (eq. (1.6))

$$s(t) = \frac{\tilde{h}(t)}{2} = \frac{0.5V_{op}}{1 + (2t/pw_{50})^2} = \frac{0.5V_{op}}{1 + (2Rt/D_uT)^2}. \tag{2.15}$$

With $V_{op} = 2$, the Fourier transform of $s(t)$ is

$$S(\Omega) = \frac{\pi D_{ch} T}{2} e^{-\pi D_{ch}|\Omega|}. \tag{2.16}$$

Since $H(\Omega) = S(\Omega)(1 - e^{-j2\pi\Omega})$ (using eq. (1.4)), we get

$$\frac{2|H(\Omega)|^2}{N_0 T} = \frac{2T}{N_o}(\pi D_{ch})^2 \sin^2(\pi\Omega) e^{-2\pi D_{ch}|\Omega|}. \tag{2.17}$$

Substituting (2.17) in (2.13), the timing function becomes

$$\rho_{ML}(\tau) = \frac{4T\pi^3 D_{ch}^2}{N_o} \int_{-\infty}^{\infty} \Omega e^{-2\pi D_{ch}|\Omega|} A(e^{j2\pi\Omega}) \sin^2(\pi\Omega) \sin(2\pi\Omega\tau) d\Omega \ . \tag{2.18}$$

Without loss of generality, we normalize the noise power spectral density $N_o/2$ to 1. We want to study the timing function for different cases of input data sequence, viz. uncorrelated data, rate 2/3 (1,7) coded data, and rate 16/17 (0,6/6) coded data, and periodic training data with periods $4T$ and $6T$. The $4T$ and $6T$ patterns are given by '$\cdots++--++--\cdots$' and '$\cdots+++---+++---\cdots$', respectively. For uncorrelated data with unit power, $A(e^{j2\pi\Omega}) = 1$ for all Ω. For the training data with periods of $4T$ and $6T$ with unit power, $A(e^{j2\pi\Omega}) = \frac{1}{2}\sum_{n=-\infty}^{\infty}[\delta(\Omega+\Omega_0+n)+\delta(\Omega-\Omega_0-n)]$ for $\Omega_0 = 1/4$ and $\Omega_0 = 1/6$, respectively. Note that $\delta(\Omega)$ is Dirac's delta function. That is, for any function $f(\Omega)$, $\int_{-\infty}^{\infty} f(\Omega)\delta(\Omega-\Omega_0)d\Omega = f(\Omega_0)$. Here, for periodic preambles, we assume that the power in the harmonics is negligible compared to that in the fundamental. This, in conjunction with the attenuation provided by the channel, implies that we can neglect the harmonic contents at the channel output. For the rate 2/3 (1,7) and rate 16/17 (0,6/6) RLL coded data, the PSD can be evaluated numerically. We show the PSDs of 2/3 (1,7) and 16/17 (0,6/6) coded data in Fig. 2-11. Using these PSDs in (2.18), we can evaluate the timing function of the DA ML TED for the Lorentzian channel model for various user densities D_u.

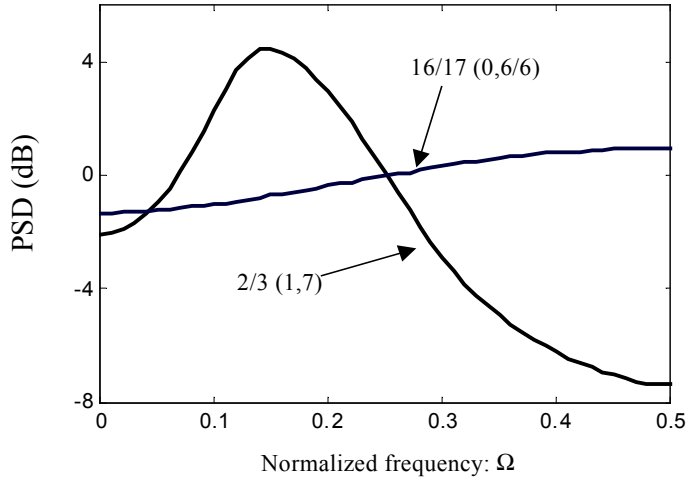


Fig. 2-11: Power spectral densities of 2/3 (1, 7) and 16/17 (0, 6/6) RLL coded data.

Fig. 2-12 shows the timing functions for the cases of uncorrelated data and training data with periods $4T$ and $6T$. Similarly, Fig. 2-13 shows the timing functions for the cases of data coded with 16/17 (0,6/6) and 2/3 (1,7) RLL codes. These figures show that the value of user density D_u and the degree of randomness of the input data are two dominating factors that influence the TED gain. The TED gain is the slope of the timing function at the origin (i.e.

slope at the ideal timing phase) and it represents the TED sensitivity to timing phase errors in the incoming signal. The greater the TED gain, the better will be the ability of the TED to detect even small timing phase errors, and vice versa. Observe that the TED gain decreases as data becomes more random-like or as the user density increases. For low recording density or periodic training data, the TED gain tends to become high. This explains why it is desirable to use periodic preamble data during timing acquisition. Compared to the situations of low recording density and the use of periodic training data, timing recovery becomes more difficult with random data as the user density increases.

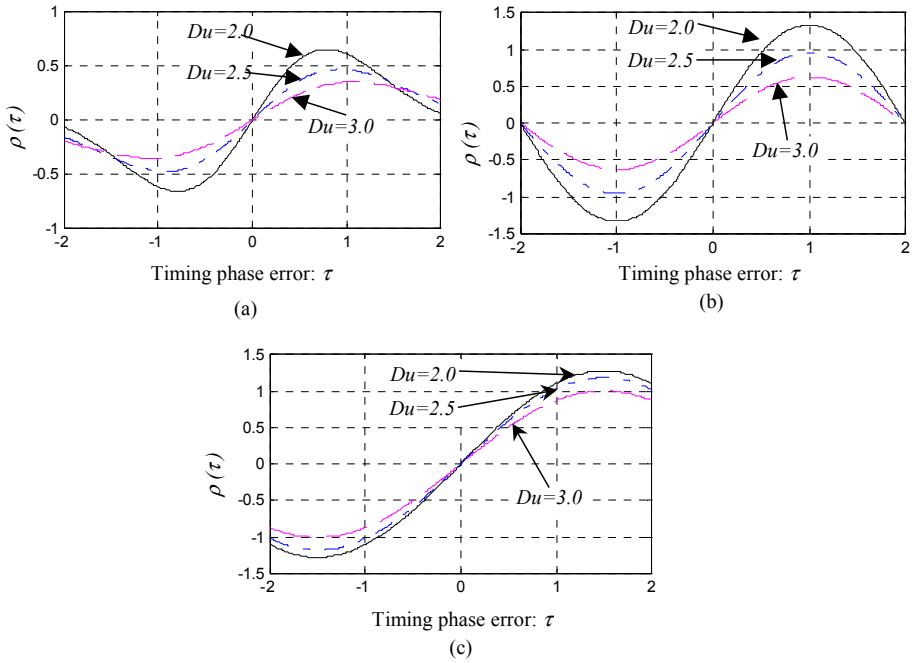


Fig. 2-12: ML TED timing functions for the Lorentzian channel at different user densities D_u with (a) uncorrelated data, (b) 4*T*-training data, and (c) 6*T*-training data.

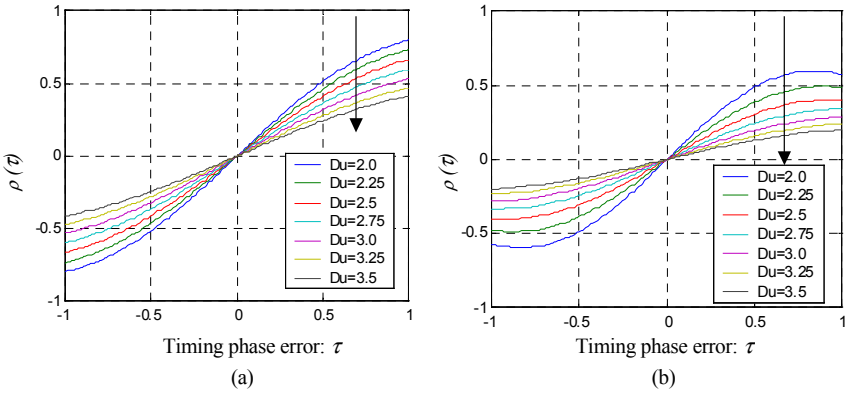


Fig. 2-13: ML TED timing functions for the RLL coded Lorentzian channel at different user densities D_u with (a) 2/3 (1,7) coded data and (b) 16/17 (0, 6/6) coded data.

The ML TED performance can be assessed using the TED efficiency defined in (2.7). Using (2.7), (2.8) and (2.13), the ML TED efficiency can be evaluated as [18]

$$\gamma_{ML} = \frac{\int_{-\infty}^{\infty} (2\pi\Omega)^2 A(e^{j2\pi\Omega}) \,|\, H(\Omega) \,|^2 \, d\Omega}{\int_{-\infty}^{\infty} |\, H(\Omega) \,|^2 \, d\Omega}. \tag{2.19}$$

Because of the presence of Ω^2 in the numerator, the high frequency components of $A(e^{j2\pi\Omega})$ and $H(\Omega)$ have significant contribution to efficiency. Thus, for optimum efficiency, the data should have its energy concentrated at those frequency regions where $\Omega^2 \,|\, H(\Omega) \,|^2$ is large. Consequently, sinusoidal data with a proper frequency will result in better efficiency compared to random data.

For the Lorentzian channel, substituting (2.17) in (2.19), we get

$$\gamma_{ML} = 8\pi^3 D_{ch}(1+D_{ch}^2)\int_{-\infty}^{\infty} \Omega^2 A(e^{j2\pi\Omega}) \sin^2(\pi\Omega) e^{-2\pi D_{ch}|\Omega|} d\Omega. \tag{2.20}$$

We use (2.20) to evaluate the ML TED efficiency for the Lorentzian magnetic recording channel with input training patterns $2T$ (‘+−’), $4T$ (‘++−−’), $6T$ (‘+++−−−’), and $8T$ (‘++++−−−−’), and random data coded with rate 2/3 (1,7) code and rate 16/17 (0,6/6) code. The calculation results are shown in Fig. 2-14. Here, the vertical axis is in dB and the horizontal axis is the channel density D_{ch}. Observe that the pseudo-random data, such as uncorrelated data and the 16/17 (0, 6/6) and 2/3 (1,7) coded data, generally yields a much lower γ_{ML} than the periodic patterns for from medium to high densities. This is expected because of the Ω^2 term in (2.20), as explained above.

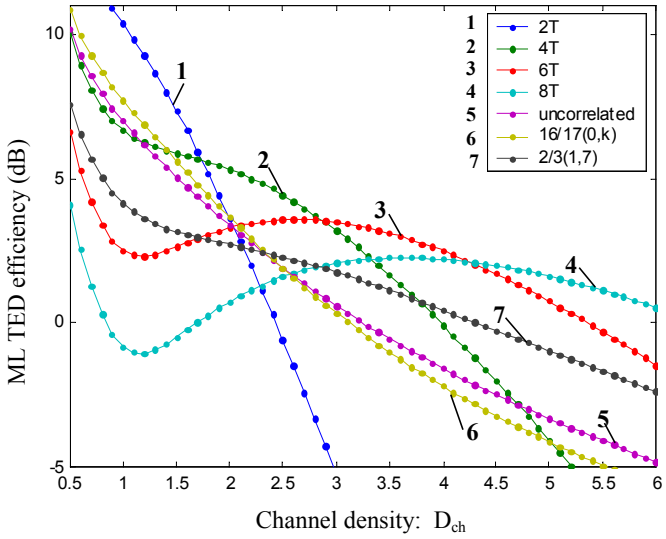


Fig. 2-14: ML TED efficiency for the Lorentzian recording channel with various data patterns versus the channel density.

Fig. 2-14 shows that the $2T$ pattern is unsuited for high densities. This is because the recording channel response has little content at the Nyquist frequency $1/(2T)$ and its bandwidth decreases rapidly with the channel density D_{ch}. The efficiency γ_{ML} declines, in general, with D_{ch}. But, the γ_{ML} curves for $6T$ and $8T$ are non-monotonic. This is because the term

$(2\pi\Omega)^2 |H(\Omega)|^2$ is non-monotonic in D_{ch} for the Lorentzian channel with the 6T or 8T pattern. Fig. 2-14 also shows that, for medium to high channel densities, the 6T and 8T patterns outperform the 4T pattern, and the (1,7) coded data outperforms the (0,k) coded data. However, if we account for the code rate by plotting Fig. 2-14 with user density on the horizontal axis, we will find that the efficiencies resulting from the (1,7) and (0,k) coded data are comparable.

2.3.2 Minimum Mean-Square Error (MMSE) timing recovery

Applying the principle of the Least-Mean-Square (LMS) adaptation technique [52, Chapter 6] to timing recovery leads to MMSE timing recovery schemes. That is, the timing information is obtained as the instantaneous gradient, with respect to phase, of an appropriate error signal [11] [18]. Following [3, Chap. 10], we give a brief review of MMSE TED approaches.

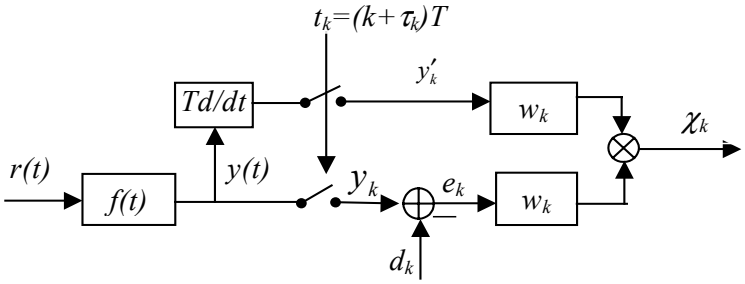


Fig. 2-15: TED structure of MMSE timing recovery scheme.

Fig. 2-15 depicts the MMSE TED structure. The continuous-time prefilter with impulse response $f(t)$ is such that its output $y(t)$, when sampled at the correct phase, approximates a certain desired sequence d_k. So an error e_k is formed as $e_k = y_k - d_k$ where y_k is the sampled output of the prefilter. Since the noise at the prefilter output may not be white, a whitening filter with taps w_k is used to whiten the noise. This is because MMSE and ML are equivalent when the underlying noise is white Gaussian and the channel has no excess bandwidth. Hence, the aim is to adjust the phase by minimizing the power of the whitened error signal $(e \otimes w)_k$ where '$\otimes$' denotes convolution. Observe that $\frac{\partial (e \otimes w)_k^2}{\partial \tau} = 2(e \otimes w)_k (y' \otimes w)_k$ where $y'_k \triangleq T\frac{dy(t)}{dt}\Big|_{t=(k+\tau_k)T}$ is the sampled derivative of the prefilter output $y(t)$. Thus, the output of MMSE TED in Fig. 2-15 is given by

$$\chi_k = (e \otimes w)_k (y' \otimes w)_k . \tag{2.21}$$

The timing loop acts to force the average of χ_k towards zero and in doing so minimizes the power of $(e \otimes w)_k$. Note that many of the existing MMSE schemes merely minimize the power of e_k yielding a suboptimal version as [21] [41]

$$\chi_k = e_k y'_k . \tag{2.22}$$

Note from Fig. 2-15 that the MMSE TED needs two samplers that are required to operate in exact synchronism. This makes its practical implementation difficult. To circumvent this, it

has been proposed to generate the samples y'_k from y_k using a discrete-time differentiator, instead of an additional sampler [18]. This leads to the simplified structure shown in Fig. 2-16.

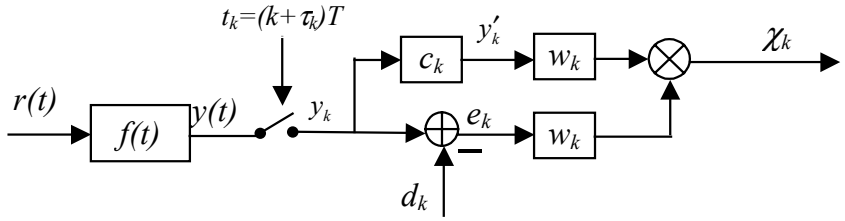


Fig. 2-16: Simplified TED structure of MMSE timing recovery scheme.

If $y(t)$ has zero excess bandwidth, then y'_k can be generated from y_k by using an ideal differentiator with discrete-time impulse response c_k given by [2]

$$c_k = \begin{cases} 0, & k = 0 \\ \dfrac{(-1)^k}{k}, & k \neq 0. \end{cases} \tag{2.23}$$

In practice, the response c_k may be limited to the first few terms when excess bandwidth is insignificant. A common practice has been to use just the three center-taps of c_k, viz. $c_{-1}=1$, $c_0=0$ and $c_1=-1$. This approximation for a simplified MMSE timing recovery scheme has been widely used in various applications [2] [42]. The performance of the simplified scheme is comparable to the original scheme of Fig. 2-15 [18].

Let $q(t) = (h \otimes f)(t)$ be the band-limited equalized channel response up until the prefilter output. Then, with $q_k = q(t)|_{t=kT}$, $q_k^\tau = q(t)|_{t=(k+\tau)T}$ and $p_k^\tau = T\left.\dfrac{dq(t)}{dt}\right|_{t=(k+\tau)T}$, we can write

$$y'_k = T\left.\frac{dy(t)}{dt}\right|_{t=(k+\tau)T} = (a \otimes p^\tau)_k \tag{2.24}$$

$$y_k = y(t)|_{t=(k+\tau)T} = (a \otimes q^\tau)_k + v_k \tag{2.25}$$

where v_k is the noise part of y_k. Further, let g_k be the target response such that $d_k = (a \otimes g)_k$. Then, substituting for $e_k = y_k - d_k$ and y'_k in (2.21) using these expressions, we get the timing function for MMSE TED as

$$\rho_{MS}(\tau) = \int_{-0.5}^{0.5} (j2\pi\Omega) QA\,|W|^2\,(Qe^{j2\pi\Omega\tau} - G)^* e^{j2\pi\Omega\tau} d\Omega \tag{2.26}$$

where Q, G, and W are the Fourier transforms of q_k, g_k and w_k, respectively, A is the PSD of the data sequence a_k, and X^* denotes the conjugate of a complex quantity X. For the sake of convenience, these frequency domain quantities are written without the argument $e^{j2\pi\Omega}$ in (2.26). The above expression (2.26) does not contain a noise term since the cross-correlation of the noise components in y_k and y'_k is odd-symmetric about the origin. The resulting TED efficiency is

$$\gamma_{MS} = \frac{1}{SNR_m} \frac{[\int_{-0.5}^{0.5} (2\pi\Omega)^2 A |Q|^2 |W|^2 \, d\Omega]^2}{\int_{-0.5}^{0.5} (2\pi\Omega)^2 A |Q|^2 |W|^4 \, V d\Omega} \tag{2.27}$$

where V is the PSD of noise v_k in y_k.

For the simplified MMSE timing recovery, the timing function is

$$\tilde{\rho}_{MS}(\tau) = \int_{-0.5}^{0.5} AQC(Qe^{j2\pi\Omega\tau} - G)^* |W|^2 \, e^{j2\pi\Omega\tau} d\Omega \tag{2.28}$$

where C is the Fourier transform of the impulse response c_k of the differentiator. The corresponding TED efficiency is given by

$$\tilde{\gamma}_{MS} = \frac{1}{SNR_m} \frac{[\int_{-0.5}^{0.5} j2\pi\Omega AQCG^* |W|^2 \, d\Omega]^2}{\int_{-0.5}^{0.5} A|Q|^2 |C|^2 |W|^4 \, V d\Omega}. \tag{2.29}$$

2.3.3 Zero-Forcing (ZF) timing recovery

The origin of ZF timing recovery can be traced back to the work of Mueller and Müller [1]. The ZF timing recovery technique provides an alternative and usually cheaper approach towards achieving near ML performance. It has been applied to a variety of codes, channels and detection techniques [1] [20] [43] [15] [16] [19]. The principle of the ZF approach is to generate the control information by cross-correlating a filtered form of the data a_k with an error e_k that represents the difference between the actual and desired inputs of the detector. The control loop acts to eliminate this cross-correlation in order to force intersymbol interference components to zero.

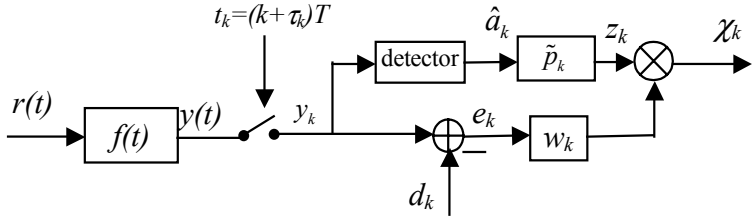


Fig. 2-17: TED structure of a ZF timing recovery scheme.

The ZF TED structure is depicted in Fig. 2-17 [3, Chap. 10]. It is very similar to the simplified MMSE scheme in Fig. 2-16. The derivative component y_k' in Fig. 2-16 is replaced by z_k in Fig. 2-17. The signal z_k is produced from the decisions $\hat{a}_k$ rather than from the noisy signal $y(t)$ or the sampler output y_k. The resulting ZF TED output is

$$\chi_k = (e \otimes w)_k z_k = (e \otimes w)_k (\hat{a} \otimes \tilde{p})_k \tag{2.30}$$

where $\tilde{p}_k$ is the impulse response of the filter used for generating the local reference z_k, which is normally chosen as $(w \otimes p)_k$ where p_k is the sampled derivative of the equalized channel response $q(t)$. Thus, the additional sampler and differentiator required in the MMSE schemes

are avoided in the ZF scheme. The timing loop acts to eliminate all cross-correlation between e_k and z_k, thereby forcing a linear combination of ISI components towards zero. ML performance will accrue when w_k and p_k are properly chosen and aliasing is avoided.

The timing function for the ZF TED given in Fig. 2-17 is [3, Chap. 10]

$$\rho_{ZF}(\tau) = \int_{-0.5}^{0.5} A(Qe^{j2\pi\Omega\tau} - G)W\tilde{P}^* d\Omega \tag{2.31}$$

where $\tilde{P}$ denotes the Fourier transform of the filter response $\tilde{p}_k$ in the reference path, i.e. $\tilde{P} = WP$ where P is the Fourier transform of the response p_k. Finally, the ZF TED efficiency can be obtained as

$$\gamma_{ZF} = \frac{1}{SNR_m} \frac{[\int_{-0.5}^{0.5} A|\tilde{P}|^2 \, d\Omega]^2}{\int_{-0.5}^{0.5} A|\tilde{P}|^2 |W|^2 \, Vd\Omega}. \tag{2.32}$$

Finally, we summarize the approaches of MMSE and ZF timing recovery schemes. In the MMSE scheme, timing-error information is produced by correlating the filtered error $(e \otimes w)_k$ with a noisy reference sequence $(y' \otimes w)_k$. This approach has various disadvantages. First, it requires a second sampler to produce y'_k (the simplified MMSE approach removes this drawback). Secondly, formation of $(e \otimes w)_k (y' \otimes w)_k$ is comparatively complicated when carried out digitally. Thirdly, when the data a_k exhibits long runs of identical symbols, the TED output will be fully induced by noise. As a result, the TED may suffer from additional noise-induced jitter. The advantage of MMSE approach is that it minimizes the mean-square error (MSE) at the detector input. Compared to the MMSE TED, the ZF TED provides an alternative and much cheaper approach aiming at ML performance. It has none of the three disadvantages mentioned above, thus presenting an extraordinarily simple and effective scheme for timing recovery. The resulting MSE can be poorer than that of an MMSE scheme. This may be a potential disadvantage of ZF timing recovery.

2.4 Timing Acquisition

The purpose of timing acquisition techniques is to acquire the correct sampling phase before the detection of user data begins. This task is accomplished during a limited length of the preamble that precedes the user data. The acquisition behavior depends not only on the preamble pattern but also on the TED scheme used. Compared to the TED used during the tracking mode of timing recovery, the TED schemes during the acquisition mode are almost always fitted with special mechanisms to ensure fast and accurate acquisition of the timing phase. In this section, we discuss the main problems that may occur during timing acquisition, solutions to take care of these, and some measures for evaluating the acquisition performance.

2.4.1 Timing acquisition problems: false lock and hang up

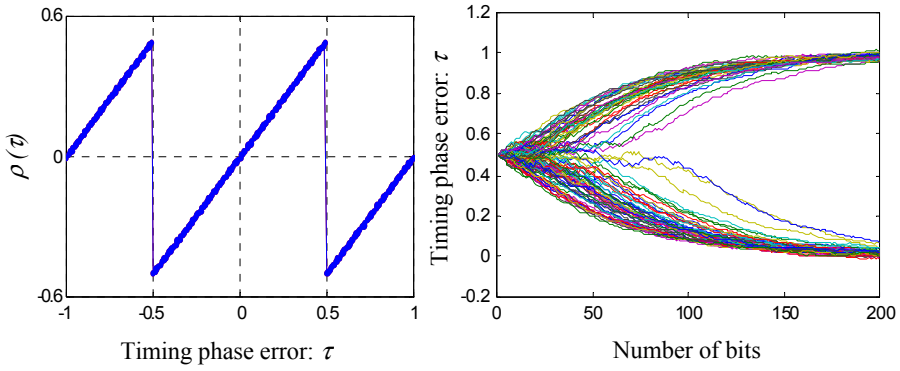
In the acquisition mode, the phase of the recovered clock varies over a considerable range since the initial phase may deviate far from the correct phase. In the presence of large timing phase errors, the timing function becomes highly nonlinear and the TED may even fail to give a

proper indication of the timing phase error. Further, with large timing phase errors, the bit decisions from the receiver are most likely erroneous. In such situations, two serious problems that the timing recovery loop may face are false lock and hang up. False lock means that the timing loop gets locked to a wrong phase. Hang up means that the timing loop takes a long period of time to get out of certain intervals of incorrect phases. Occurrence of false lock results in complete failure of acquisition, whereas hang up results in retarding the acquisition process significantly. Therefore, a serious consideration of these two problems is critical and essential for ensuring a fast and reliable timing acquisition. This section elaborates the problems of false lock and hang up, emphasizing why they occur and how to avoid them.

A. Hang up

The timing phase generated by the PLL loop may dwell at incorrect phases for prolonged intervals of time before the loop settles to equilibrium on the correct phase. This phenomenon is known as hang up and it was first investigated for time division multiple access (TDMA) modems [44]. Since the PLL always settles eventually and hang up is a low probability event, the hang up problem has been obscure for most PLL users who do not require fast acquisition. However, hang up is very troublesome for applications in magnetic recording systems where fast timing acquisition is absolutely necessary.

The reason for the occurrence of hang up is that the timing function has no response or unstable nulls at one or more undesired phases. Fig. 2-18(a) illustrates one such timing function. Observe that the timing function is discontinuous at the timing phase errors ±0.5 (normalized in units T). Fig. 2-18(b) shows the closed-loop phase convergence curves (at the PLL output) based on this timing function for 100 trials. In this experiment, the initial timing phase error is fixed at +0.5 and the noise level is such that the root-mean-square (RMS) jitter value at the output is 0.05. Observe that the convergence curves show a very sluggish behavior in moving away from the initial timing phase error 0.5. The hang up phenomenon illustrated here is caused by the TED that yields outputs with different signs at either sides of the discontinuous timing phase error 0.5. In the presence of noise, the loop phase is misled to move in inconsistent directions thereby resulting in hang up. Observe that the worst case delay in Fig. 2-18(b) is nearly 100 bits for the loop to begin moving away from the initial phase. Such a large delay is intolerable for timing acquisition in magnetic recording.

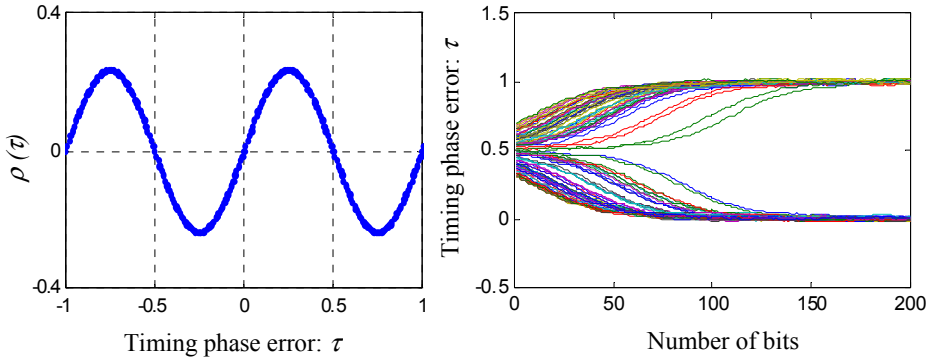


(a) Timing function with unstable nulls at τ=±0.5

(b) Closed-loop phase convergence curves (RMS jitter = 0.05)

Fig. 2-18: Demonstration of hang up problem when the unstable nulls in the timing function arise from discontinuities.

Hang up may also occur when the slope of the timing function at undesired nulls is opposite to that at the correct phase. One such hang up example is demonstrated in Fig. 2-19. Observe that the timing function in Fig. 2-19(a) is continuous at the nulls at ±0.5. Further, these nulls are unstable since for timing phase errors around ±0.5, the TED makes the timing phase drift in opposite directions. In the presence of noise, if the initial phase happens to occur near these unstable nulls, the loop phase will linger around these nulls over a prolonged period of time before it consistently converges to the desired phase. One such example is shown in Fig. 2-19(b). The sluggish convergence of the phase caused by hang up arising from the unstable nulls at 0.5 is clearly illustrated. These nulls would not cause false lock since false lock requires the correct slope in the vicinity of the zero crossing, which is not true for the zeros in the case considered here. In practice, since timing phase errors at ±0.5 are unstable, even small noise at the TED input can make the phase drift away from these unstable phases and eventually converge to one of the desired phases. Therefore, hang up is more probable than false lock in this case.

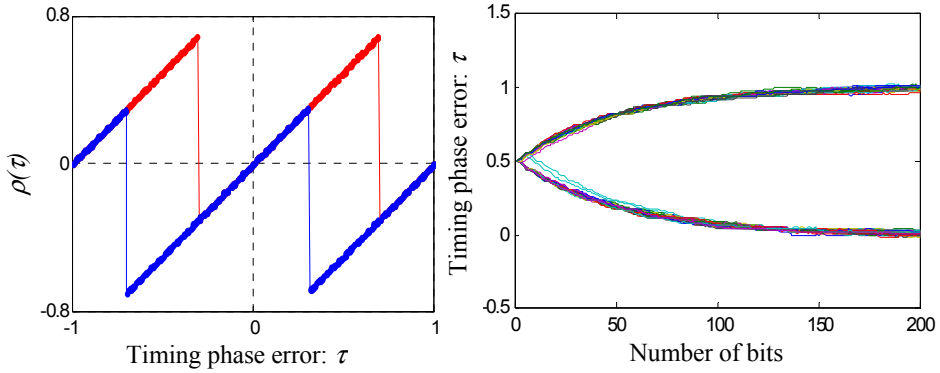


(a) Timing function with unstable nulls at ±0.5

(b) Closed-loop phase convergence curves (RMS jitter = 0.05)

Fig. 2-19: Demonstration of hang up problem when the timing function has undesired nulls with wrong slopes.

Hang up can be avoided by applying a large restoring force in the chosen direction whenever the timing phase in the loop is near the unstable nulls. This can be accomplished by adding hysteresis into the timing function in order to prevent the timing loop from ever dwelling near these undesired phases. Fig. 2-20(a) illustrates such an example, showing a significant hysteresis range in the timing function over the problematic unstable phase intervals around ±0.5. The timing function is made up of parallel and partially overlapped linear segments. At any point in time, one of these segments is active and uniquely determines the TED output for the corresponding input. The TED output follows the changes of the input until the end of a segment is reached. Then, the TED output jumps to the nearest segment. At that point, the TED output is sharply decreased towards zero, implying that the phase is close to the desired one. Therefore, the timing loop is likely to lock to this desired timing phase. Because of the hysteresis in the timing function, there are no longer any unstable nulls at which the loop might hang up for a prolonged period. Using this TED and the initial phase 0.5, we studied the closed-loop phase convergence curves with the noise power selected to result in 0.05 RMS phase jitter. The result is illustrated in Fig. 2-20(b). As expected, all the curves converge to the desired timing phases within 100 bits. No hang up occurs even during the first 50 bits.



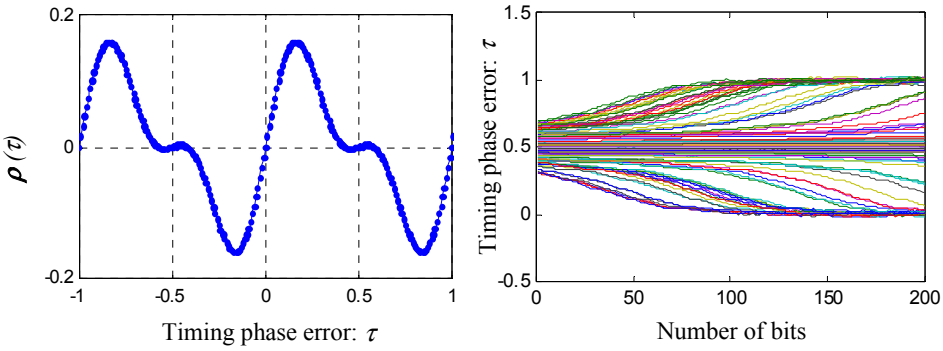
(a) Timing function with hysteresis

(b) Closed-loop phase convergence curves (RMS jitter = 0.05)

Fig. 2-20: Demonstration of how hang up can be avoided by incorporating hysteresis in the timing function.

B. False lock

The TED is expected to produce zero output only for the desired input phase, thus forcing the timing loop to lock on this input phase. However, if the TED yields zero output (i.e. timing function becomes zero) for any undesired phases as well, then the timing loop may lock on these incorrect phases, thereby resulting in false lock. Occurrence of false lock may lead to failure of the timing acquisition process. For this reason, false lock must be avoided at any cost. This is even more important in DFE read channels since erroneous past decisions can easily induce false lock under random initial conditions [47].



(a) Timing function with false lock phases at ± 0.5

(b) Closed-loop phase convergence curves (RMS jitter = 0.05)

Fig. 2-21: Demonstration of false lock phenomenon arising from undesired zero-crossings of the timing function.

Consider the timing function shown in Fig. 2-21(a). Apart from the zero-crossings for integer values of τ, which correspond to the desired phases, there are also spurious zero crossings around ±0.5. The effect of this timing function is illustrated in Fig. 2-21(b), which shows 100 runs of phase convergence curves embedded in 5% RMS jitter. The initial timing phase error is uniformly distributed in the range [0.3, 0.7]. Observe that the curves with initial phase errors located around +0.5 fail to converge to the desired timing phase. Thus, due to the

zero crossings of the timing function at the undesired phases ±0.5, the timing acquisition with initial timing phase errors around ±0.5 is doomed to result in acquisition failure. We may remark that the phase ambiguity resulting from the convergence of the timing loop to non-zero integer values of τ (e.g. ±1) is of no big concern for acquisition. This is because this ambiguity can be easily resolved at the block synchronization stage just before the detection of user data begins.

An effective way to prevent false lock is to determine the cause of false lock and improve the TED algorithm to prevent the underlying phenomenon. False lock can also be avoided by ensuring that the initial phase is near a desired phase. A periodic clock run-in pattern of preamble is used to this end and the prior knowledge of the preamble pattern is exploited. Another way is to use a non decision-aided deductive TED architecture for acquisition so that false lock arising from initial erroneous decisions can be prevented [45, 42].

2.4.2 TED solutions for reliable acquisition

We now briefly discuss two examples of TED schemes that do not suffer from false lock and hang up. These examples illustrate the typical principles that one may use while working in the decision-directed mode or non-decision-directed mode of timing acquisition.

A. Decision-directed TED schemes

Consider the decision-directed (DD) timing acquisition scheme presented in [16] for PR-IV recording systems. The TED output is given by $\chi_k = y_{k-1}\hat{x}_k - y_k\hat{x}_{k-1}$, where y_k is the input of the partial response detector and $\hat{x}_k$ is the estimate of the ideal value of y_k. The estimate $\hat{x}_k$ is usually obtained by passing y_k through a comparator with multiple thresholds. The DD TED schemes exploit the knowledge of the preamble pattern for ensuring the correctness of $\hat{x}_k$. Using the $4T$ pattern as the preamble, the ideal detector input is $x_k = a_k - a_{k-2} = 2a_k$, which takes on only two values {+2, -2}. This special structure of x_k is exploited to minimize errors in the estimates $\hat{x}_k$. Instead of using zero as the comparator threshold for making decisions, a variable threshold mechanism given by

$$\hat{x}_k = \begin{cases} 2 & \text{if } y_k \geq 2\text{sgn}(\hat{x}_{k-2}) \\ -2 & \text{if } y_k < 2\text{sgn}(\hat{x}_{k-2}) \end{cases} \tag{2.33}$$

is used for obtaining $\hat{x}_k$ from y_k [16] [46]. Here, $\text{sgn}(x)$ is the sign-function. The variable threshold used here provides hysteresis as well as a large boost in the noise margin while detecting x_k. This makes the TED immune to problems arising from erroneous decisions during acquisition.

For fast and reliable acquisition in DFE recording systems, two novel solutions to DD TED schemes are proposed in Chapter 5. One solution uses a special equalizer and several switches to ensure the correctness of the decisions at the slicer output [47]. Another solution employs a modified threshold filter to help the detector make reliable decisions and to introduce hysteresis in the TED transfer function [48]. It is shown using simulation results that the proposed TED schemes help to effectively prevent false lock and hang up problems.

B. Non-decision-directed TED schemes

The DD TED schemes inevitably introduce a delay between the signal samples at the sampler output and the TED output. This delay is not desirable since it can degrade the timing loop performance and stability [3, Chap. 11]. The non-decision-directed (NDD) schemes, on the other hand, form the TED output directly based on the equalizer or detector input without having to know the decisions. Thus, the NDD TED schemes can effectively eliminate a large part of the latency in the timing loop.

It is shown in [45, 49, 28, 50] that a near-optimum acquisition phase can be determined via the 'band-edge component maximization' (BECM) technique. We briefly present the principle of BECM here. Assume that the channel response *h(t)*, whose Fourier transform is $H(\Omega)$, has less than 100% excess bandwidth and that the channel output is sampled at rate $1/T$ with a timing phase error τ normalized in units T. Then, the Fourier transform $H_s(e^{j2\pi\Omega})$ of the sampled channel response within the bandwidth $1/T$ can be written as

$$H_s(e^{j2\pi\Omega}) = \frac{H(\Omega)e^{j2\pi\Omega\tau} + H(\Omega-1)e^{j2\pi(\Omega-1)\tau}}{T} \quad \text{for} \quad 0 \le \Omega \le 1. \tag{2.34}$$

The BECM technique suggests that the optimum phase for sampling the replay signal should maximize the magnitude of $H_s(e^{j2\pi\Omega})$ at the Nyquist frequency $\Omega_n = 0.5$. Since the Lorentzian model for the step response in magnetic recording is an even function (see eq. (2.15)), it can be easily seen that $H(-0.5) = H(0.5)$. Using this in (2.34), we get

$$H_s(e^{j\pi}) = \frac{H(0.5)e^{j\pi\tau} + H(-0.5)e^{-j\pi\tau}}{T} = \frac{2\cos(\pi\tau)}{T}H(0.5) \tag{2.35}$$

which results in the optimum sampling phase at

$$\tau = k \quad \text{for integer } k\,. \tag{2.36}$$

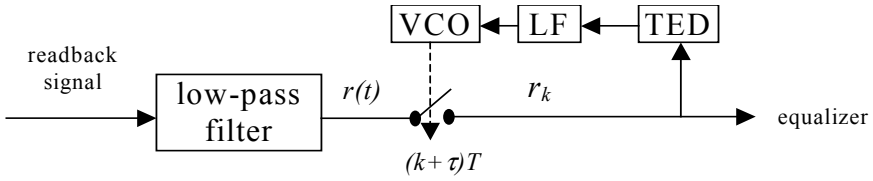


Fig. 2-22: Non-decision-directed TED for timing acquisition in recording systems.

By way of illustration we show in Fig. 2-22 the structure of a NDD TED scheme for timing acquisition in recording systems. The bandwidth of low pass filter is same as that of the channel *H(f)*. The $4T$ pattern '$++--$' and $6T$ pattern '$+++---$' are the most commonly used acquisition preamble patterns for (0, *k*) (e.g. PRML system [16]) and (1,7) (e.g. MDFE system [47]) coded magnetic recording channels. The sampler output sequences at the ideal sampling phase, which result in BECM, are shown in Fig. 2-23 for the Lorentzian channel model in the absence of noise. Exploiting the nature of the patterns formed by the readback signal samples, we developed TEDs that are very simple to implement [51]. The corresponding TED outputs for the $6T$ and $4T$ preambles are given by

$$\chi_k = (r_k + r_{k-1})[\mathrm{sgn}(r_k) - \mathrm{sgn}(r_{k-1})] \quad \text{for the } 6T\text{-preamble} \tag{2.37}$$

and

$$\chi_k = (-1)^k r_k r_{k-1} \qquad \text{for the } 4T\text{-preamble.} \tag{2.38}$$

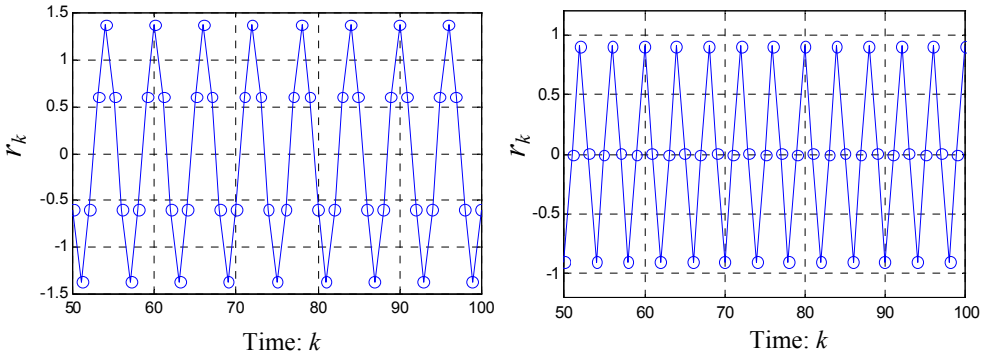


Fig. 2-23: Symbol-rate samples (marked by 'o' at the ideal sampling phase) of replay signal of the Lorentzian recording channel corresponding to (a) 6*T* pattern and (b) 4*T* pattern preamble sequences.

Fig. 2-24 shows the timing functions corresponding to the TEDs given by (2.37) and (2.38) for 6*T* and 4*T* sequences. Observe that the functions are saw-tooth and sinusoidal in nature with zero-crossings located at only the ideal phases. Clearly, the resulting timing acquisition will not suffer from the false lock problem. However, there is a potential that hang up may occur.

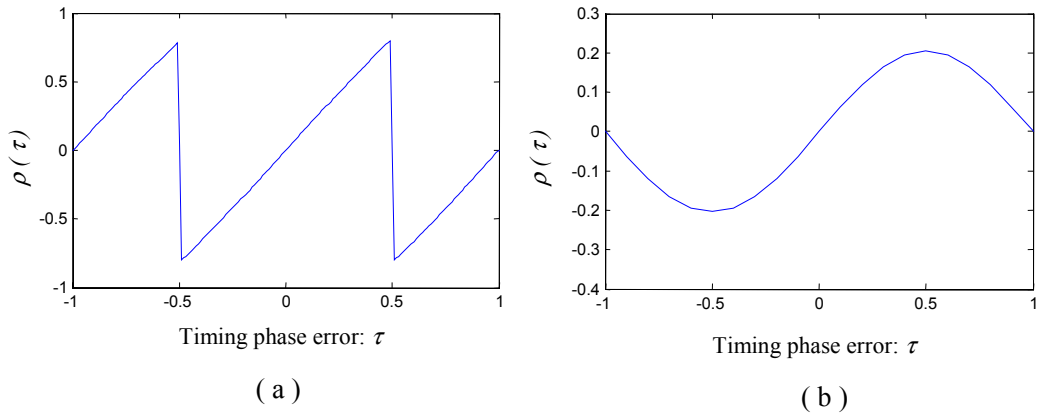


Fig. 2-24: Timing functions corresponding to the NDD TEDs given by (2.37) and (2.38) for using (a) 6*T* pattern and (b) 4*T* pattern preamble sequences.

While the NDD acquisition TED schemes shown above are able to effectively prevent acquisition problems arising from wrong decisions, it is clear that these schemes can not be used in the tracking mode since the input data sequence during tracking is random in nature. Since the detected data during tracking are more reliable, a decision-directed TED can be used during tracking. For this reason, when the timing loop enters the tracking mode, the TED has to be switched into a DD based scheme.

2.4.3 Phase acquisition bound

A quantity that is useful in assessing the quality of timing acquisition is the variance of the phase at the acquisition end. In this section, we analyze the timing acquisition process for a given preamble length, and derive an expression for the resulting phase variance.

During the phase acquisition process, the received signal is essentially a sinusoid since the input data sequence (i.e., the preamble) is periodic in nature. The channel, being band-limited, is assumed to reject the harmonic components of the periodic input data except for the fundamental. To study the phase acquisition bound, we assume that the received signal is sampled at rate $1/T$ and the phase is estimated using N samples. The resulting samples are given by

$$y_k = A_c \sin(2\pi\Omega_c k + \phi) + n_k, \quad 0 \le k \le N-1 \tag{2.39}$$

where Ω_c is the fundamental frequency of the preamble sequence that is normalized with respect to $1/T$, A_c is the sinusoidal amplitude which is determined by the channel transfer function at frequency Ω_c, ϕ is the phase to be estimated and is assumed to be uniformly distributed over the interval $[-\pi, \pi)$, and noise n_k is the channel noise and is assumed to be white and Gaussian with zero mean and variance σ_n^2.

For the observation of N samples $y_0, y_1, \ldots, y_{N-1}$, define $\mathbf{y} = [y_0 \quad y_1 \quad \cdots \quad y_{N-1}]$. An obvious approach would be to estimate the phase $\phi \in [-\pi, \pi)$ by maximizing the posteriori probability density function (PDF) $p(\phi \mid \mathbf{y})$. With the help of Bayes' rule we may write $p(\phi \mid \mathbf{y}) = \dfrac{p(\mathbf{y} \mid \phi) p(\phi)}{p(\mathbf{y})}$ where $p(\mathbf{y} \mid \phi)$ is the conditional PDF of $\mathbf{y}$ for a given phase ϕ, $p(\mathbf{y})$ is the PDF of $\mathbf{y}$, and $p(\phi)$ is the prior PDF of phase ϕ. Since $p(\mathbf{y})$ does not depend on ϕ and ϕ is uniformly distributed in $[-\pi, +\pi]$, maximization of $p(\phi \mid \mathbf{y})$ boils down to maximization of $p(\mathbf{y} \mid \phi)$. This leads to the maximum-likelihood (ML) estimate of the phase ϕ.

We note from (2.39) that for a given ϕ, the variables y_k are independent and Gaussian distributed with mean $A_c \sin(2\pi\Omega_c k + \phi)$ and variance σ_n^2. Hence, $p(\mathbf{y} \mid \phi)$ can be written as

$$p(\mathbf{y} \mid \phi) = \left(\frac{1}{2\pi\sigma_n^2} \right)^{N/2} \exp\left\{ -\frac{1}{2\sigma_n^2} \sum_{k=0}^{N-1} \left| y_k - A_c \sin(2\pi\Omega_c k + \phi) \right|^2 \right\}. \tag{2.40}$$

The term $\sum_{k=0}^{N-1} | y_k - A_c \sin(2\pi\Omega_c k + \phi) |^2$ can be expanded as

$$\sum_{k=0}^{N-1} | y_k |^2 + \frac{N A_c^{\,2}}{2} - \frac{A_c^{\,2}}{2} \sum_{k=0}^{N-1} \cos(4\pi\Omega_c k + 2\phi) - 2\sqrt{B^2 + C^2} \cos(\phi - \phi_0) \tag{2.41}$$

where $B = \sum_{k=0}^{N-1} y_k \sin(2\pi\Omega_c k)$, $C = \sum_{k=0}^{N-1} y_k \cos(2\pi\Omega_c k)$, and $\phi_0 = \tan^{-1}\left(\dfrac{C}{B}\right)$. By choosing N appropriately so as to make the acquisition period NT considerably longer than the preamble period $1/f_c$, the third term of (2.41) amounts to zero. Substituting (2.41) in (2.40), we get

$$p(\mathbf{y} \mid \phi) = \tilde{\alpha} \exp\left\{ \tilde{\beta} \cos(\phi_0 - \phi) \right\} \tag{2.42}$$

where $\tilde{\alpha} = \left(\frac{1}{2\pi\sigma_n^2}\right)^{N/2} \exp\left\{-\frac{1}{2\sigma_n^2}\left(\sum_{k=0}^{N-1} |y_k|^2 + \frac{NA_c^2}{2}\right)\right\}$ and $\tilde{\beta} = \frac{A_c\sqrt{B^2+C^2}}{\sigma_n^2}$. Since $\tilde{\alpha}$ and $\tilde{\beta}$ are positive scalars, the value of ϕ which maximizes $p(\mathbf{y}|\phi)$ in (2.42) is equal to ϕ_0. That is, the ML estimate of the phase is given by

$$\hat{\phi}_{ML} = \phi_0 = \tan^{-1}\left(\frac{\sum_{k=0}^{N-1} y_k \cos(2\pi\Omega_c k)}{\sum_{k=0}^{N-1} y_k \sin(2\pi\Omega_c k)}\right), \quad -\pi \le \hat{\phi}_{ML} < \pi. \tag{2.43}$$

This result is identical to the ML estimate of the phase of an unmodulated carrier, as shown in [52, Chap. 6]. The statistical behavior of (2.43) is also studied in [52, Chap. 6] [53]. The result shows that the conditional PDF of $\hat{\phi}_{ML}$, for a given ϕ, is determined by the number of samples N in $\mathbf{y}$ and the signal-to-noise ratio $\gamma \triangleq A_c^2/(2\sigma_n^2)$ according to the expression

$$p_{\hat{\phi}_{ML}}(\hat{\phi}|\phi) = e^{-N\gamma}[1+\sqrt{4\pi N\gamma}\cos(\hat{\phi}-\phi)e^{N\gamma\cos^2(\hat{\phi}-\phi)}Q(-\sqrt{2N\gamma}\cos(\hat{\phi}-\phi))], \quad \hat{\phi}\in[-\pi,\pi). \tag{2.44}$$

Using the fact that $p_{\hat{\phi}_{ML}}(\hat{\phi}|\phi)$ is the circularly shifted version of $p_{\hat{\phi}_{ML}}(\hat{\phi})$ restricted by phase ϕ in the range $[-\pi,\pi)$, one can readily verify that the PDF of $\hat{\phi}$ can be obtained as

$$p_{\hat{\phi}_{ML}}(\hat{\phi}) = \frac{e^{-N\gamma}}{2\pi}[1+\sqrt{4\pi N\gamma}\cos\hat{\phi}\cdot e^{N\gamma\cos^2\hat{\phi}}Q(-\sqrt{2N\gamma}\cos\hat{\phi})]. \tag{2.45}$$

Accordingly, the variance of $\hat{\phi}$ is obtained as

$$\begin{aligned}\sigma^2_{\hat{\phi}_{ML}} &= \int_{-\pi}^{\pi}\hat{\phi}^2 p_{\hat{\phi}_{ML}}(\hat{\phi})d\hat{\phi} \\ &= \frac{e^{-N\gamma}}{\pi}\int_0^{\pi}\hat{\phi}^2[1+\sqrt{4\pi N\gamma}\cos\hat{\phi}e^{N\gamma\cos^2\hat{\phi}}Q(-\sqrt{2N\gamma}\cos\hat{\phi})]d\hat{\phi}\end{aligned}. \tag{2.46}$$

This equation produces maximum variance $\sigma^2_{\hat{\phi}_{ML\max}} = \pi^2/3$ when the SNR $\gamma = A_c^2/(2\sigma_n^2)$ decreases to zero, and produces minimum variance $\sigma^2_{\hat{\phi}_{ML\min}} \simeq \frac{\sigma_n^2}{NA_c^2}$ when γ is sufficiently high. Thus, the result (2.46) provides a phase acquisition bound for the observation period of NT seconds during acquisition. In other words, this result indicates that for a preamble with a length of N samples used to estimate an ideal phase, the variance of estimate error cannot be less than $\frac{\sigma_n^2}{NA_c^2}$ and greater than $\frac{\pi^2}{3}$.

2.4.4 Time constant and acquisition speed

The phase adjustment in the timing recovery loop that employs a first-order PLL can be described as

$$\tau_{k+1} = \tau_k - \alpha\chi_k \tag{2.47}$$

where α is a small step size parameter, τ_k is the normalized timing phase error between the VCO output and the PLL input signals at the instant k, and χ_k is the TED output at the instant k. Here, we assume that the VCO has a unity gain factor. Recall from Section 2.1 that the

timing function $\rho(\tau)$, which represents the averaged TED output, is an odd symmetric function about the origin τ=0. Further, $\rho(\tau)$ can be linearized with the slope K_d as in (2.3) over a small area around τ=0, i.e. $\rho(\tau) = K_d\tau$. Beyond this linear area in the range $[-0.5, 0.5]$, $\rho(\tau)$ can be viewed as a nonlinear function of τ, which is in between the two lines with slopes s_1 and s_2, i.e. $|s_1\tau| \le |\rho(\tau)| \le |s_2\tau|$. The slope of $\rho(\tau)$ is usually maximum at the origin τ=0 and minimum at τ=±0.5 in the range $[-0.5, 0.5]$. Thus, we can determine s_1 and s_2 as $s_1 = \rho'(0.5)$ and $s_2 = \rho'(0) = K_d$, respectively, with ρ' representing $\frac{d\rho}{d\tau}$. Normally, both s_1 and s_2 are of non-negative values, i.e. $s_2 \ge s_1 \ge 0$.

We use the simplified model of the timing function described above for analyzing the average convergence behavior of the iteration (2.47). Let $\overline{\tau}_k$ denote the average of τ_k, i.e., $\overline{\tau}_k = E[\tau_k]$. Then, the above model suggests that we can bound $\overline{\tau}_k$ as

$$(1-\alpha s_2)^k |\tau_0| \le |\overline{\tau}_k| \le (1-\alpha s_1)^k |\tau_0| \tag{2.48}$$

where τ_0 is the initial timing phase error in the range $[-0.5, 0.5]$. Further, we model the phase convergence in the linear region as $\overline{\tau}_k = (1-\alpha K_d)^k \tau_0$. In convergence studies, it is a regular practice to specify the convergence speed using a time constant. Accordingly, we let

$$(1-\alpha K_d)^k \tau_0 = e^{-k/\Gamma}\tau_0 \tag{2.49}$$

where Γ denotes an effective time constant value and is given by

$$\Gamma = -\frac{1}{\ln(1-\alpha K_d)}. \tag{2.50}$$

Clearly, Γ is an important parameter for timing acquisition, because it explicitly describes the acquisition phase convergence rate. For instance, the value of time constant Γ indicates the time that is required to reduce the timing phase error by 63.21% in magnitude from the initial value (i.e. e^{-1} times smaller). Usually, a period of four time constants is sufficient for acquisition because the timing phase error reduces to 1.83% of its initial value within this period.

Let us examine the fastest and slowest acquisition situations. The fastest acquisition process is marked by the minimum time constant

$$\Gamma_{\min} = -\frac{1}{\ln(1-\alpha s_2)} = -\frac{1}{\ln(1-\alpha K_d)}, \tag{2.51}$$

and the slowest acquisition process is marked by the maximum time constant

$$\Gamma_{\max} = -\frac{1}{\ln(1-\alpha s_1)}. \tag{2.52}$$

By way of illustration, we show in Fig. 2-25 a timing function and its corresponding phase convergence region, which is bounded by the convergence curves corresponding to the maximum and minimum time constants. Even though $\Gamma_{\max}$ may be significantly larger than $\Gamma_{\min}$, the quantity that is more important during acquisition is $\Gamma_{\min}$. This is because the linearity of the timing function can be assumed to be true over a significantly large range of timing phase errors around $\tau = 0$ by virtue of the special techniques that are normally used during acquisition. This is also true for tracking mode since the timing phase error during

tracking mode is usually confined to a very small region around $\tau = 0$, thereby guaranteeing that $\rho(\tau)$ is linear during tracking.

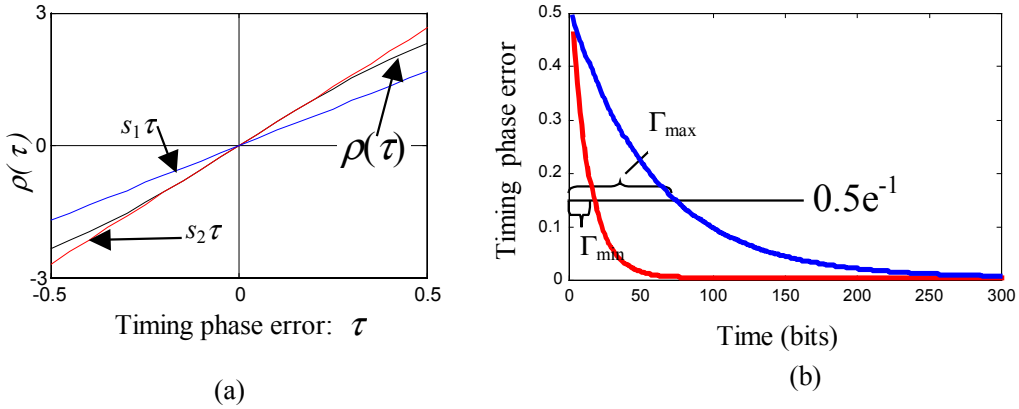


Fig. 2-25: Illustration of (a) a timing function and (b) its corresponding phase convergence with maximum and minimum time constants.

The characterization of phase convergence using minimum and maximum time constants is sufficient to describe the timing acquisition for first-order timing-recovery loops. However, for timing acquisition in the presence of a frequency error, timing recovery needs a second-order PLL [3, Chap.11]. The operation of a second-order PLL can be described as (see Fig. 2-3(b))

$$\tau_{k+1} = \tau_k - \alpha\chi_k - \delta_k(\tau_k), \quad \delta_k(\tau_k) = \delta_{k-1}(\tau_k) + \beta\chi_{k-1} \tag{2.53}$$

where α and β are step-size parameters, and δ_k is the amount of frequency compensation. The discrete-time PLL may be related to its continuous-time counterpart by replacing the sample-delay operator z by the approximation $z \approx 1 + j2\pi fT$, for small $|2\pi fT|$. For a continuous-time second-order PLL, the natural frequency ω_n and the damping factor ς are two important parameters in the study of convergence. The corresponding parameters ω_n^d and ς^d for the discrete-time second-order PLL can be related to the step size parameters α and β according to [3, Chap. 11]

$$\omega_n^d T = \sqrt{\beta}\sqrt{K_d K_o}, \quad \varsigma^d = \frac{\alpha}{2\sqrt{\beta}}\sqrt{K_d K_o} \tag{2.54}$$

where K_d and K_o are the gain factors of the TED and VCO, respectively, of the PLL.

For timing acquisition using a second-order PLL, the acquisition speed can be described using its responses to the unit phase step and the unit phase ramp (frequency step). By way of illustration, we show these responses for a continuous-time second-order PLL in Fig. 2-26(a) and (b), respectively. The damping factor ς is used as a parameter and the timing phase error decays with increase of the relative time t/T. Observe that large values of ς yield a slower response to frequency steps but a faster response to phase steps. In practice, values of ς significantly smaller than 0.707 are not often encountered. For a discrete-time second-order PLL, the damping factor ς^d is typically chosen as 0.707 and the natural frequency ω_n^d is chosen for $\omega_n^d T < 0.1$, which covers most cases of practical interest. The parameters α and

β of the loop filter need to be properly chosen, taking into account the TED gain K_d in order for the loop to have the prescribed damping factor ς^d and natural frequency ω_n^d.

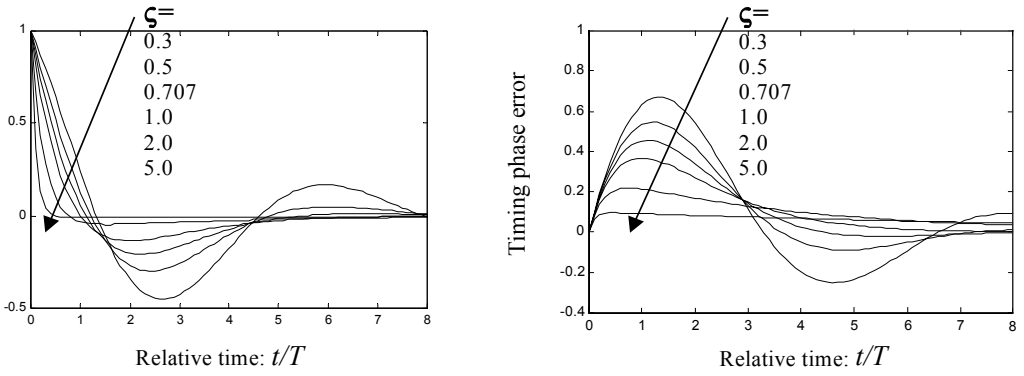


Fig. 2-26: Second-order continuous-time PLL transient responses with (a) timing phase error due to a unit phase step and (b) timing phase error due to a unit frequency step. The damping factor ς is used as a parameter.

2.5 Summary

In this chapter, we have presented a detailed review on timing recovery. This review relates to timing recovery structures, requirements, and performance measures of timing recovery. We have also discussed the generic timing error detector algorithms and the main issues that arise during timing acquisition. Numerical analyses and simulation results are presented for supporting our discussions. The review and the related discussions presented here constitute the basics for the study and development of timing recovery techniques for digital recording systems in the following chapters of this thesis.

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CHAPTER 3

TIMING SENSITIVITY ANALYSIS FOR MAGNETIC RECORDING

At high densities and/or data rates, the data recovery performance of a read channel depends strongly on the accuracy of the timing phase delivered by the timing recovery loop. The timing sensitivity of recording channels indicates how fast the data detection performance deteriorates when the timing phase deviates from its ideal value. In this chapter, we develop analytical approaches for investigating the effect of timing error on the performance of MDFE (multi-level decision feedback equalization) and PR4-VD (partial-response class-IV with Viterbi detection) detectors in magnetic recording systems.

The chapter is organized as follows. A brief survey of the published work on timing sensitivity is given in Section 3.1, followed by a summary of the contributions of this chapter. Section 3.2 presents the magnetic recording system model incorporating MDFE and PR4-VD detectors. The detection performance of MDFE in the presence of timing phase errors and random phase jitter is investigated in Section 3.3. The detection performance of PR4-VD in the presence of timing phase errors is investigated in Section 3.4. The chapter is concluded in Section 3.5.

3.1 Introduction

Equalizer, data-detector and timing recovery circuits are among the most important blocks that constitute the read-channel of a magnetic recording system. The equalization and detection blocks usually receive considerable attention from researchers. However, with the steady increase in data rates and recording densities, timing recovery has become crucial for reliable data recovery. Therefore, it is necessary to evaluate the sensitivity of a detector to timing errors, since timing sensitivity has significant influence on the required timing margins for reliable acquisition and tracking [1, Chap. 9].

The problem of timing sensitivity was studied by Tufts and Berger [2], Gonsalves and Tufts [3], Eriksson and Van den Elzen [4], and Yeo and Farhang-Boroujeny [5] in communication systems, and by Bergmans [6], Bergmans and Janssen [7] in recording systems, among other researchers. In these papers, a variety of methods was proposed for designing transmitter-receiver filters and equalizers that are robust to timing jitter. Bergmans [9] reported a theoretical study on the impact of static timing phase errors on various equalization and

detection schemes based on an equivalent discrete-time recording system with timing errors. Investigations on the timing sensitivity of partial response systems were reported by Osawa *et al*. [10], and Grami and Pasupathy [11]. Further, an analysis of timing sensitivity for decision feedback and partial response (PR) equalizers with low-pass and matched-filter front-end filters was reported by Roy and Raghavan [12]. Moon [13] examined the impact of a timing phase error on finite-length equalizer performance in partial response and decision feedback equalization (DFE) schemes. The effect of a static timing phase error on the performance of Viterbi detector (VD) in PR systems was studied in [14], assuming white noise at the detector input.

In this chapter, we propose a novel analytical approach for evaluating the timing sensitivity of decision feedback and Viterbi based partial response detection schemes. For a given channel and equalizer, this approach computes the probability density function (PDF) of the residual ISI that arises due to misequalization and timing error. This PDF is in turn used to compute the error event rate to quantify the detection performance in the presence of a timing error. This approach provides a fast and simple method to evaluate the timing sensitivity in the presence of misequalization. Unlike existing approaches, it can cover the performance consequences of both static phase error and random timing jitter. We consider multi-level DFE (MDFE) and class-IV partial response with Viterbi detection (PR4-VD) schemes for our study. MDFE, and its advanced versions, are excellent detectors for (1,7)-coded recording channels, in particular at high densities [15], [16]. From the family of partial response schemes, we choose the partial response 1-D^2 (D denotes one bit delay operator) for our study since it is one of the most widely studied responses [17]. Nevertheless, our approach can be extended to more advanced detectors from the DFE and PR families.

3.2 Channel Model with MDFE and PR4-VD Detectors

Fig. 3-1 shows the magnetic recording system model incorporating MDFE and PR4-VD detectors.

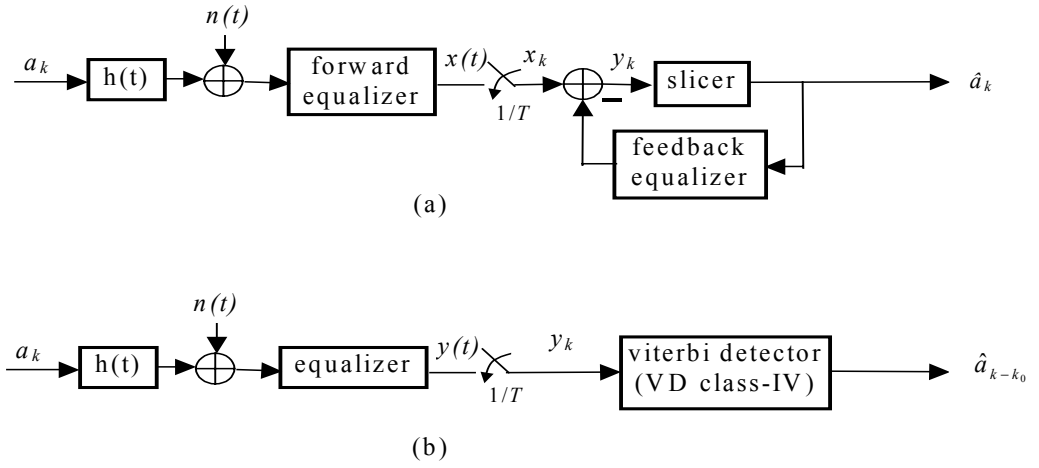

Fig. 3-1: Magnetic recording system model incorporating (a) MDFE and (b) PR4-VD detector.

The input data $\{a_k\}$, with $a_k \in \{-1,1\}$ being in the NRZ format, is a sequence of 2/3(1,7) coded bits for MDFE and 16/17 (0,6/6) coded bits for PR4-VD. The recording channel is

characterized by a bit response $h(t)$ and additive white Gaussian noise (AWGN) $n(t)$ of two-sided power spectral density $N_0/2$. Media noise, which is important at high densities [18] [19], is not included in the channel model. The equalizer output, designated $x(t)$ for the MDFE case and $y(t)$ for the PR4-VD case, is sampled at rate $1/T$, where T is the channel bit duration, resulting in $x_k = x((k+\tau)T)$ and $y_k = y((k+\tau)T)$ for MDFE and PR4-VD, respectively. Here, τ is the timing phase error (normalized in units T) at the sampler.

In the simulations, the continuous-time channel response *h(t)* is replaced by a fractionally-spaced discrete-time filter with impulse response h_m given by $h_m = h(t)|_{t=mT/L}$ where L is a positive integer representing an oversampling factor. We use L=4. Consequently, the equalizer is replaced by an FIR filter with a T/L-spaced impulse response, denoted by w_m. Similarly, the noise *n(t)* is replaced by discrete-time white Gaussian noise n_m whose variance σ_n^2 is determined by the SNR defined as[1]

$$SNR\,[\mathrm{dB}] = 10\log_{10}\left(\frac{V_{op}^2}{\sigma_n^2}\frac{L}{R}\right) \tag{3.1}$$

where V_{op} is the base-to-peak amplitude of the isolated transition response (see eq. (1.6)) and the factor $\frac{L}{R}$ represents the bandwidth expansion resulting from the modulation encoding rate R and the oversampling factor L in the recording channel. Note that $\sigma_n^2 R/L$ is the variance of the noise in the user bandwidth R/T. Finally, an interpolator will be used at the equalizer output to generate $x_k = x((k+\tau)T)$ and $y_k = y((k+\tau)T)$ for MDFE and PR4-VD, respectively, for a normalized timing phase error τ. The design of the equalizer is done as described in [20]. The decision delay of the Viterbi detector (VD) is denoted k_o.

We denote by q_k the T-spaced discrete-time equalized bit response, from the recording channel input to the sampler output. The equalizers in MDFE are designed to result in a target response of the form $q_{-1}D^{-1} + q_0 + q_1 D$, with $q_0 > q_{-1} = q_1 > 0$, at the slicer input [20]. Thus, because of the d=1 code constraint, the ideal slicer input (noiseless, τ=0) has four levels[2], $\pm q_0$ and $\pm(q_{-1} + q_0 + q_1)$, and the decision at the k^{th} instant is $\hat{a}_k$. This is illustrated in Fig. 3-2(a), which shows the equalized bit response q_k for τ=0 and the slicer input for different timing phase errors. For the partial response system with PR target 1-D^2, Fig. 3-2(b) shows the equalized bit response q_k for τ=0 and the equalizer output for different timing phase errors.

The figures on the right hand side of Fig. 3-2 show the inputs of the slicer and VD as functions of timing phase error τ at the sampler. They resemble standard eye-patterns. Fig. 3-2

[1] We may remark that the SNR defined in (3.1) does not take into account the recording density and code rate. This definition helps to normalize the noise power spectral density with respect to the reference signal amplitude V_{op} for a given user data rate. Starting from these normalized signal and noise levels, the effects of coding and density are accounted for in the way that bit response h_m and the noise variance σ_n^2 are defined. Thus, the SNR defined in (3.1) can be used as a common reference to compare the performances with different codes and/or densities.

[2] Note that due to the d=1 code constraint, the triplet { a_k, a_{k-1}, a_{k-2} } can assume only 6 out of the 8 possibilities, viz. ±{+1, +1, +1}, ±{+1, +1, -1}, ±{-1, +1, +1}. The patterns ±{-1, +1, -1} are not allowed.

clearly shows four decision levels for MDFE and three levels for PR4-VD when τ=0. The smearing of decision levels at the ideal phase τ=0 is due to the residual ISI resulting from misequalization. As the magnitude of timing phase error is increased from 0 to 0.5, the residual ISI increases due to mismatch between the sampled equalized bit response and the ideal target response. Therefore, the noise margins between the decision levels decrease sharply as τ increases, and they vanish for τ=±0.5. Further, the effect of erroneous decision feedback in MDFE around τ=±0.5 can also be clearly seen. In the timing sensitivity studies reported here, the equalizers and the gain are not optimized for each timing phase error; instead they are kept fixed at the optimum values corresponding to τ=0.

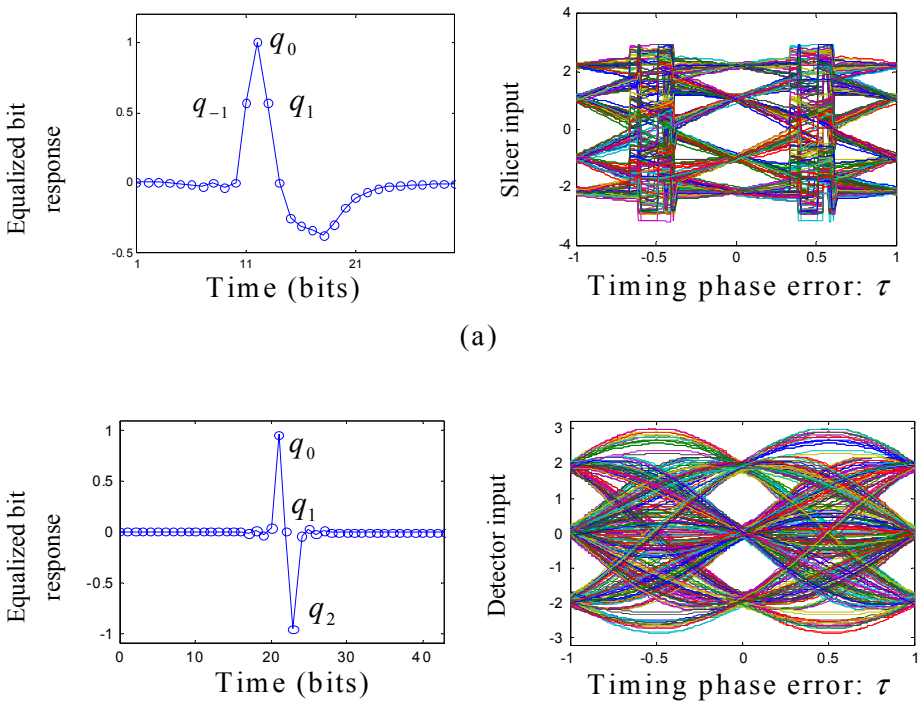

Fig. 3-2: Equalized bit response q_k and the noiseless detector inputs y_k for different timing phase errors τ for (a) MDFE and (b) PR4-VD detectors at user density 2.5.

3.3 Timing Sensitivity of MDFE Detector

In this section, we develop an analytical approach to investigate the timing sensitivity of the MDFE detector. This is done in two parts. First, we address the case of a static timing phase error. Second, we address the case of random phase jitter by combining the result for a timing phase error with the distribution of the jitter. We use error event rate (EER) as the performance measure for studying the timing sensitivity. We use EER rather than bit error rate (BER) since numerical evaluation of EER is easier compared to BER. In MDFE, the EER is the probability of making a decision error when there are no erroneous decisions in the feedback register. Our approach given below is aimed at deriving an expression for EER with the timing phase error τ as a variable.

3.3.1 Error event rate of MDFE with static timing phase error

Since MDFE is a zero-threshold detector and the outer levels $\pm(q_{-1}+q_0+q_1)$ are relatively large, its performance is mainly determined by the value of inner level $\pm q_0$. This is true even with non-zero timing phase errors, because the slicer inputs at the outer levels vary very slowly with τ for moderate excursions of τ (see Fig. 3-2(a)). Thus, the performance mainly depends on the effective noise acting on the inner levels. Therefore, in our analysis, we only consider the noise and residual ISI seen by the inner levels.

Let the feedback register be free from erroneous decisions. Then, with timing phase error τ, the slicer input can be written as (see Fig. 3-1(a))

$$y_k(\tau) = d_k(\tau) + \xi_k(\tau) \tag{3.2}$$

where $d_k(\tau)$ is either the inner level $q_0(\tau)a_k$ or the outer level $\left(q_{-1}(\tau)+q_0(\tau)+q_1(\tau)\right)a_k$, and $\xi_k(\tau) = z_k(\tau) + v_k$ is the sum of residual ISI and noise. Here, $z_k(\tau)$ is the residual ISI due to timing phase error and misequalization, and v_k is the Gaussian channel noise. The variables $q_{-1}(\tau)$, $q_0(\tau)$ and $q_1(\tau)$ represent the values of the main samples q_{-1}, q_0 and q_1 with timing phase error τ. Assuming that decision errors occur only at the inner levels, the probability of detection error (i.e., EER) for a given timing phase error can be given by

$$\Pr_{\mathrm{MDFE}}(err\,|\tau) = \Pr_{in} \cdot \Pr\left(\xi_k(\tau) > q_0(\tau)\right) \tag{3.3}$$

where 'Pr' denotes probability and $\Pr_{in} \simeq 0.608$ is the probability of occurrence of the inner level, which is given by the sum of the probabilities of the patterns $\pm$\{-1, +1, +1\} and $\pm$\{+1, +1, -1\} [22]. To compute the probability $\Pr\left(\xi_k(\tau) > q_0(\tau)\right)$, we need to obtain the PDF of the random variable $\xi_k(\tau)$. Note that $\xi_k(\tau)$ is not Gaussian because of the residual ISI $z_k(\tau)$. Since the noise component v_k is a zero-mean Gaussian random variable, its PDF can be written as

$$p_v(v) = \left(\sqrt{2\pi}\sigma_v\right)^{-1} \exp\left(-v^2 \big/ \left(2\sigma_v^2\right)\right), \quad -\infty < v < \infty \tag{3.4}$$

where σ_v^2 is the variance of noise v_k. Let $p_z(z|\tau)$ be the PDF of the residual ISI component $z_k(\tau)$. Since the data a_k is independent of the noise v_k, the PDF of $\xi_k(\tau)$ can be obtained as

$$p_\xi(\xi\,|\,\tau) = \int_{-\infty}^{\infty} p_z(z\,|\,\tau)\, p_v(\xi - z)\, dz. \tag{3.5}$$

Substituting (3.5) and (3.4) in (3.3), we get

$$\begin{aligned} \Pr_{\mathrm{MDFE}}(err\,|\,\tau) &= \frac{\Pr_{in}}{\sqrt{2\pi}\sigma_v} \int_{q_0(\tau)}^{\infty} \int_{-\infty}^{\infty} p_z(z\,|\,\tau) \exp\left(-\frac{(v-z)^2}{2\sigma_v^2}\right) dz\, dv \\ &= \Pr_{in} \cdot \int_{-\infty}^{\infty} p_z(z\,|\,\tau)\, Q\left(\frac{q_0(\tau) - z}{\sigma_v}\right) dz \end{aligned} \tag{3.6}$$

where $Q(u) = \left(\sqrt{2\pi}\right)^{-1} \int_u^{\infty} \exp\left(-x^2/2\right) dx$. It remains to determine the PDF, $p_z(z|\tau)$, of inner-level residual ISI $z_k(\tau)$.

3.3.2 Distribution of inner-level ISI

In the absence of channel noise (i.e., $v_k=0$), using (3.2), we can write

$$z_k(\tau) = y_k(\tau) - q_0(\tau)a_k \,. \tag{3.7}$$

This ISI can be modeled as the output of a filter with impulse response $c_i(\tau)$ and input a_k. The coefficients $c_i(\tau)$ can be obtained from the equalized bit response coefficients $q_i(\tau)$ and the feedback equalizer taps b_i according to

$$c_i(\tau) = \begin{cases} q_i(\tau), & -M \le i < -1, \;\; N_b + 1 < i \le N \\ q_{-1}(\tau) - q_1(\tau) + b_1, & i = -1 \\ 0, & i = 0, 1 \\ q_i(\tau) - b_i, & 2 \le i \le N_b + 1 \end{cases} \tag{3.8}$$

where integers $M>0$ and $N>0$ define the span of the equalized bit response $q_i(\tau)$, and N_b+1 is the number of feedback equalizer taps. The tap values b_i, $i = 1, 2, \cdots, N_b+1$, at T-spacing, are given by

$$b_1 = q_1 - q_{-1} = 0$$
$$b_i = q_i \quad \text{for} \quad i = 2, \cdots, N_b + 1.$$

Using (3.8), we can express inner-level ISI as

$$z_k(\tau) = \sum_{i=-M}^{N} c_i(\tau) a_{k-i} = \sum_{i=-M}^{N} f_{k,i}(\tau) \tag{3.9}$$

where $f_{k,i}(\tau) = c_i(\tau)a_{k-i}$. We need the joint PDF of the random variables $\{f_{k,i}(\tau)\}$ to compute the PDF of $z_k(\tau)$. Since these are correlated random variables because of the correlation in the (1,7) coded bits $\{a_k\}$, it requires considerable mathematical and computational effort to obtain the exact PDF of $z_k(\tau)$. Hence, we make the simplifying assumption that the random variables $\{a_k\}$ are independent. We will later confirm the adequacy of this assumption. Thus, we get from (3.9)

$$p_z(x \mid \tau) = p_{f_{-M}}(x \mid \tau) \otimes p_{f_{-M+1}}(x \mid \tau) \otimes \cdots \otimes p_{f_N}(x \mid \tau), \quad -\infty < x < \infty. \tag{3.10}$$

Here, $p_z(x \mid \tau)$ and $p_{f_i}(x \mid \tau)$ are the PDFs of $z_k(\tau)$ and $f_{k,i}(\tau)$, respectively, and '$\otimes$' denotes convolution. Since a_k takes on only two values +1 or –1 with probability 0.5, and $c_i(\tau)$ is deterministic, we obtain the PDF of $f_{k,i}(\tau)$ for a given τ as

$$p_{f_i}(x \mid \tau) = \begin{cases} 0.5 & \text{if} \quad x \in \{+c_i(\tau), -c_i(\tau)\} \\ 0 & \text{otherwise.} \end{cases} \tag{3.11}$$

Taking the Fourier transform on the both sides of (3.10), we get

$$P_z(w \mid \tau) = \prod_{i=-M}^{N} P_{f_i}(w \mid \tau) \tag{3.12}$$

where $P_z(w \mid \tau)$ and $P_{f_i}(w \mid \tau)$ denote the Fourier-transforms of $p_z(x \mid \tau)$ and $p_{f_i}(x \mid \tau)$, respectively. It follows from (3.11) that $P_{f_i}(w \mid \tau) = \cos(wc_i(\tau))$, $-\infty < w < \infty$. Substituting this in (3.12), we get

$$P_z(w\,|\,\tau) = \prod_{i=-M}^{N} \cos(wc_i(\tau)), \quad -\infty < w < \infty. \tag{3.13}$$

Taking the inverse Fourier transform on the both sides of (3.13) and noting that $P_z(w|\tau)$ is real and even-symmetric, we obtain

$$p_z(x\,|\,\tau) = \frac{1}{\pi}\int_0^{\infty} \prod_{i=-M}^{N} \cos(w\,c_i(\tau))\cos(wx)dw, \quad -\infty<x<\infty. \tag{3.14}$$

Fig. 3-3 shows the PDF of inner-level ISI, computed using (3.14), for various values of τ.

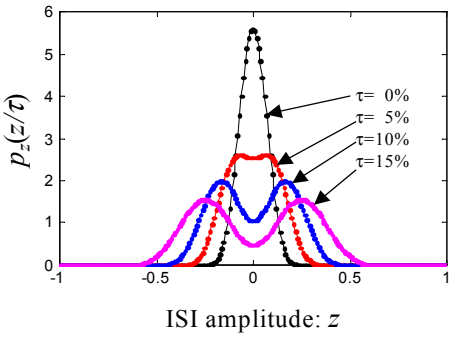

Fig. 3-3: PDF of inner level residual ISI in the presence of timing phase errors (obtained by computation using (3.14)).

We observe that as τ increases, the peak value of the distribution falls off rapidly and the peak splits into two symmetric peaks about zero. For small τ, the residual ISI is dominated by misequalization, which is normally very small in amplitude. This explains the large amplitude single peak observed for small τ. As τ increases, the residual ISI becomes dominated by timing phase error. Furthermore, the term $c_{-1}(\tau)=q_{-1}(\tau)-q_1(\tau)$ becomes more significant for large τ and hence the distribution peaks at $\pm(q_{-1}(\tau)-q_1(\tau))$. Note that $q_{-1}(\tau)-q_1(\tau)=0$ for $\tau=0$. This explains the fall in peak value as well as the observed peak splitting.

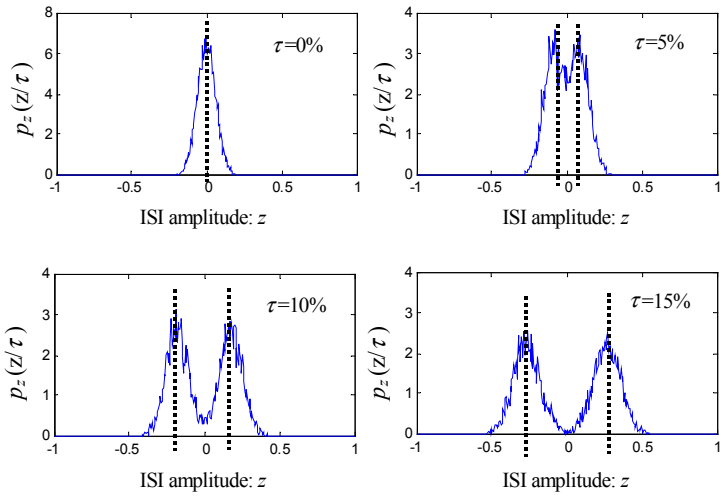

Fig. 3-4: PDF of inner-level residual ISI in the presence of timing phase errors (obtained by simulation).

We made Monte Carlo simulations to verify the above analytical observations. Fig. 3-4 shows the PDF of inner-level ISI for different τ, obtained by simulations. Observe that the simulations do match the analytical results in Fig. 3-3 in terms of shape, peak amplitude, and peak splitting of the distributions.

3.3.3 Evaluation of MDFE detection performance

In this section, we evaluate the error event rate (EER) of MDFE in the presence of timing phase error and random phase jitter, by making use of the ISI distribution developed above. The EER in the presence of a timing phase error can be evaluated by substituting the PDF of inner level ISI given by (3.14) for the one in (3.6) and evaluating the integral. Doing this for the Lorentzian channel with user density 2.5, we get the performance curves shown in Fig. 3-5. The EER estimated using direct bit-by-bit simulations is also shown in the figure. Observe that the analytically obtained values match well with those from simulations, especially for not too large timing phase error. Note that the SNR loss due to a 5% timing phase error is about 0.4~0.5 dB at 1e-5 EER. Studies conducted for negative timing phase errors revealed that the SNR loss is less compared to positive phase errors (e.g. 0.1 dB less for $\tau = -5\%$ compared to that for +5%). This is due to the asymmetry of the equalized bit response in MDFE, as was also observed in [9].

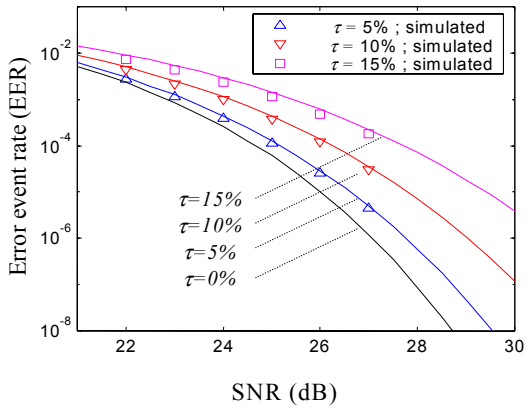

Fig. 3-5: Error event rate of MDFE in the presence of timing phase error τ (solid curves: EER obtained by calculation using (3.6)).

We can easily extend the above approach to evaluate the impact of steady state timing loop phase jitter on detection performance. Let the PDF of steady state phase jitter be $p_\tau(\tau)$. Then, the resulting EER can be obtained as

$$EER = \int_{-\infty}^{\infty} \Pr_{\text{MDFE}}(err \mid \tau)\, p_\tau(\tau)\, d\tau \tag{3.15}$$

where $\Pr_{\text{MDFE}}(err \mid \tau)$ is obtained from (3.6). Assuming Gaussian distributed phase jitter in the tracking loop, the EER calculated using (3.15) and that obtained by bit-by-bit simulations are shown in Fig. 3-6. Observe that there is a close agreement between the results obtained from the computations and simulations. Further, these curves show that RMS phase jitter of 3%, 5% and 8% results in SNR loss of about 0.1 dB, 0.4 dB and 1.2 dB, respectively, at EER 1e-5, compared to the ideal timing.

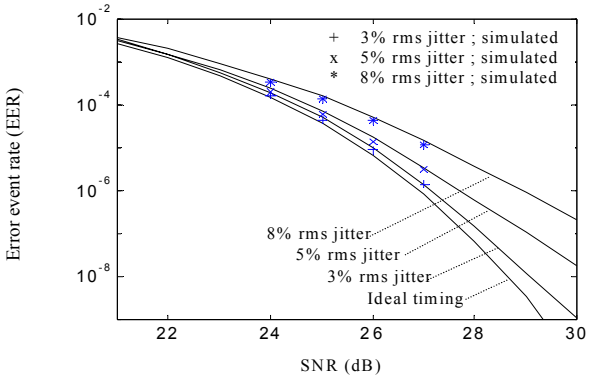

Fig. 3-6: Error event rate of MDFE in the presence of random phase jitter (solid curves: EER obtained by calculation using (3.15)).

The close agreement between the computed and simulated EER values in Fig. 3-5 and Fig. 3-6 justifies our simplifying assumption on the independence of data bits. For the sake of the completeness, we give in Appendix 3.A the analysis of the ISI distribution by taking the dependence of (1,7) data into account.

3.4 Timing Sensitivity of PR4-VD

The EER of PR4-VD is the probability that the Viterbi detector (VD) chooses an incorrect sequence of bits $\hat{\boldsymbol{a}} = \{\hat{a}_k\}$ instead of the correct sequence $\boldsymbol{a} = \{a_k\}$. For this to happen, the path metric associated with the sequence of bits $\boldsymbol{a}$ in the trellis for the given partial response target should be greater that that with $\hat{\boldsymbol{a}}$ [21, Chap. 9]. Thus, with timing phase error τ, the EER can be given by

$$\Pr_{\mathrm{PR}}\left(err\,|\tau\right) = \sum_{\boldsymbol{a},\hat{\boldsymbol{a}}} \Pr(\boldsymbol{a}) \Pr(\hat{\boldsymbol{a}}\,|\boldsymbol{a},\tau) \tag{3.16}$$

where

$$\Pr(\hat{\boldsymbol{a}}\,|\boldsymbol{a},\tau) = \Pr\left(m(\boldsymbol{a}\,|\tau) > m(\hat{\boldsymbol{a}}\,|\tau)\right). \tag{3.17}$$

Here, $m(\boldsymbol{a}|\,\tau)$ denotes the path metric for the path $\boldsymbol{a}$ and $\Pr(\boldsymbol{a})$ denotes the probability of the data sequence $\boldsymbol{a}$.

Let g_k be the ideal coefficients of the partial response target. For example, $[g_0,\ g_1,\ g_2] = [1,\ 0,\ -1]$ and $g_k = 0$ for $k < 0$ and $k > 2$ for PR4-VD. Following the notation from the preceding section, let $q_k(\tau)$ denote the T-spaced equalized channel bit response with timing phase error τ. Then, the path metric $m(\hat{\boldsymbol{a}}\,|\tau)$ is given by [1, Chap. 3]

$$m(\hat{\boldsymbol{a}}\,|\,\tau) = \sum_k \left[(a \otimes q(\tau))_k + v_k - (\hat{a} \otimes g)_k\right]^2. \tag{3.18}$$

With $c_i(\tau)=q_i(\tau)-g_i$, the residual ISI $z_k(\tau)$ at the detector input with τ is given by (3.9). Substituting for $q_i(\tau)$ in (3.18), we get

$$m(\hat{\boldsymbol{a}} \mid \tau) = \sum_k [2(e \otimes g)_k + z_k(\tau) + v_k]^2 \tag{3.19}$$

where $e_k \triangleq (a_k - \hat{a}_k)/2$ is the error sequence between the two paths $\boldsymbol{a}$ and $\hat{\boldsymbol{a}}$. Substituting (3.19) in (3.17), we get

$$\Pr(\hat{\boldsymbol{a}} \big| \boldsymbol{a}, \tau) = \Pr\left[\sum_k \big(v_k + z_k(\tau)\big)(e \otimes g)_k < -\sum_k (e \otimes g)_k^2 \right]. \tag{3.20}$$

At reasonable SNRs, the EER can be approximated by considering the pairs $(\boldsymbol{a}, \hat{\boldsymbol{a}})$ which result in maximum $\Pr(\hat{\boldsymbol{a}} \big| \boldsymbol{a}, \tau)$ given in (3.20). In other words, we use the dominant error events for computing error event rate. In the case of the partial response 1-D^2, the single-bit error event is the dominant event at the density 2.5. Hence, we get $(e \otimes g)_k = g_k$. Using this, (3.20) becomes

$$\Pr(\hat{\boldsymbol{a}} \mid \boldsymbol{a}, \tau) \simeq \Pr[\tilde{v}_k + \tilde{z}_k(\tau) < -2] \tag{3.21}$$

where $\tilde{v}_k = v_k - v_{k-2}$ and $\tilde{z}_k(\tau) = z_k(\tau) - z_{k-2}(\tau)$. Clearly, $\tilde{v}_k$ is Gaussian with zero mean and variance $\sigma_{\tilde{v}}^2 = 2\sigma_v^2 - 2r_2^v$ where $r_2^v = E[v_i v_{i-2}]$.

To obtain the PDF of the ISI part $\tilde{z}_k(\tau)$, we proceed as follows. Using b_k=a_k-a_{k-2}, we can write $\tilde{z}_k(\tau) = \sum_i \tilde{f}_{k,i}(\tau)$ where $\tilde{f}_{k,i}(\tau) = c_i(\tau) b_{k-i}$. Hence, the PDF of $\tilde{f}_{k,i}(\tau)$ is given by

$$p_{\tilde{f}_i}(x) = \begin{cases} 0.25, & x \in \{+2c_i(\tau), -2c_i(\tau)\} \\ 0.5 & x = 0 \\ 0 & \text{otherwise.} \end{cases} \tag{3.22}$$

As we did before, we make the simplifying assumption that b_k's are independent[3]. Then, following similar steps as in (3.12) to (3.14), we get the PDF of the residual ISI $\tilde{z}_k(\tau)$ as

$$p_{\tilde{z}}(x \big| \tau) = \frac{1}{\pi} \int_0^\infty \left[\prod_i \cos^2(w c_i(\tau)) \cos(wx) dw \right], \quad -\infty < x < \infty. \tag{3.23}$$

This follows from the fact that the Fourier transform of the PDF of $\tilde{f}_{k,i}(\tau)$ is $\cos^2(c_i w)$. Fig. 3-7 shows the PDF of residual ISI $\tilde{z}_k(\tau)$ computed using (3.23) as well as bit-by-bit simulations. Observe that the analytical results agree closely to those from simulations.

[3] Because $b_k = a_k - a_{k-2}$, the $\{b_k\}$ constitute a correlated sequence even if $\{a_k\}$ is a sequence of independent data bits. However, for the sake of simplicity, we assume that b_k's are independent. We also note that (3.22) is based on the assumption that the pair of data bits $\{a_k, a_{k-2}\}$ assumes {-1, -1}, {-1,+1}, {+1, -1} or {+1, +1} with equal probability 0.25.

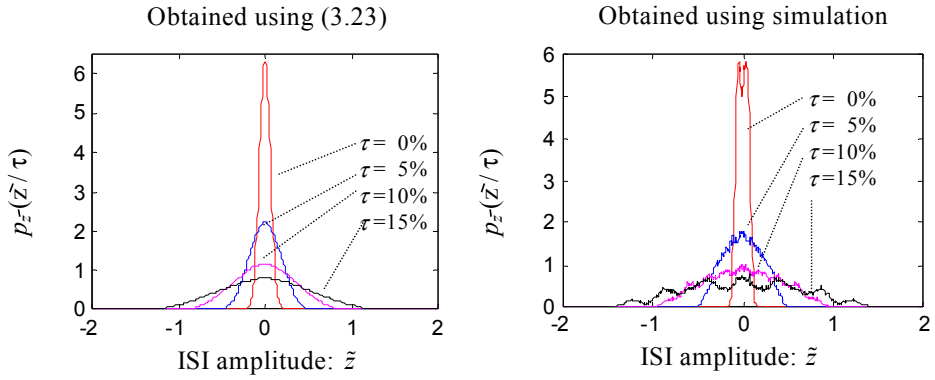

Fig. 3-7: PDF of residual ISI $\tilde{z}_k(\tau)$ obtained using analytical and simulation approaches.

Since $\tilde{v}_k$ and $\tilde{z}_k(\tau)$ are independent random variables, the PDF of $\tilde{v}_k + \tilde{z}_k(\tau)$ can be obtained by convolving their individual PDFs. For the *1-D*^{2} recording system, the values of $\Pr(\hat{\boldsymbol{a}}|\boldsymbol{a},\tau)$ given by (3.20) are identical for error events of the form $\{e_k\} = \pm\{+1\}$, $\pm\{+1,0,+1\}$, $\pm\{+1,0,+1,0,+1\}$, …. Hence, following similar steps as for the derivation of (3.6), the EER for the PR4-VD with τ can be approximated using the dominant error events (from (3.16), (3.17), (3.21) and (3.23)) as

$$\Pr_{\mathrm{PR}}(err|\tau) \simeq 2\int_{-\infty}^{\infty} p_{\tilde{z}}(x|\tau) Q\left(\frac{2+x}{\sigma_{\tilde{v}}}\right) dx. \tag{3.24}$$

The scale factor 2 on the right side of (3.24) is the sum of the probabilities of the data patterns that support the single-bit error events [17].

Fig. 3-8 shows the EER computed using (3.24) as well as bit-by-bit simulations in the presence of a timing phase error. Observe that the theoretical and simulation results match well. Further, timing phase errors of 5% and 10% cause about 0.9 dB and 3.0 dB loss in SNR, respectively, at 1e-5 EER.

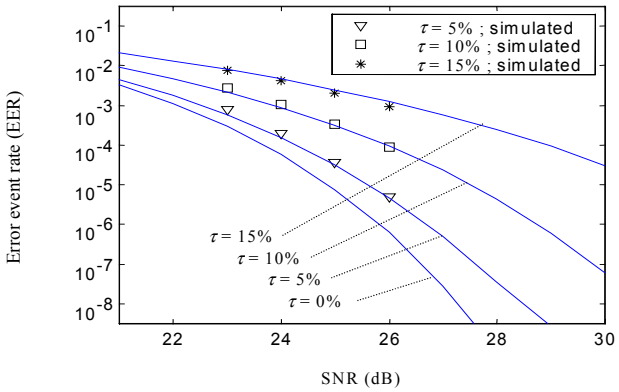

Fig. 3-8: Error event rate of PR4-VD in the presence of timing phase error (solid curves: obtained using calculation based on Eq. (3.23)).

Comparing Figs. 3-8 and 3-5, we see that the timing sensitivity of PR4-VD is higher than that of MDFE at the density considered here. Separate studies based on bit error rate performance rather than error event rate (not shown here) also led to the same conclusion as above. However, if we specify the timing phase error in terms of user bit interval rather than channel bit interval (i.e., multiply the timing phase errors considered here by 2/3 for MDFE and 16/17 for PR4-VD), then the timing sensitivities of MDFE and PR4-VD would be comparable. The performance of PR4-VD for random jitter can also be evaluated in the same way as for the MDFE detector in the preceding section. We skip this work here for brevity.

3.5 Conclusions

In this chapter, using the error event rate as a performance measure, we investigated the timing sensitivity of MDFE and PR4-VD detectors. We developed analytical methods for estimating the probability density function of the residual ISI in the presence of misequalization and timing phase error. Using this, the error event rates of the detectors were evaluated numerically. These numerical results have been shown to match well with those obtained from bit-by-bit simulations. The principle of this approach can be easily extended to evaluate the timing sensitivity of advanced versions of MDFE and PR4-VD detectors.

Appendix 3.A : PDF of ISI with Correlated Data

The analysis of the ISI PDF given in Section 3.3.2 assumed that the data bits $\{a_k\}$ are independent. Clearly, this assumption is not true for (1,7) coded sequences. In this section, we present a more accurate analysis by removing this independence assumption.

According to (3.9), we can write the MDFE inner-level ISI as

$$z_k(\tau) = \sum_{i=-M}^{N} c_i(\tau) a_{k-i} = \mathbf{c}^{\mathrm{T}}(\tau)\mathbf{a}_k \tag{3.25}$$

where $\mathbf{c}(\tau) \triangleq [c_{-M}(\tau) \ \cdots \ c_N(\tau)]^{\mathrm{T}}$ and $\mathbf{a}_k \triangleq [a_{k+M} \ \cdots \ a_{k-N}]^{\mathrm{T}}$. To obtain the PDF of $z_k(\tau)$, the probability of the (1,7) data vector $\mathbf{a}_k$ needs to be computed. In (3.25), for a given τ, $\mathbf{c}(\tau)$ is deterministic and $\mathbf{a}_k$ is a stochastic (1,7) data vector at the time instant k. As a result, $z_k(\tau)$ is a discrete random variable with the probability equal to that of $\mathbf{a}_k$. Therefore, calculation of the distribution of ISI boils down to computing the probability of all possible vectors $\mathbf{a}_k$ in the (1,7) data sequence. To do this, we resort to the method proposed by Howell [22] to compute the probabilities of RLL 2/3 (1,7) data patterns. Then, the ISI distribution is given by

$$P_z(z \mid \tau) = \Pr(z_k(\tau) = z \mid \tau) = \sum_{i \in S_z} \Pr(\mathbf{a}_i) \tag{3.26}$$

where the set S_z is such that $\mathbf{c}^{\mathrm{T}}(\tau)\mathbf{a}_i = z$ for all $i \in S_z$. One of the main advantages of this approach is that we can compute the probabilities of $z_k(\tau)$ for any timing phase error τ by using one-time calculated probabilities of data vectors $\mathbf{a}_k$.

Fig. 3-9 shows the PDF of ISI obtained using (3.26) for various values of τ. The length of data vectors $\mathbf{a}_k$ used in this computation is 20 bits. The computation results shown in Fig. 3-9 match well with the simulation results shown in Fig. 3-4.

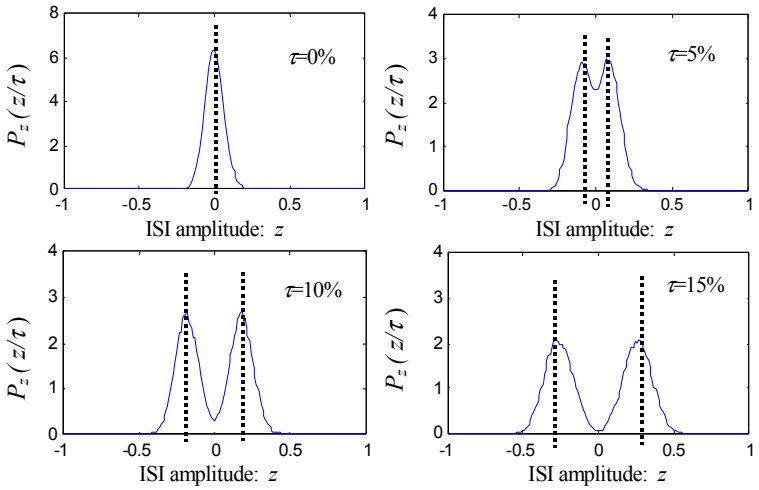

Fig. 3-9: PDF of inner-level ISI in the presence of timing phase errors (obtained using calculation based on (3.26)).

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CHAPTER 4

ANALYSIS OF TIMING ERROR DETECTORS

The timing error detector (TED) is considered to be the most important part of the timing recovery system. The ability of the timing recovery loop to track the timing base of the input signal depends on how much timing information the TED can extract from the noise-corrupted input signal. The effectiveness of the TED can be characterized by the TED efficiency which is a measure of the amount of extracted timing information. In this chapter, we present analyses for examining the efficiencies of TEDs used in partial response (PR) and decision feedback equalized magnetic recording systems. For the read channel with decision feedback equalization (DFE), we analyze the noise performance at the TED output and provide an improved TED for jitter minimization. We also study optimality issues for timing acquisition.

The chapter is organized as follows. A brief introduction to TED efficiency and a survey of published work are given in Section 4.1, followed by a summary of the contributions of this chapter. In Section 4.2, we examine the TED efficiency for PR systems using a given TED and different PR targets. The TED efficiency for DFE read channels is examined in Section 4.3 using the multilevel DFE (MDFE) as an example. In Section 4.4, we propose a marginal detection-based TED for reducing the phase jitter under low signal-to-noise ratio (SNR) channel conditions, and analyze its output noise variance and the resulting timing jitter performance. Section 4.5 deals with issues related to the optimality of MDFE timing acquisition. The chapter is concluded in Section 4.6.

4.1 Introduction

When designing a timing recovery loop, we need to consider a fundamental trade-off between tracking ability and noise rejection. Good suppression of noise requires the loop bandwidth to be as small as possible, whereas a wider bandwidth is required for a better tracking ability. This trade-off can be quantified using the measure 'efficiency'. The efficiency of a TED is a measure of the amount of timing information that the TED is able to extract from the incoming signal per unit of time and SNR [15]. In Section 2.2.3 of Chapter 2, we have given more details on the efficiency of timing error detectors. To recall, the TED efficiency is defined as

$$\gamma = \frac{1}{SNR_m} \frac{K_d^2}{S_u(1)} \tag{4.1}$$

where SNR_m is the SNR in the matched-filter bound sense, K_d is the slope of the timing function at the origin (also called the TED gain), and $S_u(1)$ is the power spectral density $S_u(e^{j2\pi\Omega})$ of the noise u_k at the TED output (see Fig. 2.2) at DC ($\Omega = 0$) (Ω being a normalized frequency variable in units 1/*T*). Thus, whereas the efficiency is independent of the loop filter and voltage-controlled oscillator, it is dependent on the power spectral densities of the data and noise as well as the transfer function of the channel. This will become clearer in the sections below.

Among the various types of TED (see Section 2.1), the zero-forcing (ZF) TEDs are commonly used in practice because of their cost effectiveness and implementation simplicity and relatively good performance. Bergmans and Lam [1] proposed, with analysis, a class of data aided ZF based timing recovery techniques. In fact, the classical paper of Mueller and Müller [2] reported the first ZF based baud-rate timing recovery scheme. In [15], Bergmans proposed the concept of TED efficiency and presented analyses for evaluating the efficiencies of maximum-likelihood (ML) and various baud-rate timing recovery schemes as a function of the data and channel parameters. The TED algorithms given in [3] and [4] are typical examples of ZF based timing recovery techniques used in PR systems. References [7] and [8] give typical examples of timing recovery techniques used in DFE systems. The techniques in [7] and [8] were not developed from a ZF point of view. In fact, the TED in [7] is of the minimum mean-square error (MMSE) type. Further, the analysis of these algorithms has not been reported, except by means of simulation results.

In this chapter, we analyze the TED algorithms used in PR and DFE read channels. We derive the TED efficiencies of PR systems for different PR target polynomials and input data coding schemes. We also derive the TED efficiency for the MDFE. In addition, we show that the PR and MDFE TEDs can be reworked into a form that resembles an error-based ZF TED [14]. We propose and analyze an improved TED for the MDFE detector that can reduce jitter variance at low SNRs. Further, using the TED efficiency as a measure, we show that the MDFE TED is near optimal during timing acquisition. We also examine the optimality of the different preamble patterns for different recording densities and coding schemes.

4.2 TED Analysis for PR Recording Systems

The classical paper of Mueller and Müller [2] suggested that the TED output for baud-rate timing recovery in digital synchronous receivers could be of the form $\chi_k = y_{k-1}\hat{a}_k - y_k\hat{a}_{k-1}$, where y_k and $\hat{a}_k$ are the equalizer output and the corresponding bit decision, respectively. This concept was reapplied for timing recovery in PR magnetic recording systems [3] [4]. As described in [3], the TED output for PR systems is given by

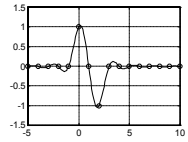
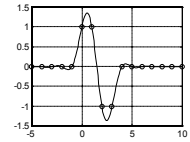
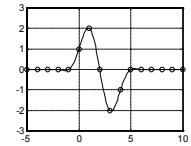
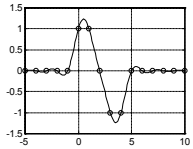
$$\chi_k = y_{k-1}x_k - y_k x_{k-1} \tag{4.2}$$

where y_k is the actual equalizer output which depends on a timing phase error, and x_k is the desired value of y_k (See Fig. 3-1(b) in Chapter 3). In this section, we evaluate the efficiency of this TED algorithm for PR magnetic recording systems with selected PR targets and input coding schemes.

4.2.1 The TED analysis

We define the vector of PR target coefficients as $\mathbf{p}=[p_0 \quad p_1 \quad \cdots \quad p_{N-1}]^T$ where N is the number of target coefficients. Typical examples of PR targets used in magnetic recording are listed in Table 4-1, where 'D' denotes one symbol delay [5] [6]. Here, $\mathbf{p}=[1\ 0\ -1]^T$ for PR-IV, $\mathbf{p}=[1\ 1\ -1\ -1]^T$ for EPR-IV, $\mathbf{p}=[1\ 2\ 0\ -2\ -1]^T$ for E^{2}PR-IV, and $\mathbf{p}=[1\ 1\ 0\ -1\ -1]^T$ for a modified E^{2}PR-IV.

Table 4-1: PR TARGETS FOR MAGNETIC RECORDING SYSTEMS.

PR scheme	*p(t)*	Target
PR-IV		$P(D) = 1\text{-}D^2$
EPR-IV		$P(D) = 1+D\text{-}D^2\text{-}D^3$
E^{2}PR-IV		$P(D) = 1+2D\text{-}2D^3\text{-}D^4$
M-E^{2}PR-IV		$P(D) = 1+D\text{-}D^3\text{-}D^4$

For the analysis in this section for deriving the efficiency of the TED according to (4.2) for PR systems, we will use Fig. 3-1(b) (see Chapter 3) which shows the magnetic recording system model incorporating PR equalizer and detector. Let the continuous-time signal at the equalizer output be given by

$$y(t) = \sum_i a_i q(t - iT) + v(t) \tag{4.3}$$

where a_i is the input data at the rate *1/T,* $q(t)$ is the bit response of the equalized PR channel, and $v(t)$ is the noise at the equalizer output. For the sake of convenience, we assume in this section that the equalized channel response $q(t)$ is equal to the ideal PR target response $p(t)$ given in Table 4-1. Further, the autocorrelation function of noise $v(t)$ is defined by the impulse response of the equalizer, since the noise $n(t)$ at the equalizer input is assumed to be white. The equalizer output $y(t)$ is sampled at the sampling instants $t_k = (k+\tau)T$ where τ denotes the timing phase error normalized in units T, i.e., the ideal sampling instants correspond to $t_k = kT$. The resulting sampled output $y_k = y(t_k)$ of the equalizer is given by

$$\begin{aligned} y_k &= \sum_i a_i p((k+\tau)T - iT) + v((k+\tau)T) \\ &= \sum_i a_i p_{k-i}^{\tau} + v_k \end{aligned} \tag{4.4}$$

where $p_k^{\tau} = p((k+\tau)T)$ and $v_k = v((k+\tau)T)$. Denote the desired value of y_k by x_k, which is the noise-free value of y_k at the ideal sampling instants $t_k = kT$, i.e. $x_k = \sum_{i=0}^{N-1} p_i a_{k-i}$ where $p_i = p_i^0$. Then, we can obtain the timing function, which is the expected value of χ_k, as

$$\rho_{\mathrm{PR}}(\tau) = E[\chi_k] = E[y_{k-1}x_k - y_k x_{k-1}].$$

For uncorrelated data a_k, one can readily obtain

$$\rho_{\mathrm{PR}}(\tau) = \mathbf{p}^{\mathrm{T}}(\mathbf{p}_{-1}^{\tau} - \mathbf{p}_1^{\tau}) \tag{4.5}$$

where $\mathbf{p}_i^{\tau} = [p_i^{\tau} \quad p_{i+1}^{\tau} \quad \cdots \quad p_{i+N-1}^{\tau}]^{\mathrm{T}}$. Then, the TED gain K_d can be computed as

$$K_d = \left.\frac{d\rho_{\mathrm{PR}}(\tau)}{d\tau}\right|_{\tau=0} = \mathbf{p}^{\mathrm{T}}(\dot{\mathbf{p}}_{-1} - \dot{\mathbf{p}}_1) \tag{4.6}$$

where $\dot{\mathbf{p}}_{\mathbf{i}} = [p_i' \quad p_{i+1}' \quad \cdots \quad p_{i+N-1}']^{\mathrm{T}}$ and $p_i' = T\left.\frac{dp(t)}{dt}\right|_{t=iT}$.

The TED output χ_k consists of contributions from the data a_k and the noise v_k. To distinguish them, we calculate the variance of χ_k as $\mathrm{V}(\tau) = E[\chi_k^2] - (E[\chi_k])^2$. This results in

$$\mathrm{V}(\tau) = \mathbf{p}^{\mathrm{T}}[(\mathbf{P}_{\mathrm{I}}^{\tau} + \mathbf{P}_{\mathrm{II}}^{\tau} - 2\mathbf{P}_{\mathrm{III}}^{\tau}) - (\mathbf{p}_{-1}^{\tau} - \mathbf{p}_1^{\tau})\cdot(\mathbf{p}_{-1}^{\tau} - \mathbf{p}_1^{\tau})^{\mathrm{T}}]\mathbf{p} + \delta_v \tag{4.7}$$

where $\delta_v = 2[r_v(0)\sum_{i=0}^{N-1}(p_i)^2 - r_v(1)\sum_{i=1}^{N-1} p_i p_{i-1}]$ with $r_v(l) = E[v_k v_{k+l}]$ being the autocorrelation function of v_k for lag l. The matrices $\mathbf{P}_{\mathrm{I}}^{\tau}$, $\mathbf{P}_{\mathrm{II}}^{\tau}$ and $\mathbf{P}_{\mathrm{III}}^{\tau}$ are given by

$$\mathbf{P}_{\mathrm{I}}^{\tau} = \begin{bmatrix} p(1,1) & p(1,2) & \cdots & p(1,N) \\ p(2,1) & p(2,2) & \cdots & p(2,N) \\ \vdots & \vdots & \cdots & \vdots \\ p(N,1) & p(N,2) & \cdots & p(N,N) \end{bmatrix},$$

$$\mathbf{P}_{\mathrm{II}}^{\tau} = \begin{bmatrix} p(-1,-1) & p(-1,0) & \cdots & p(-1,N-2) \\ p(0,-1) & p(0,0) & \cdots & p(0,N-2) \\ \vdots & \vdots & \cdots & \vdots \\ p(N-2,-1) & p(N-2,0) & \cdots & p(N-2,N-2) \end{bmatrix},$$

and

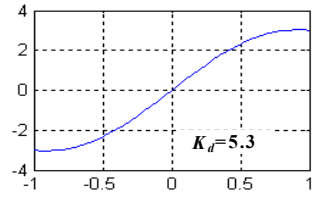
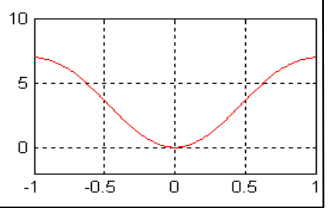
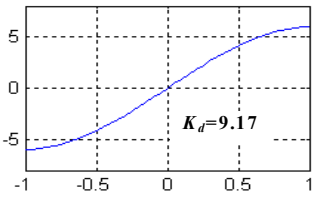
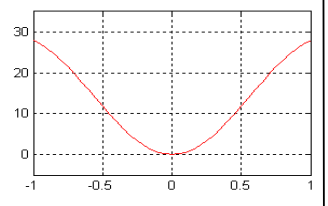
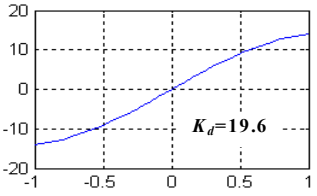
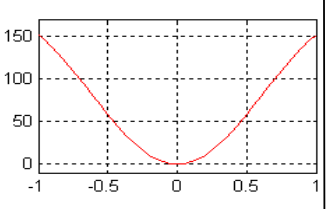
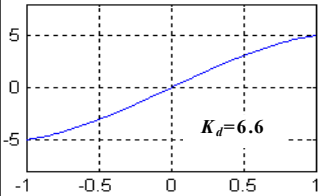
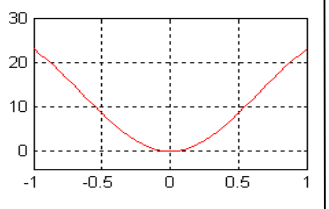
$$\mathbf{P}_{\mathrm{III}}^{\tau} = \begin{bmatrix} \tilde{p}(1,0) & \tilde{p}(1,1) & \cdots & \tilde{p}(1,N-1) \\ \tilde{p}(2,0) & \tilde{p}(2,1) & \cdots & \tilde{p}(2,N-1) \\ \vdots & \vdots & \cdots & \vdots \\ \tilde{p}(N,0) & \tilde{p}(N,1) & \cdots & \tilde{p}(N,N-1) \end{bmatrix},$$

where $p(i,j) = \begin{cases} 2p_i^{\tau}p_j^{\tau}, & i \neq j \\ \sum_i (p_i^{\tau})^2, & i = j \end{cases}$ and $\tilde{p}(i,j) = \begin{cases} p_i^{\tau}p_{j-1}^{\tau} + p_{i-1}^{\tau}p_j^{\tau}, & i \neq j \\ \sum_i p_{i-1}^{\tau}p_i^{\tau}, & i = j. \end{cases}$

Clearly, the expression (4.7) for $V(\tau)$ shows the contributions from the data and noise to the total TED output variance. The first term on the right side of (4.7) pertains to data-dependent phase jitter, and vanishes at the ideal phase with $\tau = 0$ if there is no misequalization. If misequalization exists at $\tau = 0$ then a static timing phase error could accrue as can be seen from (4.5). The second term, δ_v, is due to noise and hence characterizes noise induced phase jitter.

Using (4.5) and (4.7), we compute the mean and the variance of χ_k for noiseless PR channels and illustrate the results in Table 4-2.

Table 4-2: MEAN AND VARIANCE OF THE TED OUTPUT FOR PR MAGNETIC RECORDING SYSTEMS.

PR scheme	**Timing function (K_d is the TED gain)** x-axis: Timing phase error (units T) y-axis: Mean of the TED output	**Variance of TED output** x-axis: Timing phase error (units T) y-axis: Variance of the TED output
PR-IV: $P(D)=1-D^2$		
EPR-IV: $P(D)=1+D-D^2-D^3$		
E^{2}PR-IV: $P(D)=1+2D-2D^3-D^4$		
M-E^{2}PR-IV: $P(D)=1+D-D^3-D^4$		

In the computation of χ_k, we assume that the desired reference sequence x_k is without errors. In practice, this sequence can be produced in various ways depending on the data and

the channel characteristics. For instance, x_k takes on values {+2, 0, -2} for PR-IV and can be constructed by using a simple 2-level threshold-detector[1] [3]. But, x_k takes on several values for higher order PR channels (e.g., $x_k \in$ {-4, -2, 0, 2, 4} for EPR-IV). Hence, extending the threshold method for constructing x_k for such systems may not be effective since the detector would require several threshold levels and the noise margin for correct detection has a decreasing trend. In these situations, x_k can be produced using the bit decisions $\hat{a}_k$ according to $x_k = \sum_{i=0}^{N-1} p_i \hat{a}_{k-i}$. In the following TED efficiency analysis, we assume that decisions $\hat{a}_k$ are correct.

In the above analysis, we assume that the input data a_k is uncorrelated. For correlated data a_k with autocorrelation function $r_a(l) \triangleq E[a_k a_{k+l}]$, the timing function based on (4.2) can be shown to be

$$\rho_{\mathrm{PR}}(\tau) = \sum_i \sum_j p_i^{\tau} p_j (r_a(j-i-1) - r_a(j-i+1)) \tag{4.8}$$

from which one can readily calculate the TED gain K_d as

$$K_d = \sum_i \sum_j p_i' p_j (r_a(j-i-1) - r_a(j-i+1)) \cdot \tag{4.9}$$

Further, the noise component of the TED output can be obtained as

$$u_k = v_{k-1} \sum_{i=0}^{N-1} p_i a_{k-i} - v_k \sum_{i=0}^{N-1} p_i a_{k-1-i} \cdot \tag{4.10}$$

Then, it is not difficult to compute the noise autocorrelation function as

$$\begin{aligned} r_u(l) &= E[u_k u_{k+l}] \\ &= 2r_v(l) \sum_m r_p(m) r_a(m+l) - r_v(l+1) \sum_m r_p(m) r_a(m+l-1) - r_v(l-1) \sum_m r_p(m) r_a(m+l+1) \end{aligned} \tag{4.11}$$

where $r_p(m) = \sum_{i=0}^{N-1-m} p_i p_{i+m}$. Using this, we can calculate the DC portion of the power spectral density of noise u_k at the TED output as

$$S_u(1) = \sum_{l=-\infty}^{\infty} r_u(l) \,. \tag{4.12}$$

Substituting (4.9) and (4.12) in (4.1), we get the efficiency of the TED of (4.2) as

$$\gamma_{\mathrm{PR}} = \frac{1}{SNR_m} \frac{[\sum_i \sum_j p_i' p_j (r_a(j-i-1) - r_a(j-i+1))]^2}{\sum_{l=-\infty}^{\infty} r_u(l)} \tag{4.13}$$

where

$$SNR_m = \frac{\int_{-\infty}^{\infty} h^2(t) dt}{N_o / 2} \tag{4.14}$$

[1] The preamble pattern used during timing acquisition in PR-IV channels is the $4T$ pattern $\{\cdots + + - - + + - - \cdots\}$. With this, x_k takes on only two values {-2, +2} and can be obtained using a simple slicer (with zero-threshold) at the equalizer output.

with $h(t)$ and $N_o/2$ denoting the unequalized channel bit response and noise power spectral density at the channel output, respectively.

To calculate the numerical values of the TED efficiency according to (4.13), we consider the Lorentzian model of the magnetic recording channel (see eq. (2.15), Chapter 2) with PR targets PR-IV, EPR-IV and E^{2}PR-IV. Note that the absolute SNR should not matter because efficiency is independent of SNR. The results for various user densities (see eq. (2.14), Chapter 2) are given in Fig. 4-1 and Fig. 4-2 for the coding schemes of the rate 16/17 (0,6/6) code and the rate 2/3 (1,7) code, respectively.

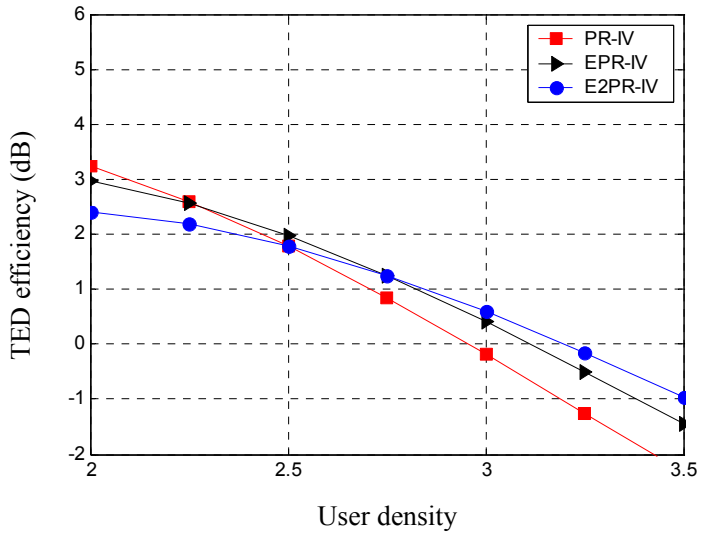


Fig. 4-1: TED efficiency for Lorentzian recording channel and rate 16/17 (0,6/6) code.

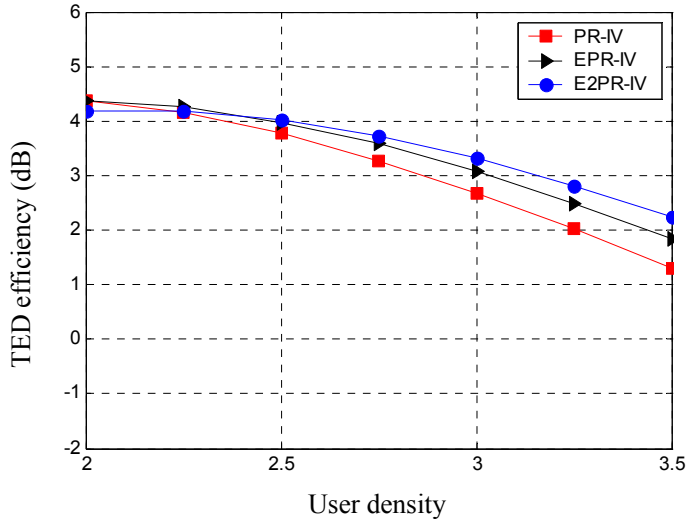


Fig. 4-2: TED efficiency for Lorentzian recording channel and rate 2/3 (1,7) code.

Observe that the TED efficiency decreases as the user density increases because the recording channel bandwidth decreases as user density increases. At high densities, the E^{2}PR-IV and EPR-IV targets afford better TED efficiency than PR-IV. This is because at high densities the higher order PR schemes can better match the recording channel characteristics,

thereby extracting timing information more effectively with minimum noise enhancement or coloration. Also observe that the use of the 2/3 (1,7) code results in better TED efficiency compared to the 16/17 (0, 6/6) code. This is because the power spectrum of the 2/3 (1,7) code has its power concentrated in the low frequency region whereas that of the 16/17 (0,6/6) code is spread almost uniformly over the entire frequency range (see Fig. 2-11, Chapter 2). Therefore, the 2/3 (1,7) code is better matched to the recording channel characteristics compared to the 16/17 (0,6/6) code. Combining this with the insight we got from the expression for the efficiency of the ML TED (see eq. (2.19), Chapter 2), we see why the efficiency for the 2/3 (1,7) code is better than for the 16/17 (0,6/6) code, especially at high densities.

4.2.2 Error based ZF TED for PR systems

The analysis we presented above is for the TED according to (4.2), which uses the equalizer output y_k. We now show that this TED scheme can be realized alternatively in the form of a symbol-rate ZF TED, which uses the error $e_k = y_k - x_k$ at the equalizer output rather than y_k. This results in an error based ZF TED for PR systems. One of the advantages of using error based ZF TED is the simplicity of implementing the TED. Since both the equalizer output y_k and its reference x_k have large magnitude ranges, calculation of the TED output according to (4.2) yields an even larger range, which is not convenient for TED implementation. The use of e_k in the TED can greatly reduce the TED output range. Furthermore, by taking the sign of e_k we can even avoid the multiplier (a high-speed multiplier) for calculating the TED output. These advantages make the error based ZF TED attractive in practice.

Note that the TED output according to (4.2) has two components, namely $y_{k-1}x_k$ and $y_k x_{k-1}$. Because the timing loop effectively averages the TED output, the relative delay between $y_{k-1}x_k$ and $y_k x_{k-1}$ is immaterial to the TED performance. Therefore, advancing the first component by one symbol interval, we can obtain an equivalent TED output

$$\chi_k = y_k(x_{k+1} - x_{k-1}) \ . \tag{4.15}$$

We rework this output into an equivalent error-based output by noting that $e_k = y_k - x_k$. Correspondingly,

$$\chi_k = e_k(x_{k+1} - x_{k-1}) + (x_{k+1}x_k - x_k x_{k-1}) \ . \tag{4.16}$$

Since the timing function is the expected value of χ_k and the quantity $E[x_{k+1}x_k - x_k x_{k-1}]$ is zero irrespective of the input data, we can omit the corresponding component from (4.16). Thus, we get an equivalent TED output

$$\chi_k = e_k(x_{k+1} - x_{k-1}) \ . \tag{4.17}$$

The TED according to (4.17) is in the form of a standard error-based ZF TED. Analysis shows that the timing function $\rho_{\mathrm{PR}}(\tau)$ and the TED gain K_d derived for (4.2) in the preceding analysis are also valid for (4.17). Further, analysis of the TED efficiency for (4.17) yields the same result as given in (4.2). This means that the error based ZF TED does not degrade the timing recovery performance in PR systems.

4.3 TED Analysis for DFE Recording Systems

4.3.1 The TED analysis

The TED algorithm analyzed in the previous section for PR systems can in principle be used for any type of recording system including DFE. One such application is the simplified TED suggested by Abbott and Cioffi [7] for an adaptive DFE magnetic recording system. For a particular DFE read channel, however, depending on the specific features of the signals in the forward path and at the input of the detector, the TED algorithm can be derived in various forms for implementation simplicity. Kenney and Wood [8] reported a TED algorithm for MDFE timing recovery, which makes use of the inner-level slicer input samples to form a transition-based TED. The output of this TED is given by

$$\chi_k = (y_k + y_{k-1})(\hat{a}_k - \hat{a}_{k-1}) \tag{4.18}$$

where y_k is the sample value of the slicer input at the time instant k and $\hat{a}_k$ is the corresponding decision (see Fig. 3-1(a), Chapter 3). This TED can be well understood with the help of Fig. 4-3, which shows the samples of the waveform at the slicer input in the presence of a timing phase error τ (τ being normalized in units T). At the ideal phase (i.e. $\tau = 0$), the positive and negative inner-level samples have equal magnitudes but opposite signs. This results in zero at the TED output. For a positive (resp. negative) τ, the sample magnitudes at the positive and negative transitions do not match each other thereby producing a positive (resp. negative) TED output and subsequently yielding an estimate of timing phase error.

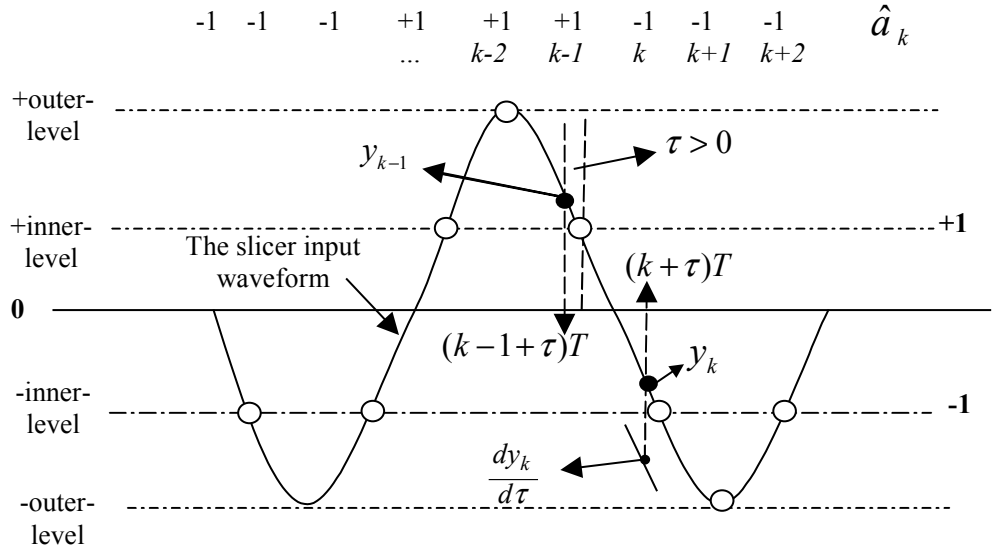


Fig. 4-3: Illustration of the existing transition-based MDFE TED algorithm.

Referring to Fig. 3-1(a), we can write the slicer input in the presence of a timing phase error τ as

$$\begin{aligned} y_k &= \sum_i a_i q((k+\tau)T - iT) + v(t_k) - \sum_{i=2}^{N_b+1} a_{k-i} q(iT) \\ &= \sum_i a_i q_{k-i}^{\tau} + v_k - \sum_{i=2}^{N_b+1} q_i a_{k-i} \\ &= \sum_{i=-N_1}^{N_2} q_i^{\tau} a_{k-i} + v_k - \sum_{i=2}^{N_b+1} q_i a_{k-i} \end{aligned} \tag{4.19}$$

where $t_k = (k+\tau)T$, $v_k = v(t_k)$, $q_k^{\tau} = q((k+\tau)T)$ and $q_k = q_k^0 = q(kT)$. Here, we denote by $v(t)$ the noise at the forward equalizer output, and $q(t)$ the equalized channel bit response from the channel input to the forward equalizer output with its duration given by $N_1 + N_2 + 1$ bits. We assume the past decisions to be correct and the number of taps in the feedback equalizer to be N_b with tap values q_i, $i = 2, 3, \cdots, N_b + 1$.

It is not difficult to analyze the transition-based TED of (4.18). Using (4.19) and (4.18), the timing function can be obtained as

$$\rho(\tau) = E[\chi_k] = \sum_{i=-N_1}^{N_2} q_i^{\tau}(r_a(i+1) - r_a(i-1)) + \sum_{i=2}^{N_b+1} q_i(r_a(i-1) - r_a(i+1)) \tag{4.20}$$

where $r_a(l) = E[a_k a_{k+l}]$. The TED gain K_d can be computed as

$$K_d = \sum_{i=-N_1}^{N_2} q_i'(r_a(i+1) - r_a(i-1)) \tag{4.21}$$

where $q_i' = \left.\frac{dq_i^{\tau}}{d\tau}\right|_{\tau=0}$. The noise component at the TED output is given by

$$u_k = (v_k + v_{k-1})(a_k - a_{k-1}). \tag{4.22}$$

The autocorrelation function of the TED output noise is given by

$$\begin{aligned} r_u(l) &= E[u_k u_{k+l}] \\ &= (2r_v(l) + r_v(l-1) + r_v(l+1))(2r_a(l) - r_a(l-1) - r_a(l+1)) \end{aligned} \tag{4.23}$$

where $r_v(l) = E[v_i v_{i+l}]$. Then, the PSD of the noise component at DC is given by

$$S_u(1) = \sum_{l=-\infty}^{\infty} r_u(l) \quad . \tag{4.24}$$

Substituting (4.24) and (4.21) in (4.1), we obtain the TED efficiency of the transition-based MDFE TED scheme of (4.18) as

$$\gamma_{\text{MDFE}} = \frac{1}{SNR_m} \frac{[\sum_{i=-L_1}^{L_2} q_i'(r_a(i+1) - r_a(i-1))]^2}{\sum_{l=-\infty}^{\infty} r_u(l)} \tag{4.25}$$

where SNR_m is defined as in (4.14). We compute the TED efficiency for the MDFE incorporating the rate 2/3 (1,7) code at various user densities and 27 dB SNR, and plot the result in Fig. 4-4. The result reveals that the TED efficiency varies inversely with the user density. This is because the channel bandwidth, and thereby the timing information at the input of the TED, decreases with increase in user density.

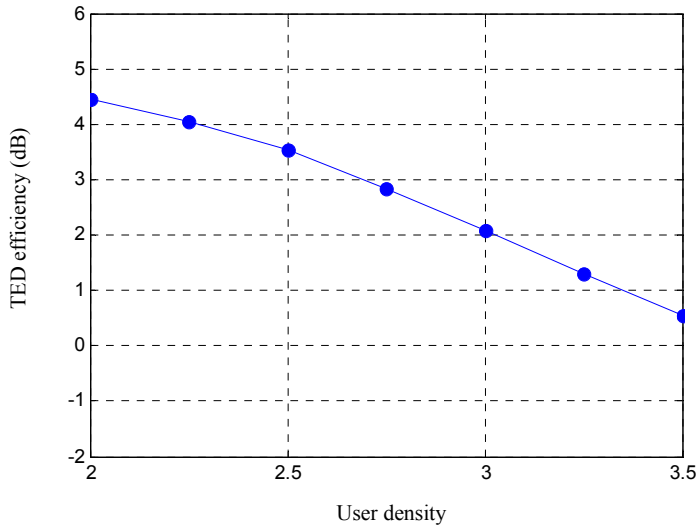


Fig. 4-4: TED efficiency for the MDFE transition-based TED.

4.3.2 Error based ZF TED for MDFE

As we did for PR systems in Section 4.2.1, we now derive an error-based ZF TED scheme for the MDFE [9] for easy implementation. The error signal at the inner level is given by $e_k = y_k - \hat{a}_k$, which represents the difference between the actual slicer input y_k and its desired value $\hat{a}_k$. Then, $y_k = e_k + \hat{a}_k$. As a result, (4.18) becomes

$$\chi_k = e_k(\hat{a}_k - \hat{a}_{k-1}) + e_{k-1}(\hat{a}_k - \hat{a}_{k-1}). \tag{4.26}$$

Clearly, the TED output is non-zero only when there are transitions in the data, i.e., $\hat{a}_k \neq \hat{a}_{k-1}$. Since the MDFE detector uses a (1,7) code, the transition condition $\hat{a}_k \neq \hat{a}_{k-1}$ implies that $\hat{a}_{k+1} \neq \hat{a}_{k-1}$ and $\hat{a}_k \neq \hat{a}_{k-2}$. Using this, we rework (4.26) into

$$\chi_k = e_k(\hat{a}_{k+1} - \hat{a}_{k-1}) + e_{k-1}(\hat{a}_k - \hat{a}_{k-2}) \ . \tag{4.27}$$

The two terms on the right side of (4.27) are delayed versions of each other whenever $\hat{a}_k \neq \hat{a}_{k-1}$. Since the loop averages the TED output, both terms essentially convey the same information, and we might drop one of them. Thus, we could simplify the TED according to

$$\chi_k = \begin{cases} e_k(\hat{a}_{k+1} - \hat{a}_{k-1}) & \text{if } \hat{a}_k \neq \hat{a}_{k-1}, \\ 0 & \text{if } \hat{a}_k = \hat{a}_{k-1}. \end{cases} \tag{4.28}$$

The condition $\hat{a}_k \neq \hat{a}_{k-1}$ implies that $\hat{a}_{k+1} \neq \hat{a}_{k-1}$, whence χ_k will be nonzero. Conversely, if $\hat{a}_k = \hat{a}_{k-1}$, then $\hat{a}_{k+1}$ does not necessarily equal $\hat{a}_{k-1}$. In this event, if $\hat{a}_{k+1} \neq \hat{a}_{k-1}$, then the cross-product $e_k(\hat{a}_{k+1} - \hat{a}_{k-1})$ could convey significant timing information, while (4.28) would nevertheless stipulate the TED output to be zero. To also take this timing information into account, we remove the conditioning from (4.28) to obtain the new TED output

$$\chi_k = e_k(\hat{a}_{k+1} - \hat{a}_{k-1}) = \begin{cases} 2e_k\hat{a}_{k+1} & \text{if } \hat{a}_{k+1} \neq \hat{a}_{k-1}, \\ 0 & \text{otherwise}. \end{cases} \tag{4.29}$$

This expression coincides with that of the error-based Zero-Forcing TED in [14]. Compared to the MDFE TED according to (4.18), the new TED according to (4.29) takes more timing information into account, and can be verified to have a higher efficiency.

4.4 Marginal Detection-Based TED

In Section 4.3, we analyzed the efficiency of the error-based ZF TED for the MDFE detector. In this section, we develop a method for this TED that can reduce the variance of phase jitter resulting from low-SNR conditions, and analyze the resulting performance.

For the ZF TED according to (4.29), the noise component u_k at the TED output is $u_k = v_k(\hat{a}_{k+1} - \hat{a}_{k-1})$. Its variance is

$$\sigma_u^2 = 2(r_a(0) - r_a(2)) \cdot \sigma_v^2 . \tag{4.30}$$

For the 2/3 (1,7) code, the correlations $r_a(0)$ and $r_a(2)$ are given by (estimated using data-averaging) $r_a(0) = 1.0$ and $r_a(2) = -0.2167$. Thus, we get

$$\sigma_u^2 \simeq 2.43\sigma_v^2 . \tag{4.31}$$

The above equation shows that the variance of the noise component of the TED output is proportional to the variance of noise v_k at the TED input. Therefore, reducing the variance of v_k leads to a decrease in the TED output noise variance. However, v_k is superimposed upon a useful signal component, and it is sometimes difficult to distinguish v_k and signal in practice, especially at poor SNRs. For the MDFE detector that uses a zero-threshold slicer, it is possible to use an augmented TED, named marginal detection-based TED, for minimizing the variance of the TED output noise. This TED distinguishes big noise components at the TED input and subsequently removes their effect on the timing loop.

The proposed marginal detection-based TED has output

$$\chi_k = \begin{cases} (y_k - \hat{a}_k)(\hat{a}_{k+1} - \hat{a}_{k-1}) & \text{if } |y_k| > M, \\ 0 & \text{if } |y_k| \le M \end{cases} \tag{4.32}$$

where the slicer input y_k is given in (4.19) and $0 < M < 1$ is a marginal threshold for detecting large noise components. Since $\hat{a}_k = \pm 1$, the condition $|y_k| \le M$ is equivalent to

$$1 - M \le |v_k| \le 1 + M . \tag{4.33}$$

This means that whenever the TED input noise v_k meets the conditions $1 - M \le v_k \le 1 + M$ for $\hat{a}_k = -1$ and $-1 - M \le v_k \le -1 + M$ for $\hat{a}_k = 1$, the TED output χ_k becomes zero. Both conditions indicate that y_k is around zero and thus unreliable for bit detection. Making χ_k zero can suppress large noise disturbances under these conditions.

4.4.1 Performance analysis

Now, we analyze the TED output noise variance in the TED according to (4.32). Assume that the total noise v_k at the slicer input has a Gaussian distribution with a probability density function (PDF) $\mathrm{P}(v) = (1/\sqrt{2\pi\sigma_v^2}) \exp\left(-\frac{v^2}{2\sigma_v^2}\right)$ where σ_v^2 is the variance of v_k. Denote by $\tilde{v}_k$

the noise that induces disturbances at the TED output. Clearly, $\tilde{v}_k$ is the noise portion in v_k that does not meet conditions $1-M \le v_k \le 1+M$ and $-1-M \le v_k \le -1+M$. Thus, the variance of $\tilde{v}_k$ can be obtained as

$$\sigma_{\tilde{v}}^2 = \int_{\substack{-\infty \\ v \notin \mathrm{V}}}^{\infty} v^2 \mathrm{P}(v) dv \tag{4.34}$$

where $\mathrm{V} = \{1-M \le v_k \le 1+M \text{ or } -1-M \le v_k \le -1+M\}$. To calculate $\sigma_{\tilde{v}}^2$, we define

$$S \triangleq \int_{\substack{-\infty \\ v \in \mathrm{V}}}^{\infty} \mathrm{P}(v) dv = 1 - 2\left[Q\left(\frac{1-M}{\sigma_v} \right) - Q\left(\frac{1+M}{\sigma_v} \right) \right] \tag{4.35}$$

where $Q(x) = \frac{1}{\sqrt{2\pi}} \int_x^{\infty} e^{-u^2/2} du$, and

$$\begin{aligned} S_V &\triangleq \int_{\substack{-\infty \\ v \in \mathrm{V}}}^{\infty} v^2 \mathrm{P}(v) dv \\ &= 2\sigma_v \left[\frac{1-M}{\sqrt{2\pi}} \exp\left(-\frac{(1-M)^2}{2\sigma_v^2} \right) - \frac{1+M}{\sqrt{2\pi}} \exp\left(-\frac{(1+M)^2}{2\sigma_v^2} \right) + \sigma_v Q\left(\frac{1-M}{\sigma_v^2} \right) - \sigma_v Q\left(\frac{1+M}{\sigma_v^2} \right) \right]. \end{aligned} \tag{4.36}$$

Then, the variance $\sigma_{\tilde{v}}^2$ of $\tilde{v}_k$ can be obtained as

$$\sigma_{\tilde{v}}^2 = (\sigma_v^2 - S_V)/S. \tag{4.37}$$

As a result, the proposed TED of (4.32) has a noise component at the output given by $u_k = \tilde{v}_k \cdot (\hat{a}_{k+1} - \hat{a}_{k-1})$, which has variance

$$\sigma_u^2 \simeq 2.43\sigma_{\tilde{v}}^2. \tag{4.38}$$

Thus, relative to the TED given in (4.29), the TED of (4.32) has its output noise variance reduced by a factor

$$\kappa = \frac{S\sigma_v^2}{\sigma_v^2 - S_V}. \tag{4.39}$$

One can verify that the factor κ is always greater than 1.0. It is a function of the marginal threshold *M*. By way of illustration we calculate κ for different *M* and SNR, and show the result in Fig. 4-5. From Fig. 4-5 we obtain the following observations. First, the suppression factor κ depends strongly on the threshold M. The larger the threshold M is, the larger will be the suppression factor κ, and vice versa. In practice, however, the choice of M is based on a tradeoff. If M is too small, the reduction in the output noise variance will also be small. If M is too large, then undesirable things occur: large amounts of noise as well as the desired signal will be rejected by the TED at its output, and as a result, the TED output may become zero for a long period of time, thereby leaving the timing loop without control. In considering this trade-off, a compromise of *M* equal to 0.25 is selected. It is found by experiment that this threshold can make the TED work satisfactorily for our purpose. Second, the marginal detection-based TED lowers the noise variance at its output significantly at low SNRs but not apparently at high SNRs. This is so because the probability of large noise for low SNR is greater than that for high SNR. Whenever noise exceeds the threshold *M*, the marginal detection-based TED effectively shields this noise from the timing loop. When SNR is high enough such that noise is small, the threshold *M* does not have much influence on the TED output.

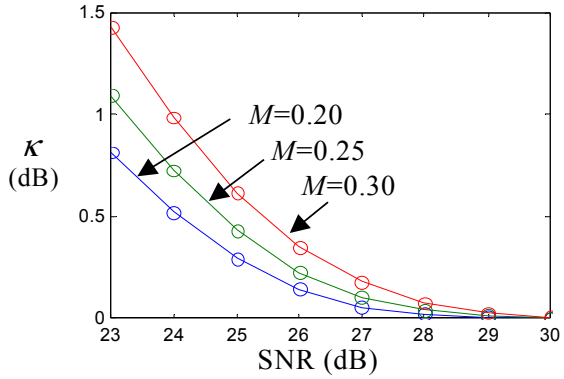


Fig. 4-5: TED output noise variance suppression factor κ at user density 3.0.

We also examine the jitter variance, which is the variance of the noise component of the timing phase error τ, specified as σ_{ψ}^2 and $\sigma_{\tilde{\psi}}^2$ for the conventional TED according to (4.29) and the marginal detection-based TED according to (4.32), respectively [14, Chap. 11]. The numerical results are shown in Table 4-3. Observe that the jitter variance of marginal detection-based TED is significantly reduced at low SNR. The jitter suppression factor κ decreases with increase in SNR. Phase jitter suppression at SNR above 27 dB is negligible.

Table 4-3: RMS VALUES OF THE TIMING LOOP JITTER AND SUPPRESSION GAIN κ (USER DENSITY 3.0).

SNR dB	Conventional TED σ_{ψ} (rms: %)	Marginal detection TED $\sigma_{\tilde{\psi}}$ (rms: %)	Loop jitter suppression κ (dB)
23	2.5174	2.2123	1.1224
24	2.2606	2.0698	0.7660
25	2.0337	1.9264	0.4707
26	1.8335	1.7798	0.2583
27	1.6573	1.6337	0.1249
28	1.5027	1.4937	0.0523
29	1.3676	1.3646	0.0187
30	1.2498	1.2490	0.0057

To verify the above analysis results, we conducted 1000 simulations at 23 dB SNR and user density 3.0. We examined the timing phase error distribution at the 800th bit instant, well within the steady state of tracking mode of operation. The timing phase error distributions for the conventional TED and the marginal detection-based TED are illustrated in Fig. 4-6. This result is basically consistent with the numerical computations. A small discrepancy with those computations may arise from several factors such as the limited number of simulations in collecting the histogram of timing phase error, and residual ISI effects.

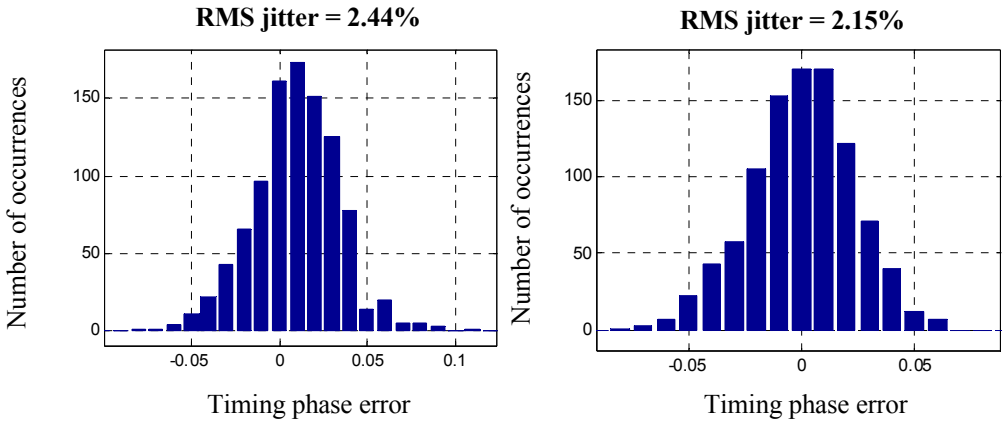


Fig. 4-6: Distribution histogram of timing phase error for the TEDs with (right) and without (left) the marginal detection scheme.

4.5 Optimality of MDFE Acquisition Performance

Fast and accurate acquisition of clock timing is an essential prerequisite for reliable data detection in magnetic recording. Therefore, accuracy and speed of acquisition are important factors when assessing the acquisition performance. Accuracy and speed of acquisition depend largely on the preamble pattern and TED algorithm used. In this section, we investigate the optimality of preamble pattern for the acquisition process, and particularly consider the MDFE magnetic recording system as an example, and study its TED optimality issues.

This section first considers the optimality of the preamble pattern[2] and then analyzes the MDFE TED performance during acquisition.

4.5.1 Optimality of preamble pattern for magnetic recording

The optimality of the preamble pattern can be assessed in terms of the timing SNR of the replay signal at the recording channel output. The timing SNR is defined as the ratio of the power of the time derivative of the replay signal to noise variance within the band $[-0.5, 0.5]$ that is normalized with respect to $1/T$, at the sampling instants. As mentioned in Chapter 2, the harmonic contents of the periodic preamble a_k are assumed to be negligible at the output of the channel. Therefore, for a periodic preamble pattern a_k of period $T_0 = MT$, the replay signal is essentially sinusoidal at normalized frequency $\Omega_0 = 1/M$.

Assuming unit power for the fundamental component of a_k, the PSD of a_k becomes $A(e^{j2\pi\Omega}) = 0.5\left(\delta\left(\Omega+\Omega_0\right)+\delta\left(\Omega-\Omega_0\right)\right)$ in the normalized band [-0.5, 0.5]. Normalizing the variance of noise to unity within the band [-0.5, 0.5], we can compute the timing SNR of the replay signal as

$$SNR_t = (2\pi\Omega_0 / T)^2 \mid H(\Omega_0) \mid^2 \tag{4.40}$$

[2] The problem of signal selection for phase-locked loops so as to minimize the tracking error due to additive noise was addressed by Stiffler in [10].

where $H(\Omega)$ is the frequency response of the channel. For the Lorentzian channel model at user density $D_{u,}$ $H(\Omega)$ is

$$H(\Omega) = j\pi T(D_u / R\ )e^{-j\pi\Omega} \sin(\pi\Omega)e^{-\pi D_u|\Omega|/R} \tag{4.41}$$

where R is the code rate of the channel encoder.

We consider the 4T, 6T and 8T preamble patterns, which result in the replay waveforms as shown in Fig. 4-7. They are sinusoids at normalized frequencies 1/4, 1/6 and 1/8, respectively. We compute the timing SNR of these signals for various user densities. The amplitudes of the sinusoids are given by

$$A_M = \frac{\pi D_u}{R}\sin(\frac{\pi}{M})e^{\frac{-\pi D_u}{MR}} \tag{4.42}$$

where $M = 4, 6$ and 8. The resulting timing SNRs are shown in Fig. 4-8 for the rate 2/3 (1,7) coded Lorentzian channel. The (1,7) code is used for the MDFE detector. Observe that the 4T-pattern is optimal for very low densities and the 8T-pattern for very high densities. The 6T pattern is optimum for medium to high recording densities.

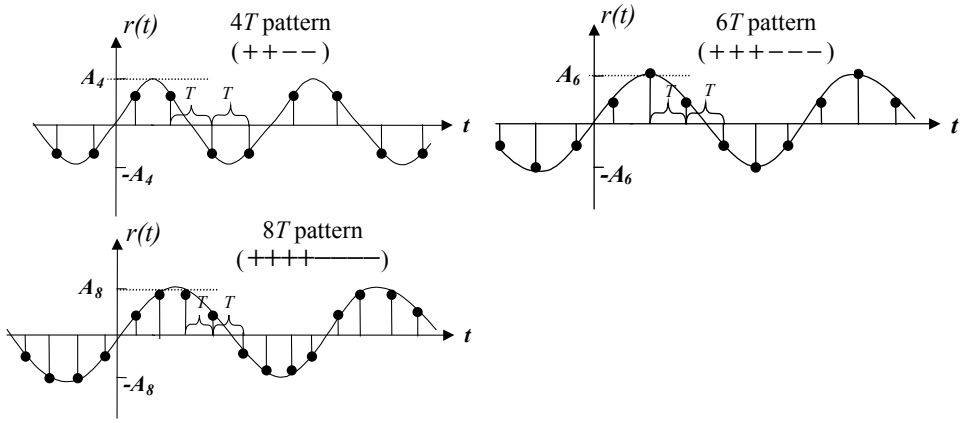


Fig. 4-7: Replay waveforms at the output of Lorentzian channel.

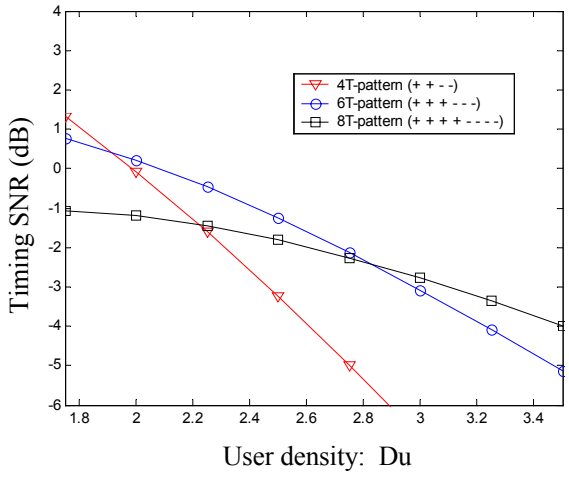


Fig. 4-8: Timing SNR for the 4*T*, 6*T* and 8*T* preamble patterns, on a rate 2/3 (1,7) coded Lorentzian channel.

Similar conclusions were reached in Section 2.3.1 (see Fig. 2-14, Chapter 2) by investigating the efficiency of the ML TED for each of the above preamble patterns. We recall that the TED efficiency is a measure of how much timing information a TED can extract, for a given amount of channel SNR. Timing SNR, by comparison, is a measure of how much timing information the incoming signal carries, normalized with respect to noise power. For a periodic preamble as in the case at hand, timing SNR and efficiency are essentially equivalent.

For comparison purposes, we also evaluate the timing SNR for the Lorentzian channel using the rate 8/9 (0, 4/4) and rate 16/17 (0, 6/6) codes [11] [12]. The results are shown in Fig. 4-9. Observe that the 4*T* pattern is an optimum preamble for low to medium user densities. For medium to high user densities, the 6*T* pattern tends to be optimum. In conclusion, for recording densities that are typical in magnetic recording, the 6*T* pattern is an optimum preamble for both d=0 and d=1 recording systems.

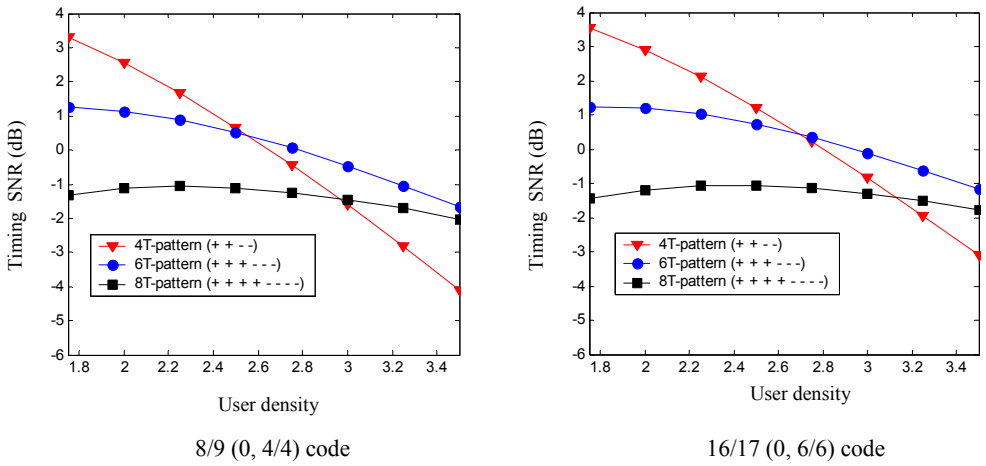


Fig. 4-9: Timing SNR for the 4*T*, 6*T* and 8*T* patterns in a (0,*k*) coded Lorentzian channel.

4.5.2 Optimality of TED for MDFE acquisition

Apart from the type of preamble pattern, the timing acquisition performance depends heavily on the type of TED scheme used. We will show in Chapter 5 that the decision-directed TEDs discussed in the previous section (see (4.18), (4.29)) can also be used for timing acquisition if appropriate precautions are taken to ensure correct detection of the preamble bits [9] [13].

As derived in the preceding section, the error-based ZF TED for MDFE has output (see (4.29))

$$\chi_k = e_k\left(\hat{a}_{k+1} - \hat{a}_{k-1}\right) = \left(y_k - \hat{a}_k\right)\left(\hat{a}_{k+1} - \hat{a}_{k-1}\right). \tag{4.43}$$

The TED performance can be assessed by comparing its efficiency with that of the ML TED [14] [15] since the TED efficiency is a measure of its ability to extract timing information while rejecting noise. Assuming that the noise at the equalizer input is white and that the channel frequency response $H(\Omega)$ has little energy outside the band $[-0.5, 0.5]$, we can deduce the ML TED efficiency for a preamble with frequency Ω_0 as [14]

$$\gamma_{ML} = (2\pi\Omega_0)^2 \left|H(\Omega_0)\right|^2 \Big/ \int \left|H(\Omega)\right|^2 d\Omega \tag{4.44}$$

where $\Omega_0 = 1/6$ for the 6T pattern preamble. The harmonics of the preamble at frequencies $\pm 3\Omega_0$, $\pm 5\Omega_0$, $\cdots$, are assumed to be eliminated by the channel attenuation.

We proceed as follows to derive the efficiency of the error based ZF TED according to (4.43) for MDFE during timing acquisition using the 6T pattern preamble.

Denote the MDFE band-limited equalized bit response in the presence of timing phase error τ (normalized in units T) by q_k^τ, the feedback equalizer taps by b_k, and the Fourier transforms of the ideal equalized bit response q_k^0 and the feedback equalizer taps b_k by $Q(e^{j2\pi\Omega})$ and $B(e^{j2\pi\Omega})$, respectively. Then the Fourier transform of q_k^τ is $Q(e^{j2\pi\Omega})e^{j2\pi\Omega\tau}$, assuming that $q(t)$ has no excess bandwidth, and the slicer input is $y_k = (a \otimes q^\tau)_k - (a \otimes b)_k$ where '$\otimes$' denotes convolution. For the error based ZF TED given in (4.43), the timing function is

$$\begin{aligned}\rho(\tau) &= E[\chi_k] \\ &= E[y_k(a_{k+1} - a_{k-1})] \\ &= \int_{-0.5}^{0.5} -2jQ(e^{j2\pi\Omega})A(e^{j2\pi\Omega})e^{j2\pi\Omega\tau}\sin(2\pi\Omega)d\Omega + \int_{-0.5}^{0.5} 2jB(e^{j2\pi\Omega})A(e^{j2\pi\Omega})\sin(2\pi\Omega)d\Omega .\end{aligned} \tag{4.45}$$

Because q_k^0 and b_k are real-valued, we have $Q(e^{j2\pi\Omega}) = Q^*(e^{-j2\pi\Omega})$ and $B(e^{j2\pi\Omega}) = B^*(e^{-j2\pi\Omega})$ where '*' denotes complex conjugation. Using these facts as well as that $\rho(\tau)$ is a real valued function, we can rework (4.45) into

$$\begin{aligned}\rho(\tau) &= -j\sin(2\pi\Omega_0)\{[Q(e^{j2\pi\Omega_0})e^{j2\pi\Omega_0\tau} - Q(e^{-j2\pi\Omega_0})e^{-j2\pi\Omega_0\tau}] - [B(e^{j2\pi\Omega_0}) - B(e^{-j2\pi\Omega_0})]\} \\ &= 2\sin(2\pi\Omega_0)\{\mathrm{Im}[Q(e^{j2\pi\Omega_0})e^{j2\pi\Omega_0\tau}] - \mathrm{Im}[B(e^{j2\pi\Omega_0})]\} \\ &= 2\sin(2\pi\Omega_0)\{\mathrm{Re}[Q(e^{j2\pi\Omega_0})]\sin(2\pi\Omega_0\tau) + \mathrm{Im}[Q(e^{j2\pi\Omega_0})]\cos(2\pi\Omega_0\tau) - \mathrm{Im}[B(e^{j2\pi\Omega_0})]\}\end{aligned} \tag{4.46}$$

where $\mathrm{Re}[x]$ and $\mathrm{Im}[x]$ denote the real and imaginary parts of a complex number x, respectively. Since $K_d = \left.\dfrac{d\rho(\tau)}{d\tau}\right|_{\tau=0}$, we obtain the TED gain as

$$K_d = 4\pi\Omega_0 \sin(2\pi\Omega_0)\,\mathrm{Re}[Q(e^{j2\pi\Omega_0})]. \tag{4.47}$$

We now consider the noise component $u_k = v_{k-1}(a_k - a_{k-2})$ of the TED output. Denote the Fourier transform of the MDFE forward equalizer coefficients c_k by $C(e^{j2\pi\Omega})$ and the PSD of channel noise $n(t)$ by $N_0/2$. Then, the PSD of u_k at DC can be calculated as

$$\begin{aligned}S_u(1) &= \frac{N_0}{2T}\int_{-0.5}^{0.5} |C(e^{j2\pi\Omega})|^2 \, A(e^{j2\pi\Omega})(2 - e^{-j4\pi\Omega} - e^{j4\pi\Omega})d\Omega \\ &= \frac{N_0}{2T}\int_{-0.5}^{0.5} 4|C(e^{j2\pi\Omega})|^2 \, A(e^{j2\pi\Omega})\sin^2(2\pi\Omega)d\Omega \\ &= \frac{2N_0}{T}\sin^2(2\pi\Omega_0)|C(e^{j2\pi\Omega_0})|^2 .\end{aligned} \tag{4.48}$$

Also note that the SNR in the matched-filter bound sense is $SNR_m = \frac{1}{T}\frac{\int |H(\Omega)|^2 \, d\Omega}{N_0/2}$.

Therefore, by the definition given in (4.1), we obtain the MDFE TED efficiency of the error based ZF TED according to (4.43) as

$$\gamma_{\text{MDFE}} = \frac{(2\pi\Omega_0)^2 T^2 \, |\text{Re}[Q(e^{j2\pi\Omega_0})]|^2}{|C(e^{j2\pi\Omega_0})|^2 \int |H(\Omega)|^2 \, d\Omega}. \tag{4.49}$$

Then, using (4.44), (4.49) and the fact that $Q(e^{j2\pi\Omega}) = H(\Omega)C(e^{j2\pi\Omega})/T$, we can gauge the TED efficiency loss of the MDFE error based ZF TED relative to the ML TED by computing the ratio

$$\boldsymbol{L} \triangleq \frac{\gamma_{\text{ML}}}{\gamma_{\text{MDFE}}} = \frac{|H(\Omega_0)|^2 \, |C(e^{j2\pi\Omega_0})|^2}{T^2 \, |\text{Re}[Q(e^{j2\pi\Omega_0})]|^2} = \frac{|Q(e^{j2\pi\Omega_0})|^2}{|\text{Re}[Q(e^{j2\pi\Omega_0})]|^2}. \tag{4.50}$$

This is a very simple equation indicating that the efficiency loss is fully determined by the equalized bit response. Reducing the difference between $|Q(e^{j2\pi\Omega_0})|$ and $|\text{Re}[Q(e^{j2\pi\Omega_0})]|$ results in a decrease in efficiency loss. The ideal case is $|Q(e^{j2\pi\Omega_0})| = |\text{Re}[Q(e^{j2\pi\Omega_0})]|$ which corresponds to a symmetric equalized bit response. Table 4-4 lists this loss over a range of user densities based on the 6*T* preamble for the Lorentzian channel. A loss factor of 2 means that the timing-jitter variance at TED output will be twice as large for the same channel and timing loop parameters. Observe that the loss of the MDFE TED is small even at very high densities. This suggests that the MDFE TED using the algorithm (4.43) is near optimum for timing acquisition.

Table 4-4: TED EFFICIENCY LOSS OF THE MDFE TED RELATIVE TO THE ML TED.

User density	TED Loss	TED Loss (dB)
2.50	1.0321	0.1372
2.75	1.0470	0.1673
3.00	1.0620	0.2613
3.25	1.0826	0.3449
3.30	1.0930	0.3863
3.50	1.1175	0.4824

4.6 Conclusions

In this chapter, we analyzed the efficiencies of the TEDs used in PR and MDFE magnetic recording systems. In addition to examining the existing TEDs, we developed error based ZF TED schemes for these systems. The error based TEDs are not only simple to implement but also exhibit equivalent or better efficiencies compared to the existing non-error based TEDs. In addition, the MDFE was considered as an example to study the marginal detection-based TED. The result shows that the marginal detection-based TED algorithm can reduce jitter variance. The reduction in jitter variance is significant at low SNRs. Further, using the timing SNR as a measure, we examined the problem of optimal choice of preamble pattern for timing

acquisition for a given recording density. Finally, using the TED efficiency as a measure, we showed that the MDFE TED with 6*T* pattern preamble is near optimum for timing acquisition over a range of recording densities of interest.

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CHAPTER 5

FAST TIMING ACQUISITION FOR DECISION FEEDBACK EQUALIZATION RECEIVERS IN MAGNETIC RECORDING

5.1 Introduction

In hard disk drives, data is written in concentric tracks that are subdivided into sectors. The first 10 to 15 bytes of each sector are put aside for a periodic preamble pattern, which serves, among other purposes, for timing acquisition [1] [2]. Timing acquisition techniques aim to acquire the sampling phase so as to enable the bit detection process to commence. This task should be accomplished reliably in a limited amount of time. In particular, false lock and hang up [9] are to be avoided. Fast timing acquisition techniques were proposed for partial response magnetic recording systems in [10] [12] [11]. In developing these techniques, DC offset and gain were assumed ideal. A non-decision-directed acquisition scheme was reported in [3] [4] for decision feedback equalization (DFE) receivers. Even though this scheme is not affected by erroneous feedback decisions, it is rather sensitive to channel noise and can induce considerable jitter. Moreover, the effects of DC offsets and gain errors were not considered in [3] [4].

Ideally, the same timing error detector (TED) can be used for both acquisition and tracking modes. Resulting advantages include simplicity and effective suppression of channel noise. In practice, the timing acquisition process has to deal with DC offsets and gain errors in the channel, as well as with timing phase errors. In this situation, false lock and hang up problems may become severe. In DFE receivers, wrong decisions in the feedback equalizer due to possibly large initial timing, gain and DC errors can easily cause false lock and hang up. It is necessary to develop techniques for avoiding these problems even in worst-case initial situations.

This chapter is devoted to the development of fast timing-acquisition techniques for DFE receivers in magnetic recording. In particular, we consider the multi-level DFE (MDFE) receiver [5] [6]. Section 5.2 provides a novel timing acquisition scheme, which can prevent the

false lock problem [7]. Section 5.3 proposes another new scheme in a more general form to ensure an effective, rapid and reliable acquisition process [8]. In Sections 5.2 and 5.3, a number of simulations on the MDFE receiver are presented. The conclusions are drawn in Section 5.4.

5.2 Fast Acquisition for DFE with Modified Equalization

The false lock problem arises if the TED has zero output at non-ideal phases. If these spurious zeros are avoided or eliminated, then false lock can be prevented. In DFE receivers, erroneous TED outputs can stem from wrong decisions in the feedback loop. To solve this problem, we propose an acquisition scheme that uses a modified forward equalizer to ensure that the feedback register is loaded with the correct data pattern.

5.2.1 Inherent false lock in the MDFE TED

As shown in Chapter 4, the 6T pattern (+++−−−) is an optimal preamble for a d=1 recording channel from medium to high densities. The MDFE receiver is designed for delivering a good performance on d=1 recording channels. Recall from Chapter 4 that the transition-based TED used for timing acquisition in MDFE has output $\chi_k = (y_k - \hat{a}_k)(\hat{a}_{k+1} - \hat{a}_{k-1})$ where y_k is the slicer input sample and $\hat{a}_k$ is the corresponding decision that is produced by the slicer. To illustrate the features of the transition-based TED, the output is calculated while timing phase error is gradually ramped up from -T to +T and then down again with the timing loop open (see Fig. 5-1).

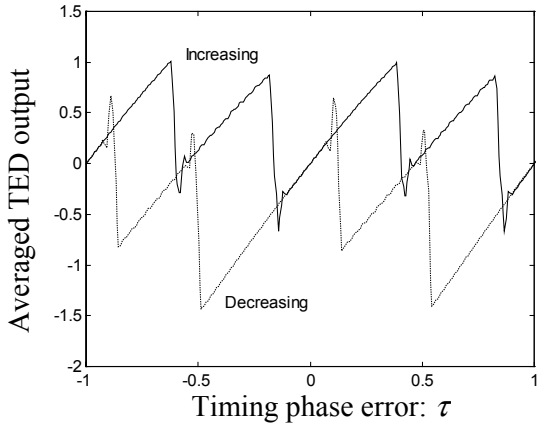

Fig. 5-1: Averaged TED output when the normalized timing phase error is changed dynamically from -1 to 1 and from 1 to –1.

Since the TED output is non-zero only when there is a transition in the input data bits, it is averaged through a six-bit sliding window for continuous display. It is clear that there is hysteresis in the process. The hysteresis is useful in that it may eliminate the 'hang-up' problem. However, observe that the timing loop may falsely lock to the phases with errors near ±0.5T. On closer examination, we found that the preamble pattern was incorrectly detected as '++−−−−' or '++++−−' in the false lock regions. In the general case, where there may also be large initial DC offsets and gain inaccuracies, the system can be even more susceptible

to false lock. To illustrate the false lock effect, we do following. Setting the initial timing phase error to 0.45T and SNR to 27 dB at user density 3.0, we made 10 simulation runs with the timing loop closed. The phase error convergence during the first 300 channel bits is shown in Fig. 5-2. As expected, the curves are all falsely locked to wrong phases with errors around 0.5T.

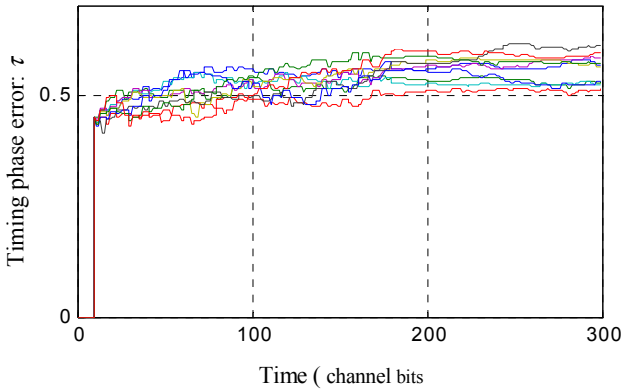

Fig. 5-2: Phase convergence curves at D_u = 3.0 and SNR = 27 dB with the MDFE TED (10 simulation runs).

5.2.2 Modified acquisition scheme

We now propose an acquisition scheme for eliminating the false lock problem associated with the MDFE TED [7]. The key idea is to prevent erroneous data patterns in the feedback register, thereby preventing erroneous TED outputs. The scheme, which contains a modified forward equalizer and several switches, is illustrated in Fig. 5-3. It is worth noting that this scheme is also applicable for other DFE-type receivers.

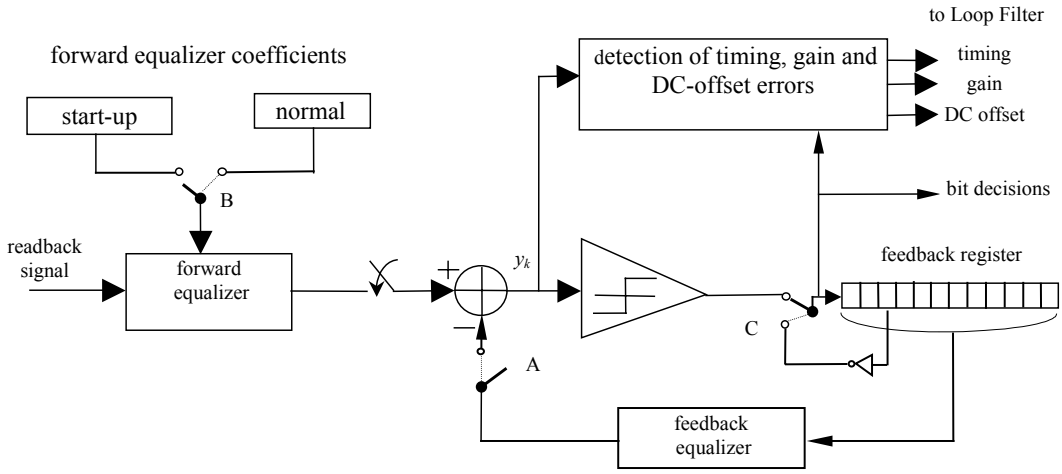

Fig. 5-3: Modified forward equalizer based MDFE timing acquisition scheme.

The acquisition procedure involves the following four steps:

Step 1: In this step, the feedback shift register gets loaded with the correct 6T '+++−−−' pattern that is close in phase to the one that should ideally be detected. This is done with no feedback equalizer applied. To acquire the correct 6T pattern with no feedback equalizer, the forward equalizer must be modified (i.e., Switch B is set to 'Start-up') to provide the correct

phase for the preamble waveform. This may be done by cascading the equalizer with a *(a+bD)* filter. Suitable coefficients are a = 0.9091 and b = -0.0949 at the user density 2.5. During this step, Switch A remains open and Switch C is connected to the slicer output.

Step 2: This step reconnects the feedback equalizer and resets the forward equalizer to normal, after the feedback register contents are detected to be the correct 6T pattern. As soon as three consecutive bits with the same sign are detected at the slicer output, Switch A is closed, Switch B is set to 'normal', and Switch C is set to the inverter output. As a result, the feedback register is disconnected from the slicer output and its contents recirculate. This ensures the register contents to be the desired '+++−−−' pattern.

Step 3: When five user bytes after **Step 2** have elapsed, the frequency loop is enabled, i.e. the timing loop switches from first-order to second-order.

Step 4: Eleven user bytes after **Step 2**, Switch C is reconnected to the slicer output so that the recirculation stops and real decisions flow through the shift register. At the same time, the timing, gain, and DC loops are switched to tracking mode (i.e. loop gains are reduced by a factor of 4) and the detected bits are checked for the presence of the synchronization word (sync byte).

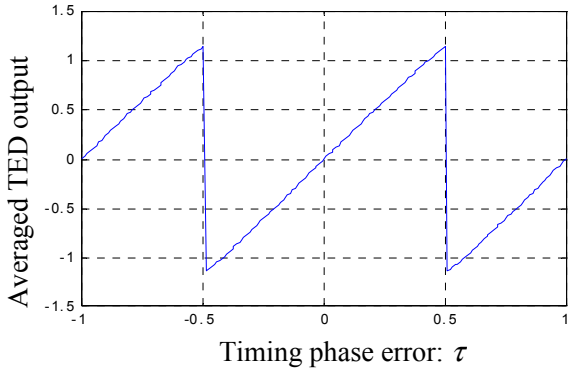

Fig. 5-4: Timing function of MDFE using the 4-step acquisition scheme.

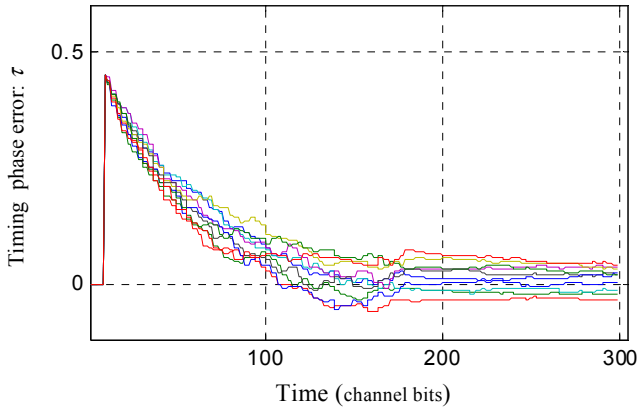

Fig. 5-5: Phase convergence curves at D_u = 3.0 and SNR = 27 dB (with the 4-step acquisition scheme).

Using this procedure we repeat the simulation of Fig. 5-1. The result is shown in Fig. 5-4. Observe that there is no difference between 'increasing' and 'decreasing' any more, and that the false-lock spots around ±0.5T have been eliminated. To illustrate this, we made the

following simulations. We introduced a normalized timing phase error of 0.45 and a normalized frequency offset of 0.001 during the initial part of the acquisition process at the 10^{th} channel bit. The initial gain and DC offset are set to 1.0 and 0, respectively. The channel SNR is 27 dB and the user density is 3.0. Timing, gain and DC loops are closed and work simultaneously. The simulation result is shown in Fig. 5-5. As expected, false lock no longer occurs.

5.2.3. Further simulations

To thoroughly study the proposed acquisition scheme, Monte-Carlo simulations were conducted at user density 2.5. Timing, gain and DC loops are closed and work simultaneously. Initial conditions are listed in Table 5-1.

Table 5-1: INITIAL CONDITIONS OF MONTE-CARLO SIMULATIONS FOR MDFE TIMING ACQUISITION.

Parameters	Initial conditions
1) Frequency error:	uniform distribution from -0.1% to 0.1%
2) Phase error:	uniform distribution from -0.5 to 0.5 bits
3) Gain error:	log uniform distribution from 0.5 to 2
4) DC offset:	uniform distribution from -0.5 to 0.5
5) Detector SNR:	14 dB (defined as the ratio of the inner eye magnitude to the RMS noise at the input of the slicer).

The termination condition of the simulations is that sync bytes are correctly recognized. Acquisition failure is said to occur when the sync bytes are not detected at the end of the acquisition process. No acquisition failures were observed in 20,000 acquisition trials. The average value of the inner eye-level error is found to be 0.2, its standard deviation is 0.004, and the maximum value is 0.29. Figs. 5-6, 5-7 and 5-8 show one set of convergence curves for the VCO frequency, VGA gain, and DC offset, respectively. The convergence is false-lock-free with good convergence speed.

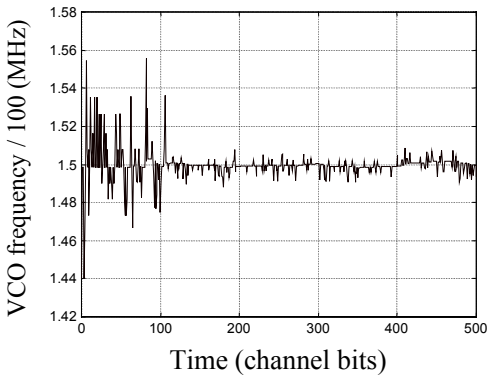

Fig. 5-6: Convergence of VCO frequency (data rate in the channel is 150 Mb/s).

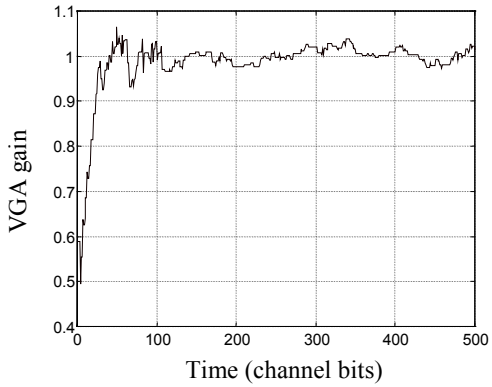

Fig. 5-7: Convergence of VGA gain (ideal value of VGA gain is 1.0).

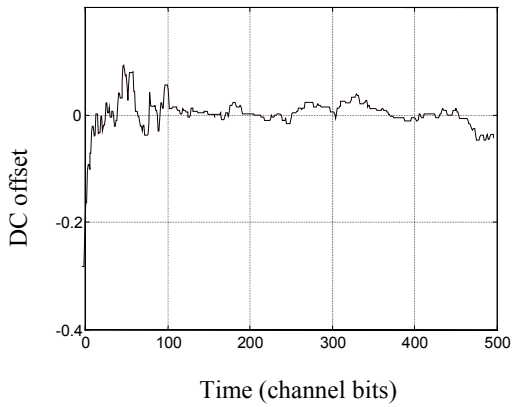

Fig. 5-8: Convergence of DC offset (ideal value of DC offset is 0).

5.3 Modified Threshold-based Timing Acquisition Scheme for DFE

Hang up during acquisition may not be easily noticed because it is an event of low probability and the sampling phase can still converge to the steady state eventually [9]. However, hang up is unacceptable in magnetic recording, where rapid phase convergence is required within a limited period of time. Hang up and false lock are two of the most serious problems of timing acquisition. This is especially true for DFE acquisition, where wrong decisions in the feedback register may propagate and degrade acquisition behavior. In this section, we propose a new and general scheme for DFE timing acquisition for eliminating false lock and effectively lowering the probability of hang up, and at the same time, tolerating large gain and DC errors [8]. The main idea of the scheme is to generate a modified threshold for the slicer to ensure the correct pattern in the feedback register for avoiding false lock, and to introduce hysteresis for preventing hang up.

5.3.1 Existing variable threshold approach for acquisition

The idea of using variable threshold detection was earlier reported for PRML receivers in which a 4*T*-pattern preamble is employed for timing acquisition [10] [11] [12]. To achieve rapid acquisition and prevent hang up, a variable threshold $c_k = \lambda \cdot \hat{a}_{k-2}$ (λ being a scale-factor)[1], is used in [10] to produce hysteresis in the timing function. However, this scheme cannot be used directly for DFE acquisition because erroneous feedback decisions due to initial errors in phase, gain and DC can lead to false lock. To illustrate this, we simulated the MDFE timing function using the 6*T* ('+++−−−') preamble in the absence of noise. The error based ZF TED has output $\chi_k = e_{k-1}(\hat{a}_k - \hat{a}_{k-2})$. Decisions $\hat{a}_k$ are made using a slicer with variable threshold $c_k = \lambda \cdot \hat{a}_{k-3}$. We investigated the impact of channel DC offset (DC), VGA gain (g) and the threshold scale-factor (λ) on the MDFE timing function. Ideal values of these parameters are $\mathrm{DC} = 0$, $g = 1.0$ and λ=1.0. At the start of acquisition process, however, DC and g may exhibit errors. We estimated the timing function (the averaged TED output) using the 6*T* pattern, for all possible initial contents in the feedback register and for normalized timing phase errors ranging from –2 to 2. The result is a set of overlapped timing functions, shown in Fig. 5-9. Fig. 5-9(a) depicts the timing function for the ideal condition. Clearly, no false lock phases exist since the timing function is zero only at integer values of τ. Also, a considerable hysteresis range is observed with its edges close to the desired phase. Such a hysteresis range gives the timing loop excellent immunity to hang-up. However, the timing function changes due to errors in g, DC and λ. For instance, increase and decrease of λ can result in the timing functions of Figs. 5-9(b) and (c), which exhibit false lock spots. Similar false lock spots are also seen in Figs. 5-9(d) to (f) in the presence of DC offset and gain errors.

To demonstrate the resulting false lock, we provide a simulation example. Fig. 5-10 illustrates the closed-loop phase convergence in the presence of a fixed DC offset 0.5. Observe that the loop may lock to the incorrect phases ±0.5 even though the modified threshold $c_k=\hat{a}_{k-3}$ is used. Closer examination reveals that during false lock the decisions of the MDFE detector differ from the 6*T* pattern "+++−−−". Further studies show that for certain initial values of DC and timing phase errors, false lock can happen even with a closed DC loop. Thus, we may conclude that the threshold $c_k=\hat{a}_{k-3}$ fails to prevent false lock in the presence of significant DC errors.

We also made similar investigations as above on the effect of a fixed gain error at the slicer input. We observed several false lock phases when the gain is set to 0.5. Note that studying the effect of gain at the slicer input is analogous to gain studies in non-feedback systems such as partial response channels. The simulations show that false lock tends to exist for conditions g<1.0, g>2.6, λ>1.0, λ<0.6 and |DC|>0.35. Hence, only for a small range of values of g, DC, and λ will this scheme work reliably.

[1] One can check that, for the 4*T* preamble, the slicer using the variable threshold $c_k = \lambda \cdot \hat{a}_{k-2}$ is most likely to make 4*T* pattern decisions. For the 6*T* preamble, same reasoning applies for the use of the threshold $c_k = \lambda \cdot \hat{a}_{k-3}$ to make 6*T* pattern decisions.

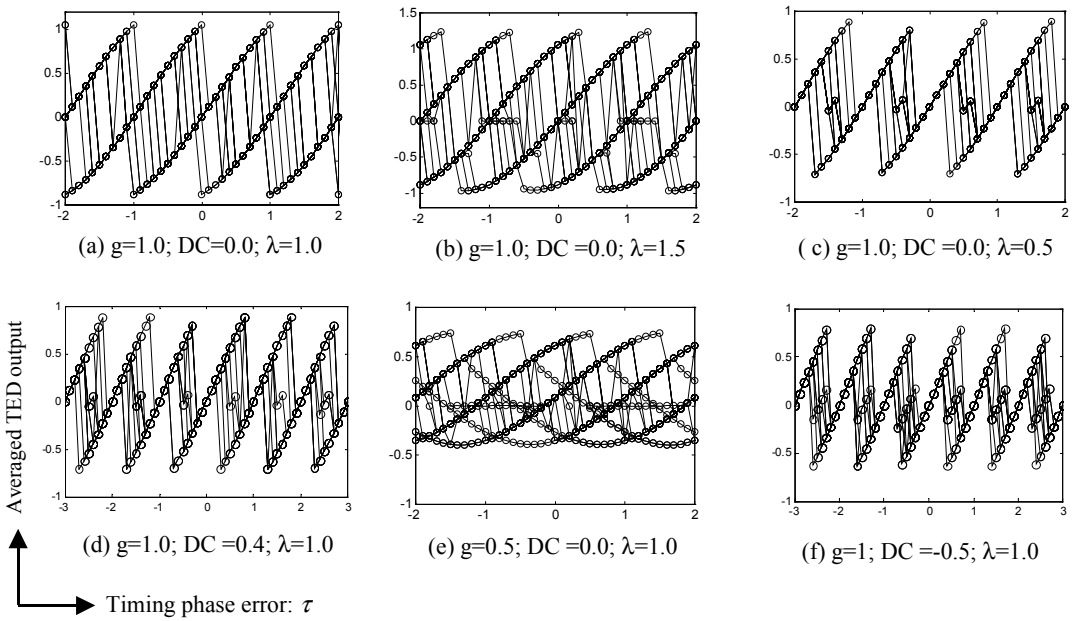

Fig. 5-9: Timing functions based on the variable threshold $c_k=\lambda\hat{a}_{k-3}$ for MDFE acquisition scheme using the $6T$ ('+++---') preamble *(*Horizontal axis: normalized timing phase error, τ; Vertical axis: averaged TED output*).*

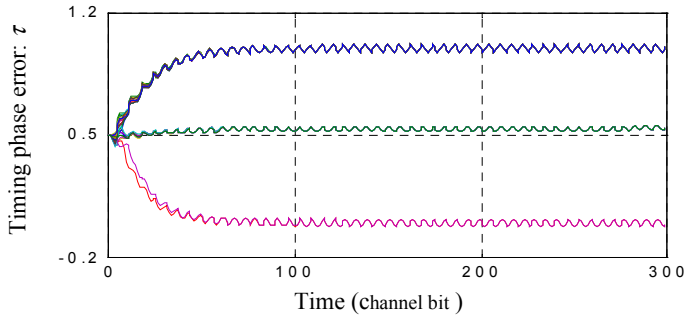

Fig. 5-10: Closed-loop phase convergence in the presence of a fixed DC offset 0.5 with modified threshold $c_k=\hat{a}_{k-3}$ in a noiseless channel.

5.3.2. Modified threshold scheme

We now proceed to develop an improved modified threshold scheme. Fig. 5-11 shows the structure of the proposed modified threshold based acquisition scheme for DFE-type receivers. During acquisition, the signal from the forward equalizer is a sinusoidal waveform. It is sampled at instants $t_k = (k+\tau)T$ which are controlled by the timing recovery system. The resulting discrete-time sequence x_k normally has rate $1/T$ and may suffer from a timing phase error τ (normalized in units T). Subtraction of the feedback equalizer output yields a sequence y_k, which in the usual case is applied to the slicer for making decisions. In the proposed acquisition scheme, a special threshold sequence c_k is subtracted from y_k to produce a

sequence $\tilde{y}_k$ that is passed to the slicer. The sequence c_k is the output of an additional FIR filter, called modified-threshold (MT) FIR filter, which uses the past decisions as its input. Note that the feedback equalizer and the threshold FIR filter could be merged into a single filter without affecting the detection performance. However, we do not do this in order to be able to use the same TED during acquisition and tracking. To this end the TED should operate on the sequence y_k, which must hence be produced explicitly.

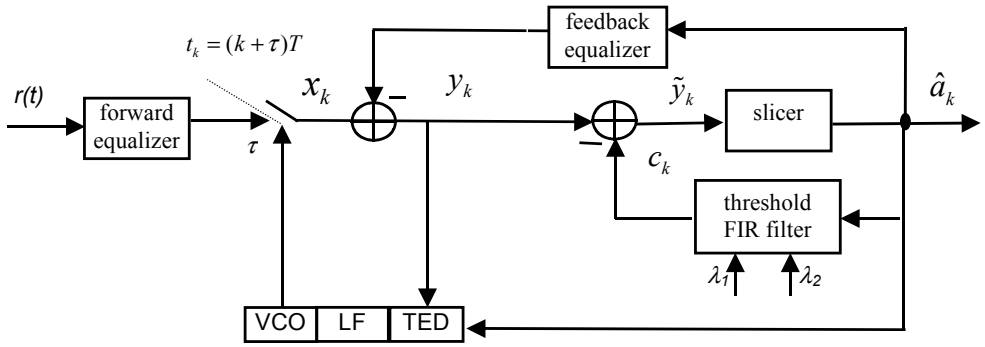

Fig. 5-11: Modified threshold timing-acquisition scheme for DFE detector.

For a preamble in the form of a 6T pattern ($+++---$), c_k is proposed to be

$$c_k = \lambda_1(\hat{a}_{k-3} - \hat{a}_{k-5}) + \lambda_2 \sum_{i=1}^{6} \hat{a}_{k-i} \tag{5.1}$$

where typical values of the real-valued scale-factors λ_1 and λ_2 are 1.0 and 1/6, respectively. The corresponding filter is depicted in Fig. 5-12. Below, we explain the reasons for constructing the threshold according to (5.1).

First, for the 6T preamble, the decision pattern should ideally obey $\hat{a}_k = -\hat{a}_{k-3}$, which is a basic feature of the correct 6T pattern ($+++---$). Any initial pattern in the feedback register should be converted into a pattern meeting this rule with the help of the MT sequence c_k. Secondly, the decision pattern should have zero DC, which is a second feature of the correct 6T pattern. The false lock patterns with DC, such as '$++++--$' and '$++----$', should be suppressed by applying the MT sequence. Similarly, the decision pattern should have no content at the Nyquist frequency 1/(2T). Notice that the 2T pattern "$+-+-$" also obeys $\hat{a}_k = -\hat{a}_{k-3}$. We must make sure that the MT FIR filter does not encourage the 2T pattern to appear in the feedback register. Finally, after loading a correct 6T pattern ($+++---$) into the feedback register, the slicer with the MT sequence should be able to shift the correct pattern from one phase to another. This provides the slicer with the ability not only to make the correct decision pattern but also to acquire the correct phase.

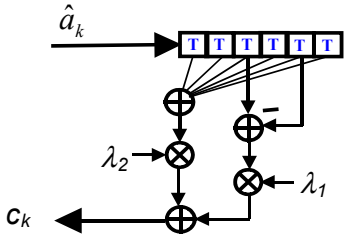

Fig. 5-12: Structure of modified threshold filter.

The first term of (5.1) promotes the slicer output sequence to obey $\hat{a}_k = -\hat{a}_{k-3}$. At the same time, it causes the frequency response of the MT FIR filter to have a null at $1/2T$ so as to suppress $2T$ patterns. The threshold scalar λ_1 is chosen to be 1.0 so that the modified threshold c_k has the form "$\cdots -2-2\,0+2+2\,0-2-2\,0+2+2\,0\ \cdots$" for a valid $6T$ pattern of any phase. Using this sequence, the slicer will most probably make a decision $\hat{a}_k$ to be +1 (resp. –1) when c_k is –2 (resp. +2), and to be +1 or –1 when c_k is zero. This yields a hysteresis effect and equips the slicer with the ability to shift a $6T$ pattern from the wrong phase to the correct phase. Thus, the sequence of (5.1) can help to convert any wrong pattern in the feedback register into the $6T$ pattern with the correct phase. The second term of (5.1) promotes the slicer output to be DC free over any block of 6 bits. It is meant to monitor and suppress the DC component in the decision sequence. We make the choice of the threshold λ_2 as 1/6 because we prefer the MT FIR filter to be as short as possible when estimating the DC value. A short length FIR filter is simple and efficient, and thus desirable for cost effective solutions. Note that for detecting the DC value of the $6T$ pattern stream, the valid window should cover at least one period of the stream. This determines that the minimum length of the window is $6T$. The scalar $\lambda_2 = 1/6$ is meant to obtain an unbiased DC level estimate.

By way of illustration, we show in Fig. 5-13 the role of the MT sequence c_k in making the slicer determine the correct $6T$ pattern. Assume that the sequence $\hat{a}_k$, which is a valid $6T$ pattern, represents the slicer output. The threshold sequence c_k is calculated by applying (5.1) to the $\hat{a}_k$ sequence. Observe that c_k is zero for every third bit instant, thereby letting the slicer make decisions based on y_k. For the next two bits of every 3-bit interval, the threshold sequence c_k is +2 or –2, thereby strongly influencing the decisions of the slicer. This introduces the possibility for the slicer output sequence to shift from one phase of the $6T$ pattern to another. To see this, consider the time instant n (i.e. $k = n$) at which $c_n = 0$. Let the slicer output at this instant be $'+'$ instead of $'-'$. Using similar arguments, we can see the slicer decisions at the instants $n+1$ and $n+2$ to be $'+'$ with the corresponding threshold $\tilde{c}_k = -1.67$ for $k = n+1$ and $n+2$. This causes the threshold $\tilde{c}_k$ at the instant $n+3$ to be +2.33, thereby resulting in a most likely decision of $\hat{a}'_{n+3} = -1$. Following this, we see that the decision sequence $\hat{a}'_k$ from the instant $k = n$ onwards is a one-bit shifted version of the sequence $\hat{a}_k$. This mechanism helps the slicer to traverse the different possible patterns to arrive at the correct pattern.

k	…	*n-3*	*n-2*	*n-1*	*n*	*n+1*	*n+2*	*n+3*	*n+4*	*n+5*	*n+6*	n+7	*n+8*	*n+9*	*n+10*	…		
$\hat{a}_k$	…	+	–	–	–	+	+	+	–	–	–	+	+	+	–	–	–	…
c_k	…	0	+2	+2	0	-2	-2	0	+2	+2	0	-2	-2	0	+2	+2	…	
$\hat{a}'_k$	…	–	–	–	+	+	+	–	–	–	+	+	+	–	–	–	…	
$\tilde{c}_k$					…	0	-1.67	-1.67	+2.33	+2	0	-2	-2	0	+2	+2	0	…

Fig. 5-13: Illustration of the role of MT sequence c_k to shift the decision sequence from one phase of the $6T$ pattern to another.

To examine the effect of the MT filter, we consider the MDFE detector with arbitrary initialization of the feedback register, and monitor the pattern in the feedback register for the $6T$ preamble input and a fixed timing phase error. The user density is 2.5, and noise is absent. The

feedback equalizer has 9 taps. All possible initial feedback register contents (512 patterns) are considered, with timing phase error ranging from –6T to 6T. Each pattern is identified using a tag number. The status of the first 25 tagged patterns is shown in Fig. 5-14.

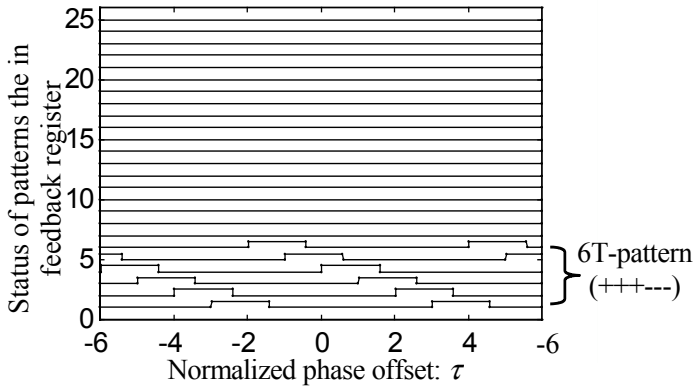

Fig. 5-14: Results indicating which of the first 25 tagged patterns are presented in the feedback register at the time of the 25th bit instant from the start of acquisition.

The numbers 0 to 5 represent the correct 6T pattern with the six different phases. The numbers 6 to 25 represent the pattern "$+++--$" with the six different phases, the pattern "$++----$" with the six different phases, the patterns "$+-$" and "$-+$", the pattern "$++++++$", and the pattern "$------$". We specifically show these 25 patterns because they are most likely to appear in the feedback register during acquisition with the 6T preamble. In the figure, the horizontal axis shows the timing phase error τ (normalized in units T) at the sampler, and the vertical axis shows the status of each pattern. Here, the k^{th} trace represents the case where the feedback register is initialized with the k^{th} pattern. A 'high-level' on the k^{th} trace for a particular timing phase error means that the k^{th} pattern is the content of the feedback register for that specific timing phase error from the 25th instant onwards, whereas a 'low-level' status means that the k^{th} pattern does not appear. Thus, the conclusion from Fig. 5-14 is that even though any random pattern can be the initial content of the feedback register, only the 6T patterns ($+++---$) will survive after 25 bits. This indicates that by using the MT FIR scheme, we need not worry about initializing the feedback register with particular patterns.

It is worth noting that the approach developed here for a 6T preamble is easily generalized to other preamble periods.

5.3.3. Effect of parameter variations

To examine the performance of the MT scheme in the presence of gain, DC and threshold variations, we repeat the simulation of Fig. 5-9 for the scheme at hand. The simulation result is shown in Fig. 5-15.

Unlike Fig. 5-9, where hysteresis is introduced at the expense of causing false lock, the timing functions in Fig. 5-15 display no false lock while preserving a considerable hysteresis range. Simulation studies show that this threshold scheme can tolerate gain factors from 0.5 to 2.0 and DC offsets from –0.5 to 0.5 with no false lock while retaining adequate hysteresis. The two threshold scale-factors can vary by ±3 dB with respect to their norminal values.

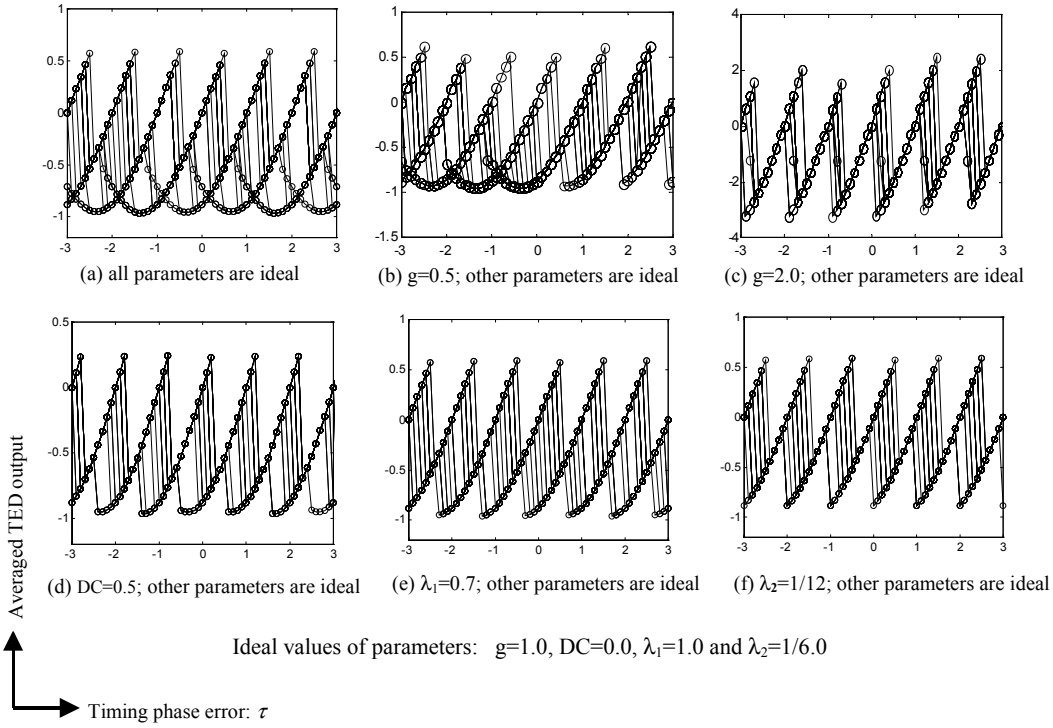

Fig. 5-15: Timing functions based on the MT scheme $c_k=\lambda_1(\hat{a}_{k-3}-\hat{a}_{k-3})+\lambda_2\sum_{i=1\to6}\hat{a}_{k-i}$. (Horizontal axis: timing phase error, τ; Vertical axis: averaged TED output).

By way of illustration, we repeated the simulation of Fig. 5-10, and show the result in Fig. 5-16. Observe that there are no false-lock phases. The oscillatory nature observed in the phase convergence curves of Fig. 5-10 and Fig. 5-16 is due to the presence of the DC offset. The curves would have been smooth if the DC offset was zero or if the DC loop was closed.

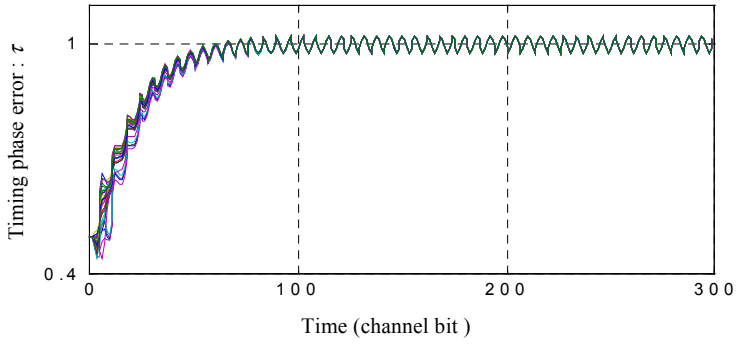

Fig. 5-16: Closed-loop phase convergence in the presence of a fixed DC offset 0.5 with the MT scheme $c_k=\lambda_1(\hat{a}_{k-3}-\hat{a}_{k-3})+\lambda_2\sum_{i=1\to6}\hat{a}_{k-i}$ for a noiseless channel.

To thoroughly examine the performance of the scheme, we conducted more extensive simulations using a second-order timing loop and first-order VGA and DC loops. The timing-loop has natural frequency $\omega_n T = 0.035$ and damping factor $\varsigma = 0.7$. The VGA and DC parameters have time constants of 25 channel bits each. Fig. 5-17 illustrates a typical acquisition simulation result for MDFE at SNR 27 dB and user density 2.5. The normalized initial timing phase error and frequency offset are set to -0.5 and 0.1%, respectively. The initial

gain and DC errors are both set to 0.5, where gain error is referred to as the ratio of the total gain and the ideal gain, and DC error as the DC offset with respect to zero. The horizontal axis represents time in number of channel bits. The total length of preamble pattern considered for acquisition is 192 channel bits. At the time instant 180, which approximately marks the acquisition end, all critical parameters have properly converged.

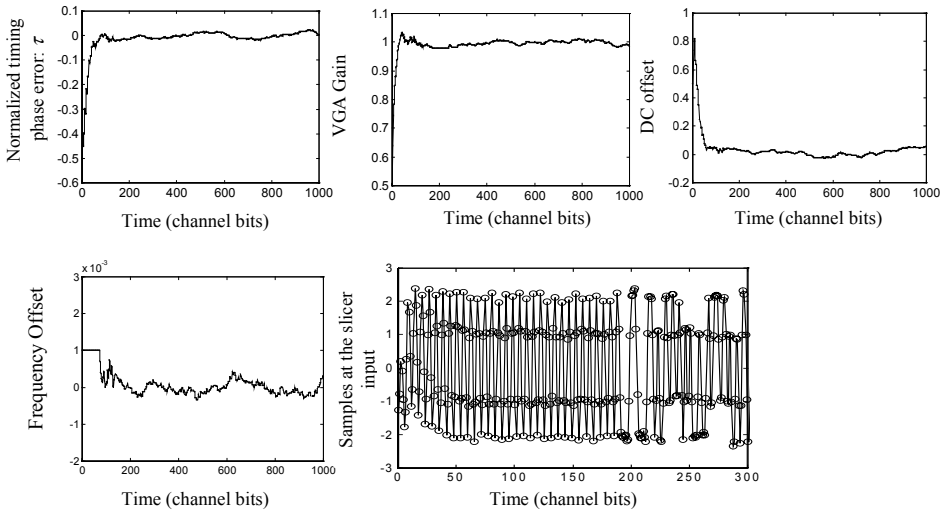

Fig. 5-17: Convergence of parameters with closed timing, gain and DC loops (horizontal axis: time in channel bits).

To gauge the robustness of the scheme, we made Monte Carlo simulations under the conditions of high user density 3.0 and low SNR 23 dB. Initially, the timing phase error is 0.5T, the frequency offset is 0.1%, and the gain and DC are 0.5 and 0.35, respectively. The overlaid phase convergence curves for 5000 simulations with different noise sequences are shown in Fig. 5-18. Analysis of the timing phase error distribution at the bit-instant 180 reveals that the phase bias is close to zero and phase-jitter is less than 1.8% RMS, thereby showing that the proposed acquisition scheme is very reliable.

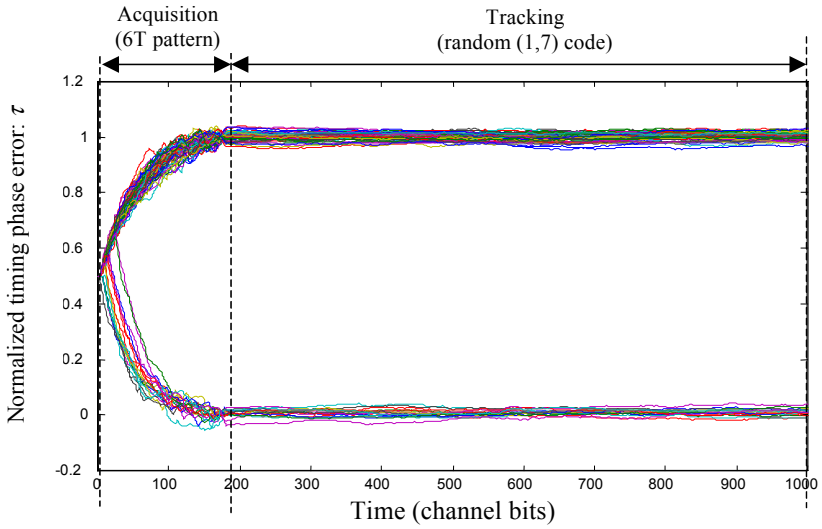

Fig. 5-18: Phase convergence curves for 5000 acquisition trials at user density 3.0 and 23 dB SNR.

5.4 Summary

In this chapter, we developed two new and effective solutions to fast timing acquisition for DFE receivers in magnetic recording systems. One solution uses special equalizer coefficients and a control procedure with switches. This technique has been shown to be effective for solving the false lock problem. On the other hand, the second solution, which uses a modified threshold scheme, prevents false lock and hang up in a more general manner. Simulations have shown that this scheme can tolerate large initial errors in gain, DC offset and threshold scalars.

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CHAPTER 6

IMPLEMENTATION OF MULTI-LEVEL DECISION FEEDBACK EQUALIZATION TIMING RECOVERY SYSTEM

Multi-level decision feedback equalization (MDFE) [1] is an elegant simplification of fixed-delay tree search with decision feedback (FDTS/DF) [2] [3], which is an alternative to the Viterbi detector for d=1 coded channels and has a similar structure to DFE. A 100 Mb/s experimental MDFE read channel was designed and prototyped using discrete-components [4] [7]. In the prototype, the analog forward equalizer consists of two bi-quads that are designed to maximize the detection signal-to-noise ratio (SNR). The feedback equalizer consists of a 6-tap FIR filter and an exponential decay circuit to reduce hardware complexity. The digitally implemented timing/gain/DC loops are updated only when there are transitions at the slicer input. The MDFE prototype project was targeted at evaluating and testing the MDFE read channel on both bench and spinstand [4] [5] [7]. The implementation work involved investigation of several aspects such as robust equalization strategy, reliable acquisition, byte-synchronization, error propagation, implementation of timing/gain recovery, and error rate evaluation on bench and spinstand.

In this chapter, we describe the prototype, illustrate the circuit realization of main functional modules, present the design and realization of timing recovery circuitry, and report on the evaluation of the prototype on bench and spinstand. The main emphasis of this chapter will be on the timing recovery system, which is the contribution of the author. The author developed the MDFE timing recovery circuitry board; he implemented and verified several critical circuit blocks including the digital TED generating circuits, charge-pump and loop filter circuits, lock-to-preamble circuits, and sync byte detection circuits. These circuit blocks constitute the MDFE timing recovery circuitry board, working at 150 MHz/s along with other parts of the MDFE prototype. Nevertheless, for the sake of completeness, we will also briefly discuss the modules related to the MDFE forward equalizer and critical loop, which were implemented by the author's partners in the MDFE project.

6.1 Introduction to MDFE Read Channel Prototype

The decision to make the prototype using discrete components, instead of a full-scale integrated circuit approach, was primarily motivated by the intention to demonstrate the main features of MDFE. The MDFE has been claimed to be a simple and low-cost solution for data detection in digital recording systems. Further, the short time frame of one year set for the demonstration of the MDFE principle in hardware was another reason to resort to an implementation using readily available discrete components.

The overall structure of the MDFE prototype is depicted in Fig. 6-1. There are several functional modules, viz. the forward equalizer, the critical loop with analog to digital converter (A/D) and feedback equalizer, timing/gain/DC extraction, timing/gain/DC offset distribution units and loop filters, voltage controlled oscillator (VCO) and crystal oscillator, sequencing generator, and analog and digital interfaces. The analog readback signal from the pre-amplifier of a disk drive head is applied to the MDFE prototype, whose output is a detected bit stream taking values +1 and –1. The user interface module equips the prototype with functions of loading and programming the equalizers, data sequences and timing/gain recovery units.

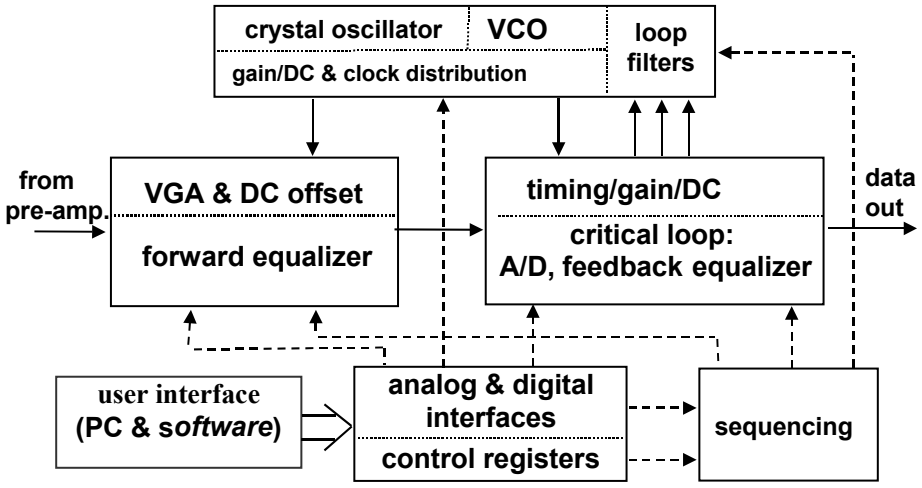


Fig. 6-1: Structure of the MDFE prototype.

An analytic procedure is developed for the design of a simple continuous-time forward equalizer (tested with different channel models at several densities) [6] [7]. Essential implementation constraints are included in the design at the cost of a minor performance degradation [7]. The first feedback tap is forced to zero to eliminate tight feedback loop. The length of the feedback equalizer and the magnitude of its taps are constrained in order to reduce error propagation. The forward equalizer is a 3-zero and 4-pole filter and the feedback equalizer has 6 taps with an exponential tail.

Fig. 6-2 shows the implementation of the forward path from the preamplifier output to the summing node of the critical loop. The input signal from the preamplifier is approximately 0.3~0.6 volts peak-to-peak (V_{pp}) differential with 50 ohms termination. The differential input is transformed and amplified into a current signal via the wide-band amplifier CLC220. The main part of the forward path is a 3-zero 4-pole analog forward equalizer and is implemented using a

pair of bi-quad filters. The first section of the bi-quads is a 1-zero 2-pole filter and has low-pass characteristics. The second section is a 2-zero 2-pole filter and has band-pass characteristics. The forward equalizer output is a low-impedance (50-ohm) differential signal, which should be amplified to 2.0 V_{pp} for subsequent A/D conversion. To accomplish this, the differential signals are applied to the low-distortion, high-precision and wide-band amplifier AD9618, which is an ideal choice for driving and buffering flash A/Ds.

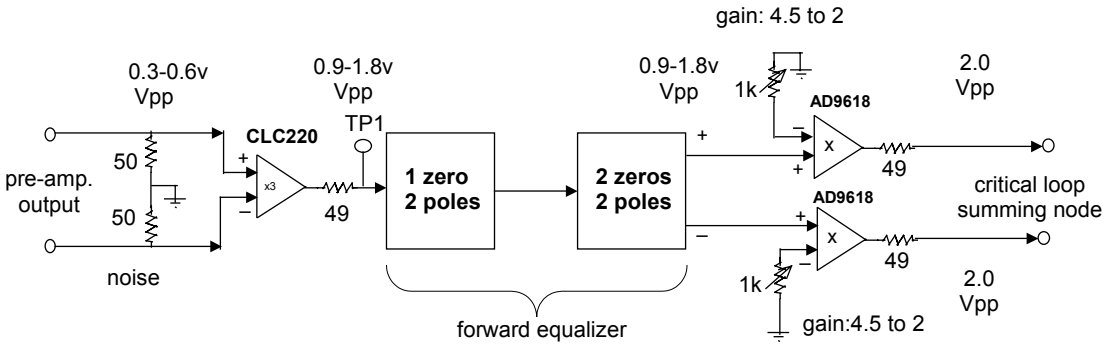


Fig. 6-2: Implementation of the forward path from the preamplifier output to the critical loop input, consisting of a 4-pole/3-zero forward equalizer.

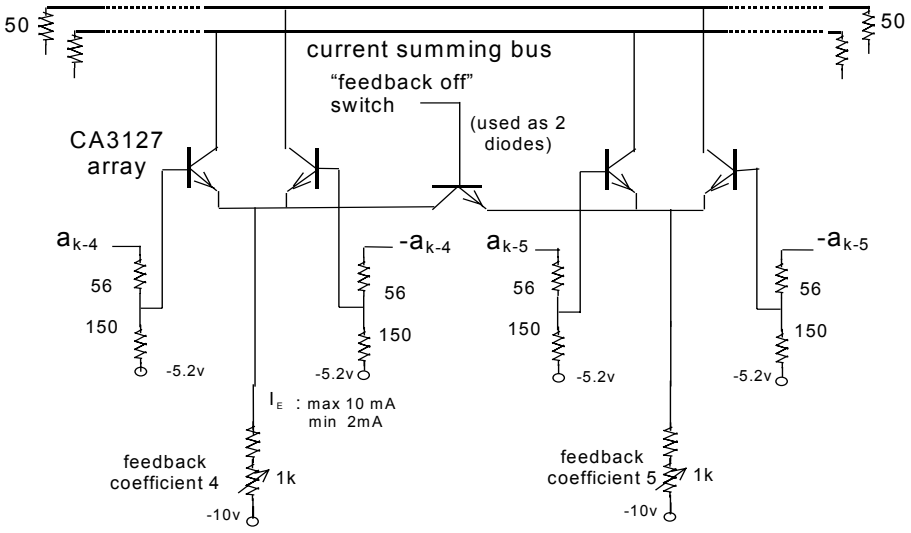


Fig. 6-3: Implementation of the feedback equalizer using current steering switches.

Fig. 6-3 shows the implementation of the feedback equalizer. The feedback equalizer is effectively a 10-tap filter, and is implemented by a 6-tap filter in tandem with an exponential decay circuit so as to reduce the implementation complexity. To ease the tight time constraint on the feedback loop, the forward equalizer is designed to force the first feedback tap to zero [7] [8]. The implementation circuit of the feedback equalizer employs a set of high frequency NPN transistor arrays, CA3127, as shown in Fig. 6-3, where each feedback filter tap is realized using a current steering switch. A CA3127 consists of five isolated general-purpose silicon

NPN transistors. These transistors are used in pairs as current steering switches (max. 10 mA.). The 1st feedback tap is zero, by design. The 2nd tap can be set to be either positive or negative. The 3rd to 7th taps can only be negative. The magnitudes of these taps are limited to half the minimum eye level at the slicer input. The remaining feedback taps are lumped into an exponential tail, which is implemented using a one-pole RC (resistor-capacitor) network [7]. The principle behind the implementation of the feedback equalizer as described above resembles the working mechanism of a set of dams. Feedback taps resemble the dam sizes, which are controlled by decision bits for damming up (via transistor array CA3127) the current on the current summing bus.

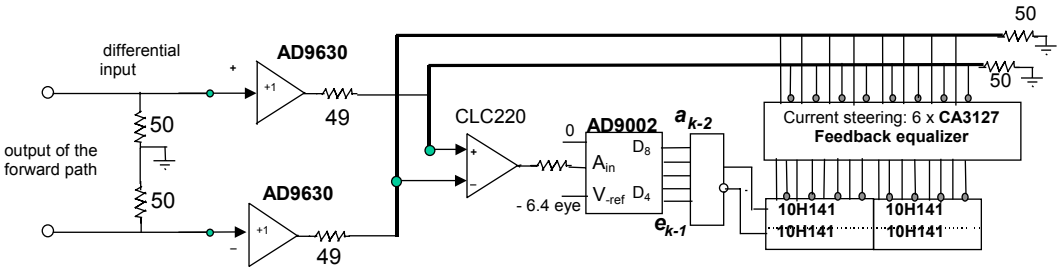


Fig. 6-4: Implementation of the critical loop.

The critical loop, which consists of the summing node, comparator (A/D) and decision feedback loop, is implemented as shown in Fig. 6-4. The input, which comes from the output of the forward path according to Fig. 6-2, is approximately 2.0 V_{pp} differential with 50-ohm terminations. The AD9630 is a 750 MHz unity-gain buffer capable of driving 50 mA at 3.5V. The outputs of the forward and feedback equalizers are summed on a low-impedance (50 ohms) differential bus for driving the comparator AD9002, which is an 8-bit high-speed A/D converter. Time constants at the bus are approximately 0.5 ns. At the input of the A/D, the MDFE eye levels are at approximately +/- 0.5V and +/- 1.0V (measured differentially). These are called the inner and outer eye levels, respectively. The six most significant bits of the A/D are used to digitize the input. The A/D and the feedback shift registers MC10H141 get the same clock, which is controlled by the VCO of the timing recovery board and is running at 150 MHz channel rate. The timing diagram of the MDFE critical loop is depicted in Fig. 6-5, along with the measured implementation delays of various signals, from the A/D via shift registers to the summing bus.

In debugging the MDFE boards, the forward and feedback equalizers are optimized separately. The forward equalizer is first adjusted to match the desired equalized bit response (observed at the forward equalizer output). Then the feedback equalizer is fine-tuned to optimize the system error rate. Fig. 6-6 shows the eye-pattern measured at user density 2.0 and 100 Mb/s user data rate. Observe that there are four distinct levels at the desired sampling instant shown by the marked block in the figure. System performance is mainly determined by the inner levels. The bumps and fuzzy traces in between the sampling instants are due to the settling of the feedback equalizer at the summing bus.

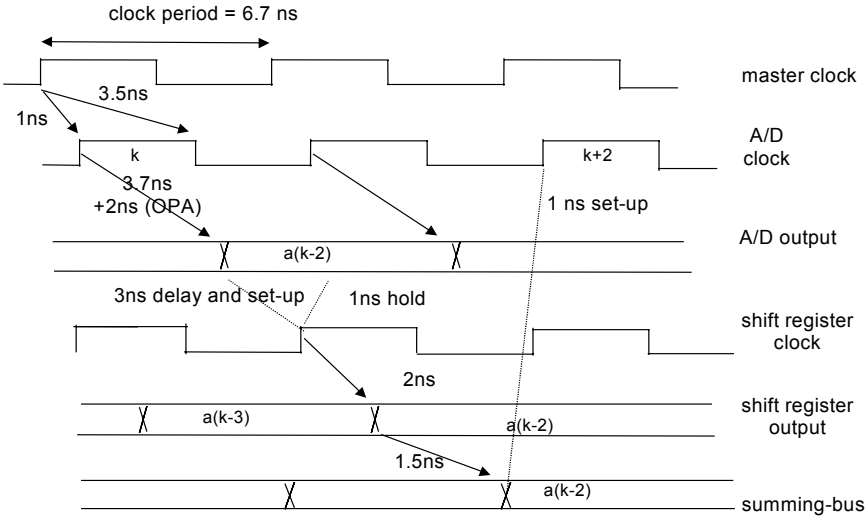


Fig. 6-5: MDFE critical-loop timing diagram.

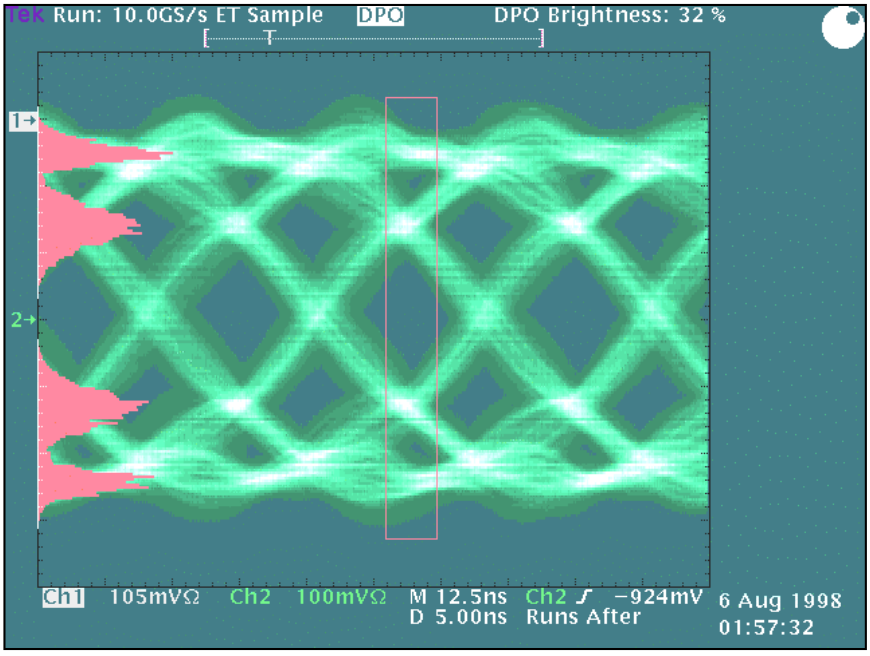


Fig. 6-6: Eye pattern measured at the analog summing bus showing the four levels at ideal sampling instants (the block marks the desired sampling instant).

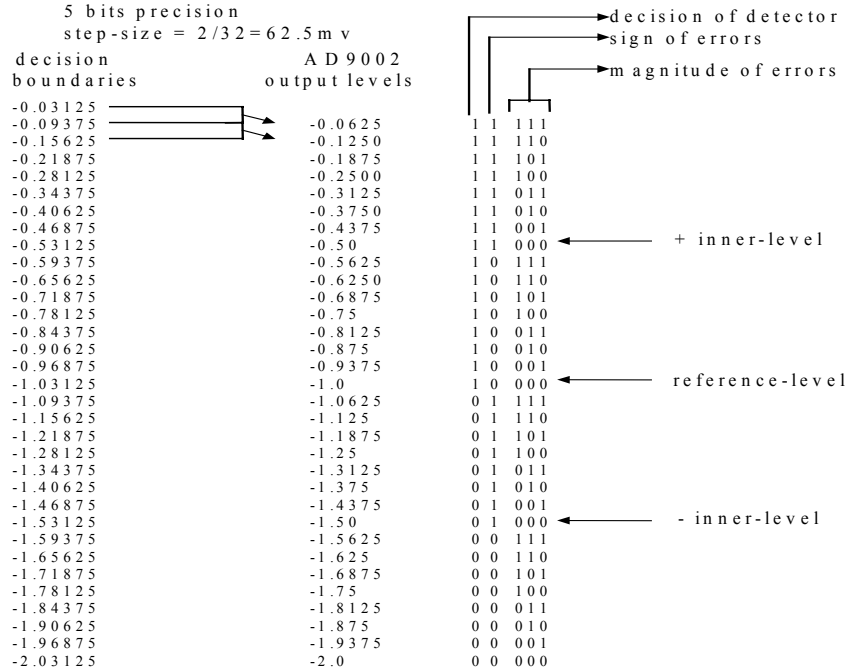


Fig. 6-7: Mapping of input to 5-bit output of the 8-bit AD9002 A/D converter and error pattern assignment.

For a 2.0 V_{pp} A/D input, both bit-error-rate (BER) simulations and experiments showed that a 5-bit A/D would suffice for our purpose, and no significant improvement can be obtained by using more bits. For this reason, the analog summing node output is digitized to 5-bit precision using the 5 most significant bits (MSBs) of the 8-bit AD9002. From these 5 bits, the most significant bit is used for the bit decision and the remaining 4 bits are used for generating the error signal for the timing recovery system. To illustrate this, we show in Fig. 6-7 the mapping of the A/D input to output for user density 2.5. The 2.0 V_{pp} input is mapped into 32 levels with a step-size 62.5 mV according to the 33 decision boundaries. Experiments show that the BER performance is sensitive to the A/D reference bias relative to the middle value of the input. Therefore, while debugging the circuits of this portion, the actual reference level is fine-tuned to have the best BER.

6.2 Implementation of MDFE Timing Recovery System

6.2.1 Data format used for MDFE timing recovery

The acquisition and tracking modes of timing recovery are associated with the use of a specific data format. The recommended data format for MDFE timing recovery is illustrated in Fig. 6-8. This format serves for timing acquisition, sync byte detection and clock tracking purposes.

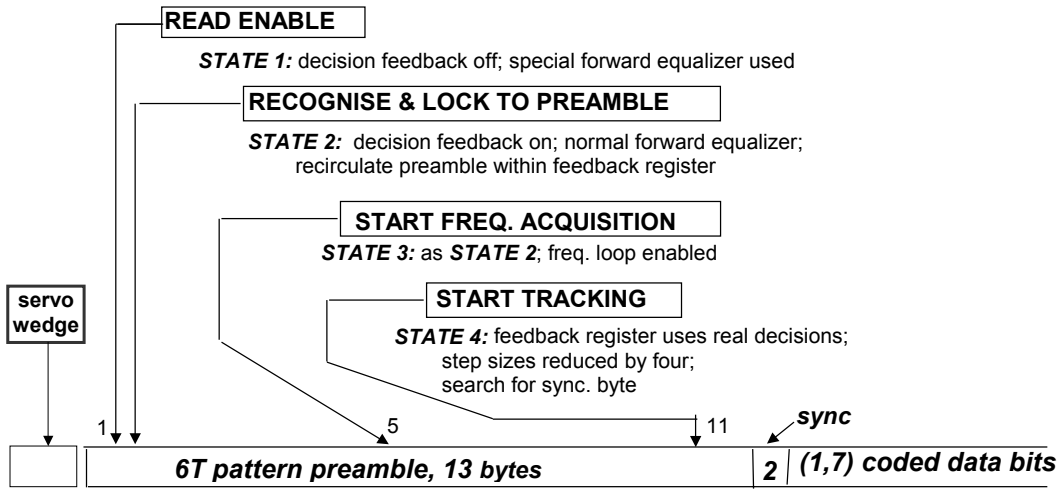


Fig. 6-8: Data format of one sector of magnetic disk for MDFE timing acquisition, sync byte detection and clock tracking.

In hard disk drives, servo wedge signals are embedded into sectors and are used to control the position of the read head in accordance with the track and sector specifications. The READ ENABLE signal is activated after the servo wedge signal. The timing acquisition scheme that is implemented in the MDFE prototype is the first scheme discussed in chapter 5 (see Section 5.2) which uses special forward equalizer coefficients and switches. As mentioned already, the preamble used for acquisition is the 6*T* (‘$++++---$’) pattern and has a length of 13 channel bytes (13×12=156 channel bits). The acquisition preamble allows the system to acquire the desired sampling phase and frequency before reading the user data. In the beginning (i.e., STATE 1), the decision feedback loop is switched off and special forward equalizer coefficients are used for acquiring the 6*T* pattern in the feedback register. When the feedback register is correctly loaded, as recognized by the lock-to-preamble circuit (in STATE 2), the feedback loop is switched on, the normal forward equalizer is used, and the preamble pattern is circulated in the feedback register. After 5 channel bytes have elapsed (in STATE 3), the frequency loop is enabled. After 11 channel bytes have elapsed, the PLL switches to the tracking mode (the loop step-sizes are scaled down by a factor of 4, circulation of the feedback register contents is stopped and actual decisions are applied) in STATE 4. The acquisition process is about to end. In order to identify the beginning of the user data, the sync byte must be detected correctly. In magnetic recording, a short preamble is desirable to leave more storage area for the user data. In MDFE, the total acquisition preamble length is 15 channel bytes (180 channel bits) inclusive of 2 sync bytes.

6.2.2 Implementation of timing recovery loop

A. The overall timing recovery loop

In MDFE, the timing, gain and DC loops are updated simultaneously. Recall from Chapter 4 (see eq. (4.29)) that the timing-error detector (TED) output is given by $\chi_k = e_k \hat{a}_{k+1}$ if $\hat{a}_{k+1} \neq \hat{a}_{k-1}$, where $e_k = y_k - \hat{a}_k$ and $\hat{a}_k$ is the decision corresponding to y_k. This indicates that only samples associated with transitions in the input data are used for timing recovery [9].

Fig. 6-9 shows the schematic of the overall timing loop and the use of the A/D output for generation of the error signal. Because of a 1-bit delay introduced by the A/D, the A/D output at the instant *k* corresponds to the input y_{k-1}. As mentioned already, the input y_k is transformed by the A/D AD9002 into a 5-bit digital output. The most significant bit gives the bit decision $\hat{a}_{k-1}$ and the remaining 4 bits, i.e., $e^3_{k-1}, e^2_{k-1}, e^1_{k-1}$ and e^0_{k-1}, give the error between y_k and $\hat{a}_{k-1}$. Among these four bits, e^3_{k-1} gives the sign of e_{k-1} and the remaining three bits give the magnitude of e_{k-1}.

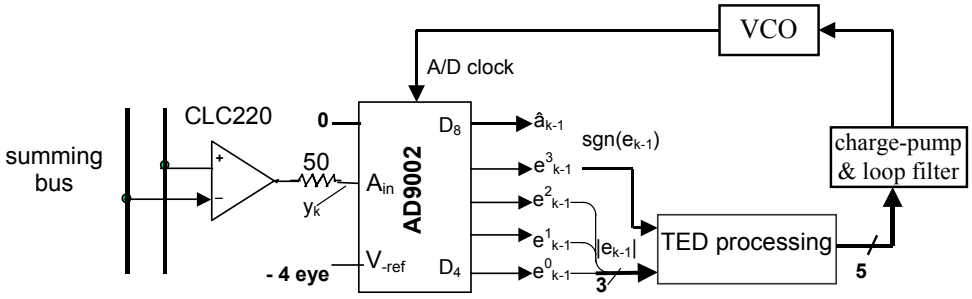


Fig. 6-9: Block schematic of the overall timing loop which uses the A/D output for generating the error signal for TED.

B. Generation of error signals for TED

The circuit for generating the digital error signals required for implementing the TED is shown in Fig. 6-10. The feedback register input α_{k-1} may be different from the decision bit $\hat{a}_{k-1}$. For example, in the beginning of acquisition, the register input α_{k-1} is updated by circulating the register contents. A large error e_{k-1} occurs whenever $\hat{a}_{k-1} \neq \alpha_{k-1}$. In this situation, the TED circuit outputs $\mathrm{sgn}(e_{k-3}) = \hat{a}_{k-1}$ and $|\overline{e_{k-3}}| = 0$, with which the subsequent charge-pump and loop filter circuits yield a maximum current output. Note that the input e_{k-1} and the output e_{k-3} are both 4-bit patterns but the input e_{k-1} represents the error $e_{k-1} = y_k - \hat{a}_{k-1}$ whiles the output e_{k-3} represents the 2-bit delayed version of $\chi_k = 0.5e_{k-1}(\hat{a}_k - \hat{a}_{k-2})$. Therefore, we can view the output e_{k-3} as a 4-bit digitized TED output. The TED output, which is activated by the condition $\overline{\alpha_{k-2} \neq \alpha_{k-4}}$, drives the subsequent charge-pump circuit whose analog output is used for controlling a voltage-controlled oscillator (VCO). When the slicer output is connected to the feedback register input, as in the case of the later stage of acquisition mode and the case of tracking mode, the condition $\overline{\alpha_{k-2} \neq \alpha_{k-4}}$ becomes $\overline{\hat{a}_{k-2} \neq \hat{a}_{k-4}}$. For maximum speed, emitter-coupled logic (ECL) components are used in the circuit of Fig. 6-10. The MC10H176 contains 6 master-slave type-D flip-flops and has much smaller propagation delay with no increase in power-supply current compared to the standard MECL 10K family. It is triggered by the same clock used for the A/D IC. The MC10H107 is a triple 2-input exclusive OR/NOR gate. MC10H104 is a quad 2-input AND gate. All these ECL components typically have 1 ns propagation delay, and are thus suitable for clock rates up to 150 MHz.

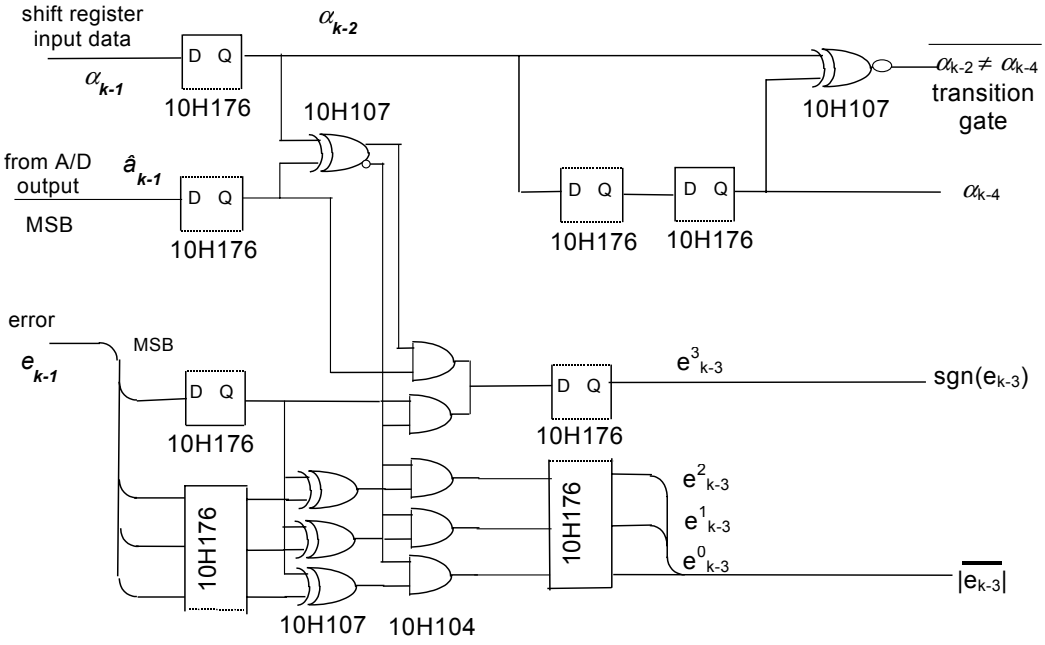


Fig. 6-10: Digital error generation for TED implementation.

C. Implementation of the charge-pump and loop filter

The digital error signals are converted into analog quantities via the charge-pump circuit as shown in Fig. 6-11 with a RC loop filter. The loop filter output is applied to a VCO with a free-running frequency of 150 MHz. Charge-pump circuits are widely used in PLL applications [10, 11].

There are three similar circuits as in Fig. 6-11 for the timing, gain and DC loops. The implementation of digital TED as shown in Fig. 6-11 becomes rather simple since it does not involve high-speed multiplier. The charge-pump circuit acts as a D/A converter. It is realized by the component OPA2662, which is a versatile driver with high bandwidth (370MHz). The OPA2662 transforms digital errors into analog currents in positive (for charge action) and negative (for pump action) values at its output. It has two parallel voltage-controlled current gates and yields zero output for zero differential input. The loop filter is realized by a RC circuit and the values of the resistor and capacitor determine the time constant and bandwidth of the loop. During acquisition, the upper and lower voltage-controlled current gates of the OPA2662 are both enabled, thus producing a large loop gain. During tracking, a small loop gain is desired in order to decrease jitter in the timing loop, and hence the upper gate of the OPA2662 is disabled via the 'gain switching' signal. In practice, an extra current compensation circuit is used (not shown in Fig. 6-11) at both sides of the OPA2662. This compensation is meant to improve the accuracy of the charge-pump circuit with zero output for zero differential input.

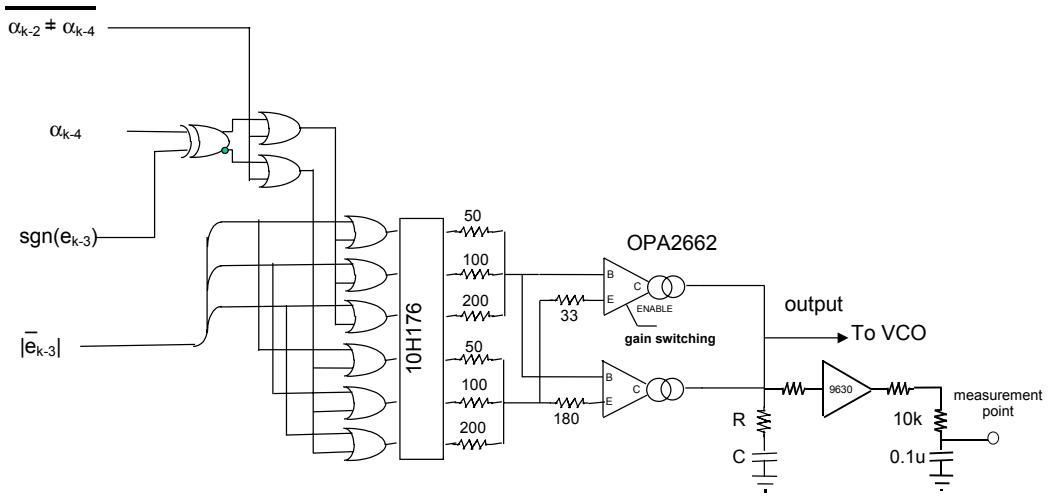
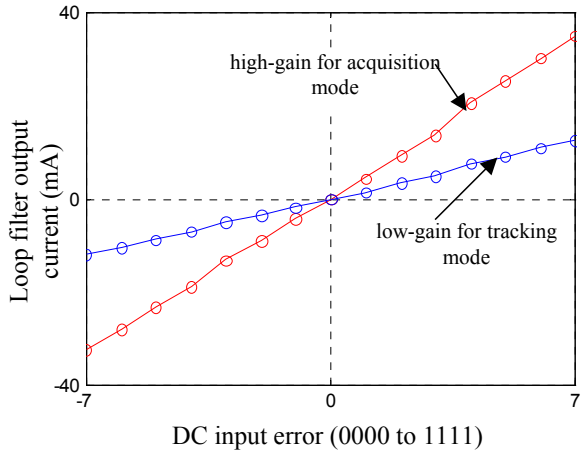


Fig. 6-11: Circuit for implementing the charge-pump and loop filter.

The measured static transfer function of the circuit according to Fig. 6-11 for deterministic input error patterns is shown in Fig. 6-12(a). This can be interpreted as the timing function since the input patterns of the digital TED represent timing errors and the output of the loop filter represents an average of the TED output. The table on the right-hand side shows the mapping from the input pattern to the equivalent timing-error output. The integers in the second column of the table in Fig. 6-12(b) represent 15 error levels arising from the negative-most to positive-most digitized timing errors that the TED detects. An arbitrary waveform generator (AWG) is used to produce a pseudo-random pattern as the input. The corresponding output current of the loop filter is measured and its result versus the averaged input error is shown in Fig. 6-13. The averaged input error is obtained by averaging the 4-bit e_k input waveforms over one period of the pseudo-random input pattern. For example, if the period of the pseudo-random input pattern is 15 bits, and we obtain 15 timing errors as {3, 5, 2, 6, -4, 4, 2, -7, 0, -5, 1, -3, 5, -2, -3} in one period, then the average input error is approximately 2.66. The transfer functions shown in Figs. 6-12 and 6-13 illustrate that the TED implemented here results in a timing function that has good linearity with zero output for zero input.

To analytically examine the TED performance, we did a modeling of the circuits that implement the TED, charge-pump and loop filter. Using this, we evaluated the timing function for high gain conditions. The result is shown in Fig. 6-14 along with the corresponding measurement result from Fig. 6-12. Observe that the actual circuit behavior (i.e., the measured result) agrees well with expectations (i.e., the computation result). The small difference in the slope may be attributed to the use of extra current compensation at the OPA2662 output, which is difficult to take into account when modeling the circuit.

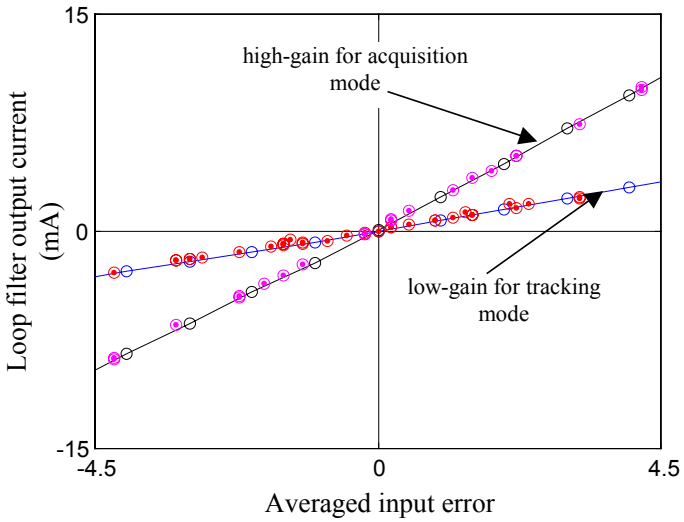


TED input pattern				timing error index
1	1	1	1	7
1	1	1	0	6
1	1	0	1	5
1	1	0	0	4
1	0	1	1	3
1	0	1	0	2
1	0	0	1	1
1	0	0	0	0
0	1	1	1	0
0	1	1	0	-1
0	1	0	1	-2
0	1	0	0	-3
0	0	1	1	-4
0	0	1	0	-5
0	0	0	1	-6
0	0	0	0	-7

$\mathrm{sgn}(e_k)$ $|e_k|$

(a) (b)

Fig. 6-12: (a) Measured static transfer function from the digital TED input to the output of the loop filter for DC input; (b) Table that shows the relation between the input patterns and timing errors.



(solid lines: measurement for the DC input; dotted circles: measurement for the pseudo-random input.)

Fig. 6-13: Measured transfer function from the input of the digital TED to the output of the loop filter for pseudo-random input.

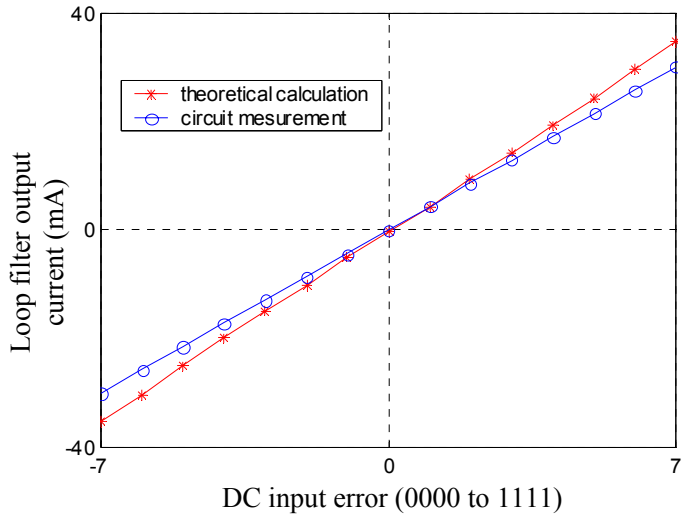


Fig. 6-14: Comparison of measured and calculated transfer functions from TED input to the loop filter output under high-gain conditions.

6.2.3 Lock-to-preamble and sync byte detection circuits

As discussed in Chapter 5 (see Section 5.2), to avoid the potential false lock problem arising from wrong decisions in the feedback register, the 6*T* preamble pattern must be preloaded. This task is to be accomplished by the lock-to-preamble circuit, as shown in Fig. 6-15, in less than 15 to 20 channel bits. The MC10H141 is a four-bit universal shift register without external gating. Two MC10H141 circuits receive decisions and complementary bits from the A/D, and pass them to the lower part of the logic gates to discriminate the 6*T* pattern. When the lock-to-preamble circuit detects the 6*T* pattern, it produces a 'preamble lock' signal. At the same time, the 'feedback on' signal for connecting the feedback equalizer output to the summer input and the '$f_c/6$' signal (i.e., the A/D clock ($f_c=1/T$) is divided by 6) for the sync byte detection circuit are activated. The timing diagram of the lock-to-preamble circuit is shown in Fig. 6-16.

The '$\overline{\text{read enable}}$' signal starts the process for reading the preamble. It activates the lower part of the logic gate array to detect the presence of a 6*T* pattern in the shift register. When it is confirmed that the 6*T* pattern is present, then the 'preamble lock', 'feedback on' and 'load S2' signals respond accordingly. At this stage, the feedback filter is connected to the summing node and the shift register is circulating so that wrong decisions have no effect on the feedback register. At the same time, a valid $f_c/6$ clock is available and the timing loop is settling to the desired phase. Near the end of the acquisition process, the '$\overline{\text{sync enable}}$', which is generated by a sequencing counter, activates the tracking mode, decision bits are used to update the shift register, and the sync byte detection circuit is engaged to start the procedure for detecting the sync byte.

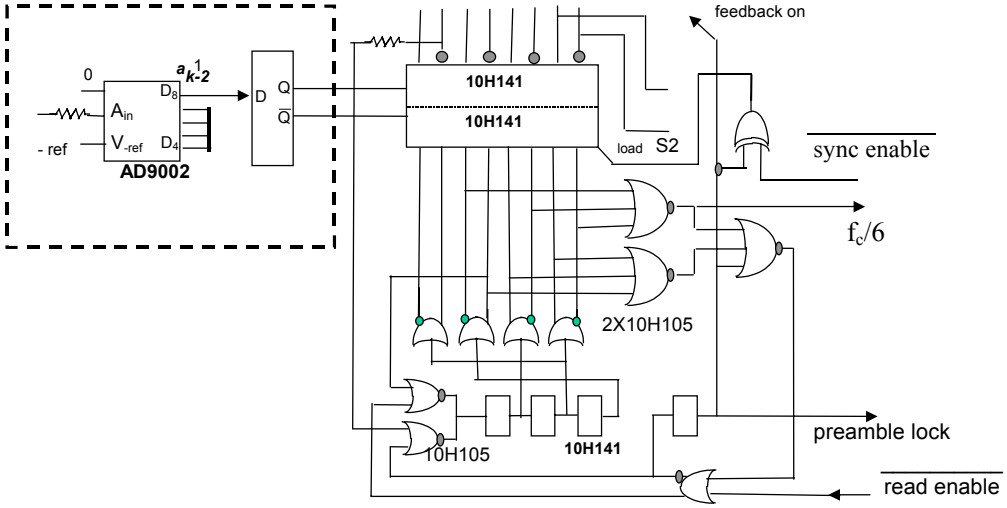


Fig. 6-15: Lock-to-preamble circuit for preloading the 6*T* pattern.

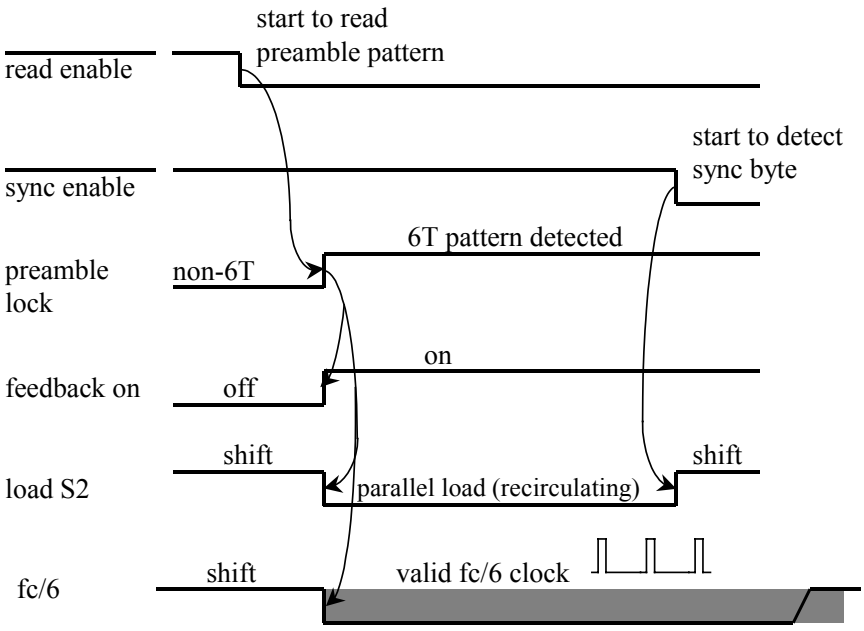


Fig. 6-16: Timing diagram of the lock-to-preamble circuit.

The purpose of the sync byte is to demarcate the start of the user data. A false or missed detection of the sync byte will necessitate a rereading the sector, and this increases average access time. Several patents are filed on error-tolerant sync byte recovery methods [12-14], but most of them have high complexity. The general method for detecting the sync byte is using correlation techniques. That is, the sync byte is designed such that it has minimum cross-correlation with preamble and user data while exhibiting a distinct autocorrelation. The sync

byte used in the MDFE read channel has 2 user bytes. The recommended sync byte in the NRZ form is '6-down 6-up 9-down 3-up' ('down' and 'up' refer to '-1' and '+1', respectively). This byte is chosen to have high autocorrelation and minimum probability of confusion with both preamble pattern and the *(1,7)* coded data. Fig. 6-17 shows the sync byte detection circuit. The sync word is preceded by the 6*T* preamble and followed by the user data. The 24-bit sync byte is detected by computing the cross-correlation of the contents of shift registers 10H141 and the specific 8-bit setting (i.e., 01100001)[1] for the connection to the input of 10H116, a line receiver. These 8 bits (01100001) are the detection result of the 24-bit sync byte in the shift registers 10H141s. When the input data stream passes through the circuit, only the segment that contains the correct sync byte can make the 10H116 produce the 'sync' pulse.

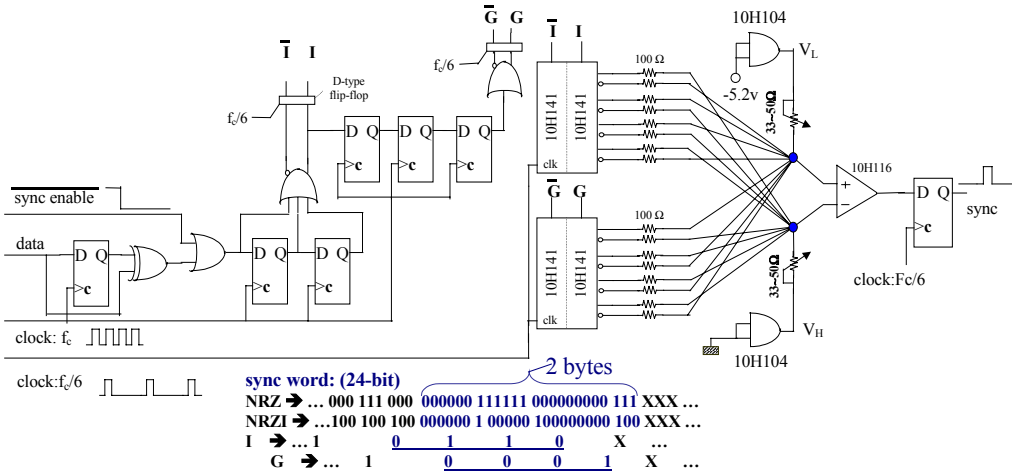


Fig. 6-17: Sync byte detection circuit.

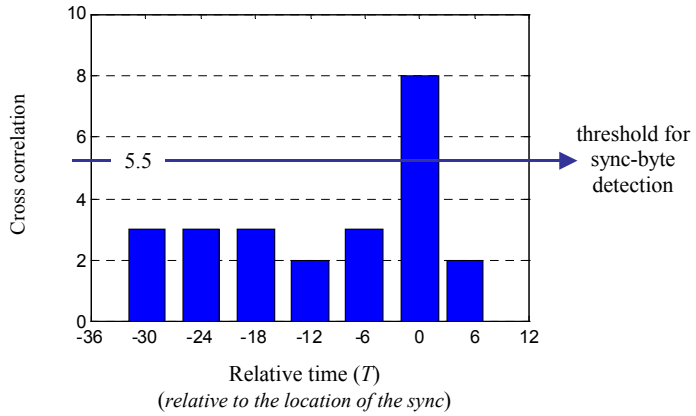


Fig. 6-18: Cross-correlation of the data in the shift-registers and the word '01100001'.

[1] Setting the connection between the output of 10H141 and the input of 10H116 to match this 8-bit pattern, makes the cross-correlation of the content in shift registers and the connection pattern (i.e., 01100001) to the input 10H116 to be maximum, which is 8 for the sync byte in the detection circuit.

The resisters at the MC10H116 input are tuned in order to achieve a certain threshold for triggering the sync byte flag. The threshold is set to be 5½, to make the detection circuit tolerant to 2 bit errors in the sync byte. The sync byte is said to be detected when the cross-correlation of data in the shift registers with the 8-bit pattern connecting to the input of MC10H116 is greater than or equal to 6. Fig. 6-18 illustrates the cross-correlation versus relative time in a time step of 6*T*. The cross-correlation has an ideal value of 8 at the end of the sync byte word, and has value of 3 or less otherwise.

By way of illustration, we show in Fig. 6-19 the measured result obtained from the circuit according to Fig. 6-17. The circuit output is normally 'low' when the sync byte has not been detected. After the sync byte has been detected, the circuit produces an output 'high' and remains 'high' for 6 bits before it goes to 'low'. This 6-bit width pulse is recognized as the sync byte flag, which marks the start of the user data zone.

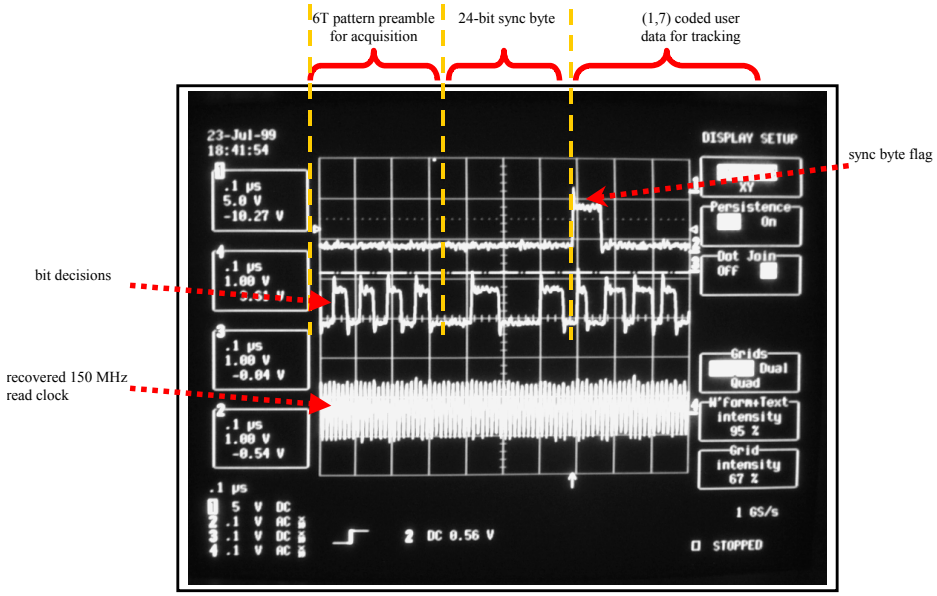


Fig. 6-19: Measured waveforms from the sync byte detection circuit.

6.3 Evaluation of MDFE Prototype

The critical loop board, which consists of the summing node, the feedback equalizer and the A/D AD9002, constitutes one of the most important modules of the MDFE prototype. To evaluate how well the critical loop works, we measured the BER performance with both the forward equalizer (i.e., the bi-quad board) and timing loop (i.e., the timing recovery board) off. The test setup is shown in Fig. 6-20. The user density for the measurement is 2.5, and the data rate is 100 Mbits/s.

Fig. 6-21 illustrates the measured and the calculated values of the BER versus the detection SNR. The detection SNR is defined as the ratio of the square of inner-eye opening to the power

of noise and residual ISI at the input to the A/D. We use the detection SNR measure because there is no forward equalizer here. At BER=10^{-6}, the critical loop operates with about 0.3 dB degradation from the theory. This loss may be due to hardware non-idealities at high data rates, for example, the feedback equalizer in hardware may not be ideal and the A/D resolution in hardware may not be accurately taken into account. That is, since the forward equalizer and timing are ideal, the loss may arise due to the fact that the detection is computed for the ideal loop whereas the experimental loop suffers from A/D resolution and inaccurate implementation of feedback taps.

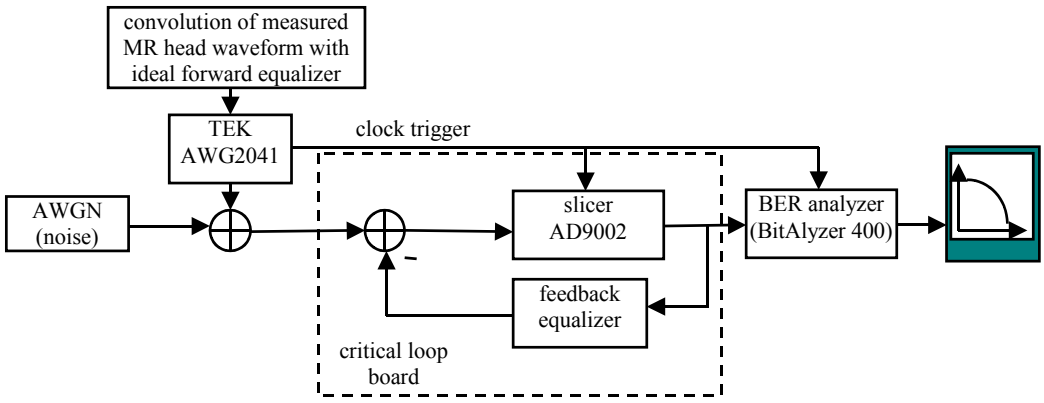


Fig. 6-20: Bench test setup for measuring the BER performance of the critical loop board (the portion in the dashed block) of the MDFE prototype.

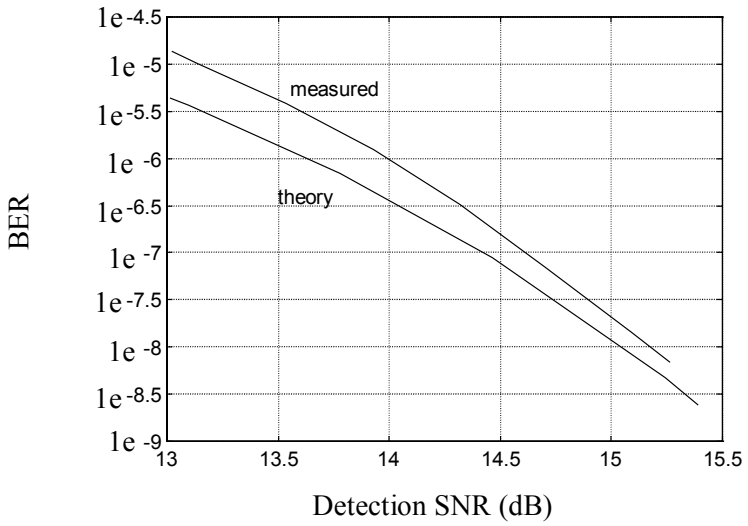


Fig. 6-21: Measured and theoretical BER performance of the critical loop board.

To thoroughly evaluate the MDFE prototype in real time, we tested it on spinstand in the clean room. The measurement involves the forward equalizer (the bi-quads module), critical loop, timing recovery and gain control modules. The replay waveform from a spinstand is used

as the input to the prototype. The measured BER performance corresponds to about 1 dB loss in SNR with respect to the theoretical performance computed for ideal implementation of the forward/feedback filters and timing/gain loops. This can be due to many factors, such as non-idealities of the equalizers and timing/gain recovery circuits, off track distortion of the MR head on the spinstand, and input waveform jitters. We also measured the error propagation performance. Error propagation can be characterized in terms of an "error burst distribution", i.e. the probability distribution of error bursts against the burst length. We measured the error propagation characteristics of the MDFE prototype using the BitAlyzer400. The result, which is shown in Fig. 6-22, shows that error propagation is a serious concern because burst errors extend to above 30 bits[2]. This issue is investigated in [15] [16] and some methods for minimizing error propagation in MDFE are suggested in [17] [18]. The measured performance shown in Fig. 6-22 is comparable to that obtained from simulations [19].

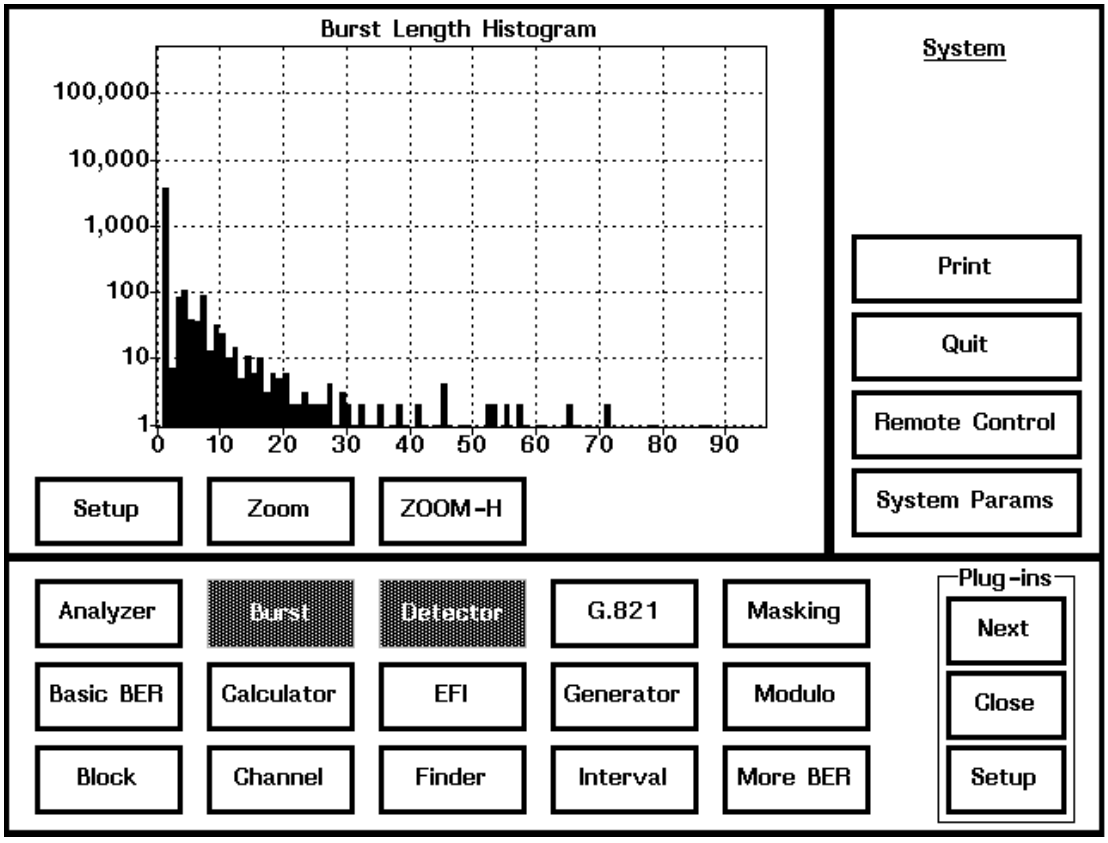


Fig. 6-22: Histogram of MDFE burst errors measured using BitAlyzer400.

[2] The longer the error bursts, the more powerful should be the ECC (error control code) that is required to correct these error bursts. This translates to poor coding efficiency and complex ECC decoding circuits.

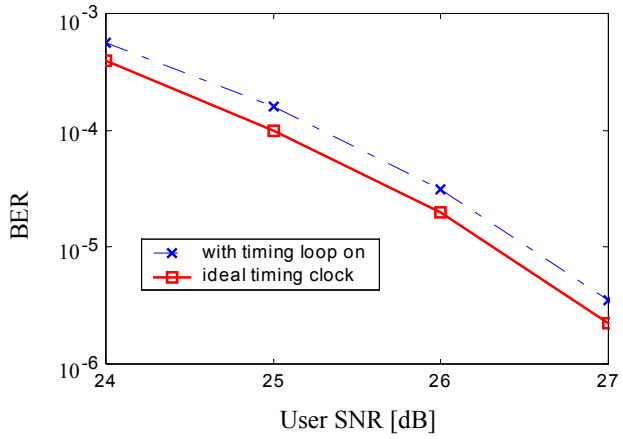


Fig. 6-23: Measurement of the BER performance of the MDFE board at user density of 2.5, with and without active timing recovery loop.

To evaluate the timing recovery performance of the MDFE prototype, we measured the BER curves by using the ideal clock and the recovered clock, respectively. With ideal clock, the circuit boards are triggered by the clock from an arbitrary waveform generator (AWG), which is also used to produce input data to the MDFE board. When using the recovered clock, the timing recovery system is active and provides the clock for all parts of the MDFE board. Measurement results for both situations are shown in Fig. 6-23. Comparison reveals that the timing recovery loop causes about 0.2 dB SNR loss at user density 2.5. Since the timing recovery circuits are implemented using discrete-components, such a loss is reasonable. We found that the recovered clock is very susceptible to external factors such as layout of the circuits, choice of decoupling of the power and signal tracks, termination of ECL outputs, and testing cables for probing the signals. For this reason, an integrated solution is expected to work better.

For the recovered timing clock of the MDFE prototype, we also measured the residual phase jitter using the approach in [20]. The measurement system is depicted in Fig. 6-24. The $6T$ (‘$++++----$’) pattern is written on the media so that the replay waveform from the spinstand MR head is essentially a sine wave. This waveform is used to drive the prototype via the Tektronix AWG2041 and MicroNetics Mx5108 programmable noise generator. The prototype is triggered by the clock provided by the timing recovery circuit. The Tektronix TDS784D DPO (Digital Phosphor Oscilloscope) is used to acquire and store the input samples y_n to the slicer. In software they are then reconstructed to an analog waveform $y(t)$ through the method of interpolation (ITP). Then, the zero-crossing detection (ZCD) technique is applied to estimate the sampling phase ϕ_k in the measured waveform. In another path, we use the same data $\{a_k\}$ to drive an MDFE jitter model that characterizes the deterministic jitter components. The output of the model is a phase estimate $\tilde{\phi}_k$. The LMS adaptation algorithm based on the estimated residual jitter $\Delta_k = \phi_k - \tilde{\phi}_k$ is used in turn to adjust the coefficients of MDFE jitter model. This method is described in more detail in [20]. The result of the estimated random jitter Δ_k shows that the timing loop has about 1.8% RMS random jitter at user density 2.5 and SNR 27 dB. This jitter is found to cause about 0.2 dB SNR loss and is reasonable for the circuits based on discrete-components.

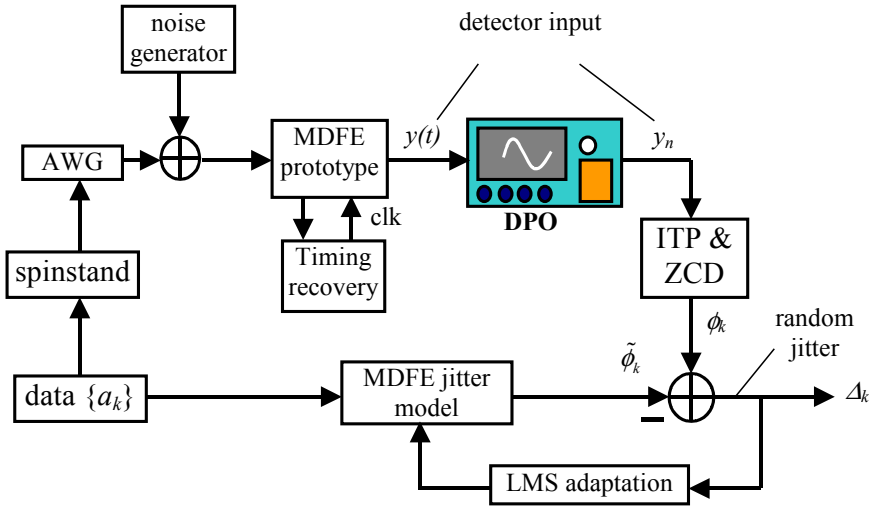


Fig. 6-24: Test setup for measuring random jitter in the recovered clock of the MDFE prototype.

6.4 Considerations of Hardware Implementation

As described in Section 6.2, the timing recovery system of the MDFE prototype operates at a speed of 150 MHz and is realized using ECL (Emitter-Coupled Logic) circuits. ECL is regarded as one of the fastest forms of digital logic. It offers both the logic speed and the logic features to meet the demands for the MDFE timing recovery circuitry. To achieve the high speed of 150 MHz, several important points must be considered.

First, time-delay through interconnect-wiring, which may be ignored in low-speed systems, becomes highly important [21]. We use short wires and provide parallel functional tracks with equal effective wire lengths as far as possible during layout. Second, waveform distortions due to line reflections also become troublesome at high data rates. Improperly terminated lines can result in reflections that may cause false triggering. The usual solution, as applied in RF (Radio Frequency) technology [22], is to employ transmission-line practices and properly terminate each line/wire with its characteristic impedance. For ECL circuits, their low-impedance and emitter-follower outputs facilitate transmission-line practices without seriously affecting voltage levels. Third, the possibility of cross talk between adjacent signal lines is proportionately increased in high-speed circuits. This is the result of very steep leading and trailing edges of the high-speed signal. These steep edges are rich in harmonics that couple readily to adjacent circuits. The Motorola ECL series that we used to design the MDFE timing circuits have specially reduced rise and fall times, this reduces cross talk without compromising other important parameters. Finally, precautions must be taken on electrical noise generation and pick-up in the circuits because these are very detrimental at high speeds. In general, these considerations are speed and frequency dependent.

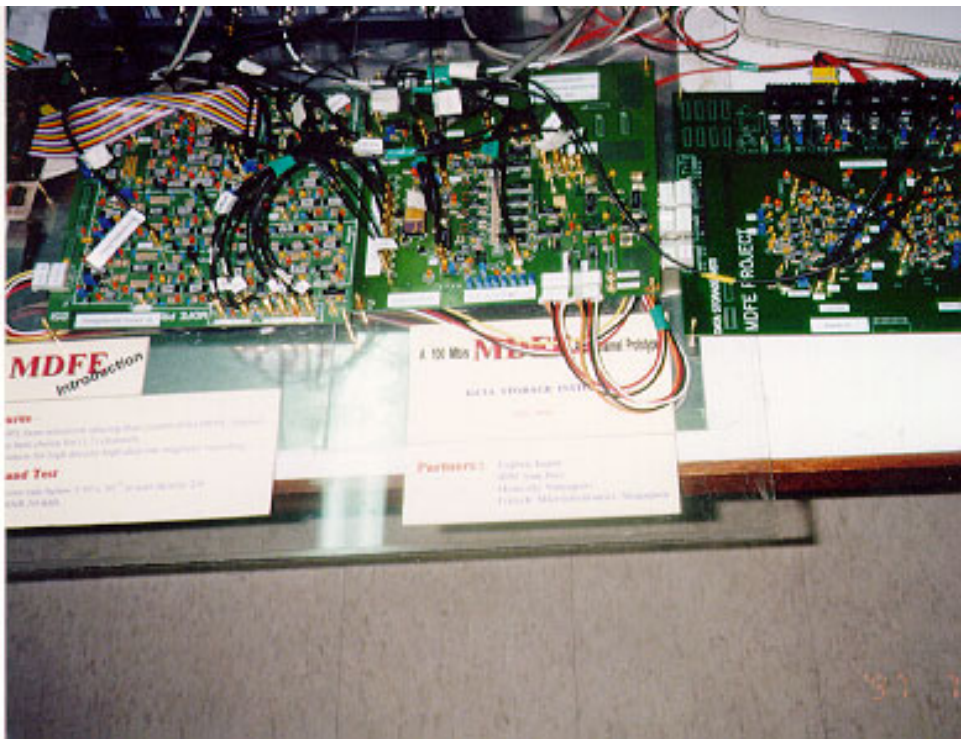


Fig. 6-25: MDFE prototype circuits and timing board.

For the MDFE timing circuit board, we designed a six-layer PCB (Printed Circuit Board) containing signal lines, terminated power, power supply and ground. Each ECL line is kept as short as possible and, at the same time, well decoupled by capacitors and shielded by the ground layer on the opposite side of the board. Interconnections of signals and the clock with other functional boards are accomplished via coaxial lines whose lengths and corresponding propagation delays have been carefully selected. Fig. 6-25 illustrates the finished timing board, and it works well for the MDFE prototype.

6.5 Conclusions

A 100 Mb/s experimental MDFE read channel was designed and prototyped using discrete-components. The MDFE timing recovery system was described, its implementation issues were investigated, and the performance was measured. The timing recovery board works well at high data rate to support a robust MDFE prototype. The measurement results show that the circuit performance is close to the expected result. The implementation is simple and reliable, and can be easily realized by an integrated solution.

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CHAPTER 7

ASYNCHRONOUS EQUALIZER ADAPTATION AND INTERPOLATIVE TIMING RECOVERY FOR A DIGITAL OPTICAL RECORDING SYSTEM

7.1 Introduction

As technology allows ever more complex functions to be implemented, digital signal processing techniques play an increasingly important role in storage systems. Good evidence is the use of sample rate conversion (SRC) and interpolative timing recovery (ITR) for replacing the conventional voltage-controlled oscillator (VCO) based timing recovery in digital recording systems [4] [5] [6] [27] [28]. The use of SRC and ITR enables a low-complexity method for using a free-running clock to sample the replay signal and permits 100% digital equalization and timing recovery. Fully digital ITR has advantages of lower cost and higher stability. State-of-the-art digital integrated circuit (IC) technology sustains digital design with greater designer productivity and much easier, more reliable system design verification as compared to analog and mixed analog/digital designs. To utilize these advantages, we develop a new asynchronous equalizer adaptation structure with fully digital ITR. The structure is generic, attractive, and widely applicable. Its development is illustrated for a digital optical recording system according to the proposed digital video recording (DVR) standard [1] [2].

The conventional approach for asynchronous equalizer adaptation uses the Least-Mean-Square (LMS) algorithm. This approach has to involve a mechanism of compensation for latency of gradient computation and an inverse sample-rate converter for synchronous-to-asynchronous conversion. This translates to a considerable implementation complexity. To avoid this, a new structure, called latch-based structure, is proposed to replace the LMS algorithm by a zero-forcing (ZF) algorithm and the inverse sample-rate converter by a simple latch. This structure does not have to compensate for latency and has no need to use an inverse sample-rate converter; thus, it provides an extremely simple solution for implementation. Study

and simulations indicate that this structure can work as well as an inverse sample-rate converter based structure.

This chapter is organized as follows. In Section 7.2, we review interpolation techniques and ITR applications. We discuss the architectures of asynchronously sampled systems and the advantages of using ITR in DVR applications in Section 7.3. In Section 7.4, we investigate equalizer adaptation algorithms and develop a new latch-based adaptation structure with ITR. We apply this new structure for investigating the asynchronously sampled read channel for the DVR system in Section 7.5. Section 7.6 studies the sample-rate converter and ITR, and investigates their realizations. In Section 7.7, we simulate the DVR system and evaluate the asynchronous equalizer adaptation and ITR loops for various sampling rates and conditions. Summary and further discussions are provided in Section 7.8.

7.2 Overview of Interpolation Techniques

This section reviews interpolation techniques, which are key to ITR systems. In asynchronously sampled recording systems, the sampling device operates on the replay signal at a fixed sampling rate. The sampling clock is not necessarily synchronized to the incoming data. The subsequent digital function must be accomplished in an asynchronous manner with respect to the data rate, and the interpolative timing recovery has to employ a sample-rate converter to convert the asynchronous samples to synchronous samples. A timing error signal is extracted based on these synchronous samples.

The ITR technique has long since been used in optical recording. The first publication on the application of ITR dates back to 1992 [3] for compact disc (CD) players, well before the applications of ITR in magnetic recording [4] [5] [6]. The approach of using an interpolation technique with a free running clock for various receiver applications has recently been appearing in the literature [22] [7] [8] [9] [10] [11] [12]. At the heart of this approach is the SRC technique. The SRC is the task of converting the sample rate of a digital signal to another sample rate while a certain amount of information, usually in a limited frequency band, must be preserved. Sampling-rate conversion is realized conceptually by first reconstructing the analog version of the input digital signal, and then re-sampling it at a different sampling rate. In practice, the task of SRC is usually accomplished by using an interpolation filter.

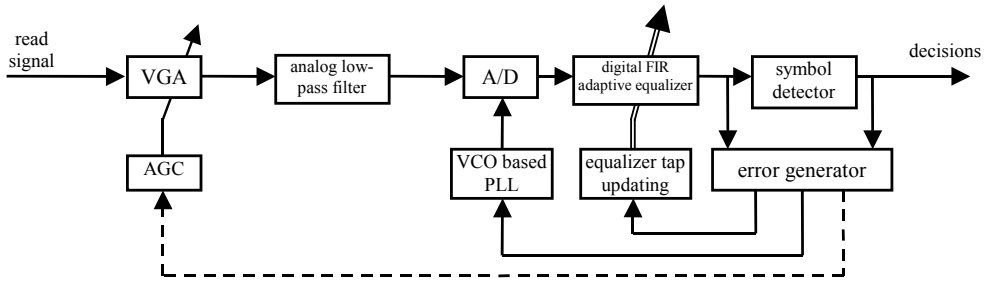
The design of interpolation filters is normally based on continuous-time functions such as the *sinc* function [13] [14] [15] or polynomials [16] [17] [30] [18] [19]. Such designs are generally not optimal in the sense of minimizing the mean-square error (MSE) at the input of the detector. There are several articles on the design of optimal interpolation filters for SRC in the context of multi-rate digital signal processing techniques [20] [21] [22], but they seldom consider noise. There are several papers investigating the design of optimal interpolation filters for symbol-rate ITR [23] [26] [27], but most of them do not present cost effective solutions that can be easily implemented.

Feasibility of implementation of interpolation filters is always an issue, and it is of much practical interest to look into how an interpolator can be designed and implemented. Since the interpolation filter applied here serves to realize the SRC task, it works as a temporal interpolation filter. This means that such filters can have time-varying coefficients, depending on a time-varying phase variable. A direct approach to design such filters is to quantize these phase variables and load appropriate filter coefficients from a predetermined table for each phase. In this approach, the filter coefficients can be designed ahead of time, for example, by

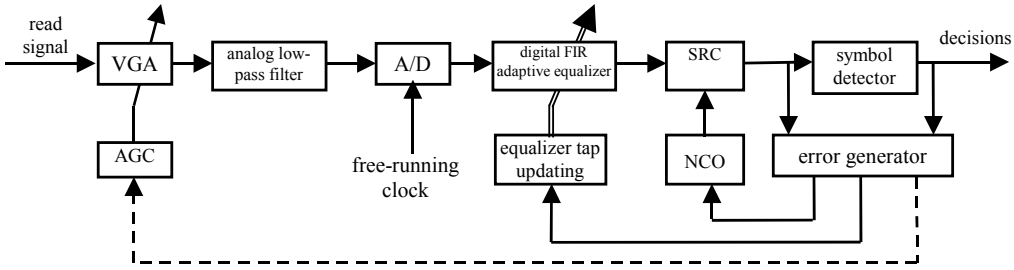
using the LMS algorithm. An alternative approach is to approximate the dependence of the coefficients on phase by a polynomial. This leads to the Farrow structure [16]. Another approach is to treat the asynchronous samples as having timing phase errors and to reconstruct the synchronous samples using a time-varying amplitude error predictor [24]. This approach is simple for the PR-IV scheme that has few decision levels. For high order PR schemes that have more decision levels, this approach is complicated and not efficient.

7.3 Advantages of using ITR for DVR

Applications of ITR for magnetic recording are described in [5] [6] [25] [26] [27] [28] [4]. In these papers, the sampling device invariably operates with an asynchronous free-running clock at a sampling rate above the data rate. This makes sense because the maximum frequency of magnetic recording channels is normally higher than the Nyquist frequency, viz. the half of the data rate. For DVR channels, however, the maximum frequency can be well below the Nyquist frequency. This implies that the sampling device in the read channel, which is usually an analog-to-digital (A/D) converter, may possibly operate in an asynchronous manner at an undersampling rate without causing information loss. The use of undersampling can significantly reduce the sampling rate of the two most important devices, the A/D converter and the equalizer, thereby considerably lowering the complexity and cost of the system.



(a) A conventional synchronously sampled read channel



(b) An asynchronously sampled read channel

Fig. 7-1: Synchronously sampled versus asynchronously sampled read channels.

By way of illustration and comparison, we show in Fig. 7-1 the block schematics of conventional synchronously sampled and asynchronously sampled read channels.

Observe that in conventional synchronously sampled read channels (see Fig. 7-1(a)), the AGC, equalizer adaptation and timing recovery form three nested loops. Here, the A/D converter and the equalizer form part of the timing-recovery loop, and add to the timing loop latency. This latency is unavoidable and can influence the timing loop stability. Because of this concern, the length of the FIR equalizer usually has to be limited in order to mitigate the equalizer latency that contributes to the timing loop. Furthermore, the A/D converter is required to operate synchronously with respect to the data rate. When the channel rate becomes high, a high-speed A/D converter has to be employed, which makes the system expensive. The advantage of this structure is that all the digital signal-processing blocks in the receiver operate with the same clock once the clock is acquired and tracked; thus, no sample-rate converter is needed.

Unlike Fig. 7-1(a), the asynchronously sampled read channel uses interpolation techniques (see Fig. 7-1(b)). The A/D converter samples the replay signal using a free-running clock. Neither frequency nor phase of this clock is required to be synchronous with respect to the data rate. The ITR loop operates on asynchronous samples to recover the synchronous samples. The A/D converter and digital equalization filter are now outside the loop. Thus, their latency does not contribute to the loop. Hence, a long equalizer can be used. On top of this advantage, it is possible to lower the sampling rate of the A/D converter, for example, for the DVR channel whose cut-off frequency is well below the Nyquist frequency. Therefore, the undersampling nature at the A/D does not lead to any information loss, and the subsequent ITR and detection tasks can, in principle, be fulfilled as well as in a synchronous read channel. With a lower sampling rate A/D converter, the digital equalizer no longer has to operate at the data rate. Another advantage of this type of read channel is that fully digital timing recovery with low cost and high reliability can be implemented. In ITR systems, the conventional analog voltage controlled oscillator (VCO) is replaced by a numerically controlled oscillator (NCO) for the timing recovery loop, in which the frequency and phase errors are stored in digit registers. These loop parameters are less easily affected by external disturbing factors, thereby providing high system reliability.

We also have to mention the drawbacks of this ITR system. The fact that the digital equalizer operates asynchronously at a different rate relative to the data rate increases the complexity of equalizer adaptation, and hence favors shifting part of the burden of the equalizer ahead to an analog filter. Furthermore, the use of SRC requires the design of an interpolation filter, and adds to complexity of the system. The interpolation filter works as a multi-phase FIR filter and its coefficients depend on a fractional phase variable that is adjusted by the ITR loop. Thus, the interpolation filter phase accuracy is rather critical and can influence the entire system performance. This has been observed in previous work reported in [30] [31] [23]. In addition, the ITR system can have a potential risk of cross talk between the physical free-running clock and the recovered synchronous clock. However, due to advances in technology permitting more complex signal-processing functions to be implemented by state-of-the-art digital IC technology, ITR can be implemented with high stability and at low cost.

7.4 Novel Asynchronous Adaptation Structure

This section develops a novel asynchronous equalizer adaptation structure, which will be used for an asynchronously sampled DVR system in the subsequent study. To develop this structure, we first study equalizer adaptation algorithms and conventional adaptation structures.

7.4.1 Equalizer adaptation algorithms

Fig. 7-2 depicts the system model for studying synchronous adaptation algorithms. The sequence r_k, which is the read signal sampled at rate $1/T$, is applied to the equalizer with the T-spaced impulse response coefficients w_k. The equalizer output y_k is compared with its desired value d_k to form an error sequence $e_k = y_k - d_k$ where d_k is obtained by applying the data a_k to a filter whose impulse response is a target response g_k. Adaptation algorithms use e_k to calculate the adaptation gradients Δ_k for updating the coefficients w_k for minimization of the power of e_k. In the following pages, we investigate how Δ_k can be calculated. Below, we briefly study the LMS and zero-forcing (ZF) algorithms of equalizer adaptation.

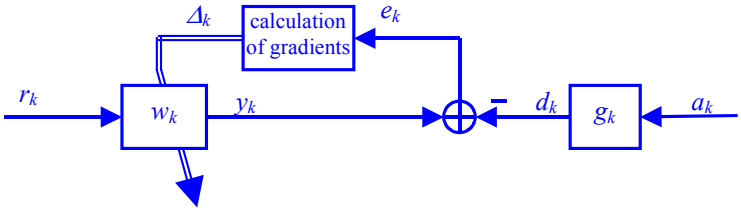


Fig. 7-2: System model for studying synchronous equalizer adaptation algorithms.

A. Conventional LMS adaptation algorithm

Assume that the equalizer has the form of a transversal FIR filter with N_w+1 taps w_k^j ('j' denotes the coefficient index and 'k' denotes the time instant). It is well known that the gradients for adaptation of w_k^j $(0 \le j \le N_w)$, based on the LMS algorithm (see [46] [32] [33] [34]), are given by

$$\Delta_k^j = e_k \cdot r_{k-j} \qquad \text{for} \quad 0 \le j \le N_w . \tag{7.1}$$

To minimize the complexity of the gradient computation, the use of so-called 'signed-LMS' algorithm was suggested in [35] in which the gradient is computed as

$$\Delta_k^j = \mathrm{sgn}(e_k) \cdot r_{k-j} \qquad \text{for} \quad 0 \le j \le N_w \tag{7.2}$$

where $\mathrm{sgn}(x) = \begin{cases} 1 & x \ge 0 \\ -1 & x < 0 \end{cases}$. It was reported in [35] that the SNR loss resulting from this simplification is less than 0.2 dB, while significantly reducing the complexity of equalizer adaptation. Note that the reference r_{k-j} is noise corrupted and may also suffer from channel distortions. To avoid this disadvantage, we resort to another simple algorithm, called the zero-forcing (ZF) adaptation algorithm.

B. ZF adaptation algorithm

In the ZF adaptation algorithm, the noisy reference r_{k-j} is replaced by d_{k-j} in the computation of Δ_k^j [36] [46]. As a result, we have

$$\Delta_k^j = e_k \cdot d_{k-j} \qquad \text{for} \quad 0 \le j \le N_w \ . \tag{7.3}$$

To avoid using a multiplier, we can use a signed-ZF adaptation algorithm as

$$\Delta_k^j = \mathrm{sgn}(e_k) \cdot d_{k-j} \qquad \text{for} \quad 0 \le j \le N_w \ . \tag{7.4}$$

Note that the target response g_k is predetermined and thus known to the receiver. It is usually far shorter than the system response. Thus, calculating d_k is very simple and introduces little delay, thereby making the computation of Δ_k^j extremely simple. Further, due to the absence of noise in d_k, equalizer adaptation behavior based on the ZF algorithm becomes comparatively smooth and reliable.

The gradients (7.3) update the equalizer coefficients w_k^j at instant *k+1* via the recursive equations

$$w_{k+1}^j = w_k^j - \mu \cdot e_k d_{k-j} \qquad \text{for} \qquad 0 \le j \le N_w \tag{7.5}$$

where μ is a constant step-size parameter that controls the speed of adaptation.

C. Effects of ZF adaptation loop convergence

It can be analyzed that the time constant of adaptation, say Γ, is given by

$$\Gamma = \frac{-1}{\ln(1-\mu K_\Delta)} \simeq \frac{1}{\mu K_\Delta} \tag{7.6}$$

where $K_\Delta \triangleq E[\frac{\partial \Delta_k^j}{\partial w_k^j}] = E[(a \otimes h)_{k-j} \cdot (a \otimes g)_{k-j}]$, h_k is the channel bit response, and ' $\otimes$ ' stands for linear convolution. The second step in (7.6) is only valid when $\mu K_\Delta \ll 1$. Correspondingly,

$$\Gamma \simeq \frac{1}{\mu \cdot E[(a \otimes h)_{k-j} \cdot (a \otimes g)_{k-j}]} \ . \tag{7.7}$$

From this expression, we obtain some insights into the influence of the channel gain on Γ. Observe that Γ is inversely proportional to the magnitude of h_k. If a channel gain error occurs resulting in twice larger magnitude compared to the ideal value, the convergence time constant will be halved. Consequently, the equalizer will converge two times faster than expected. At the same time, the magnitude of the equalizer steady-state coefficients will also be halved due to the two times larger gain. On the contrary, if the channel gain is half of the ideal value, the value of Γ will be doubled. This will lead to a two times longer period of time for the equalizer to converge to the steady state and the equalizer coefficients will be two times larger. Hence, time constants Γ are not predictable when gain errors occur in the channel.

Because the bit error rate (BER) is reliable only after the equalizer has converged, Γ is an important parameter for the system. In practical recording systems, the replay signal usually has a large dynamic range and hence an automatic gain control (AGC) mechanism has to be placed in front of the equalizer. By doing so the power of the replay signal is constrained before it

enters the A/D converter and equalizer, so that the time constant of the adaptation loop is well defined.

D. Simplification of equalizer adaptation scheme

For digital recording, the BER performance is primarily determined by data transitions, because decision errors are most likely to occur in the vicinity of a transition, and away from transitions even a slicer will almost make no bit errors. Thus, we may focus the equalizer adaptation effort primarily on transitions. This can be realized according to

$$w_{k+1}^j = \begin{cases} w_k^j - \mu \cdot e_k a_{k-j} & \text{if} \quad a_{k-1} \neq a_{k+1} \\ w_k^j & \text{otherwise} \end{cases} \qquad \text{for} \quad 0 \le j \le N_w . \tag{7.8}$$

The replacement of $e_k d_{k-j}$ by $e_k a_{k-j}$ in (7.8) is warranted by the fact that a_k and d_k have the same sign for the optical recording system under consideration. Note that a_k is a binary sequence taking on values of +1 or –1. Thus the equalizer adaptation loop no longer requires a multiplier for calculating the adaptation gradients. This simplification may work well enough for our purposes.

7.4.2 A novel asynchronous equalizer adaptation structure

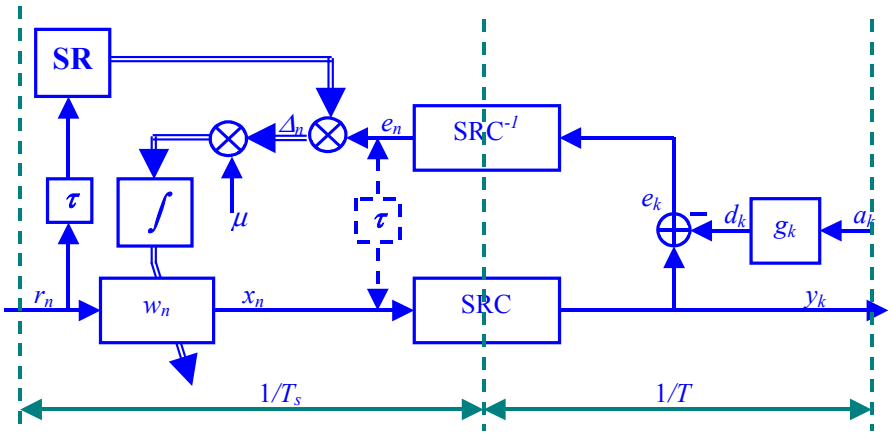
In the preceding discussion, the equalizer coefficients w_k^j are spaced by T seconds. The adaptation of equalizer coefficients and computation of equalizer output are done in synchronism with the data clock at rate $1/T$. However, in asynchronously sampled read channels with ITR as shown in Fig. 7-1(b), the equalizer and its adaptation no longer operate synchronously since the A/D converter is running at a free-running clock rate $1/T_s$. In this situation, the equalizer coefficients w_n^j ($0 \le j \le N_w'$ where $N_w'+1$ is the number of coefficients) are spaced by T_s rather than T seconds. Unless mentioned otherwise, in what follows we will use the subscript 'n' and 'k' to denote T_s-spaced and T-spaced samples, respectively. The equalizer coefficients w_n^j are adjusted via the adaptation loop every T_s seconds. As a result, the equalizer adaptation becomes

$$w_{n+1}^j = w_n^j - \mu \cdot \Delta_n^j \quad \text{for} \quad 0 \le j \le N_w' \tag{7.9}$$

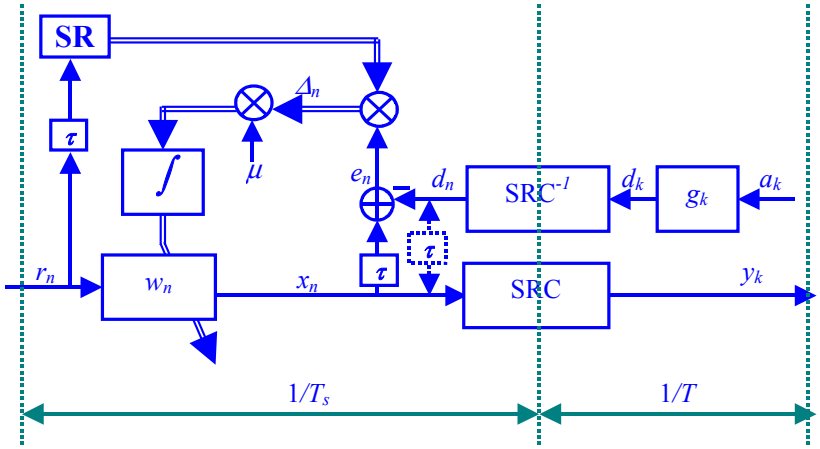
where μ is a constant step-size and Δ_n^j is the gradient at the instant nT_s for updating the *j-th* equalizer coefficient.

Now, an essential question is how to calculate Δ_n^j. Unlike the conventional gradient Δ_k^j, the gradient Δ_n^j has to be calculated every T_s rather than T seconds.

Existing asynchronous equalizer adaptation topologies can be found in [4], which pertains to a free-running sampling frequency above the data rate. Fig. 7-3 depicts these topologies.



(a): Topology I with LMS scheme



(b): Topology II with LMS scheme

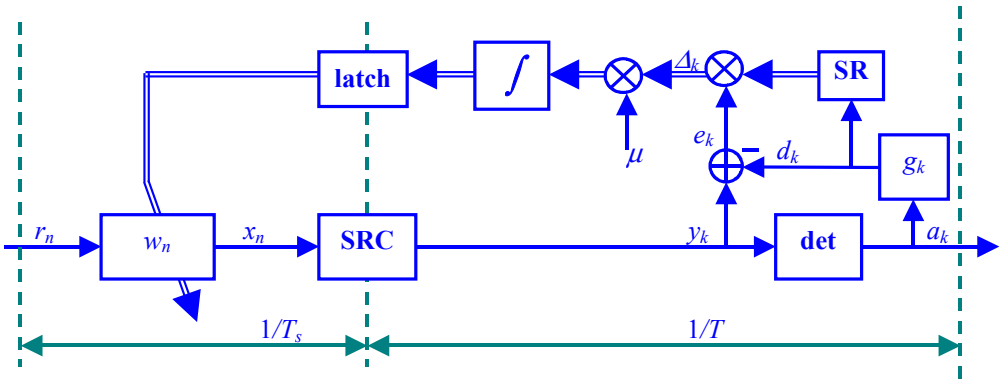
Fig. 7-3: Existing topologies for asynchronous equalizer adaptation with LMS algorithm.

The structure of Fig. 7-3(a) performs the error calculation in the synchronous ($1/T$) domain and converts the error e_k to the asynchronous ($1/T_s$) domain via an inverse sample-rate converter. Due to the presence of the SRC and inverse SRC, there is a delay τ between x_n and e_n in the adaptation loop. The compensation for this delay needs to be done in the forward path before the reference sequence r_n is applied to the shift register (SR). Unlike the structure of Fig. 7-3(a), the structure of Fig. 7-3(b) calculates the error e_n in the asynchronous ($1/T_s$) domain directly, but in this structure both equalizer input and output paths must include the compensation for the delay τ. In this sense, the structure of Fig. 7-3(a) is simpler than the structure of Fig. 7-3(b).

Observe that both topologies employ LMS adaptation. The advantage is that they provide an accurate and straightforward gradient calculation for adaptation. This advantage is obtained at the cost of an extra inverse sample-rate converter for producing the error e_n, which makes the system more complex and expensive. Moreover, the use of a reference r_n from the forward path introduces noise into the multiplication, and at the same time, the delay τ induced by the SRC

and the inverse SRC operation has to be compensated for in r_n in order to obtain valid gradients Δ_n^j. This delay is usually fractional and can be difficult to estimate in practice.

To overcome these disadvantages, we propose a novel structure with the ZF algorithm as shown in Fig. 7-4.



Topology with ZF scheme

Fig. 7-4: Novel structure for asynchronous equalizer adaptation with the ZF algorithm.

This structure is very simple compared with those in Fig. 7-3. First, the reference for calculating the gradient is obtained locally by using decision bits, and hence contains only signal information without noise. Secondly, there is no need to compensate for an unknown delay for calculating the adaptation gradients. This is because the detector and the target response g_k are known, and thereby the relative delay (which normally has an integer value) is known. Therefore, this delay can be predicted and compensated for easily. Thirdly, we can use an extremely simple inverse sample-rate converter, namely a bank of latches (or, equivalently, a bank of zeroth-order interpolators). The reason is that coefficient values, which are obtained from the adaptation gradients via multiplication by a small step size μ and integration, change only slowly as a function of both $1/T$ and $1/T_s$. Even the simplest conceivable inverse sample-rate converter, namely a bank of latches, will then work well for conversion of coefficient values from the synchronous to the asynchronous clock domain.

In principle, coefficient values produced by the bank of integrators pertain to a T-spaced equalizer. The actual equalizer, however, is T_s-spaced. To resolve this mismatch, T-spaced coefficient values would need to be converted into T_s-spaced values through some form of 'spatial' interpolation. For the sake of simplicity, the structure of Fig. 7-4 does not include spatial interpolation. The absence of spatial interpolation will command a performance penalty in situations when T_s deviates much from T. In the sequel, we will gauge this penalty through comparison with a reference topology that does include spatial interpolation. As this topology includes both spatial and temporal interpolation (the latter via the bank of latches), we will refer to it as 'STI' (for Spatio-Temporal Interpolation). We will find that the penalty due to the absence of spatial interpolation is negligible as long as T deviates less than about 40% from T_s.

It is worth noting that this latch-based structure can further save the high-speed multiplier by applying the signed-ZF algorithm for implementation simplicity.

7.5 DVR System Model

This section describes a DVR system model that will be used for investigating the asynchronous equalizer adaptation and ITR structures. Fig. 7-5 depicts this system model.

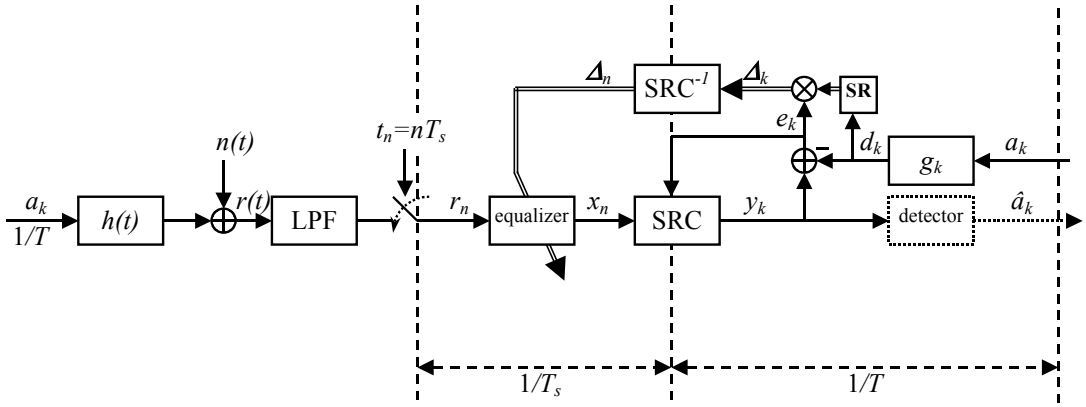


Fig. 7-5: DVR system model.

A d=1 data sequence a_k of rate $1/T$ is applied to a DVR channel with bit response $h(t)$ and additive white Gaussian noise $n(t)$ to obtain the noisy replay signal $r(t)$. A simple model for $h(t)$ is

$$h(t) = \Omega_c \left(\frac{\sin(\pi \cdot \Omega_c \cdot t/T)}{\pi \cdot \Omega_c \cdot t/T} \right)^2 \quad . \tag{7.10}$$

Here, Ω_c<0.5 is the channel cut-off frequency normalized with respect to the symbol rate $1/T$. The frequency response of the DVR channel, denoted $H(\Omega)$ ($\Omega = f \cdot T$ being the normalized frequency variable), is

$$H(\Omega) = \begin{cases} 1 - \dfrac{|\Omega|}{\Omega_c}, & |\Omega| < \Omega_c, \\ 0, & |\Omega| \geq \Omega_c. \end{cases} \tag{7.11}$$

By way of illustration we show in Fig. 7-6 $h(t)$ and $H(\Omega)$ for Ω_c=0.20, 0.25 and 0.33. The replay signal $r(t)$ is applied to a low-pass filter (LPF) that is meant to limit the noise bandwidth prior to the sampling operation. This sampling operation occurs at a crystal-controlled sample rate $1/T_s$, which is not necessarily synchronous to the data rate $1/T$. The resulting sequence r_n of rate $1/T_s$ is applied to a T_s-spaced transversal equalizer that is adapted at rate $1/T_s$ via an adaptation loop. The equalizer output x_n of rate $1/T_s$ is applied to the sample-rate converter to obtain a sequence y_k of rate $1/T$ that is synchronous with respect to the input data a_k. The phase of the sample-rate converter is updated at rate $1/T$ via the ITR loop. The sequence y_k is used by the bit detector, the TED of the ITR loop and the equalizer adaptation loop.

Since the focus of this chapter is equalizer adaptation and ITR, we assume that the detector produces correct decisions. We construct the error signal e_k as $e_k = y_k - d_k$ where d_k is the desired value of y_k and is obtained as $d_k = (a \otimes g)_k$ in terms of the target response g_k and data a_k. For the sake of convenience, we use a 5-tap target response g_k given by

$$[g_{-2}, g_{-1}, g_0, g_1, g_2] = [0.17, 0.5, 0.67, 0.5, 0.17]. \quad (7.12)$$

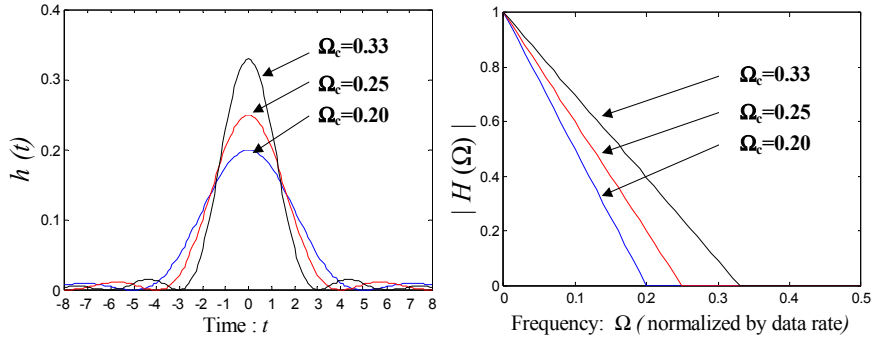


Fig. 7-6: DVR channel bit response *h(t)* and its magnitude response for Ω_c=0.20, 0.25 and 0.33.

By way of illustration, we show g_k and its magnitude response in Fig. 7-7. The reason for using this response is that it resembles a typical high-density DVR system target with a normalized cut-off frequency Ω_c around 0.33.

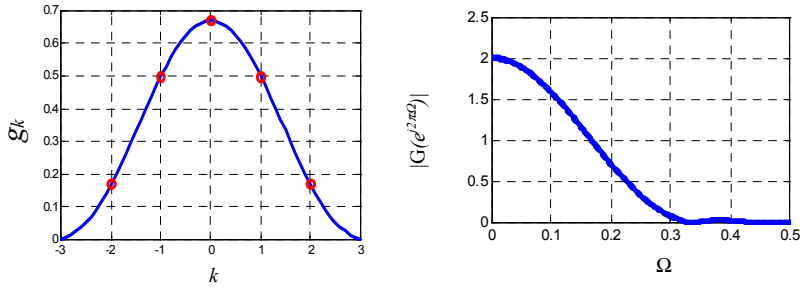


Fig. 7-7: Target response g_k and its magnitude response.

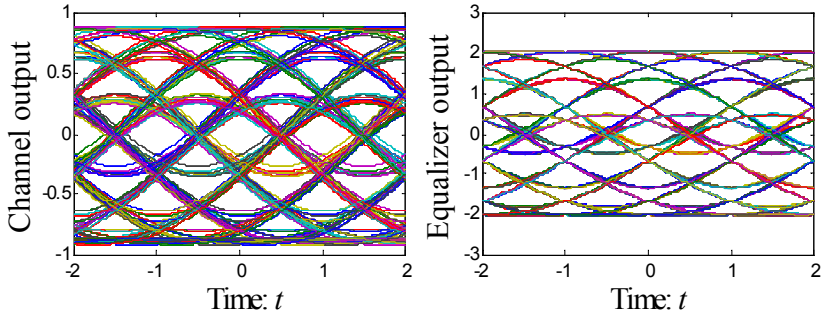


Fig. 7-8: Eye patterns at the channel output and the equalizer output in the absence of noise for Ω_c=0.33.

To better understand the DVR system model, we show in Fig. 7-8 two eye patterns for $\Omega_c = 0.33$. Observe that the eye patterns essentially have 10 levels at the input of detector. This multi-level nature of the DVR signal is determined by the DVR channel and target responses, and in return affects the complexity of equalizer adaptation, ITR and detection algorithms.

7.6 Realization of SRC and ITR for DVR

7.6.1 Realization of sample rate conversion for DVR

A. Principle of SRC and its digital realization

Sample rate conversion can be thought of as a procedure of resampling after reconstruction. Conceptually, an analog signal is first reconstructed from the digital signal by means of D/A conversion and filtering, and is then resampled at a different rate [37]. Therefore, SRC can be viewed as a process of resampling as illustrated in Fig. 7-9(a). The digital signal x_n of rate $1/T_s$ is applied to a linear pulse modulator with symbol response $c(t)$ to reconstruct the continuous-time signal $y(t)$, and $y(t)$ is then sampled at a different rate, say $1/T$, to form a digital signal y_k of rate $1/T$. Ideally, $c(t)$ is a *sinc* pulse according to $c(t) = \dfrac{\sin(\pi t / T_s)}{\pi t / T_s}$. However, this function cannot be realized in practice. One solution is to apply a truncated version of the *sinc* pulse, which will cause a certain degradation. A more practical solution is to exploit a realizable function that can meet the SRC requirements without causing a significant degradation. Basic requirements include: a) $c(t)$ should be symmetric for avoiding phase distortion; b) the in-band magnitude response of $c(t)$ should be essentially flat; and c) the response should prevent aliasing, i.e. out-of-band components should be rejected sufficiently.

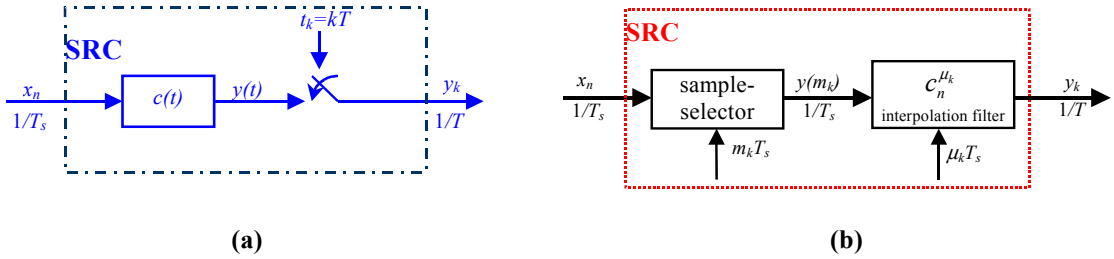


Fig. 7-9: Block diagram of SRC. (a): principle of resampling after reconstruction; (b) digital realization of SRC.

Actual implementation of the SRC is entirely digital, as shown in Fig. 7-9 (b), which can be viewed as the SRC portion of the ITR for the DVR system shown in Fig. 7-5. The equalizer output y_n of rate $1/T_s$ is applied to the sample-selector that has an integer index m_k for choosing the interpolator input samples y_{m_k} from x_n. The interpolation filter with impulse response coefficient $c_n^{\mu_k}$ operates on its inputs y_{m_k} to produce the synchronous samples y_k. The variable $\mu_k \in [0,1)$ is a time-varying phase of the interpolation filter relating to the index m_k. The instants t_k for forming the samples x_k can be expressed in terms of T_s according to $t_k = (m_k + \mu_k)T_s$, where the integer part m_k and the fractional part μ_k are determined by

$$m_k = \left\lfloor \frac{t_k}{T_s} \right\rfloor \quad , \quad \mu_k = \frac{t_k}{T_s} - \left\lfloor \frac{t_k}{T_s} \right\rfloor \tag{7.13}$$

where $\lfloor x \rfloor$ means the maximum integer not exceeding x. Ideally, the spacing of these instants t_k is equal to T seconds , i.e.

$$t_k - t_{k-1} = (m_k + \mu_k)T_s - (m_{k-1} + \mu_{k-1})T_s = T\,, \tag{7.14}$$

so that we can determine m_k and μ_k in a recursive fashion as

$$\mu_k = \mu_{k-1} + \frac{T}{T_s} - \left\lfloor \mu_{k-1} + \frac{T}{T_s} \right\rfloor, \qquad m_k = m_{k-1} + \left\lfloor \frac{T}{T_s} + \mu_{k-1} - \mu_k \right\rfloor. \tag{7.15}$$

The instants t_k are determined by the ITR loop, which involves a TED, a loop filter, and a NCO. We will investigate the ITR loop in detail later.

B. Interpolation filter design

The DVR channel has a low-pass nature. We need an interpolation filter with a pass-band that covers all the desired DVR components while rejecting the out-of-band noise as much as possible. One can refer to [17] [26] [27] for mathematical formulas of interpolation filter design in the presence of noise. For the sake of simplicity and convenience for study and simulation, we use an existing six-point Lagrange-interpolator with impulse response [38]

$$c_n^{\mu} = \begin{cases} \dfrac{\mu(\mu^2-1)(\mu^2-4)}{120} & n=-3, \\ \dfrac{-\mu(\mu^2-1)(\mu+2)(\mu-3)}{24} & n=-2, \\ \dfrac{\mu(\mu+1)(\mu^2-4)(\mu-3)}{12} & n=-1, \\ \dfrac{-(\mu^2-1)(\mu^2-4)(\mu-3)}{12} & n=0, \\ \dfrac{\mu(\mu-1)(\mu^2-4)(\mu-3)}{24} & n=1, \\ \dfrac{-\mu(\mu^2-1)(\mu-2)(\mu-3)}{120} & n=2. \end{cases} \tag{7.16}$$

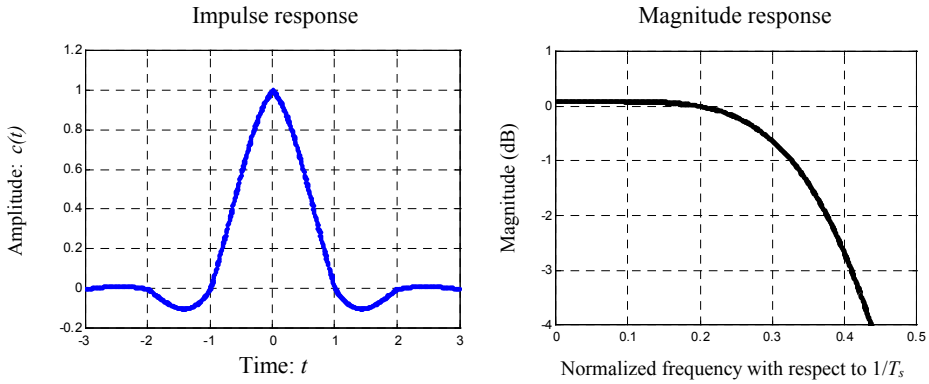


Fig. 7-10: Impulse response and frequency response of the six-point Lagrange interpolator.

This interpolator has six coefficients and induces a three-symbol delay at its output. The reason for using this interpolator is that it is simple and has good features in its time- and frequency-domain responses. It exhibits a symmetric time-domain response that induces no phase distortion, and its frequency response has a 3 dB cut-off frequency at $0.4/T_s$, which is sufficiently good for our purposes. These features are illustrated in Fig. 7-10.

7.6.2 Realization of ITR for DVR

Having studied the DVR system model, the equalization filter, and the SRC structure, we can now describe the asynchronously sampled DVR system of Fig. 7-5 in more detail, as shown in Fig. 7-11.

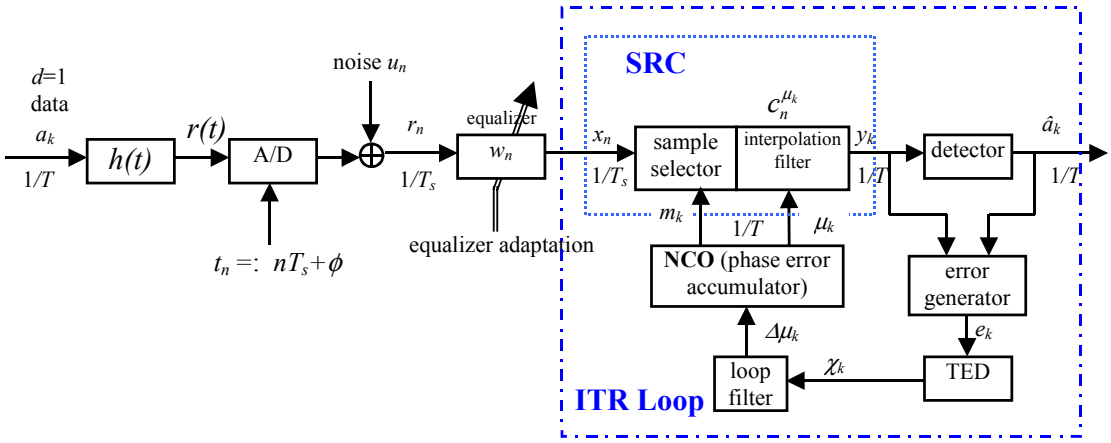


Fig. 7-11: Asynchronously sampled DVR system with ITR loop.

In the ITR loop, the TED output χ_k is computed based on the error samples e_k. It is then filtered by the loop filter to create a gradient $\Delta\mu_k$ for the phase error accumulator. The loop filter is similar to the one used in the conventional VCO-based timing recovery loop. The phase error accumulator can be viewed as a numerically controlled oscillator (NCO), similar to the VCO in an analog timing-recovery loop. Its outputs are used to update the integer index m_k and the fractional phase μ_k for the sample-selector and interpolation filter, respectively, of the SRC.

A. ITR loop recursive update

In practice, each instant t_k can suffer from a timing phase error $\tau_k T$. One objective of the ITR loop is to update the interval of instants t_k to track T. Thus, the ITR loop update should strive to accomplish

$$[t_k + \tau_k T] - [t_{k-1} + \tau_{k-1} T] = T \,. \tag{7.17}$$

Using the fact that $t_k = (m_k + \mu_k)T_s$, we reformulate (7.17) as

$$m_k + \mu_k - m_{k-1} - \mu_{k-1} = \frac{T}{T_s}[1-(\tau_k - \tau_{k-1})]. \tag{7.18}$$

Upon realizing that the value of μ_k is fractional and that m_k is integer, we obtain the recursive equations for updating m_k and μ_k in the presence of a timing phase error as

$$\mu_k = \left(\mu_{k-1} + \frac{T}{T_s}[1-(\tau_k - \tau_{k-1})] \right) \bmod 1 \tag{7.19}$$

and

$$m_k = m_{k-1} + \left\lfloor \mu_{k-1} + \frac{T}{T_s}[1-(\tau_k - \tau_{k-1})] \right\rfloor \tag{7.20}$$

where $(x \bmod 1) \triangleq x - \lfloor x \rfloor \in [0,1)$.

The difference of normalized timing phase errors, say $[\tau_k - \tau_{k-1}]$, is updated under the control of the NCO-based ITR loop. This difference can be interpreted as the NCO control variable, which is effectively a period or frequency control knob. The ITR loop is responsible to force this difference, on average, to zero. This can be accomplished by using a second-order PLL loop, given by

$$\begin{aligned} \lambda_k &= \lambda_{k-1} - \beta \cdot \chi_{k-1} \\ [\tau_k - \tau_{k-1}] &= \lambda_k - \alpha \cdot \chi_{k-1} \end{aligned} \tag{7.21}$$

where α and β are step-size values and χ_k is the TED output. The term λ_k compensates for frequency offset and the NCO output accounts for accumulation of $[\tau_k - \tau_{k-1}]$. The use of negative sign in (7.21) is due to the fact that the TED has positive (negative) outputs for positive (negative) timing phase errors. In practice, α and β can be determined by

$$\alpha = \frac{2\varsigma^d \omega_n^d T}{K_d K_o}, \quad \beta = \frac{(\omega_n^d T)^2}{K_d K_o} \tag{7.22}$$

where K_d and K_o are the gain factors of the TED and NCO, respectively. Here, ς^d and ω_n^d are the damping factor and natural frequency of the PLL, respectively. In most practical situations, $\varsigma^d \simeq 0.707$ and $\omega_n^d T \ll 0.1$.

B. ZF based TED for DVR

Several algorithms have been reported in the literature for symbol-rate timing recovery [39] [40] [41] [42] [43] [44] [45] [46]. Among these algorithms, the zero-forcing (ZF) TED is attractive for its simplicity and near optimal performance.

In this section, we consider sample-based and transition-based ZF TEDs, and compare their data-aided (DA) and decision-directed (DD) schemes. The DA TEDs use the original data,

while the DD TEDs use the actual decisions. For the ITR system given in Fig. 7-11, one example of the symbol-rate ZF TED output can be written as (see Chapter 4)

$$\chi_k = (y_{k-1} - d_{k-1})(d_k - d_{k-2}) \tag{7.23}$$

where y_k is the reconstructed synchronous sample value at the interpolation filter output and d_k is the desired value of y_k, given by $d_k = (a \otimes g)_k$ where a_k is the data and g_k is the target response. Usually, d_k is produced based on decisions $\hat{a}_k$ rather than the data a_k, i.e., $\hat{d}_k = (\hat{a} \otimes g)_k$. This leads to the DD TED scheme given by

$$\chi_k = (y_{k-1} - \hat{d}_{k-1})(\hat{d}_k - \hat{d}_{k-2}) . \tag{7.24}$$

Concentrating primarily on transitions in y_k, we may simplify the TED in (7.24) into a transition-based TED as

$$\chi_k = (y_{k-1} - d_{k-1})[\mathrm{sgn}(d_k) - \mathrm{sgn}(d_{k-2})] .$$

This implies that only the samples y_{k-1} that meet the condition $\mathrm{sgn}(d_k) \neq \mathrm{sgn}(d_{k-2})$ contribute to the TED output. The TED output is set to zero under other conditions.

For the DVR system incorporating the rate 2/3 (1,7) code and the 5-tap target response g_k given in (7.12), one can verify that d_k and a_k are of same sign, i.e. $\mathrm{sgn}(d_k) = a_k$ for all instants *k*. Applying this fact to $\chi_k = (y_{k-1} - d_{k-1})[\mathrm{sgn}(d_k) - \mathrm{sgn}(d_{k-2})]$ and noting that the useful component of χ_k is the average value of χ_k, we can further simplify the transition-based TED as $\chi_k = y_{k-1}(a_k - a_{k-2})$, or equivalently as (after allowing the loop to absorb a gain factor of 2),

$$\chi_k = \begin{cases} y_{k-1} a_k & \text{if} \quad a_k \neq a_{k-2} , \\ 0 & \text{otherwise} . \end{cases} \tag{7.25}$$

Substituting $\hat{a}_k$ for a_k, we obtain the DD TED scheme as

$$\chi_k = \begin{cases} y_{k-1} \hat{a}_k & \text{if} \quad \hat{a}_k \neq \hat{a}_{k-2} , \\ 0 & \text{otherwise} . \end{cases} \tag{7.26}$$

This is a very simple TED algorithm, which does not need a multiplier and the conventional error calculation $e_{k-1} = y_{k-1} - d_{k-1}$. The TED output is given by y_k at transitions with its sign controlled by $\hat{a}_k$. Thus, this TED is simpler than the conventional error-based TEDs according to (7.23) and (7.24).

By way of illustration, we evaluate the timing functions for the DVR based on the TEDs according to (7.23), (7.24), and (7.26), and show the result in Fig. 7-12.

In this simulation, the normalized timing phase error τ ranges from –1 to +1. The six-point Lagrange interpolator of (7.16) is used for forming y_k. Timing phase errors are introduced by changing the phase of the interpolation filter. For the DD TED scheme, bit

decisions $\hat{a}_k$ are obtained from a threshold detector. Observe that the timing functions cross zero at the ideal phase ($\tau = 0$), and have good linearity. The timing function in the data aided case is monotonic due to the consistent use of the correct data a_k. The decision-directed function exhibits multiple zero crossings, which can be distinguished in practice by using specific acquisition and byte synchronization mechanisms. Also, observe that the linear ranges of the timing functions of these TEDs are comparable. The identical slopes of the functions are due to the fact that the timing information resides mainly in the vicinity of transitions.

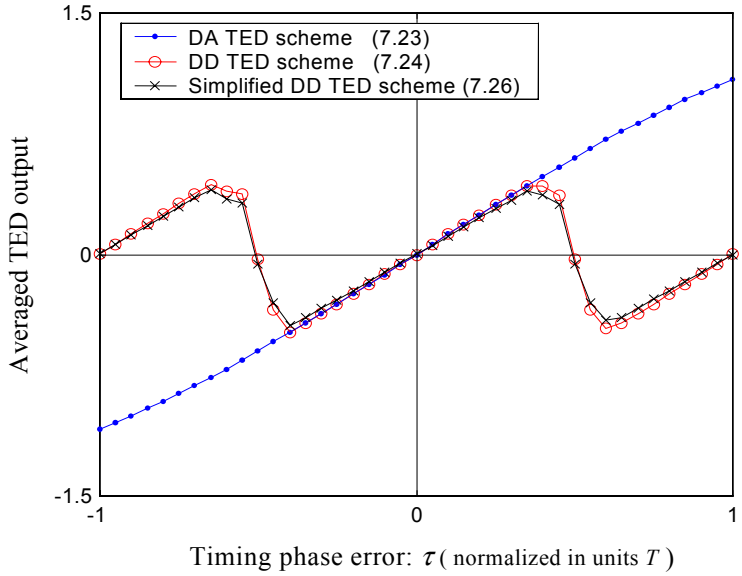


Fig. 7-12: Timing functions for the DVR with Ω_c=0.33 TED, no noise, and *d*=1 data.

7.7 Simulations of Asynchronous Equalizer Adaptation and ITR Loops for DVR

In this section, we simulate the asynchronous equalizer adaptation and ITR loops for DVR. We show the simulation block diagram of the DVR system in Fig. 7-13. We specifically study the latch-based asynchronous adaptation structure, which involves the adaptation calculation block shown in Fig. 7-14, and the ITR calculation block shown in Fig. 7-15, where '*D*' represents one bit interval delay. We first study adaptation and timing recovery separately, and later consider joint adaptation and timing recovery. The DVR channel considered here has a normalized cut-off frequency $\Omega_c = 0.33$ and additive white Gaussian noise (AWGN). The noise is added behind the A/D converter according to Fig. 7-11. The SNR, which is defined in the matched filter bound sense, is assumed to be 9 dB, which represents a worst-case situation with BER around $10^{-2} \sim 10^{-3}$. We characterize the oversampling rate by a parameter

$\text{src} \triangleq (T - T_s)/T_s$. For instance, $\text{src} < 0$ denotes undersampling ($T_s < T$), $\text{src} > 0$ denotes oversampling ($T_s > T$), and $\text{src} = 0$ denotes synchronous sampling ($T_s = T$).

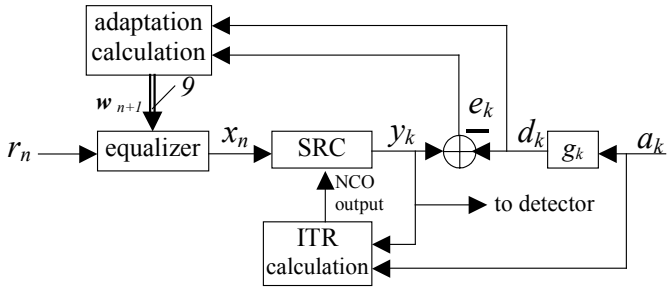


Fig. 7-13: Block diagram showing the equalizer adaptation and ITR loops in the DVR receiver (the quantity w_{n+1} represents a vector consisting of 9 equalizer coefficients).

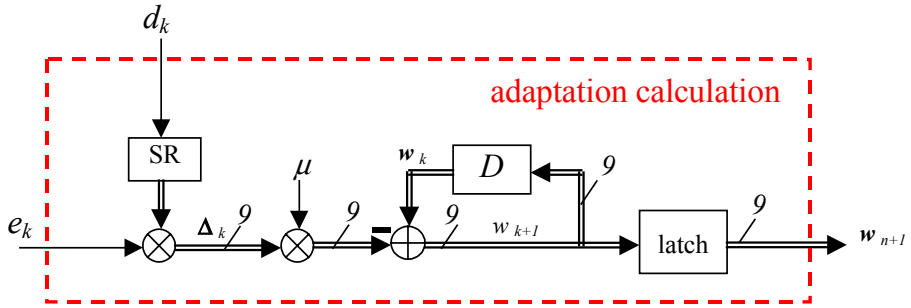


Fig. 7-14: Schematic showing the equalizer adaptation based on the latch-based asynchronous ZF adaptation structure.

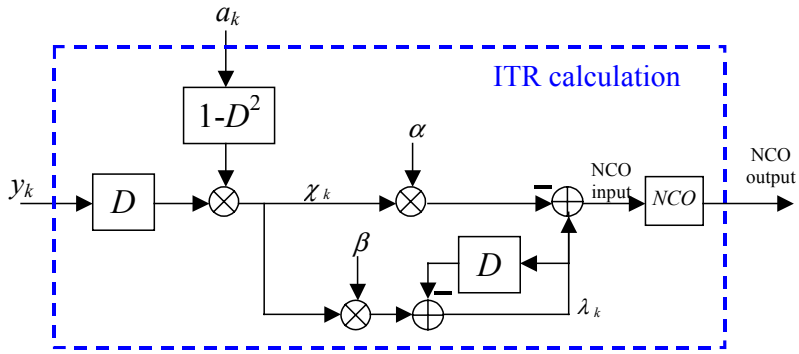


Fig. 7-15: Schematic showing the ITR calculation for the NCO adjustment in the ITR loop.

7.7.1 Asynchronous equalizer adaptation

In the simulations of this subsection, only the equalizer is adapted. The timing recovery loop is kept open and ideal sampling phase is assumed in the sample-rate converter.

A. Simulation of synchronous sampling operation scheme

First, we perform simulations for src=0. The objective is to investigate the synchronous equalizer adaptation performance, and to check if the interpolation filter is working fine. This simulation sets a reference for asynchronous adaptation. Illustrative results are shown in Fig. 7-16.

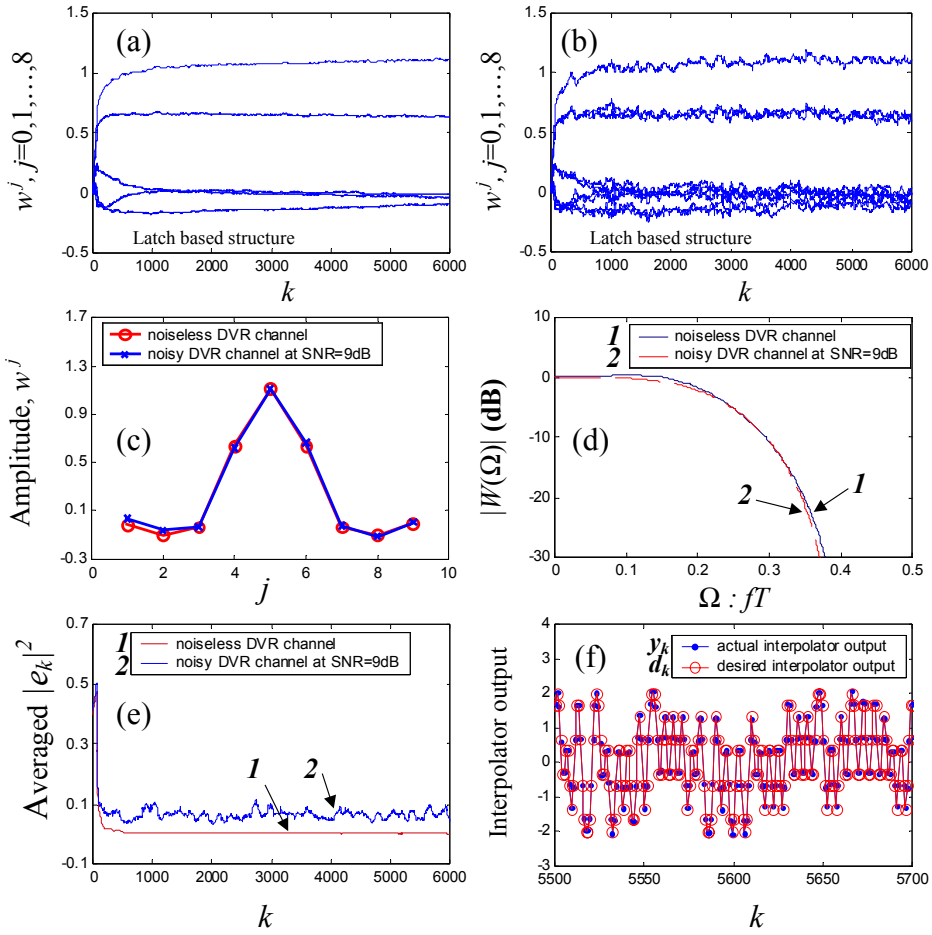


Fig. 7-16: Simulation results of synchronous adaptation at T_s=T for a 9-tap equalizer. (a) coefficient convergence for the noiseless channel; (b) for the 9 dB SNR channel; (c) steady-state equalizer coefficients; (d) corresponding equalizer magnitude response; (e) time-averaged squared error convergence; (f) detector inputs.

Fig. 7-16 illustrates the equalizer convergence for both the ideal (noise-free) and the worst-case (9 dB SNR) channel conditions. The squared errors are averaged over 100 bits for smooth display. The simulation shows that the 9-tap equalizer converges well to a symmetric impulse response. The steady-state equalizer has a low-pass nature and even at 9 dB SNR its magnitude response matches the ideal response very well. The error power converges well enough to produce the desired detector inputs. The noise-like convergence of the equalizer coefficients at 9 dB SNR arises due to the gradient noise resulting from the use of a relatively large step size. This simulation confirms that the sample-rate converter and latch-based adaptation structure are working satisfactorily.

B. Simulation of asynchronous schemes

We now consider the asynchronous situation. For undersampling, we choose src=-0.25 , or equivalently, $T_s = (4/3)T$, so that aliasing is avoided, albeit marginally. For oversampling, we choose src=0.25 , i.e. $T_s = (3/4)T$. The objectives of this part of the simulation are threefold: (a) investigate the suitability of the 6-point Lagrange interpolator given in (7.16); (b) examine the latch operation; and (c) evaluate the adaptation loop performance.

Since the latch replaces a spatio-temporal interpolation (STI), we evaluate the latch vis-a-vis a STI. Recall from Section 7.4.2 that when we use a 'latch' for the conversion of equalizer coefficients from the synchronous ($1/T$) to the asynchronous ($1/T_s$) clock-domain, only the temporal interpolation operation is involved in the conversion, whereas 'STI' involves both spatial and temporal interpolation operations. Performance is evaluated by examining the differences in error power and by measuring the equalizer frequency response. The simulation results are shown in Fig. 7-17 and Fig. 7-18 for $T_s = (4/3)T$ and $T_s = (3/4)T$, respectively.

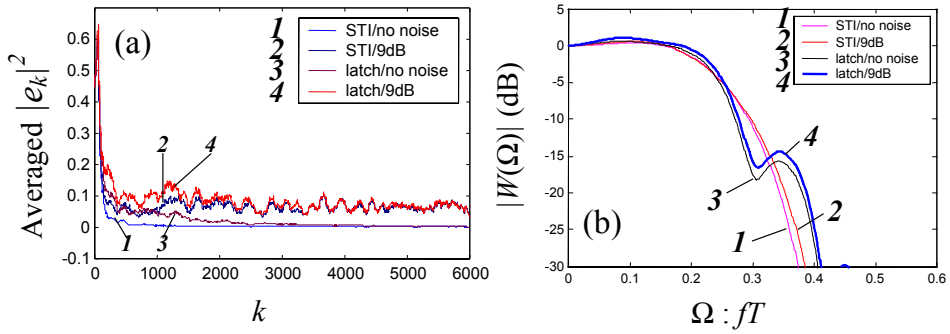


Fig. 7-17: Simulation results of undersampled asynchronous adaptation (T_s=(4/3)T): (a) time-averaged squared error convergence, (b) steady-state equalizer magnitude response.

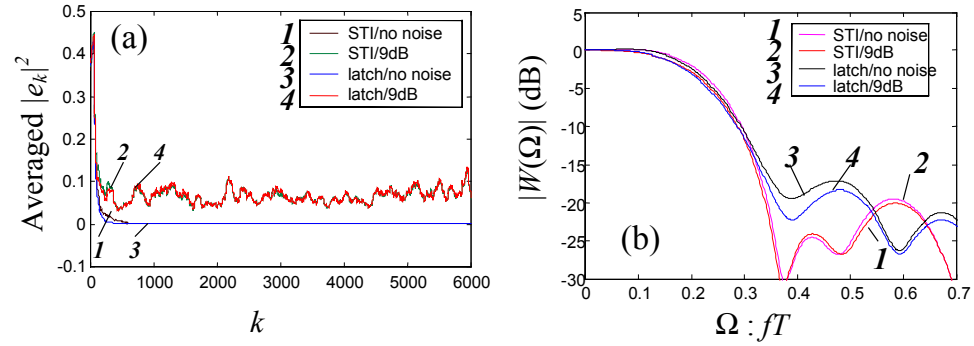


Fig. 7-18: Simulation results of oversampled asynchronous adaptation (T_s=(3/4)T): (a) time-averaged squared error convergence, (b) steady-state equalizer magnitude response.

From the above simulations, we obtain the following observations. First, the 6-point Lagrange interpolator according to (7.16) and Fig. 7-10 is sufficient for our purpose. The error power converges well to comparable levels as in the synchronous situation, even at 9 dB SNR. This confirms that the 6-point Lagrange interpolator can well preserve the in-band components of the DVR channel.

The second observation concerns the adequacy of the latch as replacement of the STI. Observe that the error powers for the latch- and STI-based structures are almost identical in the steady state. The most apparent difference between both can be observed in the steady state equalizer magnitude responses. These responses differ significantly in the out-of-band region (Ω>0.33) and match well in most of the in-band region ($\Omega \leq 0.33$). For undersampling ($T_s = (4/3)T$), the responses for the latch-based structure produce some in-band deviations near Ω=0.33. For oversampling ($T_s = (3/4)T$), the in-band deviation is insignificant. In both cases, however, the out-of-band attenuation differs by more than 10 dB. The use of a latch tends to boost the stop-band response as T_s deviates from T and to move its corner frequency away from 0.33, which is the cut-off frequency of the target response.

Reasons for the above observations are twofold. One is that the effective span (in seconds) of the equalizer is different for undersampling and oversampling for the fixed length (9 taps) equalizer. Another reason is that compared to the STI-based structure, the latch-based structure may produce quite different taps at the two ends of the equalizer due to the absence of the spatial interpolator. This could be the reason for the boost in the out-of-band components (high frequency region) and for the shifted corner frequency.

During the simulation, we observed big fluctuations in the coefficients in the cases of oversampling relative to the cases of undersampling. This is because of the fact that for a given SNR, noise power is considerably higher for $T_s<T$ than for $T_s>T$. The noise power is proportional to the channel bandwidth, and hence increases with the oversampling factor. However, the effective span of the equalizer is less for $T_s<T$ compared to $T_s>T$ since the number of taps is kept fixed.

To investigate the tolerable range of sampling rates and the latch-based adaptation loop performance, we consider the sampling rates ranging from undersampling to oversampling schemes, with the ITR loop opened. We evaluate the steady state error power and compare with that for the STI-based structure. The results are shown in Fig. 7-19.

From Fig. 7-19, we obtain the following observations. First, at 9 dB SNR, noise increases the error power baseline from –27 dB to –11 dB. At the baseline of –11 dB, we examined the equalizer response, and found that it matched the ideal response very well. This was verified through the simulations according to Fig. 7-16 to Fig. 7-18. Second, at 9 dB SNR, the asynchronous adaptation loop works well for oversampling ratio T/T_s from 0.7 to 1.7, which corresponds to T_s from T_s=1.43T to T_s=0.59T. Observe that the error power throughout this range remains essentially constant and that the error power levels obtained for the latch- and STI-based structures almost coincide. Performance of the latch-based structure deteriorates rapidly relative to that of the STI-based structure when T_s<0.59T. The latch-based structure is relatively sensitive to noise and to the selection of T_s when $T_s<T$. One reason could be the insufficient span of the equalizer resulting in poor stop-band suppression.

We also observe a deterioration for T_s>1.43T. Unlike the deterioration for oversampling, this deterioration is not primarily due to noise, but to the undersampling scheme itself. This is because the latch-based structure causes a considerable in-band signal loss for T_s>1.43T. We investigated and found that for T_s>1.43T and T_s<0.59T the equalizer performs badly in terms of the frequency response and the sample-rate converter output samples. In both cases, the equalizer taps are not well centered and the frequency response has a large in-band distortion and weak out-of-band attenuation. Moreover, the cut-off frequency deviates far from its desired position.

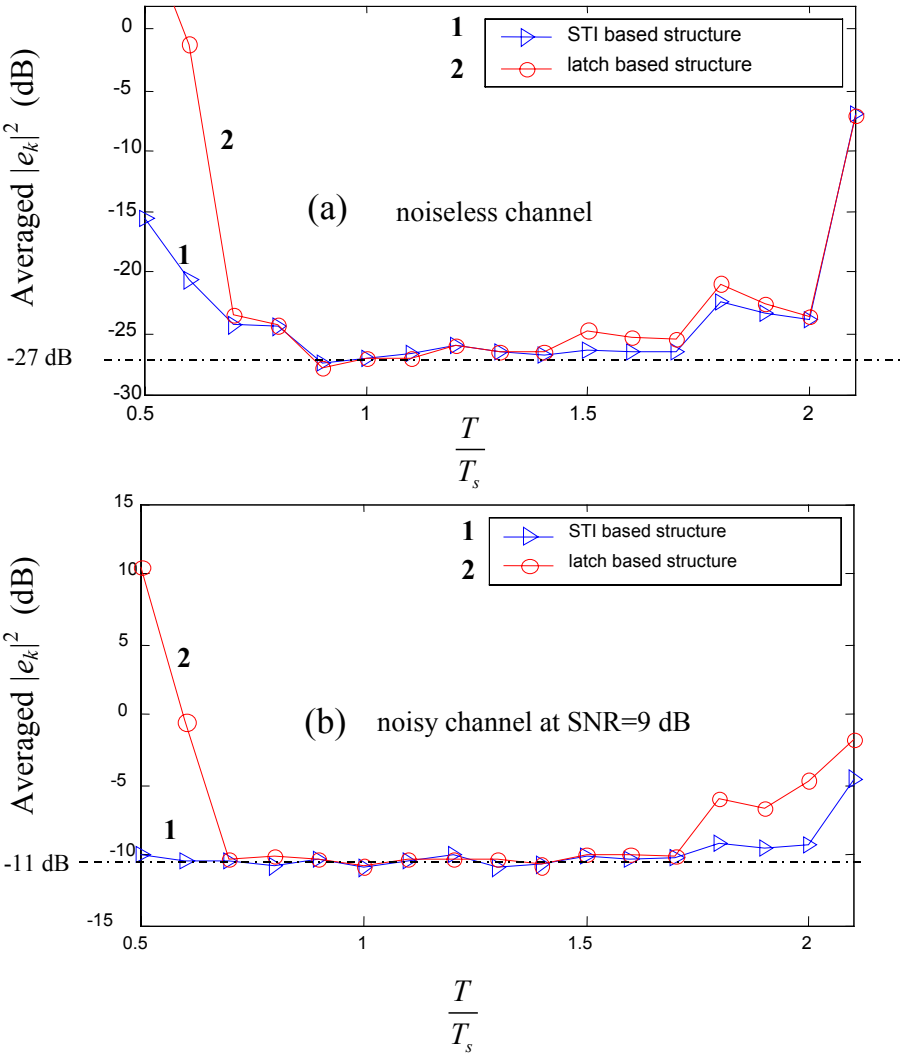


Fig. 7-19: Equalizer adaptation performance of the latch-based and STI-based structure for various sampling rates with (a) no noise; (b) 9 dB SNR.

We explain the above observations as follows: The performance of the latch-based structure, compared to the STI-based structure, deteriorates rapidly when T_s<0.59T and T_s>1.43T. This roughly corresponds to T_s, being at least 40% of T smaller and bigger, respectively, than T. In both situations, the omission of spatial interpolation, as in the latch-based structure, seems too serious. The consequence is that the equalizer taps are effectively located at least 40% away from their desired positions. As a result, large inaccuracies of the equalizer taps inevitably occur, thereby making the latch-based loop work inadequately.

The above results suggest that for a considerable sampling rate range from T_s=1.43T to T_s=0.59T, the latch-based structure can adequately replace the STI-based structure while causing only a negligible degradation. This replacement greatly reduces the complexity of the asynchronous adaptation loop. For DVR, undersampled operation is attractive in practice. The investigation results suggest that the latch-based structure is promising for DVR systems.

7.7.2 Interpolative timing recovery simulation

In the simulations of this subsection, we restrict the investigation to the interpolative timing recovery loop for a fixed equalizer. The objective is to examine the performance of a fully digital NCO-based timing recovery loop with the ZF TED algorithm according to (7.26). We examine the ITR loop convergence and NCO outputs, and check if the injected initial timing phase error and frequency offset eventually converge to zero. The initial values of timing phase error and frequency offset are set to 0.3 and 0.002, respectively, which are normalized with respect to the synchronous bit interval at the interpolator output. We use a second order PLL as shown in Fig. 7-15. Unless noted otherwise we use $\varsigma^d \cong 0.707$ and $\omega_n^d T \cong 0.01$.

We simulate the second-order ITR loop and monitor the behaviors of the TED output, the NCO output and the frequency offset. The results are shown in Fig. 7-20, Fig. 7-21 and Fig. 7-22, respectively. The simulations cover the synchronous (src=0) and asynchronous (src=-0.25, src=0.25 and src=-0.123) conditions. Observe that all ITR loop variables properly converge to zero. This validates the adequacy of the TED. Even though we conducted the simulations in the absence of noise, similar simulation results were obtained when the channel has noise.

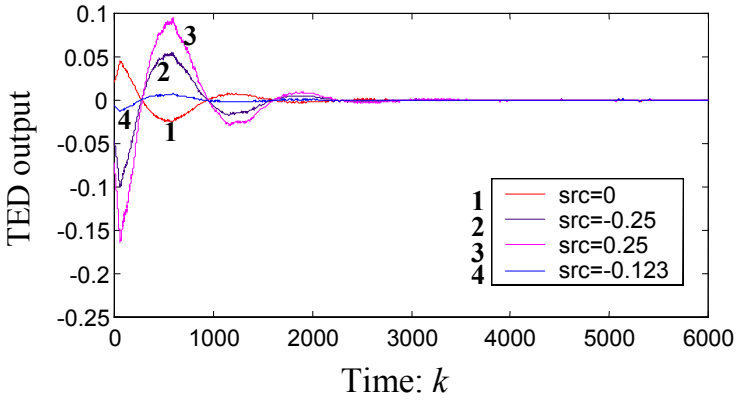


Fig. 7-20: TED output for various sampling rates for the noiseless DVR channel with a fixed equalizer.

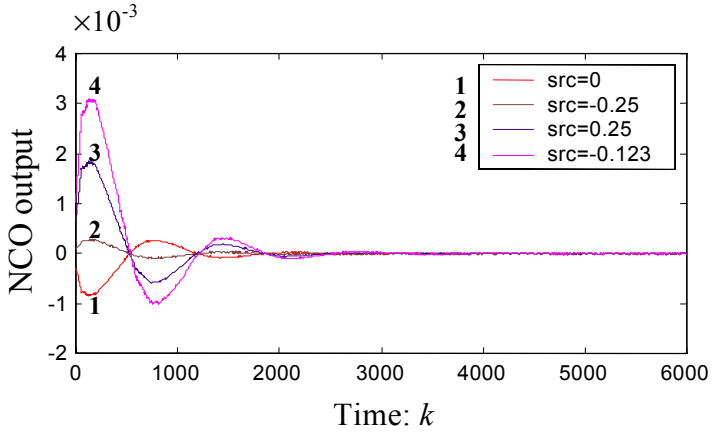


Fig. 7-21: NCO output for various sampling rates for the noiseless DVR channel with a fixed equalizer.

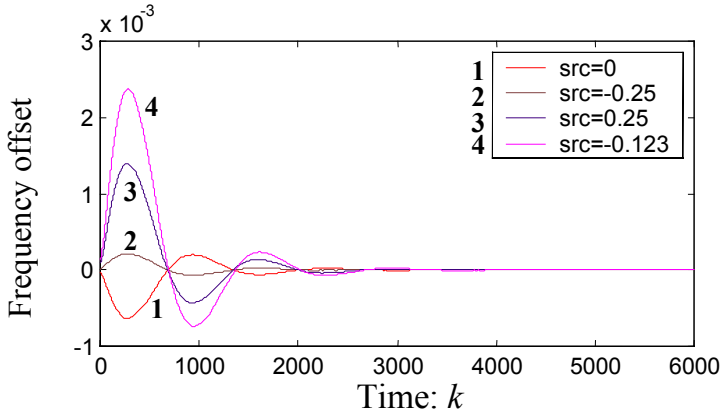


Fig. 7-22: Frequency offset for various sampling rates for the noiseless DVR channel with a fixed equalizer.

7.7.3 Simulations for joint asynchronous equalizer adaptation and ITR loops

Having separately investigated the asynchronous equalizer adaptation and ITR loops, we can now operate these two loops simultaneously. The objectives of these simulations are to evaluate the convergence behaviors of adaptation and ITR loops when they operate together, and to examine their interaction. We consider synchronous and asynchronous situations and simulate both noiseless and noisy conditions. For the asynchronous situation, we consider both undersampled and oversampled operations. For undersampling we consider $T_s=(4/3)T$ and $T_s=(10/9)T$, which represent heavily and lightly undersampled cases. For oversampling we consider $T_s=(4/5)T$ and $T_s=(1/2)T$, which represent lightly and heavily oversampled cases.

A. Results in the absence of noise

In the absence of noise, the error power curves all converge to zero in the steady state in all the cases considered here. The 9 coefficients of the equalizer converge well and are properly centered in the steady state. By way of illustration, we show in Fig. 7-23 the simulation results of the error power convergence, the steady-state equalizer magnitude response versus normalized frequency $f \cdot T$, and the convergence of ITR loop parameters (i.e. the TED output, NCO output and frequency offset).

Observe that the magnitude response of the equalizer changes as a function of sampling rate. For the synchronous case ($T_s=T$), the equalizer has approximately flat in-band response and the cut-off frequency occurs at around 0.33. Out-of-band attenuation is greater than 10 dB. For the heavily undersampled case ($T_s=(4/3)T$), the in-band response hardly changes, but the out-of-band attenuation is less than 8 dB. The attenuation improves to slightly more than 15 dB for the lightly undersampled case ($T_s=(10/9)T$). For the lightly oversampled case ($T_s=(4/5)T$), the out-of-band attenuation exceeds 20 dB and the in-band response is perfectly flat. However, the cut-off frequency increases thus increasing the equalizer bandwidth. This effect is even more pronounced for the heavily oversampled case ($T_s=(1/2)T$). The increased bandwidth does not pose a problem here because noise is absent. But we will observe later that when noise is present, this increased bandwidth can lead to a performance degradation.

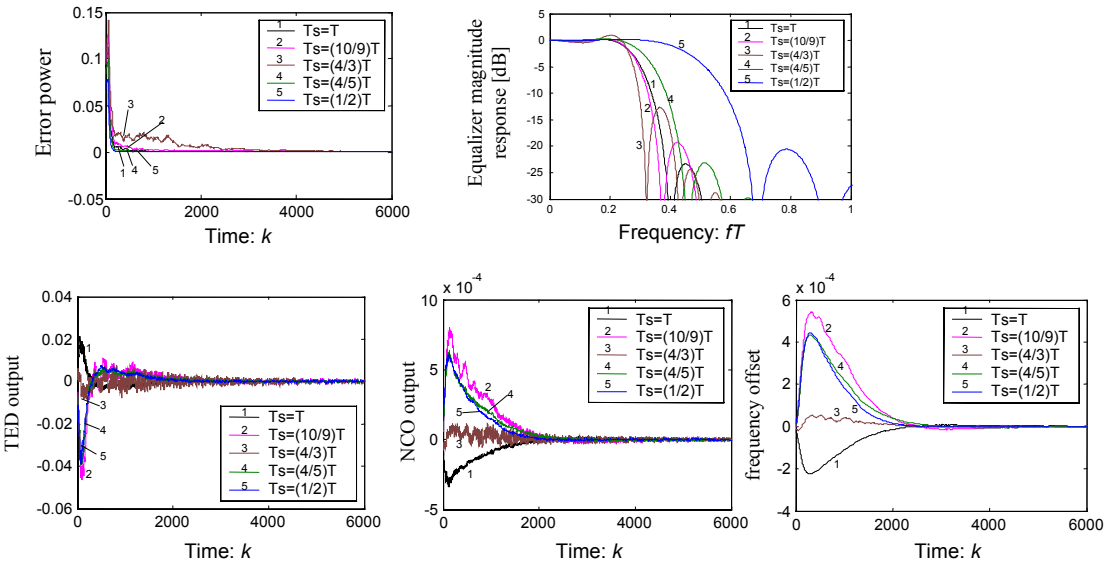


Fig. 7-23: Simulation results of the latch-based equalizer adaptation and ITR loops for the noiseless DVR channel for $T_s=T$, $T_s=(10/9)T$, $T_s=(4/3)T$, $T_s=(4/5)T$ and $T_s=(1/2)T$.

The ITR loop parameters converge well as desired. For the synchronous, lightly undersampled, lightly and heavily oversampled situations, the TED output, the NCO output and the frequency offset converge smoothly. Only for the heavily undersampled case, ITR convergence curves have small fluctuations. These simulation results suggest adequate convergence behaviors for the noiseless case.

B. Results in the presence of noise

Now we look into the results in the presence of noise. Fig. 7-24 shows the results for the equalizer adaptation loop.

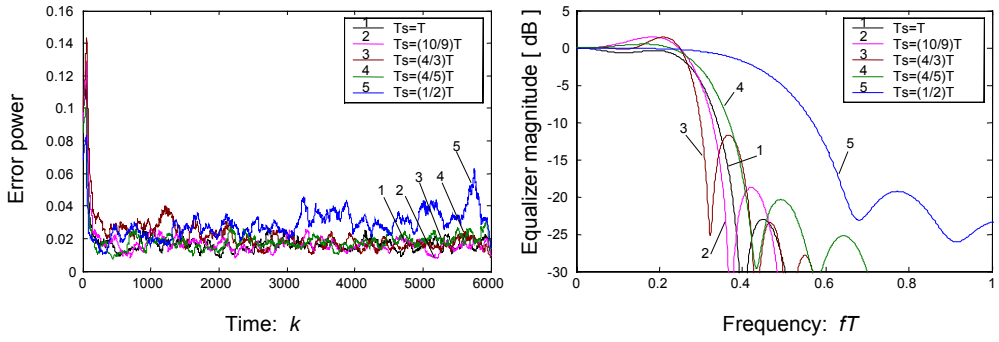


Fig. 7-24: Error power convergence of equalizer output and steady-state equalizer magnitude response with latch-based equalizer adaptation and ITR loops at 9 dB SNR for $T_s=T$, $T_s=(10/9)T$, $T_s=(4/3)T$, $T_s=(4/5)T$ and $T_s=(1/2)T$.

For the synchronous case (T_s=T), the equalizer properly converges to the steady state, with a symmetric impulse response. The error power in the steady state is roughly –17 dB, as compared to –11 dB without ITR loop. Similar observations are obtained for the heavily and lightly undersampled cases. The equalizer impulse responses for these cases converge to be symmetric with good linear phase characteristics. No visible interaction was observed between the adaptation and ITR loops. This benefit could be due to the low cut-off frequencies of the DVR channel and the selected target, which are well below the Nyquist frequency, as well as to the symmetric features of the channel and target responses. Consequently, the equalizer has linear phase characteristics and a low-pass nature with a high attenuation at the Nyquist frequency.

We also observed that the equalizer responses are similar to those obtained in the absence of noise, which roughly have the same in-band flatness and at least 8 dB out-of-band attenuation. Their band edges are located around or below the DVR channel cut-off frequency 0.33. These characteristics effectively prevent noise aliasing for SRC. The in-band distortion, however, leads to some signal loss and thus causes errors at the sample-rate converter output. For this reason, reconstructed samples at the sample-rate converter output can induce decision errors. In general, for synchronous and undersampled conditions, the adaptive equalizer behaves properly. Similar observations and conclusions apply to the ITR loop. Also, no apparent interaction between the adaptation and ITR loops was observed for these situations.

The results for both lightly and heavily oversampled situations are quite different from those in the absence of noise. The converged equalizer coefficients are no longer symmetrically centered, indicating a phase distortion. The response has a flat in-band response but the bandwidth extends far beyond that of the channel. The band edge, in fact, has moved towards the Nyquist frequency. This is particularly true for the heavily oversampled case, where the expected low-pass equalizer now becomes almost an all-pass equalizer. As a result, much of the noise passes through the equalizer, and the sample-rate converter output exhibits severe noise aliasing. In this situation, the adaptive equalizer is likely to diverge. This can be prevented by using a smaller adaptation step-size, which was confirmed by simulation. Excessive gradient noise could be the reason for this, because the equalizer can converge very well to the steady state in the absence noise at this oversampling rate. In addition, we observe an interaction between the equalizer adaptation and ITR loops. This is because the inadequately converged equalizer coefficients result in large errors at the sample-rate converter output, yielding big TED and NCO output errors, which in turn degrade the SRC performance and produce even bigger errors at the sample-rate converter output. The resulting errors at the sample-rate converter output cause gradient computation inaccuracy for the adaptation loop, and result in erroneous equalizer coefficients. Consequently, these errors increase further and cause the equalizer adaptation to diverge.

7.8 Summary and Further Discussions

In this chapter, we studied an asynchronously sampled DVR system with asynchronous equalizer adaptation and fully digital interpolative timing recovery. We modeled the DVR system, developed adaptation algorithms, performed analysis, and simulated the system under various conditions. We proposed a new structure for the asynchronously sampled DVR system, in which a simple latch replaces the spatio-temporal interpolator for equalizer adaptation and a fully digital ITR replaces the conventional VCO-based timing recovery. The simulations show that the proposed latch-based equalizer adaptation structure with the ITR loop works well for a

considerable range of sampling rates. In conclusion, the structure is simple, cost-effective and thus promising for DVR.

So far, two problems have hindered an efficient application of asynchronous adaptive equalizers. The first problem is the cost and complexity of real-time, multi-tap equalizer adaptation. The second is the interaction between the adaptation process and other control loops such as the AGC and timing recovery loops. To deal with the first problem, we proposed a zero-forcing adaptation algorithm and investigated a simple and effective latch-based structure for asynchronous adaptation. This greatly simplifies the equalizer adaptation relative to the one based on the LMS algorithm. For timing recovery, we exploited the SRC technique and developed a fully digital interpolative timing recovery, which makes the timing loop operate at low cost and high stability. For the second problem, interaction, we notice that AGC, equalizer adaptation and timing recovery constitute three nested control loops. An adjustment in one loop can interact with the operation of the other loops. Since we focused on asynchronous adaptation in this chapter, we did not investigate the interaction issue further. Also, in our study we assumed that the AGC and detector decisions do not suffer from errors.

The interaction issue can be a topic for future research. Given the strong potential for interactions between the equalizer adaptation, AGC and timing loops, a constrained adaptation algorithm is needed to reduce or eliminate interaction. This issue is explored, for example, in [4], [5], [26], [28], [47], [48] and [49].

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CHAPTER 8

SUMMARY AND CONCLUSIONS

The objectives of this work are the study and development of timing recovery techniques for digital recording systems. Partial-response and decision feedback equalized magnetic recording systems and asynchronously sampled digital video recording systems are considered. We study issues related to the tracking and acquisition performance, develop practical timing recovery techniques, and carry out numerical analysis and evaluation simulations for various recording densities. This chapter summarizes the thesis work and notable conclusions, and provides suggestions for future research.

Chapter 2 reviews basics of timing-recovery techniques. We discuss basic structures, requirements, performance measures, and the existing approaches. We compare inductive and deductive timing recovery structures, and explore the effects of RLL modulation codes on timing recovery. We also study measures of timing sensitivity, timing-error detector (TED) efficiency, and tracking and acquisition performances. We particularly investigate the maximum-likelihood (ML), minimum mean-square error (MMSE) and zero-forcing (ZF) timing recovery techniques and analyze their tracking performances for magnetic recording systems. We study the acquisition problems, investigate the issues of hang up and false lock during timing acquisition, and explore solutions. In addition, we review practical decision-directed (DD) and non-decision-directed (NDD) TED schemes for timing acquisition and study several acquisition issues such as phase acquisition bound and acquisition speed measures.

Chapter 3 studies the timing sensitivity of multi-level decision feedback equalization (MDFE) and partial-response class-IV with Viterbi detector (PR4-VD) for magnetic recording. We develop an efficient approach for evaluating the error rate performance based on the estimated probability density function of residual intersymbol interference (ISI) due to misequalization and timing phase errors. This approach can cover the performance consequences of both static phase error and random timing jitter. The numerical results have been shown to closely match those obtained from bit-by-bit simulations. The principle of this approach can be easily extended to evaluate the timing sensitivity of advanced versions of MDFE and PR4-VD detectors.

Chapter 4 performs TED efficiency analysis of timing recovery for partial response (PR) and decision feedback equalization (DFE) receivers in magnetic recording. We analyze several TED schemes and propose error-based ZF TED schemes. The error based TEDs are not only simple to implement but also exhibit equivalent or even better efficiencies compared to the existing non-error based TEDs. We also analyze the TED noise performance and provide a

marginal-detection based TED algorithm for jitter minimization. Simulation results show that this algorithm can reduce jitter variance, especially for low SNRs. In addition, we study optimality issues for timing acquisition. The investigation shows that the MDFE TED with 6*T*-pattern preamble is near optimum in terms of efficiency for timing acquisition over a range of recording densities of interest.

Chapter 5 focuses on hang-up and false-lock acquisition problems, and develops two effective solutions to these problems for DFE receivers in recording systems. We demonstrate that these solutions can facilitate a fast and reliable acquisition process. One solution uses special equalizer coefficients and a control procedure with switches. This technique has been shown to be effective for solving the false lock problem. On the other hand, the second solution, which uses a modified threshold scheme, prevents false lock and hang up in a more general manner. Simulations have shown that this solution can tolerate large initial errors in gain, DC offset and threshold scalars.

In Chapter 6, we present an implementation of timing recovery for a 100Mb/s experimental MDFE read channel prototype. We specifically detail the TED realization, charge-pump control, lock-to-preamble detection, and sync-byte detection circuits. We evaluate the prototype on both bench and spinstand, and measure the performance of the timing recovery system. The timing recovery board works well at high data rate to support a robust MDFE prototype. The measurement results show that the circuit performance is close to the expected result. The implementation is simple and reliable, and can be easily realized by an integrated solution.

Chapter 7 investigates a new type of receiver for digital video-recording (DVR) channels. It proposes a new asynchronous equalizer adaptation structure with fully digital interpolative timing recovery (ITR) for DVR. The investigation shows that this new structure is promising for DVR in optical recording applications. The structure is attractive for its low-cost high-stability timing-recovery implementation and low-sample-rate adaptive equalizer. We study and simulate the DVR system with this new structure for a wide range of sampling rates. The results show that the proposed structure is robust enough even in the worst-case SNR, and that performance is satisfactory.

8.1 Further Work

By the end of this dissertation work, we have developed an experimental MDFE read channel prototype and its extended version, called M2DFE prototype. Both systems use the timing recovery system that is developed and analyzed in this thesis. The current TED algorithm is active at transitions. The transition conditions are checked only by the two most recent decisions in the feedback register. Wrong decisions may mislead the TED and degrade the timing recovery loop performance. One approach to improving the TED is to make use of reliable decisions and to check for code-rule violations. This approach seems worth pursuing for the M2DFE read channel, where more reliable decisions are available within the structure.

Noise performance of timing recovery loops is always a concern, especially for high density and low SNR recording channels. For this reason, a good recording channel model should include media noise in addition to electronic additive white Gaussian noise (AWGN). For simplicity, we do not consider media noise effects. Studying timing recovery loop behavior in the presence of media noise is a good topic of further work.

Future work might also consider timing recovery for recording channels using turbo coding, where good BER performance is obtainable at poor SNR. In this situation, the effect of noise and distortion becomes even more critical, and robust techniques for timing recovery are of great interest.

Another topic of future work might be the investigation of the interaction between the equalizer adaptation, timing recovery and automatic gain control (AGC) loops. As the gradients for controlling these three loops are normally derived from the same error signal that is obtained from the detector input, parameter variations of one loop will inevitably affect parameters of the other loops. To make the three loops operate well and converge within an expected period of time, interaction effects among these loops have to be investigated and effective approaches have to be developed to mitigate these effects. To reach this aim, new adaptation and timing recovery schemes may be needed.

Samenvatting

Een kritisch deel van systemen voor digitale gegevensopslag is het zogenaamde lees-schrijfkanaal, dat bestaat uit de elektronische circuits die nodig zijn voor het schrijven van digitale gebruikersgegevens op het opslagmedium en voor het betrouwbaar teruglezen van de geschreven gegevens. Een goed ontworpen lees-schrijfkanaal kan zowel de opslagcapaciteit als de overdrachtssnelheid van het opslagsysteem vergroten. Egalisatie, bit-detectie en klokterugwinning behoren tot de belangrijkste functies van een lees-schrijfkanaal.

De eerstgenoemde twee functies mogen zich verheugen in een ruime belangstelling van onderzoekers. Naarmate opslagsystemen efficiënter worden in termen van bijvoorbeeld modulatie-code, bandbreedte en informatiedichtheid, wordt de taak van het klokterugwinningssysteem moeilijker en tegelijkertijd kritischer voor betrouwbare bit-detectie. Het klokterugwinningssysteem dient om optimale beslissingstijdstippen voor de bit-detector te demarceren. Het onderzoek dat beschreven wordt in dit proefschrift behelst aspecten van klokterugwinning voor lees-schrijfkanalen.

Dit proefschrift is gewijd aan de studie en ontwikkeling van klokterugwinningstechnieken voor digitale gegevensopslagsystemen. Het bestudeert de structuur en prestaties van klokterugwinningstechnieken, en ontwikkelt nieuwe klokterugwinningstechnieken voor magnetische en optische gegevensopslagsystemen. Het proefschrift omvat acht hoofdstukken. Hoofdstuk 1 geeft een korte inleiding op het gebied van digitale gegevensopslagtechnieken en lees-schrijfkanalen. Dit hoofdstuk beschrijft verder de motivatie voor het onderhavige werk, alsook de belangrijkste bijdragen en opbouw van het proefschrift. Hoofdstuk 2 verschaft een gedetailleerd overzicht van klokterugwinning, en in het bijzonder van de diverse mogelijke structuren, eisen, en prestatie-maatstaven. Dit hoofdstuk beschrijft ook generieke algoritmen voor tijdfoutschatting en de belangrijkste aspecten van tijdbasisacquisitie. Waar mogelijk worden de discussies ondersteund door analyses en simulatie-resultaten. Hoofdstukken 3 tot en met 7 beschrijven de belangrijkste nieuwe onderzoeksbijdragen van het proefschrift. Hoofdstuk 8 beëindigt het proefschrift met enkele aanbevelingen voor toekomstig werk.

Hoofdstuk 3 onderzoekt de gevoeligheid voor tijdbasisfouten van twee soorten bit-detectoren, te weten de ‘partial-response Viterbi detector’ en de beslissingsteruggekoppelde egalisator. Tevens wordt een analytische benadering ontwikkeld voor de invloed van statische en stochastische tijdbasisfouten op de prestatie van deze detectoren. Hoofdstuk 4 bestudeert de efficiëntie van bestaande en nieuw voorgestelde algoritmen voor schatting van tijdbasisfouten in systemen met ‘partial-response’ detectoren en beslissingsteruggekoppelde egalisatoren. Tevens ontwikkelt en analyseert dit hoofdstuk een ‘marginaal-detectie’ algoritme voor schatting van tijdbasisfouten in een meer-niveau beslissingsteruggekoppelde egalisator. Verder onderzoekt het hoofdstuk de acquisitie-prestaties van bij deze egalisator bruikbare data-preambules en schattings-algoritmen. Hoofdstuk 5 bestudeert het probleem van tijdbasis-acquisitie in beslissingsteruggekoppelde egalisatoren. Het hoofdstuk ontwikkelt een tweetal nieuwe technieken voor snelle acquisitie die vrij zijn van ‘hang-up’ en ‘false-lock’ problemen, zelfs bij grote initiele fouten van tijdbasis, versterking en DC niveau. Hoofdstuk 6 beschrijft het ontwerp en de implementatie van een praktisch klokterugwinningssysteem, opgebouwd met discrete ECL (emitter-coupled logic) componenten, voor een 100 Mb/s experimenteel lees-

schrijfkanaal met meer-niveau beslissingsteruggekoppelde egalisator. De prestatie van dit systeem wordt geëvalueerd voor zowel synthetische weergave-golfvormen als voor een experimenteel magnetisch gegevensopslag-systeem.

De nadruk bij de ontwikkeling van de algoritmen en systemen in Hoofdstukken 3 t/m 6 ligt op magnetische gegevensopslag, alhoewel deze algoritmen en systemen met geringe wijzigingen ook bruikbaar zijn voor optische gegevensopslag. Daarentegen ligt de nadruk in Hoofdstuk 7 op optische gegevensopslag. In dit hoofdstuk wordt een nieuwe en aantrekkelijke architectuur ontwikkeld voor volledig digitale ‘zero-forcing’ egalisator-adaptatie in combinatie met interpolatieve klokterugwinning. De ontwikkeling van de algoritmen en systemen in Hoofdstukken 3 t/m 7 wordt ondersteund door uitvoerige computersimulaties. De simulatieresultaten dienen ter illustratie van de effectiviteit van de voorgestelde algoritmen, en ter bevestiging van de analytische resultaten.

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Curriculum Vitae

Jianjiang Wang was born in Korla, China, on October 23, 1965. In 1983, he entered the Tsinghua University, Beijing, the most renowned university in China, to major in Communications in the Department of Electronic Engineering. He received the B.Sc and M.Sc degrees in Electrical Engineering from Tsinghua University in 1988 and 1993, respectively. From 1988 to 1990, he was an electronic engineer with the Industrial Applied Television Institute, Changzhou, China, and from 1993 to 1995, he was a researcher with the Tsinghua University, Beijing, in the Advanced Communications Group of the Department of Electronic Engineering. From 1995 to 2001, he worked in the Coding and Signal Processing Department of the Data Storage Institute (DSI) in Singapore. In 2001, he joined the Maxtor Corporation, Milpitas, California, USA, in the Advanced Channels and ASICs Department.

During his association with DSI, he worked on a series of research projects on multilevel decision feedback equalization (MDFE) technology. These projects were sponsored by two international consortia (MDFE and M3DFE consortia) whose members included the disk drive companies IBM San Jose, USA, Fujitsu Japan, Hitachi Japan, Texas Instruments, USA, Tektronix, USA and DSI, Singapore. As part of his industrial research at DSI and his academic research towards a Ph.D., he made several contributions to the development of MDFE technology. In view of the significance of his contributions, in particular of the hardware prototyping and demonstration of MDFE and M2DFE read channels, he was awarded along with two other colleagues the Distinguished Researcher Award of the Year 1998 by DSI. This is the highest annual award in DSI for recognizing research achievements. Following this, he and his colleagues received the Outstanding Researcher Award by the National University of Singapore (NUS) in 1999.

Since 1996, he also pursued a Ph.D. degree in the Department of Electrical and Computer Engineering of NUS, and subsequently was selected to be part of the joint Ph.D. program between NUS and Eindhoven University of Technology (TU/e), The Netherlands. From September to December in 2000, he carried out his Ph.D. research in the Signal Processing Systems group in the Department of Electrical Engineering of TU/e. During this period, he also was a guest researcher in the Storage Signal Processing Group of Philips Research Laboratories, Eindhoven, The Netherlands.