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Digitally Generated CPFSK IF Test Signals Including Phase Noise

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Abstract— We present a simple, all electrical method for the generation of test signals for testing of fiber-optic coherent CPFSK IF receiver systems, using a programmable bit error rate tester. The feature to be able to add phase noise to the IF signal makes it possible to evaluate receiver system behavior with relation to local oscillator phase noise.

I. INTRODUCTION

THE choice for CPFSK modulation for coherent optical communication systems is attractive because of the simple laser modulation concept.

The generation of CPFSK IF test signals, which are used during the development of CPFSK receiver IF systems (Fig. 1) is, on the other hand, difficult. In our case, we have a communication system for a bitrate of 311 Mbit/s, a modulation index $m = 1$, and an IF bandwidth of 700 MHz centered at 465 MHz. To generate a CPFSK IF test signal, we would require a voltage controlled oscillator at 465 MHz, which can be swept over 311 MHz at the 311 Mbit/s bitrate. Practically, this is impossible. Another method has been presented [1], but this method requires several phase and frequency locked synthesized generators. Moreover, it does not take into account the phase noise. This latter phenomenon being of major importance in optical coherent communication systems.

II. DIGITALLY GENERATED SIGNALS

To synthesize the IF signal of a 311 Mbit/s heterodyne CPFSK receiver (modulation index $m = 1$, IF centered at 465 MHz) we would need a generator that is switched between $f_l = 311$ MHz and $f_h = 622$ MHz at the 311 Mbit/s rate, while the phase of the output signal should be continuous at the frequency change overs. This can easily be realized digitally by the simple setup, shown in Fig. 2. The output of a clock generator, running at twice the bitrate, is applied to an input of an AND gate and to a frequency divider (flip flop). The output of the divider is connected to an input of a second AND gate and to the clock input of a pattern generator. The data output of this generator is connected to the second input of the first AND gate and inverted to the second input of the second AND gate. Both AND outputs are "ORed" together
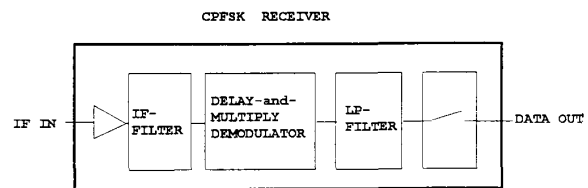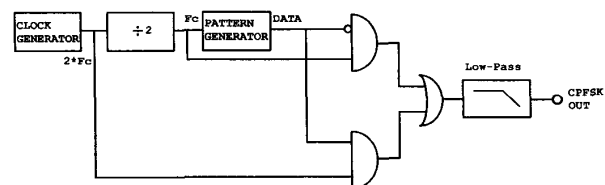
Fig. 1. CPFSK receiver.

Fig. 2. Schematic diagram of the digital generation of a CPFSK IF signal.
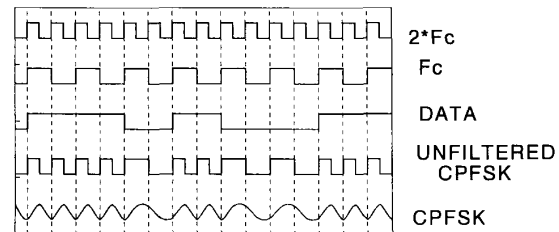

Fig. 3. Composition of the CPFSK IF signal from the clock signal, twice the clock signal and the DATA signal.

and lowpass filtered. Fig. 3 shows a diagram of the various signals which compose at the end the CPFSK signal.

III. USING A PROGRAMMABLE BIT ERROR RATE TESTER

The availability of a programmable BERT [2] makes it even more simple to generate the desired IF signal. Fig. 3 shows that f_l is generated by a 0011 sequence, while f_h is generated by a 0101 sequence on the basis of the $2f_c$ clock.

These sequences can easily be programmed in the pattern memory of the BERT (Fig. 4, upper part). The first step is to download the standard test pattern (PRBS) from the BERT to a personal computer via the IEEE-488 interface. Then substitute a 0011 sequence for every 0 in the downloaded pattern and a 0101 sequence for a 1 data bit. Manchester coded CPFSK signals can be generated as well. In this case a data 0 results in a 00110101 sequence and a data 1 gives 01010011. In this last case, the clock rate of the BERT is eight times the data baud
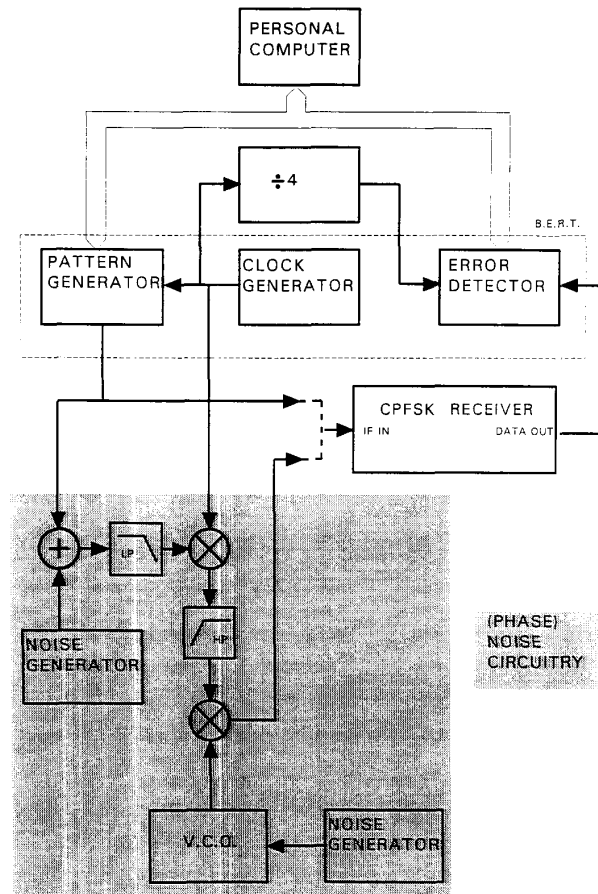
Fig. 4.   Block diagram of the CPFSK IF signal generation by means of the BERT and the circuitry for (phase) noise addition (lower part of the diagram).

Fig. 5.   (a) Measured, (b) calculated, and (c) simulated spectra.

rate, whereas in the case of uncoded CPFSK, the clockrate is four times the bit rate.

The last step is to upload the modified pattern from the pc to the user memory of the pattern generator. In the case of a Manchester coded CPFSK signal, the reference pattern of the error detector can also be downloaded and accordingly modified (a 0 data signal becomes 01, a 1 becomes 10). The CPFSK IF test signal is now available at the DATA output of the pattern generator; harmonics of the test signal can be filtered by a lowpass filter with a cutoff frequency at about three times the bit rate, but are also suppressed by the IF filter of the CPFSK receiver. As the clock generator runs at four times the bit rate (CPFSK) or at eight times the baud rate (Manchester coded CPFSK), it is necessary to use a divider to offer the correct clock information to the error detector.

IV. ADDING NOISE TO THE SIGNAL

To evaluate a CPFSK receiver, we can add noise to the signal and measure the influence of the noise on the receiver performance [1]. However, the performance not only degrades due to shot noise, thermal noise, and local oscillator relative intensity noise (RIN), but also by the phase noise of the
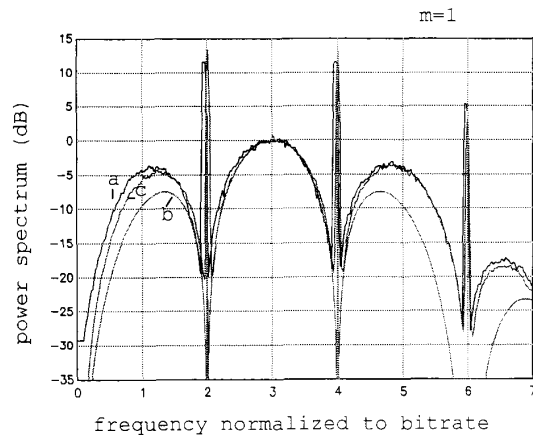
transmitting laser and the local oscillator laser. To evaluate a receiver, we changed the setup to add additive noise and phase noise to the test signal (Fig. 4, lower part).

White noise is added to the CPFSK signal and then, after lowpass filtering (given a cut-off frequency of 900 MHz, in our case) to remove higher harmonics, the spectrum is up-converted by mixing with the clock. A highpass filter (cut-off frequency 1.2 GHz) removes the image spectrum, then the signal is mixed down by the output of a voltage controlled oscillator (VCO) that runs at an average frequency equal to the clock frequency.

Phase noise is added to the CPFSK signal by modulating the VCO with noise. The simulated laser linewidth can be adjusted by varying the input noise level to the VCO. It is well known that laser phase noise is modeled as a random walk process of the phase [3]. A Gaussian probability density function of the phase drift results into a Lorentzian lineshape, where the linewidth is proportional to the spectral density of the (white) Gaussian noise impressed onto the phase of the VCO. This has been verified experimentally, both by the authors and reported in literature [4]. Moreover, mixing the light from two lasers gives an IF spectrum that maintains the Lorentzian shape and has a linewidth equal to the sum of the linewidths of the individual lasers. This latter linewidth should be generated by the test circuit.

V. MEASUREMENTS

We measured the CPFSK IF spectrum of a Manchester coded PRBS (2^7-1) signal at the data output of the BERT (Fig. 5(a)). This spectrum is compared to a calculated spectrum [5] (Fig. 5(b)) and it is noticed that the calculated spectrum for $m = 1$ differs from the generated spectrum. This can be explained by the fact that, in the case of the generated signal, the frequencies f_l and f_h are derived from the clock signal and that the generated waveforms are square instead of sinusoidal. To confirm this we simulated the spectrum under the conditions of square wave output, and the frequency changeover from f_l to f_h, and vice versa, were locked to the clock signal (Fig. 5(c)). Now the resulting spectrum corresponds well to the generated spectrum.
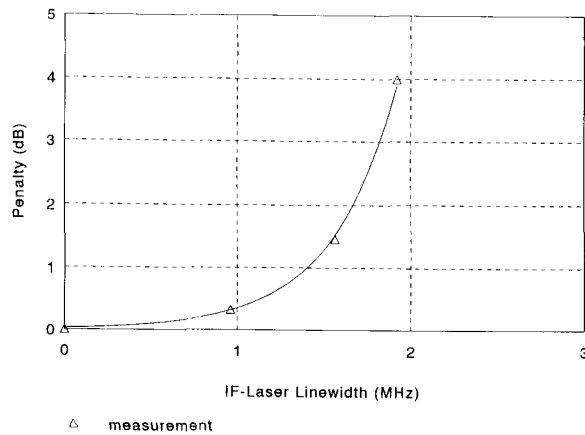
Fig. 6. Receiver performance degradation (BER $= 1* 10^{-9}$) as a function of IF laser linewidth, for a 311 Mbit/s CPFSK receiver (modulation index $m = 1$).

Using the setup, we measured the performance degradation of a heterodyne CPFSK receiver due to the total laser linewidth of the transmitting laser and the local oscillator laser (Fig. 6). The results given in this figure are in perfect agreement with the results presented in [6].

VI. CONCLUSION

Using a programmable bit error rate tester is an attractive and simple alternative for a setup using frequency and phase locked synthesizers or lasers to generate CPFSK IF test signals. The feature that enables testing the IF-circuitry, without using optical sources and components is, especially, an advantage. This testing includes both the additive noise and the phase noise.

The method presented in this paper is rather simple, but is limited as well. There has to be a relationship between the send frequencies and the bit rate. Nevertheless, small modulation indexes can be produced, including $m = 0.5$. This latter is achieved by taking the lower frequency equal to the bit rate and the higher one 1.5 times the bit rate. In that case, some extra processing (bit sequence dependent phase reversals of the constituting signals) may be required to guarantee phase continuity. In a similar way schemes for $m = 0.66$ and $m = 0.75$ were developed.

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