A power-efficient, low-distortion variable gain amplifier consisting of coupled differential pairs

Brief Papers

A Power-Efficient, Low-Distortion Variable Gain Amplifier Consisting of Coupled Differential Pairs

Pieter J. G. van Lieshout and Rudy J. van de Plassche

***Abstract*— A variable gain amplifier incorporating a plurality of coupled differential pairs has been designed in a bipolar technology. By applying variable offset voltages to these differential pairs, the overall gain of the system can be varied. The linear input region is inversely proportional to gain, making the amplifier very well suited for automatic gain control circuits. Furthermore, the gain of the proposed amplifier is 0–25 dB, the signal bandwidth is 35 MHz, and the output IP3 is 24–30 dBm. It operates from a 5-V power supply and dissipates 40 mW. The active chip area is 0.15 mm^2 in a 1-μm bipolar technology.**

***Index Terms*— Bipolar, gain control, multi-tanh technique, transadmittance element, variable gain.**

I. Introduction

SUCCESSFUL implementations of variable gain amplifiers and, more general, multipliers were demonstrated throughout time [1], [2], [5], [6]. For use in automatic gain circuits, a linear input region inversely proportional to gain is an important feature [7].

This paper describes a variable gain amplifier, incorporating a plurality of differential pairs coupled in parallel, thus forming a transadmittance stage. The input of each differential pair is provided with the system input voltage, shifted by a certain offset voltage. The offset voltage of each individual differential pair is variable and can be different from other offset voltages. When all offset voltages are made equal, the transadmittance stage is set to maximum gain. The linear input region is now comparable to that of a single differential pair transadmittance stage. When the offset voltages are made equidistant, the distance being about 40 to 60 mV, the transadmittance stage is set to minimum gain. The linear input range has now increased compared to the situation of maximum gain and is dependent on the number of differential pairs. Gain settings between minimum and maximum gain can be achieved by values of equidistance of the offset voltages between 0 and 40 to 60 mV. First, the principle of coupled differential pairs will be further explained in Section II. Section III will then go into some circuit implementation details. Measurement results will be presented in Section IV. Finally, conclusions on this design will be drawn in Section V.

Manuscript received April 10, 1997; revised June 27, 1997.

P. J. G. van Lieshout was with Philips Semiconductors, 6534 AE Nijmegen, The Netherlands. He is now with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

R. J. van de Plassche is with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands.

Publisher Item Identifier S 0018-9200(97)08785-4.

II. System Architecture

A. Coupling of Differential Pairs

Systems incorporating a plurality of coupled differential pairs can be used to synthesize arbitrary transfer functions [3]. Fig. 1 shows an example of such a *multi-tanh structure*, here used as a variable gain amplifier. The transfer function of each individual differential pair DP_i can be shifted by varying the corresponding offset voltage ϕ_i. The overall output current $I_{\mathrm{out}} = I_{\mathrm{pos}} - I_{\mathrm{neg}}$ is the sum of the n individual output currents and can be written as

$$I_{\mathrm{out}}(V_{\mathrm{in}}) = \alpha_F I_{\mathrm{tail}} \sum_{i=1}^{n} \tanh \frac{V_{\mathrm{in}} - \phi_i}{2V_T} \tag{1}$$

where I_{tail} is the differential pair tail current, α_F is the ratio between collector and emitter current of the used transistors, and V_T is the thermal voltage. The transconductance follows by differentiating I_{out} to V_{in} in (1)

$$G_m(V_{\mathrm{in}}) = \frac{dI_{\mathrm{out}}}{dV_{\mathrm{in}}} = \frac{\alpha_F I_{\mathrm{tail}}}{2V_T} \sum_{i=1}^{n} \mathrm{sech}^2 \frac{V_{\mathrm{in}} - \phi_i}{2V_T}. \tag{2}$$

B. Offset Voltages

When all offsets ϕ_i are equal and have a value of zero, the transconductance will come to $n \cdot (\alpha_F I_t ail)/(2V_T)$ for $V_{\mathrm{in}} = 0$. So, the gain of the multi-tanh structure with n differential pairs, all with the same offset, is n times the gain of a single differential pair. When all offsets ϕ_i are taken equidistant according to a series (c.f. Fig. 2)

$$\phi_i = \frac{2i - 1 - n}{2} \cdot \Delta\Phi \quad \text{for } 1 \le i \le n \tag{3}$$

the transfer curves are spread evenly around $V_{\mathrm{in}} = 0$. When $\Delta\Phi$ is taken as zero, the case considered earlier arises. When $\Delta\Phi$ is increased, the transfer curves will move apart. The effect of this on the overall transconductance curve is that it gets wider and also lower, which shows the tradeoff between linear input region and gain.

When the transfer functions are shifted too much apart by making $\Delta\Phi$ too large, the tails of the individual transconductance curves will not compensate the tails of neighboring curves. The overall transconductance will start showing an unwanted variation as a function of V_{in}. There is a value of

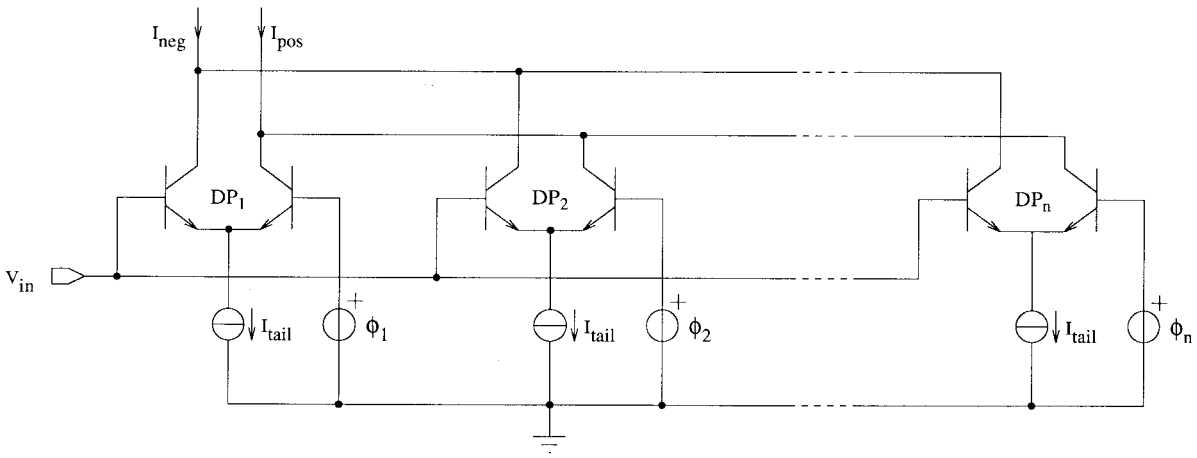

Fig. 1. System consisting of n coupled differential pairs.

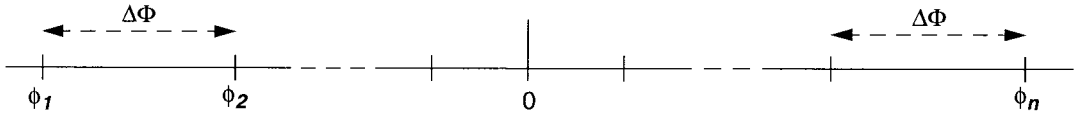

Fig. 2. Series of equidistant offset voltages.

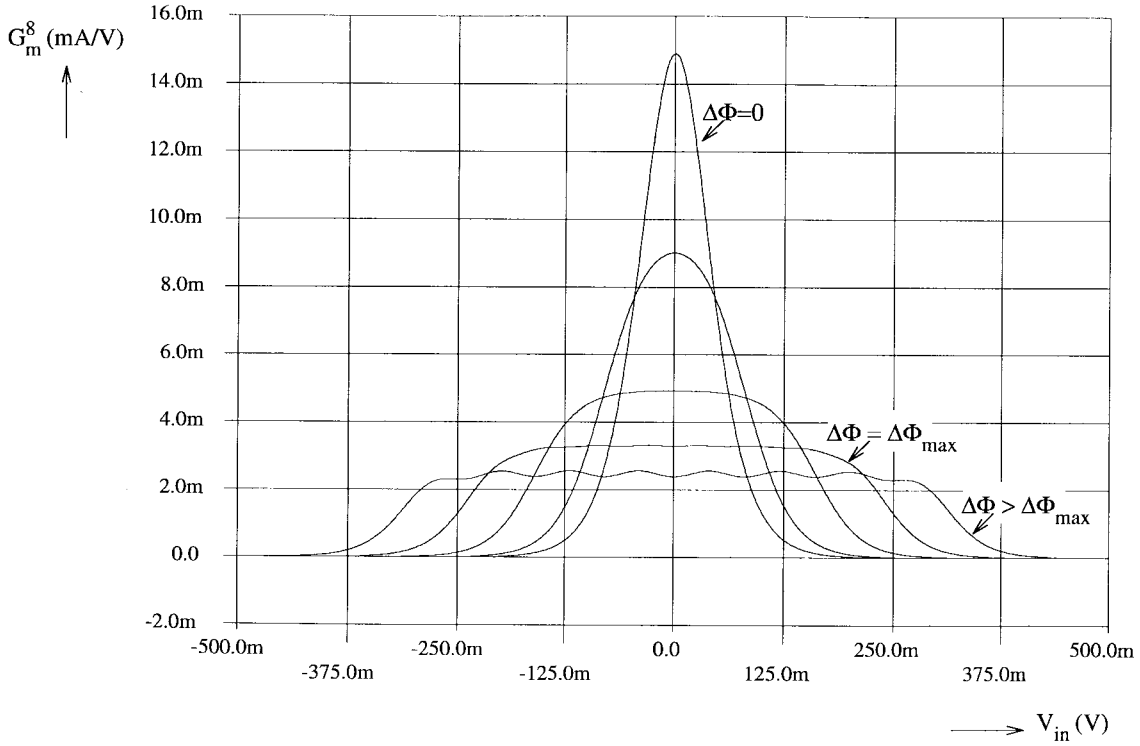

Fig. 3. Simulated transconductance versus input voltage of amplifier with eight parallel differential pairs.

$\Delta\Phi$, referred to as $\Delta\Phi_{\max}$, for which the transconductance characteristic is maximally flat. Raising $\Delta\Phi$ beyond this value will introduce a ripply nature in the transconductance characteristic. $\Delta\Phi_{\max}$ can be found after some extensive calculations [4]. It was found to be 40 to 60 mV, depending on the type of transistors used in the differential pairs. The value of the emitter series resistance, especially, is of great influence on the value of $\Delta\Phi_{\max}$ because of local feedback phenomena.

Fig. 3 shows transconductance versus input voltage for several values of $\Delta\Phi$ of a simulated system comprising eight differential pairs.

C. Overall Transconductance

To characterize the transconductance of the multi-tanh circuit, the value of G_m around $V_{\text{in}} = 0$ will be considered. This value is a function of the applied offset voltage $\Delta\Phi$, and of

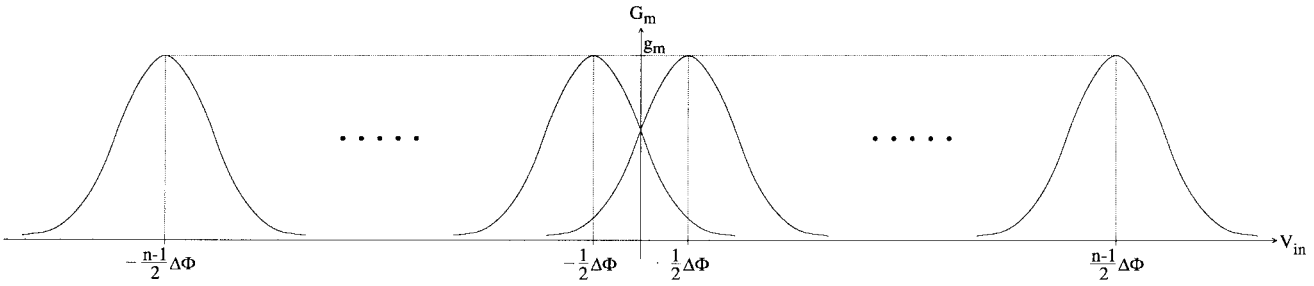

Fig. 4. Summing of transconductance functions.

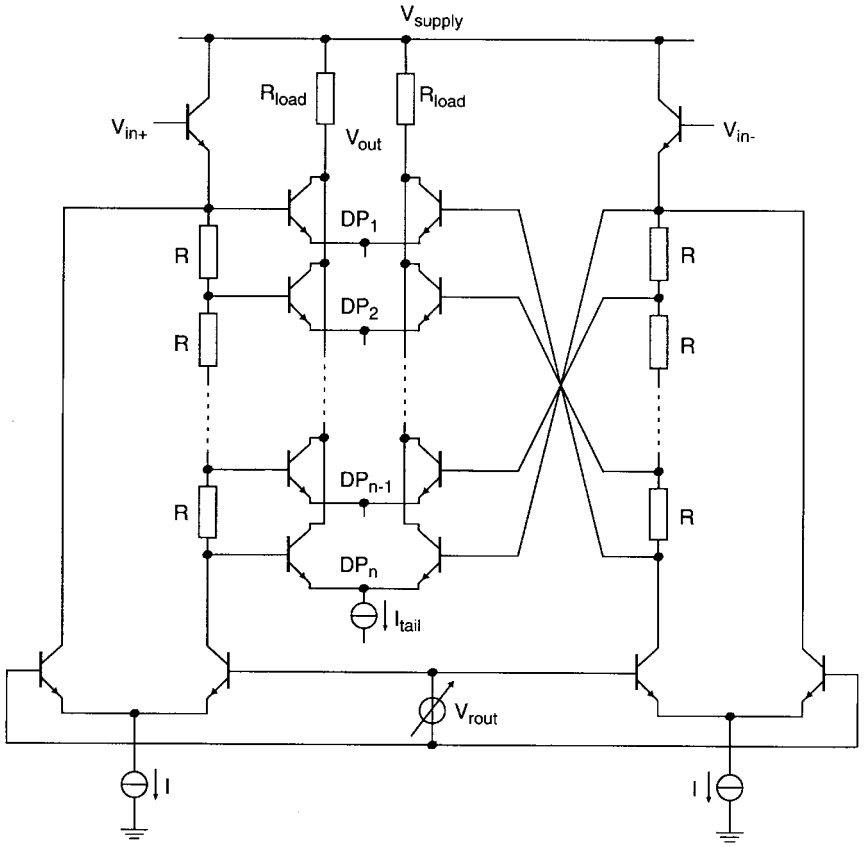

Fig. 5. Circuit diagram of complete variable-gain amplifier.

course of the number of pairs n and the transconductance g_m of these pairs. In the sequel, n is assumed to be even.

To calculate the gain around $V_{\text{in}} = 0$ for a given $\Delta\Phi$, Fig. 4 is considered. To $G_m(0)$, all differential pairs contribute. However, the contribution from the pairs operating around $V_{\text{in}} = 0$ is considerably larger than from pairs with large positive or negative offsets, whose only contributions are the asymptotic tails of their transconductance curve. After some manipulation, $G_m(0)$ can be written as a function of n and $\Delta\Phi$

$$G_m(0) = 2\sum_{i=1}^{\frac{n}{2}} g_m\left(\frac{(2i-1)\Delta\Phi}{2}\right) \tag{4}$$

where $G_m(\cdot)$ denotes the transconductance of the complete system and $g_m(\cdot)$ denotes the transconductance of a single differential pair, both as a function of input voltage.

D. Transconductance Range

From the previous, the gain range (the ratio between the gain for $\Delta\Phi = 0$ and $\Delta\Phi = \Delta\Phi_{\max}$) can be determined. For $\Delta\Phi = 0$, maximum gain is achieved. From (4) follows

$$[G_m(0)]_{\max} = G_m(0)|_{\Delta\Phi=0} = n \cdot \frac{\alpha_F I_{\text{tail}}}{2V_T} = n \cdot g_m(0). \tag{5}$$

Minimum gain is achieved when $\Delta\Phi = \Delta\Phi_{\max}$, where $\Delta\Phi_{\max}$ is about 50 mV. Applying this to (4) yields

$$[G_m(0)]_{\min} = G_m(0)|_{\Delta\Phi=50\,\text{mV}} \approx 2 \cdot \frac{\alpha_F I_{\text{tail}}}{2V_T} = 2 \cdot g_m(0). \tag{6}$$

The gain dynamic range (GDR) of the n-fold differential pair thus comes to

$$\text{GDR} = \frac{[G_m(0)]_{\max}}{[G_m(0)]_{\min}} \approx \frac{n}{2}. \tag{7}$$

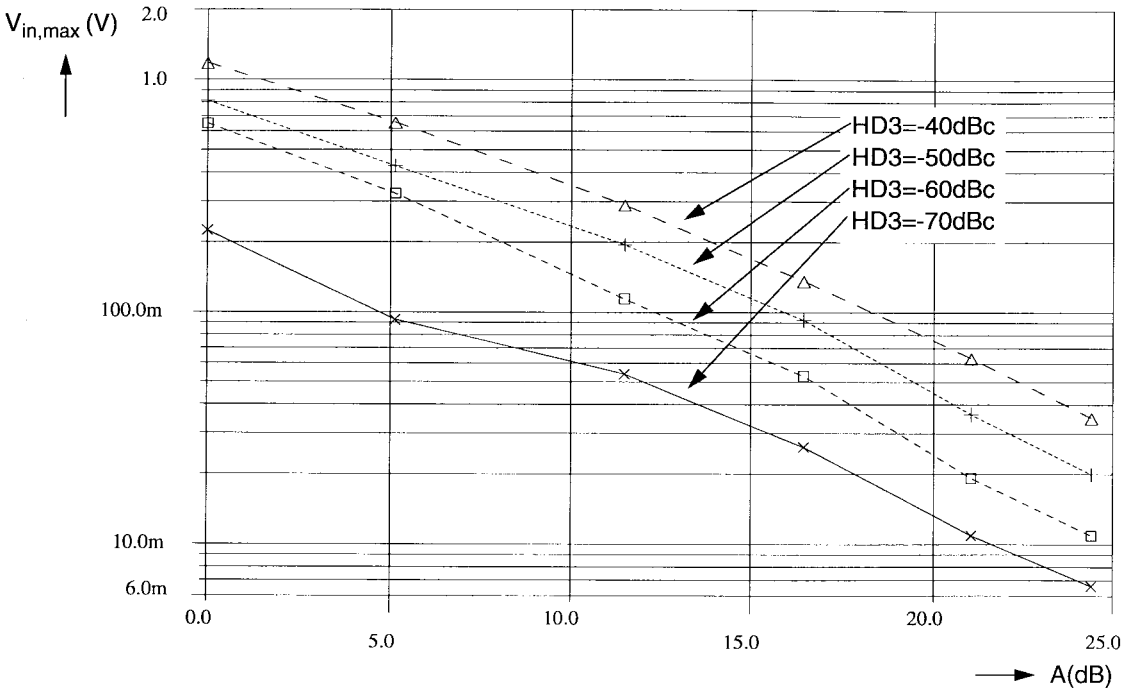

Fig. 6. Measured linear input region versus gain for several levels of HD3 at 10-MHz signal frequency.

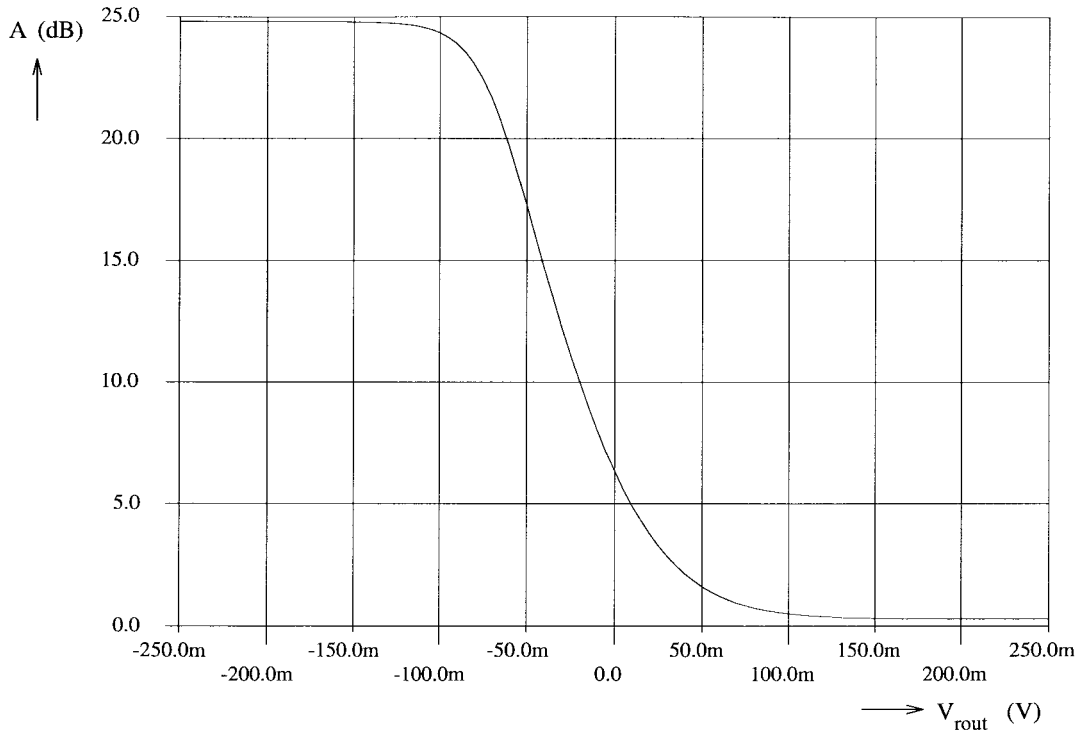

Fig. 7. Gain versus gain setting voltage.

So when, e.g., 32 differential pairs are used, the gain range will be about 16× (24 dB).

E. Distortion

The most important causes for distortion are as follows:

- global nonlinearity caused by the finite number of differential pairs and gradients in the series of offset voltages and tail currents;
- local nonlinearities caused by undesirable offsets in the differential pairs or deviations in the applied offset voltages;
- local nonlinearities caused by mismatch in the tail current sources.

In general, the first will cause lower order harmonic distortion, while the latter two will cause higher order harmonic distortion. From this, the importance of matching the differential

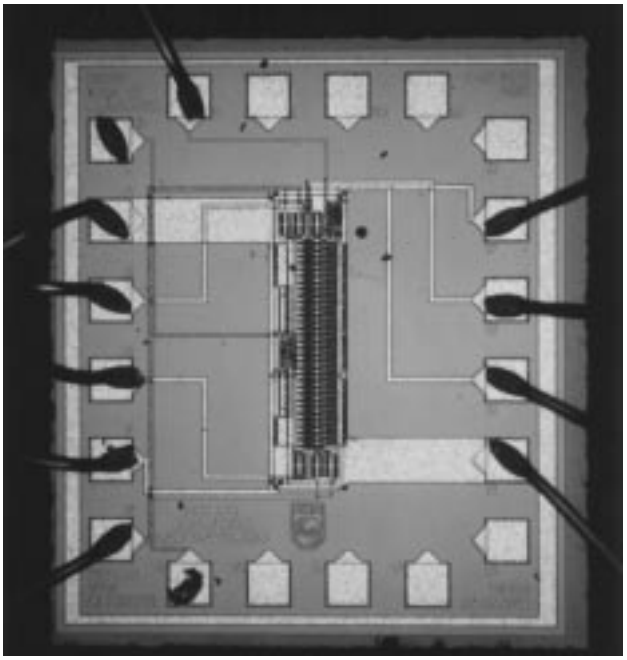

Fig. 8. Die micrograph of variable gain amplifier.

pairs, current sources, and offset voltage sources becomes clear.

F. Noise

The most important noise sources in the multi-tanh circuit are:

- differential pair transistors;
- tail current sources;
- offset voltage generation circuits;
- load resistors (which convert the system's differential output current to a voltage).

It can be shown that the first and last noise sources are dominant. Worst-case condition with respect to noise appears when the gain is set to minimum. At maximum gain, all differential pairs are effectively put in parallel, reducing the total noise by a factor $\sqrt{n}$ compared to the noise of a single differential pair. When the noise of the load resistors is transformed to the input, it gets divided by the gain of the amplifier, making maximum gain best-case for this noise source also. For the realized chip with 32 differential pairs, the equivalent input noise voltage at minimum gain is about four times higher than at maximum gain.

In an automatic gain control system, signal-to-noise ratio benefits from this dependency of noise on gain, because then both noise and signal level are inversely proportional to gain.

III. Variable Gain Amplifier Implementation

A circuit diagram of the complete variable gain amplifier is shown in Fig. 5. The next paragraphs will describe some design aspects in more detail.

Each of the differential pairs has to be supplied with a shifted version of the input signal. The amount of shift, the offset voltage, should be adjustable and should be according to (3). Fig. 5 shows the offset generation circuits with one differential input voltage and 32 differential output voltages at the left and right of the differential pairs. The circuit consists of two emitter followers, each loaded with a resistor ladder. The current through the ladders can be adjusted between zero and a certain maximum voltage by means of the current routers at the bottom of the ladders.

The top of each ladder is connected to the output of the emitter follower. The voltage at this node is a level-shifted copy of the input voltage. The current through the resistor ladder determines the voltage drop between two subsequent ladder taps. This way, a series of level-shifted copies of the input voltage is created. The current router makes sure the emitter follower remains biased at the same current, independent of the gain setting.

The ladder taps are connected to the bases of the differential pair transistors, causing a small base current to flow out of each of the taps. This causes the current through the ladder to increase toward the top, thus increasing the distance between the ladder tap voltages. By cross-coupling the differential pairs between the two ladders, this effect is compensated. However, it still is a cause for nonlinearity and the best way to prevent it is by making the ladder resistors low-impedant at the expense of a larger current consumption.

The maximum current through the ladders, together with the value of the ladder resistors, determines the maximum voltage drop across the resistors. Because of the differential topology, two resistors, one from each ladder, both contribute $\Delta\Phi/2$ to the total offset voltage $\Delta\Phi$.

The rest of the circuit implementation is straightforward. The differential pairs are biased by a rail of current sources. The collectors of the differential pair transistors are connected to a pair of load resistors. The differential output voltage is not buffered, which causes the bandwidth to be limited because of package parasitics.

TABLE I
Variable Gain Amplifier Specifications

Technology	1 μm bipolar (3 metal layers)
Bandwidth (-3 dB)	$>$35 MHz
Gain range	25 $\cdots$ 0 dB
Output IP3	24 $\cdots$ 30 dBm
Equivalent input noise	1.6 $\cdots$ 6.4 nV/$\sqrt{\text{Hz}}$
Supply voltage	5 V
Power dissipation	40 mW
Active chip area	0.15 mm^2

IV. Measurement Results

A prototype variable gain amplifier has been made in a 1-μm triple-metal bipolar process. It contains 32 parallel differential pairs and has a differential voltage input as well as output. The gain range is 0–25 dB. A photograph of the chip is shown in Fig. 8. Active chip area is 0.15 mm^2. Power dissipation is 40 mW at a supply voltage of 5 V. Signal bandwidth is about 35 MHz, determined by package parasitics loading the unbuffered outputs. For a signal frequency of 10 MHz, distortion measurements were performed. Fig. 6 shows the results of these measurements. The curves show

the maximum input voltage level as a function of gain for HD3-values between -40 dBc and -70 dBc. Fig. 7 shows the relation between the differential gain setting voltage $V_{\rm rout}$ and the resulting gain A. The transfer from $V_{\rm rout}$ to $\Delta\Phi$ is a tanh-function and the transfer from $\Delta\Phi$ to A (dB) is a hyperbolic function. Table I, finally, gives an overview of the specifications of the variable gain amplifier.

V. Conclusion

A variable gain amplifier, incorporating a plurality of coupled differential pairs, has been presented. It shows a linear input region inversely proportional to gain, making it well suited for use in automatic gain control systems. It shows good linearity and low noise levels. Amplifier topology is simple and the gain range can be adapted to other values by changing the number of differential pairs.

References

[1] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. SC-3, pp. 365–373, Dec. 1968.

[2] ———, "A new technique for analog multiplication," *IEEE J. Solid-State Circuits*, vol. SC-10, pp. 437–447, Dec. 1975.

[3] ———, "Circuits for the precise synthesis of the sine function," *Electron. Lett.*, vol. 13, no. 17, pp. 506–508, Aug. 1977.

[4] W. D. Mack, "Wideband transconductance amplifiers," Master of Science Report, Berkeley: University of California, Berkeley, USA, 1979.

[5] W. M. C. Sansen and R. G. Meyer, "An integrated wideband variable-gain amplifier with maximum dynamic range," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 159–166, Aug. 1974.

[6] R. G. Meyer and W. D. Mack, "A DC to 1-GHz differential monolithic variable gain amplifier," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1673–1680, Nov. 1991.

[7] M. W. Hauser, "Large-signal electronically variable gain techniques," Master of Science Report, Massachusetts Institute of Technology, Cambridge, Dec. 1991.