A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF

A Sixth-Order Continuous-Time Bandpass Sigma–Delta Modulator for Digital Radio IF

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***Abstract*— This paper presents a sixth-order continuous-time bandpass sigma–delta modulator (SDM) for analog-to-digital conversion of intermediate-frequency signals. An important aspect in the design of this SDM is the stability analysis using the describing function method. Key to the analysis is the extension of the linear gain model for the sampled quantizer with a phase uncertainty. The single-loop, one-bit SDM is tuned at 10.7 MHz, is sampled at 40 MHz, and achieves 67-dB signal-to-(noise + distortion) ratio in 200 kHz and 80 dB in 9 kHz. The third-order intermodulation is at −82 dBc for a −13-dBFS input level. The 0.5-μm CMOS chip occupies 0.9 × 0.4 mm^2 and consumes 60 mW at 3.3 V (digital) and 5.0 V (analog). The sample frequency is variable and can be set from 30 to 80 MHz.**

***Index Terms*— Analogue, data conversion, digital conversion, receivers, sigma–delta modulator (SDM), stability criteria.**

I. Introduction

SIGMA–delta modulation [1], [2] has become a widely applied technique for high-performance analog-to-digital (A/D) conversion of narrow-band signals. Through the use of oversampling and negative feedback, the quantization errors of a coarse quantizer are suppressed in a narrow signal band in the output of the modulator. Bandpass sigma–delta modulation [3]–[7] is well suited for A/D conversion of narrow-band signals modulated on a carrier, as occur in communication systems such as AM/FM radio receivers.

A/D conversion of intermediate-frequency (IF) signals moves the IF signal-processing stage of receivers to the digital domain, thus providing more flexibility, better noise immunity, and potential improvements in performance and power consumption by scaling of the technology.

A typical digital IF architecture for a broadcast radio receiver using a sigma delta modulator (SDM) is shown in Fig. 1. The receiver consists of a low-noise amplifier (LNA) followed by a wide-band bandpass filter. A mixer converts the signal to the IF frequency of 10.7 MHz using a tunable local oscillator (LO). For FM signals (88–108 MHz), the mixer performs a common downconversion; in the case of AM signals (520–1650 kHz), the mixer performs an upconversion. This configuration allows a single (ceramic) surface acoustic wave filter for channel selection for both AM and FM signals. The filter is followed by an automatic gain control (AGC) amplifier, which feeds the signal to the SDM. Additional filtering, final channel selection, and demodulation of the signals is done by a digital signal processing (DSP) unit. The demodulated signal is passed to the digital-to-analog converter (DAC) and made audible by a power amplifier (PA) followed by a loudspeaker.

The requirements for the SDM are determined by its input signal characteristics. For FM and AM broadcast radio receivers, a dynamic range (DR) of 65 and 90 dB, respectively, is desirable. Preferably, the SDM should achieve this DR at low input signal levels to alleviate the requirements for the AGC. The ceramic filter has a fixed bandwidth of approximately 200 kHz, corresponding to a single channel for FM signals. For AM signals, the typical carrier spacing is 9 kHz, and the filter feeds several channels to the AGC and SDM. The A/D conversion of the *multichannel* AM signals places stringent requirements on the linearity of the SDM in order to avoid intermodulation distortion of adjacent channels.

II. Modulator Architecture

The theoretically achievable signal-to-noise ratio (SNR) and dynamic range of an SDM depends on the order N of the loop filter, the resolution B of the quantizer, and the oversampling ratio (OSR), which is defined as half the sample frequency $f_s/2$ divided by the signal bandwidth BW. As high-order (>4) single-loop bandpass SDM's exhibit signal-dependent stability, multibit quantizers and/or multistage (MASH) architectures are often used to increase the SNR of low-order SDM's. However, both solutions suffer from performance degradation due to mismatch of, for example, quantization levels. The required accuracy of the intermediate quantizer levels of a multibit quantizer is very high as mismatch introduces nonlinear distortion. Note that mismatch of the quantization levels of a one-bit quantizer only results in a gain-mismatch and a dc offset, which are linear deviations. Mismatch of loop filter transfer functions in a MASH structure causes imperfect cancellation of the quantization errors of the first lower order loop. A part of the low-order noise-shaped quantization errors leaks to the output of the SDM, thus reducing the SNR. For reason of the required linearity, a single-loop one-bit modulator architecture is chosen here (see Fig. 2).

In order to achieve the required DR, our SDM uses a sixth-order loop filter. The loop filter uses continuous-time (CT) circuitry, which has several advantages over a switched-

Manuscript received April 13, 1999; revised July 8, 1999.

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Publisher Item Identifier S 0018-9200(99)08978-7.

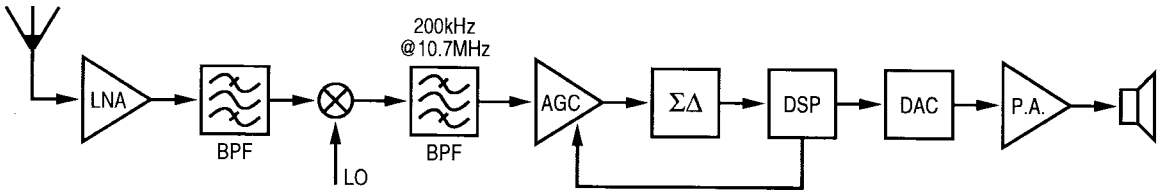

Fig. 1. A typical digital IF radio receiver using a $\Sigma\Delta$ modulator.

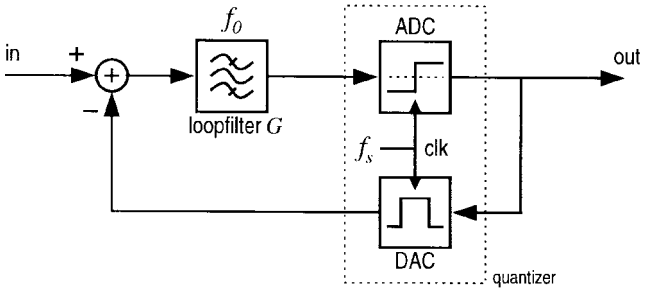

Fig. 2. A one-bit single-loop bandpass $\Sigma\Delta$ modulator.

capacitor (SC) implementation. First, the clock feedthrough and settling errors of the sampler are also suppressed by the feedback loop as the sampler is placed between the loop filter and ADC inside the loop. Second, a CT circuit can operate at higher frequencies, as the sample frequency f_s is not limited by charge transfer accuracy requirements. Third, the tuning frequency of a CT filter does not depend on the sample frequency. The filter can be easily tuned and set to a frequency other than $f_s/4$ to prevent aliasing of the third-order harmonic distortion component at $3f_s/4$ into the signal band, without requiring additional circuitry.[1] As a result, the sample frequency can be determined by the requirements for the DSP unit. A disadvantage of using a CT loop filter is the increased sensitivity to clock jitter of the feedback DAC.

In the case of such a high-order one-bit SDM, the design of the CT loop filter transfer function $G(p)$ is mainly determined by the signal-dependent stability of the SDM. As the loop of the SDM is sampled by the quantizer, the stability of the loop can be analyzed in discrete-time (DT) domain. The (sampled) response of the CT loop filter $G(p)$ to the pulse shape $R(p)$ of the quantizer DAC can be replaced by an equivalent DT loop filter $G_{\rm eq}(z)$, and the loop filter transfer function design can be done in the DT domain (invariant impulse response method) [8], [9]. While the poles of the loop filter ensure high in-band gain, the zeros of the DT loop filter determine the SDM's stable operating range. Locating the zeros near the poles results in a loss of performance, but placing the zeros too far away from the poles results in unstable behavior, even at low input amplitudes.

III. Stability Analysis

With respect to the SDM, the concept of stability needs some explanation, as it differs from linear systems. Commonly, stability refers to the boundedness of states of a system. Consequently, constant-amplitude oscillations (resulting from limit cycles) are considered stable behavior. This definition is unsuitable for SDM's as some constant-amplitude oscillations are tolerated (namely, "idle patterns") whereas other oscillations are considered "unstable" behavior as they effectively disable the noise shaping behavior. Limit cycles resulting in a small amplitude (quasi-) periodic signal at the output of the loop filter are easily disturbed by an input signal applied to the SDM and are called idle patterns. In contrast, a limit cycle will be called a "large signal limit cycle" when it results in a large amplitude at the output of the loop filter and cannot be disturbed easily by an input signal. Here, an SDM will be called stable when (for a certain class of input signals) the states of the SDM are bounded and the SDM is free of large signal limit cycles.

Design rules for the stability of high-order SDM's such as Lee's rule [10] are often based on an intuitive model combined with empirical results. Here, we analyze the stability of the SDM using the describing function method, in which the nonlinear quantizer is modeled by a quasi-linear, signal-dependent transfer [11]. The quantizer model should be adequate for an accurate stability analysis. Commonly, the one-bit quantizer is modeled by a linear, signal-dependent gain [12], [13]. However, when using this model, the describing function method fails to predict small-signal stability issues such as idle patterns and instability under zero-input and zero-initial state conditions. For example, a second-order low-pass modulator exhibits an idle pattern with a frequency of $f_s/4$, whereas the describing function method predicts a frequency of $f_s/2$ [14]. Therefore, the commonly used "linear signal gain" model for a one-bit quantizer is extended with a phase shift. The gain results from the variable input and fixed output amplitude of the quantizer. The phase shift is in fact a phase uncertainty and represents the inaccuracy in time with which the zero-crossings of the quantizer input signal are detected. Sampling of the input signal causes a zero crossing to be detected by the sample moment following this crossing. As the zero crossing could have occurred anywhere within the previous sample period, an uncertainty in the phase transfer of the signal is introduced [15]. Fig. 3 shows an example in which an input signal with frequency $f_s/4$ (solid line) is shifted in phase without changing the output samples of the quantizer (denoted by impulses).

In Appendixes I and II, it is shown that adding this phase uncertainty to the quantizer model improves the stability analysis and allows calculation of a small-input stability boundary on the location of the zeros of the loop filter transfer function. Choosing the zeros near this boundary optimizes the dynamic range of the SDM [14].

[1] In the case of a DT filter, half of the filter coefficients is zero when the filter is tuned at $f_s/4$ and does not have to be implemented.

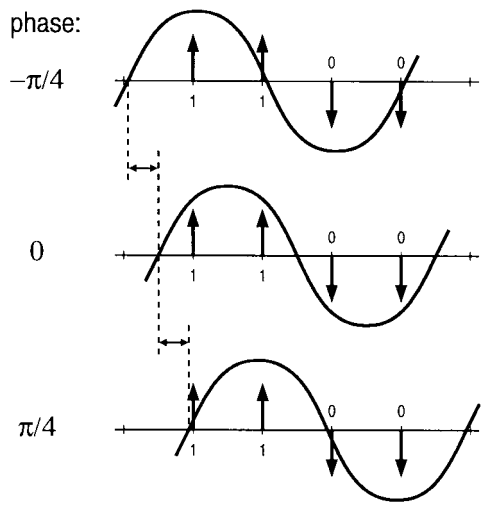

Fig. 3. Phase uncertainty of a one-bit quantizer with $f_{in} = f_s/4$.

IV. Discrete-Time Design

As mentioned in Section II, the design of the loop filter will start in the discrete-time domain. For the sixth-order bandpass SDM, the "equivalent" DT loop filter transfer function is chosen from the class of bandpass loop filters described in Appendix II

$$G_{\rm eq}(z) = \frac{(1+ac^{j\theta_0}z^{-1})^3(1+ae^{-j\theta_0}z^{-1})^3}{(1+e^{j\theta_0}z^{-1})^3(1+e^{-j\theta_0}z^{-1})^3} - 1 \quad (1)$$

in which θ_0 represents the normalized angular tuning frequency. With a tuning frequency of 10.7 MHz, the sample frequency is set to 40 MHz, which gives an oversampling ratio of 100 for a bandwidth of 200 kHz (FM signals) and a tuning frequency of $\theta_0 = 1.681$. The parameter a determines the location of the zeros and provides the tradeoff between stability and performance. For $a = 0$, this modulator is unstable, even for zero-input and zero-initial state conditions. For $a \approx 1$, the modulator is stable, but the in-band loop gain is low and the quantization noise is not shaped significantly. According to the analysis in Appendix II (Fig. 23), the loop filter parameter a should satisfy $a > 0.68$ for small-signal stability when $\theta_0 = 1.681$ and the order is six. In order to allow stable operation at an acceptable input signal amplitude level and provide a safety margin for implementation tolerances, a is set to $a = 0.75$. Simulations show that the maximum stable input amplitude equals $A_{\max} = -6.6$ dB relative to the DAC output power (see Fig. 2). Simulations predict a maximum SNR of 93 dB in a bandwidth of 200 kHz.

V. Continuous-Time Design

Now that the equivalent DT transfer function has been designed, the corresponding CT loop filter transfer function can be found by means of the invariant impulse response transformation. The equivalent DT transfer function $G_{\rm eq}(z)$ designed in the previous section depends on the sampled response of the CT loop filter transfer function $G(p)$ to the pulse shape $R(p)$ of the DAC (see Fig. 4). As sampling can be represented mathematically by multiplication with a sum of time-shifted Dirac pulses (δ) [16], the equivalent DT loop filter can be written as

$$G_{\rm eq}(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\{G(p)R(p)\} \cdot \left(\sum_{k=0}^{\infty} \delta(t - kT_s)\right)\right\} \quad (2)$$

in which $\mathcal{Z}$ represents the z-transform and $\mathcal{L}^{-1}$ the inverse Laplace transform. Writing the multiplication in the time domain as a convolution in the frequency domain and applying $z = e^{pT_s}$ gives

$$G_{\rm eq}(z) = \frac{1}{2\pi j}\int_{c-j\infty}^{c+j\infty} \frac{G(s)R(s)}{1 - e^{sT_s}e^{-pT_s}}\, ds\bigg|_{z=e^{pT_s}}. \quad (3)$$

This integral can be solved using the residue theorem of Cauchy [17]. Note, however, that we are trying to find the CT transfer function $G(p)$ from (3) for a given $G_{\rm eq}(z)$. As the inverse of the transformation described by (3) does not have a unique solution, a suitable CT loop filter prototype should be used to solve (3). In order to result in the desired DT transfer function $G_{\rm eq}(z)$, the CT loop filter prototype should have a filter structure that provides sufficient degrees of freedom for the placement of the poles and zeros of the CT (and DT) transfer function.

The loop filter structure of the sixth-order bandpass SDM is based on a cascade of resonators (see Fig. 5). Three resonators realize the complex conjugate poles for the passband of the filter. Six feed-forward paths provide sufficient degrees of freedom to place the five zeros of the equivalent DT transfer function independently. The resonators should have current inputs to simplify the summing nodes within the filter and voltage outputs such that the coefficients in the feed-forward paths can be realized by resistors (R_1 to R_6). The coupling resistors R_{c1} and R_{c2} are used for scaling the voltages within the filter to the same level. In the case that the quality factor of the resonators is high (i.e., $Q > 100$), the transfer function of the loop filter of the SDM can be written as

$$G(p) = \omega_0 \frac{N(p)}{(p^2 + p\omega_0/Q + \omega_0^2)^3} \quad (4)$$

with $\omega_0 = 2\pi f_0 = 2\pi \cdot 10.7$ MHz and

$$N(p) = c_2p^5 + \omega_0(c_1 + c_4)p^4 + \omega_0^2(2c_2 + c_3 + c_6)p^3 + \omega_0^3(2c_1 + c_4 + c_5)p^2 + \omega_0^4(c_2 + c_3)p + \omega_0^5c_1. \quad (5)$$

The coefficients $c_1, \ldots, c_6$ are defined by

$$\begin{aligned} c_{1,2} &= R/R_{1,2} \\ c_{3,4} &= R^2/R_{c1}R_{3,4} \\ c_{5,6} &= R^3/R_{c1}R_{c2}R_{5,6} \end{aligned} \quad (6)$$

in which R is the resistor used in the resonator (see below). As the coefficients depend on the ratio of resistive values, an accuracy of $\pm 1\%$ can be achieved and no tuning or trimming is required for the feed-forward resistors.

The DAC uses a $T_s/4$-delayed return-to-zero (RTZ) pulse shape with a duration of $T_s/4$ for minimizing intersymbol distortion and for reducing signal-dependent jitter of the quantizer. The Laplace transform of the DAC pulse is given by

$$R(p) = e^{-pT_s/4}\frac{1 - e^{-pT_s/4}}{p}. \quad (7)$$

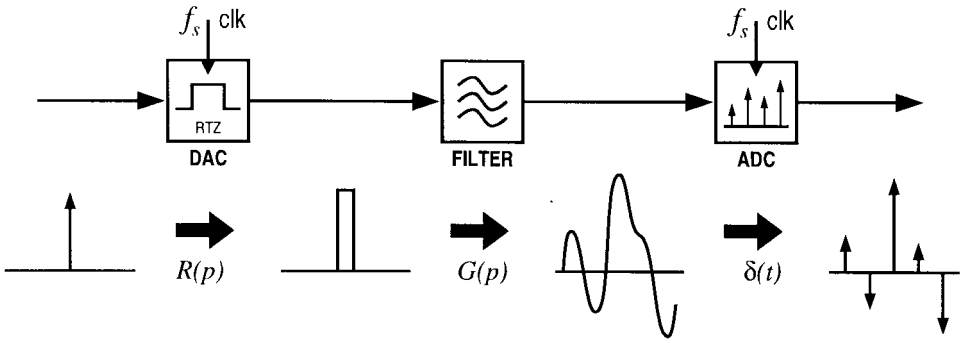

Fig. 4. Sampled impulse response of the pulse shaping DAC followed by a CT loop filter.

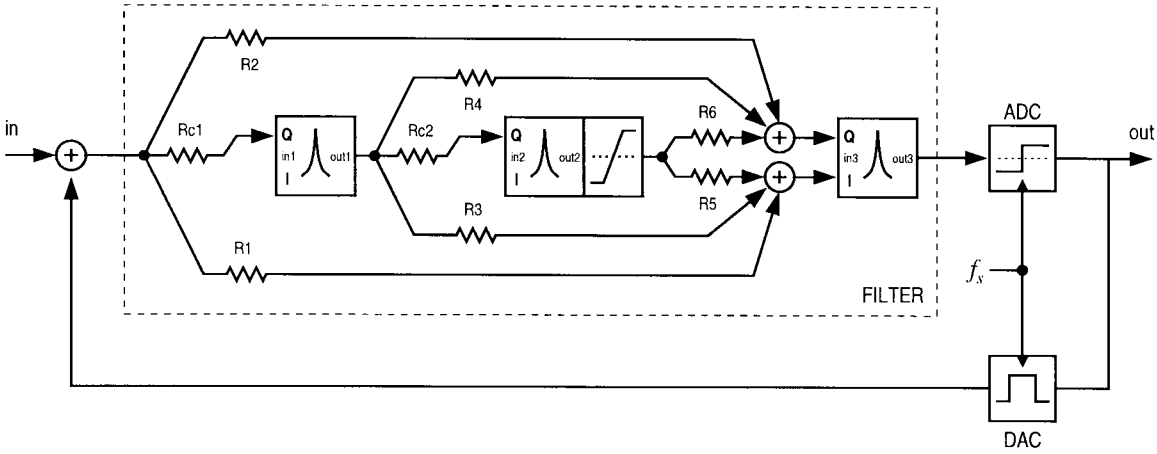

Fig. 5. Diagram of the sixth-order bandpass SDM.

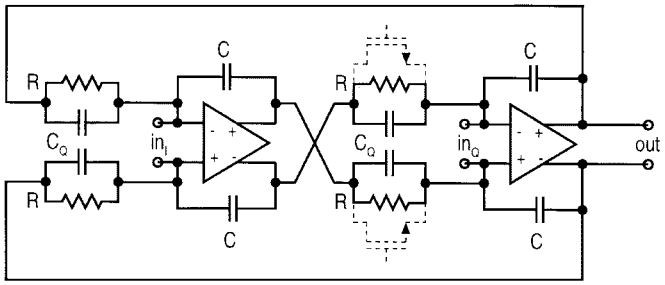

Fig. 6. Balanced integrator resonator. Tuning transistors are dashed.

By substituting (4), (5), (7), and (1) into (3) the coefficients $c_1, \ldots, c_6$ and thus $G(p)$ can be solved

$$c_1 = -1.339 \quad c_2 = 1.000$$
$$c_3 = -0.413 \quad c_4 = 0.314$$
$$c_5 = -0.041 \quad c_6 = 0.035. \tag{8}$$

In order to ensure stability at large input signal amplitudes, the output of the second resonator is limited, as is indicated in Fig. 5. When the limiter is active, the effective order of the loop filter is reduced and stable operation is ensured while degrading the performance of the SDM gracefully [18].

VI. Implementation

The resonators of the loop filter use balanced integrators, as shown in Fig. 6. The balanced integrator has a large linear output range, and parasitic capacitances to the substrate have little influence as the integrating capacitors are placed in feedback. The tuning frequency equals $\omega_0 = 2\pi/RC$. As the tuning frequency is fixed, a choice for R automatically determines C. The choice for the value for R allows a tradeoff between power consumption and noise as it determines the value of all resistors in the filter. Here, the value is set to $R = 24$ kΩ. The resulting nominal values of the components are listed in Table I. Two transistors are placed in parallel to the resistors to provide the required tuning mechanism. In order to assess the amount of nonlinear distortion introduced by these transistors, two versions of the SDM were made: with and without the tuning transistors. The capacitors C_Q limit the quality factor of the resonator. The balanced implementation allows easy implementation of negative coefficients by simply reversing positive and negative terminals. The ADC and DAC of the quantizer are also fully differential, improving the noise and distortion immunity. The supply voltage is 3.3 V for the digital part and 5 V for the analog sections. The common-mode dc level of the signals is 3 V, and the amplitude is 3 V_{pp} maximally.

TABLE I
Nominal Component Values

R	=	24kΩ	R_2	=	48kΩ	R_6	=	695.66kΩ
C	=	0.62pF	R_3	=	116.16kΩ	R_{c1}	=	24kΩ
C_Q	=	3.88pF	R_4	=	152.8kΩ	R_{c2}	=	48kΩ
R_1	=	35.84kΩ	R_5	=	579.72kΩ			

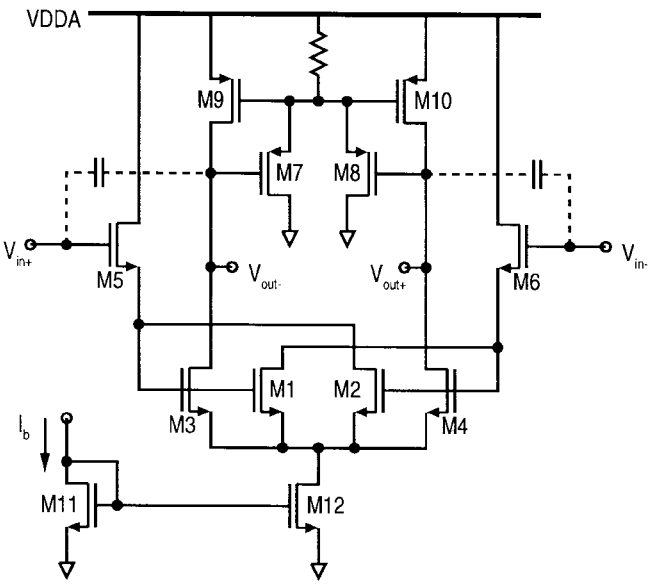

Fig. 7. Transconductance amplifier.

The key aspects of the design of the amplifiers of the resonator are the gain and the delay. A reasonable gain is required to prevent deterioration of the overall filter transfer characteristic. The delay of the amplifier should be small to prevent the resonator from oscillating. For these reasons, the single-stage transconductance amplifier of Fig. 7 is used [19]. The (negative) impedance of the cross-coupled transistors M1 and M2 together with the input pair M5 and M6 increase the voltage swing on the gates of the differential pair formed by M3 and M4. The overall transconductance is increased without seriously affecting the delay. The transistors M7 and M8 provide the common-mode feedback. The amplifier consumes 1 mA and has a gain-bandwidth product of 1.1 GHz. The (simulated) equivalent input noise power density of the filter at the tuning frequency equals $8.4 \cdot 10^{-8}$ V/$\sqrt{\text{Hz}}$. Combined with a quantizer output power of -3.5 dBm[2] (see below), the noise of the filter results in a maximum achievable SNR of 72 dB in 200 kHz. Due to the high Q of the resonators, the noise caused by the filter will exceed the theoretical quantization noise and serve as a dither signal for the SDM.

The performance of the one-bit ADC of the quantizer is mainly determined by the offset voltage and bit error rate of the comparator used. The bit error rate is related to the meta-stability of the comparator: when the input signal of the comparator decreases, the decision time of the comparator increases. This may cause erroneous decisions by the comparator. Note that the delayed RTZ pulse shape of the DAC alleviates this problem as more decision time for the ADC is allowed. The quantizer ADC (see Fig. 8) consists of two flip-flops in a master–slave configuration that reduces the bit error rate without increasing the parasitic load on the filter. The master flip-flop consists of two cross-coupled transistors (M8, M9) and contains two diodes (M6, M7) for limiting the voltage swing and increasing the speed of the comparator. Two nonoverlapping clock signals are generated internally by dividing the external clock. A low offset voltage of the comparator is achieved by a separate input gain stage (M1, M2). The input stage is disabled by transistor M3 during latching to prevent input-signal-induced switching of the master flip-flop.

The DAC of the quantizer is shown in Fig. 9. It consists of a logic block to create RTZ signals, a cascoded differential stage (M1–M4), and two source followers (M7, M8). Two dummy transistors (M5–M6) are added to the differential stage to reduce glitches caused by charge storage. The RTZ pulses of the quantizer DAC have a width of $T_s/4$ and an amplitude of 1.2 V_{pp} which gives -3.5 dBm. The resulting maximum differential input voltage is 200 mV_{pp}.

The loop of the SDM was closed off-chip to allow detailed measurements. The summing node at the input of the SDM (see Fig. 5) operates in voltage mode and is implemented by a single transconductance amplifier (similar to Fig. 7) with an external feedback resistor and two input resistors (also external) connecting the SDM input signal and DAC feedback signal.

In order to monitor the individual outputs of the resonators in the loop filter, three analog buffers are also included in the design of the SDM. Both the tunable and nontunable versions of the SDM are realized in 0.5-μm double-poly CMOS. A die photograph is shown in Fig. 10. The total chip area including bondpads measures 1.8×1.0 mm^2. The core circuit (analog filter, ADC, and DAC) measures 0.9×0.4 mm^2 and consumes 60 mW at a sample rate of 40 MHz. The digital buffers consume 9.5 mW at 40 MHz with a load capacitance of 8 pF. The analog buffers, required for testing purposes only, consume 117 mW. The total power consumed by the chip equals 186.5 mW at 40 MHz. As most of the power is consumed by the analog filter and the output buffers, the sample frequency is insignificant for the total power consumption.

VII. Measurements

As the tuning frequency and sample frequency are not coupled, the sample frequency is variable and can range from 30 to 80 MHz. For this sample frequency range, the SDM was free of large signal limit cycles (as expected), and the performance (in terms of SNR and distortion) remained constant (within 0.5 dB). This observation confirms the assumption that the SNR performance is limited by thermal noise. Unless stated otherwise, a sample frequency of 40 MHz was used for the measurements.

The typical tuning frequency of the filter of the nontunable version is 9.15 MHz. The designed and measured transfer characteristics of a single resonator of the tunable version is shown in Fig. 11 when tuned at 10.7 MHz. The measured amplitude and phase characteristics show little deviation from the designed response. The parasitic delay caused by the poles of the transconductance amplifier increases the quality factor of the resonators from the designed value of $Q = 100$ to $Q = 180$. The total filter transfer is shown in Fig. 12. The measured amplitude response shows a loss of gain owing to the fact that the three resonators do not have an identical tuning frequency: the amplitude response of the filter shows two local

[2]Here, 0 dBm refers to the *voltage* that gives 1 mW across 50 Ω. Actual impedance levels may vary.

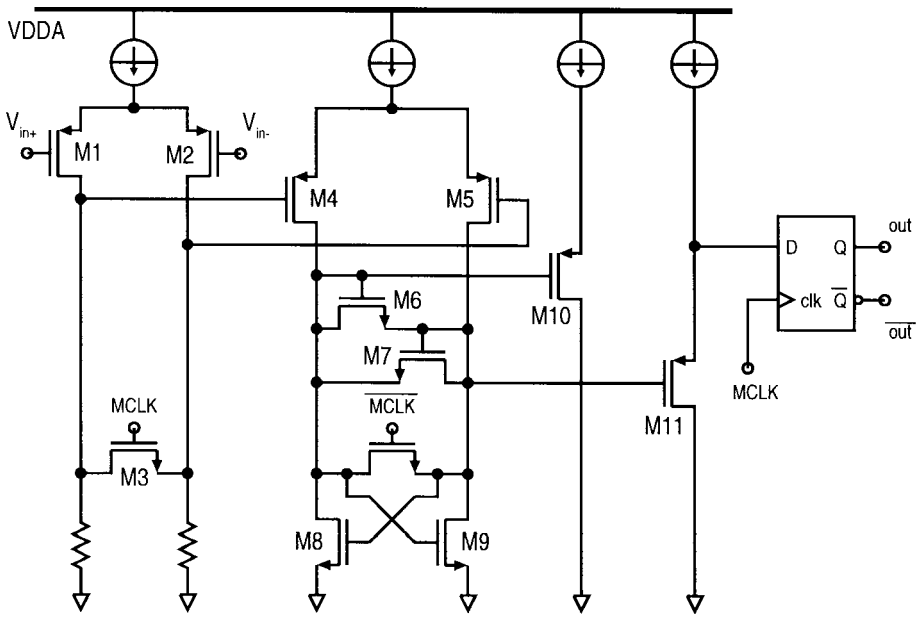

Fig. 8. One-bit ADC.

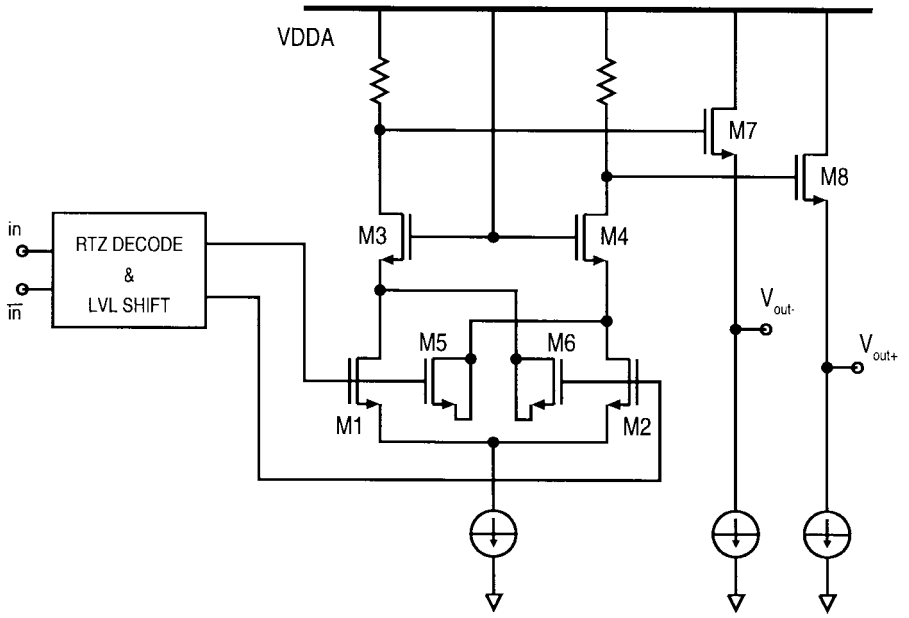

Fig. 9. One-bit DAC.

maxima in passband. The phase response of the loop filter agrees with the designed characteristic. This is important as the phase characteristic of the loop filter mainly determines the stability of the modulator.[3]

Typical output spectra of the nontunable and tunable SDM are shown in Figs. 13 and 14, respectively. The spectrum of the tunable version not only shows a higher noise floor than the output spectrum of the nontunable version but also shows larger distortion components near 1 and 19 MHz. The nonlinearity of the tuning transistors in the resonators clearly introduces additional distortion that affects the performance of the SDM.

[3]The quantizer provides a variable signal gain.

The nontunable version has an idle channel noise of -78.5 dBm in 200 kHz and -92.5 dBm in 9 kHz, resulting in DR of 72 dB and 86 dB, respectively. Fig. 15 shows the signal-to-(noise + distortion) ratio (SNDR) versus input power characteristic. At an input of -6 dB relative to the DAC output power (full scale), the maximum SNDR is 67 dB in 200 kHz and 80 dB in 9 kHz, giving an effective number of bits of 10.8 and 13 bits, respectively. The performance of the tunable version is slightly less with a DR of 67 dB (200 kHz) and 81 dB (9 kHz) and an SNDR of 63.5 and 76 dB, respectively.

In order to determine the third-order intermodulation distortion (IM3), a two-tone measurement is performed. Two input signals ("carriers") with frequencies $f_0 - \Delta f$ and $f_0 - 2\Delta f$

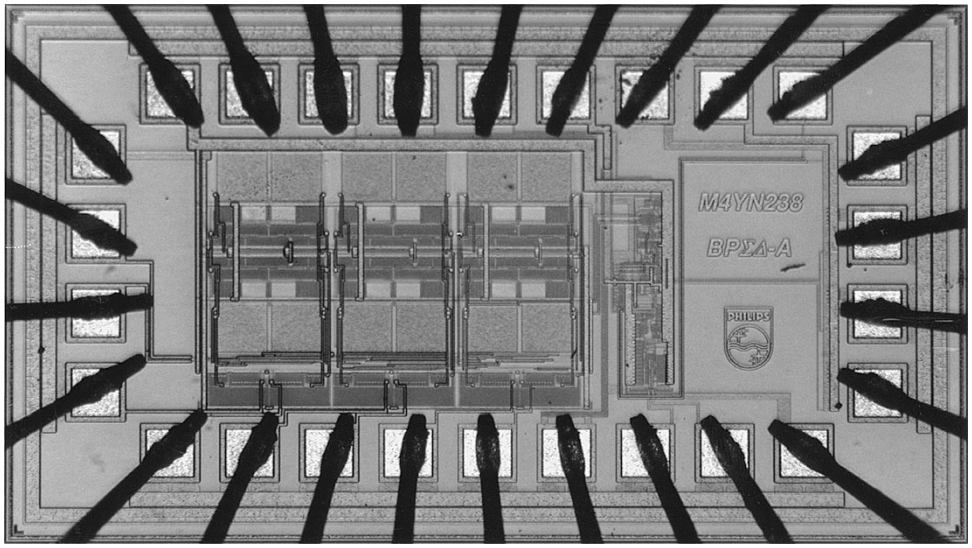

Fig. 10. Die photo of the sixth-order SDM IC.

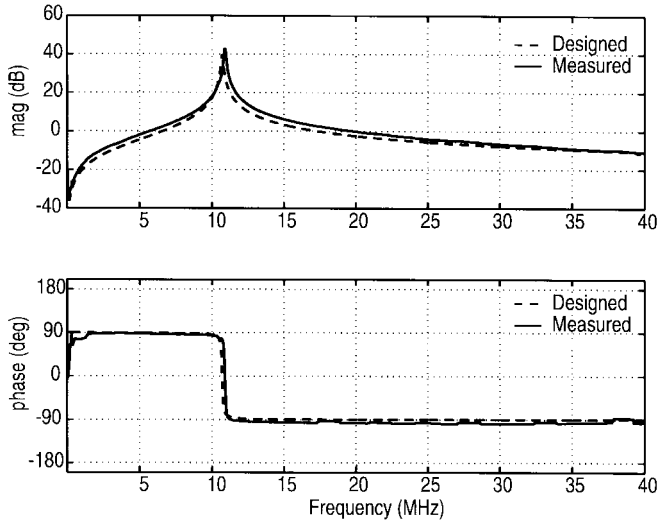

Fig. 11. Measured resonator transfer characteristic of the tunable version.

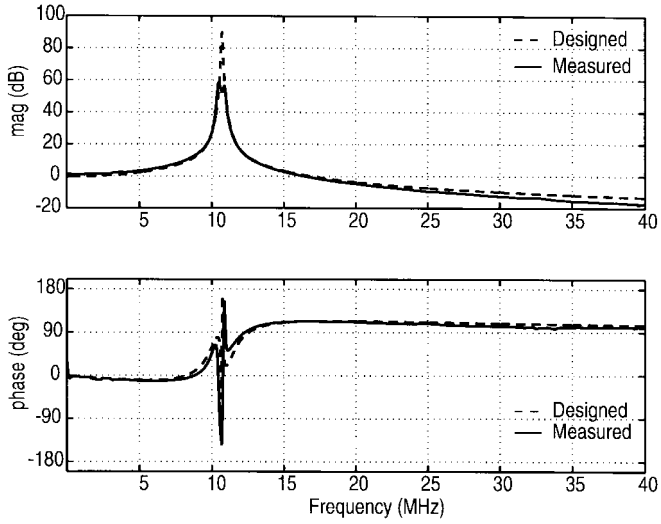

Fig. 12. Measured filter transfer characteristic of the tunable version.

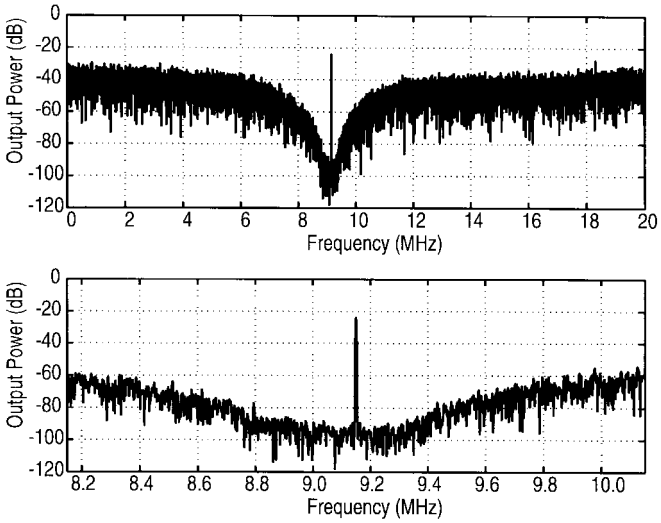

Fig. 13. Measured output spectrum of nontunable version ($f_s = 40$ MHz, $f_{\rm in} = 9.15$ MHz, 32k FFT, RBW = 1.22 kHz).

(or $f_0 + \Delta f$ and $f_0 + 2\Delta f$) are applied to the modulator, and the spurious response at the tuning frequency f_0 is measured as a function of the carrier amplitude level. In Fig. 16, the resulting characteristic of the nontunable version is shown for three different carrier spacings. The optimal IM3 of -82 dBc is reached at -13-dB carrier power, corresponding to an IP3 of $+24.5$ dBm. For carrier levels lower than -16 dB, the IM3 intermodulation product is near the measurement noise floor. Note that the measurement noise floor is not horizontal, as the vertical scale is relative to the carrier level (in dBc). When the carrier level decreases, the distance between the noise floor and the carrier also becomes smaller. Although the absolute noise floor remains constant, the relative noise floor increases as the carrier power is decreased. For carrier powers exceeding -11 dB, the IM3 intermodulation distortion increases rapidly. At such high input powers, the signals inside the loop filter become large. The limiter of the

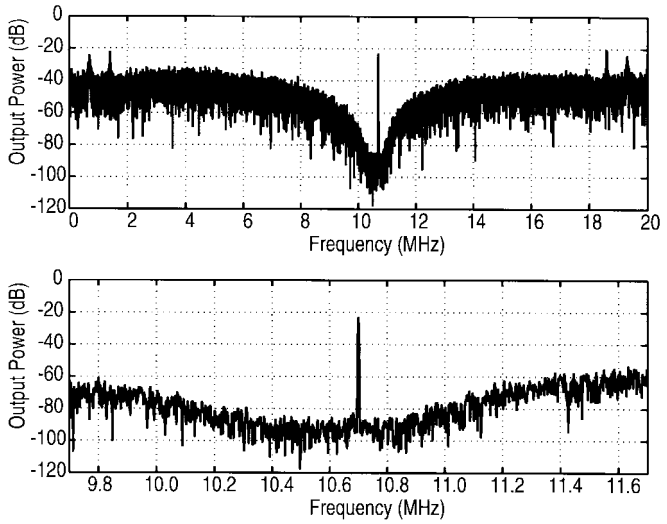

Fig. 14. Measured output spectrum of tunable version ($f_s = 40$ MHz, $f_{\text{in}} = 10.7$ MHz, 32k FFT, RBW = 1.22 kHz).

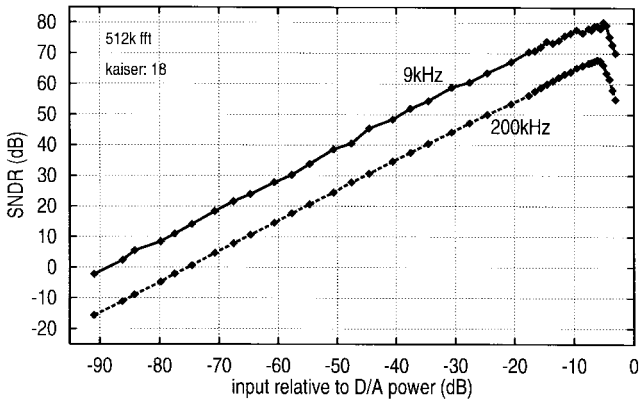

Fig. 15. SNDR versus input power characteristic of the nontunable SDM.

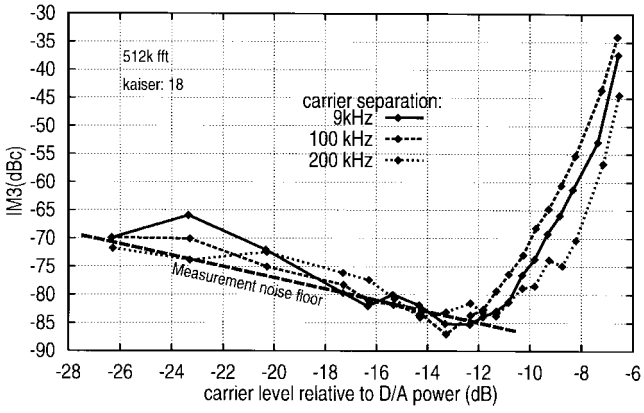

Fig. 16. IM3 versus carrier power characteristic of the nontunable SDM for three different carrier spacings.

second resonator in the loop filter will be active, increasing the (intermodulation) distortion. An output spectrum of the nontunable modulator during the two-tone test is shown in Fig. 17. The carrier spacing is 100 kHz. Note that the *in-band* IM3 distortion component at 9.25 MHz is more than

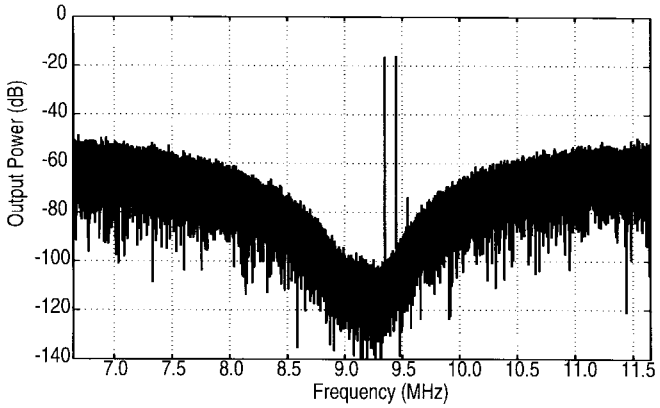

Fig. 17. Output spectrum of the two-tone IM3 measurement of the nontunable SDM ($f_s = 40$ MHz, $f_1 = 9.35$ MHz, $f_2 = 9.45$ MHz, $\Delta f = 100$ kHz, 512k FFT, RBW = 76.3 Hz).

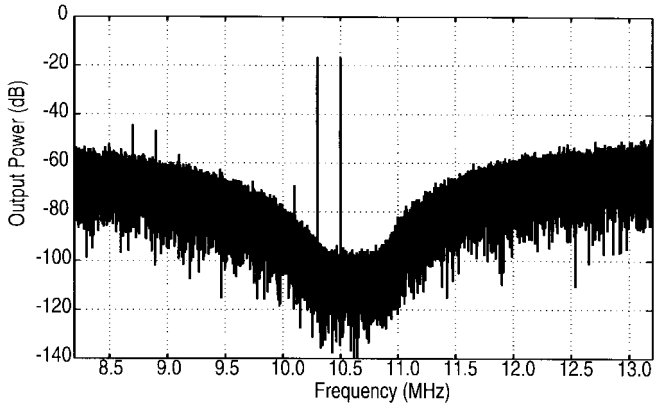

Fig. 18. Output spectrum of the two-tone IM3 measurement of the tunable SDM ($f_s = 40$ MHz, $f_1 = 10.3$ MHz, $f_2 = 10.5$ MHz, $\Delta f = 200$ kHz, 512k FFT, RBW = 76.3 Hz).

20 dB lower than the *out-of-band* component at 9.55 MHz. This shows that the IM3 distortion is partly suppressed by the feedback loop. This observation suggests that the distortion is mainly caused within the filter, and not within the DAC or at the summing node, in which case the two IM3 distortion components should have been identical. Fig. 18 shows a two-tone measurement of the tunable version with a carrier spacing of 200 kHz. Again, the amplitudes of the two IM3 distortion components at 10.1 and 10.7 MHz differ more than 20 dB.

Table II shows a summary of the performance of the sixth-order bandpass SDM. The power consumption does not include the consumption by the analog output buffers, which are not required for the operation of the SDM.

VIII. Discussion

The DR and SNDR performance of the SDM is limited by the thermal noise of the filter. The performance can be improved by reducing the impedance level in the filter at the penalty of a higher power consumption. In particular, the noise contribution of the first resonator should be reduced. A comparison between the tunable and nontunable version shows that the tuning transistors have a slight impact on the

TABLE II
SIXTH-ORDER BANDPASS SDM PERFORMANCE

	non tunable		*tunable*	
technology	0.5μm CMOS			
supply voltage	5.0V analog, 3.3V digital			
power consumption	60 mW @ f_s=40MHz			
sample frequency	30 - 80 MHz			
tuning frequency	9.15 MHz		10.7 MHz	
	Bandwidth		Bandwidth	
	200kHz	9kHz	200kHz	9kHz
idle channel noise	-78.5dBm	-92.5dBm	-73.5dBm	-87.5dBm
DR	72dB	86dB	67dB	81dB
peak SNDR	67dB	80dB	63.5dB	76dB
ENOB	10.8	13	10.2	12.3
IM3 rel. to carriers	-82dBc		-75dBc	
max. diff. input	200mV_{pp}			

performance of the SDM. The tuning mechanism may be improved by adding two cross-coupled transistors to cancel the nonlinear part in the transconductance [20].

IX. CONCLUSION

A sixth-order single-loop one-bit continuous-time bandpass sigma–delta modulator for digitizing IF signals in a combined AM/FM radio receiver has been designed and tested. The SDM achieves a DR of 72 dB in a 200-kHz bandwidth centered at 10.7 MHz. An important aspect in the design of the SDM is the stability analysis using the describing function method. Key to the analysis is the modeling of the phase uncertainty of a sampled quantizer. Together with the SDM presented in [21], this SDM shows that the signal-dependent stability of high-order, one-bit SDM's can be dealt with and that these SDM's are a viable solution for high-performance low-power A/D conversion of IF signals.

APPENDIX I
PHASE UNCERTAINTY OF A ONE-BIT QUANTIZER

First, an expression for the maximum phase uncertainty of a one-bit quantizer as a function of the input frequency f is calculated [22]. Let the input signal be a sinewave $A\sin(2\pi ft+\phi)$ with amplitude $A>0$, frequency f, and phase ϕ. Let the input signal be sampled at a rate of $f_s=1/T_s$. The zero crossing of the input signal is detected without any phase error when a sample moment $t_k = kT_s$ coincides with the zero crossing

$$A\sin(2\pi fkT_s+\phi)=0. \tag{9}$$

Solving phase ϕ of the input signal from (9) results in a set Φ of phases for which the phase error is zero

$$\Phi: \quad \phi=\pi\left(l-k\frac{2f}{f_s}\right) \quad \text{with} \quad k,l\in\mathbb{Z}. \tag{10}$$

Any phase $\phi\notin\Phi$ will result in a phase error of $\phi-\phi^*$ with $\phi^*\in\Phi$ that is nearest to ϕ. As a result, the maximum absolute phase error or phase uncertainty equals half the maximum distance between two adjacent solutions $\phi_1,\phi_2\in\Phi$

$$\Delta\phi_{\max}=\tfrac{1}{2}\ \max(\phi_2-\phi_1) \quad \text{with} \quad \begin{cases}\phi_2>\phi_1\\ \langle\phi_1,\phi_2\rangle\cap\Phi=\emptyset.\end{cases} \tag{11}$$

For an input frequency that is not a rational fraction of the sample frequency, i.e., $f/f_s\in\mathbb{R}\backslash\mathbb{Q}$, the maximum phase uncertainty is zero. According to [23], any set $m+n\xi$ with m,n arbitrary integers and ξ an irrational number will be dense in $\mathbb{R}$. As f/f_s is assumed to be an irrational number, set Φ in (10) will also be dense in $\mathbb{R}$, and the distance between any two adjacent solutions will be zero. Therefore, the maximum phase uncertainty is also zero.

For input frequencies that are a rational fraction of the sample frequency, the phase uncertainty can be calculated as follows. In this case, the fraction f/f_s can be written as

$$\frac{f}{f_s}=\frac{m}{M} \quad \text{with} \quad \begin{cases}m,M\in N\\ \gcd(m,M)=1.\end{cases} \tag{12}$$

In the case that the Nyquist criterion ($f/f_s\le\frac{1}{2}$) is taken into account, m and M also satisfy

$$\begin{cases}M\ge 2\\ m\le\left\lfloor\dfrac{M}{2}\right\rfloor.\end{cases}^{4} \tag{13}$$

The zero phase error solution set Φ can be simplified by substituting (12) into (10). Using Bezout's theorem [24]

$$\forall_{m,M\in\mathbb{Z}}|\gcd(m,M)=1 \quad \exists_{\alpha_1,\alpha_2\in\mathbb{Z}} \quad \alpha_1 m+\alpha_2 M=1. \tag{14}$$

Equation (10) is reduced to

$$\Phi: \quad \phi=\begin{cases}\dfrac{2\pi}{M}\,k & M \text{ even}\\ \dfrac{\pi}{M}\,k & M \text{ odd}\end{cases} \qquad k\in\mathbb{Z}. \tag{15}$$

For input frequencies equal to a rational fraction of the sample frequency, the solutions in Φ are equidistant. The maximum phase uncertainty is equal to half this equidistance

$$\Delta\phi_{\max}(\theta)=\begin{cases}\dfrac{\pi}{M} & M \text{ even}\\ \dfrac{\pi}{2M} & M \text{ odd.}\end{cases} \tag{16}$$

From (16), it follows that the maximum phase uncertainty does not depend on the sinewave amplitude. The maximum phase uncertainty is shown in Fig. 19 for $M=3,\ldots,64$. For an input frequency of $f_s/2$ ($M=2$), the maximum phase uncertainty is $\pi/2$. However, for a sampled sinewave with frequency $f_s/2$, a phase shift is indistinguishable from a change in amplitude, regardless of quantization. Therefore, the phase uncertainty for $M=2$ may also be considered equal to zero.

The discrete nature of the solutions for the phase uncertainty complicates a model for the stability analysis. A first-order

[4] $\lfloor x\rfloor$ represents the highest integer smaller than x.

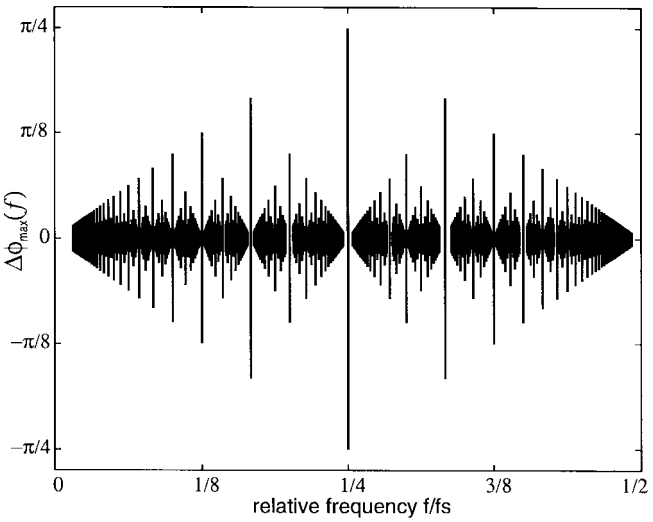

Fig. 19. Phase uncertainty of a one-bit quantizer.

approximation of the envelope of the maximum phase uncertainty can be written as a function of the normalized angular frequency $\theta = 2\pi f/f_s$

$$\Delta\phi_{\max}(\theta) = \begin{cases} \theta/2 & 0 \le \theta \le \pi/2 \\ \pi/2 - \theta/2 & \pi/2 < \theta < \pi \end{cases} \tag{17}$$

APPENDIX II
STABILITY ANALYSIS

Now that the phase uncertainty of a sampled quantizer has been calculated, a stability model can be derived. The maximum phase uncertainty $\Delta\phi_{\max}$ determines the *range* of the phase uncertainty of the sampled quantizer. To represent the actual phase uncertainty, a new model parameter α is introduced. The actual phase uncertainty can be written as $\alpha \cdot \Delta\phi_{\max}(\theta)$. Together with the gain parameter λ that models the effects of amplitude quantization, the linearized z-domain model for the one-bit quantizer can be written as

$$\tilde{Q}(z) = \lambda \cdot e^{j\alpha\Delta\phi_{\max}(\theta)} \quad \text{with} \quad \begin{cases} z = r \cdot e^{j\theta} \\ \lambda \in [0, \infty\rangle \\ \alpha \in [-1, 1]. \end{cases} \tag{18}$$

Note that for $\alpha = 0$, the model is reduced to the previously mentioned linear gain model. For the maximum phase uncertainty, the previously derived approximation in (17) is used. The stability of the SDM with the DT loop filter $G(z)$ can now be analyzed by drawing the root locus of the (linearized) closed loop transfer function of the system (see Fig. 20), i.e., the roots of

$$1 + \lambda e^{j\alpha\Delta\phi_{\max}(\theta)} G(z) = 0. \tag{19}$$

Modeling the phase uncertainty adds a second parameter to the root locus analysis. In order to simplify the evaluation, the root trajectories are plotted as a function of the gain parameter λ for discrete values of the phase uncertainty parameter α. The basic thought behind this is that any instability will give rise to a higher amplitude of the signal within the loop and

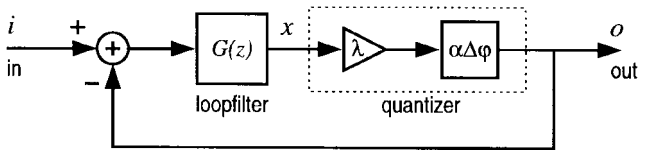

Fig. 20. Stability model of a sigma–delta modulator.

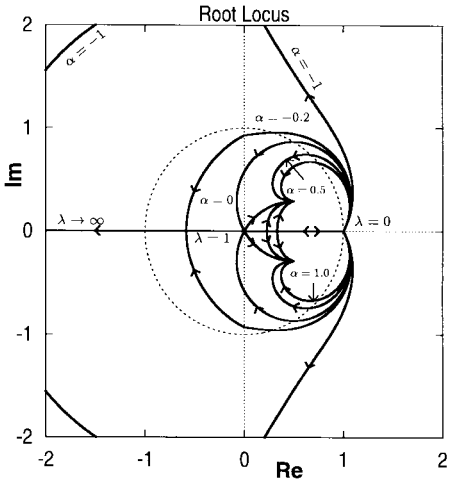

Fig. 21. Root locus of a third-order low-pass SDM ($a = 0$) for different values of the phase uncertainty parameter α.

a corresponding change in λ. As the phase uncertainty is independent of the amplitude of the signal, α can be considered constant.

As an example, consider the third-order low-pass SDM with loop filter

$$G(z) = \frac{(1 - az^{-1})^3}{(1 - z^{-1})^3} - 1. \tag{20}$$

The parameter a determines the location of the zeros and provides a tradeoff between stability and performance. For $a = 0$, this modulator is unstable, even for zero-input and zero-initial state conditions. For $a \approx 1$, the modulator is stable, but the in-band loop gain is low and the quantization noise is not shaped significantly. In order to find the minimum required value for a for which the third-order SDM is stable for zero-input conditions, the root locus is analyzed. In Fig. 21, the root locus is shown for $a = 0$ and several (discrete) values of the phase parameter α. Now, a very small amplitude signal ($\lambda \gg 1$) is assumed to be present in the loop. A single root will be outside the unit circle in the left-hand plane, and the loop is unstable. Consequently, the amplitude of the signal will increase and λ will decrease, thus moving the unstable root toward the unit circle. However, for some values of α, this root does not enter the unit circle when λ decreases. The root can remain outside the unit circle even for very small λ: a large-signal limit cycle is possible. The SDM cannot be considered stable, even for small input signals. This instability is not predicted without modeling the phase uncertainty ($\alpha = 0$).

By changing the value of the filter parameter a, this modulator can be made stable for small input signals. In Fig. 22, the outer (worst case) branch of the root locus is shown for several values of a. For $a \ge 0.412$, this branch does intersect

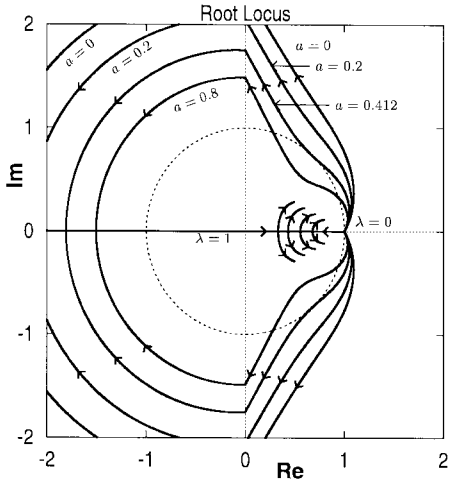

Fig. 22. Root locus ($\alpha = -1$) of a third-order low-pass SDM for different values of the filter parameter a.

TABLE III
MINIMAL VALUES FOR a FOR WHICH A LOW-PASS SDM WITH LOOP FILTER $G(z) = (z-a)^n/(z-1)^n - 1$ IS STABLE FOR SMALL SIGNALS

n	a	
	model	*experimental*
3	0.412	0.416
4	0.587	0.619
5	0.679	0.717
6	0.736	0.771

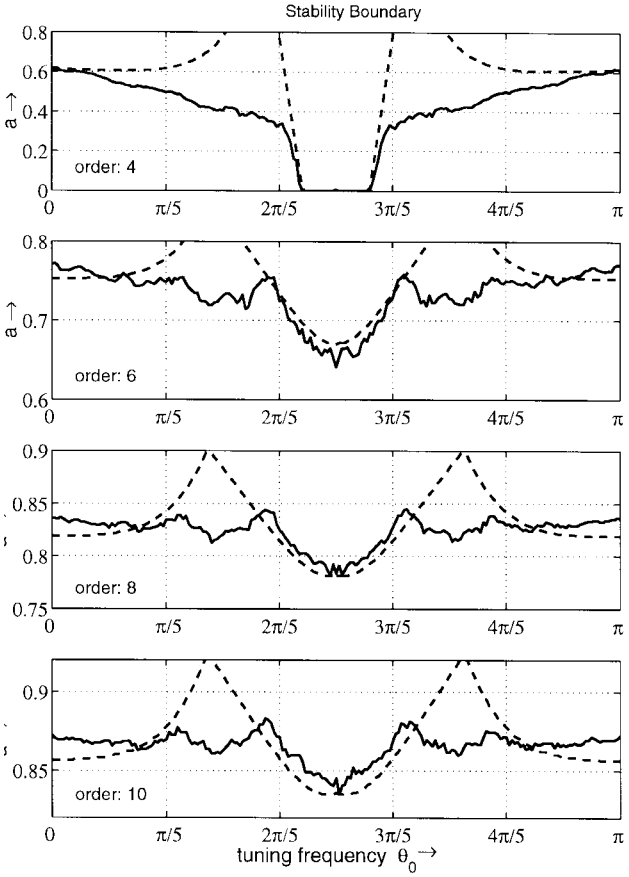

Fig. 23. Theoretically (dashed) and experimentally (solid) determined minimum values for a of a fourth-, sixth-, eighth-, and tenth-order band-pass SDM, for which it is stable for small signals.

with the unit circle, and all the roots will move inside the unit circle for a certain range of λ and all α. This provides a stable operating range. Note that, as some roots can leave the unit circle again in case λ decreases further (due to an applied input signal), the modulator is only conditionally stable. The theoretical minimum found for a is within 1% of the experimentally determined value of $a = 0.416$. Higher order modulators have a similar root locus, and minimum values for the filter parameter a can be found in the same manner (see Table III).

As the outer branches of root loci of higher order low-pass modulators all touch the unit circle near $\theta = \pi/3$, the analysis can be simplified. The radius of the outer root locus branch needs only to be evaluated for $\theta = \pi/3$. To extend this analysis to high-pass modulators, evaluation at $\theta = 2\pi/3$ is required as well (this follows from symmetry considerations). This leads to the following stability criterion.

An SDM with loop filter $G(z)$ will be stable for small input signals when the roots of the stability equation

$$1 + \lambda e^{j\alpha\pi/6} G(z) = 0 \quad \text{with} \quad z = r \cdot e^{j\theta} \tag{21}$$

lie within the unit circle for $\theta = \pi/3 \vee \theta = 2\pi/3$, $\lambda > 0$, and all $\alpha \in [-1, 1]$.

Although derived for low- and high-pass modulators only, we now apply this stability test to a class of tunable modulators with the following loop filter:

$$G(z) = \frac{(1 + ae^{j\theta_0} z^{-1})^N (1 + ae^{-j\theta_0} z^{-1})^N}{(1 + e^{j\theta_0} z^{-1})^N (1 + e^{-j\theta_0} z^{-1})^N} - 1. \tag{22}$$

The order of the modulator equals $2N$, and the tuning frequency is θ_0. In Fig. 23, both the theoretical required minimum value for a and the experimental minimum value for a found by lengthy simulations are shown as a function of the tuning frequency θ_0 for a fourth-, sixth-, eighth-, and tenth-order modulator. For tuning frequencies $\theta_0 \in [0, \pi/5]$, $[2\pi/5, 3\pi/5]$, and $[4\pi/5, \pi]$, this extended model provides an accurate estimate for minimal values of loop filter parameters, required for small-signal stability of the SDM.

As the minimum value for a only provides conditional stability (at small input signal levels), additional measures for absolute stability are required. By limiting a number of filter states, the effective order of the loop filter is reduced and stable operation of the SDM is ensured.

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