# CH4/H2/Ar electron cyclotron resonance plasma etching for GaAs-based field effect transistors

# $CH_4/H_2/AR$ Electron Cyclotron Resonance Plasma Etching for GaAs-Based Field Effect Transistors

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ABSTRACT

Electron cyclotron resonance (ECR) plasma etch processes with $CH_4/H_2/Ar$ have been investigated on different III-V semiconductor materials (GaAs, AlGaAs, InGaAs, and InP). The passivation depth as a function of the GaAs carrier concentration and the recovery upon annealing at different temperatures have been determined by C-V measurements. Little degradation on the characteristics of Schottky diodes is observed with increasing process biases. If the GaAs top layer of an AlGaAs/GaAs heterostructure is removed by plasma processing the Hall mobility is restored to 74% after annealing at 425°C. This is compared to a wet chemically etched reference sample. The 2-DEG sheet density fully recovers. However, if an Si δ-doped layer is incorporated in the heterostructure the Hall mobility and the sheet density completely restore after plasma etching and subsequent annealing. In the experiments minimal damage is observed at a substrate bias of −40 V. The direct current and high frequency characteristics of a dry and wet etched pseudomorphic heterostructure field-effect transistors are compared.

## Introduction

There is an increasing interest in $CH_4/H_2$-based plasma etching since Niggebrügge *et al.* used this gas mixture in reactive ion etching (RIE) processes for InP.[1] The alternative use of chlorinated gas mixtures $SiCl_4$, $Cl_2$, and $BCl_3$ have the disadvantage of being very corrosive and toxic. Electron cyclotron resonance (ECR) plasma discharges offer advantages over RF-based plasmas.[2] ECR provides a high degree of ionization at low pressures. The discharge is generated remotely and independently from the substrate stage. In this way the substrate does not suffer from excessive ion bombardment and less damage is created since it is possible to work at low dc biases. This is essential for devices susceptible to performance degradation due to their sensitivity to ion bombardment.[3] This is in contrast to RIE where RF power on the substrate is used for maintaining the plasma and providing the process bias.

In this paper the behavior and the etch rates of the $CH_4/H_2/Ar$ ECR plasma on different III-V semiconductors is studied, and the passivation depth and recovery upon annealing, as measured by C-V measurements are discussed. Subsequently the influence of the ECR plasma on Schottky diodes as a function of the process bias is studied by *I-V* measurements. The influence of an additional silicon δ-doped layer in an AlGaAs/GaAs heterostructure on the damage introduced by the $CH_4/H_2/Ar$ ECR plasma is studied by Hall measurements. As a function of temperature the Hall mobility and the sheet density are measured. The results obtained with ECR are compared to identical measurements on the same structures with RIE using a methane hydrogen gas mixture. Finally the dc and high frequency characteristics obtained on dry and wet processed pseudomorphic heterostructure field-effect transistors (HFETs) are compared.

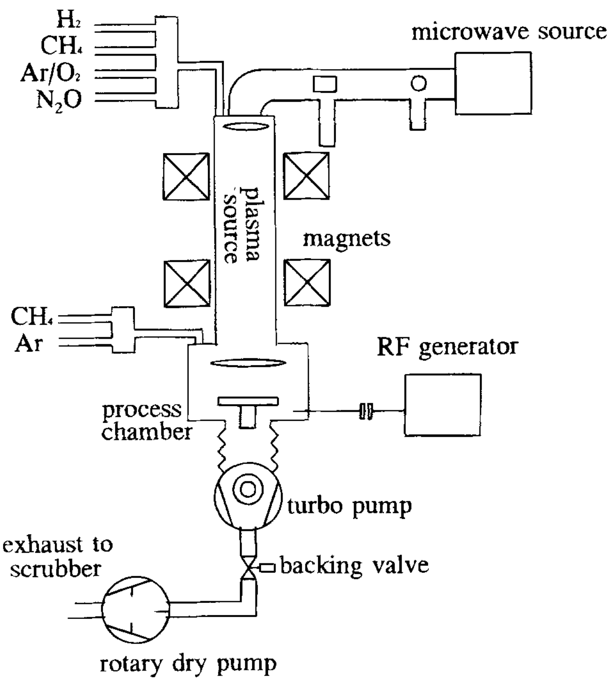


**Fig. 1. Schematic layout of the $CH_4/H_2/Ar$ ECR etch chamber.**

## Experimental

Figure 1 shows schematically the load-locked ECR reactor (Oxford Plasma Technology) used during the experiments. The vacuum is created by a Maglev (Seiko Seiki) 1000 $ls^{-1}$ ($N_2$) turbomolecular pump which is supported by a rotary dry pump (Edwards DP 80). The base pressure is $6 \cdot 10^{-6}$ Torr. The gases are exhausted via a dry scrubber to break possible volatile process gas reactants. The microwave power at 2.45 GHz is introduced through a waveguide into the top of the vacuum chamber. Tuning of the reflected power is accomplished by two motor driven tuning stubs on the waveguide. Two magnets produce the magnetic fields necessary for the cyclotron resonance condition. The substrate table is located downstream of the microwave discharge zone. On the substrate table additional RF power, operating at 13.56 MHz, can be supplied to obtain a certain dc bias level. The RF power is varied from

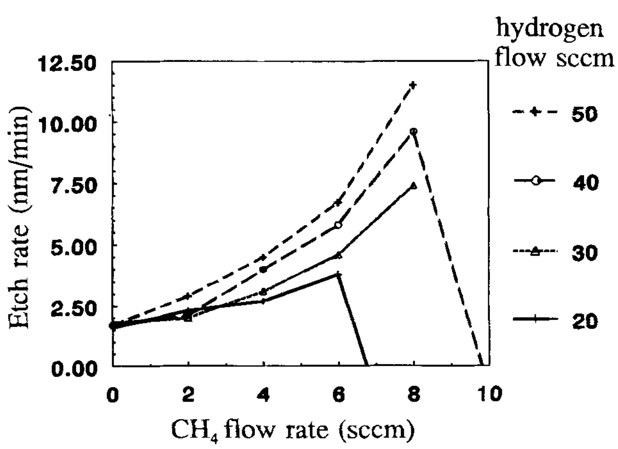


**Fig. 2. The etch rate on GaAs at −80 V dc bias as function of the methane flow for different hydrogen flows.**

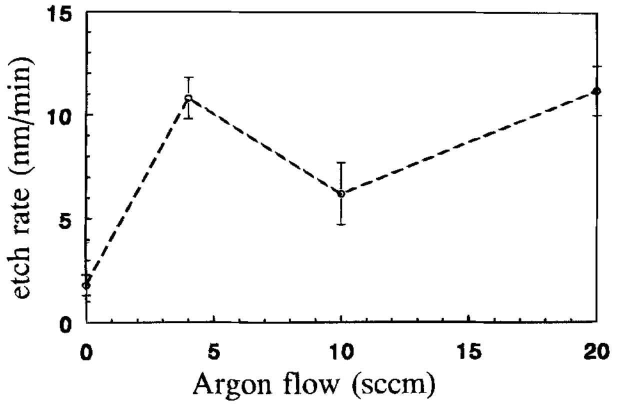


**Fig. 3. The influence on the etch rate of an increasing argon flow at a dc bias of −40 V.**

18 to 96 W which results in a dc bias of −20 and −120 V, respectively. The table temperature is controlled with a heater/chiller, and the table can be moved with respect to the plasma. It is possible to introduce the gas mixtures at two different places. In the top of the chamber, adjacent to the upper magnet, it is possible to introduce the process gases $CH_4$, $H_2$, and Ar. Nitrous oxide and oxygen are used for cleaning purposes. $CH_4$ and Ar can also be introduced by a second gas distribution ring in the vicinity of the substrate.

## Results and Discussion

*$CH_4/H_2/Ar$ ECR etch characteristics.*—The influence of the $CH_4$:$H_2$ ratio and of additional argon on the average etch rate of GaAs is investigated. A sample size of 1 $cm^{-2}$ was used and 80% covered with a resist mask. Before loading, the substrate was cleaned in dilute ammonium hydroxide, and the chamber was prepared for 10 min with a hydrogen plasma to reduce the amount of residual oxygen. The etch depth is measured with a Tencor α-step 200. Methane and hydrogen are supplied via the top gas manifold. Figure 2 shows the etch rates as a function of the methane flow for different hydrogen flows. No argon was used during these experiments. The microwave power is 600 W and the RF power varied from 45 to 57 W to obtain a constant dc bias of −80 V. The pressure varied from 1 mTorr at a hydrogen flow of 20 sccm to 2.5 mTorr at 50 sccm. The etch rate increases with increasing methane and hydrogen flow until polymer deposition was initiated on the GaAs surface. Similar observations have been described in the literature.[4] Polymer deposition is initiated at a methane hydrogen ratio of about 1:3. Identical behavior was observed at a dc bias of −40 V although polymer formation occurred at a methane-hydrogen ratio of 1:5.

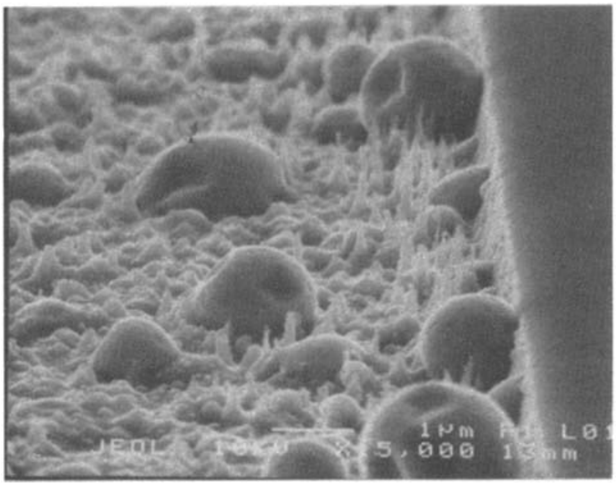

**Fig. 4. InP etched at a microwave power of 600 W.**

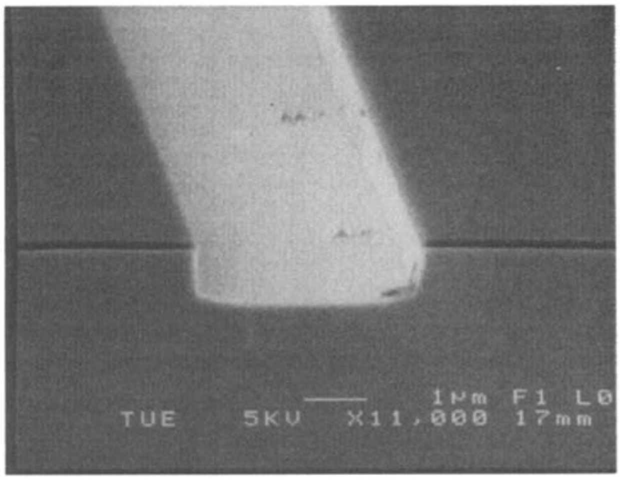


**Fig. 5. InP etched at a microwave power of 150 W.**

If argon was added (top manifold) a dip in the etch rate at an argon flow of 10 sccm was observed as shown in Fig. 3. This experiment was done at a dc bias of −40 V and a methane and hydrogen flow, respectively, of 20 and 4 sccm. The etch rate increased from 1.8 to 10.8 nm/min if 4 sccm argon was supplied but decreased to 6.1 nm/min at an argon flow of 10 sccm. We assume that increasing the argon flow to 4 sccm increases the desorption of reaction products from the surface which leads to an improved etch rate. A further increase of the argon flow causes the etch to become adsorption limited. From 10 to 20 sccm the increase in etch rate is mainly initiated by argon sputtering. Based on the experiments, an argon flow of 4 sccm together with the above mentioned hydrogen and methane flow was chosen for further experiments.

The etch rates on different III-V materials exhibit a first-order dependence on the applied dc biases (RF power). For GaAs the etch rates increased from 3.1 to 22.3 nm/min for dc biases, respectively, of −20 V (18 W) and −80 V (66 W). For AlGaAs (25 and 50% Al) and $In_{0.53}$ GaAs, respectively, lower and higher etch rates are observed. $Al_{0.5}$GaAs showed an increase of 5.6 nm/min (−40 V) to 15.3 nm/min (−80 V) whereas the etch rate of $In_{0.53}$GaAs increased from 10 to 30.3 nm/min for identical dc biases. The methane flow was increased during these experiments from 2 to 6 sccm at −20 and −80 V, respectively, to maintain the amount of reactive species close to the point of polymer formation. The etch rates are comparable with the literature.[5]

For InP the etch rates at a microwave power of 600 W and a dc bias of −40 V is 17.4 nm/min, although the surface becomes very rough as shown in the SEM photograph of Fig. 4. This is due to the formation of indium droplets caused by a preferential removal of the phosphorus molecules from the surface. By reducing the microwave power to 150 W and increasing the dc bias the surface morphology is improved as shown in Fig. 5. This has also been observed by others.[6,7] At 150 W the sidewalls are nearly vertical, and the surface is reasonably smooth. The etch rates at dc biases of −100 V (21 W), −150 V (38 W), and −210 V (65 W) are, respectively, 3.7, 7.5, and 10.3 nm/min. Pearton[6,7] attributed the improvement in surface morphology to a reduction of the imbalance between the active hydrogen species and methane radicals.

*Passivation and Schottky diodes.*—Due to the penetration of hydrogen in semiconductor materials, passivation or neutralization of dopant atoms occurs.[8] In silicon-doped materials this loss of electrical activity is explained by the formation of a neutral silicon-hydrogen complex. Recovery of the electrical activity or carrier density is generally obtained after annealing at temperatures around 400°C. In our experiments the passivation depth is measured by C-V measurements (HP 4280A) at a frequency of 1 MHz on Ti/Pt/Au Schottky diodes. The experiments are done on Si-doped bulk GaAs grown on a highly doped substrate. The

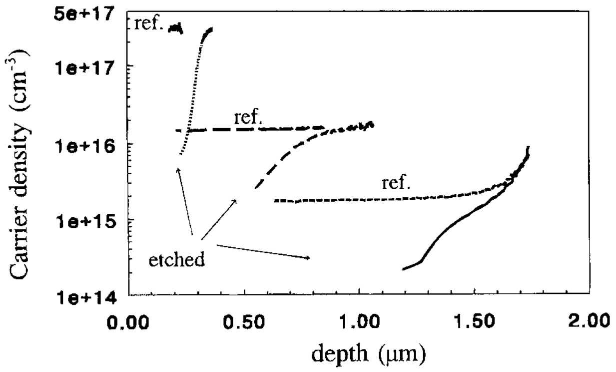


**Fig. 6. The passivation depth after 10 min etching at a −20 V dc bias as a function of the donor concentration compared to reference structures.**

bulk layers are grown by molecular beam epitaxy (MBE). A back side ohmic contact is used. Figure 6 shows the passivation depth after 10 min processing at a dc bias of −20 V as function of different doping levels. The carrier density is compared to a reference diode. It can be seen that the passivation depth increases with decreasing donor concentration. It is observed that the passivation depth also increases with increasing substrate biases. Recovery of the carrier density is obtained after annealing for 1 min at different temperatures in a rapid thermal annealer (AST shs 100) in a nitrogen ambient. The results are shown in Fig. 7. After annealing at 375°C the carrier density is recovered to its initial value of $3 \cdot 10^{17}$ $cm^{-3}$. Little increase is observed at higher temperatures. These results are comparable to the literature.[9]

The influence of $CH_4/H_2/Ar$ ECR plasma etching prior to a Ti/Pt/Au Schottky diode evaporation is investigated. This is done for different dc biases (−20, −40, and −80 V, respectively). 200 · 200 μm diodes are evaporated at $3 \cdot 10^{17}$ $cm^{-3}$ (Si) doped GaAs. The etch depth was maintained as a constant. The results are compared to a wet chemical etched diode with and without an annealing step at 375°C.

The plasma-etched diodes recover after annealing at a temperature of 375°C for 1 min. At a temperature of 400°C the contacts degrade due to intermixing of the Schottky metallization and the GaAs. Table I shows the *I-V* measurements extracted barrier height ($\Phi_b$), ideality factor ($n$), and saturation current ($I_s$) as function of the dc bias. The characteristics degrade with increasing substrate bias but are comparable to the unannealed reference diode. Compared to the annealed reference diode little degradation is observed. These results confirm the low structural or physical damage introduced by ECR plasma etching.

*Influence of Si δ-doped layer on AlGaAs/GaAs heterostructure.*—The influence introduced by $CH_4/H_2$ reactive ion etching on AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures has been investigated by Van Es and

**Table I. The influence of $CH_4/H_2/Ar$ ECR plasma etching on the barrier height, $\Phi_b$, the ideality factor, $n$, and the situation current, $I_s$, of Schottky diodes. The results are compared to a wet chemically etched reference diode.**

| | $n$ | $\Phi_b$ (V) | $I_s$ (mA) |
|---|---|---|---|
| Reference | 1.25 | 0.68 | $1.5 \cdot 10^{-6}$ |
| Reference (375°C) | 1.18 | 0.74 | $1.8 \cdot 10^{-7}$ |
| −20 V | 1.22 | 0.73 | $3.6 \cdot 10^{-7}$ |
| −40 V | 1.24 | 0.74 | $6.4 \cdot 10^{-7}$ |
| −80 V | 1.30 | 0.68 | $2.3 \cdot 10^{-6}$ |

Pereira.[10] They measured the optical and transport properties of these heterostructures. Upon annealing they obtained full recovery of the 2-DEG sheet density and 60% recovery of the Hall mobility in AlGaAs/GaAs heterostructures. With an additional Si δ-doped layer 75% recovery of the Hall mobility was obtained. From their experiments it was suggested that an additional Si δ-doped layer could prevent the mobility degradation. Identical observations have been reported for chlorine-based plasma chemistries.[11,12] In this work a closer investigation is done on the influence of an additional Si δ-doped layer in an AlGaAs/GaAs heterostructure. Two different MBE grown AlGaAs/GaAs structures have been used. The first structure (W24) consists of a 4 μm undoped GaAs buffer layer, a 20 nm $Al_{0.33}GaAs$ undoped spacer, a 38 nm $Al_{0.33}GaAs$ $1 \cdot 10^{18}$ $cm^{-3}$ (Si) donor layer, and a 17 nm undoped GaAs top layer grown on a semi-insulating GaAs substrate. In the second structure a $5 \cdot 10^{12}$ $cm^{-2}$ Si δ-doped layer was incorporated on top of the AlGaAs spacer (W482). The GaAs top layer is removed by the ECR plasma after the Hall bar was defined by optical lithography and wet etching, and Ge/Ni/Au ohmic contacts were evaporated and annealed. Hall measurements are performed as a function of temperature (5 to 300 K) to obtain the Hall mobility and the 2-DEG sheet density. This is done as function of different process biases (−20, −40, and −80 V) and as function of annealing temperature. Layers W24 and W482 are the same as used by Van Es.[10] This gives the opportunity to compare the results obtained with RIE and ECR plasma processes. Figure 8 and 9 show, respectively, the Hall mobility and sheet density of sample W24 after removing the GaAs top layer at an ECR substrate bias of −40 V. The results are shown as a function of measurement and annealing temperature and compared to a wet chemically etched reference sample. The top layer of the reference sample was removed in a dilute $NH_4OH:H_2O_2$ solution. The annealing temperature was raised to 450°C and maintained for 1 min. Whereas the sheet density nearly fully recovered the Hall mobility recovered only 74%. Little change in the Hall mobility and sheet density is observed at temperatures above 400°C. Table II shows the recovery of both structures as a function of substrate bias, and when compared to a reference sample, measured at 5.6 K, the influence of an additional Si δ-doped layer is clearly demonstrated. It seems that pro-

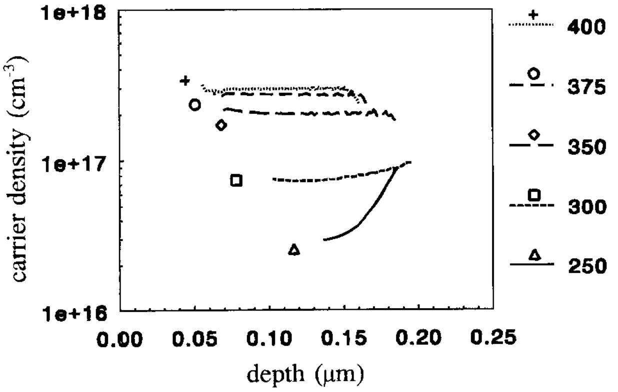


**Fig. 7. The recovery of the carrier density as function of annealing temperature.**

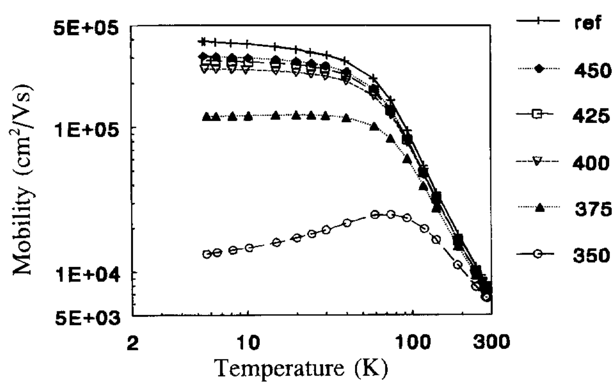


**Fig. 8. The Hall mobility of an after removing the GaAs top layer at a dc bias of −40 V.**

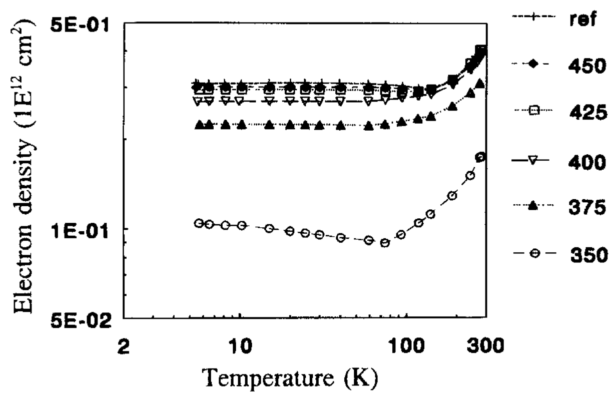


**Fig. 9. The electron sheet density after removing the GaAs top layer at a dc bias of −40 V.**

cessing at a dc bias around −40 V leads to an optimum recovery for both structures. This is in contrast to results observed on the Schottky diodes where the least amount of damage is observed at a process bias of −20 V. We believe that this optimum is created by minimizing the plasma exposure time, which is obtained by increasing the substrate bias, and on the other side a reduction in substrate bias is necessary to minimize the structural damage. The etch time for removing the GaAs top layer at a −20 V dc bias is at least three times as long as in the case of −40 V. Compared to the results obtained by RIE,[10] less damage is introduced by ECR plasma etching. In both cases the sheet density fully recovers. However, by RIE a 40% reduction in the Hall mobility is observed compared to 26% at a dc bias of −40 V in our experiments. Improved results are also obtained by ECR on the structure with the additional silicon δ-doped layer. The Hall mobility is recovered to 94% in ECR compared to 75% by RIE.

*Pseudomorphic HFET.*—The $CH_4/H_2/Ar$ ECR plasma process is used in pseudomorphic AlGaAs/InGaAs/GaAs heterostructure field-effect transistor (PMHFET) gate recess fabrication. The PMHFET were characterized by direct current and high frequency measurements (≤40 GHz), and the results were compared those obtained with wet chemically recessed PMHFETs. The structure (W385) is grown by MBE on a semi-insulating substrate and consists of a 1.5 μm undoped GaAs buffer layer, a 15 nm undoped $In_{0.15}Ga_{0.85}As$ pseudomorphic layer, a 3 nm undoped $Al_{0.2}Ga_{0.8}As$ spacer, a 50 nm $1.5 \cdot 10^{18}$ $cm^{-3}$ (Si) doped $Al_{0.2}Ga_{0.8}As$ donor layer, and a 70 nm $2 \cdot 10^{18}$ $cm^{-3}$ (Si) doped GaAs top layer. The process is performed at a dc bias of −40 V. The transistors have a gate length and width of 1 and 100 μm, respectively. The dc and microwave measurements are listed in Table III. Whereas the dc characteristics improve, a slight degradation is observed in the high frequency parameters. Nevertheless, it is possible to fabricate good performance pseudomorphic HFETs using the $CH_4/H_2/Ar$ ECR plasma.

**Table II. The measured 2-DEG mobility and sheet density of an AlGaAs/GaAs heterostructure after annealing and as a function of different process biases. Measured at 5.6 K and compared to a wet etched reference sample.**

| | | −20 V | −40 V | −80 V | Ref. |
|---|---|---|---|---|---|
| W24 | $n_s$ ($10^{11}$ $cm^{-2}$) | — | 3.00 | 2.70 | 3.10 |
| | μ ($10^5$ $cm^2/Vs$) | — | 3.07 | 2.05 | 3.88 |
| W482 | $n_s$ ($10^{11}$ $cm^{-2}$) | 3.56 | 3.78 | 3.62 | 3.51 |
| δ-doped | μ ($10^5$ $cm^2/Vs$) | 2.85 | 5.81 | 5.13 | 6.16 |

**Table III. The parameters extracted from dc and microwave measurements of a dry processed pseudomorphic 1 · 100 μm HFET compared to a wet chemically etched transistor.**

| | Wet | Dry |
|---|---|---|
| $g_{m,max}$ (mS/mm) | 340 | 370 |
| $g_d$ (mS/mm) | 6.8 | 5.6 |
| $I_{dss}$ ($V_{gs}$ = 0 V) (mA) | 4.42 | 4.66 |
| $V_T$ (V) | −0.64 | −0.53 |
| $f_t$ (GHz) | 22.4 | 20.6 |
| $f_{max}$ (GHz) | >45 | 38 |

## Conclusions

A $CH_4/H_2/Ar$ ECR plasma process is optimized and the damage is investigated on Schottky diodes and AlGaAs/GaAs heterostructures and compared to wet chemically etched reference samples. This damage appears to be a function of the process substrate bias. For Schottky diodes a minimal damage is observed at −20 V substrate bias. The diode characteristics are comparable to unannealed wet chemically etched diodes. A minimal damage for AlGaAs/GaAs heterostructures is measured at −40 V. The electron density in these structures fully recovers whereas the Hall mobility recovers 74%. Compared to RIE, less damage is introduced. Introduction of an Si δ-doped layer in an AlGaAs/GaAs heterostructure behaves as a shield and nearly full recovery of the Hall mobility is obtained. The process is suitable for HFET gate recess fabrication.

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