CCD imaging : concepts for low noise and high bandwidth

CCD Imaging

Concepts for Low Noise and High Bandwidth

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de
Technische Universiteit Eindhoven, op gezag van de
Rector Magnificus, prof.dr. M. Rem, voor een
commissie aangewezen door het College voor
Promoties in het openbaar te verdedigen
op maandag 29 maart 1999 om 16.00

door

Petrus Gijsbertus Maria

Centen

geboren te Goirle

Dit proefschrift is goedgekeurd door de promotoren:

prof.dr. F.M. Klaassen

en

prof.dr. T.G.M Kleinpenning

Copromotor:

dr.ir. A.J.P Theuwissen

The work described in this thesis has been carried out at the Philips Research Laboratories in Eindhoven and Philips Digital Video Systems (Breda) B.V., The Netherlands.

Aan mijn vrouw Peti
Aan mijn ouders Bertus en Lies

CIP-DATA LIBRARY TECHNISCHE UNIVERSITEIT EINDHOVEN

Centen, Petrus G.M.

CCD Imaging : concepts for low noise and high bandwidth /
by Petrus G.M.Centen. - Eindhoven : Technische Universiteit Eindhoven, 1999.
Proefschrift. - ISBN 90-386-1570-1
NUGI 832
Trefw.: optische sensoren / optimale filters / elektronische beeldtechniek / beeldopname techniek / fotohalfgeleiders.
Subject headings: CCD image sensors / semiconductor device noise / matched filters / optoelectronic devices / video signal processing.

Druk: Universiteitsdrukkerij, Technische Universiteit Eindhoven
Coverdesign by Ben Mobach

TABLE OF CONTENTS

Chapter 1

INTRODUCTION

The first section of this introductory chapter provides some background on Charge Coupled Device imagers (CCDs). It starts by explaining the way a two-dimensional imager is built, showing the on-chip amplifier and signal processor as part of the imaging signal chain. Next a CMOS imager is introduced. Then some quantities used in calculating the noise performance are discussed. Finally, a presentation of the scope of this thesis is given.

1.1 CCD imagers

A broadcast colour camera usually contains three CCD imagers. These CCDs are glued on a colour splitter, or prism, to obtain the optical red, green and blue signals (primary colours). The CCD converts the optical signal into an electrical signal, one for each colour channel. This electrical signal is further processed in a signal processor to obtain what is known as base band video. The CCDs used are of the two-dimensional type. Of the latter three architectures are used commercially: Interline Transfer (IT), Frame Interline Transfer (FIT) and Frame Transfer (FT). A lengthy discussion of these imager types has been given by Theuwissen [1].

A two-dimensional FT imager or FIT imager consists of an image area, a

storage area, a horizontal register, and an on-chip amplifier (see Figure 1.1). In the image area a two-dimensional charge image is generated by a light pattern projected onto the array. In a PAL video camera it takes about 20 ms to generate the charge image. The whole charge image is transported quickly (typically some 100 μs) to the storage area. The storage area is covered with a light shield to prevent false images being generated. After the fast vertical transport the image area is cleared and a new charge image is generated. The charge image, now present in the storage area, is shifted relatively slowly into a horizontal register one row at a time. This row is also called a TV line. A row is shifted from the storage area into the horizontal register in parallel and shifted serially towards the detection node with its on-chip amplifier. Transporting a row through the horizontal register takes about 64 μs. The clock frequency for driving the horizontal register has increased over the years from about 4 MHz, Collet [2], to 54 MHz, Moelands et al. [3].
The charge image consists of individual charge packets, which are usually formed by electrons but sometimes by holes, Roks [4]. The number of image cells or charge packets in one charge image (frame) can be as low as $3 \cdot 10^5$, or as high as 63.10^6, Kreider [5]. A charge packet arriving at the end of the horizontal register is dumped on a floating diffusion region, symbolized by a capacitor. This capacitor, together with the parasitic capacitances of the on-chip amplifier input, converts the charge packet into a voltage change. The on-chip amplifier buffers the voltage change and drives a signal processor. The latter processes the on-chip amplifier output signal to obtain base band video.

The floating diffusion region together with the input of the on-chip amplifier is called the detection node.
After the charge packet has been converted into a voltage pulse the reset FET clamps the detection node to a reference voltage. During the clamp action the charge is drained off and the detection node is prepared for the conversion of the next charge packet. During clamping the reset FET channel is conducting and together with the detection node capacitance forms a first order low pass filter for the thermal noise of the conducting reset FET channel. At the end of the clamping interval the reset FET is switched off and the momentary value of the noise voltage is sampled on the detection node capacitance. This is called reset noise, Carnes and Kosonocky [6].

Whether one focuses on IT, FIT, FT or CMOS imagers, all have in common that a charge packet is generated in an image cell which is converted into a voltage pulse on a detection node which is followed by an on-chip amplifier and a signal processor. Generally, the noise sources in the signal chain of Figure 1.1

are:

- photon generated shot noise in the image cell,
- shot noise arising from dark current in the image and storage cells (significant at high temperatures),
- reset noise generated when the reset FET is switched off,
- thermal noise and 1/f noise caused by the on-chip amplifier,
- the filtering effect of the signal processor.

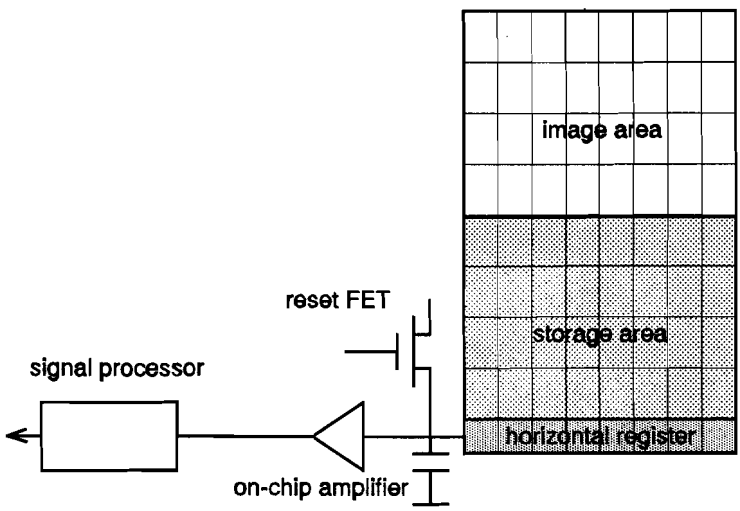

Figure 1.1: *An imager signal chain.*

A broadcast colour camera generates 50 images per second in the PAL system and about 60 images per second in the NTSC system. The number of TV lines, or image cells in the vertical direction, is determined by the imaging/transmission standard. For PAL this amounts to 575 image cells vertically in one frame and for NTSC 485. These standards are generally known as SDTV or standard television. In addition to SDTV there also exists HDTV, high definition television. The number of vertical image cells (TV lines) that make up one frame varies between 720, 960, 1035, 1080 and 1152. The number of image cells per TV line, or pixels per line, varies between 740 and 1440 for SDTV and between 1280 and 1920 for HDTV, Theuwissen et al. [7], Blankevoort [8] et al., Spitzer et al. [9].

In Figure 1.2 a cross section of a CCD is given showing the transport of an electron charge packet. The voltages applied to the polysilicon gates are changed in such a way that the electron charge packet moves in a peristaltic way from right to left.

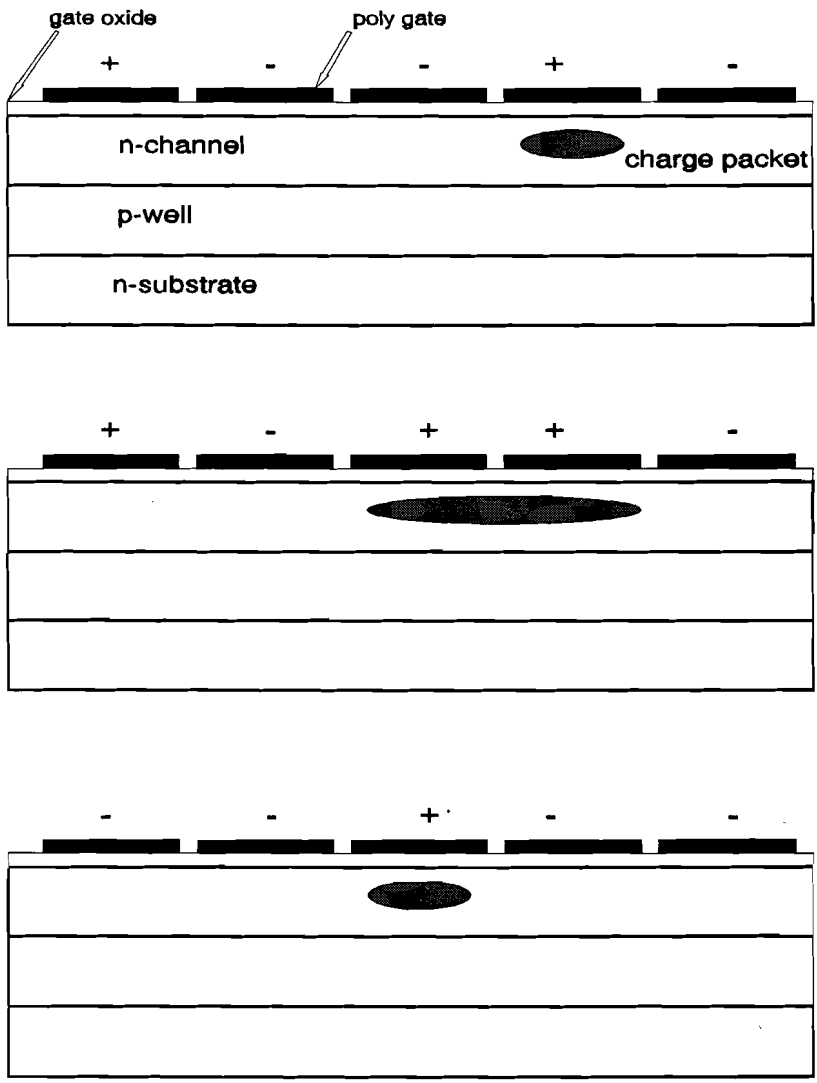

***Figure 1.2**: Cross section of a CCD, showing the transport of electron charge packets. The charge packet is transported from right to left.*

After the charge packet has been transported through the CCD register it will be dumped on the floating diffusion region (see Figure 1.3) where the charge is stored for about half a clock period. After that time the reset gate is positively biased to clamp the floating diffusion region to the drain potential. The floating diffusion region is connected to the input of an on-chip amplifier. An architecture where the floating diffusion region is the base of a pnp bipolar has been discussed by Roks et al. [10].
An alternative way to extract the charge packets from the CCD register makes use of a floating gate structure.

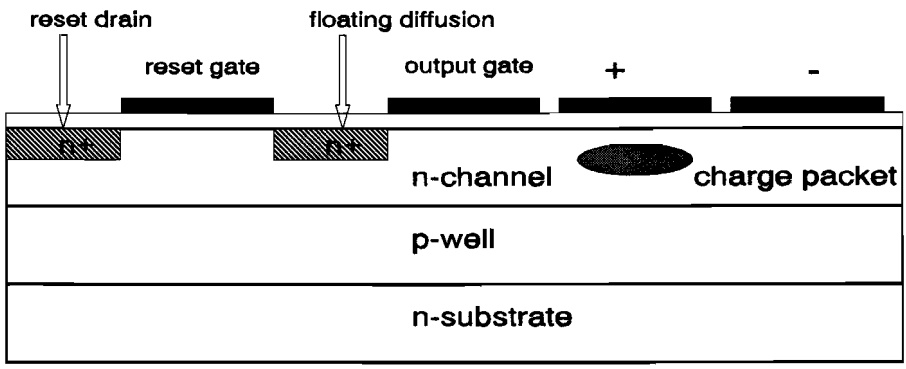

Figure 1.3: *The charge packet prior to being dumped at the floating diffusion region.*

Figure 1.4 shows a floating gate structure where the charge packet is underneath, ready to be sensed by the on-chip amplifier.
The main difference between Figure 1.3 and Figure 1.4 is the lack of reset noise in the latter structure, Carnes and Kosonocky [6].

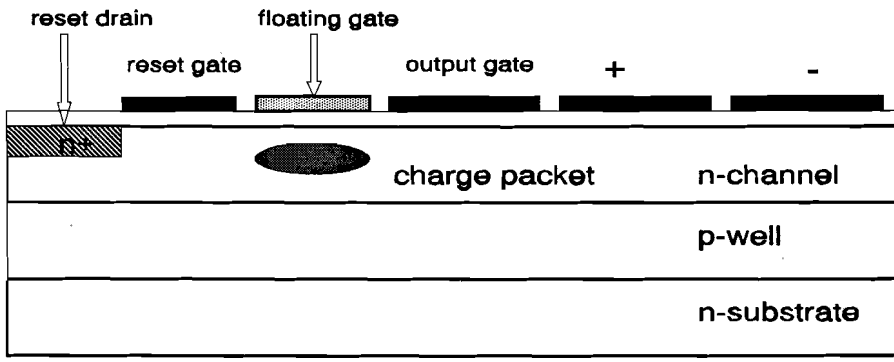

Figure 1.4: Cross section of a floating gate structure with the electron charge packet underneath a floating gate.

Several other architectures which are of the floating gate type have been reported: Brewer [11], Mutoh et al. [12], Matsunaga [13], and Roks et al. [14]-[15]

1.2 CMOS imagers

In contrast to CCD imagers described above the charge packets in a full CMOS imager (Wong [16], Fossum [17]) are not transported in a peristaltic CCD manner. In the image cell the electrons are collected in the same way as with CCDs. However, the charge of an image cell is transported through a wire as a current. Each image cell has an addressable output which is wired to a column amplifier. A common type of CMOS imager is one which has an amplifier in each image cell. This is known as active pixel readout, and every column has an integrating amplifier. During the horizontal retrace interval a row is read into the column amplifiers. A row (TV line) is read out by multiplexing the output of the column amplifiers one after another. In contrast to CCDs there is ample time for noise reduction due to the relatively long horizontal retrace interval (some μs), compared to a clock period of 55 ns. This is possible due to the huge amount of amplifiers, one for each column.

Presently no CMOS imagers are used in the professional broadcast video cameras. The reason for this is the high gain differences between pixels, column

effects, and fixed pattern noise. Even though the CMOS imager can be produced more cheaply than a CCD imager and can have processing power on-chip, it does not reach the CCDs performance. Also the ever-decreasing dimensions of the CMOS process degrades optical performance, characterised by collection depth, and causes increased gain differences between pixels. A thorough discussion about the down scaling of CMOS processes and its effects on the CMOS imager has been given by Wong [16]. The CMOS imager will be an ideal vehicle for the low-end high-volume consumer market.

1.3 Noise quantities in CCD imaging

In the field of CCD imaging it is customary to convert a noise voltage in terms of an equivalent number of electrons, Carnes and Kosonocky [6], Barbe [18]. The reason for this is that almost all the important performance parameters of a CCD imager are related to the number of electrons a charge packet contains. Sometimes those numbers are countable electrons and sometimes they are an arithmetic number and should be called an equivalent number of electrons. The conversion of a noise voltage into a number of electrons is done by making use of the sensitivity S. The sensitivity is the change in output voltage of the on-chip amplifier ΔV_{out} due to one electron being present at the detection node and is expressed as V/e.

$$\Delta V_{out} = A\ \Delta V_{in} = A\ \frac{\Delta Q}{C} = \frac{A}{C}\ q\ \Delta N = S\ \Delta N$$

In the above A is the amplifier gain, ΔQ the amount of charge one charge packet contains, C the detection node capacitance and ΔN the number of electrons one charge packet contains.
Assuming a noise voltage of 250 μV and a sensitivity of S=10 μV/e then the noise is equivalent to 25 electrons, abbreviated as 25 e. Strictly speaking this is not within the normal system for units but it is common practice in the field of CCD imaging for over 20 years now. Expressing the noise in 'electrons' is only meaningful after signal processing.

Elaborating on the above equation one can distinguish three quantities of fluctuations:

S_V [V^2/Hz] as the voltage noise spectral density of fluctuations ΔV_{out}
S_N [e^2/Hz] as the noise spectral density of fluctuations ΔN
S_Q [C^2/Hz] as the noise spectral density of fluctuations ΔQ.

$$S_V = S^2 S_N = \left(\frac{S}{q}\right)^2 S_Q$$

In general the noise voltage is expressed as $V/\sqrt{Hz}$ and the voltage noise spectral density as V^2/Hz. The above units can also be converted with the use of the sensitivity S. Now the noise "number of electrons" becomes $e/\sqrt{Hz}$ and the noise spectral density as e^2/Hz, Centen [19]. The latter will be used extensively throughout this thesis as the Noise Electron Density (NED).

$$NED = S_N$$

Another quantity that one can encounter is the ENC, which stands for: Equivalent Noise Charge, Sansen and Chang [20], Fasoli and Sampietro [21]. It is the noise spectral density of the fluctuations ΔQ integrated over the whole bandwidth and expressed in 'Coulomb',

$$ENC = \int_0^\infty S_Q(f)df$$

or 'electrons',

$$ENC = \int_0^\infty S_N(f)\,df$$

as such it is a full bandwidth parameter. In the above the filtering which is usually applied to the imager output signal is not taken into account.

One also encounters the Noise Equivalent Signal or NES, White et al. [22], with dimensions J/m^2. This too is a full bandwidth expression for the noise.

1.4 Scope of this thesis

Since the work described in this thesis covers a relatively long period of time and therefore is interwoven with others results, we first discuss our work in relation to that of others. This is followed by a summary of the various chapters.

Noise and noise optimization have always been an important issue in CCD Imaging [6], [11]-[15], [18]-[28] and even recently, Fasoli and Sampietro [21], Centen and Roks [24]. From this work it has become clear that in practical imagers the noise performance of a camera is mainly determined by the on-chip amplifier and the signal processor. The focus in this thesis is on the on-chip amplifier and signal processor. Regarding the latter it does not matter whether one focuses on IT, FIT, FT or CMOS imagers.

In [11]-[15], different types of detection nodes have been presented and the noise performance has been determined experimentally. The newer detection node types show a better noise performance. But no experiment or model has been offered to show that after optimization the newer types still have a better performance. It is the aim of Chapter 2 through to Chapter 4 to give a systematic approach for optimizing the noise of the imaging chain. The method is based on the Noise Electron Density and the use of a figure of merit for the signal processor. It will be investigated whether the method can be applied to any type of capacitive detection node. In [19]-[22], [24] and [26]-[28] noise optimization models can also be found. In addition to these papers in Chapter 2 the weakness of that the noise optimum, which determines the dimensions of the detection node transistor, is investigated with respect to noise performance.

In addition to the models presented in the latter papers the validity of the noise optimization model for any type of on-chip amplifier topology (with capacitive detection node), such as source follower and common source configurations is studied in Chapter 2.

Another extension to the above papers is the inclusion of the noise ideality factor of the MOS transistor in the on-chip amplifier. This factor is 2/3 for an ideal MOS transistor. In Chapter 3 the effect of using a non ideal MOS transistor, surface and buried channel, in the on-chip amplifier is studied.

In [6,12,13,18,25,26] the on-chip amplifier noise voltage has been calculated by integrating the noise spectral density over the on-chip amplifier bandwidth to determine the performance. Following the latter papers, a low noise level and a huge bandwidth can produce a poorer noise performance than a high noise level in a small bandwidth. Yet, in a well designed imaging chain, the one with the low noise level will always be the better of the two.

The dimensions of the MOS transistor in the first stage of the on-chip amplifier determine both the bandwidth of the amplifier and its noise. Of course one can minimize the mean squared noise voltage over the bandwidth of the on-chip amplifier. But in this case, as explained above, the wrong parameters have been optimized and a sub-optimum result occurs.

Finally, in Chapter 3, the use of surface and buried channel transistors in the

detection node is studied for its effects on sensitivity, bandwidth and noise.

Considering the signal processor as a matched filter, it is shown in Chapter 4 that the noise performance of a well designed imaging chain is given by the product of the noise spectral density of the on-chip amplifier, the noise figure of the signal processor, and the clock frequency. Generally the noise bandwidth determining the noise voltage should be determined by the signal processor rather than by the on-chip amplifier.
Although the performance of CCD signal processors has been studied extensively in [22], [23], [25] and [29]-[38], no one has derived a figure of merit as given in Chapter 4. This figure of merit has the powerful property that it has a theoretical lower bound. This figure of merit can be applied to any type of CCD signal processing irrespective of the CCD imager and type of detection node used, including CMOS imagers. In many cases this figure of merit is only determined by two ratios one between the pixel period time and the duration of the reset hold level and one between the pixel period time and the duration of the video in one pixel.

The bandwidth of the on-chip amplifier influences the shape of the output signal, determines the interference between pixels, and the ability to suppress the reset noise in the signal processor. For satisfactory operation of the imaging chain the bandwidth must be at least 3 times the clock frequency used to drive the horizontal register [23]. Above this value the noise behaviour of a well designed imaging chain does not change any more and its noise performance becomes independent of the bandwidth of the on-chip amplifier. On-chip amplifier bandwidth has become more and more important, in particular for HDTV, Theuwissen et al. [7], and high speed camera applications, Moelands et al. [3]. In the early days of CCD imaging the clock frequency was, for example, 5 MHz and the bandwidth during charge dump, at the detection node, 15 MHz. However, at present the clock frequency can be 36 MHz and the bandwidth can be as high as 158 MHz.
In [10]-[15], [18]-[21] and [24]-[28] different detection node topologies, such as floating diffusion, floating gate, junction FET, floating well, and floating surface, are described and their noise performance has been evaluated. None, except [19,24], give an analysis of the effect of the detection node on the bandwidth of the on-chip amplifier. Chapter 2 and Chapter 3 discuss the bandwidth of the on-chip amplifier and the way the distribution of capacitors at the input node (detection node plus parasitics) affect the bandwidth. These capacitors form a feedback path in the detection stage of the on-chip amplifier.

This feedback path causes the bandwidth to deteriorate. In addition the use of surface and buried channel transistors in the detection node and their effect on the bandwidth of the on-chip amplifier is studied.

Regarding the methods for experimental determination of design parameters, some novel and elegant methods are presented and discussed in Chapters 2-4. The aim is to determine important design parameters of the signal processor and on-chip amplifier.

In **Chapter 2** a model is derived to predict the noise and bandwidth behaviour of the on-chip amplifier. A parameter is introduced which is more suited for noise optimisation than the traditional ones. It is shown that this parameter is valid for any type of detection node architecture. Based on the model and the experiments conducted a second parameter is identified that has a large influence on the bandwidth of the on-chip amplifier. A special method is developed for the measurement of important design parameters.

In **Chapter 3** the effects of sensitivity, 1/f noise, white noise, and bandwidth are studied for the case of using either a buried-channel or a surface-channel MOS transistor in the input stage of the on-chip amplifier.

In **Chapter 4** the matched filter properties of the signal processor are derived with the aid of variational calculus. The derivation differs from the usual treatment given in the literature since it includes the effect of an important but often neglected noise contribution. Now a better solution for the matched filter can be found. The properties of the matched filter when excited with white noise and more generally with white and 1/f noise are studied. Based on this study a noise figure of merit for the signal processor is introduced and a lower bound is derived. For three types of signal processors the figure of merit is derived.

The basis of **Chapter 5** is an apparently academic question: "Is the noise performance of the current output of a CCD imager worse than the classical voltage output?" The discussion results in a novel way of using a floating diffusion detector. In fact we present a way of using a floating diffusion detector without generating reset noise. Criteria are established which determine the performance of the new readout scheme.

References

[1] A.Theuwissen. *"Solid-State Imaging with Charge-Coupled Devices"*. Kluwer Academic Publishers 1995; ISBN 0-7923-3456-6.

[2] M.Collet, *"Solid State Image Sensors"*. Proceedings SPIE Vol. 591, 1985, pp 82-93, 26-27 November 1985, Cannes, France.

[3] T.Moelands, P.Centen, R. Voet. *"A High Speed Sports Action Camera System"*. Technical Papers International Broadcast Convention, pp 86-92, Amsterdam, September 11-15, 1998.

[4] E.Roks. *"Advanced CCD Imaging by Opposite Carrier Interaction"*. Ph.D. Thesis Enschede, ISBN 90-74445-13-6, 1994

[5] G.Kreider. *"An mKxnK Modular Image Sensor Design"*. IEDM Technical Digest 1995, pp 155-158.

[6] J.Carnes and W.Kosonocky, *"Noise Sources in Charge-Coupled Devices"*. RCA Review, vol. 33, pp. 327-343, June 1972.

[7] A.Theuwissen, H.Peek, P.Centen, R.Boesten, J.Cox, P.Hartog, A.Koskhoorn, H. van Kuijk, B.O'Dwyer, J.Oppers, F.Vledder. *"A 2.2 Mpixel FT-CCD imager, according to the Eureka HDTV-standard"*. IEDM Tech. Dig. 1991 pp. 167-170.

[8] J.Blankevoort, H.Blom, P.Brouwer, P.Centen, B. van de Herik, R.Koppe, A.Moelands, J. van Rooy, F.Stok and A.Theuwissen. *"A High-Performance, Full Bandwidth HDTV Camera Applying the First 2.2 Million Pixel Frame Transfer CCD Sensor"*. SMPTE Journal, Vol. 103, No. 5, 1994, pp. 319-329.

[9] S.Spitzer, J.Toker, A.Moelands, P.Centen, J. van Rooy, B.Gerovac. *"Design and Implementation of a 3-CCD State of the Art, 750-line HDTV Progressive Scan Broadcast Camera"*. Proc. NAB 1996, pp. 171-178.

[10] E.Roks, P.Centen, L.Sankaranarayanan, J.Slotboom, J.Bosiers, W.Huinink. *"A Bipolar floating-base detector (FBD) for CCD Image Sensors"*. Technical Digest IEDM92, pp 109-112, San-Francisco, Dec 13-16, 1992.

[11] R.Brewer, *"A Low Noise CCD Output Amplifier"*, Technical Digest IEDM79, pp. 610-612, Washington DC, Dec 3-5, 1979.

[12] N.Mutoh, M.Morimoto, M.Nishimura, N.Teranishi and E.Oda, *"New Low Noise Output Amplifier for High Definition CCD Image Sensor"*, Technical Digest IEDM89, pp. 173-176, Washington DC, Dec 3-6, 1989.

[13] Y.Matsunaga, *"A High Sensitivity Output Amplifier For CCD Image Sensor"*, Technical Digest IEDM87, pp. 116-119, Washington DC, Dec 6-9, 1987.

[14] E.Roks, P.Centen, J.Bosiers, W.Huinink. *"The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD image sensors"*. IEEE Trans. Electron Devices, vol. ED-43, No. 9, pp. 1583-1591, 1996.

[15] E.Roks, J.Bisschop, P.Centen, L.Sankaranarayanan. *"Theory and Modelling of the Floating-Surface Detector: An Enhanced CCD Output Structure"*. Philips Journal of Research, Vol. 48. No. 3, 1994, pp. 233-260.

[16] H.S.Wong, *"Technology and Device Scaling Considerations for CMOS Imagers"*. IEEE Trans. Electron Devices, vol. ED-43, no. 12, pp. 2131-2142, December 1996.

[17] E.R.Fossum, *"CMOS Image Sensors: Electronic Camera-On-A-Chip"*. IEEE Trans. Electron Devices, vol. ED-44, no. 10, pp. 1689-1698, October 1997.

[18] D.Barbe, *"Imaging Devices Using the Charge-Coupled Concept"*. Proceedings of the IEEE, pp. 38-67, Jan. 1975.

[19] P.Centen, *"CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions"*. IEEE Trans. Electron Devices, vol. ED-38, no. 5, pp. 1206-1216, May 1991.

[20] W.Sansen, Z.Y.Chang, *"Limits of Low Noise Performance of Detector Readout Front Ends in CMOS Technology"*, IEEE Trans. Circuits and Systems, vol. CAS-37, no. 11, pp. 1375-1382, November 1990.

[21] L.Fasoli, M.Sampietro, *"Criteria for setting the Width of CCD Front End Transistor to Reach Minimum Pixel Noise"*, IEEE Trans. Electron Devices, vol. ED-43, no. 7, pp. 1073-1076, July 1996.

[22] M.White, D.Lampe, F.Blaha, I.Mack, *"Characterization of Surface Channel CCD Image Arrays at Low Light Levels"*, IEEE Journal of Solid-State Circuits, vol. SC-9, No. 1, February 1974, pp 1-13.

[23] P.Centen. *"CCD signal processing for better signal-to-noise ratio"*. Philips Eindhoven, The Netherlands, TN 180-88, May 1988. Internal report.

[24] P.Centen, E. Roks. *"Characterization of Surface- and Buried-Channel Detection Transistors for On-Chip Amplifiers"*. Technical Digest IEDM97, pp.193-196, San Francisco, Dec 7-10, 1997.

[25] J.Hynecek, *"High-Resolution 8-mm CCD Image Sensor with Correlated Clamp Sample and Hold Charge Detection Circuit"*. IEEE Trans. Electron Devices, vol. ED-33, no. 6, pp. 850-862, June 1986.

[26] J.Hynecek, *"Design and Performance of a Low-Noise Charge Detection Amplifier for VPCCD Devices"*. IEEE Trans. Electron Devices, vol. ED-31, no. 12, pp. 1713-1719, Dec. 1984.

[27] N.Teranishi, N.Mutoh, *"Partition Noise in CCD Signal Detection"*. IEEE Trans. Electron Devices, vol. ED-33, no. 11, pp. 1696-1701, November 1986.

[28] D.Heidtmann, F.Yang, *"The effects of FET dimensions and bias on the noise performance of CCD output amplifier"*, Electronic Imaging 1987, pp. 248-253, Boston, Nov 2-5, 1987.

[29] D.Hegyi and A.Burrows, *"Optimal sampling of charge-coupled devices"*, Astronomical Journal, Vol.85, No. 10, pp 1421-1424, Oct. 1980

[30] G.Hopkinson and D.Lumb, *"Noise reduction techniques for CCD image sensors"*, J. Phys. E: Sci. Instrumm., Vol. 15, 1982, pp 1214-1222.

[31] P.Levine, *"Low-Noise CCD Signal Recovery"*. IEEE Trans. Electron Devices, vol. ED-32, no. 8, pp. 1534-1537, Aug. 1985.

[32] W.Buttler, B.Hosticka and G.Lutz, *"Noise Filtering for Readout Electronics"*, Nuclear Instruments and Methods in Physics Research, A288 (1990), pp 187-190

[33] M.Ohbo, I.Akiyama, T.Tanaka, *"A new suppression method for high-definition CCD cameras"*. IEEE Trans. on Consumer Electronics, Vol. 35, No. 3, August 1989, pp. 368-374.

[34] H.Wey and W.Guggenbühl, *"An improved Correlated Double Sampling Circuit for low Noise Charge-Coupled Devices"*, IEEE Transactions on Circuits and Systems, Vol. 37, No. 12, december 1990, pp 1559-1565.

[35] T.McCurnin, L.Schooley, G.Sims. *"Charge-coupled device signal processing models and comparisons"*. Journal of Electronic Imaging, vol 2(2), pp. 100-107, April 1993.

[36] C.Enz, *"Analyses of low frequency noise reduction by auto-zero technique"*, Electronic Letters, Vol. 20, No. 23, pp 959-960, Nov 1984.

[37] M.v.Buul and P.Centen, *"Sampling Circuit"*, PCT application WO 96/01475, January 1996.

[38] R.Kansy, *"Response of a correlated double sampling circuit to 1/f noise"*, IEEE Journal of Solid-State Circuits, vol. SC-15, June 1980, pp 373-375.

Chapter 2

ON-CHIP AMPLIFIER
Amplification and conversion[1]

2.1 Introduction

The main purpose of the on-chip amplifier in a CCD imager is the conversion of a charge packet into a voltage or a current. In addition to this conversion the on-chip amplifier must exhibit a good noise performance and it must be capable of driving an external load at the pixel frequency.

A popular way of detecting the charge of the CCD channel is to use a floating diffusion region [1,2] which, together with the input of the on-chip amplifier, forms a (capacitive) detection node. The change in the detection node voltage (V=Q/C) when a charge packet enters the node is sensed by the on-chip amplifier.

In order to achieve a large bandwidth one often encounters a two-stage source follower amplifier, the typical structure of which is shown in Figure 2.1. The first stage consists of a source follower (M_1) and a current sink (M_{c1}) for biasing purposes. Both determine the noise performance. The second stage (M_2) drives

---

[1] *Based on the publication: P.Centen, "CCD-On-Chip Amplifiers: Noise Performance versus MOS transistor Dimensions". IEEE Trans. Electron Devices, vol. ED-38, no. 5, pp. 1206-1216, May 1991.*

the load. For HDTV CCD imagers as many as three source follower stages can be needed [3].
The reset FET (M_r) is connected to the floating diffusion region (FD) discussed above. In the off-state it can collect the next charge packet and in the on-state it resets the detection node to a reference voltage (V_{RD}). The drain of the reset FET is a current output (all signal charge appears here) but in general is not used as such (Chapter 5).
The bias voltage (V_{CS}) at the gate of the current sink (M_{cl}) determines the bias current (I) of the first stage. This gate can be used as a test signal injection point to measure both the ratio (Θ_n) between the total capacitance (C_{tot}) and the detection node capacitance (C_{det}) and the bandwidth in the reset FET off- and on-state. The total capacitance is defined as the capacitance between the gate of the detection node transistor and all the other nodes. The detection node capacitance is the effective capacitance of the detection node with the gain of the first stage taken into account.
When the reset FET is off, as is the case when charge is dumped at the detection node, there is a large (capacitive) feedback from the source to the gate of M_1. Due to this phenomena the bandwidth is decreased during charge dumping. This decrease is controlled by the ratio between the total capacitance of the detection node C_{tot} and the detection node capacitance C_{det}. The latter capacitance (C_{det}) consists for a small part of the floating diffusion region capacitance and for a large part of stray and wiring capacitance, and the capacitance of the first MOS transistor. Nowadays much attention is paid to the design of low-capacitance detection nodes and scaling rules become important. Enlarging a structure on silicon not only increases the active MOS transistor capacitances but also the wiring and stray capacitance. It will be shown that the noise performance is proportional to the total capacitance C_{tot} of the detection node and the equivalent noise voltage of the first MOS transistor.

The designer of a signal processor generally uses its noise spectral density to determine the (noise) optimum filter. In the case of a CCD imager, where electrons are usually the signal, it is most natural to use the equivalent Noise Electron Density as a representation of the noise spectral density. The Noise Electron Density [e^2/Hz] is the ratio between the voltage noise spectral density [V^2/Hz] and the sensitivity squared [$(V/e)^2$].
In contrast to earlier reports in literature [4,5] about noise optimization, the approach in this chapter is quite different: *"the noise optimization is not based on minimizing the equivalent noise electrons but on minimizing the equivalent Noise Electron Density".*

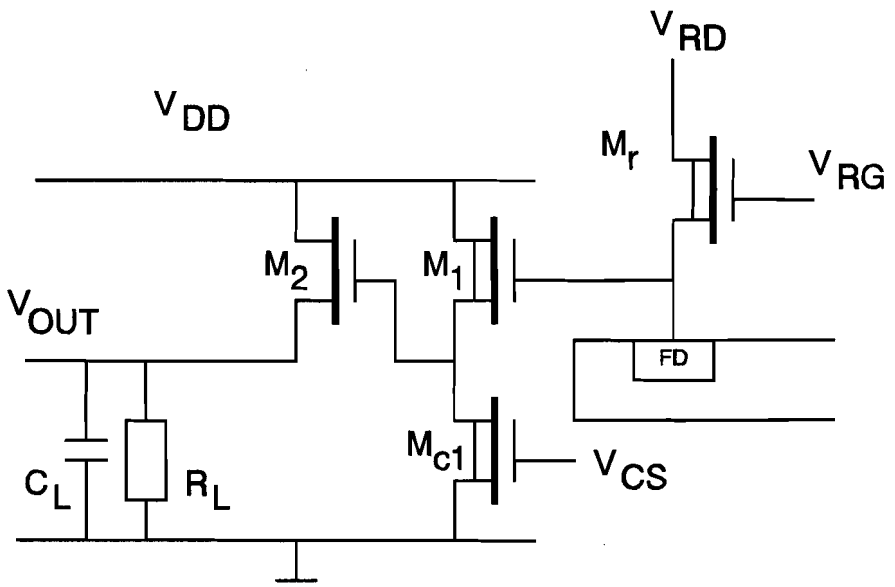

Figure 2.1: A typical on-chip amplifier for CCD imagers, with a floating diffusion detection node.

It will be shown that the optimum, with respect to signal-to-noise ratio, is valid for each type of signal processing.
Since the signal processors that are nowadays available [2,5,6,7,8,9], such as Correlated Double Samplers, suppress the reset noise sufficiently it is not taken into consideration.
In a well-designed on-chip amplifier the noise contribution of the first stage exceeds that of the second stage; therefore most attention will be paid to the first stage.
It is the goal of this chapter to establish both in theory and in practice the optimum values of the critical parameters of the detection node MOS transistor (the first source follower); namely, the bandwidth, the channel width and length, the bias current, the total capacitance, and the equivalent Noise Electron Density.
In **Section 2.2** the first stage will be analyzed. First the charge dumping and

resetting of the floating diffusion region will be discussed, then the time response will be calculated, and then the 3 dB bandwidth in the reset FET on- and off-state. Finally the noise in the on- and off- state will be discussed.
It will be shown that the ratio between total capacitance and detection node capacitance $\Theta_n=C_{tot}/C_{det}$ is an important design parameter for the bandwidth. A method for measuring the latter ratio is discussed in **Section 2.3**. In **Section 2.4** a second important design parameter is introduced. It is the concept of equivalent Noise Electron Density. A general expression will be derived which is valid for both types of capacitive detection node, destructive and non-destructive [1,2,10,11,12,13,14].
In **Section 2.5** a calculation for noise optimization is presented based on the concept of the equivalent Noise Electron Density. The optimum dimensions and bias current of the detection node MOS transistor and current sink are derived for the case where thermal noise is dominant.
In **Section 2.6** a comparison with some experimental results is presented.
Finally, the theory developed in the previous sections, together with the experimental results, is applied in **Section 2.7**. It describes an improvement in the design of the on-chip amplifier of the FT5 SDTV CCD imager [15] and discusses the design of the on-chip amplifier for the FT8 HDTV CCD imager [3].

2.2 Analysis of the first stage: a source follower

2.2.1 Small signal equivalent circuit.

The small signal equivalent diagram of the first stage consisting of a source follower M_1 and a current sink M_{c1} is given in Figure 2.2. The capacitance between the gate and ground (C_1) is made up of the floating diffusion capacitance (FD), the drain overlap capacitance ($C_{gd,o}$) and some stray and wiring capacitances. The capacitance between the gate and the source (C_2) of M_1 consists of the source overlap capacitance ($C_{gs,o}$), the active channel capacitance, and stray and wiring capacitances. At any biasing point the following small signal parameters are defined: the transconductance (g_1) of M_1, a load resistance (R_o) which includes the output resistance of M_1 and M_{c1}, and a capacitive load (C_o) which also includes the input capacitance of the second stage. The current noise source (i_n) represents the noise of both the follower M_1 and sink M_{c1}. Finally, i_i is the current flowing into the detection node. In the reset FET off-state charge is dumped onto the detection node. By definition the current i_i is the time derivative of the charge of the detection node. The reset FET is omitted

in the diagram. The loading effect of the second stage is represented by R_o and C_o.

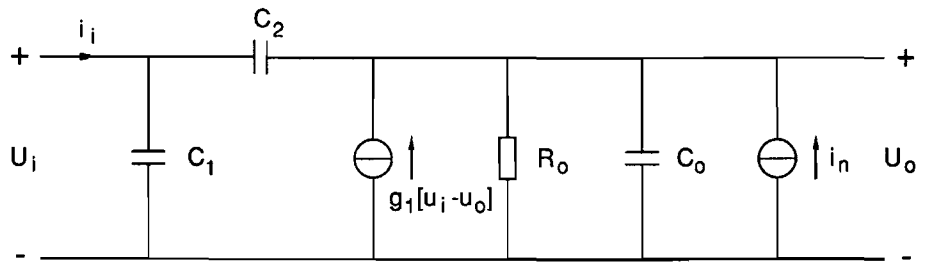

Figure 2.2: The small signal equivalent diagram of the first stage of the on-chip amplifier.

2.2.2 Charge packet response: rise and fall time.

There exists an asymmetry between the reset FET on- and off-state. In the on-state the detection node is almost short circuited. When it is placed in the off-state the detection node floats and is very high ohmic; from this moment on an effective feedback exists from the source to the gate of follower M_1 due to C_2, which forms a capacitive divider with C_1.
In the frequency domain the node equations written in matrix form are:

$$\begin{bmatrix} I_i \\ I_n \end{bmatrix} = \begin{bmatrix} j\omega(C_1+C_2) & -j\omega C_2 \\ -(j\omega C_2 + g_{m1}) & \frac{1}{R_o} + g_{m1} + j\omega(C_o+C_2) \end{bmatrix} \begin{bmatrix} U_i \\ U_o \end{bmatrix} \qquad (2.1)$$

I_i and I_n are the Fourier Transforms of i_i and i_n, respectively.
In practice the capacitive load C_o is much larger than the gate-to-source capacitance of M_1 ($C_o >> C_2$). Furthermore, the 3 dB bandwidth (F_3) caused by the load capacitance is well below the transit frequency ($F_T = g_{m1}/(2\pi C_2)$) of the detection node MOS transistor. Typically F_T has a value of 500 MHz - 1 GHz.
A derivation of the transfer functions when using the above approximations is given in Appendix A. The result will be used in the remainder of this section.

In the reset FET off-state charge is dumped on the floating diffusion region. The frequency response of the first stage is calculated by solving the matrix equation (2.1). By definition the input current is the time derivative of the charge. After Fourier transformation the relation between the input current I_i and the charge packet $Q(\omega)$ is:

$$I_i = j\omega Q(\omega) \tag{2.2}$$

Assuming $I_n(\omega)=0$, the response at the source (U_o) becomes

$$U_o = \frac{A_{10}}{1+j\omega\tau\theta_n} \cdot \frac{Q(\omega)}{C_{det}} \tag{2.3}$$

(see Appendix A)

In the above the following definitions have been used:

DC gain of the first source follower stage

$$A_{10} = \frac{g_{m1} R_o}{1 + g_{m1} R_o} \tag{2.4}$$

time constant of the output

$$\tau = \frac{C_o}{g_{m1}} A_{10} \tag{2.5}$$

and detection node capacitance

$$C_{det} = C_1 + (1 - A_{10})C_2 \tag{2.6}$$

The ratio between the total capacitance $C_{tot}=C_1+C_2$ and the detection node capacitance C_{det} is Θ_n and determines the feedback between the source of M_1 and the detection node in the reset FET off-state

$$\theta_n = \frac{C_{tot}}{C_{det}} \tag{2.7}$$

In the case of a source follower the ratio Θ_n is always larger than one. With a

common source configuration it is possible to obtain values for Θ_n smaller than one.

The charge packet in a CCD imager usually consists of electrons. Let us assume that one charge packet with a charge -qN is dumped on the floating diffusion region at t=0. Using the Dirac impulse function $\delta(t)$ this is written as

$$i_i(t) = -qN\delta(t) \tag{2.8}$$

The effect of such a current impulse is a step-wise change in charge for which the Fourier transform equals

$$Q(\omega) = -qN\left(\pi\,\delta(\omega) + \frac{1}{j\omega}\right) \tag{2.9}$$

The source voltage U_o as a function of time is calculated making use of the inverse Fourier transformation of equation (2.3) after substituting equation (2.9).

Introducing the sensitivity

$$S = A_{10}\,\frac{q}{C_{det}} \tag{2.10}$$

the time response is given by

$$u_o(t) = V_o - S\,N\left[1 - e^{-\frac{t}{\tau\Theta_n}}\right] \qquad t \geq 0 \tag{2.11}$$

At t=0 the output voltage has the reference value V_o; the stationary value (t = ∞) is $u_o(t=\infty) = V_o - S{\cdot}N$. The output swing due to a charge packet of N electrons is therefore $S{\cdot}N$. This explains the reason for introducing the sensitivity through equation (2.10). The stationary value means that S equals the change in output voltage due to a charge packet of one electron. The sensitivity of the detection node is determined by the capacitance between the gate and the source of the detection node MOS transistor (C_2), the capacitance between the gate and ground (C_1), and the voltage gain of the detection node MOS transistor (A_{10}). Because a source follower configuration is used only a fraction of the gate-to-source capacitance C_2 contributes to the detection node capacitance (equation (2.6)). The fall time of the output signal is $\tau\,\Theta_n$.

Before commenting on the fall time, the time response of the charge draining off in the reset FET on-state will first be calculated.
In the on-state the charge that has been dumped at the floating diffusion region is drained to the reset drain terminal (V_{RD} in Figure 2.1). The response for the on-state is arrived at by solving equation (2.1) under the condition of $I_n(\omega) = 0$ (Appendix A)

$$U_o(\omega) = \frac{A_{10}}{1 + j\omega\tau} U_i(\omega) \qquad (2.12)$$

Next we assume that at t=0 the output voltage has reached its stationary value V_o-S·N and that for t>0 the reset FET is switched on, clamping the floating diffusion region at the reset drain potential. The time response is then given by:

$$u_o(t) = V_o - S\,N\,e^{-\frac{t}{\tau}} \qquad t \geq 0 \qquad (2.13)$$

Note that the fall time $\tau\Theta_n$ in equation (2.11) is a factor $\Theta_n = C_{to}/C_{det}$ larger than the rise time τ of equation (2.13).

2.2.3 Bandwidth and Θ_n.

Instead of calculating the time response one can focus on the transfer function and determine the 3 dB bandwidth. In the reset FET on-state the transfer function is given by equation (2.12). Therefore the 3 dB bandwidth in the on-state has a value:

$$F_3(on) = \frac{1}{2\pi\tau} \qquad (2.14)$$

On the other hand the 3 dB bandwidth in the reset FET off-state follows from equation (2.3)

$$F_3(off) = \frac{1}{2\pi\tau\theta_n} \qquad (2.15)$$

and therefore is (much) smaller than in the on-state.

The fact that the ratio $\Theta_n=C_{tot}/C_{det}$ determines the loss of bandwidth is an important result. It is therefore one of the major design parameters for amplifiers on CCD imagers. In the design of high speed on-chip amplifiers one should focus on a low-Θ_n design. Practically Θ_n ranges from 1.5 to 3.5.
For example, when $\Theta_n=3.3$ and the bandwidth during charge dumping is 15 MHz than the bandwidth increases to 50 MHz when the floating diffusion region is clamped.

In order to measure the bandwidth and the DC gain of the on-chip amplifier the on-state is often used to apply a test signal at the reset drain. In this example the measured bandwidth of 50 MHz would be far too optimistic.

2.2.4 Noise in the Reset FET on- and off-state.

The noise current i_n induces a voltage swing U_o at the source of M_1 (Figure 2.2). With the substitution of an equivalent noise voltage $e_n=i_n/g_{mc}$ equation (2.1) can be solved for the case $C_o>>C_2$ under the condition that the reset FET in the on-state represents a short circuit ($U_i=0$). The solution can be written as

$$U_o(\omega) = \frac{A_{10}}{1 + j\omega\tau} e_n \qquad \textbf{(2.16)}$$

However, in the reset FET off-state with $I_i=0$, we have

$$U_o(\omega) = \frac{A_{10}}{1 + j\omega\tau\theta_n} \theta_n e_n \qquad \textbf{(2.17)}$$

Comparing equation (2.16) in equation (2.17), note that the output noise of the first stage has increased by the factor Θ_n and that at the same time the bandwidth has decreased by the same factor.
The asymmetry between off-state and on-state has already been discussed for the charge handling (equations (2.11) and (2.13)).
This is a well-known result from feedback theory which states that for a given system the gain-bandwidth product is (almost) a constant.
The same conclusions apply for the situation in which the gate of the current source V_{CS} is used as an input to inject a test signal.

The noise of the source follower and the current sink. The noise current i_{nc} of sink M_{c1} and of the detection node MOS transistor M_1, i_{n1}, together determine

the noise i_n of the first stage.
That is,

$$i_n^2 = i_{n1}^2 + i_{nc}^2 \tag{2.18}$$

Using the definition of the equivalent noise voltage for M_1

$$e_{n1} = \frac{i_{n1}}{g_{m1}} \tag{2.19}$$

and M_{c1}

$$e_{nc} = \frac{i_{nc}}{g_{mc}} \tag{2.20}$$

one obtains for the total equivalent noise voltage e_n

$$e_n^2 = e_{n1}^2 + \left[\frac{g_{mc}}{g_{m1}}\right]^2 e_{nc}^2 \tag{2.21}$$

The ratio g_{mc}/g_{m1} is the voltage gain of the cascode section M_{c1} and M_1.
In order to obtain a low noise level, it is trivial but very important to note that this gain must be small.

2.3 Procedure to determine C_{tot} and Θ_n.

For measurement purposes a second input, other than the reset drain, is usually available: the gate of the current source (M_{c1} in Figure 2.1).

Given the following two constraints (equation (2.22))

- the reset FET (M_r) has a resistance R,
- and the current source M_{c1} has a transconductance g_{mc},

$$\frac{U_i}{I_i} = -R$$
$$I_n = -g_{mc}\, U_{cs} \tag{2.22}$$

and substituting the above in equation (A1) of Appendix A, the transfer function between the output (U_o) and the current source gate (U_{cs}) is found to be

$$\frac{U_o}{U_{cs}} = \frac{g_{mc}}{g_{m1}} A_{10} \frac{1 + j\omega C_{tot} R}{1 + j\omega \left(\frac{A_{10}}{g_{m1}} (C_0 + C_2) + C_{det} R \right) - \omega^2 \frac{A_{10}}{g_{m1}} R (C_0 C_{tot} + C_2 C_1)} \qquad (2.23)$$

The transfer function has one zero and two poles.

In Figure 2.3 the transfer function is calculated with the following parameter values substituted in equation (2.23): C_1=13 fF, C_2=35 fF, A_{10}=0.90, C_o=350 fF, g_{m1}=10^{-4} Ω^{-1}, g_{mc}=g_{m1}/4 and R=300 MΩ.
(C_{tot}=C_1+C_2=48 fF, C_{det}=C_1+(1-A_{10}).C_2=16.5 fF, and Θ_n=C_{tot}/C_{det}=2.9)

For frequencies far below 1/(2 π R C_{tot}) the transfer function is approximately

$$\frac{U_o}{U_{cs}} = \frac{g_{mc}}{g_{m1}} A_{10} = 0.225 \qquad (2.24)$$

For frequencies between 1/(2 π R C_{tot}) and 1/(2 π R C_{det}) there is a transition region in which the gain increases and stabilizes at

$$\frac{U_o}{U_{cs}} = \frac{g_{mc}}{g_{m1}} A_{10} \theta_n = 0.654 \qquad (2.25)$$

For still higher frequencies bandwidth limiting occurs above g_{m1}/(2 π C_o Θ_n A_{10}).

The value of the reset FET channel resistance, which is determined by the bias voltage (V_{RG}), must be chosen so that the transition from equation (2.24) to equation (2.25) occurs well below the point where bandwidth limiting occurs. In the example 300 MΩ for the reset FET channel resistance was a suitable value. The exact value is not critical.
The importance of the above derivation lays in the fact that it is possible to determine the ratio Θ_n=C_{tot}/C_{det} via a single measurement in which the bias conditions of the on-chip amplifier are not changed.

Since C_{det} and Θ_n are measurable, the total capacitance C_{tot}, which controls the noise performance and bandwidth, can be measured and the optimum layout can be established.

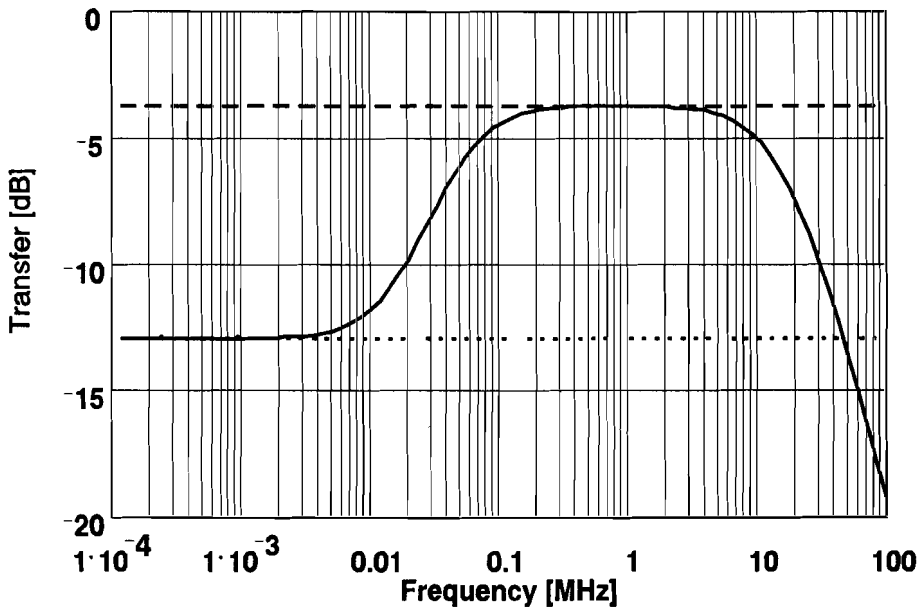

Figure 2.3: *The transfer function between the current source gate and the output for a reset FET channel resistance of 300 MΩ. The dotted and the dashed lines are the asymptotic values and their difference is the value of* $\Theta_n = C_{tot}/C_{der}$

For cases in which no network analyzer is available a second measurement technique is to determine the DC gain from the current source gate V_{CS} to the output in the reset FET off-state and on-state.

The reset FET channel resistance is determined by the value of the reset gate voltage. In equation (2.23) the following values for the reset FET channel resistance can be substituted: R=0 and R=∞. These are respectively obtained by setting a high and low value for V_{RG}.

After substituting R=0, the gain in the reset FET on-state is

$$\frac{U_o}{U_{cs}} = \frac{g_{mc}}{g_{ml}} A_{10} \frac{1}{1 + j\omega \frac{A_{10}}{g_1} (C_0 + C_2)} \qquad (2.26)$$

and in the reset FET off-state (R=∞)

$$\frac{U_o}{U_{cs}} = \frac{g_{mc}}{g_{ml}} A_{10}\, \theta_n \frac{1}{1 + j\omega \frac{A_{10}}{g_1} \theta_n \left(C_0 + \frac{C_2 C_1}{C_1 + C_2} \right)} \qquad (2.27)$$

Therefore the ratio between the gain in the on- and off-states for low frequencies is Gain(off)/Gain(on)=Θ_n=C_{tot}/C_{det}.

2.4 Equivalent Noise Electron Density (NED)

2.4.1 Equivalent noise electrons versus NED

In CCD imagers it is common practice to express the noise performance as the number of equivalent noise electrons. This figure of merit is determined by the product of the square root of a noise level (spectral density) and an equivalent noise bandwidth. A low figure can be obtained in two ways: a low noise level or a small equivalent noise bandwidth. In optimizing the design it is better to separate the two effects and to use the Noise Electron Density as a figure of merit which is determined by the image sensor. The equivalent noise bandwidth is determined by off-chip signal processing.

One usually expresses the noise level as an equivalent noise voltage in V/√Hz or as a noise current in A/√Hz. These units squared are called the voltage spectral density V^2/Hz and the current spectral density A^2/Hz. In the case of a CCD imager with its electrons (charge) as the signal it is more appropriate to express the noise in [electrons^2/Hz] for which we propose the name equivalent Noise Electron Density (NED). This value can be given in two states, with the reset FET on or off. Of course the value in the off-state is more important because this is the state in which charge is dumped on the detection node. This is also the state in which the signal processor suppresses reset noise and 1/f noise [2,5,6,7,8,9] and amplifies the charge signal.

Dividing equation (2.17) by equation (2.3), where the charge Q is taken to be the unit charge q, and using equation (2.7), the expression for the NED becomes

$$NED(f) = \left[\frac{e_n(f)\,C_{tot}}{q}\right]^2 \qquad (2.28)$$

This equation, because it is valid for each frequency, also includes 1/f noise. From the above one can conclude that a requirement for a noise optimum is that the capacitances which are independent of the transistor geometry and are part of C_{tot} have to be made as small as possible. Furthermore, neither the gain A_{10} of the first stage nor the detection node capacitance C_{det} appears directly in the formula. Expression (2.28) can be generalized to any capacitive detection node [1,2,10,11,12,13,14], shown in Figure 2.4a, when the following conditions are fulfilled:

- the noise of the detection node MOS transistor is dominant and
- the only high ohmic node in the charge detection system during charge sensing is the gate of the detection node MOS transistor.

One can show that the Noise Electron Density is proportional to the sum of all capacitances connected to this gate multiplied by the intrinsic noise properties e_n of the detection node MOS transistor.

The proof is as follows:

The current noise source i_n across the MOS transistor source and drain can be shifted towards the gate by the use of $e_n=i_n/g_m$, (Figure 2.4b).

Applying:

• *The Blakesly transformation (see Figure 2.5):*

-"A single voltage source in one branch may be shifted through a node by removing the voltage source from that branch and adding it to every other branch connected to that node" (Figure 2.5a)

-"A single current source between two nodes can be split up into two current sources in series and the middle point can be connected to an arbitrary third node" (Figure 2.5b).

and

• *the Norton-Thevenin transformation to change a voltage source into an equivalent current source or visa versa.*

we arrive at the equivalent circuit depicted in Figure 2.6.

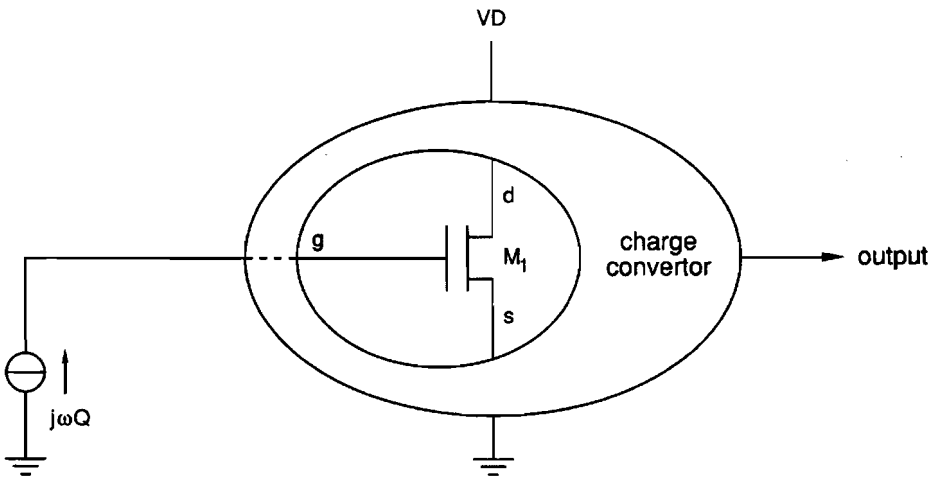

Figure 2.4a: *General scheme of a capacitive detection node with a MOS transistor as the first stage of the charge-convertor (M_1). The charge dumped on the detection node is represented by a current source jωQ.*

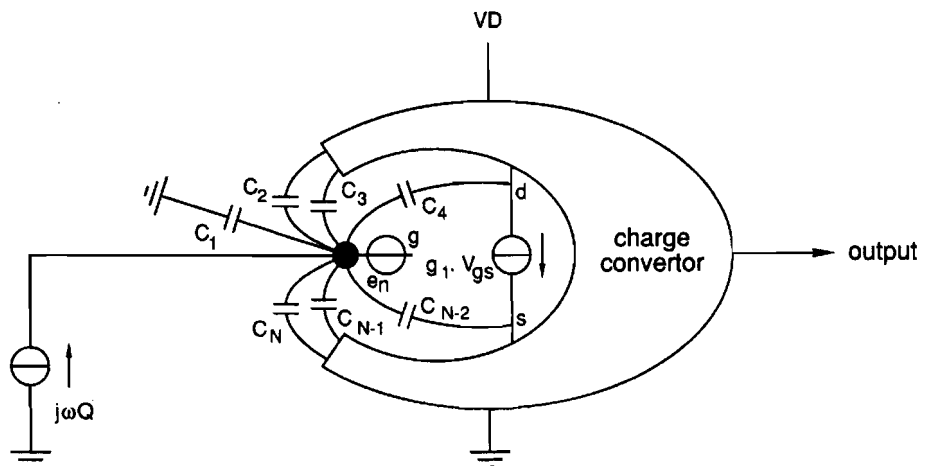

Figure 2.4b: *Similar to 2.4a but now including a small signal replacement. The noise of the detection node MOS transistor (trans-conductance g_1) is represented by an equivalent noise voltage e_n.*

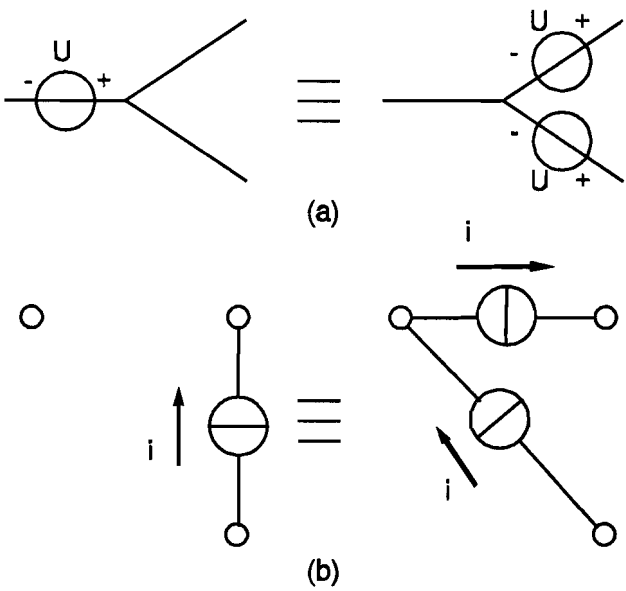

Figure 2.5: *(a) represents the Blakesly transformation of a single voltage source (U) in one branch through a node into the remaining branches.*
(b) is the transformation of a current source (i) between two nodes into two current sources between those two nodes and a third one.

The detection node is represented in Figure 2.6 with its capacitances C_i and two injecting current sources, one of which is the charge j ω Q and the other the noise current j ω C_{tot} e_n). The total capacitance is

$$C_{tot} = \sum_{i=1}^{N} C_i \qquad (2.29)$$

In Figure 2.6 the noise current is j ω C_{tot} e_n and the current noise spectral density amounts to (ω C_{tot} e_n)^2 [A^2/Hz].

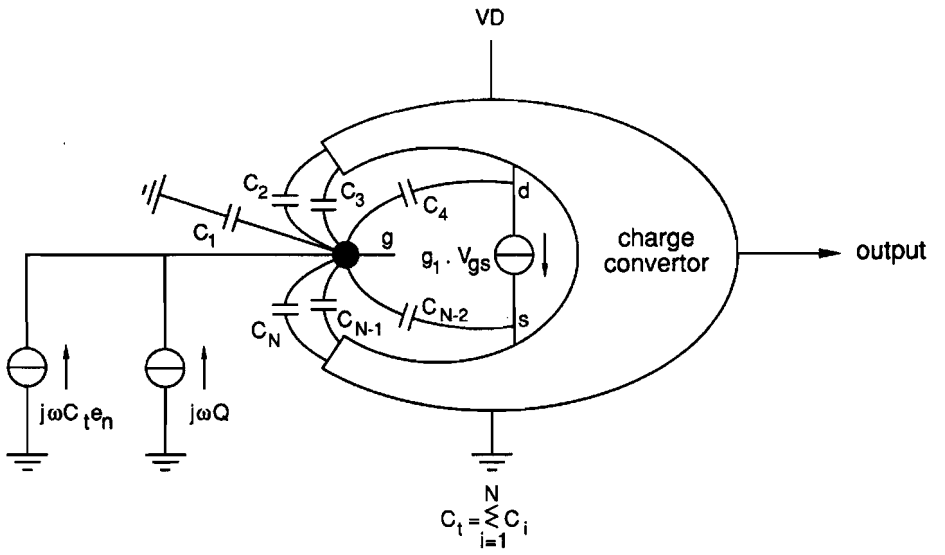

Figure 2.6: *Similar to 2.4b but with the equivalent noise voltage (e_n) of the detection node MOS transistor transformed into a current noise source at the detection node.*

Instead of the current noise spectral density one could also express it as a charge noise spectral density with dimension [A^2s^2/Hz] since the current is the time derivative of the charge $(C_{tot} \cdot e_n)^2$ or as Noise Electron Density by dividing the above equation by the unit charge q

$$NED = \left[\frac{e_n \, C_{tot}}{q}\right]^2 \qquad (2.30)$$

The units in equation (2.30) are [1/Hz] or, because of conventions in use in the CCD imaging field as [e^2/Hz]. (see Section 1.3). The above equation is independent of circuit topology!

2.4.2 Equivalent noise electrons and signal processing.

Depending on the camera system one wants to minimize the noise in a bandwidth (B_m) of 0.2-5 MHz (PAL) or 0.2-4.2 MHz (NTSC) or 0.4-30 MHz (HDTV). In general the on-chip amplifier noise spectrum contains a 1/f portion. Many CCD imager signal processors suppress the 1/f noise and the reset noise [2,4,6,7,8,9]. One can show (see Chapter 4) that the number of equivalent noise electrons squared due to thermal noise after signal processing in a bandwidth (B_m) can be written as the product of the Noise Electron Density (NED) before signal processing, a noise increasing factor (M) due to signal processing, and the effective bandwidth $B_{m,eff}$:

$$N_{proc}^2 = M \cdot NED \cdot B_{m,eff} \tag{2.31}$$

Generally M and $B_{m,eff}$ depend on the signal processor[2] and the Noise Electron Density depends on the CCD imager only.

This means that, in the case of only thermal noise, *"any noise minimum remains a minimum no matter what signal processor one uses".*
In the case that 1/f noise is also present one can show (see Chapter 4, section 4.3.4) that equation (2.31) is still valid except that the Noise Electron Density must now be given at a frequency near the clock frequency with which the reset FET is switched. The reason is rather simple: *"A minimum condition for suppressing 1/f noise and reset noise is that the transfer function of the signal processing has a gain equal to zero for f=0 Hz. The first maximum in the transfer function of the signal processing occurs near the reset FET clock frequency and there the noise will reach its maximum value too".*
Equation (2.31) can be expressed as the sum of a white noise contribution and a 1/f noise contribution:

---

[2] *With a rather straightforward calculation one can show that for the correlated double sampler the factors M and $B_{m,eff}$ are:*

$$M = \frac{4B_n}{f_p} \quad and \quad B_{m,eff} = \int_0^{B_m} sinc\left(\frac{f}{f_p}\right)^2 df$$

where B_n is the noise bandwidth at the sampler, f_p is the clock frequency at the output of the signal processing and, $B_{m,eff}$ is the effective bandwidth at which one measures the noise after signal processing.

$$N^2_{proc} = N^2_{proc,white} + N^2_{proc,1/f}$$

where the white noise term can be written as

$$N^2_{proc,white} = M \cdot NED_{white} \cdot B_{m,eff}$$

and the 1/f noise as

$$N^2_{proc,1/f} = M \cdot NED_{white} \cdot B_{m,eff} \cdot \frac{F_c}{F_{eq}}$$

The frequency F_{eq} has a value near the pixel clock frequency F_p.

2.5 Noise optimization

2.5.1 Equivalent Noise Electron Density for the case of thermal noise.

The model outlined in this chapter is valid for any type of capacitive detection node. The number of noise electrons after signal processing is only determined by the thermal noise when the crossover frequency between the 1/f and thermal noise of the on-chip amplifier is far below the reset FET clock frequency (see Chapter 4). This is the case with the measurements outlined in Section 2.6.
In Section 2.4 a general expression for the Noise Electron Density was derived (equation (2.28)). In the case of thermal noise only one arrives at a simple expression. Using the simple saturated MOS transistor model for the equivalent noise voltage [16] of the detection node MOS transistor M_1 and the current sink MOS transistor M_{c1} we have

$$e^2_{n1} = 4kT\frac{\alpha}{g_{m1}} \qquad (2.32)$$

and

$$e^2_{nc} = 4kT\frac{\alpha}{g_{mc}} \qquad (2.33)$$

The constant α is 2/3 for the ideal MOS transistor without backbias effect. With backbias effect [16,17,18] it becomes 2/3 $(1+g_b/g_m)$ where g_m is the

transconductance from gate to source and g_b is the transconductance from the well to source. At short channel lengths the electron temperature [19,20] increases and

$$\alpha = \frac{2}{3}\left(1+\frac{g_b}{g_m}\right)\frac{T_e}{T} \qquad (2.34)$$

where T_e is the electron temperature and T the lattice temperature.
Substituting both equation (2.32) for the equivalent noise voltage of follower M_1 and equation (2.33) for sink M_{c1} into equation (2.21), and using equation (2.28), one arrives at the expression for the Noise Electron Density

$$NED = \alpha\frac{4kT}{g_{m1}}\left[1+\frac{g_{mc}}{g_{m1}}\right]\left[\frac{C_{tot}}{q}\right]^2 \qquad (2.35)$$

with $C_{tot}=C_1+C_2$.
The first term between brackets represents the relative contribution of the current sink (M_{c1}) to the thermal noise.

2.5.2 Total capacitance C_{tot}.

Changing the dimensions of the detection node MOS transistor affects the total capacitance C_{tot}. Generally C_{tot} consists of the following components:

- the MOS transistor gate-channel capacitance (C_{gs}), which is proportional to the area ($W_1 \cdot L_1$),
- the overlap of the gate and that part of the silicon area not belonging to the MOS transistor ($C_{g,o}$), proportional to the length L_1,
- the overlap of gate and drain and source regions ($C_{gs,o}+C_{gd,o}$), proportional to the width W_1,
- and a constant parasitic part due to wiring, stray capacitances and floating diffusion capacitance (C_{fixed}).

$$\begin{aligned} C_{tot} &= C_{gs} + C_{g,o} + C_{gs,o}+C_{gd,o} + C_{fixed} \\ &= AW_1L_1 + BL_1 + CW_1 + D \end{aligned} \qquad (2.36)$$

A, B, C, D are proportionality constants which depend on the layout and technology. One can obtain these parameters via measurements on actual structures (see Section 2.6).

2.5.3 Minimum NED

Because a current sink is used to bias the source follower there are three parameters that control the noise behaviour of the amplifier. These are the bias current I of the source follower, and the channel width W_1 and length L_1 of the follower. In the simple saturated MOS transistor model [21] the transconductance can be written as

$$g_{m1} = \sqrt{2\mu C_{\square}\frac{W_1}{L_1}I} \qquad g_{mc} = \sqrt{2\mu C_{\square}\frac{W_c}{L_c}I} \tag{2.37}$$

where $C_{\square}$ is the channel capacitance per unit square, and W_c and L_c the dimensions of M_{C1}

The use of the above long channel expressions is a compromise between keeping the model as simple as possible and being able to predict the experiments.

Substituting equations (2.36) and (2.37) into (2.35), the expression for the Noise Electron Density becomes

$$NED = \alpha\frac{4kT}{\sqrt{2\ \mu\ C_{\square}\ I}}\sqrt{\frac{L_1}{W_1}}\left[1+\sqrt{\frac{W_c}{L_c}\frac{L_1}{W_1}}\right]\left[\frac{AW_1L_1+BL_1+CW_1+D}{q}\right]^2 \tag{2.38}$$

To minimize the NED the easy solution is to use the shortest possible channel length and highest bias current. Given these conditions, the NED can be minimized for the channel width by finding where the first derivative of equation (2.38) with respect to W_1 is zero.

For normalization purposes define a typical channel width W_T as

$$W_T = \frac{BL_1 + D}{AL_1 + C} \tag{2.39}$$

Letting $w=W_1/W_T$, the optimum channel width is the solution of

$$0 = \sqrt{w}(3w-1) + 2\beta(w-1) \tag{2.40}$$

where the parameter ß accounts for the influence of the current sink.If M_{c1} has a channel width W_c and channel length L_c.

$$\beta = \sqrt{\frac{W_c}{L_c}\frac{L_1}{W_T}} \tag{2.41}$$

Figure 2.7 plots the solution of equation (2.40) for the optimal channel width as a function of the current sink parameter ß.
Two special cases can be considered: ß=0 and ß=∞. In the case of ß=0 the current source is a very high ohmic sink and does not contribute to the Noise Electron Density. The optimum channel width is $W_1=W_T/3$. For ß=∞ the Noise Electron Density is determined only by the current source and the optimum channel width is $W_1=W_T$.
One can show by inspection of equation (2.40) that the optimum channel width will always be between $W_T/3$ and W_T.
In practice small values for β (<1) should be used; in this case the noise is mainly determined by the detection node MOS transistor.

For a large signal-to-noise ratio the NED must be made as small as possible by taking the following actions:

1) make the parasitic capacitances C_{fixed} in the detection node MOS transistor as small as possible;
2) make the length L_1 of the MOS transistor channel as small as practically possible;
3) make the bias current I as large as practically possible and g_{c1}/g_{m1} as small as possible by setting the gate-to-source bias voltage of the current sink as high as possible.
4) determine the scaling rule constants A,B,C and D for C_{tot};
5) determine the current sink parameter; and

6) make the channel width W_1 of the MOS transistor equal to the optimum value W_{opt} as read from Figure 2.7.

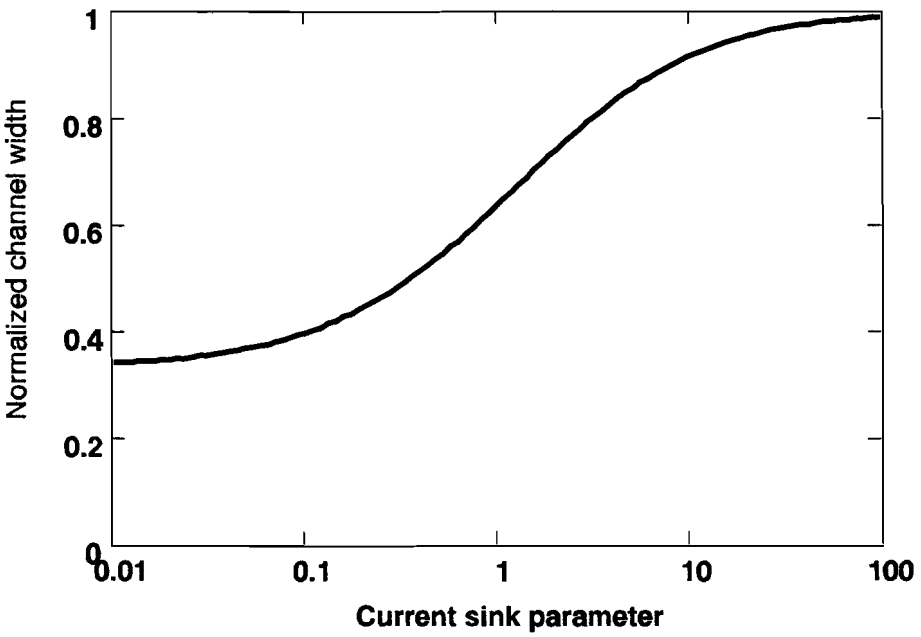

Figure 2.7: The optimum channel width W_1 of the detection node MOS transistor (normalized to the typical width W_T) as a function of the current sink parameter $\beta=\sqrt{[(W_c \cdot L_1)/(L_c \cdot W_T)]}$.

Since the bias voltage of the on-chip amplifier is somewhere between 15 V and 25 V hot electron effects and channel shortening (among other things) affect the practical length of M_1. The gain A_{10} also decreases at short channel lengths, and this means the contribution of other stages to the noise may not be neglected any more.

In the case that the parasitic capacitances, such as under-diffusion and overlap, are negligible a simple interpretation of the optimum is possible. The optimum value of the gate-to-source capacitance of the detection node transistor will always be between

$$\frac{1}{3}C_{fixed} \leq C_{gs} \leq C_{fixed} \qquad (2.42)$$

The left hand side applies when the noise contribution of the current source is negligible (see also [22]). The right hand side is valid when the noise of the current source dominates.
In a well designed on-chip amplifier the noise contribution of the current source will be small and the optimum gate capacitance is therefore about half the value of the fixed capacitance. Depending on the layout the value for the fixed capacitance is in the range of 10 fF-30 fF.

Sensitivity of the optimum with respect to variation of the parameters W,L and I.
Figure 2.8 plots the scaling in the NED (equation (2.38)) relative to the optimal value as the width of the detection node transistor changes from the optimal width W_{opt}. This scaling is only a function of W_1/W_{opt} and β. Note that when the actual width W_1 is chosen to be between $W_{opt}/2$ and $2 \cdot W_{opt}$ the noise performance deteriorates by only 0.5 dB.

Thermal noise decreases with increasing bias current I. One can achieve this by externally increasing the gate-to-source voltage of the current source M_{c1}. Another possibility is to increase W_c/L_c of M_{c1} and to connect the gate to the source (depletion MOS transistor, see Chapter 3). Then an increase in I results in a decrease of noise, but this effect is counteracted by the increased thermal noise contribution of the current sink.

Finally the thermal noise decreases with decreasing channel length L_1 as long as the hot electron region is not reached and the channel length shortening is not too large.

2.6 Experimental results.

A number of two-stage on-chip amplifiers (see Figure 2.1) with a floating diffusion region and a CCD delay line have been placed on a test chip to measure the effect of different values of W/L for the detection node MOS transistor M_1. The gate of the current sink M_{c1} connected separately to a bonding pad to control the bias current I in both transistors. It also serves as an injection point for test signals to measure both the bandwidth in the reset FET on- and off-states and the ratio Θ_n.

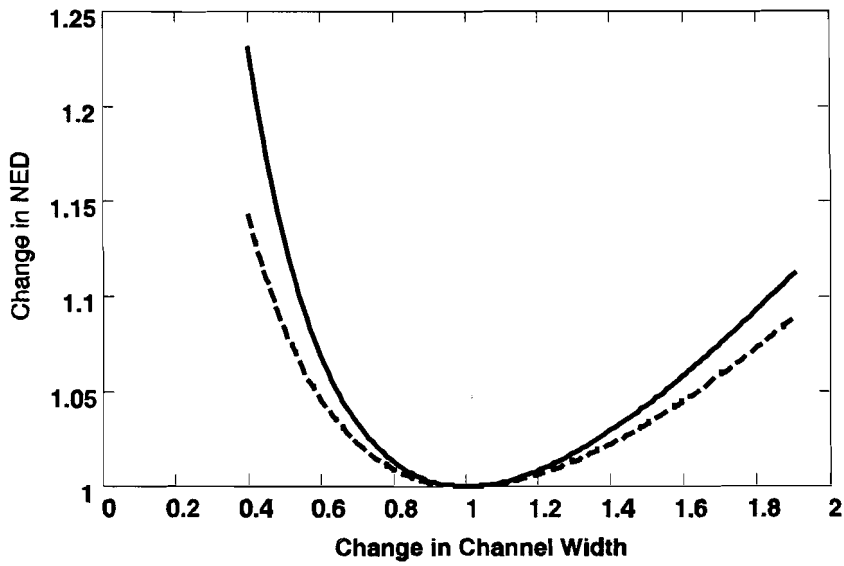

Figure 2.8: *The predicted relative change in Noise Electron Density as the channel width W, of the detection node transistor deviates from the optimum value. The horizontal axis is* W_1/W_{opt}. *The dotted line is for* $\beta=0$ *and the solid line for* $\beta=10$.

2.6.1 Total capacitance of the detection node.

The total capacitance is given by equation (2.7) $C_{tot}=\Theta_n \cdot C_{det}$. To obtain the total capacitance C_{tot} the following measurements have been performed:

- the sensitivity[3] [V/e] (equation (2.10)) and the gain from floating diffusion region to the output was measured and from this the detection node capacitance C_{det} was calculated; and
- the ratio $\Theta_n=C_{tot}/C_{det}$ was measured in two steps using the gate of the current sink M_{c1} as an injection point, taking the ratio Θ_n=Gain(off)/Gain(on) of the gain from the gate to the output in the reset

[3] *The measurement of the sensitivity S is done by injecting charge in the CCD delay line which is clocked at a speed* f_p. *One measures the current* I_{RD} *through the reset drain terminal* (V_{RD}) *and at the same time the change in output voltage* (dU_o) *of the on-chip amplifier. Then* $S=q \cdot f_p \cdot dU_o / I_{RD}$.

FET off-state and in the on-state (see Section 2.3).

Figure 2.9 gives the detection node capacitance C_{det} as a function of channel width W_1 using the channel length L_1 as a parameter.
The capacitance is slightly smaller at longer channel lengths. This is caused by the higher gain A_{10} for longer channels. The higher gain reduces the effect of the gate-source capacitance (equation (2.6)).

The measured values of Θ_n range between 2.5 and 4.3, with the smaller values for shorter channel lengths. These are rather high values, since this means a reduction in bandwidth by the same amount during charge dumping (equations (2.14) and (2.15)).

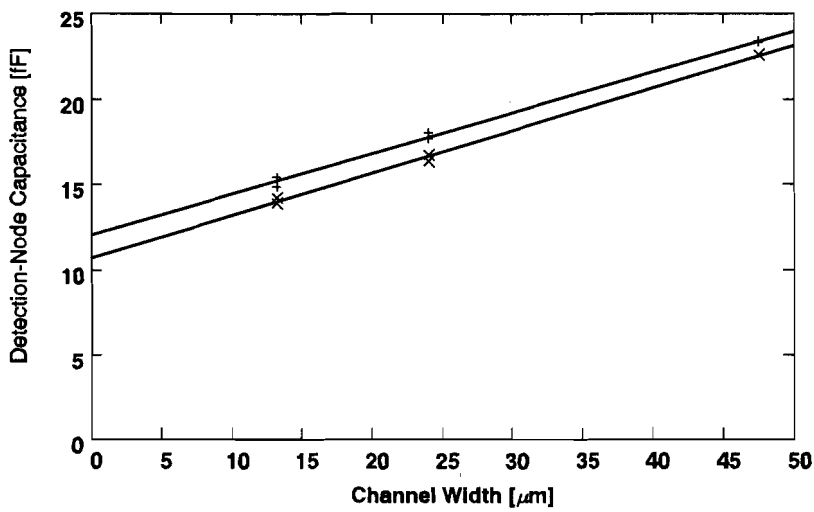

Figure 2.9: *The measured detection node capacitance C_{det} as a function of channel width W_1 with the channel length L_1 ((x): 8.7μm and (+): 3.2μm) as a parameter. The solid lines are least square fits.*

The total capacitance C_{tot} as a function of the same parameters is shown in Figure 2.10. Following equation (2.36) we have made a straight line fit to the experimental data in Figure 2.10. This fit yields:

$$C_{tot} = 0.12\,W_1 L_1 + 0.58 L_1 + 0.27\,W_1 + 29 \qquad [fF] \qquad (2.43)$$

where the channel length L_1 and channel width W_1 are given in μm.

- The value A=(0.12±0.01) fF/μm^2 is the capacitance of the MOS transistor channel per unit area. The buried channel is about 0.4 μm ($\varepsilon_{r,si}$=11.9) below the SiO_2 interface and, with an equivalent oxide thickness of 0.1μm ($\varepsilon_{r,ox}$=3.9), one would expect a value of 0.10 fF/μm^2.
- B=(0.58±0.05) fF/μm is mainly caused by the overlap between the gate and the guard ring surrounding the MOS transistor needed for electric insulation.
- The value for the overlap capacitance for drain and source regions per unit gate width is (0.135±0.01) fF/μm. This corresponds to about 0.39 μm under-diffusion.
- Finally, the fixed capacitance has a value of (29±3) fF.
  The high value of the fixed capacitance limits the noise performance considerably.

The scaling of the capacitance can be measured quite well with the above procedure.

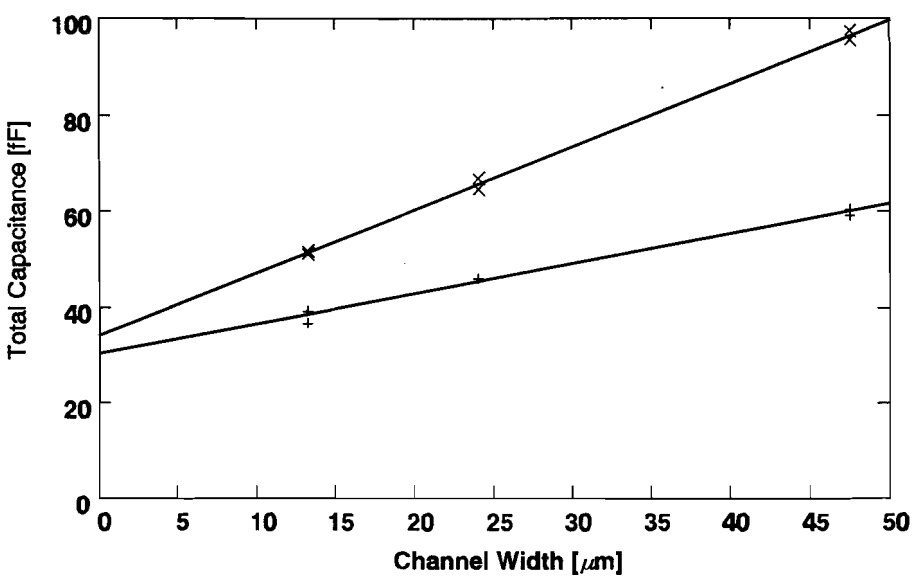

Figure 2.10: *The measured total capacitance of the detection node C_{tot} as a function of channel width W_1 and with the channel length L_1 ((x): 8.7μm and (+): 3.2μm) as a parameter. The solid lines are least square fits.*

The above data formed the input to the improvement in noise performance, as reported in Section 2.7.1.

2.6.2 The 3dB bandwidth and Θ_n.

In a CCD imager the bandwidth in the reset FET on-state can be easily measured by injecting a test signal at the reset drain. In the off-state one can not use this terminal. Using the gate of the current source as a test signal injection point allows one to measure the bandwidth in both the reset FET on- and off-state (see Section 2.3, equations (2.26) and (2.27)).

The decrease in bandwidth as predicted by equation (2.14) and equation (2.15) will in practice be smaller than Θ_n due to the fact that the second stage also limits the bandwidth. The ratio Θ_n is therefore an upper limit for the decrease in bandwidth. A lower bound for the ratio $F_3(on)/F_3(off)$ is 1. In Figure 2.11 the ratio $F_3(on)/F_3(off)$ is plotted as a function of Θ_n. Clearly the ratio remains within the upper limit given by Θ_n and the lower bound of 1.

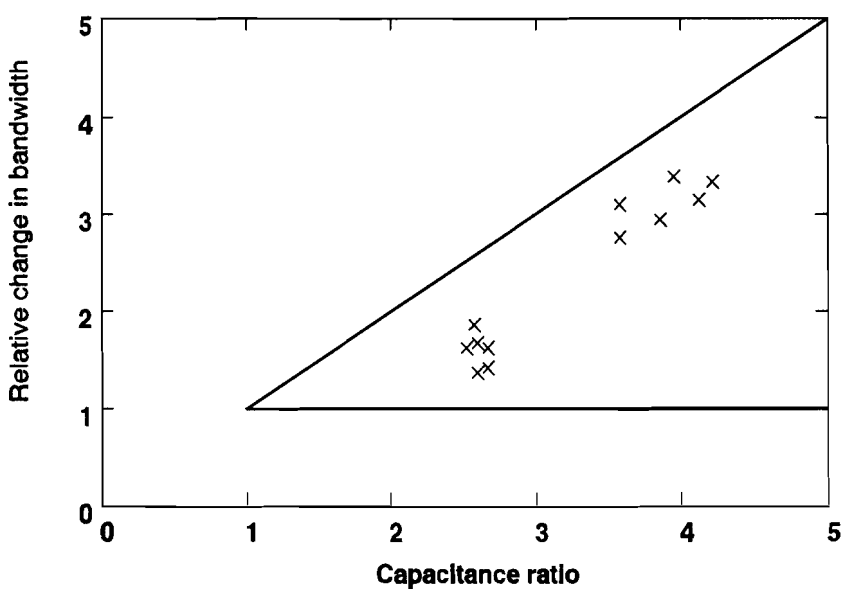

Figure 2.11: *The change in 3dB bandwidth in the reset FET on-state and the reset FET off-state $F_3(on)/F_3(off)$ as a function of the capacitance ratio $\Theta_n=C_{tot}/C_{der}$. The solid lines show the theoretical upper (Θ_n) and lower (1) limits. The measurements are represented by (x).*

2.6.3 Optimum value of the channel width

Figure 2.12 gives a typical experimental result for the noise in the reset FET on- and off-state. Notice the higher level in the reset fet off-state and the drop in bandwidth. The increase in noise is less than Θ_n because of the extra contribution of thermal noise in the channel in the on-state.

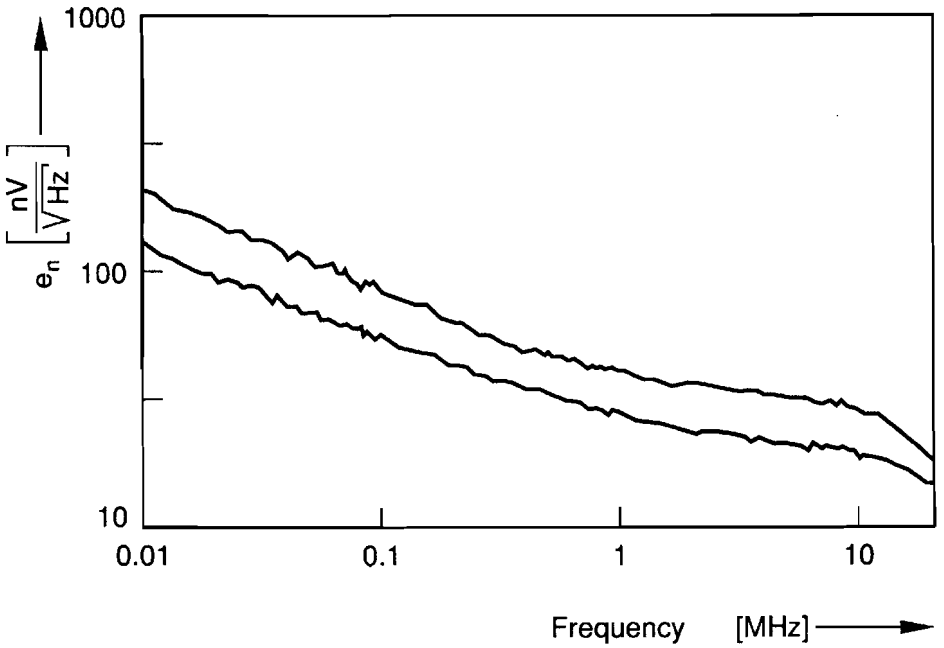

Figure 2.12: A noise measurement on a test module. The upper trace is the noise in the reset FET off-state and the lower trace in the on-state.

The typical width W_T of M_{c1} given in equation (2.39) and the normalized parameter ß from equation (2.41), have been calculated from the measured scaling results of the total capacitance C_{tot}.

At L_1 = 3.2 µm: W_T = 47 µm ß=0.17 w=0.43;

at L_1 = 8.7 µm: W_T = 26 µm ß=0.38 w=0.51.

The solution of equation (2.40) for the optimum width w is given in the last column. The corresponding optimal channel widths are W_1=20 µm and

W_1=13 μm, respectively.
A smaller optimum width when the channel length is larger seems odd. However, another interpretation of the optimum given in equation (2.42) states that the gate capacitance of the detection node MOS transistor should be constant. Therefore, increasing the channel length results in a smaller optimum channel width.
In Figure 2.13 the Noise Electron Density is given as a function of channel width W_1 with the length L_1 as a parameter. The weak dependence on the width, as predicted by equation (2.38), is clearly seen. Furthermore, a smaller optimum width for a longer channel length is also present.

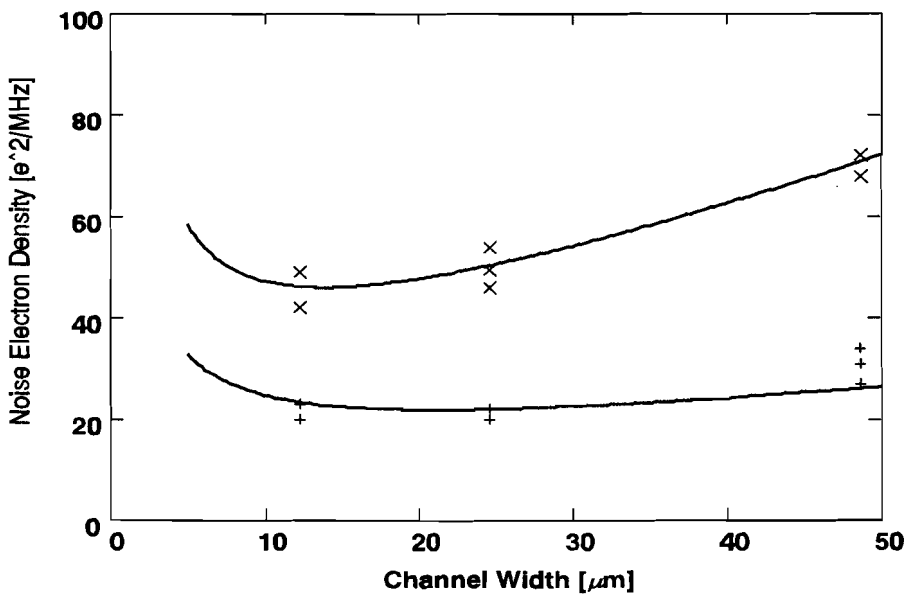

Figure 2.13: *The Noise Electron Density of the thermal noise as a function of the channel width W_1 with the channel length L_1 as a parameter ((x): 8.7μm and (+): 3.2μm). The bias current is 100 μA. The solid lines are calculated results according to equation (2.38).*

In Figure 2.14 the Noise Electron Density as a function of bias current I for one of the samples is given. As predicted by equation (2.38) the $1/\sqrt{I}$ dependence is obvious.

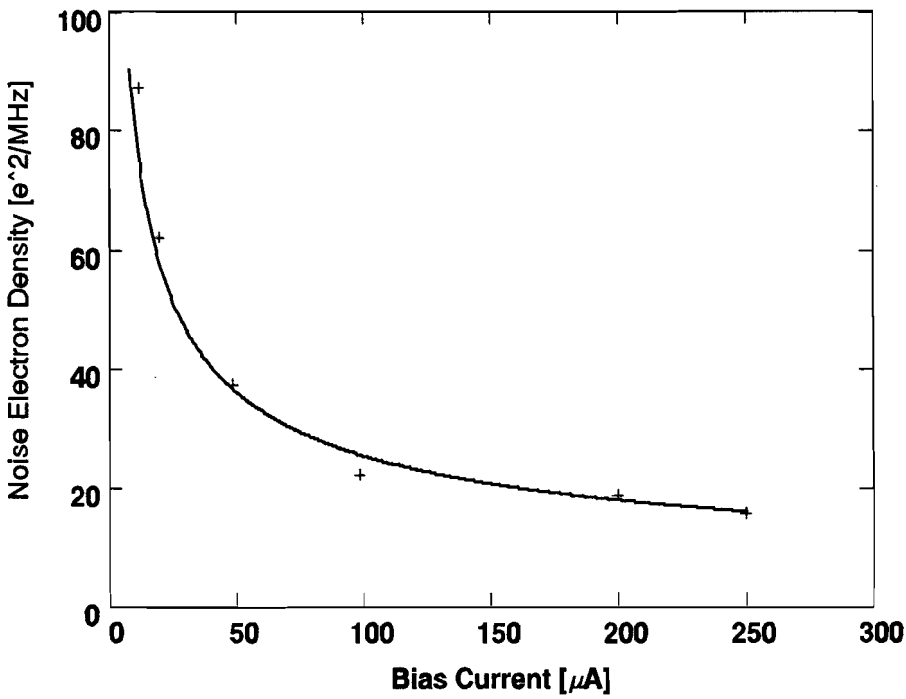

Figure 2.14: The Noise Electron Density of the thermal noise as a function of the bias current I of one of the test modules. The crosses represent measurements and the solid line is the predicted bias current dependence ($1/\sqrt{I}$).

After Correlated Double Sampling the noise expressed as an equivalent number of noise electrons was measured in a frequency band of 0.2 MHz - 5.0 MHz. The on-chip amplifier is used at a clock frequency of 5 MHz. The 1/f corner frequency is well below this frequency (F_c < 0.5 MHz) and limiting the calculation to thermal noise is valid. The rms noise voltage ([V]) after CDS is measured and divided by the sensitivity ([V/e]) to arrive at the equivalent number of noise electrons [e]. This value, as a function of channel width W_1 with the gate-to-source bias voltage of the current sink (V_{CS}) as a parameter, is given in Figure 2.15. (Changing the gate-to-source voltage (V_{CS}) changes the bias current I). The same soft minimum behaviour from Figure 2.13 is also seen here.

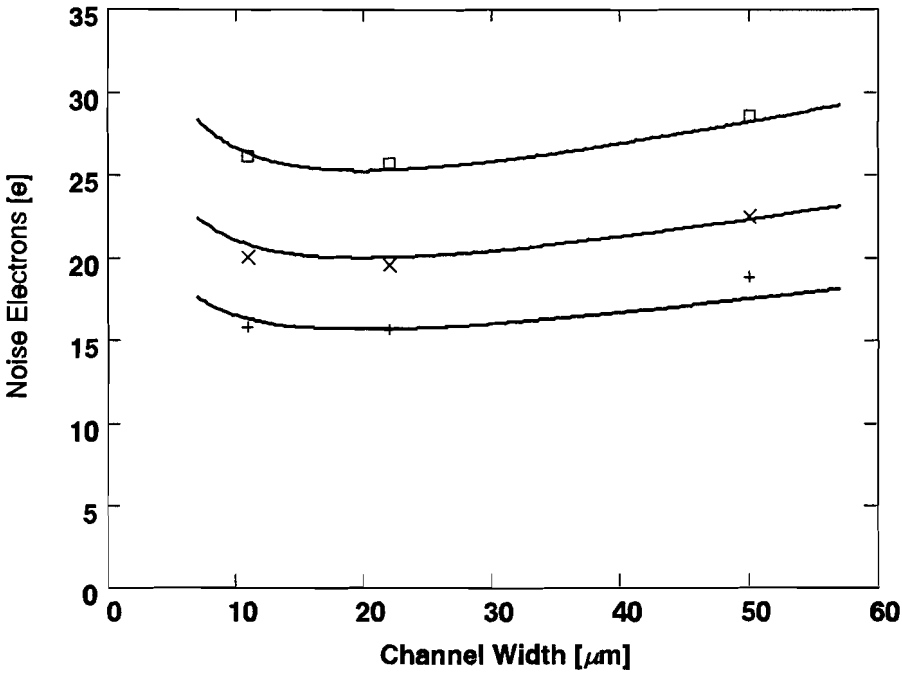

Figure 2.15: The noise equivalent number of electrons after Correlated Double Sampling expressed in relative units as a function of source follower channel width W_1 and with the gate-to-source voltage of the current sink as a parameter. The channel length L_1 is 3.2 μm. The markers ((□): V_{CS}=-3 V, (x): V_{CS}=0 V, (+): V_{CS}=5 V) show experimental data and the solid lines are predicted results according equations (2.31) and (2.38).

2.7 Application of the model.

2.7.1 Improvement of the FT5 on-chip amplifier.

One of the commercially available Frame Transfer Imagers from Philips Imaging Technology is the FT5 [15]. The experiments and capacitance scaling rules explained in Section 2.6 were done with the FT5 on-chip amplifier (Figure 2.16). Once C_1 and C_2 were known (see Appendix B) it was possible to establish the presence of parasitic capacitances that could be reduced

considerably, improving noise performance.

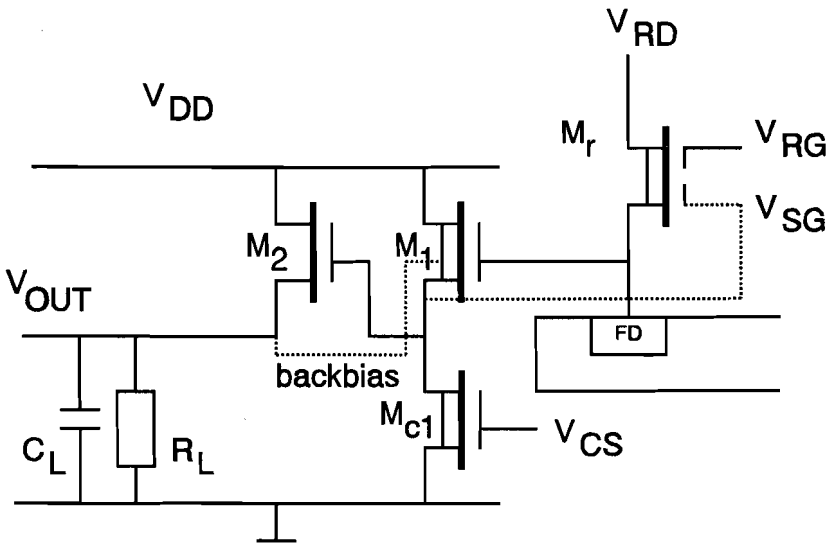

Figure 2.16: *Schematic view of the on-chip amplifier of the FT5 type CCD imager. The screening gate (V_{SG}) and the backbias connection are drawn as dotted lines.*

The on-chip amplifier has a number of parasitics:

- A screening gate between the source of the first follower M_1 and the reset FET M_r was introduced to reduce cross-talk from the pulsed reset gate (V_{RG}) to the detection node. It increases the total capacitance without a significant reduction of sensitivity (μV/e).
  -Removing this gate would result in more cross-talk and less noise.
- The buried-channel transistor M_1 has a rather large underdiffusion capacitance of 0.27 fF/μm, corresponding to 0.39 μm overlap per n+ source/drain region.
  -Using retarded drain and source regions would reduce the underdiffusion. Due to a blanket p^+ implant after the source and drain regions where formed, however, it was not possible to do this.
- The connection between the gate of follower M_1 and the floating diffusion region crosses a guard ring. The guard ring is used for isolation.

-Adding a floating poly gate underneath the connection where it crosses the guard ring halved the corresponding capacitance.

- The bias current of the current source is rather low because the transistor received an unintended threshold implant. The p-well is not depleted and this also gives rise to higher thermal noise due to the noisy (resistive!) p-well.

In total, by removing the screening gate, adding a floating poly layer underneath the gate of the first follower where it crosses the guard ring, and removing an additional threshold implant, an improvement in equivalent noise electrons from 20 e to 14 e has been obtained (3 dB).

2.7.2 The FT8 HDTV imager on-chip amplifier.

A second application of our theory is shown in the design of the on-chip amplifier of the FT8 HDTV imager [3]. Its clocking frequency is 36 MHz and the required bandwidth at least 120 MHz. As already discussed, the ratio Θ_n between the total capacitance and the detection node capacitance is of major importance in the design of high-bandwidth on-chip amplifiers. A high bandwidth demands a low Θ_n value and low noise requires a low C_{tot} design.

- The backbias of the detection node transistor M_1 is connected to ground to decrease the gain A_{10} and, in doing so, reducing Θ_n.
- The gate-source capacitance (C_2) and the gate-ground capacitance (C_1) of M_1 is reduced through the use of non-self-aligned n^+ diffusions for the source and drain regions. This helps to reduce the total capacitance.
- A third follower stage shown in Figure 2.17, is added and the various stages re-dimensioned.

With the optimal dimensions of the first follower, and using a non- self-aligned n^+ diffusion for the floating diffusion region, a low-noise, high-bandwidth on-chip amplifier is obtained.

After its realization the bandwidth of the on-chip amplifier was found to be 158 MHz and the equivalent Noise Electron Density NED=6.2 e^2/MHz. The above amplifier has improved the noise performance by 5 dB over the FT5HS sensors and 8 dB compared over the FT5-type.
The bandwidth has increased by a factor 10 (compare Figure 2.12 with Figure 2.18).

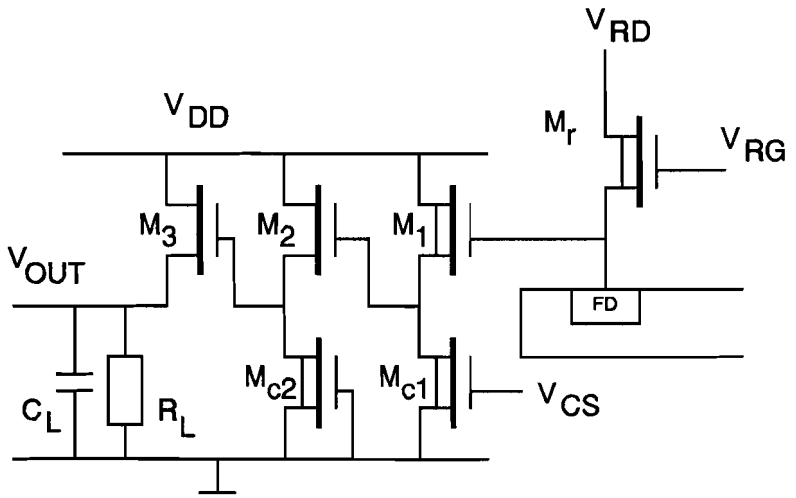

Figure 2.17: Shown is a schematic view of the on-chip amplifier of the FT8 HDTV imager.

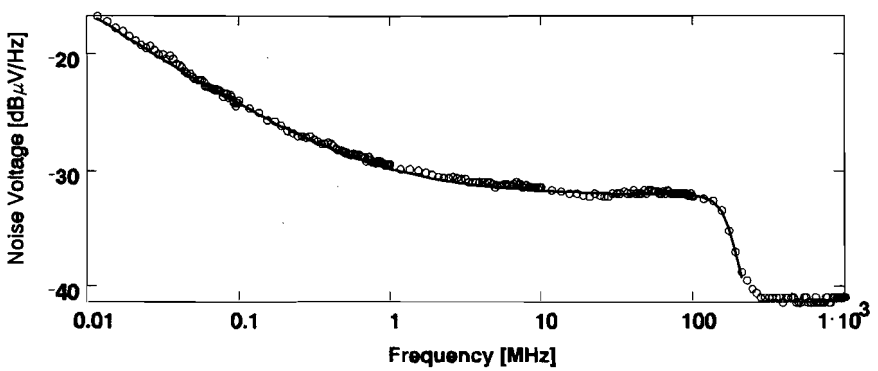

Figure 2.18: Noise spectral density of the FT8-HDTV on-chip amplifier with its low noise and high bandwidth. Dots are measurements and the solid line is a least square fit.

2.8 Conclusions

With the help of specially designed test modules it has been possible to obtain the scaling coefficients of the total capacitance C_{tot} of the detection node. Together with the detection node capacitance C_{det} and the DC gain of the first source follower stage A_{10}, the capacitance C_1 between gate and ground and the capacitance C_2 between gate and source of the detection node MOS transistor have been determined. Using this knowledge it was possible to locate points in the design that could be improved.

It is proven that near an optimum value the thermal noise does not vary much with the channel width of the source follower MOS transistor. In fact the noise depends more strongly on bias current and channel length.

With a simple MOS transistor model it was possible to calculate the optimum value of the channel width. These optimum values are found to be in good agreement with experimental results.

Furthermore it was shown that the bandwidth in the reset FET off-state is smaller than in the on-state. The fall time of the CCD imager output signal (for charge dumped on the detection node) was shown to be larger than the rise time. However the value for the on-chip amplifier bandwidth is too optimistic by a factor Θ_n when measured by injection at the reset drain. The same applies to the noise. The ratio $\Theta_n=C_{tot}/C_{det}$ is therefore of extreme importance as a (first) design parameter.

It was shown that the equivalent Noise Electron Density [e^2/Hz] is a well chosen noise quantity for charge detection nodes detectors, such as CCD imagers. It is the second design parameter for on-chip amplifiers. The Noise Electron Density depends on the product of the equivalent noise voltage at the gate and the total capacitance associated with the detection node, and this is valid for any type (topology) of capacitive charge detection node. The equivalent Noise Electron Density, and therefore the noise equivalent electrons, do not depend on the gain of the on-chip amplifier and are not directly related to the sensitivity. This implies that the best design strategy is to minimize the total capacitance even when the improvement in sensitivity is small.

The noise optimum for the on-chip amplifier does not depend on the signal processor that is used. The image sensor determines the Noise Electron Density and the signal processor the equivalent noise bandwidth that controls processing

performance.

In summary, to optimize the noise the channel length of the detection node MOS transistor should be as small as possible and the bias current should be as large as (practically) possible. The channel width should be close to its optimal value as established from the scaling rules. The current sink should have a small W/L ratio and its gate-to-source bias voltage must be as large as possible. Finally the layout should minimize as many fixed (non-scaling) parasitic capacitances as possible.

Appendix A: Transfer function

The node equations for the first stage of the on-chip amplifier read:

$$\begin{bmatrix} I_i \\ I_n \end{bmatrix} = \begin{bmatrix} j\omega(C_1+C_2) & -j\omega C_2 \\ -(j\omega C_2+g_{m1}) & \frac{1}{R_o}+g_{m1}+j\omega(C_o+C_2) \end{bmatrix} \begin{bmatrix} U_i \\ U_o \end{bmatrix} \qquad \textbf{(A1)}$$

The following abbreviations will be used:

the DC gain of the follower stage

$$A_{10} = \frac{R_o\, g_{m1}}{1 + R_o\, g_{m1}} \qquad \textbf{(A2)}$$

the detection node capacitance at low frequencies

$$C_{det} = C_1 + (1 - A_{10})\, C_2 \qquad \textbf{(A3)}$$

and the ratio between the total capacitance and detection node capacitance

$$\theta_n = \frac{C_{tot}}{C_{det}} \qquad \textbf{(A4)}$$

The charge-to-voltage conversion in the reset FET off-state is characterized by the following boundary conditions:

$$I_i = j\omega Q$$

$$I_n = 0 \qquad \textbf{(A5)}$$

The solution of equation (A1) with boundary conditions (A5) gives the charge-to-voltage conversion

$$\frac{U_o}{Q} = \frac{A_{10}}{C_{det}} \frac{1 + j \frac{\omega C_2}{g_{m1}}}{1 + j \omega \frac{A_{10}}{g_{m1}} \theta_n \left(C_0 + \frac{C_1 C_2}{C_1 + C_2} \right)} \tag{A6}$$

which for low frequencies reduces to

$$\frac{U_o}{Q} = \frac{A_{10}}{C_{det}} \tag{A7}$$

In the reset FET on-state a transfer function can be defined between input voltage and output voltage. The boundary condition is characterized by:

$$U_i = U_{RD}$$
$$I_n = 0 \tag{A8}$$

and the solution is given by

$$\frac{U_o}{U_i} = A_{10} \frac{1 + j \frac{\omega C_2}{g_{m1}}}{1 + j \omega \frac{A_{10}}{g_{m1}} (C_0 + C_2)} \tag{A9}$$

which for low frequencies reduces to just the DC gain of the follower.

The above equations reduce to equations (2.3) and (2.12) used in Chapter 2 when the following approximations apply

$$\frac{\omega C_2}{g_{m1}} \ll 1 \tag{A10}$$

and

$$C_o \gg C_2 \tag{A11}$$

Appendix B: Procedure to determine C_1 and C_2

To determine where the capacitances are located one can differentiate between the capacitance of the detection node MOS transistor between gate and ground (C_1) and gate and source (C_2). They are defined in Figure 2.2 and can be determined by re-shuffling equations (2.6) and (2.7) and using $C_{tot}=C_1+C_2$:

$$C_1 = \frac{C_{det}}{A_{10}}\left[\theta_n(A_{10}-1)+1\right] \qquad \textbf{(B1)}$$

and

$$C_2 = \frac{C_{det}}{A_{10}}(\theta_n-1) \qquad \textbf{(B2)}$$

References

[1] J.Carnes and W.Kosonocky, *"Noise Sources in Charge-Coupled Devices"*. RCA Review, vol. 33, pp. 327-343, June 1972.

[2] D.Barbe, *"Imaging Devices Using the Charge-Coupled Concept"*. Proceedings of the IEEE, pp. 38-67, Januari 1975.

[3] A.Theuwissen, H.Peek, P.Centen, R.Boesten, J.Cox, P.Hartog, A.Koskhoorn, H.van Kuijk, B.O'Dwyer, J.Oppers, F.Vledder. *"A 2.2 Mpixel FT-CCD imager, according to the Eureka HDTV-standard"*. Technical Digest IEDM91, pp. 167-170, Washington DC, December 8-11, 1991.

[4] J.Hynecek, *"Design and Performance of a Low-Noise Charge Detection Amplifier for VPCCD Devices"*. IEEE Trans. Electron Devices, vol. ED-31, no. 12, pp. 1713-1719, December 1984.

[5] J.Hynecek, *"High-Resolution 8-mm CCD Image Sensor with Correlated Clamp Sample and Hold Charge Detection Circuit"*. IEEE Trans. Electron Devices, vol. ED-33, no. 6, pp. 850-862, June 1986.

[6] P.Levine, *"Low-Noise CCD Signal Recovery"*. IEEE Trans. Electron Devices, vol. ED-32, no. 8, pp. 1534-1537, Augustus 1985.

[7] M.Ohbo, I.Akiyama and T.Tanaka, *"A New Noise Suppression Method for High-Definition CCD Cameras"*. IEEE Trans. Consumer Electronics, vol. CE-35, no. 3, pp. 368-374, December 1989.

[8] Chapter 4, this thesis.

[9] E.Oda, K.Orihara, T.Kitagawa, K.Arai, T.Kamata, Y.Ishihara, *"A CCD Image Sensor with 768X490 Pixels"*. IEEE Trans. Electron Devices, vol. ED-32, no. 8, August 1985, pp 1457-1461.

[10] R.Brewer, *"A Low Noise CCD Output Amplifier"*, Technical Digest IEDM79, pp. 610-612, Washington DC, December 3-5, 1979.

[11] Y.Matsunaga, *"A High Sensitivity Output Amplifier For CCD Image Sensor"*, Technical Digest IEDM87, pp. 116-119, Washington DC, December 6-9, 1987.

[12] N.Mutoh, M.Morimoto, M.Nishimura, N.Teranishi and E.Oda, *"New Low Noise Output Amplifier for High Definition CCD Image Sensor"*, Technical Digest IEDM89, pp. 173-176, Washington DC, December 3-6, 1989.

[13] G.Hobson, R.Longstone and R.Tozer, *"Dual-gate charge sensing in charge-coupled devices"*. IEEE Trans. Electron Devices, vol. ED-2, no. 6, pp. 207-214, November 1978.

[14] E.Roks, P.Centen, J.Bosiers, W.Huinink. *"The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD image sensors"*. IEEE Trans. Electron Devices, vol. ED-43, No. 9, pp. 1583-1591, 1996.

[15] A.Theuwissen, J.Bakker, H.Cox, A.Kokshoorn, P.van Loon, B.O'Dwyer, J.Oppers, C.Weijtens. *"A 400k pixels 1/2" accordion CCD imager"*. Digest Technical Papers ISSCC88, pp 48-49, San Francisco, February 17-19, 1988.

[16] M.Das, *"Fet Noise Sources and their Effects on Amplifier Performance at Low Frequencies"*. IEEE Trans. Electron Devices, vol. ED-19, no. 3, pp. 338-348, March 1972.

[17] C.Sah, S.Wu and F.Hielscher, *"The Effects of Fixed Bulk Charge on the Thermal Noise in Metal-Oxide-Semiconductor Transistors"*, IEEE Trans. Electron Devices, vol. ED-13, no. 4, April 1966, pp 410-414.

[18] F.Klaassen and J.Prins, *"Thermal Noise of MOS Transistors"*, Philips Res. Reports 22, pp 505-514, 1967.

[19] S.Kim and A.v.d.Ziel, *"Hot Electron Noise Effects in Buried Channel MOSFETs"*, Solid-State Electronics Vol. 24 pp 425-428, 1981.

[20] F.Klaassen, *"On the Influence of Hot Carrier Effects on the Thermal Noise of Field-Effect Transistors"*, IEEE Trans. Electron Devices, vol. ED-17, no. 10, October 1970, pp 858-862.

[21] D.Treleaven and F.Trofimenkoff, *"MOS FET Equivalent Circuit at Pinch-Off"*, IEEE Proceedings Letters, September 1966, pp 1223-1224.

[22] Z.Chang and W.Sansen, *"Low-Noise Wide-Band Amplifiers in Bipolar and CMOS Technologies"*, Kluwer Academic Publishers 1991; ISBN 0-7923-9096-2, pp 163-169.

Chapter 3

SENSING TRANSISTORS
Surface or buried channel type[4]

3.1 Introduction

A new CCD imager technology for making very small pixels has been recently reported [1,2]. Using this technology for the on-chip amplifier poses two possible problems: the high resistance of the thin (50 nm) polysilicon membrane and of the contacts to the poly-Si membrane above junctions. For this reason new amplifiers that use only one or two layers of this membrane were tried.
Figure 3.1 shows a three stage amplifier with M_1, M_2, and M_3 in source follower configuration and M_{c1} and M_{c2} as current sinks. The reset FET M_r is connected to the detection node consisting of the gate of the first follower M_1 and a floating diffusion region (FD). The source of M_3 is the output of the on-chip amplifier and is loaded with an off-chip capacitance C_L and a resistor R_L for biasing purposes.
An important characteristic of the underlying technology is that the leakage current generated at the surface is very low.

---

[4] *Based on the publication: P. Centen, E. Roks, "Characterization of Surface- and Buried-Channel Detection Transistors for On-Chip Amplifiers", IEDM Technical Digest, pp 193-196, Dec. 1997.*

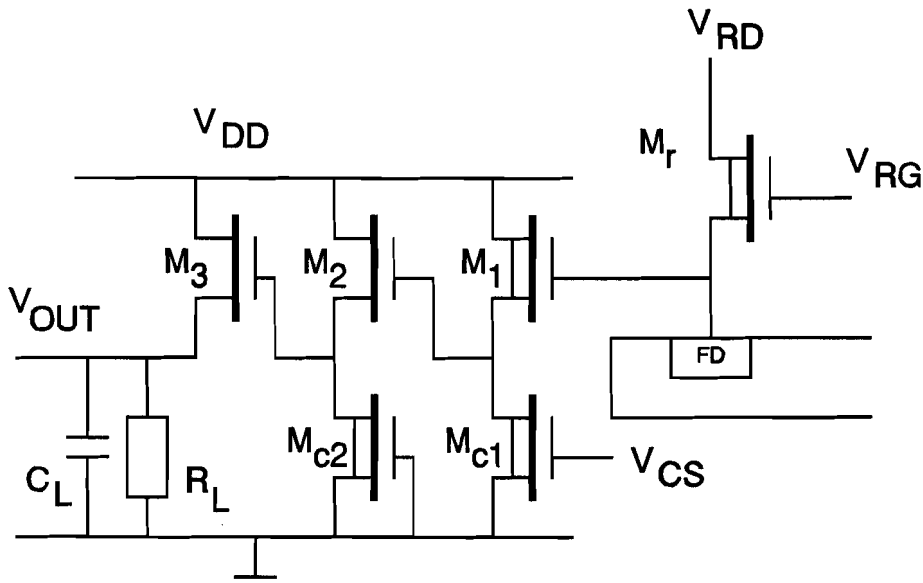

Figure 3.1: Schematic view of the floating diffusion amplifier in which transistor M_1 can be of the buried channel or surface channel type.

It also improves 1/f noise generation in the sensing transistor. Figure 3.2 gives typical noise measurements of an old on-chip amplifier with a surface channel MOS transistor connected to the detection node. The 1/f noise cross-over frequencies of those early types are as high as 10 MHz. These measurements were performed in the reset FET on- and off-state. Two different on-chip amplifiers were measured. The high cross-over frequency made it nearly impossible to obtain low noise numbers with surface channel MOS transistors in the detection node. The present state of the art is given in Figure 3.6.

In this chapter it is shown that in the new CCD imager technology the 1/f noise generation is almost the same for both surface channel and buried channel types. Therefore both transistors are candidates for future amplifiers.
The surface channel type has a higher transconductance and gate capacitance compared to the buried channel type.

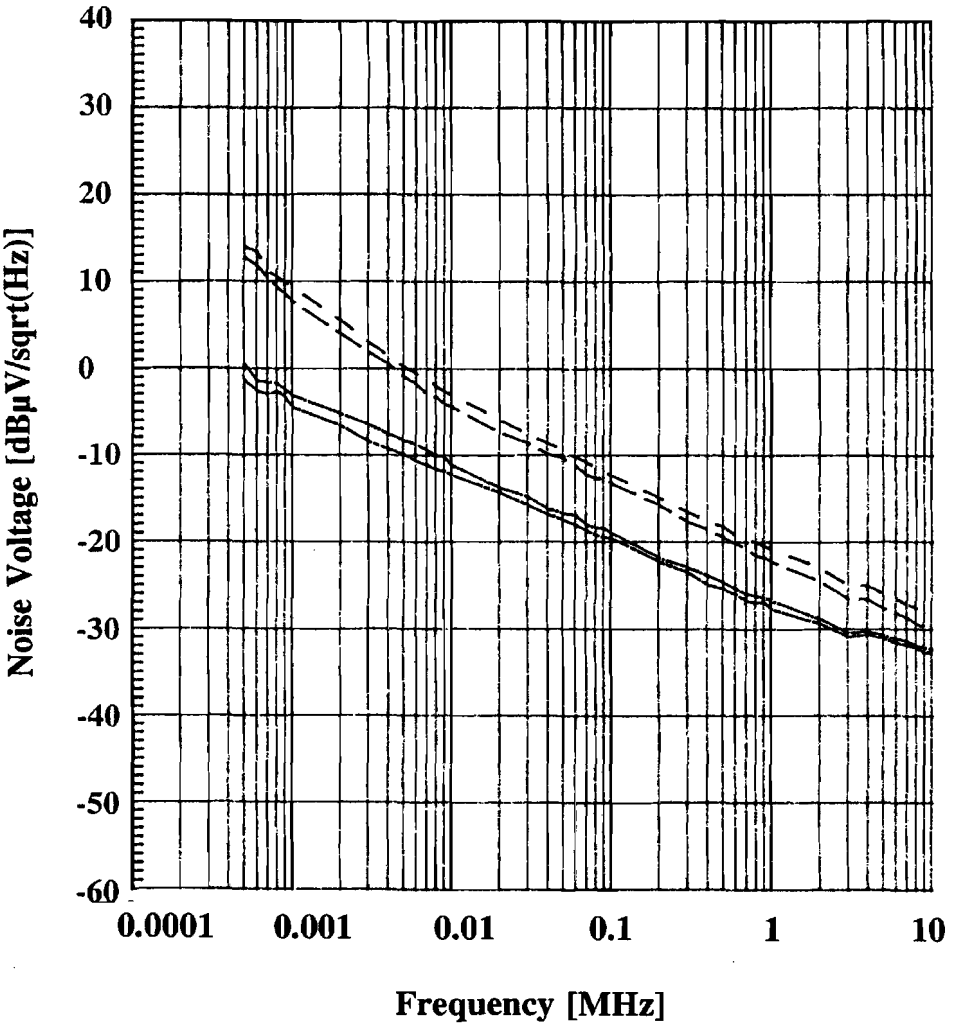

Figure 3.2: Noise voltage of two on-chip amplifiers with an older style MOS transistor as the sensing transistor. The upper trace is a noise measurement in the reset FET off-state and the lower trace for the reset FET on-state.

Experimentally one can give an answer to the question of which type will offer the best performance.
Figure 3.3 shows a cross section of an n-type surface MOS transistor. The

source and drain n^+ regions are self-aligned.

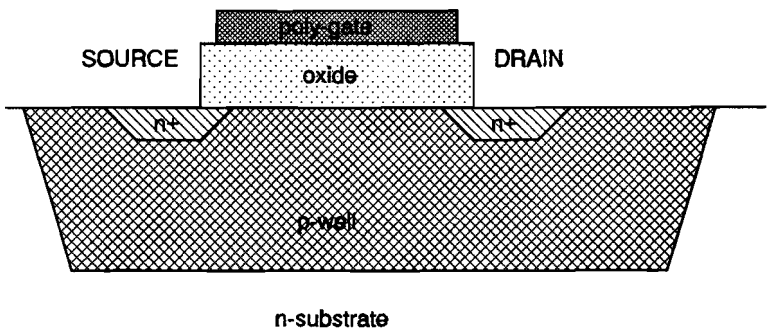

***Figure 3.3**: A cross sectional view of an n-type surface channel MOS transistor.*

Figure 3.4 presents an n-type buried channel transistor which also has self-aligned n^+ diffusion regions.

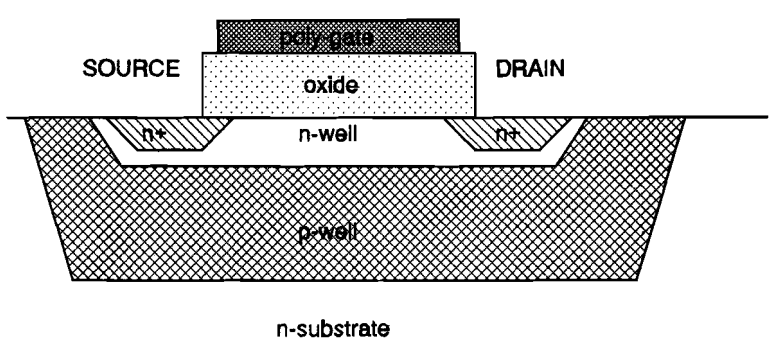

***Figure 3.4**: Cross sectional view of an n-type buried channel MOS transistor.*

In Figure 3.5 an n-type buried channel type with non-self-aligned n^+ diffusion regions is given. In this type the overlap capacitance is reduced.

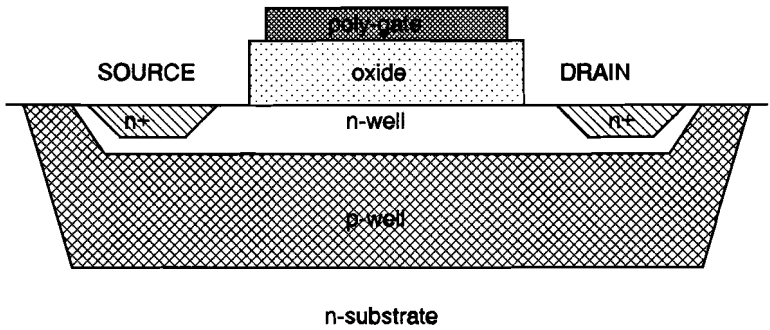

***Figure 3.5**: A cross section of an n-type buried channel MOS transistor with non-self-aligned drain and source regions.*

There are many applications in which high speed operation is needed, putting a high demand on the bandwidth of the on-chip amplifier. It will be shown that the choice between high bandwidth, low noise, and high conversion gain causes a conflict.

3.2 1/f noise

The imagers in which the above amplifiers will be used have pixel frequencies above 5 MHz. The effect of the 1/f noise on the signal-to-noise ratio is negligible when its cross-over frequency (F_C) with the thermal noise is well below the clock frequency (see Chapter 4, section 4.3.4). Figure 3.6 gives a typical noise spectral density for an on-chip amplifier in which the first MOS transistor has a surface or buried channel. It shows that, for equal W/L and biascurrent, both surface and buried channel transistors have a much reduced and almost equal 1/f noise performance. The cross-over frequencies are 142 kHz and 156 kHz, respectively.

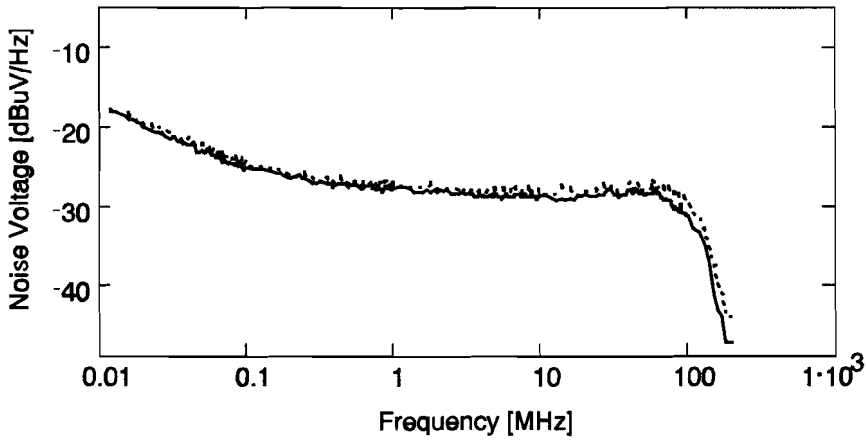

Figure 3.6: *Typical noise spectral density for an on-chip amplifier in which the sensing transistor is of the buried channel (solid line) or surface channel type (dotted line).*

A parameter of interest for 1/f noise is the Hooge factor α_H. Following the interpretation of Klaassen [3], who derived a relation between Hooge's and McWhorter's 1/f noise model, one arrives at the following equation for the squared noise voltage of a saturated MOS transistor

$$S_{vv}(f) = \frac{q\ \alpha_H\ \bar{V}_{gs}}{C_g\ 2}\ \frac{1}{f} = \frac{q\ \alpha_H}{C_g}\ \frac{I}{g_m}\ \frac{1}{f} \qquad (3.1)$$

With the above relation for a transistor in saturation, one can calculate the Hooge factor between the measured spectral density and some MOS transistor parameters. It is plotted in Figure 3.7 for both surface and buried channel transistors. For the surface channel the Hooge factor is $\alpha_H=2\cdot10^{-5}$, and for the buried channel $\alpha_H=4.5\cdot10^{-6}$.

In addition to the Hooge factor another parameter of interest for 1/f noise is the cross-over F_C frequency between 1/f noise and thermal noise. The cross-over frequency can be determined from the noise spectral density measurements.

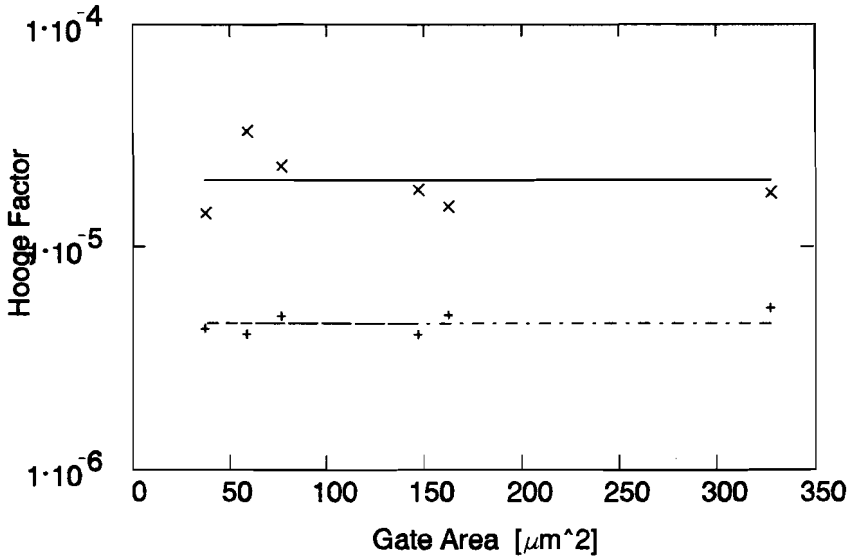

Figure 3.7: *Hooge's factor α_H for the 1/f noise generated in buried channel (+) or surface channel (x) detection node transistors.*

Figure 3.8 gives the cross-over frequency, F_C, as a function of the gate area (W·L) of the sensing transistor. It demonstrates that the bias current, the Hooge factor, and the dimensions of the detection node transistor are such that for clock frequencies above F_C (above 5 MHz) the contribution of 1/f noise to the signal-to-noise ratio after CDS is negligible. Therefore, to optimize the noise of these amplifiers one only has to focus on the thermal noise.

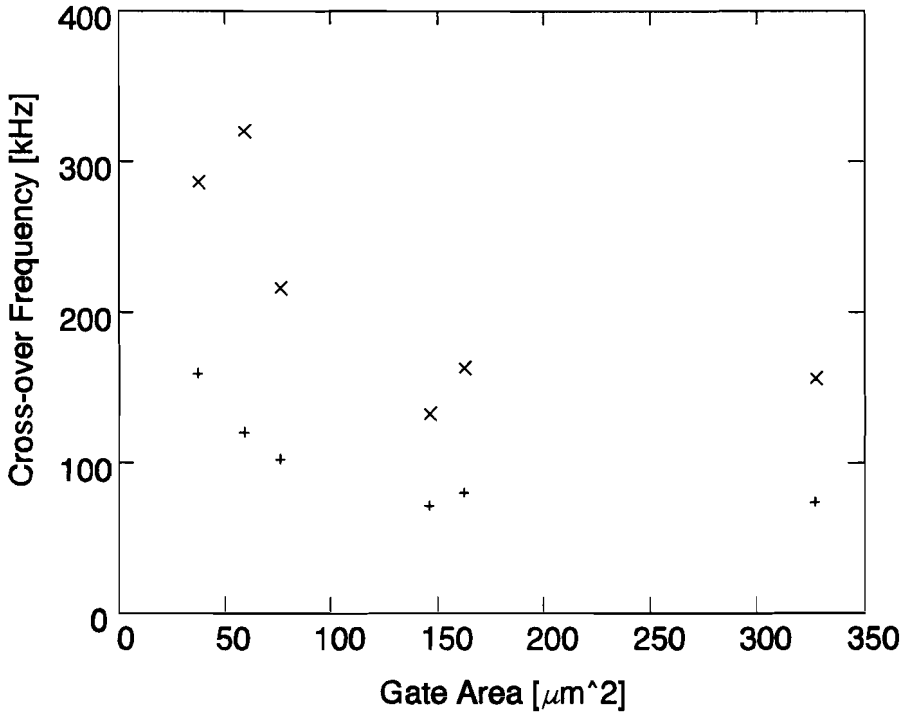

Figure 3.8: Cross-over frequency as a function of gate area of the sensing buried channel transistors (+) and surface channel transistors (x).

3.3 Thermal noise

The thermal noise of a MOS transistor is determined by its transconductance, the backbias effect [4,5], and shot noise caused by the hot-electron effect [6,7]. The noise ideality factor α [5,6,7], which is the product of the equivalent noise resistance R_n of a MOS transistor and its transconductance, is given by:

$$\alpha = R_n \cdot g_m = \frac{2}{3}\left(1 + \frac{g_b}{g_m}\right) + \frac{qI}{2kTg_m}\frac{\delta L}{L} \qquad (3.2)$$

where g_m is the transconductance, g_b the backbias related transconductance, I the

bias current of the first source follower stage, and δL a constant for the shot noise term. In the ideal case α is 2/3. For the surface channel type the backbias effect is negligible. Since the buried channel is located deeper below the surface a larger backbias effect follows.

Assuming a simple MOS transistor model, the transconductance is:

$$g_{m1} = \sqrt{2\ \mu_n\ C_\square\ \frac{W_1}{L_1}\ I} \tag{3.3}$$

Because the transconductance g_{m1} of the sensing transistor can be measured, as demonstrated in Appendix A, and the channel width and channel length are known, one can calculate the gain factor $\mu_n\ C_\square$ with equation (3.3). The Figures 3.9a and 3.9b. show the relationship, which is nearly a constant in the range of interest. This is important since it gives credibility to the approximations involved in the simple saturated MOS transistor model in the calculation of the transconductance. The gain factor for the buried channel transistor is $\mu_n.C_\square$=21 $\mu A/V^2$ and $\mu_n\ C_\square$=60 $\mu A/V^2$ for the surface channel transistor. The difference in gain factor between buried and surface channel seems rather large at first glance. However the surface channel is at the SiO_2 interface whereas the buried channel is further away. The capacitance per unit area ($C_\square$) for a surface channel is much higher than for a buried channel. This explains the difference in gain factor.

The Figures 3.10a and 3.10b give the observed noise ideality factor α for both types of MOS transistors as a function of current density. It shows clearly that even for moderate current densities the noise factor α deviates from the ideal value of α=2/3. This indicates that hot electron effects exist.

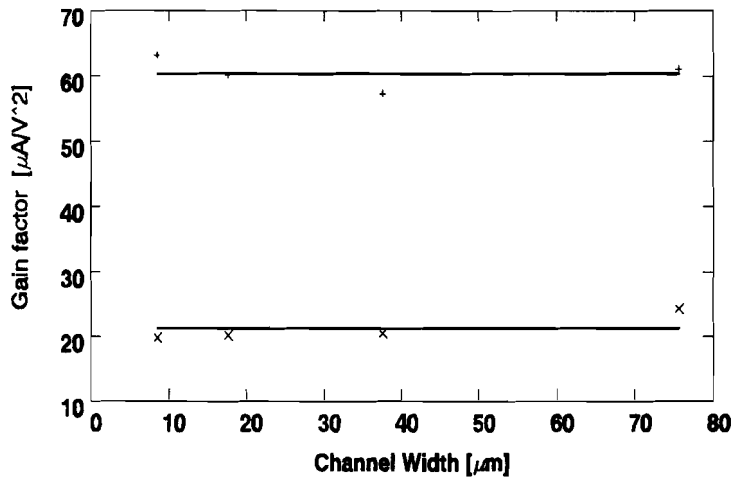

Figure 3.9a: *Gain factor $\mu_n C_\square$ of a buried channel (x) and surface channel (+) transistor as a function of channel width W_l. The channel length L_l and bias current I are fixed.*

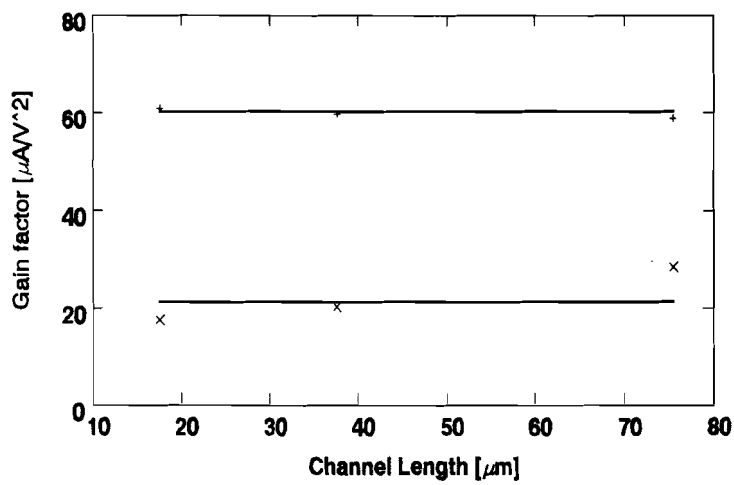

Figure 3.9b: *Gain factor $\mu_n C_\square$ of a buried channel (x) and surface channel (+) transistor as a function of channel length L_l. The channel width W_l and bias current I are fixed.*

The effect is less pronounced for the buried channel transistor due to the use of non-self-aligned diffusions for the source and drain regions. They act as a Lightly Doped Drain structure, reducing the lateral field at the drain. Figure 3.10a and 3.10b superimposes equation (3.2) (solid lines) over the measured data. The curves are least square fits and the factor δL is found to be δL=0.06 μm for buried channel and δL=0.39 μm for surface channel transistors.

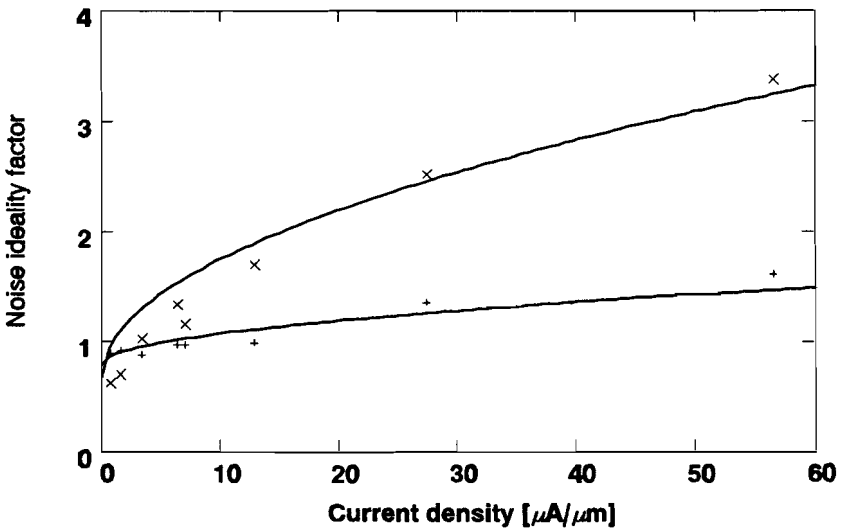

Figure 3.10a: *Noise ideality factor (α) as a function of current density (I/W) for buried channel type ((+): δL=0.06 μm) and surface channel type ((x): δL=0.39 μm). The channel length L is fixed.*

The backbias transconductance g_{bl} is determined from the DC gain of the first stage which equals $A_{10}=1/(1+g_{bl}/g_{ml})$.

3.4 Equivalent Noise Electron Density

In this section the experimentally obtained values of the detection node capacitance, the total capacitance, and the Noise Electron Density are given. One needs the sensitivity of the detection node (inversely proportional to the detection node capacitance) to calculate the Noise Electron Density from the measured noise voltage. Yet the noise model shows that the Noise Electron Density is only dependent on the total capacitance. Θ_n is also needed to convert between the two.

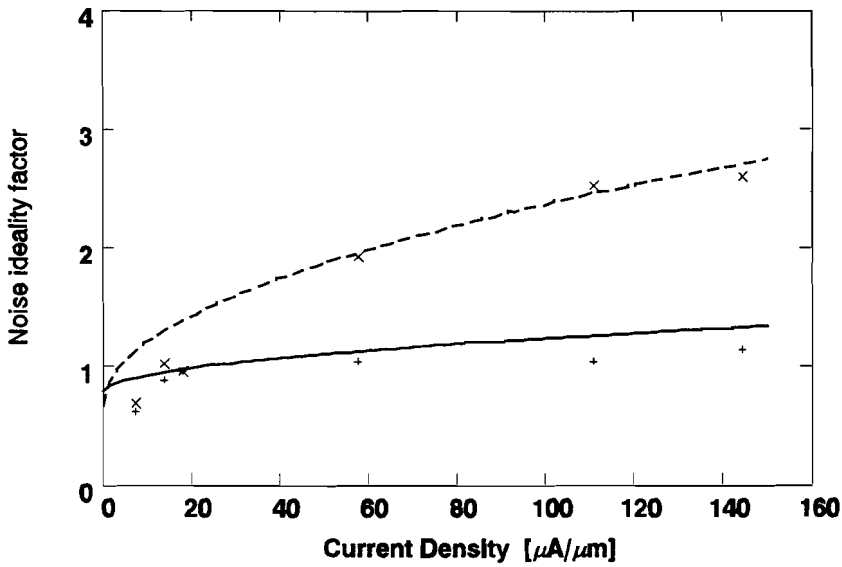

Figure 3.10b: Noise ideality factor (α) as a function of I/L for buried channel type (+) and surface channel transistors (x). The channel width W is fixed.

The total capacitance C_{tot} at the detection node (FD) is therefore determined in two steps. First, measure the sensitivity μV/e at the output node and the DC gain from the floating diffusion region to output. This gives the detection capacitance C_{det}, equation (2.10). The result is displayed in Figure 3.11. Next, find the ratio Θ_n ($=C_{tot}/C_{det}$) using the gate of the current source (M_{cl} in Figure 3.1) as an injection point and measuring the gain from this gate to the output. Figure 2.3 and equations (2.24) and (2.25) show that with only one measurement the ratio C_{tot}/C_{det} can be determined. This guarantees identical voltage settings for the reset FET (M_r) on- and off-state. The product of Θ_n and C_{det} yields the total capacitance C_{tot}, which is an important parameter for the noise performance (see Section 2.4).

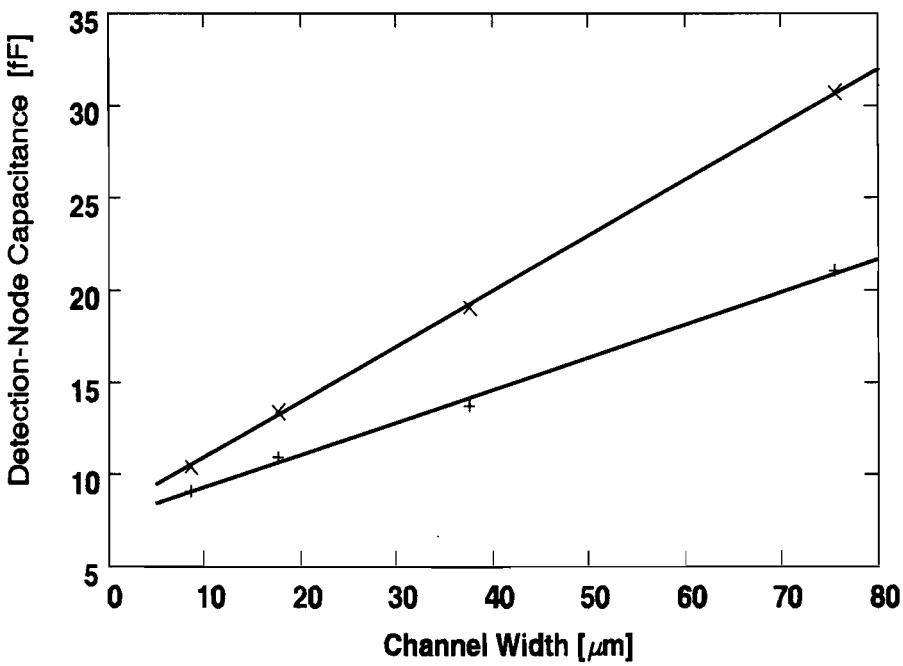

Figure 3.11: Detection node capacitance C_{det} for fixed channel length L_1 as a function of the channel width W_1 (Surface channel (x) or buried channel (+)).

In the Figures 3.12a and 3.12b C_{tot} is given as a function of W_1 and L_1 for both types of transistor channels. From the slope and intercept of these lines it is possible to determine how the capacitance is distributed.

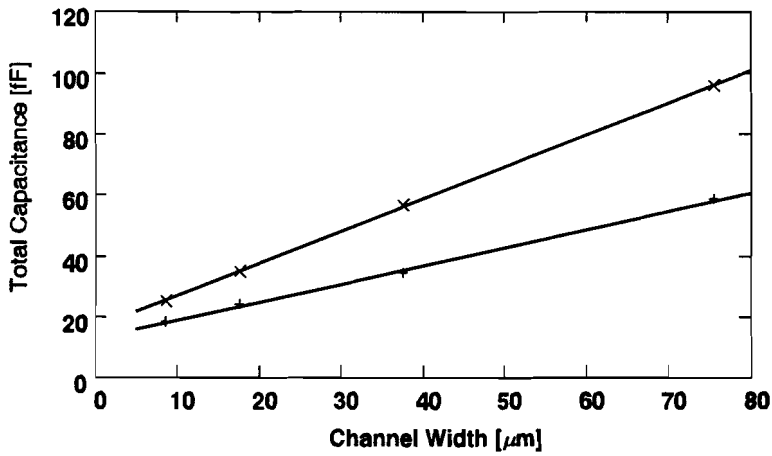

Figure 3.12a: *Total capacitance C_{tot} of the detection node transistor as a function of the channel width W_1 with fixed channel length L_1, for the surface channel (x) and buried channel (+) cases.*

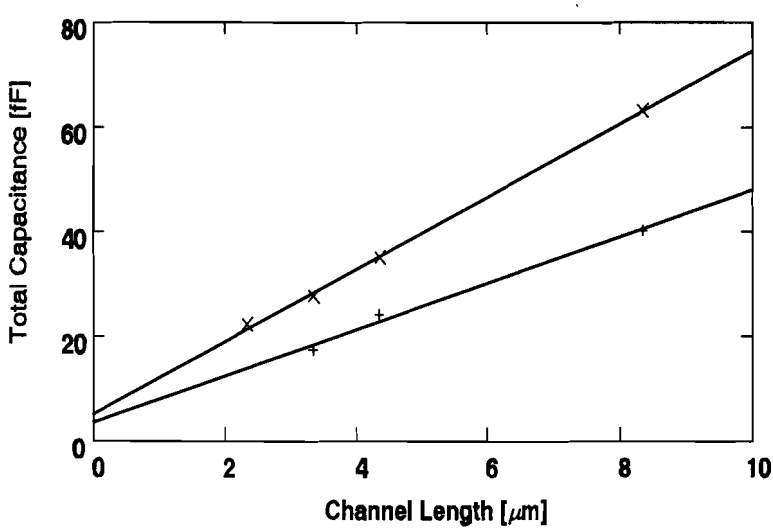

Figure 3.12b: *Total capacitance C_{tot} as a function of the channel length L_1, for fixed channel width W_1, for surface channel (x) and buried channel (+) transistors.*

The equivalent Noise Electron Density (NED), discussed in Section 2.4 and defined by equation (2.28), is given in Figure 3.13 as a function of the channel width W_1 for both types of transistor.
In these measurements V_{CS} is set such that a bias current I=60 μA flows through the first stage of the amplifier. One can conclude that the noise performance of both types of sensing transistor is almost the same. The higher C_{tot} of the surface transistor is compensated by the higher transconductance. From the NED model, which includes α and C_{tot} (see Section 2.4), the optimal width for the surface transistor is found to be W_1=9 μm and for the buried channel W_1=13 μm.

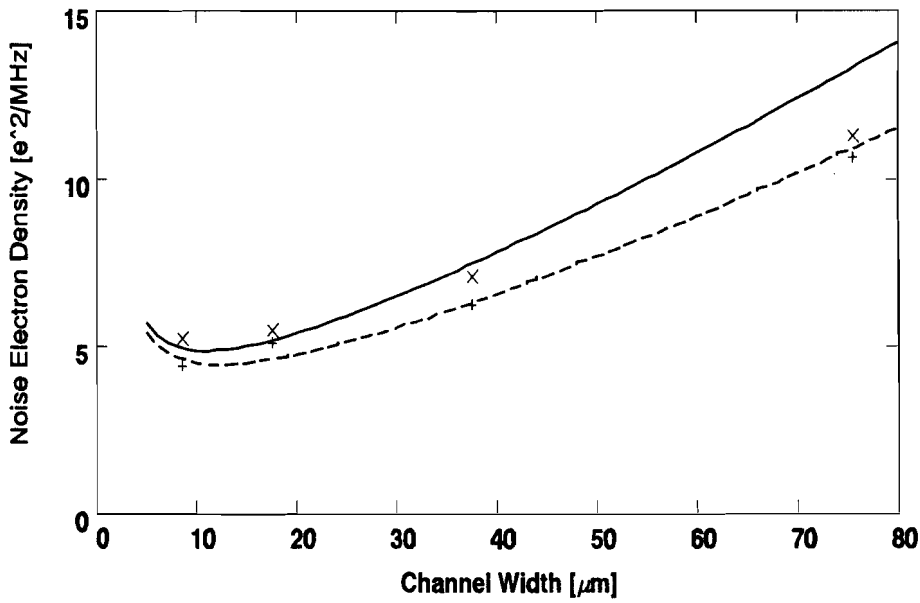

Figure 3.13: Noise Electron Density (NED) versus the channel width W_1 for surface channel (x) and buried channel (+). The channel length L_1 is fixed. The filled lines are from equation (2.28).

3.5 Bandwidth

The bandwidth in the reset FET off-state determines the signal shape ([8] and Section 2.2) and the amount of reset noise suppression that is possible. In Section 2.2.3 an equation was derived for the noise spectral density in the reset FET on- and off-state. It shows that the thermal noise (white spectrum) of the

first source follower stage can be used as a test signal source to measure the transfer function from detection node to on-chip amplifier output.
With the use of least squares fitting of equation (3.4) to the measured spectral density one can determine the 3 dB bandwidth F_{3dB}, the thermal noise as an equivalent noise resistor R_{eq} value, and the 1/f cross-over frequency F_C.

$$S_{vv}(f) = 4kTR_{eq} \frac{\left[1 + \left(\frac{F_c}{f}\right)\right]}{1 + \left(\frac{f}{F_{3dB}}\right)^{2n}} \tag{3.4}$$

This method has been extensively used for determining on-chip amplifier parameters in the reset FET off-state. It is based on the practical assumption that the noise of the first source follower stage is dominant. Beyond the 1/f noise cross-over frequency this noise source is white and is therefore usable as an internal test signal source for bandwidth measurements. Theoretically the 3 dB bandwidth (F_{3dB}) follows from equations (2.5) and (2.15) with

$$C_o = C_{load} + \frac{C_1 C_2}{C_1 + C_2} + a W_1 \tag{3.5}$$

and reads as:

$$F_{3dB} \approx \frac{g_{m1}}{2 \pi \theta_n A_{10} \left(C_{load} + \frac{C_1 C_2}{C_1 + C_2} + a W_1 \right)} \tag{3.6}$$

g_{m1} is the transconductance of the first source follower, Θ_n the ratio C_{tot}/C_{det}, A_{10} the DC gain of the first source follower stage, C_{load} the load capacitance at the source of the first source follower, C_1 the capacitance between the gate and the source of M_1, C_2 the gate-to-ground area capacitance, and finally the source region capacitance.
The bandwidth was measured using a least squares fit between the measured spectral density and equation (3.4) and is given in Figure 3.14 as a function of channel width. From equation (3.6) all parameters are known except for the load capacitance C_{load} and the scaling constant a. These are determined by a least squares fit of equation (3.6) to the data from Figure 3.14. The fixed load capacitance was determined to be C_{load}=77 fF and the scaling capacitance of the

source region a=0.68 fF/μm.
In the region of interest the bandwidth increases for larger channel width, just as the noise spectral density does. The buried channel transistor shows a lower bandwidth than the surface channel type owing to its lower transconductance.

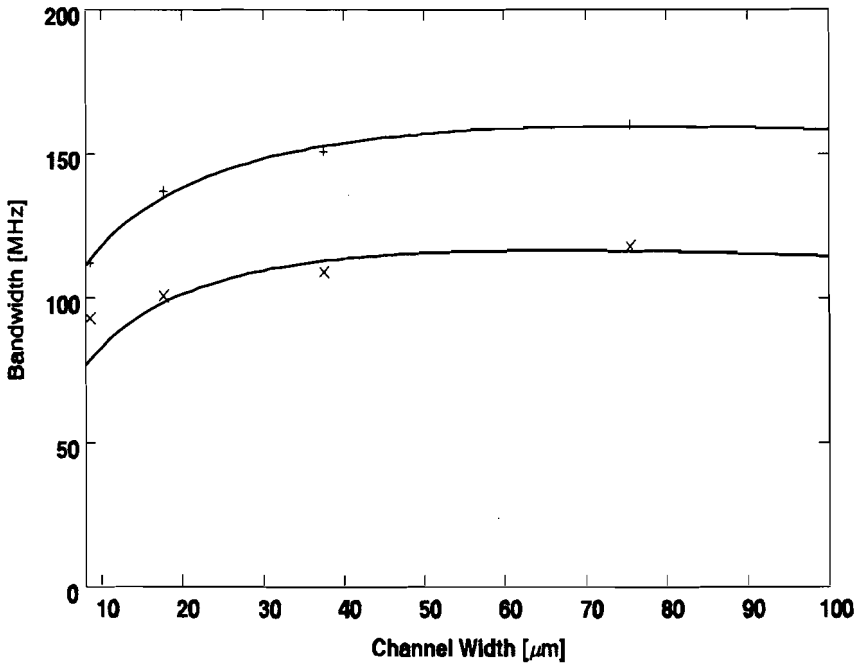

Figure 3.14: Bandwidth F_{3dB} of the on-chip amplifier as a function of channel width W_l for surface channel detection node transistors (+) and buried channel detection node transistors (x). The solid lines are least squares fits with equation (3.6).

3.6 Conclusions

Because of its lower detection capacitance, the buried channel sensing transistor has a higher sensitivity than the surface channel transistor. Its transconductance is lower, however, which compensates the higher total capacitance. As a result the noise performance is nearly the same for both transistors. Although both types have a very high bandwidth it has been shown that the choice between high bandwidth and low noise causes a conflict.

Appendix A: Determination of the transconductances

The measurement of the transconductance of M_1, is done in 3 steps:

- first, the transconductance of the current source M_{c1} is measured by applying a test signal to the current source gate and measuring the change in bias current, giving by definition

$$g_{c1} = \frac{dI}{dV_{CS}} \tag{A1}$$

- next, the DC gain A_{CS} from the current source gate to the output is measured with the reset FET on

$$A_{CS} = \frac{dV_{out}}{dV_{CS}} \tag{A2}$$

- finally, the DC gain (A_{RD}) from the reset drain to the output is measured

$$A_{RD} = \frac{dV_{out}}{dV_{RD}} \tag{A3}$$

With the above three parameters the transconductance (g_{m1}) of the first source follower is given by

$$g_{m1} = g_{c1} \frac{A_{RD}}{A_{CS}} \tag{A4}$$

References

[1] H.Peek, D.Verbugt, M.Beenhakkers, W.Huinink, A.Kleimann, *"An FT-CCD imager with true 2.4*2.4 μm^2 Pixels in Double Membrane Poly-Si Technology"*, Technical Digest IEDM96, pp. 907-910, San Francisco, December 8-11, 1996

[2] H.Peek, D.Verbugt, J.Maas, M.Beenakkers, *"Technology and Performance of VGA FT-imagers with Double and Single Layer Membrane Poly-Si Gates"*, IEEE Workshop on CCDs and Advanced Image Sensors, June 5-7, 1997 Bruges Belgium.

[3] F.Klaassen, *"Characterization of Low 1/f Noise in MOS transistors"*. IEEE Trans. Electron Devices, vol. ED-18, no. 10, pp. 887-891, October 1971.

[4] C.Sah, S. Wu and F. Hielscher, *"The Effects of Fixed Bulk Charge on the Thermal Noise in Metal-Oxide-Semiconductor Transistors"*, IEEE Trans. Electron Devices, vol. ED-13, no. 4, April 1966, pp 410-414.

[5] J.Hynecek, *"Design and Performance of a Low-Noise Charge-Detection Amplifier for VPCCD Devices"*. IEEE Trans. Electron Devices, vol. ED-31, no. 12, pp. 1713-1719, December 1984.

[6] F.Klaassen, *"On the Influence of Hot-Carrier Effect on the Thermal Noise of Field-Effect Transistors"*. IEEE Trans. Electron Devices, vol. ED-17, no. 10, pp. 858-862, October 1970.

[7] S.Kim and A.v.d.Ziel, *"Hot Electron Effect in Buried Channel MOSFET's"*. Solid-State Electronics, vol. 24, pp 425-428, October 1981.

[8] P.Centen, *"CCD On-Chip Amplifiers: Noise Performance versus MOS Transistor Dimensions"*. IEEE Trans. Electron Devices, vol. ED-38, no. 5, pp. 1206-1216, May 1991.

Chapter 4

CCD SIGNAL FILTERING
A figure of merit[5]

4.1 Introduction

The three main features which a CCD signal processor must provide are:

- suppression of reset noise (when present),
- suppression of 1/f noise at low frequencies.
- matched filtering for the joint thermal and 1/f noise and the charge signal

The reason for the first and third features is the improvement in noise performance they give and for the second is the reduction in low-frequency line noise which degrades image quality.

In the past many CCD signal processors have been proposed.
White et al. [1] introduced Correlated Double Sampling, abbreviated CDS, in 1974. CDS has been from that moment on famous for its simplicity. Simple as it may seem it does not offer a matched filter for a charge signal embedded in white noise.

---

[5] *The principles are based on a presentation at the 17th International Television Symposium Montreux, P.Centen, "Noise Optimization of CCD-on-chip amplifiers", pp. 466-496, June 1991.*

Hegyi and Burrows [2] showed that the optimal (or matched) filter for CCD signals is a differential averager, also known as a two-slope integrator. In their discussion of the matched filter they did not include the reset noise. Despite this fact they arrived at the correct result. In contrast with their findings it will be shown here that when the 1/f noise is dominant the noise performance of a differential averager compared to the optimal filter for 1/f noise will be worse for lower the clock frequencies.

Hopkinson et al. [3] gave an overview and an analysis of several types of signal processors for Floating Diffusion and Floating Gate detectors. They claimed that the work of Hegyi and Burrows was erroneous. They claimed that better filtering is possible when applying DC restoration and an additional single pole filter prior to the two-slope integration.
Unfortunately Hopkinson et al. represented the DC restoration as a Dirac sample. They neglected the fact that this makes the suppression of all reset noise impossible. This is due to the fact that the single pole filter will not reach its final value in a short time when a unit step is applied, as is the case with reset noise.

Levine [4] suggested differentiating the CCD output signal and sampling it at the moment that the charge signal reaches a maximum. Due to the differentiation the time that the charge signal is available with reduced reset noise is rather small. Hence the sample window has to be equally small as well. This leads to a high bandwidth for the sampler circuit and therefore a higher noise level than with the matched filter approach. The 'differentiation and integration' is a well established way of signal filtering in the field of particle detectors and astronomy (Buttler et al. [5]).

Hynecek [6] has developed a theory to optimize an on-chip circuit for clamp and sample processing which is a variation to the theme of CDS-type CCD signal processing. In doing so he introduced the noise efficiency factor F_n where the noise refers to the reset noise or kTC noise of the detection node. The noise after CCD signal processing (N_{proc}) is then expressed as:

$$N_{proc} = F_n \frac{\sqrt{kT\,C}}{q} \qquad \textbf{(4.1)}$$

Another variation to the theme of CCD signal filter has been devised by Ohbo et al. [7] who used a delay line (see also Centen [8]) for the subtraction of the reset level from the output signal (charge and reset level). This needs only one

sample and hold, but in principle it is just the well-known Correlated Double Sampling. The improvement in noise that is claimed is only caused by parasitic bandwidth limiting. This could also be realized by making use of some bandwidth limiting before the CDS, or by including an RC lowpass filter before the CDS and resetting the capacitor (as proposed by Wey and Guggenbühl [9]). In doing so inter-symbol (pixel) interference is reduced. This approach comes closer to a two-slope integrator. This same type of filtering, together with some other alternatives, has been discussed by McCurnin et al. [10].

All of the above-mentioned papers, with the exception of Hynecek [6], lack a practical/theoretical figure of merit to compare the signal-to-noise ratio of CCD signal processors. A figure of merit can be used to compare in a general way the performance of the different circuits with respect to the signal-to-noise ratio of the signal processing itself.

In this chapter an optimal filter for Floating Diffusion and Floating Gate detectors is derived based on first principles and variational calculus.
Based on this optimal filter a noise figure of merit is proposed (Centen [8,11]) and derived, and a lower bound is established.

The optimal signal filtering derived in this chapter is more general than the others in the sense that it also includes a class of non-destructive readout structures and structures without reset transistors. It is an extension to the theory developed by Heygi and Burrows [2].

Many CCD applications are in the field of two-dimensional imaging arrays, such as the camcorder consumer market and the professional video camera market. In these applications the imager is read out periodically. Each row resembles a TV line and each pixel on a row is clocked in a periodical fashion at a speed of f_p. Each row starts with dark reference pixels which can be used for DC restoration.

In **Section 4.2** the CCD output signal is decomposed into the following parts: reset noise, charge signal (video signal), readout noise and cross-talk.

In **Section 4.3** the optimal filter is derived based on variational calculus. After having derived the optimal filter the white noise case is studied, and, more generally, the white noise plus 1/f noise too. The consequences for the optimal filter are discussed. A first attempt is made to define a figure of merit.

In **Section 4.4** a figure of merit for the optimal filter will be defined and a lower bound will be established.

In **Section 4.5** the simplest of signal processors is discussed using the figure of merit.

In **Section 4.6** a passive implementation of an integrator section is given and its noise performance is discussed, including a comparison with the ideal integrator.

The figure of merit for the classical Correlated Double Sampler is derived in **Section 4.7**.

Finally in **Section 4.8** the conclusions are presented.

Only the effects of the filtering behaviour are studied. The reason is that with careful design it is possible to keep the noise voltage below that of the on-chip amplifier. The noise of a typical on-chip amplifier is about 20 nV/$\sqrt{}$Hz and for an op-amp about 4 nV/$\sqrt{}$Hz.

4.2 The CCD output signal decomposed

The CCD output signal is a converted charge signal. The conversion takes place on a capacitive detection node. A popular detection element is the floating diffusion region with a reset FET. Such a detection node is called a floating diffusion with reset. Theuwissen [12] gives a thorough discussion of output structures.

Before the charge signal reaches the detection node it is transported as a charge packet from an image cell through the horizontal register to the output. The end of the horizontal register is usually composed of an output gate followed by the capacitive detection node. The charge packet is dumped on the node and is converted into a voltage, the charge signal. The detection node is kept at a reference potential by means of a reset FET which is switched on and off in between charge packets. The voltage change of the detection node is sensed by the on-chip amplifier.

The output signal of a CCD consists of a stream of periodically repeated pixels, as seen in Figure 4.1:

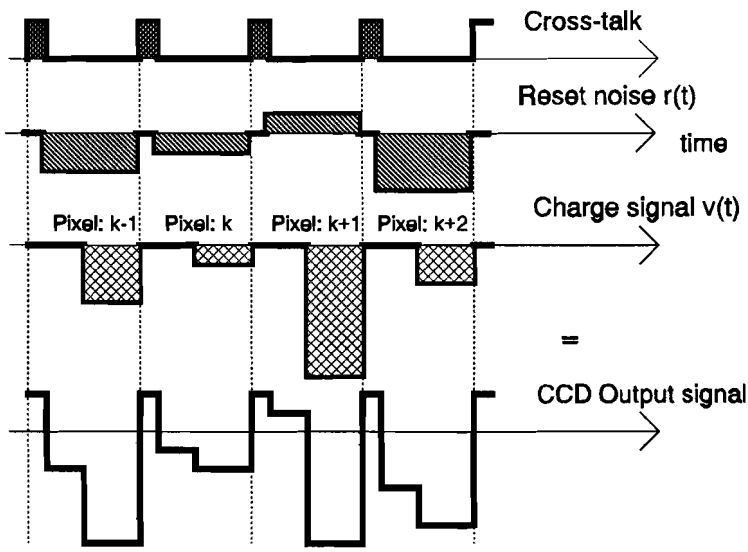

Figure 4.1: The CCD output signal decomposed into three sources.

The signal for each pixel is composed of:

- Cross-talk
- Reset noise r(t)
- Charge signal v(t)
- On-chip amplifier noise $e_n(t)$

In Figure 4.1 the cross-talk, reset noise and charge signal are depicted. The cross-talk is generated due to capacitive coupling between the capacitive detection node and the driving clocks needed to transport a charge packet through the horizontal register. It is additive in nature and therefore not really important. The only exception to this case is when one wants to quickly sample or clamp the CCD output signal. Cross-talk can deteriorate the precision with which one can sample/clamp the signal and one therefore becomes sensitive to jitter on the clocks.

The detection node is a capacitor which is charged with a charge packet. The

charge packet usually is a collection of electrons. However, before the detection node can receive a charge packet, it must be reset or cleared to avoid interference between packets (pixel cross-talk). For this purpose a reset FET is turned on for a short period of time to drain all charge from the node and off during a longer period to receive the next packet. The reset FET (switch) together with the detection node (capacitance) is a sampler with zero order hold. It also samples and holds the thermal noise of the reset FET at the instant when the reset FET is switched off. The latter is called reset noise and was first analyzed by Carnes and Kosonocky [13].
In practice the duration (T_v) of the charge signal is half a pixel period (T_p), so T_v=0.5 T_p. The reset-hold level has a duration (T_{rs}) which is usually between 25%-33% (0.25 T_p < T_{rs} < 0.33 T_p) of one time period. The reset time T_r is the time during which the reset FET is conducting. It is the difference between one pixel period and the sum of the durations for the charge signal and reset-hold level. T_r is usually between 0.16 T_p and 0.25 T_p.

4.2.1 Reset noise.

In every pixel period (T_p) the detection node capacitance is charged with a charge packet. The detection node has to be reset before the next packet can be dumped on the capacitor. This is done with a reset FET that sets the sensing node to a reference voltage. The reset FET can be electrically modelled by placing an ideal switch in series with a resistance. The circuit consisting of the reset FET and the detection node capacitance acts as a sampler circuit in which the thermal noise of the transistor channel is sampled every time it is switched off.
When the time constant of the resistance R_{on}, of the reset transistor's channel in its on state, and the capacitance C_{det}, of the detection node, is small compared to the reset time then the stationary value will be reached and the amount of reset noise is:

$$<\Delta V_{rr}^2> = \frac{kT}{C_{det}} \qquad (4.2)$$

The sensitivity of the sensing node is usually expressed in [V/e] and equals q/C_{det}. The reset noise ΔV_{rr} can also be expressed as a number of equivalent electrons (see Section 1.3):

$$N_{rr} = \frac{\sqrt{kT\ C_{det}}}{q} \tag{4.3}$$

Present day values for C_{det} are often 10 fF, and the reset noise is equivalent to about 40 e.
Teranishi [14] has added to this model by showing that the amount of reset noise depends not only on R_{on} but also the shape of the channel. The shape determines how much of the charge stored in the channel of the reset FET is partitioned between the detection node side and the reference voltage side when the transistor switches off. This introduces partition noise. The shaping of the reset FET has also been applied by Theuwissen et al. [15] in one of the Philips CCD imagers. The partition noise is a second order effect to the reset noise and of no importance in present day cameras, which have signal filtering which suppresses reset noise to a large extent.

A second modification is the effect a high channel resistance will have on the reset noise, which will decrease because the signal will not reach a stationary value (Barbe [16]) within the time allotted for resetting (T_{rs}).
Then

$$<\Delta V_{rr}^2> = \frac{kT}{C_{det}} \left(1 - e^{-2\frac{T_{rs}}{\tau}} \right) \tag{4.4}$$

with $\tau=C_{det}\ R_{on}$. This equation is only valid for a capacitor which has no initial charge. However, the reset FET switches periodically and the reset noise will reach a stationary value after some time. Therefore, changing the on-resistance will not help in reducing the amplitude of the reset noise. It will only change the shape of the reset noise spectral density.

Some extensive calculations on the reset noise have been performed by Hynecek [17] and Centen [18].

The shape of the reset noise is the same for each pixel (Figure 4.1). Only the amplitude differs from pixel to pixel. It is this property which makes it possible to write the reset noise r(t) in the k-th pixel as the product of an amplitude R_k and a waveform function $g_r(t)$

$$r(t) = R_k \, g_r(t - kT_p) \tag{4.5}$$

After a Fourier transformation this becomes

$$R(f) = R_k \, G_r(f) \, e^{-j2\pi fkT_p} \tag{4.6}$$

The amplitude of the reset noise differs from pixel to pixel with an average value of zero. The variance of the reset noise is

$$< R_k \, R_k > = N_{rr}^2 = \frac{kT\,C}{q^2} \tag{4.7}$$

The output $r_h(t)$ of a yet unknown filter h(t) with input r(t) is

$$r_h(t) = h(t) \otimes r(t) \tag{4.8}$$

4.2.2 The charge signal.

Halfway trough the pixel period (Figure 4.1) charge is dumped onto the capacitive detection node and causes a change in potential. This is called the charge signal. The reset noise that was generated prior to the charge dump and the noise of the on-chip amplifier are added to the charge signal. At the end of one pixel period (T_p) the reset FET is again switched on.
Just as is the case with the reset noise, the charge signal can also be written as the product of an amplitude (V_k) and a waveform function (g_v).
Consequently the charge signal in the k-th pixel is written as

$$v(t) = V_k \, g_v(t - kT_p) \tag{4.9a}$$

or as its Fourier transform

$$V(f) = V_k \, G_v(f) \, e^{-j\,2\pi fkT_p} \tag{4.9b}$$

where

$$V_k = \frac{q\,N}{C_{det}} \tag{4.10}$$

and

q charge of one electron
N the number of electrons in charge packet n
C_{det} the detector capacitance

The ratio V_k/N is called the "sensitivity" and is expressed in [μV/e]. Although this is not a standard unit, its use is an established custom in the field of CCD imaging.

4.2.3 Readout noise.

The detection node capacitance can be made as low as 10 fF. To drive a capacitive load of several picofarads it is necessary to buffer the potential changes at the node with an on-chip amplifier. Of course this amplifier adds noise to the signal. The number of stages of the on-chip amplifier is usually 1, 2 or 3 depending on speed requirements. The part of the on-chip amplifier that determines noise is the first stage and the driving properties are determined by the last stage. In general, the noise spectral density can be written as:

$$S_{ee}(f) = \frac{\eta}{2}\left[1 + \left|\frac{F_c}{f}\right|\right] \qquad (4.11)$$

where η is the white noise level and F_c the cross-over frequency between 1/f noise and white noise. The factor of 2 in the spectral density comes from the two-sided representation.
After linear filtering of the readout noise $e_n(t)$ we obtain

$$e_{n,h}(t) = h(t) \otimes e_n(t) \qquad (4.12)$$

The noise spectral density of the on-chip amplifier can be expressed as [V^2/Hz] but when divided by the charge-to-voltage gain (sensitivity) of the capacitive detection node [V/e] the noise spectral density can also be represented in [e^2/Hz]. It is then known as the Noise Electron Density (NED, Chapter 2). This is a better way to express the noise of an on-chip amplifier, rather than expressing it in the number of electrons or V^2/Hz.

Figure 4.2 gives a block diagram which shows the input signals to the on-chip amplifier and an optimal filter h(t) which has yet to be determined.

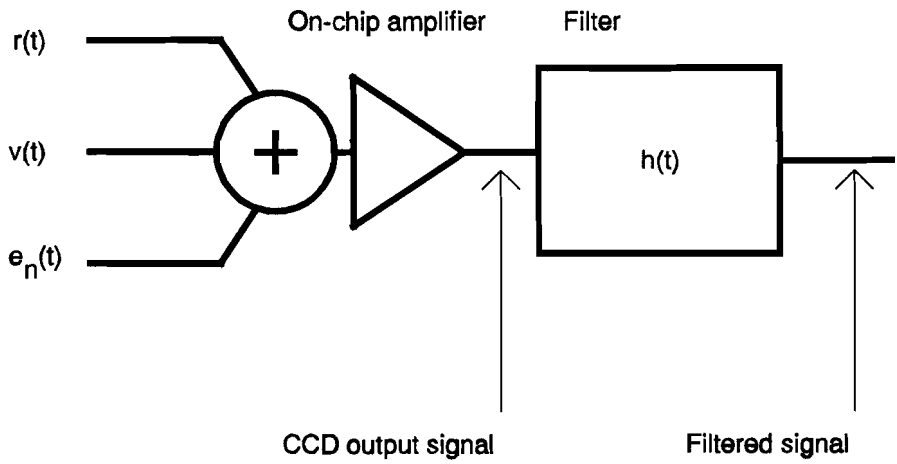

Figure 4.2: Depiction of the signal sources that enter the (matched) filter.

4.3 The optimal filter problem

4.3.1 Posing the variational problem.

One pixel consists of the charge signal, the reset noise, and the amplifier noise (Figure 4.1).

The problem is to find a filter that does not degrade the resolution (by introducing inter-pixel cross-talk) and has optimal filtering properties with respect to the amplifier noise and reset noise as a whole.

For the k-th pixel it is desired that the sum of the mean squared on-chip amplifier noise (e_n and $e_{n,h}$, Section 4.2.3) and the reset noise (r and r_h, Section 4.2.1) must reach a minimum after filtering at $t=kT_p$:

$$\min \left[< r_h(kT_p)\, r_h^*(kT_p) > + < e_{n,h}(kT_p)\, e_{n,h}^*(kT_p) > \right] \qquad (4.13)$$

Provided that the amplitude of the charge signal (v and v_h, Section 4.2.2) is the same before and after filtering at $t=kT_p$, which is equivalent to no degradation of the resolution,

$$v_h(kT_p)\ v_h^*(kT_p) = V_k^2 \tag{4.14}$$

Transforming the above time domain description into the frequency domain gives a rather simple solution to the optimisation problem.
Without losing generality by taking k=0 the following must be minimized

$$\min \left[\begin{array}{l} \langle R_k\ R_k \rangle \int_{-\infty}^{\infty} G_r(f)\ H(f)\ df \int_{-\infty}^{\infty} G_r^*(f)\ H^*(f)\ df \\ \\ \qquad + \int_{-\infty}^{\infty} S_{ee}(f)\ H(f)\ H^*(f) df \end{array} \right] \tag{4.15}$$

with the constraint

$$V_k^2 \int_{-\infty}^{\infty} G_v(f)\ H(f)\ df \int_{-\infty}^{\infty} G_v^*(f) H^*(f)\ df = V_k^2 \tag{4.16}$$

After introducing the Lagrange λ-multiplier and equating the above variational we obtain after the use of equation (4.7)

$$\int_{-\infty}^{\infty} \int_{-\infty}^{\infty} \delta H^* \left[N_{rr}^2\ G_r^*\ \Gamma_1 \ + \ S_{ee}\ H(f) \ + \ \lambda\ G_v^*\ \Gamma_2 \right] df = 0 \tag{4.17}$$

Here

$$\Gamma_1 = \int_{-\infty}^{\infty} G_r(f) H(f) df$$

and

$$\Gamma_2 = \int_{-\infty}^{\infty} G_v(f)H(f)df$$

are two constants.

Equation (4.17) is zero for any frequency (f) and variation (δH) if and only if the term between brackets is zero. By re-defining the constants in equation (4.17) as $\alpha=-N_{rr}^2\cdot\Gamma_1$ and $\beta=-\lambda\cdot\Gamma_2$ the optimal filter H should satisfy:

$$H_{opt}(f) = \left[\alpha \frac{G_r^*(f)}{S_{ee}(f)} + \beta \frac{G_v^*(f)}{S_{ee}(f)} \right] \qquad (4.18)$$

This filter has a high gain when the on-chip amplifier noise $S_{ee}(f)$ is low and/or the charge signal spectral contribution is high. In contrast to the matched filter derived by Hegyi and Burrows [2] the denominator also includes the reset noise. In the following section some special cases will be investigated further.

4.3.2 The optimal filter in the presence of white noise only.

With a simple approximation (which is not that far off from reality) one can describe the function for the reset noise and the charge signal as rectangular waveforms.
For the timing of the signals the following relations are defined (Figure 4.3). At $t=-T_p$ the reset FET is turned on and after a time T_p-T_r the reset FET is switched off. During T_{rs} (reset-hold level interval) only reset noise is present and at the end of this time interval charge is dumped on the detection node capacitance. During the time interval T_v both the charge signal and reset noise are present. One readout cycle takes a pixel period T_p.

The reset noise waveform function can be described by

$$g_r(t) = RECT\left(\frac{t+\frac{T_r}{2}}{T_r}\right) = RECT\left(\frac{t+\frac{T_v}{2}}{T_v}\right) + RECT\left(\frac{t+T_v+\frac{T_{rs}}{2}}{T_{rs}}\right) \qquad (4.19)$$

where the addition of the two terms on the right side are two non-overlapping (disjoint) waveform functions. This latter description simplifies the following analyses.

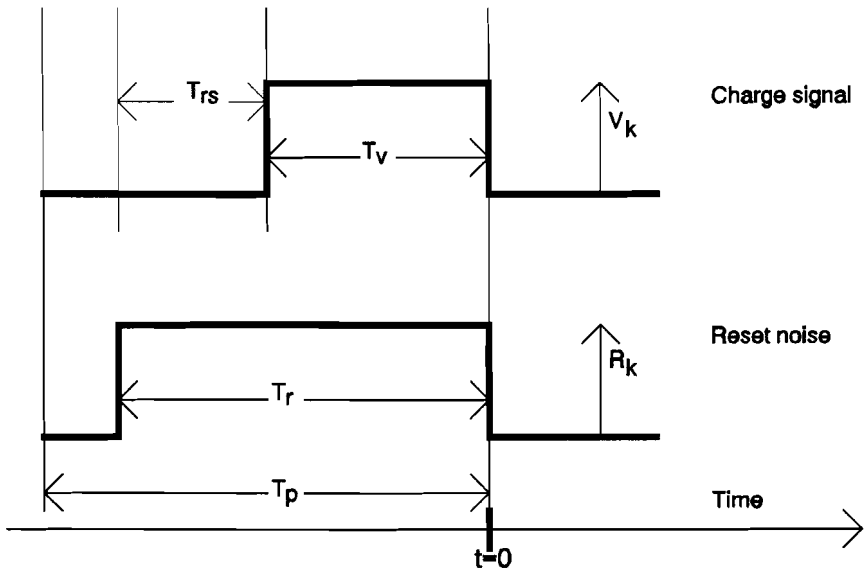

Figure 4.3: Shape of the reset noise and the charge signal.

The charge signal waveform function is given by

$$g_v(t) = RECT\left(\frac{t+\frac{T_v}{2}}{T_v}\right) \tag{4.20}$$

When only white noise ($S_{ee}(f)$=NED/2 is a constant) is present the optimal filter can be written as

$$H_{opt}(f) = \left[\alpha\ G_r^*(f) + \beta\ G_v^*(f)\right] \tag{4.21}$$

The Fourier transforms of equation (4.19) and equation (4.20) are denoted by $G_r(f)$ and $G_v(f)$, respectively.

In the time domain the output of the filter is the convolution of the impulse response of the filter to the input signal. However the impulse response is a constant for a given period of time, as described by the rectangular functions (4.19) and (4.20). It therefore describes an integrator (Figure 4.4); to be precise, a two-slope integrator with one slope for the reset noise and the other for the charge signal.

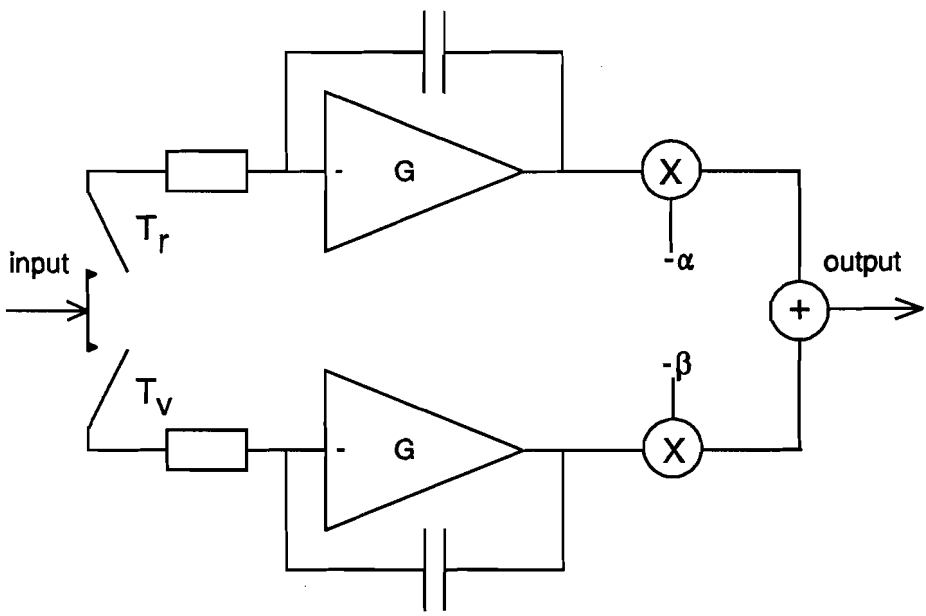

Figure 4.4: The matched filter for the white noise case.

With this in mind one can evaluate the filter coefficients in equation (4.21) in an easy way.
By integrating the charge signal as shown in Figure 4.3, and from the condition that the amplitude must remain the same after filtering (equation (4.16)), we obtain:

$$\alpha\ T_v\ V_k + \beta\ T_v\ V_k = V_k \qquad (4.22)$$

which reduces to

$$\alpha + \beta = \frac{1}{T_v} \tag{4.23}$$

The noise after filtering, N^2_∞ (equation (4.15)), consists of two parts. The first term is the remainder of the reset noise and the second term is the filtered noise of the on-chip amplifier:

$$N^2_\infty = \langle R_k\, R_k \rangle \int_{-\infty}^{\infty} G_r(f_1)\, H(f_1)\, df_1 \int_{-\infty}^{\infty} G_r^*(f)\, H^*(f)\, df$$

$$+ \int_{-\infty}^{\infty} S_{ee}(f)\, H(f)\, H^*(f) df \tag{4.24}$$

The second term in the above equation is evaluated using equation (4.21) after substituting the Fourier transforms of equation (4.19) and (4.20). Defining the spectral density of the on-chip amplifier as $S_{ee}(f)=NED/2$ and using $T_{rs}=T_r-T_v$ (Figure 4.3) to define two disjunct time intervals T_{rs} and T_v, the mean squared noise after filtering reads

$$\int_{-\infty}^{\infty} S_{ee}(f)\, H(f)\, H^*(f)\, df = \alpha^2\, NED\, \frac{T_{rs}}{2} + (\alpha+\beta)^2\, NED\, \frac{T_v}{2} \tag{4.25}$$

Substituting equation (4.23), equation (4.25) reduces to

$$\int_{-\infty}^{\infty} S_{ee}(f)\, H(f)\, H(f)^* df = \alpha^2\, NED\, \frac{T_{rs}}{2} + \frac{NED}{2T_v} \tag{4.26}$$

The other contribution to the mean squared noise after filtering is the reset noise, given by the first term in equation (4.24). The reset noise, which has a constant value (R_k) during the time T_r (see Figure (4.3)), is much easier to evaluate in the time domain where the integration is over T_v and T_r (see Figure (4.4)). The latter reads

$$\alpha\ R_k\ T_r + \beta\ R_k\ T_v \quad , \tag{4.27}$$

the mean squared value of which is given by

$$\langle R_k\ R_k \rangle \int_{-\infty}^{\infty} G_r(f_1)\ H(f_1)\ df_1 \int_{-\infty}^{\infty} G_r^*(f)\ H^*(f)\ df = (\alpha T_r + \beta T_v)^2 \langle R_k R_k \rangle \tag{4.28}$$

This is the evaluation of the first term of equation (4.24).
With equations (4.7) and (4.23) and using $T_{rs}=T_r-T_v$ equation (4.28) reduces to

$$\langle R_k\ R_k \rangle \int_{-\infty}^{\infty} G_r(f_1)\ H(f_1)\ df_1 \int_{-\infty}^{\infty} G_r^*(f)\ H^*(f)\ df = (\alpha T_{rs} + 1)^2\ N_{rr}^2 \tag{4.29}$$

Both noise contributions in equations (4.26) and (4.29) are added to obtain the total noise

$$N_\infty^2 = (\alpha\ T_{rs} + 1)^2\ N_{rr}^2 + \alpha^2\ NED\ \frac{T_{rs}}{2} + \frac{NED}{2T_v} \tag{4.30}$$

In order to determine the value of the coefficients α and ß in equation (4.30) which minimize the noise energy the first derivative of equation (4.30) with respect to α has to be calculated. From the zero value of the first derivative it follows that

$$\alpha = -\frac{1}{T_{rs}}\ \frac{1}{1 + \dfrac{NED}{2\ T_{rs}\ N_{rr}^2}} \tag{4.31}$$

The other coefficient ß is related to α via equation (4.23).
The noise after optimal filtering is therefore obtained by substituting the α value given in equation (4.31) into equation (4.30)

$$N_\infty^2 = NED \left[\frac{1}{2T_{rs}} \frac{1}{1 + \frac{NED}{2\,T_{rs}\,N_{rr}^2}} + \frac{1}{2T_v} \right] \tag{4.32}$$

The noise after optimal filtering N_∞ is only determined by the amount of reset noise (N_{rr}), the noise spectral density of the on-chip amplifier (NED), the time $T_{rs}=T_r-T_v$ that only reset noise is available, and the time T_v that both reset noise and the charge signal is available.

Equation (4.32) shows that the noise voltage after optimal filtering consists of two parts. One is the contribution of the noise during the reset-hold level (T_{rs}) and the other is during the time the charge signal is available (T_v). The latter is independent of the reset noise level. The first contribution depends on both the reset noise level and the readout noise NED during the interval T_{rs}.
When no reset noise is generated there is no need for the use of the reset reference level interval T_{rs} and one only has to filter the noise and signal during interval T_v. However, when there is a large amount of reset noise one must reduce it and the penalty is an increase in the noise level due to the additional readout noise.

The factor

$$R_{rr} = \frac{2T_{rs}N_{rr}^2}{NED} \tag{4.33}$$

can be considered as a normalized reset noise. It is the ratio between the reset noise and the noise of the on-chip amplifier that is collected during the time when only reset noise is present.

Introducing at this point somewhat artificially

$$N_\infty^2 = M \cdot NED \cdot \frac{f_p}{2} \tag{4.34}$$

then M is defined via equations (4.32) and (4.34) as:

$$M = \frac{2N_\infty^2}{f_p NED} = \frac{T_p}{T_{rs}} \frac{1}{1 + \frac{NED}{2\,T_{rs}\,N_{rr}^2}} + \frac{T_p}{T_v} \qquad (4.35)$$

M is a dimensionless quantity.
Since the derivation of the optimal filter was under the condition of minimized mean squared noise (minimal N_∞^2), this implies that the dimensionless quantity M is also at a minimum for a given clock frequency f_p. Therefore it represents a figure of merit for the filter action.

Substituting some practical values for the timing intervals,
$T_{rs}=T_p/3$ and $T_v=T_p/2$, M ranges from 2 to 5 depending on the level of reset noise. When use is made of a floating gate readout, which exhibits no reset noise ($N_{rr}=0$), the figure of merit M=2.

Generally two asymptotic regimes can be distinguished, one at zero reset noise and the other at high reset noise.
Regime 1: zero reset noise $N_{rr}=0$,

$$M = \frac{T_p}{T_v} \qquad (4.36)$$

Regime 2: infinite reset noise $N_{rr}=\infty$,

$$M = \frac{T_p}{T_v} + \frac{T_p}{T_{rs}} \,. \qquad (4.37)$$

Take for example present state of the art values for the noise: $N_{rr}=40$ e and $NED=6\cdot10^{-6}$ e^2/Hz. At $f_p=18$ MHz readout $T_{rs}=18.5$ ns and $T_v=27.8$ ns. The normalized reset noise is then $R_{rr}=N^2_{rr}\ 2\ T_{rs}/NED = 10$ and a lower bound for the figure of merit M (given by the optimal filtering) is M=4.73 .

In Figure 4.5 the figure of merit M is plotted as a function of the (normalized) reset noise $R_{rr}=N^2_{rr}\cdot2\cdot T_{rs}/NED$ for the cases in which the duration of the reset noise reference level equals the duration of the charge signal ($T_{rs}/T_v=1$) and for $T_{rs}/T_v=2/3$ and $T_{rs}/T_v=1/2$.

The asymptotic values of the figure of merit are M=2 (independent of T_{rs}/T_v) for

small values of reset noise and M=4 (T_{rs}/T_v=1), M=5 (T_{rs}/T_v=2/3) and M=6 (T_{rs}/T_v=1/2) for large values of reset noise.

A transition region exists for values of the normalized reset noise R_{rr} between 0.1 and 10. For small values less than 0.1 the optimal filter can be used for floating gate readout structures. The optimal filter for these cases is a one-slope integrator. This can be seen from inspection of equation (4.21) where in this case α (equation (4.31)) is negligibly small compared with β (equation (4.23)). For measurements of the figure of merit for actual signal processors see Section 4.5.5 and Section 4.7.

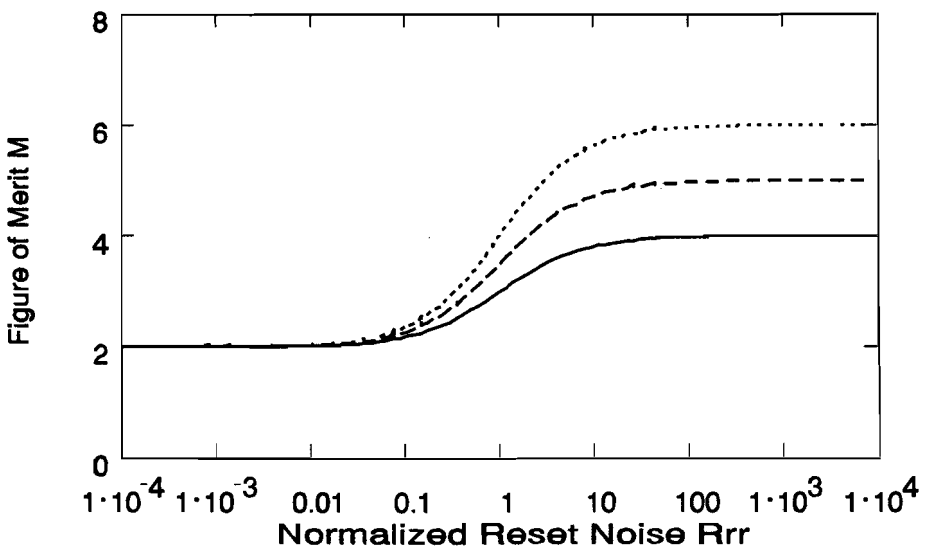

Figure 4.5: *A figure of merit M, equation (4.35), for the optimal filter in the white noise case. The parameter values used are T_{rs}/T_v=1 (solid line), T_{rs}/T_v=2/3 (dashed line) and T_{rs}/T_v=1/2 (dotted line). The curves are a function of the normalized reset noise $R_{rr}=N^2_{rr}\cdot 2\cdot T_{rs}/NED$.*

Note that a small value for the normalized reset noise does not necessarily mean small values for the reset noise itself. It could also be that the clock frequency is high, and therefore T_{rs} is small in equation (4.33).
For values of R_{rr} higher than 10 the optimal filter is a two-slope integrator, as

an inspection of equations (4.31), (4.23), and (4.21) shows. This will be elaborated upon in the next section.

4.3.3 Two limiting cases.

The two limiting cases are zero reset noise and infinite reset noise. The case of zero reset noise is encountered when one uses a floating gate readout structure (Brewer [19], Hobson et al. [20], Matsunaga [21], Roks et al. [22]). A more exotic structure has been proposed by Roks et al. [23]. The case of infinite reset noise is for the purpose of inspecting equation (4.32). This case is also equivalent with the condition of 'DC blocking' and 1/f noise suppression.

Zero reset noise or $N_{rr}=0$; In this case the mean squared noise after optimal filtering reduces to:

$$N_{\infty}^2 = \frac{NED}{2\,T_v} \tag{4.38}$$

To calculate the noise one only needs to know the spectral density of the on-chip amplifier (NED) and the time that the charge signal is available (T_v). The filter coefficients in equation (4.21) are $\alpha=0$ (equation (4.31)) and $\beta=1/T_v$ (equation (4.23)). Using the Fourier transform of equation (4.20) and substituting into equation (4.21) the impulse response is given by

$$h_{opt}(t) = \frac{1}{T_v}\,RECT\left(\frac{t+\frac{T_v}{2}}{T_v}\right) \tag{4.39}$$

The function RECT(x) is 1 for $|x|<0.5$ and 0 elsewhere and can be found in the "List of symbols and functions". The Fourier transform of the above impulse response is the transfer function of this filter and is given by

$$H_{opt}(f) = sinc(f\,T_v)\,e^{-j\,2\pi f\,\frac{T_v}{2}} \tag{4.40}$$

At f=0, H_{opt} is not zero, the DC component is not suppressed, and neither is the 1/f noise.

In a practical imager application the above impulse response would not be sufficient: it would fulfil the part of having an optimal filter characteristic but it lacks DC restoration. DC restoration means that the output of an optimal filter should be zero when no charge signal is applied. Clamping once during a TV line would be sufficient to fulfil the DC restoration. For this reason many CCD imagers have so-called black reference pixels, pixels that are covered by a light shield, at the beginning of each row. These can be used for DC restoration without deteriorating the noise properties of the camera.
If 1/f noise suppression is also needed then a solution is given in the next section.
The figure of merit for the optimal filter for floating gate structures is $M=T_p/T_v=2$.

DC blocking and/or reset noise is very dominant: $N_{rr}=\infty$
There are cases in which one wants to block any DC component that is contained in the base band signal or when there is a need for 1/f noise suppression since it causes large scale disturbances in the image.
In the this situation two additional constraints must be applied to the solution of the filter coefficients α and β. First, the transfer function (equation 4.21) at zero frequency must be zero to obtain DC blocking. Second, the squared transfer function multiplied by 1/f must be zero in the limit as the frequency approaches zero to suppress 1/f noise.

With the above additional constraints equation (4.32) reduces to:

$$N_\infty^2 = \left(\frac{1}{2T_{rs}} + \frac{1}{2T_v} \right) \cdot NED \qquad (4.41)$$

The above equation shows that the noise present at the output of the optimal filter is determined only by the noise of the on-chip amplifier (NED) and the length of the time intervals during which only reset noise (T_{rs}) and both charge signal and reset noise (T_v) are available.
Using equations (4.21), (4.23) and (4.31) the impulse response of this filter is given by

$$h_{opt}(t) = \frac{1}{T_v} RECT\left[\frac{t + \frac{T_v}{2}}{T_v}\right] + - \frac{1}{T_{rs}} RECT\left[\frac{t + T_v + \frac{T_{rs}}{2}}{T_{rs}}\right] \tag{4.42}$$

By Fourier transforming the above impulse response the transfer function is found and reads:

$$H_{opt}(f) = sinc(f\,T_v)\, e^{-j2\pi f \frac{T_v}{2}} - sinc(f\,T_{rs})\, e^{-j2\pi f\left(T_v + \frac{T_{rs}}{2}\right)} \tag{4.43}$$

This transfer function has a maximum near f_p. (See Figure 4.6)
On the one hand this kind of solution is sometimes found in the literature even though there is a better choice with respect to noise performance. On the other hand when additional 1/f noise suppression and DC blocking is needed then equation (4.43) is the transfer function to use.
(The better noise performance is given by the transfer function given in equation (4.21) under substitution of equations (4.23) and (4.31) and can be judged from Figure 4.5)

A typical value for the figure of merit is $M=T_p/T_v+T_p/T_{rs}=5$. The maximum duration of the time interval in which only reset noise is available (T_{rs}) is T_p-T_v. Since many CCD imagers are driven in such a fashion that $T_v=T_p/2$ this limits the ratio T_{rs}/T_p to 2. This implies that the figure of merit can never reach a value below M=4.

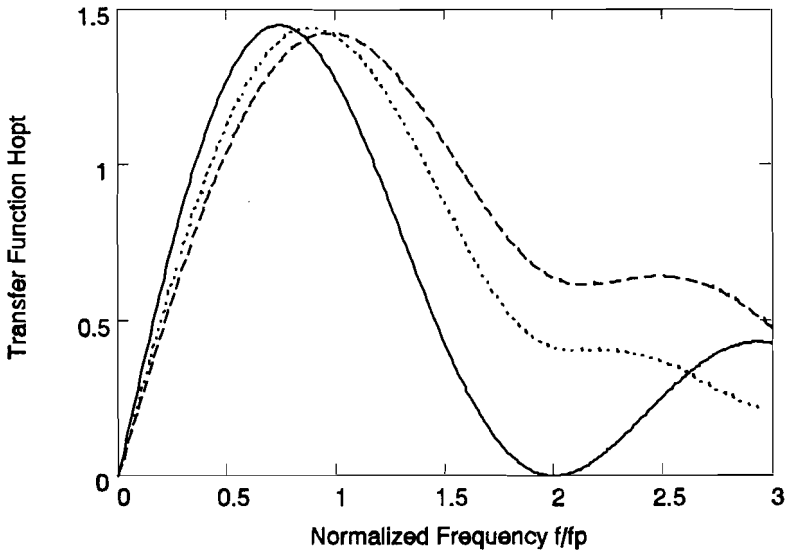

Figure 4.6: The transfer function for the optimal filter for $T_v=T_p/2$ and the cases $T_{rs}=T_p/2$ (solid line). $T_{rs}=T_p/3$ (dotted line), and $T_{rs}=T_p/4$ (dashed line)

4.3.4 1/f noise and the optimal white noise filter.

The optimal filter in the presence of only white noise was derived in the previous sections. In practice one will never encounter only white noise. 1/f noise will be present too.

Especially in video applications it is necessary to have 1/f noise suppression to avoid low frequency disturbances for the effect is has on image quality.

A condition for 1/f noise suppression is that the transfer function of the filter has no response for f=0. This situation has already been described in Section 4.3.3. Given the transfer function in equation (4.43) the effect of the mean squared 1/f noise can be calculated. The reset noise is fully suppressed and only the second term of equation (4.24) remains. For a noise spectrum consisting of 1/f noise and white noise the noise energy after 'white noise optimal filtering' (equation (4.24)) reduces to

$$N_\infty^2 = \int_{-\infty}^{\infty} H(f)\, H^*(f) S_{ee}(f) df = \int_{-\infty}^{\infty} | H_{opt}(f) |^2 \frac{NED}{2} \left[1 + \left| \frac{F_c}{f} \right| \right] df \quad (4.44)$$

With the figure of merit M defined in equation (4.34) and using M_{white} as the value for the white noise case equation (4.37) the above simplifies with equation (4.43) to:

$$N_{\infty}^2 = M \cdot NED \cdot \frac{f_p}{2} = M_{white} \cdot \left[1 + \frac{F_c}{F_{eq}} \right] NED \cdot \frac{f_p}{2} \qquad (4.45)$$

The ratio F_c/F_{eq} is a relative measure for the amount that the 1/f noise contributes to the total noise performance.
In the following table the noise performance is given for this case of white and 1/f noise. The table gives calculated values for the figure of merit M and the relative contribution of the 1/f noise for several values of the duration of the reset reference level T_{rs}.

T_{rs}/T_v; T_v/T_p=1/2	M_{white}	F_{eq}/f_p
1	4	0.721
2/3	5	0.900
1/2	6	1.050
2/5	7	1.196

From the above table one can conclude that as long as the corner frequency between 1/f noise and thermal noise (F_c) is (far) below the horizontal clock frequency (f_p) the contribution of the filtered 1/f noise to the noise energy is so low that the white noise approximation remains valid. When the clocking frequency is at least 10 times the corner frequency of the 1/f noise, the deviation from the white noise case will be less than 0.6 dB.

Inspection of equation (4.45) shows that it helps to clock the sensor as slowly as possible. But no improvement in noise performance is to be gained from a clock frequency below $F_c/10$.

In this case the noise is limited to

$$N_\infty^2 = M_{white} \cdot NED \cdot \frac{F_c}{2r} \tag{4.46}$$

and is fully determined by the ratio of the timing intervals T_{rs}/T_v and T_v/T_p (M_{white}, equation (4.37)) and the corner frequency (F_C) of the 1/f noise.

4.3.5 Discussion of the figure of merit for the white noise case.

The previous section gave a derivation of the optimal filter in the presence of white noise was given and an expression for the noise was derived. Its value N^2_∞ can be obtained when the optimal filtered CCD signal is digitized. However, the signal is more often than not digitized but is used in an analog fashion. The output signal of the optimal filter is usually put through a zero-order hold circuit. This sampler shapes the noise spectral density with sin(x)/x, just as the electrical modulation transfer function does:

$$S_{nn}(f) = \frac{N_\infty^2}{f_p} sinc^2\left(\frac{f}{f_p}\right) \tag{4.47}$$

Integrating the noise spectral density in the full bandwidth gives the same result as before:

$$\int_{-\infty}^{\infty} S_{nn}(f)\, df = N_\infty^2 \tag{4.48}$$

Therefore digitizing is only a special case of the analog output.

With equation (4.34) the noise spectral density (equation (4.47)) can also be written as:

$$S_{nn}(f) = M \cdot \frac{NED}{2} \cdot sinc^2\left(\frac{f}{f_p}\right) \tag{4.49}$$

Here M, which was introduced in Section 4.3.2, plays the role of noise figure. The noise figure M is the amount with which the white noise is increased due to

signal processing. For white noise with a matched filter it is given by equation (4.35). Both on-chip amplifier noise and reset noise form part of this noise figure.

In a practical application one has to suppress 1/f noise at low frequencies and DC blocking is needed. Then the figure of merit M reduces to

$$M = \frac{T_p}{T_{rs}} + \frac{T_p}{T_v} \qquad (4.50)$$

M is determined only by the timing ratios of the reset-hold level (T_{rs}) and the duration of the charge signal (T_v).
Since the noise was derived for the optimal case, this figure of merit is at the same time the lowest possible value one can achieve.
Its value cannot become lower than M=4 since $T_{rs} \leq T_v$ and the duration of the charge signal is fixed to $T_v=T_p/2$.
In a practical situation $T_{rs}=T_p/3$ and M increases towards 5.
One cannot go below this figure without sacrificing pixel resolution or suffering pixel cross talk.

4.3.6 Multiple outputs and the figure of merit.

In the early days of CCD imaging an imager could have as many as 3 outputs. The output signals of these three outputs were separately filtered and multiplexed into one output stream of pixels. HDTV imagers, with pixel frequencies of 72 MHz, use only 2 outputs. Each output runs at 36 MHz and are multiplexed after filtering into a single pixel stream at 72 MHz. Present day CCD imagers usually have 1 output. In the emerging field of CMOS imagers (Wong [24], Fossum [25]) the number of outputs is again 1, but the pixel stream of one output is generated internally by multiplexing every column into one output stream of pixels. The number of columns can be as high as 640.
The figure of merit for the case of m outputs multiplexed into one can be derived using equation (4.50).
The clock frequency f_p is the pixel rate after multiplexing the output signals. The clock frequency of one output is f_p/m, the duration of the reset-hold level $T_{rs}=\delta_{rs}\ m/f_p$, and the duration of the charge signal $T_v=\delta_v\ m/f_p$. Compared to the one output situation the time intervals, for averaging the noise, are increased by a factor m. The duration of one pixel after multiplexing is $1/f_p$. Therefore, in the

case of m multiple CCD output stages multiplexed into one the noise figure becomes

$$M_m = \frac{M}{m} \tag{4.51}$$

This is one of the reasons why a CMOS imager (m=640 or more!) can reach a reasonable noise figure even when the noise performance of a CMOS column amplifier and/or active pixel readout is worse than the on-chip amplifiers used in CCD imagers.

4.3.7 The optimal filter with 1/f noise.

In a previous section the optimal filter was calculated for the white noise case with rectangular shaped wave forms. In every day practice one also encounters 1/f noise. In this section the mean squared noise will be calculated for this general situation and a figure of merit for the filter will be derived too.

The optimal filter defined in equation (4.18), after substituting the Fourier transformed charge and reset noise waveform functions in equations (4.19) and (4.20), reads as:

$$H_{opt}(f) = \frac{\beta\ T_v\ sinc(fT_v)\ e^{-j\omega\frac{T_v}{2}} + \alpha\ T_{rs}\ sinc(fT_{rs})\ e^{-j\omega\left(T_v+\frac{T_{rs}}{2}\right)}}{1 + \left|\frac{F_c}{f}\right|} \tag{4.52}$$

A first inspection shows that H_{opt} does block DC signals since $H_{opt}(0)=0$ as long as $F_c>0$. Furthermore,

$$\lim_{f\to 0} \frac{|H_{opt}(f)|^2}{f} = 0 \tag{4.53}$$

The latter is needed for sufficient suppression of the 1/f noise in CCD imaging applications. The coefficients α and β can be calculated from the condition

$$\int_{-\infty}^{\infty} H_{opt}(f)\ G_v(f)df = \int_{-\infty}^{\infty} \frac{\alpha\ G_{rs}^*(f) + \beta\ G_v^*(f)}{S_{ee}(f)}\ G_v(f)\ df = 1 \tag{4.54}$$

for the normalized charge signal and the minimized mean squared noise.

Now one needs to find the values for the coefficients α and β.

First a recapitulation of some parameters from Appendix C is given.
Parameter A (equation (C17)) is

$$A = \int_{-\infty}^{\infty} \frac{G_v^*(f)\, G_v(f)}{S_{ee}(f)}\, df \tag{4.55}$$

and parameter B (equation (C18)) is

$$B = \int_{-\infty}^{\infty} \frac{G_{rs}^*(f)\, G_v(f)}{S_{ee}(f)}\, df \tag{4.56}$$

and parameter C (equation (C19) is

$$C = \int_{-\infty}^{\infty} \frac{G_{rs}^*(f)\, G_{rs}(f)}{S_{ee}(f)}\, df = 1 \tag{4.57}$$

Using the analysis in Appendix C, the normalisation of the charge signal (equation (4.54)) reduces to

$$\beta A + \alpha B = 1 \tag{4.58}$$

or

$$\beta = \frac{1 - \alpha B}{A} \tag{4.59}$$

The amount of reset noise after filtering is given by

$$R_k \int_{-\infty}^{\infty} H_{opt}(f)\, G_r(f)\, df = \tag{4.60}$$

$$R_k \left[\int_{-\infty}^{\infty} \frac{\left(\alpha\, G_{rs}^*(f) + \beta\, G_v^*(f) \right)}{S_{ee}(f)}\, G_{rs}(f)\, df + 1 \right]$$

where use has been made of the Fourier transform of equations (4.19) and (4.20) under substitution of equation (4.54).

After substituting equations (4.56) and (4.57) in the above equation the following result is obtained

$$R_k \int_{-\infty}^{\infty} H_{opt}(f)\, G_r(f)\, df = R_k \left[\alpha\, C + \beta\, B + 1 \right] \tag{4.61}$$

Finally, the mean squared reset noise after filtering equals (first part of equation (4.24))

$$N_{rr}^2 \left[\alpha\, \frac{A\, C - B^2}{A} + \frac{B}{A} + 1 \right]^2 \tag{4.62}$$

where for the calculation of the mean squared value in equation (4.61) use has been made of equations (4.7) and (4.59).

The readout noise after filtering, the second part of equation (4.24), is given by

$$\int_{-\infty}^{\infty} H_{opt}(f)\, H_{opt}^*(f)\, S_{ee}(f)\, df = \tag{4.63}$$

$$\int_{-\infty}^{\infty} \left[\frac{\left(\alpha^2\, G_{rs}^*(f)\, G_{rs}(f) + \beta^2\, G_v^*(f)\, G_v(f) \right)}{S_{ee}(f)} + 2\, Re\left(\alpha\, \beta\, \frac{G_v(f)\, G_{rs}^*(f)}{S_{ee}(f)} \right) \right] df$$

which reduces with the parameters A-C defined in equations (4.55), (4.56) and (4.57) to

$$\int_{-\infty}^{\infty} H_{opt}(f)\, H_{opt}^{*}(f)\, S_{ee}(f)\, df = \frac{NED}{2}\left[\, \alpha^2\, C + \beta^2\, A + 2\, \alpha\, \beta\, B \,\right] \qquad (4.64)$$

This uses the noise spectral density from equation (4.11) with η=NED.

After substituting β (see equation (4.59)) in the above equation one obtains

$$\int_{-\infty}^{\infty} H_{opt}(f)\, H_{opt}^{*}(f)\, S_{ee}(f)\, df = \frac{NED}{2}\left[\, \alpha^2\, \frac{AC - B^2}{A} + \frac{1}{A} \,\right] \qquad (4.65)$$

The reset noise and the readout noise together after filtering are given by adding the mean squared contributions derived in equation (4.62) and equation (4.65). The sum is

$$N_{\infty}^2 = N_{rr}^2\left[\, \alpha\, \frac{AC - B^2}{A} + \frac{B}{A} + 1 \,\right]^2 + \frac{NED}{2}\left[\, \alpha^2\, \frac{AC - B^2}{A} + \frac{1}{A} \,\right] \qquad (4.66)$$

and reaches a minimum for

$$\alpha = -\frac{A + B}{AC - B^2}\, \frac{1}{\dfrac{NED}{2\, N_{rr}^2}\, \dfrac{A}{AC - B^2} + 1} \qquad (4.67)$$

At this minimum

$$N_{\infty}^2 = NED\left[\, \frac{1}{2A} + \frac{(A + B)^2}{2A\,(AC - B^2)}\, \frac{1}{\dfrac{NED}{2\, N_{rr}^2}\, \dfrac{A}{AC - B^2} + 1} \,\right] \qquad (4.68)$$

The analytical expressions for A-C are given in Appendix C.
The first term on the right side (1/2A) describes the noise collected during the presence of the charge signal and is independent of the reset noise level or

duration of it. It is only determined by the duration of the charge signal T_v and the cross-over frequency F_c of the 1/f noise as equation (C17) in Appendix C shows.
The second term is determined by the relative reset noise level (see equation (4.33)) and the ratio (T_{rs}/T_v) between the duration of the reset noise level and the charge signal, where T_{rs} and T_v can be found respectively in equations (C18) and equation (C19).

Case 1: Equation (4.68) reduces to the white noise solution (equation (4.32)) for the case of no DC blocking when the cross-over frequency F_c=0. Under this condition A=T_v, C=T_{rs} and B=0.

Case 2: Another case is the floating gate detection node with zero reset noise N_{rr}=0 for which the noise after filtering is given by

$$N_\infty^2 = \frac{NED}{2A} = \frac{NED}{2T_v}\frac{1}{g_1(F_cT_v)} \qquad \textbf{(4.69)}$$

The auxiliary function $g_1(y)$, defined in Appendix C, is monotonic between 0 and 1.

Case 3: For infinite reset noise N_{rr}=∞, equation (4.68) reduces to

$$N_\infty^2 = NED\,\frac{A + 2B + C}{2(AC - B^2)} =$$

$$= \frac{NED}{2T_{rs}}\,\frac{\left(1 + \frac{T_{rs}}{T_v}\right) g_1\left(F_c\left(1 + \frac{T_{rs}}{T_v}\right)\right)}{g_1(F_cT_v)g_1(F_cT_{rs}) - \frac{T_{rs}}{T_v}g_2\left(F_cT_v, \frac{Trs}{T_v}\right)^2} \qquad \textbf{(4.70)}$$

Here use has been made of the auxiliary functions defined in Appendix C.

The optimal filter for the case where the noise spectrum consists of 1/f noise and white noise cannot be build (the solution is not physical). The expression for the optimal filter is given in equation (4.52). The 1/f noise term results in a sign function (SGN(f), "List of symbols and functions") in the transfer function, which, in the time domain, is a convolution with 1/t that collects information in

the past and in the present. It is the second case that makes it impossible to physically realize the filter. Even though the filter cannot be built the result can be used for determining the noise level that could be reached after optimal filtering, and a figure of merit for this configuration can be derived.
The figure of merit, defined with equation (4.34) and applied to equation (4.70), is depicted in Figure 4.7a, where three cases are shown. One is zero reset noise (equation (4.69)), a situation encountered when using a floating gate detector. The other two are for the DC blocking case (or $N_{rr}=\infty$) with two ratios (1 and 1/2) for the timing intervals between the duration of the charge signal and the duration of the reset noise alone.
For clocking speeds more than 10 times the 1/f noise cross-over frequency the figure of merit becomes a constant and the noise performance is determined by the 'white noise' contribution. For frequencies below 10 times the cross-over frequency the behaviour is 1/f noise dominated.

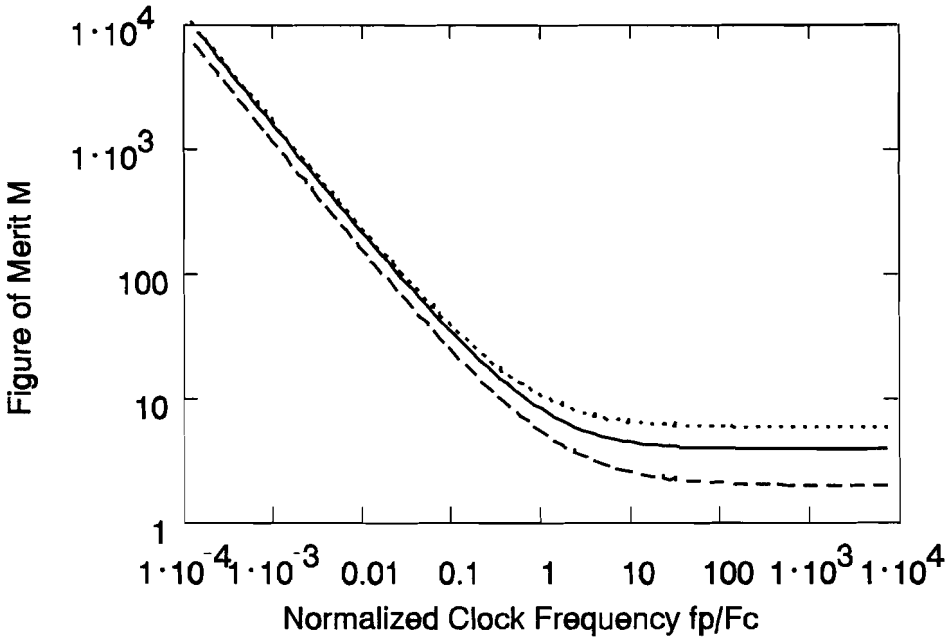

Figure 4.7a: *Figure of merit M for $T_{rs}/T_v=1$ (solid line) and $T_{rs}/T_v=1/2$ (dotted line) for the DC blocking case ($N_{rr}=\infty$) and for the second case $N_{rr}=0$ (dashed line). M is given as a function of the normalized clock frequency f_p/F_C.*

In Figure 4.7b the figure of merit M for the optimal filter is compared with the figure of merit for the two-slope integrator. For clocking frequencies above the 1/f cross-over frequency ($f_p>10\ F_C$) there is no difference in performance between the two filters. The two-slope integrator is the optimal filter for the white noise case.

It should be noted that the figure of merit M deteriorates faster for the integrator when the clocking frequency is below the 1/f cross-over frequency ($f_p<F_C/10$); it is then proportional to F_C/f_p. The optimal filter figure of merit is proportional to $F_C/[f_p \ln(f_p/F_C)]$ and so it deteriorates less quickly in an actual camera. The noise performance of the two-slope integrator becomes a constant at low pixel rates while that of the optimal filter continues to improve. The figure of merit M approaches a constant value if f_p/F_C is larger than 10. This means that for clock frequencies above 10 F_C the noise behaviour can be considered as though the noise source was white.

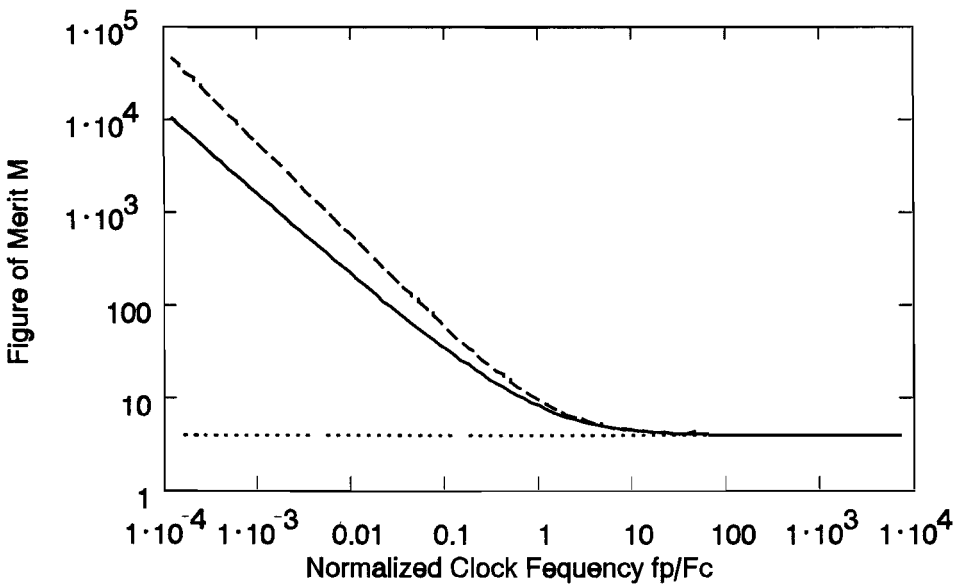

Figure 4.7b: *The figure of merit M for optimal filtering for the case of 1/f noise and thermal noise (solid line) as a function of the normalized clock frequency f_p/F_C. The result for the integrator, which is the optimal filter for the white noise case, is shown as a dashed line. The ratio between the duration of the reset level and charge signal is $T_r/T_v=1$.*

4.4 A general figure of merit

In the previous sections a figure of merit was introduced for the filter action of the optimal filter. Now a generalisation will be given to include other types of filters. The only noise term that never vanishes is the noise of the on-chip amplifier. The signal filtering should suppress the reset noise to a negligible level, leaving only the amplifier's noise. This must be taken up into the figure of merit.

The noise after a zero-order hold circuit (ZOH) can be written as

$$S_{nn}(f) = M \cdot \frac{NED}{2} \cdot sinc^2\left(\frac{f}{f_p}\right) \qquad (4.71)$$

with NED being the noise spectral density of the on-chip amplifier and M a figure of merit. The sin(x)/x noise spectrum is caused by the sample and hold.

A function that describes the frequency response is known as the Modulation Transfer Function (MTF). For the ZOH the MTF is the same sin(x)/x that shapes the noise spectrum.

Defining the figure of merit for CCD signal processing as above it is possible to obtain a practical figure for the performance of the signal processor. In a crude way the figure of merit is the ratio between the input and the output noise spectral density. This ratio is easy to measure, giving a tool to determine the performance of the signal processor one has built (Figures 4.5 and 4.7).

One also encounters filters for CCD imagers which use a combination of switched filtering and time continuous filtering. Now the shape of the noise spectral density for these filters cannot be written as a sin(x)/x relationship and the frequency response as given by the MTF is not a sin(x)/x either. This means that a general figure of merit should also include a correction for the frequency response. With the elements described above a general definition for the noise figure can be given. It includes as a limiting case the previous definition.

$$M = \frac{2}{f_p \, NED} \int_{-\frac{f_p}{2}}^{\frac{f_p}{2}} \frac{S_{nn}(f)}{MTF^2(f)} df \qquad (4.72)$$

In the above equation the noise spectral density is divided by the electrical MTF. This is a fair thing to do since limiting the bandwidth affects the signal resolution and the noise spectral density equally. The integration is done between the Nyquist limits because no useful signal reconstruction is possible outside those frequencies and because all the cosine terms in $S_{nn}(f)$ that are caused by a correlation between pixels are integrated out (Appendix A).

In general the MTF, or modulation transfer function, is a normalized transfer function that describes the way the resolution (frequency response) of a system changes with frequency. Part of the MTF is determined by the optical properties of the imaging system, such as lenses and the pixel aperture. Another part is the electrical MTF. The latter has to be taken into account when comparing types of signal filtering methods.

In the previous case with zero-order hold circuit (ZOH) the MTF is

$$MTF(f) = \left| sinc\left(\frac{f}{f_p}\right) \right| \qquad (4.73)$$

and the noise spectral density is given in equation (4.49); for the ZOH case the noise figure M defined with equation (4.72) reduces to equation (4.35).

Generally, when a noise spectrum is sampled it has the property of repeating with the sampling frequency f_p, as shown in Appendix A. Such a noise spectrum can be evaluated in a Fourier series. Substituting the series in equation (4.72) and evaluating M will leave only the auto-correlation at t=0, since all cosine terms vanish. The result is equivalent to the mean squared value of the noise $R_{nn}(0)$ after filtering. It is this quantity that has been minimized in the derivation of the optimal filter. Therefore its figure of merit is also minimal.

4.5 Clamp processing

4.5.1 The soft-clamp circuit

Clamp processing is a very simple technique. With three components one can suppress reset noise and filter some readout noise. These components are a capacitance C, a resistor R, and a MOS transistor (see Figure 4.8).

During the time that the reset FET is switched off and no charge is dumped on the floating diffusion detector the MOS transistor is conducting and fixes the output voltage of the clamp at the ground potential. The capacitance C charges towards the reset reference level with a time constant RC. The ratio between the RC-time constant and the time the MOS transistor is conducting (T_{on}) determines the amount of reset noise which is suppressed. At the same time it also determines the amount of readout noise that is clamped at the capacitance. The maximum available clamping time is $T_{on} \leq T_p - T_v$ (Figure 4.3). From this time period only a time interval with duration T_{rs} can be used for reset noise suppression.

When the charge signal arrives the MOS transistor is switched off. Now the pixel information is available at the output of the clamp with the reset noise suppressed.

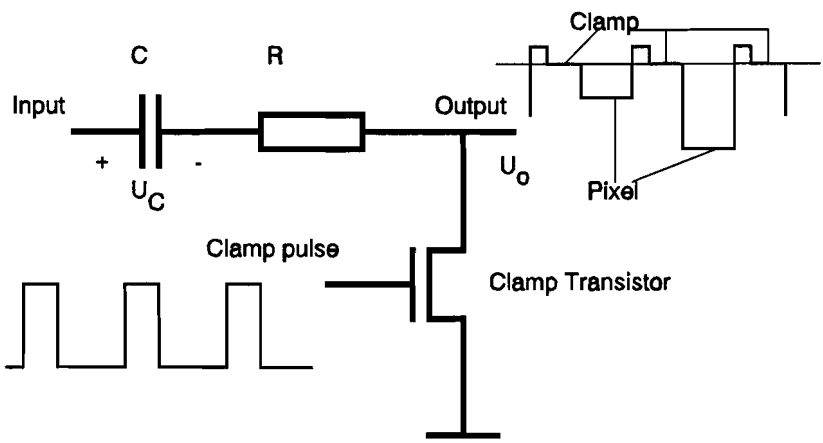

Figure 4.8: *The simplest form of signal processing: a soft-clamp.*

The voltage gain of this circuit depends on the duty cycle δ_v of the pixel signal. We define the on time of the MOS transistor as $T_{on}=T_v=\delta_v/f_p$. The MOS transistor has the additional function of windowing the charge signal.
In the following analysis only the white noise will be studied and two sided spectral densities will be used. A different approach can be found with Enz [26] who described only the effect on the readout noise, neglecting the reset noise term.

The noise at the clamp circuit output consists of:

- readout noise which is present during the time that the MOS transistor is off:
- readout noise which has been clamped at the capacitance C and lasts during the off time of the MOS transistor
- the fraction of the reset noise which is left after clamping, including the memory effect of the capacitor C.

In **Section 4.5.2** the value of the MTF is calculated which is needed in the calculation of the figure of merit defined in Section 4.4. The clamp circuit does not suppress the reset noise completely, as is shown in **Section 4.5.3**. In **Section 4.5.4** the effect of the clamp circuit on the readout noise is calculated. Finally these contributions are added together in **Section 4.5.5** to arrive at a determination of the clamp time constant and its relation to the figure of merit. **Section 4.5.6** presents experimental data to show the effect of the clock frequency and to determine the figure of merit.

4.5.2 The Modulation Transfer Function: MTF

In Section 4.4 it was shown that one has to take the modulation transfer function into account when determining the figure of merit (equation (4.72)) of a CCD signal processor. That CCD signal processor is here a clamp that is active only during the time that there is no charge signal. The clamp redefines the reference level without changing the shape of the charge signal.
In general this signal has a duty cycle of around δ_v=50%. The electrical MTF is, to a good approximation, the Fourier transform of a rectangle with duration $\delta_v \cdot T_p$

$$MTF(f) = |\, sinc(f\,\delta_v\,T_p)\,| = \left| sinc\left(\frac{f}{f_p}\,\delta_v\right)\right| \qquad (4.74)$$

where δ_v is the voltage gain.

4.5.3 The reset noise residue

During the time the clamp transistor is conducting the capacitor C charges towards the reset level, as Figure 4.8 shows. For pixel k this level is R_k. When the clamp transistor is switched off, the capacitor C has reached a level of

$$(1 - a)\, R_k \tag{4.75}$$

where

$$a = e^{-\frac{T_{rs}}{RC}} \tag{4.76}$$

In the previous cycle (k-1) the capacitor had also been charged. It is discharged in the present cycle (k). The reset noise of the (k-1) pixel has a rest value at the capacitor C of

$$(1 - a)\, a\, R_{k-1} \quad , \tag{4.77}$$

the (k-2) pixel has a reset noise rest value (at cycle k) at the capacitor C of

$$(1 - a)\, a^2\, R_{k-2} \tag{4.78}$$

and the (k-m) pixel which is m pixels before the k_{th} cycle has a reset noise rest value of

$$(1 - a)\, a^m\, R_{k-m} \tag{4.79}$$

In total the sum of the rest values at the end of cycle k is given by

$$U_{c,k} = \sum_{m=0}^{\infty} (1 - a)\, a^m\, R_{k-m} \tag{4.80}$$

The final reset noise value at the output of the clamp is

$$U_{o,k} = R_k - U_{c,k} = a\,R_k - \sum_{m=1}^{\infty} (1-a)\,a^m\,R_{k-m} \tag{4.81}$$

Using the reasonable assumption that the reset noise originates from a white noise source:

$$\langle R_i\,R_j\rangle = 0 \quad for \quad i \neq j \tag{4.82}$$

and

$$\langle R_i\,R_i\rangle = N_{rr}^2 \quad for \quad i=j \quad , \tag{4.83}$$

the mean squared sum reduces to

$$\langle U_{o,k}\,U_{o,k}\rangle = N_{rr}^2\,\frac{2\,a^2}{1+a} \tag{4.84}$$

and is independent of the cycle k.

After the clamping time period this value is held at the capacitor for the duration of the charge signal $T_v=\delta_v\,T_p$. This results in an additional sin(x)/x shaped noise spectral density which, with the use of equation (4.76), equation (4.84) and $T_{rs}=\delta_{rs}\,T_p$, yields:

$$N_{rr}^2\,2\,\frac{e^{-8\frac{B_n}{f_p}\delta_{rs}}}{1+e^{-4\frac{B_n}{f_p}\delta_{rs}}}\,\frac{\delta_v^2}{f_p}\,sinc^2\left(\frac{f}{f_p}\delta_v\right) \tag{4.85}$$

4.5.4 The clamped readout noise.

If the clamp capacitor is empty at the start of pixel k, then the noise voltage at the end of the clamp interval will reach a mean squared value (Papoulis [27]) of

$$NED \cdot B_n\,(1-a^2) \tag{4.86}$$

B_n is the noise bandwidth, which for a single pole low pass filter reads:

$$B_n = \frac{1}{4RC} \tag{4.87}$$

The reduction constant (a) is given in equation (4.76) when the readout noise spectral density equals the NED.

Just as part of the reset noise carries over between pixels (Section 4.5.3), so too does the readout noise after clamping have residual effects.
The rest value at the capacitor for the (k-1) pixel equals (equations (4.76) and (4.86))

$$NED \cdot B_n (1 - a^2) a^2 \tag{4.88}$$

and for the (k-m) th pixel

$$NED \cdot B_n (1 - a^2) a^{2m} \tag{4.89}$$

The sum over all previous pixels equals

$$\sum_{m=0}^{\infty} NED \cdot B_n (1 - a^2) a^{2m} = NED \cdot B_n \tag{4.90}$$

After the clamping time period this sum is held on the capacitor for the duration of the charge signal T_v. This results in an additional sin(x)/x shaped noise spectral density and reads:

$$NED \cdot B_n \frac{\delta_v^2}{f_p} sinc^2\left(\frac{f}{f_p}\delta_v\right) \tag{4.91}$$

4.5.5 Determination of the clamp time constant.

The noise spectral density at the output of the clamp consists of the two contributions discussed in the previous sections. A third term must also be added. The clamp acts as a window function: half of the time it passes the signal as it is and half of the time it grounds the output. Therefore the third

term is the windowed readout noise and reads

$$\frac{NED}{2}\delta_v \tag{4.92}$$

At the output of the clamp the noise consists of the total of the three mean squared noise contributions given in equations (4.85), (4.91) and (4.92). It is written as:

$$S_{nn}(f) = \frac{NED}{2}\delta_v + NED\,\frac{B_n}{f_p}\,\delta_v^2\,sinc^2\left(\frac{f}{f_p}\,\delta_v\right) + \\ +N_{rr}^2\,\frac{\delta_v^2}{f_p}\,2\,\frac{e^{-8\frac{B_n}{f_p}\delta_{rs}}}{1+e^{-4\frac{Bn}{f_p}\delta_{rs}}}\,sinc^2\left(\frac{f}{f_p}\,\delta_v\right) \tag{4.93}$$

f_p is the clamp-frequency,
δ_v is the duty cycle of the video
δ_{rs} is the duty cycle of the reset level
N_{rr} is the reset noise

The first term represents the thermal noise chopped with a square wave of duty cycle δ_v, the second term the clamp noise, and the third term the residual reset noise after clamping.

An inspection of equation (4.93) shows that a large noise bandwidth B_n (small time constant) will result in good reset noise suppression but in a large amount of readout noise that is clamped at the capacitance C. A small value for B_n (large time constant) will give a low level of clamped readout noise and a large amount of reset noise. Depending on the values for the reset noise and readout noise an optimum can be found.

The optimal value of the noise bandwidth satisfies:

$$\partial_{B_n} S_{nn}(f) = 0 \tag{4.94}$$

Unfortunately the solution for the optimal B_n cannot be given in a closed form; it is a solution of

$$X^3 8R_{rr} + X^2(4R_{rr} - 1) - 2X - 1 = 0 \tag{4.95}$$

where

$$X = e^{-4\frac{B_n}{f_p}\delta_{rs}} \tag{4.96}$$

and R_{rr} is the same normalized reset noise as in equation (4.33)

$$R_{rr} = \frac{2\,T_{rs}\,N_{rr}^2}{NED} \tag{4.97}$$

Only when $R_{rr}>1/3$ is there a physical solution for X_{opt}, whose value will be between 0 and 1. This means that no optimum exists for reset noise values that are too small.

Substituting equation (4.93) in the noise figure M, which is defined in equation (4.72), and using equation (4.74), the noise figure for the clamp circuit is found to be

$$M_{clamp} = \frac{1}{f_p}\int_{-\frac{f_p}{2}}^{\frac{f_p}{2}} \frac{1}{\delta_v}\,\frac{1}{sinc^2\left(\frac{f}{f_p}\delta_v\right)}\,df + \tag{4.98}$$

$$+ 2\,\frac{B_n}{f_p} + \frac{N_{rr}^2\,4}{f_p\,NED}\,\frac{e^{-8\frac{B_n}{f_p}\delta_{rs}}}{1+e^{-4\frac{B_n}{f_p}\delta_{rs}}}$$

or, after the evaluation of the integral and using equation (4.96),

$$M_{clamp} = 2.148 - \frac{\ln(X_{opt})}{2\,\delta_{rs}} + \frac{2R_{rr}}{\delta_{rs}}\,\frac{X_{opt}^2}{1 + X_{opt}} \tag{4.99}$$

where X_{opt} is the solution of equation (4.95).

Given a duty cycle of the reset-hold level of δ_{rs}=1/3, a reset noise level of N_{rr}=40 e, a spectral density of the on-chip amplifier NED=6 e^2/MHz and a clock frequency of f_p=36 MHz the time constant of the clamp circuit is RC=6.3 ns or 1.48 τ.

In the next table the figure of merit is calculated for the soft clamp (M_{clamp}) and compared to the value for optimal filtering (M_{opt}). This is done for several different clock frequencies (f_p). In the table the optimal value for the RC time constant is given by (T_{rs}/RC).
For these calculations the duty cycle of the reset-hold level is taken as δ_{rs}=1/3 and for the charge signal δ_v=1/2. The reset noise is equivalent to 40 e and the noise of the on-chip amplifier is 6 e^2/MHz.

NED=6 e^2/MHz; N_{rr}=40 e; δ_{rs}=1/3; δ_v=1/2				
f_p [MHz]	R_{rr}	M_{clamp}	T_{rs}/RC	M_{opt}
72	2.5	5.03	1.12	4.14
36	5.0	5.63	1.48	4.50
18	10	6.22	1.84	4.72
9	20	6.79	2.19	4.86
4.5	40	7.35	2.54	4.93

At higher clock frequencies M_{clamp} (third column) tends towards the optimal M_{opt} (fifth column). The reason for this is that the readout noise collected during the reset-hold time from the on-chip amplifier is larger than the reset noise, so the reset noise becomes relatively less important. The weighting coefficients for the reset-hold level may then be smaller.
Figure 4.9 shows the relation between the normalized reset noise and the figure of merit for the soft clamp circuit and for the optimal situation. The figure of merit is for the white noise case only.
Especially for low readout frequencies (large values for the normalized reset noise R_{rr}) the difference between optimal and clamp becomes rather large.

4.5.6 Experimental data of the soft clamp.

Figure 4.10 shows the experimental data for a clamp circuit that has been optimized for a clock frequency of 18 MHz. The clamp circuit is used at two clock frequencies, 1 MHz and 6 MHz. The solid lines are based on equation (4.93) which predicts that the expected shape for the noise spectral density is sin(x)/x. The figure of merit for the two cases is M=91 and M=16.5 showing that the design is far from being optimal. For 18 MHz the figure of merit is M=8.3. The measurements are performed on a test chip with the same parameters as given in the previous table.

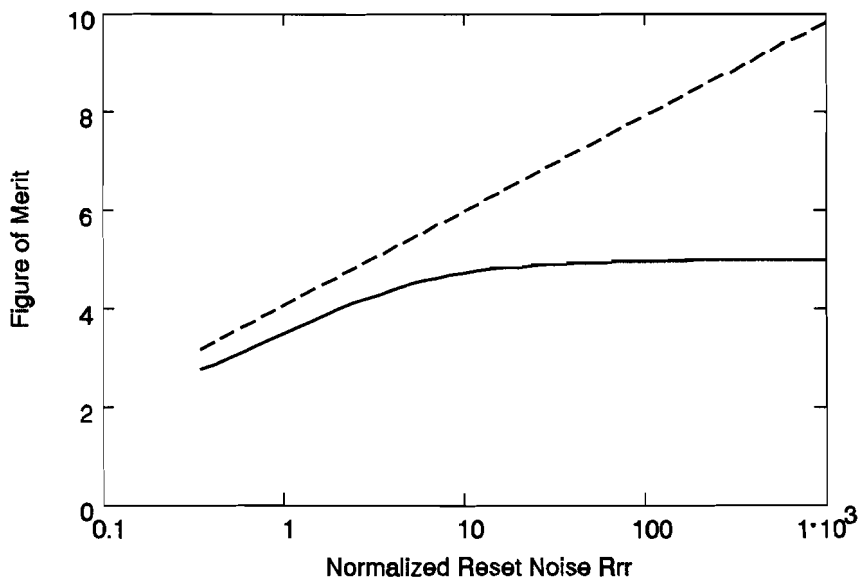

Figure 4.9: *Figure of merit for clamp processing (dashed line) and the optimal value (solid line) for the two-slope integrator.*

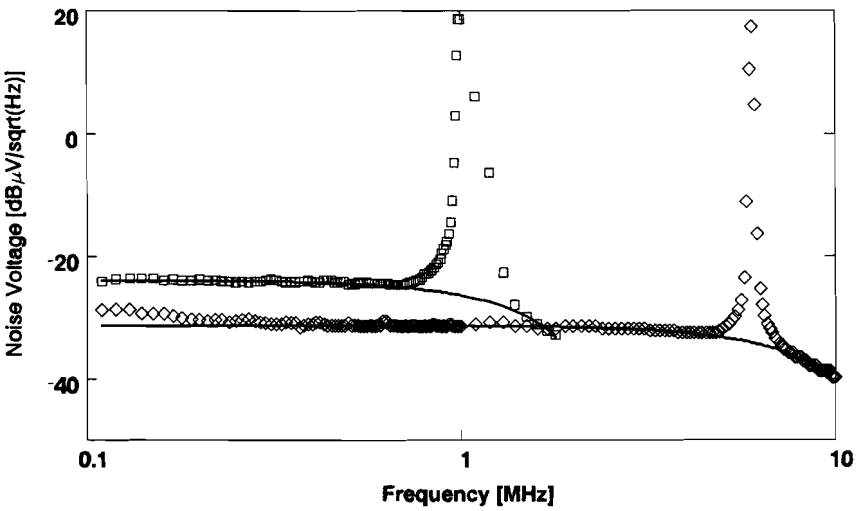

Figure 4.10: Experimental data for the noise voltage of a clamp circuit for a clock frequency of 1 MHz (□) and a clock frequency of 6 MHz (◊).

4.6 The passive integrator

4.6.1 Transfer function of the passive integrator circuit

One disadvantage of an ordinary sampler or clamp circuit consisting of a MOS transistor switch and a capacitor is that it reaches its final value after an infinite time. By adding an inductor with a parallel resistor (Figure 4.11) a second order circuit is obtained (Buul and Centen [28]). Exciting this circuit with a step impulse will cause the voltage swing across the capacitor C to oscillate around its final value. The voltage swing equals the input voltage at several moments in time. Reaching the final value in a given time interval T_x implies that full reset noise suppression is possible. It does not necessarily mean that a good noise figure of merit can be reached. In this section the figure of merit for this circuit will be calculated and minimized after which it will be compared with the theoretical lower bound for the two-slope integrator.

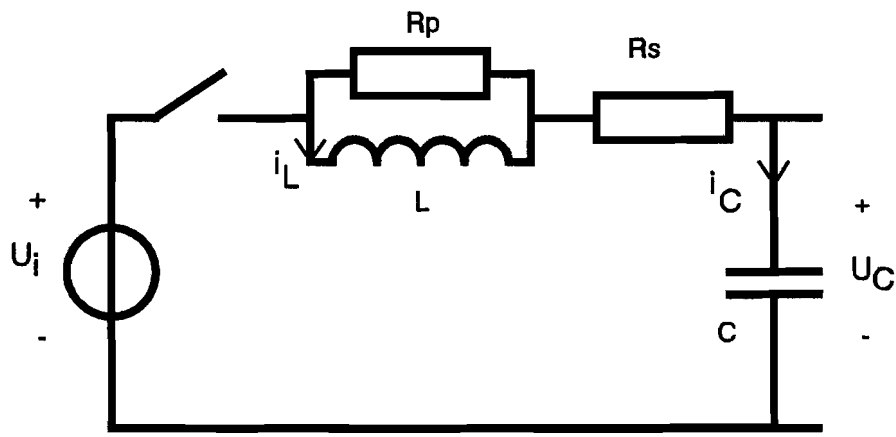

Figure 4.11: A passive integrator through the addition of a coil L and a resistor R_p.

The transfer function of the circuit given in Figure 4.11 is

$$H(s) = \frac{s\frac{L}{R_p} + 1}{s^2 L C\left(1 + \frac{R_s}{R_p}\right) + s\left(C R_s + \frac{L}{R_p}\right) + 1} \qquad \textbf{(4.100)}$$

The unit step response can be written as (Appendix D)

$$U_c(t) = 1 + e^{-at}\left(\frac{a^2+b^2-ad}{bd}\sin(bt) - \cos(bt)\right) \qquad \textbf{(4.101)}$$

and the condition for reaching the final value at a finite time T_x reads

$$\tan(bT_x) = \frac{bd}{a^2+b^2-ad} \tag{4.102}$$

In the above use was made of the definition

$$U_c(\ t = T_x\ ) = 1$$

The constants (a), (b) and (d) are defined in Appendix D, equation (D3).

Next we have to derive the noise bandwidth.

4.6.2 The noise bandwidth of the passive integrator circuit

The noise bandwidth of the transfer function H(ω) given in equation (4.100) is

$$2\ B_n = \frac{1}{2\pi}\int_{-\infty}^{\infty} H(\omega)\ H^*(\omega)\ d\omega \tag{4.104}$$

The integrand of the above equation has two poles in the upper half of the complex plane.

$$H(\omega)\ H^*(\omega) =$$

$$= \frac{j\omega + d}{(j\omega+a+jb)(j\omega+a-jb)}\ \frac{-j\omega+d}{(-j\omega+a-jb)(-j\omega+a+jb)}\left(\frac{a^2+b^2}{d}\right)^2 \tag{4.105}$$

Using the residue theorem from complex function theory, integrating along the closed Jordan curve C consisting of a segment along the ω-axis from -ρ to ρ and a semicircular arc connecting ρ and -ρ through the upper half-plane gives

$$\int_{-\infty}^{\infty} H(\omega)\ H^*(\omega)\ d\omega = \oint H(\omega)\ H^*(\omega)\ d\omega \tag{4.106}$$

The integrand has two poles within the closed curve C.

Calculating the residues reveals the following results

$$\oint H(\omega)\ H^*(\omega) d\omega = 2\pi j(\ Res_1 + Res_2\ ) =$$

$$2\pi j \lim_{\omega \to ja-b} [(\omega - ja+b)\ H(\omega)\ H^*(\omega)] + \qquad (4.107)$$

$$+ 2\pi j \lim_{\omega \to ja+b} [(\omega - ja-b)\ H(\omega)\ H^*(\omega)]$$

The contribution along the semicircular arc in the limit of ρ going to infinity is zero.

The two residues are

$$Res_1 = \frac{(ja-b-jd)(ja-b+jd)}{(ja-b-ja-b)(ja-b+ja+b)(ja-b+ja-b)} \left(\frac{a^2+b^2}{d}\right)^2 =$$

$$= \frac{(ja-b)^2+d^2}{-8jab(ja-b)} \left(\frac{a^2+b^2}{d}\right)^2 \qquad (4.108)$$

and

$$Res_2 = \frac{(ja+b-jd)(ja+b+jd)}{(ja+b-ja+b)(ja+b+ja+b)(ja+b+ja-b)} \left(\frac{a^2+b^2}{d}\right)^2 =$$

$$= \frac{(ja+b)^2+d^2}{8jab(ja+b)} \left(\frac{a^2+b^2}{d}\right)^2 \qquad (4.109)$$

These are added to obtain the right hand side of equation (4.107)

$$\oint H(\omega)\, H^*(\omega)\, d\omega =$$

$$= 2\pi j(Res_1 + Res_2) = \frac{2\pi}{4a}\left(1+\frac{d^2}{a^2+b^2}\right)\left(\frac{a^2+b^2}{d}\right)^2 \tag{4.110}$$

Under substitution of the above equation applying equation (4.104) the noise bandwidth (B_n) is finally obtained after using equation (4.106)

$$B_n = \frac{a^2+b^2}{8a}\left(1+\frac{a^2+b^2}{d^2}\right) \tag{4.111}$$

After substitution of the known parameters (a), (b) and (d) given in equation (D3) the noise bandwidth becomes

$$B_n = \frac{\frac{L}{R_p} + C(R_s+R_p)}{4C(R_s+R_p)\left(\frac{L}{R_p}+R_sC\right)} \tag{4.112}$$

For R_p=0 the above reduces to the well known equation 1/(4 R_s C) for the noise bandwidth of a single RC-network.

This finalizes the derivation of the step response (Section 4.6.1) and the noise bandwidth (Section 4.6.2), expressed in the time constants of the sampler circuit. In the next section these two values are optimized.

4.6.3 Optimizing the passive integrator circuit

The problem which needs to be solved now is to find the parameters (a), (b) and (d) such that the following condition is fulfilled:

$$\begin{aligned} &\min \quad B_n(a,b,d) \\ &with \quad U_c\,(a,b,d,\,T_x\,) = 1 \end{aligned} \tag{4.113}$$

The solution to this problem involves equation (4.102) and equation (4.112), and reads:

$a=1.4181/T_x$
$b=1.8986/T_x$
$d=7.2713/T_x$

Expressed in the time constants (equation D3) of the circuit

$$\frac{L}{R_p} = 0.1375\ T_x$$
$$R_s\ C = 0.3675\ T_x \qquad (4.114)$$
$$R_p\ C = 0.9273\ T_x$$

With these values the noise bandwidth B_n of equation (4.112) becomes

$$B_n = \frac{0.5476}{T_x} \qquad (4.115)$$

Note that for an ideal integrator the noise bandwidth would be $0.5/T_x$ (Appendix B). The departure from the ideal case is only 0.395 dB. This is a remarkably good result. The value for the time interval T_x must be $T_x=T_{rs}$ when sampling the reset-hold level and $T_x=T_v$ when sampling the charge signal (see Figure 4.3).

4.6.4 Inter-Symbol Interference (ISI)

The circuit of Figure 4.11 has two elements with 'memory', a capacitor and an inductor. As such it can cause inter-symbol interference, better known as 'pixel smearing' and pixel cross-talk. The purpose of this section is to analyze the amount of 'pixel smearing' due to the memory effect of the capacitor and the inductor. The switch in Figure 4.11 is closed during the time $T_x=T_p/2$ and open during an equal time T_x. Equation (4.102) gives T_x and indirectly the minimum pixel period for the integrator.

Due to the choice of time constants the voltage across the capacitor C reaches its final value at $t=T_x$. At that time the switched is opened and a new voltage level is fixed. The current that is still flowing through the coil L will decease in this second interval with a time constant L/R_p. This current will give rise to an output voltage at the capacitor in the second pixel.

The Laplace transform for a (step) input voltage U to the coil current I is

$$I = U \frac{sC}{s^2LC(1+\frac{R_s}{R_p}) + s(\frac{L}{R_p}+R_sC) + 1} \tag{4.116}$$

Its solution in the time domain reads

$$i_L(t) = e^{-at}(\alpha\cos(bt) + \beta\sin(bt)) \tag{4.117}$$

with boundary conditions

$$\begin{aligned} i_L(0^+) &= 0 \\ \partial_t\, i_L\,(0^+) &= \frac{U}{L}\frac{R_p}{R_s+R_p} \end{aligned} \tag{4.118}$$

Solving equation (4.117) with (4.118), the current through the coil after a time T_x is given by

$$i_L(t=T_x) = \frac{U}{bL}\,\frac{R_p}{R_p+R_s}\,e^{-aT}\sin(bT_x) \tag{4.119}$$

The energy in the coil will be dissipated in the resistor R_p during the second time interval, again with duration T_x. The switch is now open and the current is further reduced by

$$e^{-T_x\frac{R_p}{L}} \tag{4.120}$$

During the third interval with duration T_x, when the switch is closed, the only excitation of this network is the rest current flowing in the coil.
It generates a current through the capacitor

$$i_C(t) = i_L(t) + \frac{R_s}{R_p}\,L\,\partial_t i_L \tag{4.121}$$

Therefore the voltage across the capacitor due to the memory effect is

$$U_C(t) = \frac{1}{C}\int_0^t i_L dt + \frac{1}{C}\frac{L}{R_p} i_L(t) + U_C(0^+) - \frac{L}{CR_p} i_L(0^+) \qquad (4.122)$$

where the memory effect is expressed in terms of a boundary condition at $t=0^+$. Solving $U_C(t)$, the ratio of the residual value of the previous pixel ($U_C(0^+)$ and $i_L(0^+)$) to the present pixel is given by

$$residu = \frac{U_C(bT_x)}{U_C(0^+)} = \frac{1}{bC(R_p+R_s)} e^{-aT_x} e^{-T_x\frac{R_p}{L}} \sin(bT_x) \qquad (4.123)$$

The inter-symbol interference (ISI) for the passive integrator can now be calculated with the constants a, b and c given in equations (D3) and (4.118).

$$ISI = e^{-aT_x} e^{-dT_x} \sin(bT_x) \frac{a^2+b^2}{bd} = \qquad (4.124)$$

$$ISI = 6.48\,10^{-5}$$

This amounts to -83.8 dB.

This result shows that when the sampler circuit given in Figure 4.11 is switched periodically and a single pixel excitation is applied, then the next pixel contains only -84 dB of the original signal due to the memory effect of the circuit. Therefore, practically no smearing of pixel information occurs.

4.6.5 Conclusion

The addition of a coil and a resistor makes it possible to create a passive integrator circuit which has a noise bandwidth which is only 0.4 dB worse than an ideal integrator. It has an inter-symbol interference whose value of -84 dB is negligible in practical situations. Its performance for white noise is close to the theoretical limit as given in Appendix B.

This circuit can replace the soft clamp depicted in Figure 4.8. It can also be used as a replacement for the first stages of a CDS (Section 4.7) to obtain nearly optimal performance.

4.7 Correlated Double Sampler (CDS)

Again the analysis is performed for the white noise case only since the 1/f noise cross-over frequency lies well below the clocking frequency in most present day applications. Kansy [29] calculated the response of the CDS for clocking frequencies well below this frequency.

In CDS the reset reference level is sampled and subtracted from the sampled value of the charge signal which also contains the reset noise level. Figure 4.12 gives a practical implementation of a correlated double sampler. The first sample and hold (S&H1) samples the reset-hold level and the second sampler (S&H2) samples the charge signal level (see Figure 4.3). The other sample and holds (S&H3,4,5) are used to reduce clock cross-talk caused during the sample and hold phases. Two clocks are used; one is the reset-hold clock and the other is the charge signal clock. In some applications both clocks have a duty cycle of 25%.

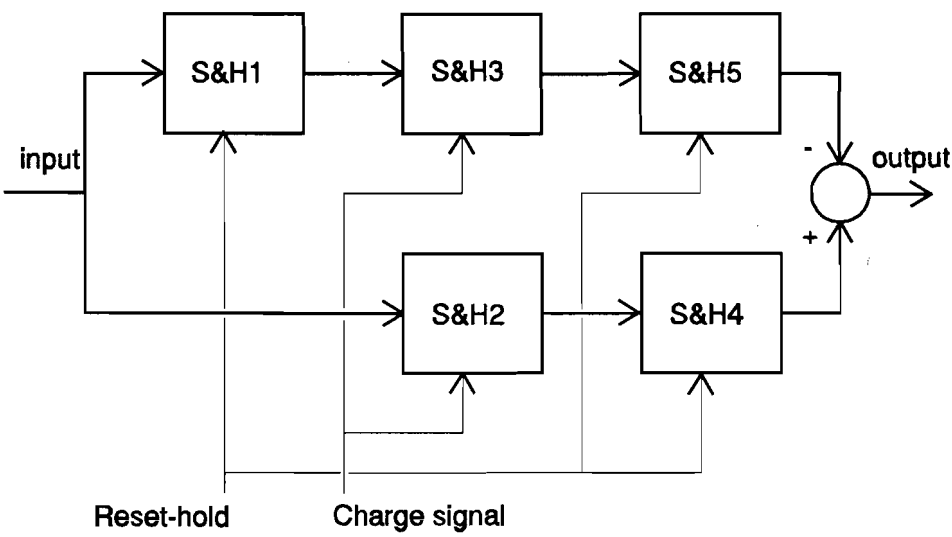

Figure 4.12: A practical implementation of a Correlated Double Sampler circuit.

In the following it is assumed that the samplers have an equal noise bandwidth

of B_n. The bandwidth is large enough to enable reset noise suppression. The noise due to sampling becomes

$$N_\infty^2 = NED\ B_n + NEDB_n = 2\ NED\ B_n \tag{4.125}$$

so the noise figure M from equation (4.34) is given by

$$M = \frac{4\ B_n}{f_p} \tag{4.126}$$

The noise spectral density is, following equation (4.49),

$$S_{nn}(f) = M \cdot \frac{NED}{2} \cdot sinc^2\left(\frac{f}{f_p}\right) \tag{4.127}$$

The figure of merit of a commercial available CDS, the Sony CXA1439A, is M=30 at f_p=10 MHz. The maximum operating frequency according to the specification is f_p=25 MHz. Therefore one can expect the figure of merit to improve to M=12 when used at the higher clock frequency. In comparison a figure of merit of M=5 can be reached with a matched filter. The timing for this CDS was $T_{rs}=T_p/3$ and $T_v=T_p/2$.
The reason for these poor values for the figure of merit stems from the high noise bandwidth of the sample and hold sections.

The figure of merit of the TDA8786, a CDS from Philips, is still worse due to its much larger noise bandwidth. Its M is 44 at a clock frequency of f_p=10 MHz. Its maximum clock frequency is also f_p=25 MHz and the figure of merit is expected to drop to M=18 at that frequency. This value is still large since M=5 is the lower bound given by the matched filter approach.

A major problem with CDS is the compromise between the noise performance determined by the noise bandwidth and the Inter-Symbol Interference which is also determined by the noise bandwidth. These are inversely related, so that a higher noise bandwidth tends to a better Inter-Symbol Interference but a worse noise performance, and vice versa.

4.8 Conclusion

In this chapter the optimal filter, also known as the matched filter, is derived using variational calculus. Based on the optimal filter a figure of merit is defined that describes the noise performance of a CCD signal processor in general.
For the figure of merit a lower bound has been derived. This lower bound is a powerful tool to determine the performance of a CCD signal processor practically.

It has been shown that the overall noise performance of a CCD imaging chain can be expressed as the product of the noise electron density of the CCD imager, the figure of merit of the CCD signal processor, and the bandwidth which is determined by the application. By separating the noise sources in the above elements one can separately optimize the noise performance of the CCD imager and the signal processor.

Furthermore it has been shown that for clock frequencies beyond ten times the cross-over frequency of the 1/f noise ($f_p > F_c \cdot 10$) the noise performance after filtering is determined by only thermal noise. In these cases it is sufficient to optimize for only thermal noise.

For three types of CCD signal processors the figure of merit has been determined and dimensioning criteria have been established. The first type is the simplest of CCD signal processors, the second has a noise performance that is very close to optimum, and the third is the classical Correlated Double Sampler.

Appendix A: The noise spectral density after sampling

A signal with a spectral density $S_{vv}(f)$ is sampled periodically with a sample frequency f_p. The Fourier spectrum of the sampled signal is a periodic function in the sample frequency f_p. This property is very useful in approximating the noise spectral density of a sampled system. In the remainder of this section this property will be derived.

Given the following Fourier transform pair for the autocorrelation function

$$R_{vv}(\tau) \leftrightarrow S_{vv}(f) \tag{A1}$$

now the sampled function and its Fourier transform will be

$$\sum_{k=-\infty}^{k=\infty} R_{vv}(\tau)\,\delta(\tau - kT_p) \leftrightarrow \sum_{k=-\infty}^{\infty} R_{vv}(kT_p)e^{-j2\pi fkT_p} \tag{A2}$$

The right hand side of the above equation, which is the power spectrum of the sampled auto correlation function, can be written as

$$R_{vv}(0) + 2\sum_{k=1}^{\infty} R_{vv}(kT_p)\cos(2\pi fkT_p) \tag{A3}$$

where

$$R_{vv}(0) = \int_{-\infty}^{\infty} S_{vv}(f)\,df \tag{A4}$$

is the variance of the noise signal.
In many cases the first term of equation (A3) is sufficient to describe the energy spectrum of the sampled auto-correlation function. Especially when the decay is exponential and higher order terms disappear, $R_{vv}(2\,T_p)=R_{vv}(T_p)^2$.

The output of a sampler circuit is usually passed through a zero-order hold circuit (ZOH).

The impulse response of such a circuit is

$$RECT\left(\frac{t}{T_p}\right) \tag{A5}$$

and its transfer function, which is the Fourier transform of the above, is a sin(x)/x

$$\frac{1}{f_p} Sinc\left(\frac{f}{f_p}\right) \tag{A6}$$

Assuming that the noise after sampling passes a zero order hold (ZOH) the noise spectral density is approximately

$$S_{zoh}(f) = \left(R_{vv}(0) + 2\sum_{k=1}^{k=\infty} R_{vv}(kT_p)\cos(2\pi fkT_p)\right)\frac{1}{f_p}\,sinc^2\left(\frac{f}{f_p}\right) \tag{A7}$$

$$S_{zoh}(f) \approx R_{vv}(0)\,\frac{1}{f_p}\,sinc^2\left(\frac{f}{f_p}\right)$$

Generally, when the ZOH has a duty cycle of δ then the noise energy is

$$\int_{-\infty}^{\infty}\left(R_{vv}(0) + 2\sum_{k=1}^{\infty} R_{vv}(kT_p)\cos(2\pi fkT_p)\right)\frac{\delta^2}{f_p}\,sinc^2\left(\frac{f}{f_p}\,\delta\right)df = \delta R_{vv}(0) \tag{A8}$$

In the above use has been made of

$$\delta\ T_p \int_{-\infty}^{\infty} \cos(2\pi f k T_p)\ sinc^2(f T_p \delta)\, df$$

$$= \frac{\left[\Delta\left(\frac{k T_p}{\delta T_p}\right) + \Delta\left(\frac{-k T_p}{\delta T_p}\right)\right]}{2} = \tag{A9}$$

$$= 1 \quad for\ k = 0$$

$$= 0 \quad for\ k \neq 0$$

Appendix B: The noise bandwidth of an integrator.

An integrator that integrates the input voltage during a time T_x and that normalizes the output voltage with T_x has unity gain for a step input. The mean squared of the noise voltage at the output of such an integrator is

$$<U(t)\ U(t)> = <\frac{1}{T_x}\int_{t-T_x}^{t} U_i(t_1)\ dt_1\ \frac{1}{T_x}\int_{t-T_x}^{t} U_i(t_2)\ dt_2> \qquad \textbf{(B1)}$$

$$<U(t)\ U(t)> = \frac{1}{T_x^2}\int_{t-T_x}^{t}\int_{t-T_x}^{t} <U_i(t_1)\ U_i(t_2)>\ dt_1\ dt_2$$

The input spectral density when the source is white is

$$<U(t_1)\ U(t_2)> = \frac{\eta}{2}\ \delta(t_1 - t_2) \qquad \textbf{(B2)}$$

After substituting equation (B2) into equation (B1), the mean squared voltage equals

$$\frac{1}{T_x^2}\int_{t-T_x}^{t}\int_{t-T_x}^{t}\frac{\eta}{2}\ \delta(t_1 - t_2)\ dt_1\ dt_2 = \frac{\eta}{2\ T_x} \qquad \textbf{(B3)}$$

At the same time the mean squared voltage can be written as the product of the noise spectral density and the noise bandwidth B_n

$$\eta\ B_n \qquad \textbf{(B4)}$$

Equating equations (B3) and (B4) gives the noise bandwidth of an integrator,

$$B_n = \frac{1}{2T_x} \qquad \textbf{(B5)}$$

Appendix C: Some auxiliary functions.

The auxiliary functions can be evaluated using the standard cosine (Ci(x)) and sine (Si(x)) integrals and can be found in Abramowitz and Stegun [30]. A useful function can be defined as

$$g(x) = -Ci(x)\ Cos(x) - \left(Si(x) - \frac{\pi}{2} \right) Sin(x) \qquad \text{(C1)}$$

For x>>1 the above reduces to

$$g(x) \approx \frac{1}{x^2} \qquad \text{(C2)}$$

and for x<<1 to

$$g(x) \approx -\gamma_e - \ln(x) + \frac{\pi}{2} x \qquad \text{(C3)}$$

where Eulers constant γ_e is given by

$$\gamma_e = 0.57721 \qquad \text{(C4)}$$

With the above preliminaries the evaluation of the first auxiliary function $g_1(y)$ is as follows

$$g_1(y) = 2 \int_0^\infty \frac{x}{x+y}\ sinc^2(x)\ dx \qquad \text{(C5)}$$

Changing variable $t=\pi x$ yields

$$g_1(y) = 2 \int_0^\infty \frac{\sin^2(\pi x)}{\pi^2 x\ (x+y)}\ dx = \frac{2}{\pi} \int_0^\infty \frac{\sin^2(t)}{t\ (t+\pi y)}\ dt \qquad \text{(C6)}$$

Using $2 \sin^2(t)=1-\cos(2t)$ we have

$$g_1(y) = \frac{1}{\pi^2 y} \int_0^\infty \frac{1 - \cos(2t)}{t} - \frac{1 - \cos(2t)}{t+\pi y}\, dt \qquad \text{(C7)}$$

This integral reduces to

$$g_1(y) = \frac{\gamma_e + \ln(2\ \pi\ y) + g(2\ \pi\ y)}{\pi^2\ y} \qquad \text{(C8)}$$

For y>>1

$$g_1(y) \approx \frac{\gamma_e + \ln(2\,\pi\, y)}{\pi^2 y} \qquad \text{(C9)}$$

and for y<<1

$$g_1(y) \approx 1 \qquad \text{(C10)}$$

The second auxiliary function $g_2(y,\rho)$ is defined as

$$g_2(y,\rho) = 2 \int_0^\infty \frac{x}{x+y} sinc(x)\ sinc(x\ \rho)\ \cos(\pi\ x\ (1+\rho))\ dx \qquad \text{(C11)}$$

From trigonometry this can be written as

$$g_2(y,\rho) = \int_0^\infty \frac{\cos(\pi x(1-\rho)) - \cos(\pi x(1+\rho))}{\pi^2 x \rho (x+y)} \cos(\pi x(1+\rho))\ dx \qquad \text{(C12)}$$

and can be reduced further to

$$g_2(y,\rho) = \int_0^\infty \frac{\sin^2(\pi x(1+\rho)) - \sin^2(\pi x \rho) - \sin^2(\pi x)}{\pi^2 \rho x (x+y)} dx \qquad \text{(C13)}$$

Using the auxiliary function $g_1(y)$

$$g_2(y,\rho) = \frac{(1+\rho)\, g_1((1+\rho)y) - g_1(y) - \rho g_1(\rho y)}{2\rho} \qquad \textbf{(C14)}$$

For y>>1

$$g_2(y) \approx -\frac{\gamma_e + \ln(2\pi y \frac{\rho}{1+\rho})}{\pi^2 y} \approx -\frac{\ln(y)}{\pi^2 y} \qquad \textbf{(C15)}$$

For y<<1

$$g_2(y,\rho) \approx 0 \qquad \textbf{(C16)}$$

The three parameters A, B and C are defined and given analytically with the help of the above auxiliary functions.

Parameter A reads

$$A = \int_{-\infty}^{\infty} \frac{G_v^*(f)\, G_v(f)}{S_{ee}(f)}\, df$$

$$A = T_v^2 \int_{-\infty}^{\infty} \frac{sinc^2(f\, T_v)}{1 + \left|\frac{F_c}{f}\right|}\, df = T_v\, g_1(F_c\, T_v) \quad . \qquad \textbf{(C17)}$$

Parameter B is

$$B = \int_{-\infty}^{\infty} \frac{G_{rs}^{*}(f)\, G_{v}(f)}{S_{ee}(f)}\, df$$

$$B = T_v\, T_{rs} \int_{-\infty}^{\infty} \frac{sinc(f\, T_v)\; sinc(f\, T_{rs})\; e^{-j\,\pi\, f\,(T_v+T_{rs})}}{1 + \left|\frac{F_c}{f}\right|}\, df \qquad \textbf{(C18)}$$

$$B = T_{rs} g_2(F_c T_v, \frac{T_{rs}}{T_v})$$

(note that B is real)
and parameter C is

$$C = T_{rs}^2 \int_{-\infty}^{\infty} \frac{sinc^2(f\, T_{rs})}{1 + \left|\frac{F_c}{f}\right|}\, df = T_{rs}\, g_1(F_c T_{rs}) \quad . \qquad \textbf{(C19)}$$

Appendix D: Step response of the LCR-circuit.

The Laplace transform of the relation between the output and input voltages of the circuit depicted in Figure 4.11 is given by equation (4.100).

$$H(s) = \frac{s\frac{L}{R_p} + 1}{s^2 L C\left(1 + \frac{R_s}{R_p}\right) + s\left(C R_s + \frac{L}{R_p}\right) + 1} \qquad \textbf{(D1)}$$

It can be written as

$$H(s) = \frac{s + d}{(s + a)^2 + b^2}\,\frac{a^2 + b^2}{d} \qquad \textbf{(D2)}$$

where the constants (a), (b) and (d) expressed in the time constants of the circuit in Figure 4.11 are

$$d = \frac{R_p}{L}$$

$$a^2 + b^2 = \frac{R_p}{LC(R_s + R_p)}$$

$$a = \frac{\frac{L}{R_p} + R_s C}{2\frac{L}{R_p}C(R_s + R_p)} \qquad \textbf{(D3)}$$

$$b = \frac{\sqrt{4\frac{L}{R_p}C(R_s + R_p) - \left(\frac{L}{R_p} + R_s C\right)^2}}{\left(2\frac{L}{R_p}C(R_s + R_p)\right)}$$

and where the step response is

$$\frac{H(s)}{s} \tag{D4}$$

Breaking up the above into partial fractions we have

$$\frac{H(s)}{s} = \frac{A}{s} + \frac{B}{s+a+jb} + \frac{C}{s+a-jb} \tag{D5}$$

The constants A, B and C are defined through

$$\begin{aligned} &A\ (s^2+2as+a^2+b^2) + B\ s\ (s+a+jb) + C\ s\ (s+a-jb) \\ &\equiv (s + d)\ \frac{a^2+b^2}{d} \end{aligned} \tag{D6}$$

Collecting all the terms in powers of s^n we finally obtain

$$\begin{aligned} &s^2\ [A+B+C] + s\ [2aA+aB+aC-jbB+jbC] + A(a^2+b^2) \\ &\equiv (s+d)\frac{a^2+b^2}{d} \end{aligned} \tag{D7}$$

Since this must be valid for all values of s the following must hold

$$\begin{aligned} &A+B+C=0 \\ &2aA+a(B+C)+jb(C-B)=\frac{a^2+b^2}{d} \\ &A(a^2+b^2)=a^2+b^2 \end{aligned} \tag{D8}$$

the solution for this set of three equations with three unknowns is

$$A = 1 \tag{D9}$$

(C is the conjugate of B)

$$C = B^* \tag{D10}$$

$$Re(B) = -\frac{1}{2} \tag{D11}$$

$$Im(B) = \frac{a^2+b^2-ad}{2b} \tag{D12}$$

After substituting (D9)-(D12) and inverse Laplace transformation of (D4), one finds the response to a unit step for t>0

$$U_c(t) = 1 + e^{-at}\left(\frac{a^2+b^2-ad}{bd} \sin(bt) - \cos(bt) \right) \tag{D13}$$

If the circuit reaches its final value at finite time T_x, then ($U_C(t=T_x)=1$). This implies

$$\tan(bT_x) = \frac{bd}{a^2+b^2-ad} \tag{D14}$$

References

[1] M.White, D.Lampe, F.Blaha, I.Mack, *"Characterization of Surface Channel CCD Image Arrays at Low Light Levels"*, IEEE Journal of Solid-State Circuits, vol. SC-9, No. 1, February 1974, pp 1-13.

[2] D.Hegyi and A.Burrows, *"Optimal sampling of charge-coupled devices"*, Astronomical Journal, Vol.85, No. 10, pp 1421-1424, Oct. 1980

[3] G.Hopkinson and D.Lumb, *"Noise reduction techniques for CCD image sensors"*, J. Phys. E: Sci. Instrumm., Vol. 15, 1982, pp 1214-1222.

[4] P.Levine, *"Low-Noise CCD Signal Recovery"*. IEEE Trans. Electron Devices, vol. ED-32, no. 8, pp. 1534-1537, Aug. 1985.

[5] W.Buttler, B.Hosticka and G.Lutz, *"Noise Filtering for Readout Electronics"*, Nuclear Instruments and Methods in Physics Research, A288 (1990), pp 187-190

[6] J.Hynecek, *"High-Resolution 8-mm CCD Image Sensor with Correlated Clamp Sample and Hold Charge Detection Circuit."* IEEE Trans. Electron Devices, vol. ED-33, no. 6, pp. 850-862, June 1986.

[7] M.Ohbo, I.Akiyama, T.Tanaka, *"A new suppression method for high-definition CCD cameras"*. IEEE Trans. on consumer electronics, Vol. 35, No. 3, August 1989, pp. 368-374.

[8] P.Centen, *"CCD signal processing for better signal-to-noise ratio"*, May 1988, Internal report Philips.

[9] H.Wey and W.Guggenbühl, *"An improved Correlated Double Sampling Circuit for low Noise Charge-Coupled Devices"*, IEEE Transactions on Circuits and Systems, Vol. 37, No. 12, december 1990, pp 1559-1565.

[10] T.McCurnin, L.Schooley, G.Sims. *"Charge-coupled device signal processing models and comparisons"*. Journal of Electronic Imaging, vol 2(2), pp. 100-107, April 1993.

[11] P.Centen. *"Noise Optimisation of CCD on-chip amplifiers"*. 17th International Television Symposium Montreux, pp.466-496, June 1991.

[12] A.Theuwissen. *"Solid-State Imaging with Charge-Coupled Devices"*. Kluwer Academic Publishers 1995; ISBN 0-7923-3456-6.

[13] J.Carnes, W.Kosonocky, *"Noise sources in Charge-Coupled Devices"*, RCA Rev. 33, pp.327-343; 1972.

[14] N.Teranishi, N.Mutoh, *"Partition Noise in CCD Signal Detection"*. IEEE Trans. Electron Devices, vol. ED-33, no. 11, pp. 1696-1701, November 1986.

[15] A.Theuwissen, J.Bakker, H.Cox, A.Kokshoorn, P.v.Loon, B.O'Dwyer, J.Oppers, C.Weijtens. *"A 400k pixels 1/2" accordion CCD imager"*. Digest Technical Papers ISSCC88, pp 48-49, San Francisco, Febr 17-19, 1988.

[16] D.Barbe, *"Imaging Devices Using the Charge-Coupled Concept"*, Proceedings of the IEEE, vol. 63, No. 1, January 1975, pp 38-67.

[17] J.Hynecek, *"Spectral Analysis of Reset Noise Observed in CCD Charge-Detection Circuits"*. IEEE Trans. Electron Devices, vol. ED-37, no. 3, pp. 640-647, March 1990.

[18] P.Centen and F.Spierings, *"Report on the Noise-Behaviour of the output structure of FT4 image sensors"*, August 1985, Internal report Philips.

[19] R.Brewer, *"A Low Noise CCD Output Amplifier"*, Technical Digest IEDM79, pp. 610-612, Washington DC, Dec 3-5, 1979.

[20] G.Hobson, R.Longstone and R.Tozer, *"Dual-gate charge sensing in charge-coupled devices."* IEEE Trans. Electron Devices, vol. ED-2, no. 6, pp. 207-214, Nov. 1978.

[21] Y.Matsunaga, *"A High Sensitivity Output Amplifier For CCD Image Sensor"*,Technical Digest IEDM87, pp 116-119, Washington DC, Dec 6-9, 1987.

[22] E.Roks, P.Centen, J.Bosiers, W.Huinink, *"The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD Image Sensors"*. IEEE Trans. Electron Devices, vol. ED-43, no. 9, pp. 1583-1591, September 1996.

[23] E.Roks, P.Centen, L.Sankaranarayanan, J.Slotboom, J.Bosiers, W.Huinink, *"A Bipolar floating-base detector (FBD) for CCD Image Sensors"*. Technical Digest IEDM92, pp 109-112, San-Francisco, Dec 13-16, 1992.

[24] H.S. Wong, *"Technology and Device Scaling Considerations for CMOS Imagers"*. IEEE Trans. Electron Devices, vol. ED-43, no. 12, pp. 2131-2142, December 1996.

[25] E.R. Fossum, *"CMOS Image Sensors: Electronic Camera-On-A-Chip"*. IEEE Trans. Electron Devices, vol. ED-44, no. 10, pp. 1689-1698, October 1997.

[26] C.Enz, *"Analyses of low frequency noise reduction by autozero technique"*, Electronic Letters, Vol. 20, No. 23, pp 959-960, Nov 1984.

[27] A. Papoulis. *"Probability, Random Variables, and Stochastic Processes"*. McGraw-Hill Kogakusha, LTD, 1965; Library of Congres Catalog Card Number 64-22956, pp. 435

[28] M.v.Buul and P.Centen, *"Sampling Circuit"*, PCT application WO 96/01475, January 1996.

[29] R.Kansy, *"Response of a correlated double sampling circuit to 1/f noise"*, IEEE Journal of Solid-State Circuits, vol. SC-15, June 1980, pp 373-375.

[30] M.Abramowitz and I.Stegun. *"Handbook of mathematical functions"*. Dover publications, Inc, New York, 1972; Standard Book number 486-61272-4.

Chapter 5

READOUT MODES
Reset noise-free readout mode for a floating diffusion detector[6]

5.1 Introduction

Although a floating diffusion region is generally used together with a correlated double sampler signal processor, the question arises as to whether the signal current which flows out of the reset drain could be used as a signal output instead, with a comparable or improved signal-to-noise ratio. This signal would not have to be corrected for offset at each pixel and the signal processing could be done in a continuous and much more simple manner.

The flow of charge through the horizontal register of a solid state image sensor can be regarded as either a series of charge packets or as a current. In the first case the obvious detector is a capacitor to convert charge into a voltage; in the second case a resistor. In many CCD imagers a floating diffusion region is used for charge to voltage conversion.

For CCD imagers where charge is clocked at high speed through the horizontal register it is difficult to design a discrete time signal processor with a good

---

[6] *Based on the publication: P.Centen, "A Reset-Noise Free High-Speed Readout Mode for a Floating-Diffusion Detector with Resistive Feedback". Philips Journal of Research, Vol. 48. No. 3, 1994, pp. 271-280.*

signal-to-noise performance. For example, suppose that the clock frequency is 72 MHz. In this case one clock interval has a period time of 13.9 ns, with 6.9 ns available for the video signal (50% duty cycle), 4.6 ns for the reset noise hold level, and 2.3 ns for switching on the reset FET. Generating pulses which have rise and fall times of less than a nanosecond and a delay with respect to the CCD clocks to compensate for the propagation delay of the on-chip amplifier is a problem.
In comparison, when using a resistor to convert current into a voltage neither special timing nor compensation for the propagation delay is required and the signal processing consists of only a low-pass filter.

In **Section 5.2** the traditional floating diffusion approach with reset is discussed. The noise spectral density and sensitivity (whose ratio is the noise electron density) have been derived for the combination of a floating diffusion detector with reset and a matching filter (Chapter 4). Now the modulation transfer function (MTF) of the whole output circuit must be calculated. By correcting the noise spectral density and the sensitivity with the modulation transfer function one finally arrives at the equivalent noise electron density (Chapter 2) that has been corrected for MTF.

Section 5.3 presents a new way of reading out a floating diffusion detector using the reset drain current. Here too the noise spectral density, the sensitivity, and the modulation transfer function are found, giving the noise electron density.

These two readout methods are then compared in **Section 5.4** using the values of the noise electron density. The relative merits of each are then clear.

Section 5.5 makes some remarks about 1/f noise and its importance for the new readout method.

One of the basic elements in the new design is a feedback resistor. In **Section 5.6** some numerical examples are given to show whether it is possible to fulfil the conditions established in Section 5.4.

Section 5.7 the reset FET is used as an adjustable feedback resistor. This section presents a possible circuit implementation and experimental results.

We close with conclusions and an overall discussion of results in **Section 5.8.**

5.2 Readout of the classical floating diffusion detector with reset

The traditional floating diffusion configuration [1,2] for reading out charge packets is extensively described in any textbook on CCD imagers [3]. Figure 5.1 shows the basic elements of the output stage: the horizontal register driven with the horizontal gates Φ_1,Φ_2,Φ_3, the output gate OG, and the floating diffusion region with capacitance C. The reset FET is connected to the diffusion to clamp the floating diffusion capacitor[7] to the RD-voltage prior to the arrival of the next charge packet.

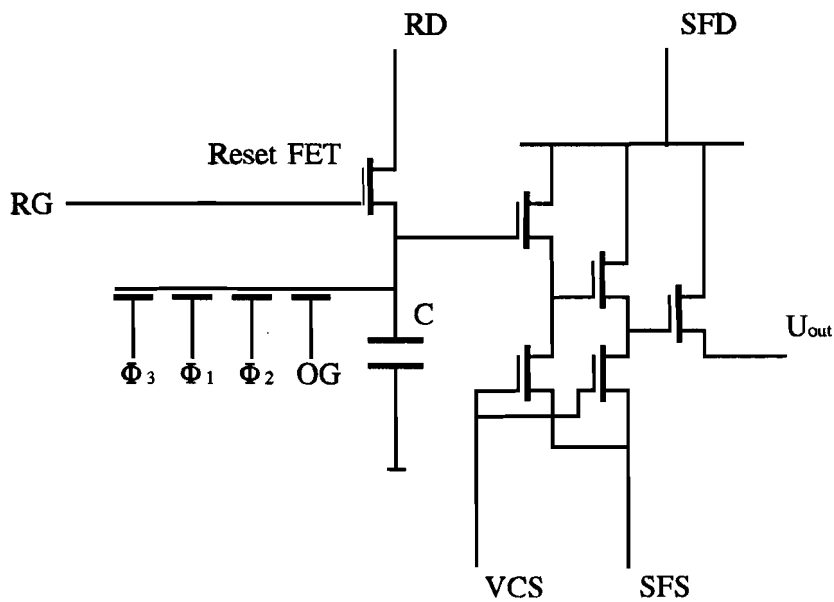

Figure 5.1: A destructive charge readout with a floating diffusion region and reset FET.

The reset FET is switched by applying a pulse to the reset gate (RG). The

[7] *For simplicity's sake the total capacitance C_{tot} and the detector capacitance C_{det} are taken as equal and are denoted by C.*

supply voltage to the on-chip amplifier is V_{SFD}, and V_{SFS} is connected to ground. The voltage applied to the current source CS (V_{CS}) determines the bias current of the first two source follower stages.
The equivalent noise voltage of the on-chip amplifier at the gate of the first stage is denoted e_n. The charge q·N dumped on the floating diffusion can be regarded as a current source i_n (see also Figure 5.5). For one charge packet the following relationship holds

$$\int_{-\infty}^{\infty} i(t)\, dt = q\, N \qquad (5.1)$$

where q is the unit charge of one electron and N is the number of electrons in one charge packet.
A charge packet in the horizontal CCD register is transported with a clock frequency f_p. Therefore, during each clock period $T_p=1/f_p$ charge will be dumped on the detection node.
After the detection node capacitor C has received a charge packet the reset FET will clamp (reset) the capacitance to a reference potential V_{RD}. This prepares the capacitor to receive the next packet. This clamping generates reset noise [2]. Such reset noise can reach high values, as much as 40 electrons. Signal processing [4,5,6,7] such as Correlated Double Sampling, two-slope integration, delay line processing, or Clamp and Sample is needed to suppress the reset noise and to obtain reasonably low noise levels. In many cases the last element in such a signal processing chain is a zero-order hold circuit which adds a sin(x)/x noise spectrum.

In the field of CCD imaging it is a custom to express the noise voltage as an equivalent number of electrons (Chapter 1). The reason for this lies in the fact that almost all the important performance parameters of a CCD imager are expressed in the number of electrons a charge packet contains. The conversion of a noise voltage into a number of electrons is made using the sensitivity S. For example, if one measures a noise voltage of 250 μV and the sensitivity is 10 μV/e then the noise is 25 electrons, abbreviated 25 e. Strictly speaking this is outside the MKS system for units, but it has been common practice for over 20 years.
Another quantity for expressing the noise is based on the above practice. The noise 'voltage' is expressed in the number of equivalent electrons and the noise spectral density can be expressed as the equivalent number of electrons squared per unit of bandwidth: the noise electron density.

Assuming a gain A for the on-chip amplifier, the noise voltage at the output of the on-chip amplifier is A e_n. To convert this to a quantity that is easier to use in noise calculations, normalize the voltage output by the voltage caused by a single electron, A q/C. This quantity has dimensions e^2/Hz and it is called the Noise Electron Density NED (see compare Chapter 2).

It was shown in Section 4.3.5 that the noise limit which can be obtained with optimal filtering is given by:

$$S_{nn}(f) = M \left(e_n \frac{C}{q} \right)^2 sinc^2 \left(\frac{f}{f_p} \right) \tag{5.2}$$

The signal processor's figure of merit (M) for the optimal filter of a single-output CCD is:

$$M = \frac{T_p}{T_v} + \frac{T_p}{T_{rs}} = 5 \tag{5.3}$$

In this equation the different time intervals are respectively:

T_p the inverse of the horizontal clock frequency, $T_p=1/f_p$.
T_v the time video is available, usually $T_p/2$.
T_{rs} the duration of the reset hold level, usually about $T_p/3$.

Integrate and dump processing is a matched filter for CCD imagers [5,7]. The integrate action gives the optimal filtering and the dump phase a sin(x)/x spectrum (equation (5.2)). Figure 5.2 plots equation (5.2) with M=5, a noise voltage of e_n=25 nV/$\sqrt{}$Hz for the on-chip amplifier, a detection node capacitance of C=16 fF, and a clock frequency of f_p=36 MHz.
In practice it is very difficult to build an optimal signal processor for high speed operation and the value M=5 will not be met. A value between 5 and 10 is more realistic for clock frequencies between 20 MHz and 50 MHz.

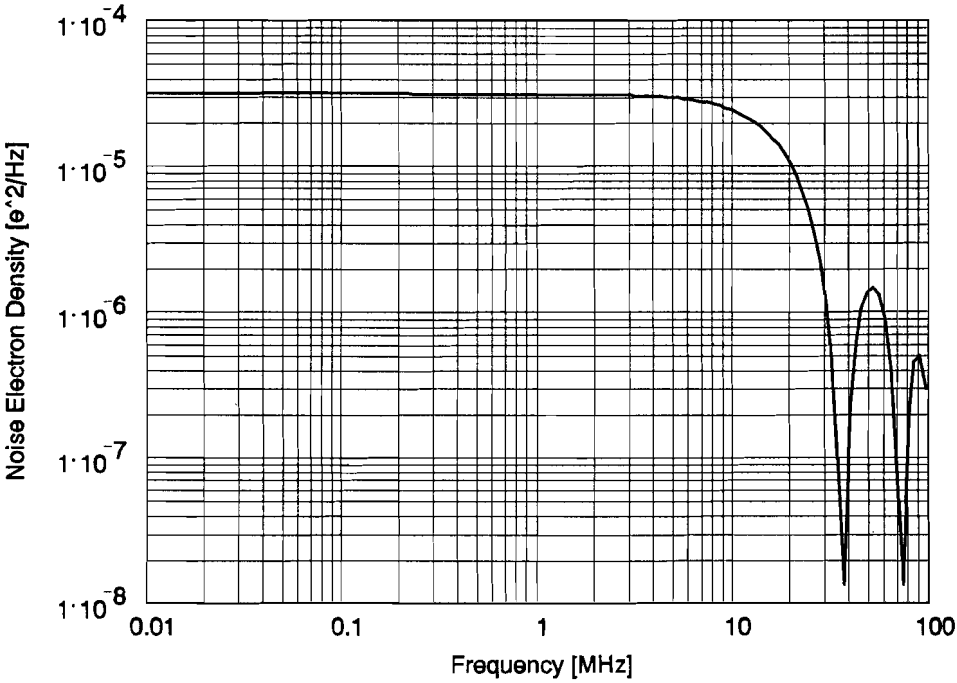

Figure 5.2: *The noise spectral density versus frequency for a horizontal register clocked at f_p=36 MHz followed by a signal processor with a figure of merit of M=5.*

To compare two readout methods the noise spectral density must be corrected for the transfer function (charge to output voltage). This makes the comparison between this method and the current based method more fair. The electrical frequency response to the transfer of one pixel containing a charge of 1 electron is given by:

$$S(f) = \frac{-qA}{Cf_p} \, sinc\left(\frac{f}{f_p}\right) \tag{5.4}$$

and the normalized frequency response, also called the electrical modulation transfer function (MTF) reads:

$$MTF(f) = \left| \frac{S(f)}{S(0)} \right| = \left| sinc\left(\frac{f}{f_p}\right) \right| \tag{5.5}$$

and is given in Figure 5.3 for a horizontal clock frequency of f_p=36 MHz.

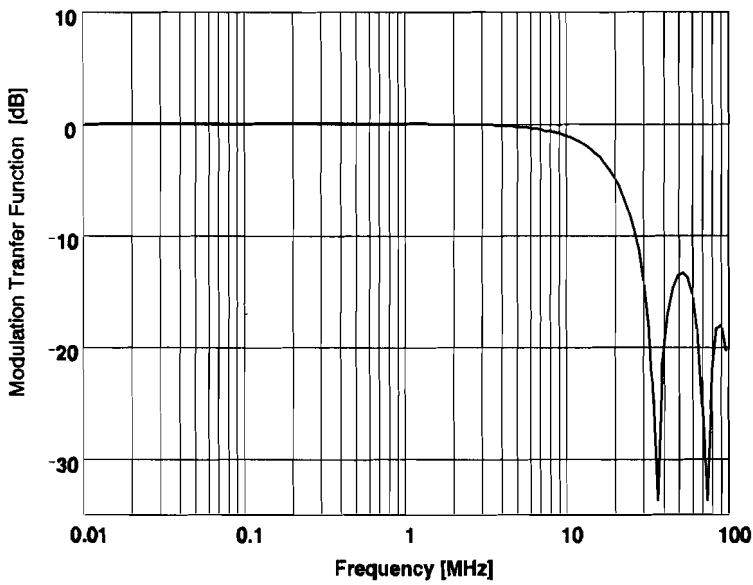

Figure 5.3: *The normalized frequency response (MTF) of the horizontal register together with an optimal signal processor running at f_p=36 MHz.*

Both the noise spectral density and the normalized frequency response are sin(x)/x shaped and the noise spectrum corrected for the frequency response will be flat (Figure 5.4). This corrected noise spectrum equals NED_C=M·NED

Its noise power over the bandwidth B_m, expressed in equivalent noise electrons N_C, equals

$$N_C^2 = M \left(\frac{e_n C}{q} \right)^2 B_m \qquad (5.6)$$

The above equation is very important since it will be used to compare the performance of the traditional readout with the resistive feedback method, described in the next section.

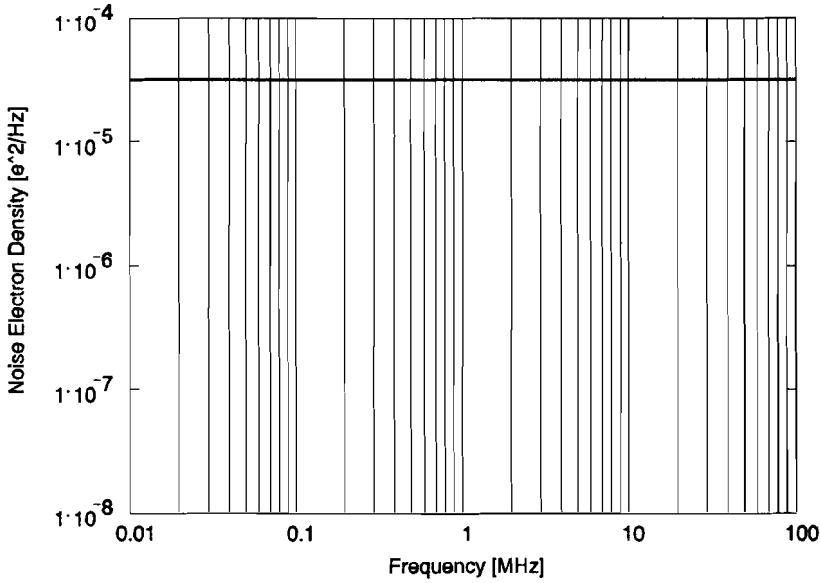

Figure 5.4: The noise electron density after normalization for the frequency response.

Reducing the number of equivalent noise electrons N_C is possible by choosing a signal processor that has matched filter properties for the signal and noise spectrum involved (Chapter 4), or by optimizing the on-chip amplifier noise properties as discussed in Chapter 2 and Chapter 3.
This chapter deals with the case where the noise properties of the on-chip amplifier are fixed and where for the signal processor the matched filter (the two-slope integrator) is chosen.

5.3 Destructive charge readout using resistive feedback

The resistive feedback mode (Figure 5.5) makes use of an on-chip high ohmic resistor instead of the well-known reset transistor (Figure 5.1) and an (off-chip) inverter stage with gain -G for feedback.

Similar to the well known floating diffusion detector with on-chip amplifier [1,2,3], the use of a resistor to convert charge packets into a voltage signal is a very old concept [8]. What is new is the feedback of the output voltage of the on-chip amplifier via an on-chip resistor back to the floating diffusion. The resistor is placed on-chip because an off-chip resistor would increase the capacitance C from tens of fF to the order of pF's due to the bondpad, wiring, and stray capacitances. In this case one could never obtain a sufficiently low noise level.

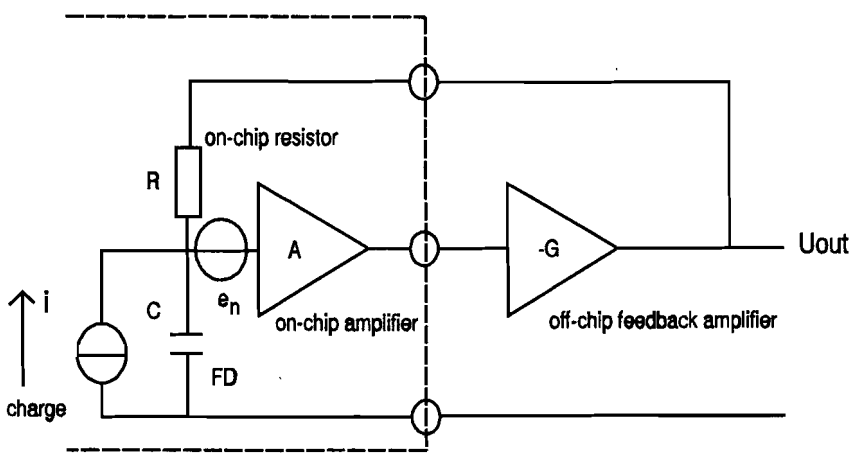

Figure 5.5: *The resistive feedback readout mode. The amplifier with gain A, the feedback resistor R, and a floating diffusion region FD with capacitance C are on-chip. Off-chip is the negative feedback amplifier with gain -G together with part of the feedback loop. Compared to the traditional concept of a floating diffusion detector, the reset FET has been replaced by the on-chip resistor R.*

The transfer function H(f) between the (charge) current I(f) and the output voltage $V_{out}(f)$ is given by:

$$\frac{V_{out}(f)}{I(f)} = H(f) = -\frac{A\,G}{1 + A\,G}\,\frac{R}{1 + \dfrac{j\,2\,\pi\,f\,R\,C}{1 + A\,G}} \tag{5.7}$$

in which R is the on-chip feedback resistor, C the capacitance of the floating diffusion detector, -G the gain of the feedback amplifier, and A the gain of the on-chip amplifier.

With a high open-loop gain (AG -> ∞) the transfer function reduces to

$$V_{out}(f) = -R\,I(f) \tag{5.8}$$

and the shape of the output spectrum equals the input spectrum.
The average current per pixel with N electrons in one charge packet is

$$\bar{i} = \frac{1}{T_p}\int_{-\infty}^{\infty} i(t)\,dt = \frac{-q\,N}{T_p} \tag{5.9}$$

The average output voltage per pixel is $V_{out}=R\cdot q\cdot N/T_p$ and, in the resistive feedback mode, the sensitivity S equals $R\cdot q/T_p$.

Assuming a Dirac pulse for the signal current, which is equivalent to a fast dump of the charge packet on the floating diffusion region

$$i(t) = -q\,N\,\delta(t) \leftrightarrow I(f) = -q\,N \tag{5.10}$$

Substituting the right hand side of equation (5.10) into equation (5.7) gives an expression for the output spectrum, and the normalized frequency response is:

$$MTF(f) = \left|\frac{H(f)}{H(0)}\right| \tag{5.11}$$

The amplitude response in Figure 5.6 is calculated using equation (5.7). The feedback resistor R=34 MΩ, the detection capacitance C=16 fF, and the open-loop DC gain $A\cdot G=50$. The on-chip amplifier represented by A(f) has a pole at 100 MHz. This pole forms a second order low-pass filter when it combines with the pole from the feedback RC-time constant. The filter causes the peak in the MTF at 10 MHz.

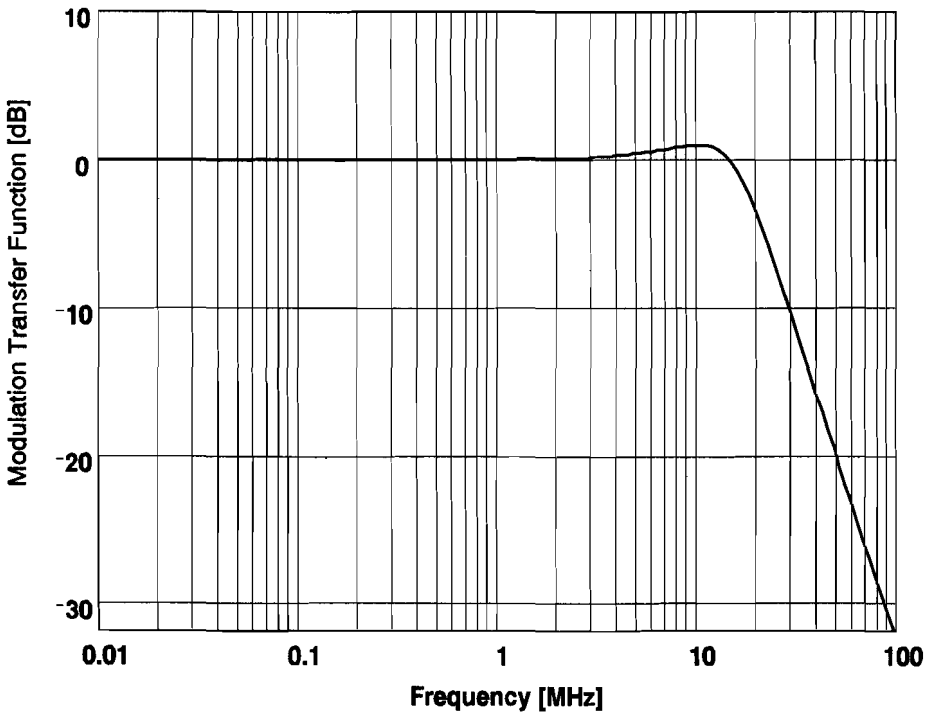

Figure 5.6: The normalized response (MTF) of the system caused by the transfer of one charge packet as a function of frequency.

The current noise spectral density of the feed-back resistor is 4kT/R and that of the on-chip amplifier e_n^2/R^2. Together they give rise to a noise spectral density $S_{vv}(f)$ at the output of the feedback amplifier

$$S_{vv}(f) = H(f)\, H^*(f) \left[\frac{4\, kT}{R} + \frac{e_n^2}{R^2} \left[1 + (2\, \pi\, f\, R\, C)^2 \right] \right] \qquad (5.12)$$

Figure 5.7 plots $S_{vv}(f)$ for a feedback resistor R=34 MΩ, a detection node capacitance C=16 fF, and a noise voltage e_n=25 nV/√Hz. The on-chip amplifier has a pole at 100 MHz and the open loop DC gain is 50.

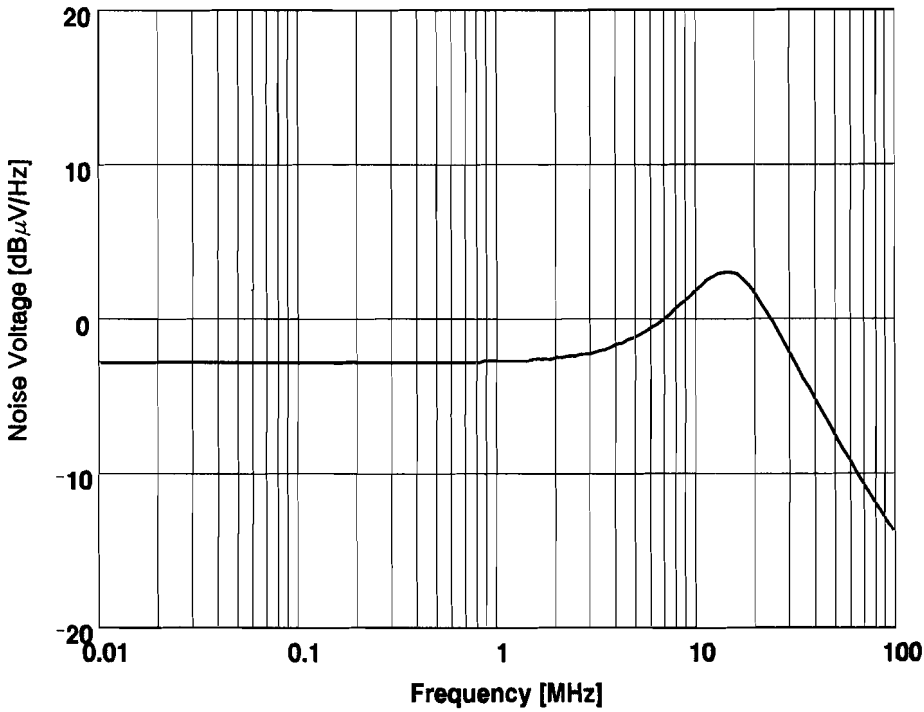

Figure 5.7: The noise spectral density at the output of the feedback amplifier as a function of frequency.

After correction for the normalized frequency response (equation (5.11)) the noise spectral density reads

$$|H(0)|^2 \left[\frac{4\ kT}{R} + \frac{e_n^2}{R^2} \left[1 + (2\ \pi\ f\ R\ C)^2 \right] \right] \qquad (5.13)$$

To compare this result to the reset FET performance, the noise voltage has to be converted into an equivalent number of noise electrons and an equivalent noise electron density. This is accomplished by dividing the noise voltage by the sensitivity.

When a continuous flow of charge packets of one electron per pixel is transported through the horizontal register and dumped at the detection node then the output voltage at the feedback amplifier -G is

$$S = \left| H(0)\ \frac{q}{T_p} \right| = \left| H(0)\ q\ f_p \right| = \left| \frac{AG}{1 + AG} \right| R\ q\ f_p \qquad (5.14)$$

In fact, this is the sensitivity.
After dividing the noise spectral density of equation (5.13) by the squared sensitivity S^2 the noise electron density for the feedback mode becomes

$$NED(f)_R = \frac{\left[\frac{4\ kT}{R} + \frac{e_n^2}{R^2} \left[1 + (2\ \pi\ f\ R\ C)^2 \right] \right]}{q^2\ f_p^2} \qquad (5.15)$$

With the parameter values used in the above calculations and a clocking speed of f_p=36 MHz, the sensitivity is S=192 μV/e.
The noise electron density for the resistive feedback mode is given in Figure 5.8. A remarkable feature of the noise electron density is that it is constant at low frequencies and increases at higher frequencies. This spectrum is said to have a triangular shape. The main portion of the noise power is at the high end of the frequency spectrum. For a given number of equivalent noise electrons the spectral density at low frequencies is small.

The equivalent number of noise electrons in a bandwidth B_m is given by

$$N_R^2 = \int_0^{B_m} NED(f)_R\ df =$$

$$\frac{4\ kT}{q^2\ f_p^2\ R}\ B_m + \left[\frac{e_n}{q\ f_p\ R} \right]^2 B_m + \left[\frac{e_n\ C}{q} \right]^2 \left[2\ \pi\ \frac{B_m}{f_p} \right]^2 \frac{B_m}{3} \qquad (5.16)$$

Together with equation (5.6), this is a very important result which forms the basis for a comparison between the two readout methods. This comparison is

made in the next section.

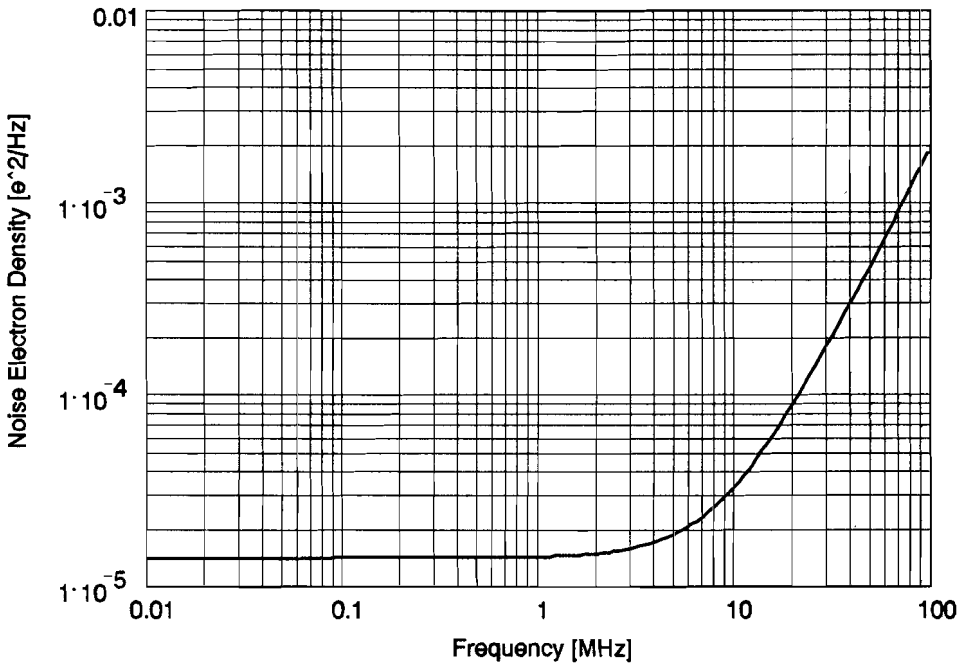

Figure 5.8: *The noise electron density after normalization for the frequency response.*

In general one wants to use the whole bandwidth up to the Nyquist frequency ($f_p/2$); the ratio between the bandwidth B_m and clock frequency f_p will be fixed at 1/2. Inspection of the above equation with this in mind shows that the contribution of the first and the second terms on the right hand side of equation (5.16) decreases with increasing values of the feedback resistor R or the clock frequency f_p. The second and third terms are proportional to the equivalent noise electron density of the on-chip amplifier, $NED=(e_n\ C/q)^2$. In addition the contribution of the third term increases with increasing value of the clock frequency f_p.

In a practical situation with a specific imager application, the bandwidth B_m, clocking frequency f_p, and noise electron density of the on-chip amplifier

$NED=(e_n \cdot C/q)^2$ are fixed. Only the feedback resistor value R is left to control the equivalent noise electrons N_R. The larger its value the lower the noise will be.

5.4 Comparison of both methods

The integrate and dump technique has a noise spectrum which, after correction for the frequency response, is flat whereas the resistive feedback mode has a triangular noise spectrum. Figures 5.4 and 5.8 are superimposed in Figure 5.9 to show the difference. The noise spectral density (flat spectrum) of the classical floating diffusion with reset technique is much higher (for the example shown in Figure (5.9) this amounts to a factor of 2.3) at low frequencies. At a frequency of about 10 MHz the performance of both equal, and beyond this the new method falls behind.
In the case of an image sensor the resistive feedback circuit has the additional benefit that at equal noise power the subjective appraisal of the noise is better. This result is due to the fact the human eye is less sensitive for noise at high frequencies.

To determine the difference in noise performance of both readout modes the ratio between the number of noise electrons must be calculated. The number of noise electrons in the resistive feedback case (equation (5.16)) divided by the number in the traditional case (equation (5.6)) is given by

$$\frac{N_R^2}{N_C^2} = \frac{\dfrac{4\ kT\ R}{en^2} + 1}{f_p^2\ R^2\ C^2\ M} + \frac{4\ \pi^2}{3\ M}\left[\frac{B_m}{f_p}\right]^2 \qquad (5.17)$$

Clearly the last term on the right hand side is only determined by the ratio (B_m/f_p) between bandwidth and clocking frequency. Since no signal reconstruction is possible for output signals above half the sample rate this ratio will always be smaller than 1/2. A reconstruction filter has to be used at $f_p/2$ or less.

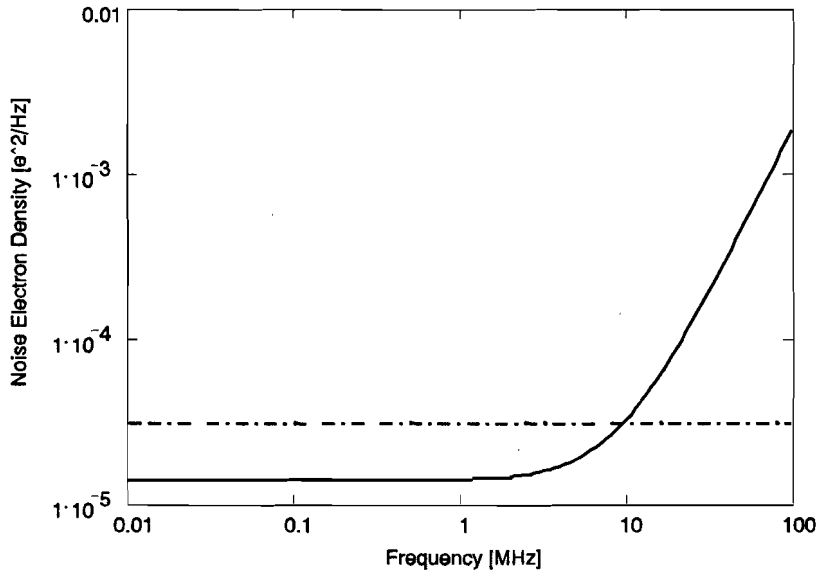

Figure 5.9: *The dashed line gives the noise spectral density of the classical floating diffusion detector with reset and the solid line the noise spectral density for the resistive feedback mode.*

Therefore a minimum requirement for the resistive feedback circuit to have an equal or a better signal-to-noise ratio is that the signal processing performance index M for a bandwidth of half the sample frequency ($B_m=f_p/2$) is larger than

$$M \geq \frac{4\ \pi^2}{3}\left(\frac{B_m}{f_p}\right)^2 = 3.29 \qquad \textbf{(5.18)}$$

In general, since M≥5, this is always the case. An exception to this is a Floating Gate structure [9,10,11,12] followed by a low pass filter, which can reach a noise performance index of M=2. This output structure will always have a better signal-to-noise ratio than the resistive feedback mode when used at up to half the sample frequency $B_m=f_p/2$. However, when used at a bandwidth below $B_m<(0.39\cdot f_p)$, the use of the feedback resistor mode can be even better than a Floating Gate structure with matched filter.

The value of the feedback resistor needed to make the signal-to-noise ratio equal to the reset FET mode is

$$R_{\min} = \frac{2R_n}{\sqrt{1+4R_n^2 f_p^2 C^2 M\left(1-\frac{4\pi^2}{3M}\left(\frac{B_m}{f_p}\right)^2\right)-1}} \qquad (5.19)$$

where

$$R_n = \frac{e_n^2}{4kT} \qquad (5.20)$$

This is the minimum value needed. A larger value will out-perform the classical way of reading out and filtering CCD imager signals.
The above equation closes the comparison between the two readout modes. It shows that, under certain conditions, the resistive feedback mode can have an equal or better signal-to-noise ratio than the floating diffusion detector.

In Figure 5.10 the minimum value for the feedback resistor R_{min}, is given as a function of the clock frequency f_p for three situations. One is for a fixed bandwidth of B_m=5 MHz, the second when the ratio between bandwidth and clock frequency is fixed at B_m/f_p=1/2, and the third for a very small ratio between the bandwidth and clock frequency, B_m/f_p=0. The parameter values used to calculated Figure 5.10 from equation (5.19) are M=5, C=16 fF and e_n=25 nV/$\sqrt{}$Hz. At low clock frequencies the minimum feedback resistor value needs to be very large. For example, at a clock frequency of 20 MHz the feedback resistor has to be between 55 MΩ and 150 MΩ for a signal-to-noise ratio that can compete with the classical way of readout. At typical clock frequencies in use for HDTV, f_p=72 MHz and f_p=144 MHz, the minimum value of the feedback resistor R=12 MΩ and R=3 MΩ, respectively.

Unfortunately feedback resistor values in the order of 10-1000 MΩ are needed to arrive at an equal signal-to-noise ratio. This will be very difficult to accomplish in silicon without introducing other drawbacks.
A feedback resistor fabricated from polysilicon requires a large area. Such a resistor adds an additional parasitic capacitor to the total capacitance of the

detection node, decreasing its noise performance.

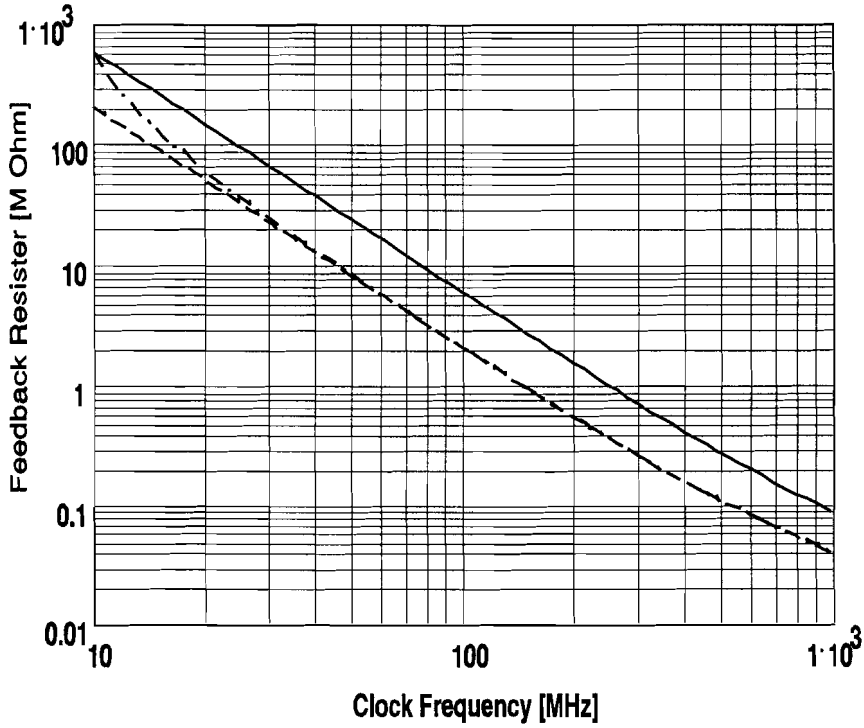

Figure 5.10: *The value of the feedback resistor R that makes current-to-voltage output and charge-to-voltage output equal in performance with regard to SNR. Two values for the bandwidth B_m/f_p=1/2 (solid line) and B_m=5 MHz (dash-dot line) are plotted as well as the asymptotic value B_m/f_p=0 (dashed line). The horizontal axis shows the clocking frequency.*

If, on the other hand, a high value for 'rho sheet' is chosen the reproducibility and linear behaviour are poor.
As shown in section 5.7 the channel resistance of the reset FET can be used to act as the feedback resistor. This method leaves the design unchanged; only the biasing conditions are changed. It does not increase the parasitic capacitances of the detection node. However, due to the fact that the reset FET is used in its sub-threshold region, a non-linear charge to voltage conversion results.

Equation (5.19) can be simplified by using the fact that the equivalent noise resistance R_n of a MOS transistor is on the order of magnitude of its transconductance g_m and the capacitance C is of the order of the MOS transistor gate capacitance. Therefore as long as the clocking frequency f_p is below the cut-off frequency g_m/C of the MOS transistor the second term under the root sign is small and equation (5.19) can be approximated by

$$R_{min} \approx \frac{R_n}{(R_n f_p C)^2 M \left(1 - \frac{4\pi^2}{3M}\left(\frac{B_m}{f_p}\right)^2\right)} \qquad (5.21)$$

For a fixed value of the processing's performance index, M=5, and a bandwidth of half the clock frequency, $B_m=f_p/2$, equation 5.21 reduces to

$$R_{min} \approx \frac{R_n}{(R_n f_p C)^2 1.71} = \frac{4kT}{NED f_p^2 q^2 1.71} \qquad (5.22)$$

The first equation is created from equation (5.20) and the definition of the noise electron density, $NED=(e_n C/q)^2$.

The minimum value for the feedback resistor decreases with the square of the clock frequency f_p and with NED.

5.5 Effect of 1/f noise

One aspect that remains to be discussed is the presence of 1/f noise and its effect on signal-to-noise ratio and the subjective appraisal of images.

So far this study is based solely on input noise with a white spectrum, but practically one also encounters 1/f noise. One of the functions of a signal processor like CDS is suppression of reset noise. However, by doing that it suppresses the 1/f noise at the same time. With the resistive feedback readout scheme the 1/f noise will not be suppressed. Normally the thermal noise of the feedback resistor with its high value masks the 1/f noise. In other words, because the thermal noise of the feedback resistor is larger than the thermal noise of a MOS transistor, the corner frequency of the 1/f noise will be lower.

Given an on-chip amplifier with thermal noise e_n=25 nV/√Hz, a cross-over frequency of F_C=0.435 MHz and a feedback resistor of R=34 MΩ the cross over

frequency will shift towards 0.5 kHz (equation (5.15)). This is well below visibility[8]. The clamp used for DC restoration in a CCD camera will also further reduce the remaining low-frequency disturbance generated by the 1/f noise.

5.6 Numerical examples

For a CCD imager the detection node capacitance C, clock frequency f_p, noise voltage of the on-chip amplifier e_n and bandwidth B_m are fixed and the only freedoms left in the design are the choice of the feedback resistor R and the ability to design a well performing signal processor (Chapter 4: figure of merit M). The feedback resistor R is the parameter that determines the performance of the new readout method and the figure of merit M describes the performance of the traditional circuit. The purpose of this study is to find a value for R, if one exists, that betters the signal-to-noise performance of the reset FET sample and hold circuit. In general an answer can be found in equation (5.17) and the associated condition in equation (5.19). Some numerical examples will now be given.

- Assume C=16 fF, f_p=72 MHz, e_n=25 nV/$\sqrt{\text{Hz}}$, B_m=30 MHz, and a signal processing figure of merit of M=5. According to equation (5.19) the value of the feedback resistor must be at least R=7.1 MΩ. Following equation (5.14), the sensitivity will be S=82 μV/e. In the case that the figure of merit for the signal processing has a poor value like M=10, the feedback resistor must be R=2.5 MΩ and the sensitivity will drop to S=29 μV/e.
- Next we assume the use of the above imager in the progressive mode. Then f_p=144 MHz and B_m=60 MHz. In this case R must be at least R=1.8 MΩ to be competitive, which corresponds to a sensitivity S=42 μV/e. With M=10 the resistor value drops to R=0.66 MΩ with a sensitivity of S=15 μV/e.

Generally a practical system does not have an infinite open-loop gain and the pole-zero combination must be considered. With a correct choice of time constants and feedback gain it is possible to shape the output waveform of one pixel. This is especially important because one can choose to shape the waveform in such a way that the main part of the signal energy is below the Nyquist frequency. This lessens the demands on the filtering properties of the low pass filter that is needed to suppress spectral components above the Nyquist

[8] *Empirically the visibility limit for the corner frequency is about 100 kHz.*

frequency.
The output voltage of an on-chip amplifier from a HDTV imager [13] has been simulated using MICROCAP, a SPICE-like analysis program. Figure 5.11 presents the result for a bandwidth of 170 MHz, and Figure 5.12 for a bandwidth of 36 MHz. Each graph consists of two parts. The upper part shows two current pulses that are the input to the detection node. The amplitude is given in arbitrary units and the amount of charge contained in the two current pulses is the same. The first current pulse has a duration of 1 ns, the other 7 ns. The spacing between the two current pulses is 8 pixels. The lower part gives the output voltage. This voltage is almost insensitive to the duration of the 'charge' pulse and the bandwidth of the on-chip amplifier.

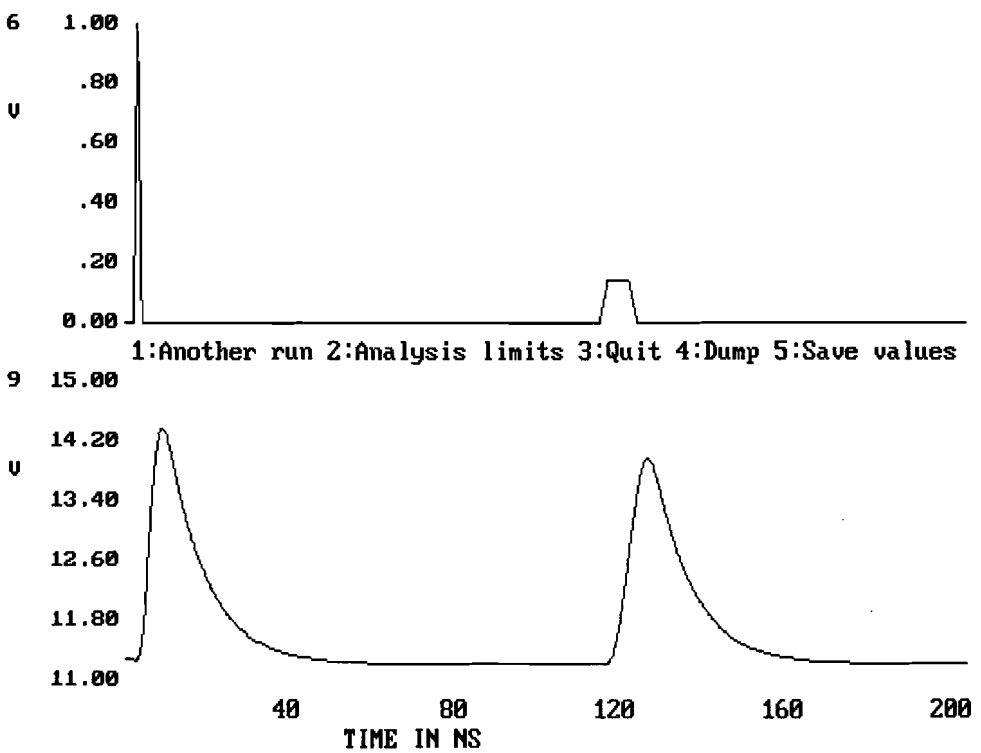

Figure 5.11: *The output voltage (V_{out}) in the resistive feedback mode as a function of two different current pulses (i) with equal charge content. One has a duration of 1 ns and the other 7 ns. The spacing between the two current pulses is 8 pixels. The bandwidth of the on-chip amplifier is 170 MHz.*

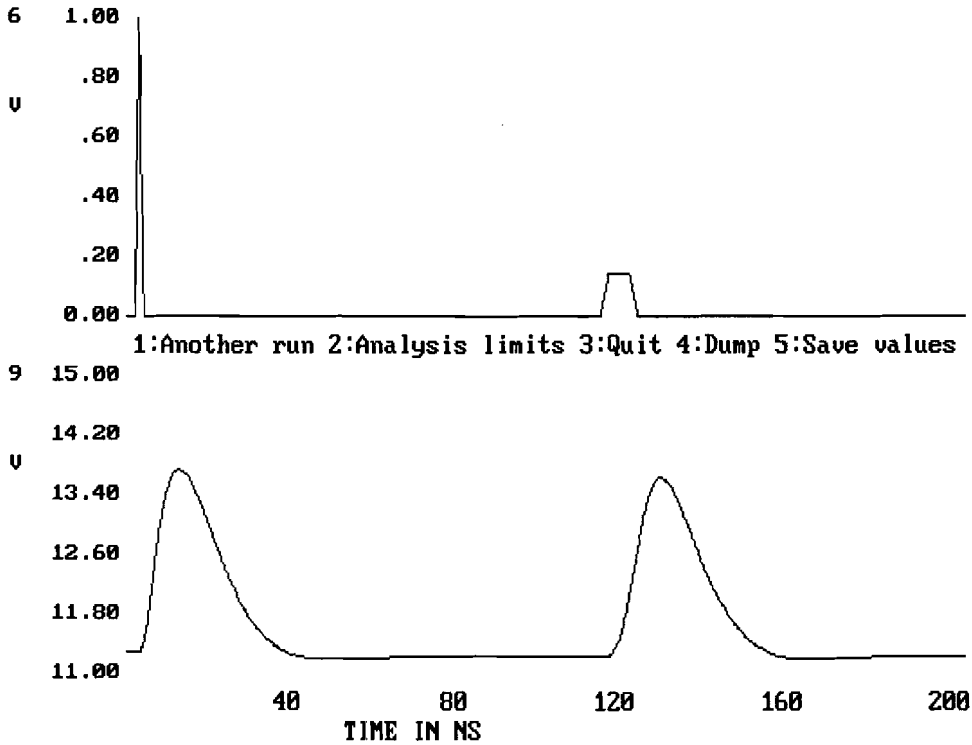

Figure 5.12: The output voltage (V_{out}) in the resistive feedback mode as a function of two different current pulses (i) with equal charge content. One has a duration of 1 ns and the other 7 ns. The spacing between the two current pulses is 8 pixels. The bandwidth of the on-chip amplifier is 36 MHz.

The duration of the pixels at the output as shown in the lower part of the Figure 5.11 and Figure 5.12 is longer than one clock period, which is 1/72 MHz=13.9 ns. In on-chip CCD image applications this can be a serious drawback since one does not have at his disposal the individual pixel values. Only a low pass filtered output is obtained.

5.7 Experimental results

In the following experiment the reset FET is used as the feedback resistor. The gate of the reset FET is not switched but kept at a fixed DC potential. For small

signals the reset FET acts as a resistor whose value depends on the gate potential.
The test circuit given in Figure 5.13 has been designed and evaluated, Rotte [14]. The sensor output signal is fed into a CE stage whose output is connected to the reset drain terminal (RD). For three different values of the reset gate DC voltage (V_{RG}) the noise spectral density (Figure 5.14) and the transfer function (Figure 5.15) were measured. To maintain stability the gain of the CE stage was changed too, by changing the emitter resistor R_e of transistor BFR92 in the figure below.

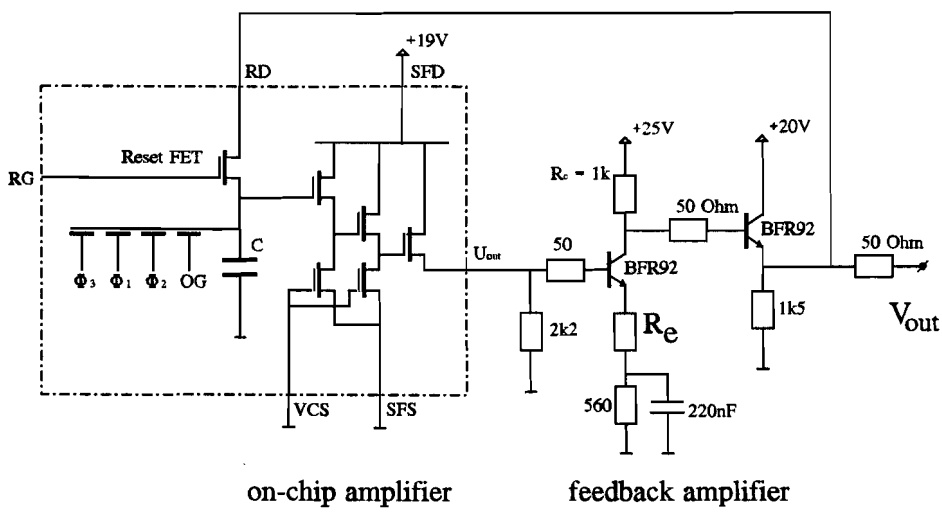

Figure 5.13: Test circuit with a CE stage used as a feedback amplifier and the reset FET used as an adjustable resistor.

Using equations (5.7) and (5.12) the reset FET channel resistance value R could be calculated from the measurements given in Figure 5.14 and Figure A1 (Appendix A). The values for R were determined to be 11 MΩ, 34 MΩ, and 2.8 MΩ.
To maintain stability the emitter resistor R_e had to be changed from 100 Ω to 33 Ω and 13 Ω, respectively.

Inspection of Figure 5.14 shows that 1/f noise is well masked by the thermal noise of the resistor.

The 50 Ω termination of the spectrum analyzer gives an additional 6 dB attenuation of the noise voltage.

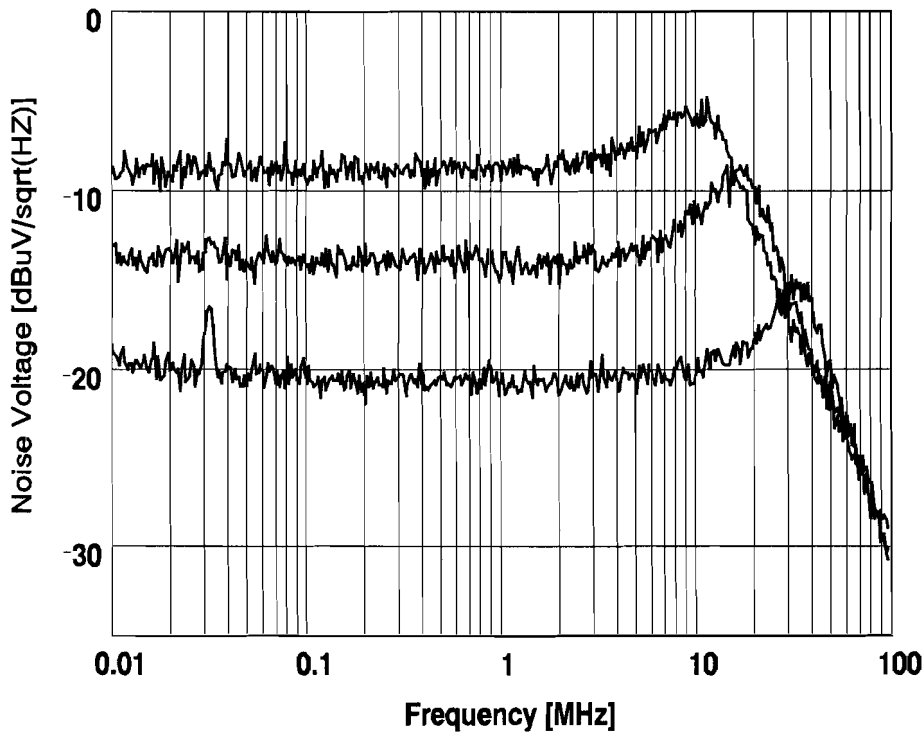

Figure 5.14: *The voltage noise spectral density for 3 values of the feedback resistor: upper trace R=34 MΩ, middle trace R=11 MΩ, and lower trace R=2.8 MΩ*

Next, one wants to determine the transfer function for the current-to-voltage conversion. To measure the transfer function a two step method has been applied, as described in Appendix A. With the transfer function given in Figure 5.15 the voltage noise spectral density can be converted into the noise electron density.

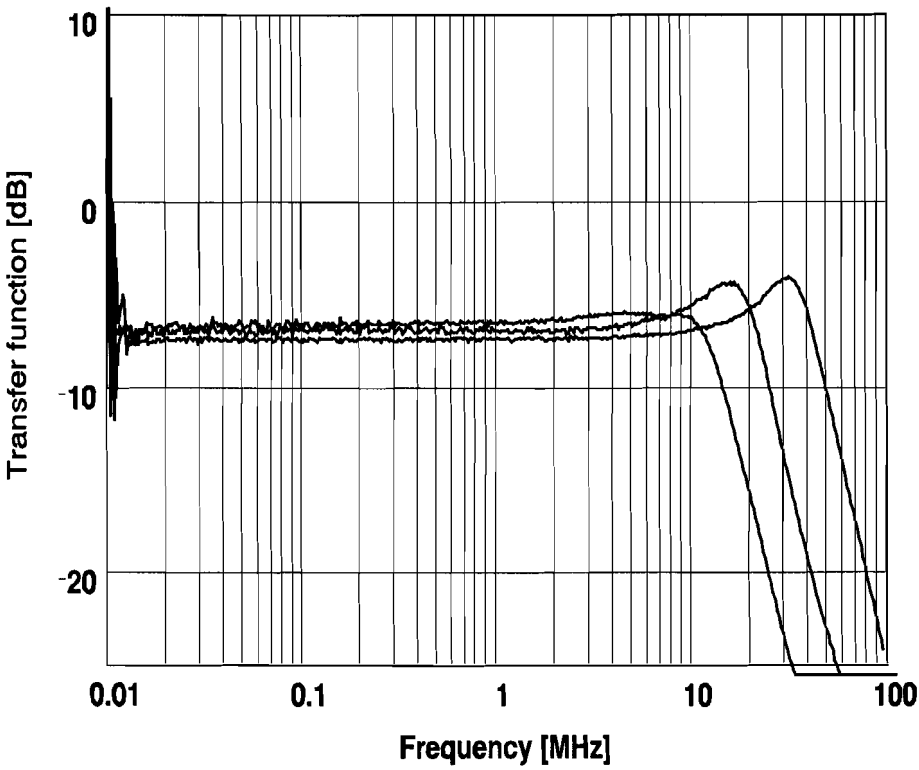

Figure 5.15: *The transfer function H(f) from current (charge) at the output divided by the feedback resistor R for 3 values of the feedback resistor: upper trace (lowest bandwidth) R=34 MΩ, middle trace R=11 MΩ and lower trace (highest bandwidth) R=2.8 MΩ.*

The Noise Electron Density expressed in [e^2/Hz] can be found by correcting the noise spectral density (Figure 5.14) for the transfer function (Figure 5.15) and dividing by the sensitivity ($S=R \cdot f_p \cdot q$). The result is given in Figure 5.16.
The on-chip amplifier used in this experiment had a noise performance of N_C=10 e in a traditional set-up with a matched filter when clocked at f_p=18 MHz and over a bandwidth B_m=5 MHz in which the noise was measured. The new output method gave the following results:

R	N_R
34 MΩ	9.5 e
11 MΩ	18 e
2.8 MΩ	42 e

Taking into account that the comparison is made for an imager clocked at 18 MHz, this is a very good result since it shows that with a simple circuit one can compete with the classical method (9.5 e versus 10 e). At higher clock frequencies the new method improves even more.

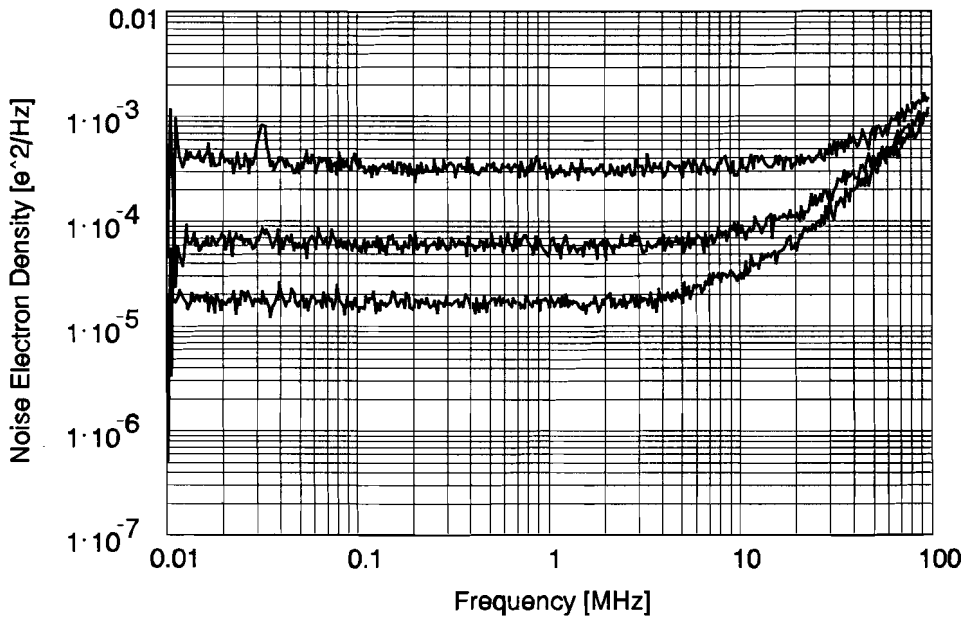

Figure 5.16: *The noise spectral density in [e^2/Hz] for R=34 MΩ (lower trace), R=11 MΩ (middle trace), and R=2.8 MΩ (upper trace).*

5.8 Discussion and conclusions

In the resistive feedback mode old sensing tradition is restored while the benefits of the current approach are retained: a low-noise on-chip amplifier with a floating diffusion detector and an on-chip resistor.

It is a suitable concept for reading out charges at high frequencies and maintaining the same or better signal-to-noise ratio as before without the need for complex signal processing schemes. This can be handy when used in a progressive scan HDTV sensor which needs pixel rates in excess of 72 MHz.

The benefits of using the resistive feedback technique lay in the fact that signal processing is continuous and that one needs no discrete-time filtering. Compare this to Integrate and Dump or Correlated Double Sampling with all their difficulties in pulse generating and timing. The rise and fall times no longer play an important role, nor does the propagation delay of the on-chip amplifier. One may even use up to one full clock time to dump the charge on the floating diffusion detector.

From a subjective point of view this scheme benefits from the triangular shape of the noise spectrum; given an equal objective noise performance for both the traditional readout method with matched filter and resistive feedback mode the latter will be perceived as much better with regard to noise performance.

It has been shown that the signal-to-noise ratio of the resistive feedback mode can be made at least equal to a floating diffusion detector with periodic reset followed by an optimal signal processor.

For a cheap CCD camera the reset FET can be used as an adjustable feedback resistor.

A major drawback is the need for a large resistor value and the fact that one does not have the individual pixel values at ones disposal. Especially in single-CCD colour applications this is a severe problem. Fabricating large resistances also creates problems which have not yet been solved, namely, parasitic capacitances at the detection node and non-linear behaviour.

Appendix A: Procedure to determine the transfer function

To measure the transfer function of the current to voltage conversion a two step method has been applied. This transfer function is needed for the conversion of the noise spectral density into a noise electron density.
First the transfer function from the gate of the current source V_{CS} to the output (Figure A.1) is measured with a network analyzer; it equals

$$\left| \frac{H(f)}{R} \left(1 + j\, 2\, \pi\, R\, C\, f \right) \right| \qquad \textbf{(A1)}$$

This is equivalent to the transfer function for just the noise e_n of the MOS transistor; compare equation (5.12). The pole-zero image of the above function has one zero more than the transfer function H(f) defined in equation (5.7), and is divided by the feedback resistor R. The corner frequency of the zero is very pronounced (Figure A.1) and can be determined well. In Figure (A.1) the transfer function from the current source gate to the output is given for three values of the feedback resistor R. At low frequencies the transfer function is nearly the same for the three resistor values. At higher frequencies the gain increases due to the reduction of the feedback caused by the low-pass character of the feedback resistor R and the input capacitor C (the $2 \cdot \pi \cdot R \cdot C \cdot f$ term of equation (A1)). At even higher frequencies the gain decreases due to the pole of the on-chip amplifier.

The 3 dB point of the additional zero $F_{zero}=(1/(2 \cdot \pi \cdot R \cdot C))$ derived from Figure (A.1) is given in the table below in the third column. The first column is the emitter resistor value (Figure 5.13) that determines the open-loop gain and stability when R changes. The second column is the reset FET channel resistance R adjusted with the V_{RG} setting.

R_e [Ω]	R [MΩ]	F_{zero} [MHz]
13	34	0.294
33	11	0.928
110	2.8	3.67

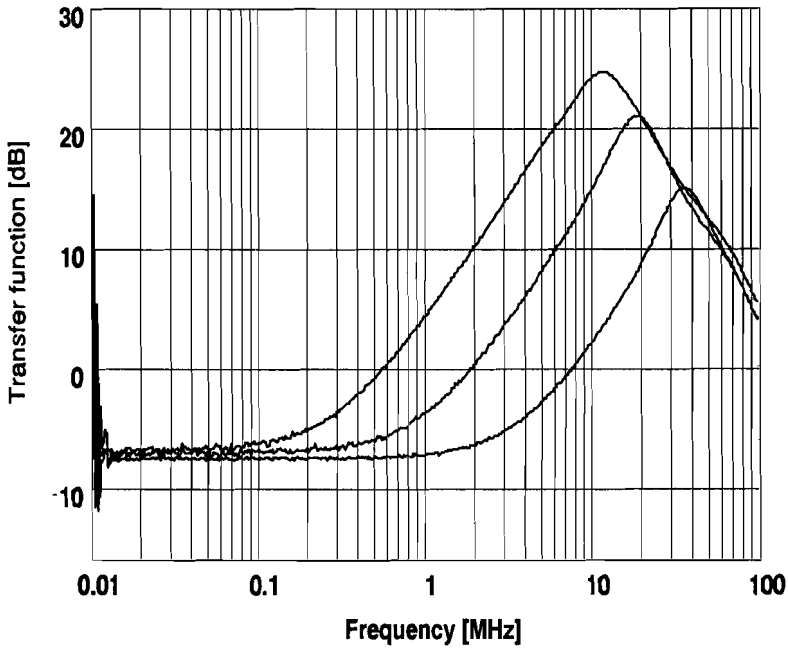

Figure A.1: *The transfer function from the current source gate to the output for 3 values of the feedback resistor: R=34 MΩ, R=11 MΩ and R=2.8 MΩ*

The transfer function H(f) for the current-to-voltage conversion divided by the feedback resistor R is given in Figure 5.15. This figure is calculated from Figure A.1 by removing the zero in the transfer function.
During the measurements the output is terminated by 50 Ω from the network analyzer and the transfer function has an additional 6 dB attenuation.

References

[1] W.Kosonocky and J.Carnes, *"Charge-Coupled Digital Circuits"*, IEEE Journal of Solid-State Circuits, vol. SC-6, No. 5, October 1971, pp 314-326

[2] J.Carnes, W.Kosonocky, *"Noise sources in Charge-Coupled Devices"*, RCA Rev. 33, 327-343; 1972.

[3] A.Theuwissen. *Solid-State Imaging with Charge-Coupled Devices.* Kluwer Academic Publishers 1995; ISBN 0-7923-3456-6.

[4] J.Hynecek, *"High-Resolution 8-mm CCD Image Sensor with Correlated Clamp Sample and Hold Charge Detection Circuit."* IEEE Trans. Electron Devices, vol. ED-33, no. 6, pp. 850-862, June 1986.

[5] H.Wey and W.Guggenbühl, *"An improved Correlated Double Sampling Circuit for low Noise Charge-Coupled Devices"*, IEEE Trans. on Circuits and Systems, Vol. 37, No. 12, december 1990, pp. 1559-1565.

[6] M.Ohbo, I.Akiyama, T.Tanaka, *"A New Noise Suppression Method for High-Definition CCD Cameras"*. IEEE Trans. Consumer Electronics., vol. CE-35, no. 3, pp. 368-374, August 1989.

[7] Chapter 4 this thesis.

[8] M.Tompsett and E.Zimany, *"Use of Charge-Coupled Devices for Delaying Analog Signals"*, IEEE Journal of Solid-State Circuits, vol. SC-8, No.2 , April 1973.

[9] E.Roks, P.Centen, J.Bosiers, W.Huinink, *"The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD Image Sensors"*. IEEE Trans. Electron Devices, vol. ED-43, no. 9, pp. 1583-1591, September 1996.

[10] R.Brewer, *"A Low Noise CCD Output Amplifier"*, Technical Digest IEDM79, pp. 610-612, Washington DC, December 3-5, 1979.

[11] G.Hobson, R.Longstone and R.Tozer, *"Dual-gate charge sensing in charge-coupled devices."* IEEE Trans. Electron Devices, vol. ED-2, no. 6, pp. 207-214, November 1978.

[12] Y.Matsunaga, *"A High Sensitivity Output Amplifier For CCD Image Sensor"*, Technical Digest IEDM87, pp. 116-119, Washington DC, December 6-9, 1987

[13] A.Theuwissen, H.Peek, P.Centen, R.Boesten, J.Cox, P.Hartog, A.Koskhoorn, H.v.Kuijk, B.O'Dwyer, J.Oppers, F.Vledder. *"A 2.2 Mpixel FT-CCD imager, according to the Eureka HDTV-standard"*. Technical Digest IEDM91, pp. 167-170, Washington DC, December 8-11, 1991.

[14] J.Rotte, *"Resetruis vrije uitleesmode voor een floating diffusion detector"*. B.Sc. thesis, May 19, 1995, Internal report Philips.

LIST OF SYMBOLS

Symbol	Description	Unit
A		
A	Scaling constant of the total capacitance C_{tot}	$F \cdot cm^{-2}$
A	Overall gain of the on-chip amplifier	
A_{10}	DC gain of the first source follower stage	
A_{20}	DC gain of the second source follower stage	
A_{30}	DC gain of the third source follower stage	
A_{RD}	DC gain from reset drain to output	
A_{CS}	DC gain from current source gate to output	
A_{tot}	DC gain of the on-chip amplifier	
α_H	Hooge factor for the 1/f noise	
α	Factor for the thermal noise of a MOS transistor	
a	Capacitance per unit length of the source diffusion region	$F \cdot cm^{-1}$
B		
B	Scaling constant of the total capacitance C_{tot}	$F \cdot cm^{-1}$
B_m	Bandwidth in which the noise is measured	Hz

B_n	Noise bandwidth	Hz
ß	g_{mc}/g_{m1}; cascode gain from the gate of the current source M_{c1} to the source of the detection node transistor M_1	

C

C	Scaling constant of the total capacitance C_{tot}	$F \cdot cm^{-1}$
C_1	Capacitance between the gate of the detection node transistor and ground	F
C_2	Capacitance between the gate and the source of the detection node transistor	F
C_{det}	Detection node capacitance; $C_{det}=C_1+(1-A_{10})\cdot C_2$	F
C_{tot},C_t	Total capacitance of the detection node; $C_{tot}=C_1+C_2$	F
C_{gs}	Transistor gate-to-source capacitance.	F
C_{fixed}	Stray capacitance, independent of the geometry of the detection node transistor.	F
C_L	External load capacitance	F
C_o	Load capacitance of/to the first stage.	F
CDS	Correlated Double Sampling	
$C_□$	Capacitance per unit square	$F \cdot cm^{-2}$
C_{load}	Load capacitance	F
C_g	Gate capacitance $W \cdot L \cdot C_□$	F

D

D	Scaling constant of the total capacitance C_{tot}	F
dU_o	Change in output voltage due to a change in charge	V
δ_{rs}	Duty cycle of the reset hold level	
δ_v	Duty cycle of the charge signal	

E

e_n	Noise voltage	$V \cdot Hz^{-½}$
e_{n1}	Noise voltage of the first source follower M_1	$V \cdot Hz^{-½}$
e_{nc}	Noise voltage of the first current source M_{c1}	$V \cdot Hz^{-½}$
ε_0	Permittivity in vacuum	$8.85 \cdot 10^{-14}$ $F \cdot cm^{-1}$
ε_i	Permittivity in silicon	$10.5 \cdot 10^{-13}$ $F \cdot cm^{-1}$
ε_{ox}	Permittivity in silicon dioxide	$3.45 \cdot 10^{-13}$ $F \cdot cm^{-1}$
η	Voltage noise spectral density	$V^2 \cdot Hz^{-1}$

η_e	Efficiency, caused by SP-stripes, poly, collection depth, etc.	

F

F_c	1/f cross-over frequency	Hz
F_T	Transit frequency of a MOS transistor	Hz
F_3(on)	3 dB roll off frequency in the reset FET on-state	Hz
F_3(off)	3 dB roll off frequency in the reset FET off-state	Hz
f_p	Pixel frequency	Hz
f	Frequency	Hz
FD	Floating Diffusion (region)	
F_{3dB}	Bandwidth	Hz
F_n	Noise efficiency factor	

G

g_m	Transconductance	Ω^{-1}
g_{m1}	Transconductance of the detection node MOS transistor	Ω^{-1}
g_{mc}	Transconductance of the first source follower's current source MOS transistor	Ω^{-1}
g_{mc1}	Transconductance of the first source follower's current source MOS transistor	Ω^{-1}
g_b	Backbias transconductance	Ω^{-1}
G	Gain of the off-chip feedback amplifier	
$g_v(t)$	Waveform of the charge signal	
$g_r(t)$	Waveform of the reset noise	
$G_v(f)$	Fourier transform of the charge signal waveform	
$G_r(f)$	Fourier transform of the reset noise waveform	

H

h(t)	Impulse response of a filter
H(t)	Fourier transform of a filter with impulse response h(t)
δH	Variation of H
$H_{opt}(f)$	Matched filter

I

I	Bias current of the detection node MOS transistor M_1	
i_i	Detection node input current, time domain	
I_i	Fourier transform of i_i	
i_n	Noise current	$A \cdot Hz^{-1/2}$
i_{n1}	Noise current of the detection node MOS transistor M_1	$A \cdot Hz^{-1/2}$
i_{nc}	Noise current of the current source MOS transistor M_{c1}	$A \cdot Hz^{-1/2}$
I_{RD}	Reset drain current	A
ISI	Inter-Symbol Interference	

J

K

k	Boltzmann's constant	$1.38 \cdot 10^{-23}\ J \cdot K^{-1}$

L

L_1	Channel length of the detection node MOS transistor M_1	µm
L_c	Channel length of the current source MOS transistor M_{c1}	µm
L	Channel length	µm
δL	Channel length shortening	µm
L	Coil with self-inductance L	H

M

M	Figure of merit for a CCD-signal processor	
M_1	Detection node MOS transistor	
M_2	Second source follower MOS transistor	
M_3	Third source follower MOS transistor	
M_{c1}	First current source MOS transistor	
μ	Mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$
μ_n	Electron mobility	150-1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$
μ_p	Hole mobility	50-500 $cm^2 \cdot V^{-1} \cdot s^{-1}$
MTF	Modulation Transfer Function	
M_m	Figure of merit for m outputs multiplexed into 1	

M_{clamp}	Figure of merit for clamp processing	
M_{white}	White noise figure of merit for a signal processor	
M_{opt}	Lower bound for the figure of merit	

N

N	Number of electrons in a charge packet	
NED	Noise Electron Density of the on-chip amplifier	$e^2 \cdot Hz^{-1}$
NED_C	Noise Electron Density after signal processing	$e^2 \cdot Hz^{-1}$
NED_R	Noise Electron Density for resistive feedback	$e^2 \cdot Hz^{-1}$
n(t)	Actual noise voltage	V
N_{rr}	Reset noise	e
N_{proc}	Noise after CCD signal processing	e^2
N_C	Number of noise electrons for classical FD-readout	e
N_R	Number of noise electrons for resistive feedback readout	e
N_∞	Number of noise electrons in the full bandwidth	e

O

ω	Angular frequency; $2 \cdot \pi \cdot f$	rad^{-1}

P

P	Average number of photons incident at the imager surface	

Q

q	Electron charge	$1.6 \cdot 10^{-19}$ A·s
QE	Overall quantum efficiency: $\eta_e \cdot QE_i$	
QE_i	Interacting quantum efficiency; number of electrons per photon	

R

R	Resistance of the reset FET channel	Ω
R	Feedback resistor	Ω
R_L	External load resistance	Ω
R_o	Load resistance of/to the first stage	Ω
R_{on}	Reset FET channel ON-resistance	Ω

R_n	Equivalent noise resistance of a MOS transistor	Ω
R_{eq}	Equivalent noise resistance in general	Ω
R_e	Resistor determining the gain of a CE stage	Ω
r(t)	Reset noise	V
R_{rr}	Normalized reset noise value	
$R_{nn}(x)$	Auto-correlation function	
R_k	Amplitude of the reset noise of the k-th pixel	V
$r_h(t)$	Reset noise after filtering with filter h(t)	
R_s	Series resistor	Ω
R_p	Parallel resistor	Ω

S

S	Sensitivity, conversion gain of the detection node $S=A_{10}\cdot q/C_{det}$	$V\cdot e^{-1}$
S_{vv}	Voltage noise spectral density	$V^2\cdot Hz^{-1}$
s	Laplace variable	
S_{ee}	Voltage noise spectral density of on-chip amplifier	$V^2\cdot Hz^{-1}$
S	Sensitivity	V/e^{-1}
S_{nn}	Noise spectral density, noise electron density	$e^2\cdot Hz^{-1}$

T

T	Temperature; lattice temperature	K
T_e	Electron temperature	K
Θ_n	C_{tot}/C_{det}, determines the bandwidth	
τ	Time constant	s
T_p	Duration of one pixel	s
T_r	Time during which the reset FET is off	s
T_{rs}	Duration of reset hold level; T_r-T_v	s
T_v	Duration of charge signal	s
T_x	Time interval	s

U

u_i	Detection node voltage; time domain
U_i	Fourier transform of u_i
u_o	First stage output voltage; time domain

U_o	Fourier transform of u_o	
u_{cs}	Test signal at the current source gate; time domain	
U_{cs}	Fourier transform of u_{cs}	

V

V_{DD}	Bias voltage of the on-chip amplifier	V
V_{RD}	Bias voltage of the drain of the reset FET	V
V_{CS}	Bias voltage of the gate of the current source MOS transistor	V
V_o	Quiescent output voltage when the detection node is clamped to V_{RD}	V
dV_{out}	Change in output voltage	V
dV_{RD}	Change in bias voltage of the drain of the reset FET	V
dV_{CS}	Change in bias voltage of the current source gate	V
v(t)	Change in output voltage due to a change in charge, 'charge signal'	V
ΔV_{rr}	Fluctuation in detection voltage due to reset	V
v(t)	Charge signal, video signal	
$v_h(t)$	Charge signal after filtering with h(t)	
V_k	Charge signal amplitude of the k-th pixel	
S_{vv}	Voltage noise spectral density	$V^2 \cdot Hz^{-1}$

W

W_1	Channel width of the first source follower MOS transistor M_1	µm
W_c	Channel width of the current source MOS transistor M_{c1}	µm
W_T	A typical channel width used to normalize the actual channel width of the detection node MOS transistor	µm
w	W_1/W_T; normalized detection node MOS transistor channel width	
W_{opt}	Optimal channel width of the detection node MOS transistor	µm

X

X_{opt}	Optimal value of soft clamp timing	

Y

Z

ZOH Zero Order Hold circuit

FUNCTIONS

Dirac impulse function

$$\forall_{\epsilon > 0} \int_{-\epsilon}^{\epsilon} f(x)\ \delta(x)\ dx = f(0)$$

Rectangle function

$$RECT(x) = \begin{cases} 1 & for\ |x| < \frac{1}{2} \\ \frac{1}{2} & for\ |x| = \frac{1}{2} \\ 0 & for\ |x| > \frac{1}{2} \end{cases}$$

Triangle function

$$TRIANGLE(x) = \begin{cases} 1 - |x| & for\ |x| \leq 1 \\ 0 & for\ |x| > 1 \end{cases}$$

The sinc function

$$sinc(x) = \frac{\sin(\pi\ x)}{\pi\ x}$$

The sign function

$$SGN(x) = \begin{array}{ll} 1 & for\ x>0 \\ 0 & for\ x=0 \\ -1 & for\ x<0 \end{array}$$

Ensemble averaging

$$<H(x)> = \int_{-\infty}^{\infty} H(x)\ p(x)\ dx$$

with

$$\int_{-\infty}^{\infty} p(x)dx = 1$$

Time averaging

$$\overline{f(t)} = Lim_{T\to\infty} \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t)dt$$

A Fourier transform pair

$$f(t) \leftrightarrow F(f)$$

Convolution of two functions

$$g(t) \otimes h(t) = \int_{-\infty}^{\infty} g(x)\, h(t-x)dx$$

The complex conjugate of G(f)

$$G^*(f)$$

The sinus integral

$$Si(z) = \int_0^z \frac{\sin(t)}{t}\, dt$$

The cosinus integral

$$Ci(z)=\gamma_e + \ln(z) + \int_0^z \frac{\cos(t) - 1}{t}\, dt \qquad (|arg(z)<\pi|)$$

Eulers constant

$$\gamma_e = 0.57721$$

SUMMARY

This Ph.D. thesis discusses several theoretical aspects behind critical design parameters of the on-chip amplifier of CCD imagers and, more generally, of the signal processing. Furthermore, methods are developed to determine these parameters experimentally.

The signal chain of a CCD imager consists of:

- A matrix of image cells which converts a fraction of the impinging photons into electron-hole pairs. Usually the electrons are gathered and the holes are drained off. The electrons that belong to one image cell are bundled together into what is called a charge packet.
- A CCD channel to transport the charge packet towards the detection node and output.
- An output circuit consisting of a reset FET with floating diffusion region which, together with the first stage of the on-chip amplifier, forms the detection node.
- A detection node where the charge packet is converted into a change in output voltage.
- A signal processor at the output of the on-chip amplifier that filters the CCD signal and is responsible for the signal-to-noise performance, the

resolution (MTF), and the dynamics of the signal.
At the output of the signal processor base band video is available, which is proportional with the light signal.

In **Chapter 2** the on-chip amplifier is analyzed. The importance of the ratio between the total input capacitance and detection node capacitance for the bandwidth is investigated. The detection node capacitance determines the sensitivity (V/e), and the total capacitance determines the noise behaviour. It is shown that the bandwidth of the first stage decreases with a factor equal to the ratio of total capacitance and detection capacitance.
As a result of the noise analysis a more appropriate quantity for the noise (Noise Electron Density) is introduced. It enables the noise optimization of the on-chip amplifier in the absence of the signal processor. The Noise Electron Density is a spectral density instead of an integral quantity. The equivalent number of noise electrons, for that matter, is an integral quantity.
In this chapter it is shown that the noise optimum, determining the dimensions of the detection node transistor, is rather flat. Changing the transistor width by a factor of 2 with respect to the optimal value only deteriorates the noise performance by 0.5 dB.
In addition the validity of the noise optimization model for any type of on-chip amplifier topology (with capacitive detection node), such as source follower and common source configurations is proved.
The gate of the current source that biases the detection node transistor can be used as a test signal input. A method is developed and used to measure quite easily the ratio between total capacitance and detection capacitance. This allows one to determine the total capacitance of the detection node.
Applying these methods results in the determination of the design parameters. The use of the design parameters and application of the noise/bandwidth model results in an improved on-chip amplifier. It was possible to determine the contribution of the various layout elements to the noise and bandwidth performance. The design of a low noise HDTV on-chip amplifier with a bandwidth of 158 MHz has been carried out successfully using the above model.

In **Chapter 3** the effect of using surface and buried channel MOSFETs as the detection node transistor is studied for the sensitivity, the bandwidth, the 1/f noise, and the thermal noise performance. The dimensionless thermal noise factor, which is 2/3 for an ideal MOS transistor, for both surface and buried channel MOS transistors has been determined experimentally. The above factor increases rapidly with increasing current density. The value of the noise ideality

factor for a surface transistor is about two times higher than for the buried channel type. The deterioration in noise performance of the on-chip amplifier, due to a deviation from the 2/3 value, can be as high as 5 dB, depending on bias current, channel width and channel length.
It is shown that the optimum dimensions and bias conditions for the detection node transistor for noise do not coincide with the maximum bandwidth. The 1/f noise Hooge factor has also been determined for both types of MOS transistors. It is shown that the CCD process technology has evolved to such a level that one can use surface MOS transistors in the first stage of the on-chip amplifier without suffering a drawback in noise performance. One even gains in bandwidth.

In **Chapter 4** a matched filter for CCD signals is derived, the model includes the effects of reset noise. Knowing the matched filter, a figure of merit for the signal processor of CCD signals is derived. A lower bound for the figure of merit is established and some examples of its use are given. In many cases this figure of merit is only determined by sum of two ratios, one between the pixel period time and the duration of the reset hold level and one between the pixel period time and the duration of the video in one pixel. It is shown that the noise performance of a well designed imaging chain is given by the product of the noise spectral density of the on-chip amplifier, the figure of merit of the signal processor and the clock frequency. It is also shown that for clock frequencies in excess of 10 times the 1/f noise corner frequency of the on-chip amplifier the behaviour can be predicted well by taking into account the white noise only. The figure of merit can be applied to any type of CCD signal processor. A new method to emulate an integrator in a passive way is analyzed. Its figure of merit is very close to the theoretical lower bound.

In **Chapter 5** a novel way of using a floating diffusion detector has been discussed. The stream of pixels is regarded as a current instead of a series of individual charge packets. In fact it is a way of reading out the imager without generating reset noise. Criteria are established that determine the noise performance of this readout scheme. Basically one can arrive at equal or better noise performance than with the classical circuit of a floating diffusion detector with destructive readout followed by correlated double sampling. The main problem for a practical implementation is the on-chip feedback resistor which needs a value in excess of several tens of MΩ. A practical implementation is given in which the reset FET acts as a (non-lineair) feedback resistor.

SAMENVATTING

In dit proefschrift worden de theoretische aspecten van enkele kritische ontwerp-parameters van CCD on-chip versterkers en de signaalverwerking besproken, geanalyseerd en met experimenten ondersteund. Daarnaast worden er methoden geïntroduceerd om die parameters experimenteel te bepalen.

Het signaalpad van een CCD imager bestaat uit:

- Een matrix van lichtgevoelige cellen die een deel van de opvallende fotonen omzet in elektron-gat paren. Gewoonlijk worden de elektronen verzameld en worden de gaten via het substraat afgevoerd. De elektronen, die in één lichtgevoelige cel worden gegenereerd, worden opgeslagen als één ladingspakketje.
- Een CCD-kanaal om het ladingspakketje in de richting van het detectie-knooppunt en de uitgang te transporteren.
- Een uitgangscircuit, bestaande uit een reset-transistor met een zwevend diffusie gebied, dat tezamen met de eerste trap van de on-chip versterker het detectieknooppunt vormt.
- Het detectieknooppunt converteert het ladingspakketje in een spannings-zwaai op de uitgang van de on-chip versterker.
- Dit uitgangssignaal is de input voor de signaal-processor. De signaal-

processor zal het CCD-signaal filteren en bepaalt het signaal-ruis getal, de resolutie (MTF) en de dynamiek van het signaal.
Op de uitgang van de signaalprocessor is basisband-video beschikbaar.

In **Hoofdstuk 2** wordt de on-chip versterker geanalyseerd. Het belang van de verhouding tussen de totale capaciteit rond het detectieknooppunt en de detectieknooppunt-capaciteit voor de bandbreedte wordt bediscussieerd. De detectieknooppunt-capaciteit bepaalt de gevoeligheid (V/e) en de totale detectieknooppunt-capaciteit het ruisgedrag.
Aangetoond wordt dat de bandbreedte van de eerste trap wordt verlaagd met een factor gelijk aan de verhouding tussen de totale capaciteit en detectieknooppunt-capaciteit.
Als resultaat van de ruis analyse wordt de Noise Electron Density als een parameter voor ruisberekeningen en optimalisatie geïntroduceerd. Het staat ruis optimalisatie toe van de on-chip versterker zonder dat daarbij de signaalprocessor betrokken hoeft te zijn. De Noise Electron Density is een spectrale dichtheid.
Aangetoond wordt dat het ruisoptimum, dat de afmetingen van de detectie transistor bepaalt, vlak is. De ruisprestatie verslechterd met 0.5 dB als de breedte van de transistor verdubbeld of gehalveerd wordt ten opzichte van de optimale waarde.
Ook wordt de geldigheid van het ontwikkelde ruis model aangetoond voor elke on-chip versterker topologie met een capacitief detectieknooppunt.
De gate van de stroombron, die de instelstroom door de detectie transistor bepaalt, kan als een testingang gebruikt worden. Een methode wordt ontwikkeld en gebruikt om de verhouding tussen de totale detectieknooppunt-capaciteit en detectieknooppunt-capaciteit te kunnen meten. Samen met de gemeten gevoeligheid kan dan de totale detectieknooppunt-capaciteit bepaald worden.
De toepassing van de ontwikkelde meetmethoden samen met het ruis/bandbreedte model heeft geresulteerd in een verbeterde on-chip versterker. Het was mogelijk om de bijdrage van diverse onderdelen van de layout tot de ruis en de bandbreedte te bepalen. Het ontwerp van een lage ruis en hoge bandbreedte on-chip versterker voor HDTV imagers is succesvol voltooid met een verhoging van de bandbreedte van 15 MHz naar 158 MHz en met een ruisvloer die met 8 dB verlaagd is ten opzichte van zijn voorgangers.

In **Hoofdstuk 3** worden de effecten bestudeerd die samenhangen met het gebruik van zowel oppervlakte- als begravenkanaal transistoren in het detectieknooppunt. De bestudeerde effecten zijn de verschillen in 1/f-ruis en thermische ruis, de bandbreedte en de gevoeligheid.

De thermische ruisfactor, die voor een ideale MOS transistor 2/3 is, is voor deze transistoren experimenteel bepaald en gemodelleerd. De ruisfactor neemt snel toe bij toename van de stroomdichtheid in het kanaal van de detectie transistor. De waarde van de thermische ruisfactor voor een oppervlakte transistor is ongeveer twee maal zo hoog dan voor een begravenkanaal type. De achteruitgang in ruisprestatie tengevolge van een van 2/3 afwijkende waarde, kan wel 5 dB bedragen afhankelijk van instelstroom, kanaal breedte en kanaal lengte.
Aangetoond wordt, dat een optimale dimensionering van de detectie transistor om een lage ruisspanning te bereiken, niet samenvalt met een maximale bandbreedte. Van beide transistor typen is de Hooge-factor, welke een maat is voor de grootte van de 1/f-ruis, bepaald. In dit hoofdstuk wordt aangetoond dat de CCD-procestechnologie zo ver ontwikkeld is dat ook oppervlakte-transistoren gebruikt kunnen worden in het detectieknooppunt zonder een verslechtering van het ruisgedrag. Men gaat er zelfs op vooruit in bandbreedte.

In **Hoofdstuk 4** wordt het optimale filter voor CCD-signalen bepaald met behulp van variatie-rekening. Aan de hand van het optimale filter is een prestatiegetal voor de signaal-processor van CDD-signalen afgeleid. De kracht van het prestatiegetal is dat er een ondergrens voor afgeleid kan worden.
In veel gevallen wordt dit prestatiegetal bepaald door de som van twee verhoudingsgetallen: een is de verhouding tussen de pixel periodetijd en de duur van het resetreferentie niveau en de andere is de verhouding tussen de pixel periodetijd en de duur van het video in één pixel.
Verder worden er enkele voorbeelden gegeven van het gebruik van dit prestatiegetal. Aangetoond wordt dat het ruis gedrag van een imaging keten wordt beschreven door het produkt van de ruis van de on-chip versterker en het prestatie getal van de signaal-processor en de klokfrequentie. Ook wordt aangetoond dat voor klokfrequenties hoger dan 10 keer de 1/f-kantel- frequentie van de on-chip versterker, het ruisgedrag van de signaal-processor voorspeld kan worden door een vlak ruisspectrum te gebruiken. Het prestatiegetal kan voor elk type CCD signaal-processor gebruikt worden.
Een nieuwe methode wordt gegeven om op een passieve manier een integrator na te bootsen, die de mogelijkheid biedt zeer dicht bij de theoretische ruisgrens te komen.

In **Hoofdstuk 5** wordt een nieuwe methode bediscussieerd om de zwevende diffusie detector te gebruiken. De ladingspakketjes worden dan opgevat als een elektrische stroom in plaats van een serie individuele ladingspakketjes. De stroom wordt via een weerstand omgezet in een spanning, dit in tegenstelling tot de benadering waarbij ladingspakketjes via een capaciteit in spanning omgezet

worden. De stroombenadering leidt tot een uitleesmethode, waarin geen reset-ruis gegenereerd wordt.
In dit hoofdstuk worden criteria vastgesteld die de ruisprestatie bepalen. In essentie kan men gelijke tot betere ruisgetallen bereiken met deze criteria dan met de klassieke wijze van het uitlezen van de zwevende diffusie detector, die gevolgd wordt door een Correlated Double Sampler. Het grootste probleem voor een praktische implementatie is de realisatie van de on-chip terugkoppel-weerstand, die groter moet zijn dan vele MΩ en nauwelijks extra capaciteit mag toevoegen. Er wordt een implementatie gegeven, waarin de reset-FET gebruikt wordt als (niet lineaire) terugkoppel weerstand.

DANKWOORD

Welke wending je leven neemt, wordt op diverse momenten mede beïnvloed door mensen die in je geloven, die bereid zijn zich voor je in te zetten en die je iets gunnen. Zonder anderen daarbij tekort te willen doen, betrek ik de volgende personen met name in mijn dank voor hun bijdrage aan het tot stand komen van dit proefschrift:

- De heren Eugène Peeters en Sjef van Mook waren mijn leraren van het eerste uur. Zij geloofden in mij en hebben zich in vroegere jaren ingezet om mijn persoonlijke ontplooiing in technische richting mogelijk te maken.
- Het was dr.ir. Edwin Roks die mij de mogelijkheid bood een gemeenschappelijke publikatie te schrijven waaruit hoofdstuk 3 ontstaan is. Zijn collegiale houding, gedurende de jaren van samenwerking op het gebied van CCD on-chip versterkers, is spreekwoordelijk.
- Mijn co-promotor dr.ir. Albert Theuwissen heeft vele CCD on-chip-versterkers voor mij ontworpen. Het onderzoek aan deze versterkers vormde de basis voor mijn eerste CCD publikatie. Zijn kritische commentaren op de concepten van dit proefschrift, hebben bijgedragen tot de leesbaarheid daarvan. *Arigato gozaimasu!*
- Het was een inspirerende ervaring om prof.dr. Frans Klaassen als eerste

promotor toegewezen te krijgen, omdat ik al zijn publikaties over ruis reeds gelezen had. Uit het in korte tijd kunnen leveren van goede en uitgebreide commentaren blijkt zijn jarenlange ervaring.

- De precisie waarmee mijn tweede promotor prof.dr. Theo Kleinpenning het proefschrift heeft becommentarieerd is de consistentheid en leesbaarheid ten goede gekomen. *Check-check double check!*
- Dr. Greg Kreider, "A professional courtesy", zei hij, kwam in korte tijd met de correcties, gelardeerd met grapjes. *Geen streepjes meer!*
- Drs. Theo Peek verlichtte 'n laatste loodje!
- Mijn vrouw en maatje, Peti Stevens, wil ik in het zonnetje zetten. Zij heeft mij altijd onvoorwaardelijk gesteund. Mijn gezelschap heeft ze vaak moeten ontberen: òf tengevolge van de claim die Philips Digital Video Systems op mij legde òf tengevolge van het schrijven van dit proefschrift. *Promoveren doe je met z'n tweeën!*

Daarnaast wil ik de volgende personen bedanken:

- Ing. Herman Peek en ing. Daniël Verbugt voor de processing en het ontwerpen van de structuren gebruikt in hoofdstuk 3.
- Ing. Jeroen Rotte, voor zijn bijdrage aan het tot stand komen van het experimentele deel uit hoofdstuk 5.
- Ing. Frans Vledder, ing. Marcel Roosen en ing. Wim Haar voor het ontwerpen en bouwen van de diverse ruismeetprinten.
- Ir. Jan Bosiers, voor de vele test-structuren die hij in de loop der jaren ontworpen heeft.
- Ing. Mike Stekelenburg en ing. Gerard van Beijsterveld voor de vele discussies en meetexpedities op het gebied van CCD on-chip versterkers en CCD signaal processing.

Verder wil ik de volgende personen noemen omdat ze het toeval een handje hebben geholpen:

- Ir. Max Collet, omdat hij mij de mogelijkheid heeft geboden om in zijn groep als gastonderzoeker werkzaam te kunnen zijn. Deze is later overgegaan in de groep Theuwissen (Philips Imaging Technology).
- Dr.ir. Frans de Leeuw en ir. Henk Blom van Philips Digital Video Systems Breda, doordat zij mij als gastonderzoeker op het Natuurkundig Laboratorium van Philips te Eindhoven werkzaam lieten zijn.

Tot slot denk ik met veel genoegen terug aan de samenwerking met de leden van Philips Imaging Technology en van Philips Digital Video Systems Breda.

BIOGRAPHY

Peter G.M. Centen was born in Goirle, The Netherlands, on October 19, 1952. In 1976 he received the B.Sc. degree in electrical engineering from the College of Advanced Technology in Den Bosch, The Netherlands. He specialized in telecommunications. In 1983 he received a Cum Laude M.Sc. degree at the faculty of Electrical Engineering of the Eindhoven University of Technology, The Netherlands. During his M.Sc. course he received an award for 'extraordinary achievements'. He served for 3 years as a president of a semi professional foundation (StIK). This foundation focuses on stimulating behavioural awareness within the university. Early 1984 he became an assistant researcher to finish a paper on a Variational Principle for the Equilibrium Conditions for a MHD-Plasma.

Peter kicked off his career when he joined Philips Digital Video Systems in Breda, The Netherlands. He carried out research on optimal signal processing for CCD imagers. As a guest researcher at the Philips Research Laboratories in Eindhoven, he devoted his attention to noise reduction and high speed operation of the CCD imager output circuitry including the reduction of hot-electrons in the on-chip amplifier. He designed a vertical npn bipolar and a JFET-floating diffusion in the CCD process. He introduced a new isolation between MOS transistors of the on-chip amplifier which enabled a compact design. He also

conducted many video image simulations for the HDTV imager to optimize for MTF and Aliasing behaviour.
For many years now he is involved in the development of HDTV camera's and switchable SDTV camera's. He was one of the co-inventors of Dynamic Pixel Management (DPM) and founder of the optical filtering method using DPM. At present he is a groupleader in the camera development department of Philips Digital Video Systems and responsible for the implementation of CCDs in professional broadcast camera's.

From 1967 onwards he was a member of the Dutch association for rocket research (NERO) for 20 years. As such he participated three times, with success, in the Young Scientists and Inventors contest with projects involving telemetry in rockets and in launch control. For conducting telemetry experiments he holds a radio amateur licence (PA0PGM) since 1974.

Since 1992 he is a teacher at the Philips Centre for Technical Training for the CCD imaging workshop.

In 1991 he became a member of the IEEE Electron Devices Society, the IEEE Consumer Electronics Society and the IEEE Solid-State Circuits Society.

LIST OF PUBLICATIONS

[1] P.Centen, M.Weenink and W.Schuurman. *Minimum energy equilibrium of a force-free plasma with a free boundary.* Proceedings of the International Conference on Plasma Physics 1984, Vol. 1, pp 9.

[2] P.Centen, M.Weenink and W.Schuurman. *Minimum Energy Principle for a Free-Boundary Force-FreePlasma,* Plasma Physics and Controlled Fusion, Vol.28, No. 1B, pp. 347-355, 1986.

[3] P.Centen. *CCD On-Chip Amplifiers: Noise Performance versus MOS transistor Dimensions.* IEEE Trans. Electron Devices. Vol. ED-38, No. 5, pp. 1206-1216, May 1991.

[4] P.Centen. *Noise Optimisation of CCD on-chip amplifiers.* 17th International Television Symposium Montreux, pp.466-496, June 1991.

[5] P.Centen. *FT5 HS: New High Sensitivity Frame Transfer Sensor.* 133th SMPTE L.A. 1991, technical session.

[6] A.Theuwissen, H.Peek, P.Centen, R.Boesten, J.Cox, P.Hartog, A.Koskhoorn, H. van Kuijk, B.O'Dwyer, J.Oppers, F.Vledder. *A 2.2 Mpixel FT-CCD imager, according to the Eureka HDTV-standard.* IEDM Tech. Dig. 1991 pp. 167-170.

[7] P.Centen. *The angle of perception.* TV technology, April 1992, pp. 7-25.

[8] A.Theuwissen, H.Peek, P.Centen, M. van de Steeg, R.Boesten, P.Hartog, A.Kokshoorn, E.de Koning, J.Oppers, F.Vledder. *HDTV IMAGE SENSOR: the pixel structure.* Proceedings of the International Broadcast Convention 1992, pp 488-491.

[9] E.Roks, P.Centen, L.Sanakaranarayanan, J.Slotboom, J.Bosiers, W.-Huinink. *A Bipolar Floating base Detector (FBD) For CCD Image Sensors.*, Technical Digest IEDM92, pp. 109-112, San Francisco, December 13-16, 1992.

[10] P.Centen. *A Reset Noise Free High-Speed Readout Mode for a Floating-Diffusion Detector with Resistive Feedback.* IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, June 9-11, 1993.

[11] M. van de Steeg, R.Boesten, P.Centen, P.Hartog, A.Koskhoorn, E. de Koning, J.Oppers, H.Peek, A.Theuwissen, F.Vledder. *CCD Imagers for HDTV.* The Journal of Photographic Science, Vol. 41, No.3, 1993, pp. 117-118.

[12] A.Theuwissen, H.Peek, M. van de Steeg, R.Boesten, P.Hartog, A.Kokshoorn, E. de Koning, J.Oppers, F.Vledder, P.Centen, H.Blom, and W.Haar. *A 2.2 M pixel FT-CCD Imager According to the Eureka HDTV standard.* IEEE Trans. Electron Devices. Vol. ED-40, No. 9, pp. 1621-1629, September 1993.

[13] E.Roks, J.Bisschop, P.Centen, L.Sankaranarayanan. *Theory and Modelling of the Floating-Surface Detector: An Enhanced CCD Output Structure.* Philips Journal of Research, Vol. 48. No. 3, 1994, pp. 233-260.

[14] P.Centen. *A Reset Noise Free High-Speed Readout Mode for a Floating-Diffusion Detector with Resistive Feedback.* Philips Journal of Research, Vol. 48. No. 3, 1994, pp. 271-280.

[15] E.Roks, P.Centen, L.Sanakaranarayanan, J.Slotboom, J.Bosiers, W.Huinink. *A Bipolar Floating-Base Charge-Detector Used as CCD Output Structure.* Philips Journal of Research, Vol. 48. No. 3 1994, pp. 261-269.

[16] P.Centen, H.Stoldt, A.Theuwissen, H.Peek, W.Huinink, L.Sankaranarayanan, A.Kleimann, G.Pine, M.Stekelenburg, A.Mierop, F.Vledder, D.Verbugt, J.Oppers, P.Opmeer: *Aspect Ratio switching with equal horizontal pixel count.*, Technical Papers International Broadcast Convention, pp 1-7, Amsterdam, September 1994.

[17] J.Blankevoort, H.Blom, P.Brouwer, P.Centen, B. van de Herik, R.Koppe, A.Moelands, J. van Rooy, F.Stok and A.Theuwissen. *A High-Performance, Full Bandwidth HDTV Camera Applying the First 2.2 Million Pixel Frame Transfer CCD Sensor.* SMPTE Journal, Vol. 103, No. 5, 1994, pp. 319-329.

[18] E.Roks, A.Theuwissen, H.Peek, M. van de Steeg, P.Centen, J.Bosiers, D.Verbugt, E. de Koning. *A Low-Noise, High-Sensitive, 1", 2.2 Mpixel FT-CCD Imager for High-Definition applications.* Proc. Workshop Dana-Point 1995.

[19] E.Roks, P.Centen, J.Bosiers, W.Huinink. *The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD image sensors.* Proc. 25th ESSDERC 1995, pp 327-330.

[20] P.Centen, A.Mierop, H.Stoldt, A.Theuwissen, G.Pine, M. Stekelenburg. *Dynamic Pixel Management for second generation aspect ratio switching.* Montreux International Television Symposium Record, june 8-13, 1995, pp 199-211.

[21] S.Spitzer, J.Toker, A.Moelands, P.Centen, J. van Rooy, B.Gerovac. *Design and Implementation of a 3-CCD State of the Art, 750-line HDTV Progressive Scan Broadcast Camera.* Proc. NAB 1996, pp. 171-178.

[22] E.Roks, P.Centen, J.Bosiers, W.Huinink. *The Double-Sided Floating-Surface Detector: An Enhanced Charge-Detection Architecture for CCD image sensors.* IEEE Trans. Electron Devices. Vol. ED-43, No. 9, pp. 1583-1591, 1996.

[23] H.Stoldt, A.Theuwissen, F.Vledder, P.Centen, A.Mierop, A.Kleimann, H.Peek, D.Verbugt, P.Hartog, R.de Gruyter. *CCD Imagers for Broadcast Applications.* Technical Digest IEDM96, pp. 899-902, San Francisco, December 8-11, 1996.

[24] P.Centen, E. Roks. *Characterization of Surface- and Buried-Channel Detection Transistors for On-Chip Amplifiers.* Technical Digest IEDM97, pp.193-196, San Francisco, December 7-10, 1997.

[25] T. Moelands, P.Centen, R. Voet. *A High Speed Sports Action Camera System.*, Technical Papers International Broadcast Convention, pp 86-92, Amsterdam, September 11-15, 1998.

[26] P.Centen. *Dynamic Pixel Management and Camera Technology.*, Technical Papers of TV symposium of the Arab States Broadcast Union, Tunis, October 1998.

STELLINGEN
behorende bij het proefschrift

CCD Imaging

Concepts for Low Noise and High Bandwidth

van

Peter G.M.Centen

Eindhoven, 29 maart 1999.

1

De fotonen hagelruis in een CCD beeldopnemer wordt altijd uitgedrukt in een factor $\sqrt{N}$. Juister zou het zijn dit te doen in $\sqrt{(N(1+QE))}$.

[1] A. Arcese. *"A Note on Poisson Branching Processes with Reference to Foton-Electron Convertors"*, Applied optics, vol. 3, no. 3, March 1964, pp 435.

[2] W.Powers and R.Aikens. *"Image Orthicon Astronomy at the Dearborn Observatory"*, Applied optics, vol. 2, no. 2, February 1963, pp 157-163.

2

In de studie van Nishida et al., gebaseerd op computer simulaties, wordt geconcludeerd dat de rms waarde van de spatieële ruis, ook wel fixed pattern noise genoemd, 5 dB onder de rms waarde van de temporele ruis (readout noise) moet liggen om niet zichtbaar te zijn. In tegenstelling tot hun generalisering naar een CCD camera geldt dat de rms waarde van de fixed pattern ruis 16 dB onder de rms waarde van de temporele ruis moet liggen om niet zichtbaar te zijn.

[3] Y. Nishida, J. Koike, N. Ohtake, M. Abe, S. Yoshikawa, *"Design Concept for a Low-Noise CCD Image Sensor Based on Subjective Evaluation"*. IEEE Trans. Electron Devices., vol. ED-36, no. 2, pp. 360-366, Februari 1989.

3

Het sensoruitgangssignaal is gequantiseerd in stappen van 1 elektron, en daarmee in stappen van S [μV/e]. Voor de analoog digitaal omzetter is daarmee het maximum aantal benodigde bits (NOB) bepaald op

$$NOB = {}^2\log(Q_{max})$$

Als men zich beperkt tot het lineaire gebied van een broadcast beeldopnemer, waarbij in een van de kleur kanalen een nominaal ladingspakketje een omvang kan hebben van Q_{nom}=15 kel en waarbij een uitsturingsmarge van 5 gehanteerd wordt, dan is volledige quantisatie mogelijk met 16.2 bit. Verder volgt hieruit dat het nominale niveau volledig gequantiseerd kan worden met 14 bit.

4

Door de bulkaansluiting van de detector transistor niet met de source te verbinden, wordt de DC versterking en S [μV/e] gereduceerd zonder dat de ruis eigenschappen verslechteren. Dit heeft als voordeel dat de bandbreedte van de on-chip versterker verhoogd wordt door een verkleining van de factor $\Theta_n=C_{tot}/C_{det}$, Hoofdstuk 2 en 3.

5

Bij het ontwerpen van een beeldopnemer voor HDTV en DTV toepassingen staat het zich richten op hoge μV/e haaks op het streven naar hoge bandbreedte, Hoofdstuk 2 en 3.

6

Een minimum voorwaarde voor een goed ontworpen CCD imager keten is dat het ruisnivo van de signaal processor, die volgt op de CCD beeldopnemer, onder die van de laatste ligt. Een andere voorwaarde, die meestal vergeten wordt, stelt eisen aan de filter werking van de signal processor, Hoofdstuk 4.

7

Ter verlaging van hete-elektronen effecten en van de thermische substraat ruis is het aan te bevelen in on-chip versterkers met NMOS transistoren de P-well te ontruimen.

8

Om een optimale filtering van beeldopnemer signalen in een DSP uit te voeren, dient het beeldopnemer uitgangssignaal gesampled te worden met een frequentie (f_s) die voldoet aan de voorwaarde:

$$f_s \geq 2\, B_n$$

waarbij B_n de ruisbandbreedte (circa 1.6 keer de 3dB bandbreedte) is van de on-chip versterker.

9

Je mag niet discrimineren maar je moet wel onderscheid maken. In sommige situaties is dit een uitermate moeilijk compromis.

10

Het idee dat orde en netheid op het bureaublad ook leidt tot orde en netheid in het werk, en daarmee tot kwaliteitsverbetering, berust op een te optimistische inschatting van de mogelijkheden van een mens tot het vertalen van de ene situatie in een andere (Transfer!).

11

De zegswijze 'in een gezond lichaam huist een gezonde geest' geeft aan hoe gevaarlijk een samenvatting kan zijn. De werkelijke tekst van Juvenalis, Romeins dichter, luidt 'Orandum est ut sit mens sana in corpore sano'; hetgeen betekent: *'We moeten bidden, dat in een gezond lichaam een gezonde geest huist'.*