Accurate equivalent-network modelling of GaAs/AlAs based resonant tunneling diodes with thin barrier layers

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Accurate equivalent-network modelling of GaAs/AlAs based resonant tunnelling diodes with thin barrier layers

J.J.M. Kwaspen, M.I. Lepsa, Th.G. van de Roer and W. van der Vleuten

Indexing terms: Resonant tunnelling devices, Semiconductor devices, Equivalent circuits

The small-signal intrinsic impedance of GaAs/AlAs based resonant tunnelling diodes with thin barriers has been measured at room temperature over the full 0–2V bias-voltage and 0.05–40.05GHz frequency ranges, on stable, non-oscillating devices. The classical Esaki and the quantum-inductance equivalent circuits were used to model the impedance for CAD purposes. Information about the quasibound-state lifetime against bias-voltage was extracted.

Introduction: Both the classical Esaki and the quantum-inductance equivalent-network models [1 – 3] are used here to describe the bias-voltage and microwave frequency dependency of the small-signal intrinsic impedance of MBE grown GaAs/AlAs based double barrier resonant tunnelling diodes (RTDs). The devices have a 5nm quantum well and symmetric barrier and spacer layers, each nominally 2.5nm thick (Fig. 1). The RTDs are of planar type (Fig. 2*a*) with coplanar microwave probe access from the network analyser to the metallised signal (SIG) and ground (GND) pads on the semi-insulating substrate. The DC I-V curve and the microwave reflection coefficient S_{11} of the extrinsic RTD, and S_{11} of an open and a short reference structure are measured at the reference plane (pads) indicated. The short and open structures (SIG-to-GND short or open-circuit at the mesa-site) are used to determine the bias-independent extrinsic elements of the equivalent circuits: C_{ex}, R_{ex} and L_{ex} (Fig. 2*b*, *c*), describing the microwave behaviour of the pad-to-mesa interconnections on the substrate. Only R_{ex} is frequency-dependent due to skin losses in the metallisation.

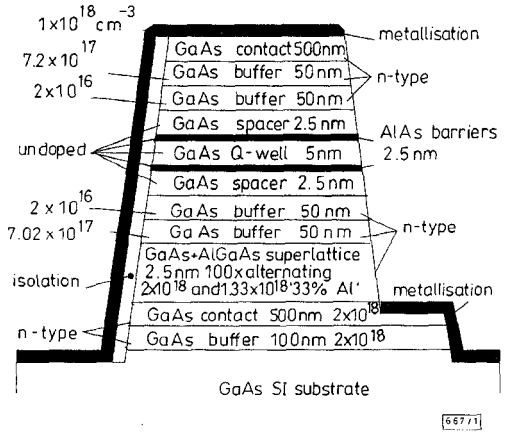

Fig. 1 *MBE-grown DBRTD layer structure*

Stability: A prerequisite for accurate determination of the actual intrinsic elements R_d (dynamic resistance), C_d (dynamic device capacitance), L_q (quantum inductance) and R_s (series resistance) is a stable, non-oscillating RTD in the negative differential resistance (NDR) region. A stable RTD has no plateaus in the NDR region of its I-V curve, so the dynamic conductance G_d (= $1/R_d$) has only one negative peak there (Fig. 4*a*, *b*). By suitable choice of device area (36μm², making $R_d + R_s + R_{ex} < -50\Omega$ in the NDR region) and a specially designed bias circuit, the stability condition was met in our experiments.

Measurements and results: An S_{11} data array was collected in the 0–2V range of the I-V curve (+ on mesa top), where S_{11} of the extrinsic RTD was measured at 75 bias points and from 0.05 to 40.05GHz, after network analyser calibration with on-wafer standards. The prober-chuck temperature was 20.5°C.

Fig. 3 shows some of the S_{11} data in a compressed Smith chart, including S_{11} of the largest negative G_d in the NDR region, the curve marked 1.0072V. Note that for a large range of bias voltages in the NDR region, the S_{11} curves show an inflection point, a feature that cannot be modelled by an equivalent circuit with frequency-independent intrinsic elements like Fig. 2*b*.

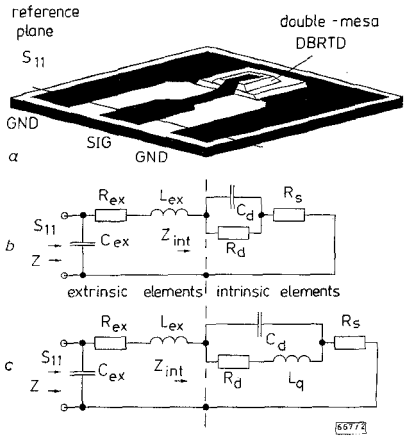

Fig. 2 *Planar DBRTD and equivalent circuits*

a Planar DBRTD with coplanar probe access
b Equivalent network with extrinsic elements and Esaki model
c Extrinsic elements and quantum inductance model

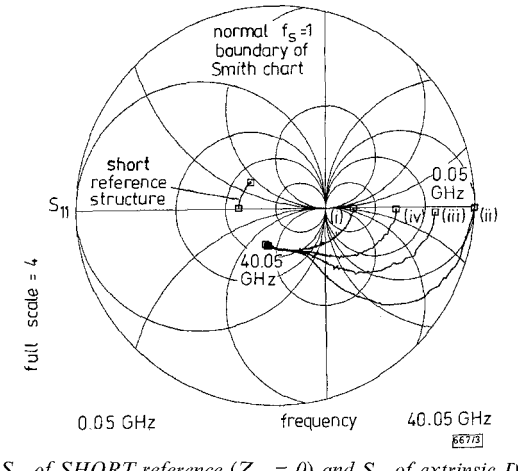

Fig. 3 *S_{11} of SHORT-reference (Z_{int} = 0) and S_{11} of extrinsic DBRTD at several bias-voltages V_d*

(i) 0.9924V
(ii) 1.0072V
(iii) 1.0139V
(iv) 1.0188V

Careful optimisation of the equivalent circuit parameters to match the measured S_{11} data (for each bias point), leads to the conclusion that the three-element Esaki model needs an extra degree of freedom to fit the measured S_{11} data array in most of the NDR region with sufficient accuracy. If the dynamic conductance G_d and the capacitance C_d were modelled as frequency-dependent elements with curve shapes in accordance with [4], matching could be obtained.

The same measured small-signal S_{11} datasets can be described 'perfectly' by the quantum-inductance circuit model (Fig. 2*c*) over the whole bias (0–2V) and frequency range (0.05–40.05GHz) with

four frequency-independent intrinsic elements. The measurement of S_{11} on the stable RTD throughout the whole NDR region results in correct determination of the parameter τ, here defined (from optimised independent elements) as $\tau = L_q/R_d = L_qG_d$ (Fig. 4*b–d*). In the passive regions of the I-V curve, the quantum-inductance model reduces to the classical Esaki model, since the optimisation process results in a low L_q.

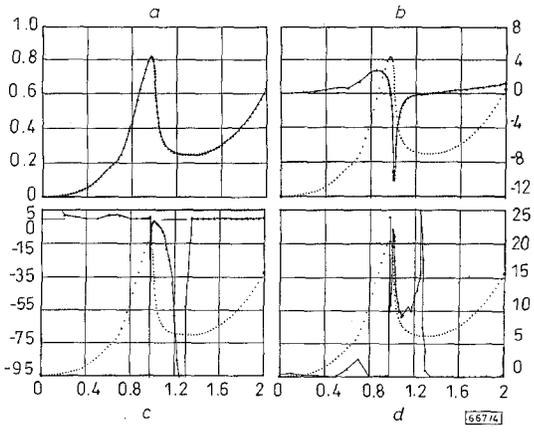

Fig. 4 *Results measurements and optimisations*

a Measured DC I-V curve (T=20.5°C); (also dotted line in Fig. 4 *b–d*
b Dynamic intrinsic conductance G_d against bias-voltage V_d
c Intrinsic quantum inductance L_{qw} against bias-voltage V_d
d Time constant τ against bias-voltage V_d; $\tau = L_{qw} \times G_d$

Discussion: According to many authors [1, 2], the time constant $\tau = L_qG_d$ should be an indication of the quasibound-state lifetime in the well. From the present measurements, this time constant has been obtained for the first time over the whole undistorted NDR region of the RTD's I-V curve and is displayed in Fig. 4*d*. Evidently this time constant only has an appreciable value in the NDR region, i.e. where there is considerable charge storage in the well. Note that the extreme values are less reliable near the points where G_d goes through zero. The calculated lifetime [5] for a nominal barrier thickness of 2.547nm is ~50ps and changes exponentially to ~18ps for a thickness of 2.264nm (1 monolayer decrease). This compares well with a time constant of 22ps measured at 1.0072V (Fig. 4*d*).

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AlGaAs/GaAs *npn* heterojunction bipolar transistors grown by molecular beam epitaxy on Si (311)

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Indexing terms: Heterojunction bipolar transistors, Molecular beam epitaxial growth

AlGaAs/GaAs *npn* heterojunction bipolar transistors grown by molecular beam epitaxy on Si (311) substrates and fabricated using a self-aligned base contact process are reported. Reflection high energy electron diffraction patterns correlate with antiphase domain-free growth. Preliminary DC measurements for a 70×70μm² device reveal a small-signal common-emitter current gain of 10 and a collector-emitter breakdown voltage of 13V.

Introduction: There has been much interest in the heteroepitaxy of GaAs-on-Si due to the potential for integration of high performance GaAs-based optoelectronic devices with Si large scale integration technology [1 – 6]. The superior cutoff frequency and current handling capabilities of AlGaAs/GaAs heterojunction bipolar transistors (HBTs) and enhanced heat dissipation via Si substrates [7] render the integration of high power HBTs-on-Si especially attractive for high power applications. However, reduction of carrier lifetimes, due to the formation of anti-phase domains (APDs), lack of electrical neutrality at the epilayer/substrate interface and high dislocation densities associated with polar-on-nonpolar (GaAs-on-Si) growth, remains the dominant limiting factor of HBT-on-Si performance.

Although APD-free GaAs growth has been achieved on vicinal Si (100) [1 – 4, 6, 8, 9], degraded device performance associated with an appreciable interface defect density remains. Growth of GaAs-on-Si has also been investigated using (211)-oriented substrates [10,11] due to the zinc-blende compatible sublattice nucleation provided by preferential site selection via sites with single- and double-dangling bonds. However, (311)-oriented growth is not as likely to result in the rough morphology and high stacking fault densities associated with the (111)-like (211) orientation [12, 13] due to the reduced step height. In this work, we report the growth of AlGaAs/GaAs HBTs on Si (311) substrates by MBE. Reflection high energy electron diffraction (RHEED) patterns correlate with APD-free growth.

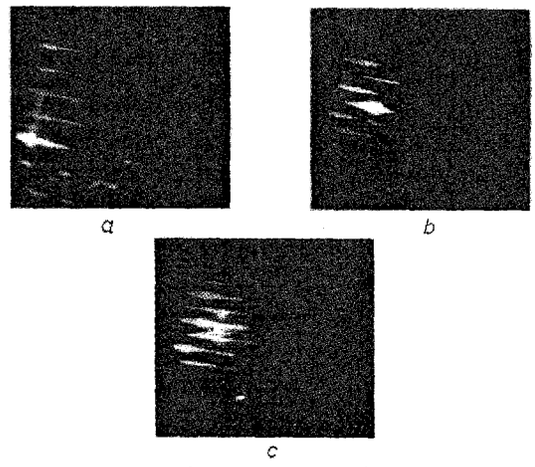

Fig. 1 *RHEED patterns for MBE growth of GaAs-on-Si (311) along [01-1] azimuth*

a Si surface after outgassing
b After 20 monolayers GaAs growth
c After 1.2μm GaAs growth

Experiment: Crystal growth was carried out in an Intevac GEN II MBE system using an As cracking cell while RHEED was used for *in-situ* monitoring. The Si (311) wafers were degreased and etched prior to loading into the chamber. Oxide desorption was performed at a substrate temperature of 900°C for 5min. After deposition of a 25nm GaAs layer at a substrate temperature of 500°C, a 2.0μm GaAs buffer was grown at 575°C at a growth rate