Dry processing of GaAs-based MESFETs and pseudomorphic HFETs

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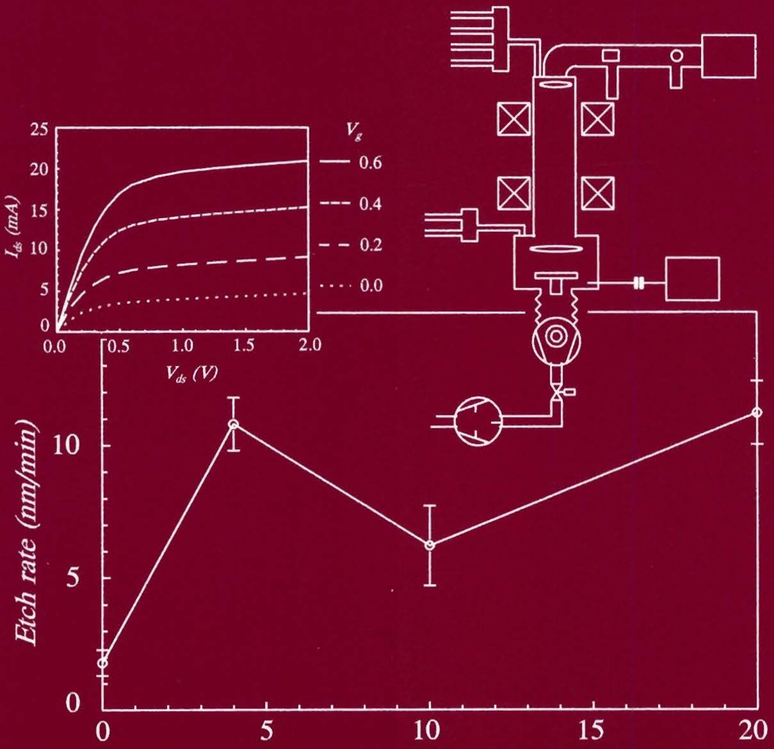

J.G. van Hassel

Dry processing of GaAs-based MESFETs and pseudomorphic HFETs

Cover: Top left: I_{ds}-V_{ds} characteristics of a pseudomorphic AlGaAs/InGaAs/GaAs HFET. Top right: schematic layout of the electron cyclotron resonance plasma etch chamber. In the middle below the influence of increasing argon flow on the average etch rate of GaAs.

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van Dekanen in het openbaar te verdedigen
op dinsdag 2 mei 1995 om 16.00 uur

door

Jan Gerard van Hassel

geboren te Eindhoven

Dit proefschrift is goedgekeurd door de promotoren:

prof.Dr.-Ing. L.M.F. Kaufmann

prof.dr. M. van Rossum

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dr. F. Karouta

aan Simon en Irene

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Introduction

Since 1985 an essential part of the research activities of the Eindhoven University of Technology (EUT) division of Electronic Devices (EEA) is concentrated on III-V compound semiconductors. The research is focused on the modelling, technology and characterisation of electronic components necessary for opto-electronic integrated circuits. The present study is limited to the technology of GaAs-based field-effect transistors. This work is performed in close collaboration with the EUT division of Solid State Physics (NV) where epitaxial structures are grown and characterised. Because no experience was available in the fabrication of field-effect transistors the research was started in close collaboration with the University of Duisburg. At the end of 1992 the research program started with the availability of the clean room and updated technological equipment.

This work is focused on GaAs-based MEtal Semiconductor Field-Effect Transistors (MESFETs) and (pseudomorphic) Heterostructure Field-Effect Transistors (PM)HFETs. The epitaxial structures necessary for transistor fabrication are grown by molecular beam epitaxy at the EUT division of Solid State Physics. Also one structure from the Walter Schottky Institute of the Technical University of Munich was used. Molecular beam epitaxy is known as to produce atomically smooth layers of high quality giving excellent interface properties and low impurity content. This is important since device characteristics are degraded by material defects. Besides, the present structures used for heterostructure field-effect transistors consist of very thin layers, typically 5 to 10 monolayers which emphasizes the requirements demanded from the growth facilities.

In MESFETs the current flows through a n-doped active layer. In a HFET the electrons are spatially separated from their donors and confined in a two-Dimensional Electron Gas (2-DEG) through which the transport takes place. Consequently improved properties are obtained in HFETs. In both structures the current or channel conductivity is controlled by a Schottky contact which is generally placed below the semiconductor surface. This fabrication step is known as the gate recess. The depth of the gate recess is important since it determines the operation characteristics of the device. By the gate recess the threshold voltage of the transistor can be adjusted and enhancement or depletion mode FETs can be defined. This gate recess can be done wet chemically or by dry plasma etching. Since plasma etching offers a great reproducibility and uniformity the interest for dry processes is rapidly increasing. A disadvantage of these processes is the introduction of damage to the epitaxial structures due to an ion bombardment. In this thesis the influence of dry processing on the characteristics of Schottky diodes and field-effect transistors is investigated. Our purpose was to obtain more information on the amount of damage introduced by the plasma. This is done as function of the process parameters in order to achieve optimised process parameters to reduce the damage. The results are continuously compared to wet chemically recessed diodes and transistors to determine the possibilities and disadvantages of using dry processes during the fabrication of these components.

Chapter 1 describes the processes developed for wet processing of GaAs-based MESFETs as well as AlGaAs/GaAs and AlGaAs/InGaAs/GaAs (pseudomorphic) HFETs. Due to the limitations of optical lithography the gate length of the transistors was restricted to 0.8 µm. Ge/Ni/Au ohmic contacts are optimised with respect to annealing time and temperature. Annealing was performed in a Rapid Thermal Annealer (AST SHS 100) in a nitrogen-hydrogen ambient. The different types of transistors are characterised by direct current and high frequency measurements. The microwave measurements are performed at frequencies ranging from 45 MHz to 40 GHz. Few measurements have been done on the noise characteristics. The results are used for comparison to dry processed transistors. Less attention was paid to the uniformity.

The new technological equipment in the clean room was arranged to reduce the damage. One facility is the single-wafer load-locked Leybold (L 560 UV) evaporator. The evaporator has two electron beam evaporators, to evaporate the different metallisations necessary for ohmic and Schottky contacts, and an ion gun (IQ 70). The ion gun is dedicated to clean the semiconductor surface: to reduce the amount of residual oxide and defects on the semiconductor surface. After optimising the characteristics of the ion gun and determining the GaAs etch rates the influence of argon cleaning on Schottky diodes and MESFETs is investigated. These experiments are performed for a neutralised and a non-neutralised argon ion beam. The energy of the argon beam was varied between 50 and 750 eV and in-situ the Schottky metallisations were evaporated. The results are described in chapter 2.

The second facility, dedicated to plasma processing, is the Oxford Plasma Technology cluster tool which was available mid 1993. The layout is shown schematically in figure 1. The cluster tool, installed in the grey room, consists of three different process chambers (stations) connected to a general transfer chamber which is loaded by an additional load lock. The load lock is located inside the clean room. Single-wafer transport is accomplished through a robot arm located in the transfer chamber. The total system is controlled by a microprocessor. Station 1 is an Electron Cyclotron Resonance Reactive Ion Etching (ECR-RIE) system dedicated for etching dielectrics. The process uses a mixture of sulphur hexafluoride (SF_6), fluoroform (CHF_3) and argon. Station 3 is used for Remote Plasma Enhanced Chemical Vapour Deposition (RPECVD) of silicon oxide and silicon nitride. For silicon oxide deposition a gas mixture of nitrous oxide (N_2O) and silane (SiH_4) diluted by nitrogen (N_2) is used. For silicon nitride deposition the nitrous oxide is replaced by ammonia (NH_3). A carbontetrafluoride/oxygen (CF_4/O_2) mixture is used for cleaning the process chamber and to minimise the cross contamination between these two processes. Station 4 is an ECR-RIE etch chamber for III-V materials. Here methane (CH_4), hydrogen (H_2) and argon (Ar) are used as process gases. It is possible to upgrade the cluster tool with a fourth process chamber (station 2). In all chambers the plasma is created and sustained remote and independent from the substrate to prevent an excessive ion bombardment. For this reason less damage is expected compared to the more conventional Reactive Ion Etching (RIE) or PECVD processes. In RIE additional RF power on the substrate table is used for maintaining the plasma and providing an adequate bias for processing.

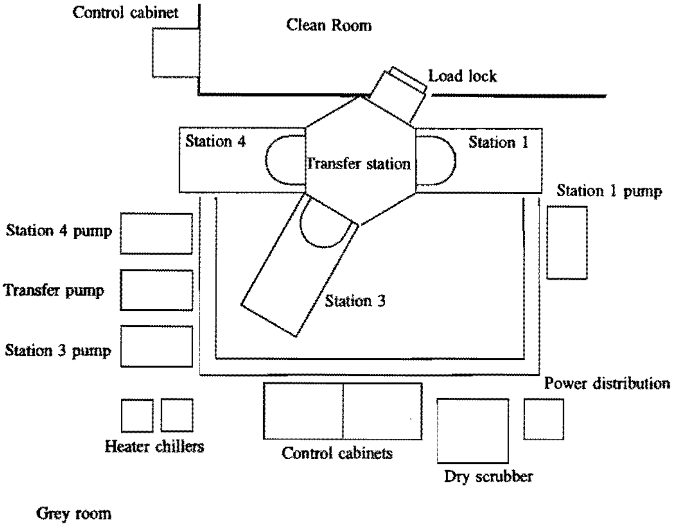
Control cabinet
Clean Room
Load lock
Station 4
Transfer station
Station 1
Station 1 pump
Station 4 pump
Transfer pump
Station 3
Station 3 pump
Power distribution
Heater chillers
Control cabinets
Dry scrubber
Grey room

Figure 1, Schematic layout of the OPT cluster tool.

In ECR based plasmas the additional RF power (DC bias) is generally low since the first condition is already satisfied. The different processes are clustered together in one system to minimise the exposure to air to allow subsequent processing in different chambers within one run.

Station 4 is dedicated to perform the gate recess. The chemical nature of this process is based on the formation of group III metalorganic compounds and group V halides. Chapter 3 describes the etch characteristics of the $CH_4/H_2/Ar$ ECR plasma on different III-V semiconductors as a function of different process parameters. The attention was mainly focused on GaAs.

Beside the chemical nature of the process a physical component is present due to additional DC bias. In addition to the structural damage created by the $CH_4/H_2/Ar$ ECR plasma also passivation occurs due to the presence of hydrogen. Passivation originates from the formation of Si-H complexes which result in a loss of electrical activity of the donor atoms in the semiconductor layers. The passivation can be restored by a heat treatment which was done in the rapid thermal annealer in a nitrogen ambient. The influence and amount of damage is described in chapter 4. Capacitance-Voltage (C-V) measurements were used to study the passivation depth as function of silicon donor concentration and as function of the additional process bias. This is investigated on MBE grown silicon doped n-GaAs bulk layers. By

current-voltage (I-V) measurements on Schottky diodes the damage is investigated as a function of the substrate bias. The characteristics are compared to wet chemically etched diodes.
For AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures the influence of the plasma on the sheet density and the Hall mobility of the 2-DEG is investigated as function of the measurement temperature. Upon annealing full recovery of the sheet density was obtained for the AlGaAs/GaAs heterostructure, whereas the Hall mobility only partially recovered. Introduction of an additional silicon δ-doped layer in the structure behaved as a shield and prevented the 2-DEG for further damage introduction. The effect of an additional δ-doped layer was even more pronounced in the pseudomorphic heterostructure. The results are compared to identical experiments with CH_4/H_2 reactive ion etching on the same structures.

Because thin resist layers, necessary for 1 μm patterns, were not resistant to the $CH_4/H_2/Ar$ ECR plasma process, silicon nitride or silicon oxide layers had to be used in the fabrication of transistors. Since little was known about the quality of these layers this is investigated as function of the process parameters. Chapter 5 describes the deposition of silicon oxide and silicon nitride films as function of the process conditions. The composition of the films was measured by Rutherford Backscattering Spectrometry (RBS) using 4 MeV Helium ions. Simultaneously the hydrogen incorporation was measured by Elastic Recoil Detection Analysis (ERDA or ERD). Furthermore the refractive index, deposition rate and etch rate have been determined and compared to the results obtained with the compositional analysis.

Chapter 6 describes the results obtained on dry recessed MESFETs and pseudomorphic HFETs. These results will be compared to wet chemically processed transistors which are described in chapter 1. Additional process steps, necessary for the fabrication of these dry processed transistors, will be discussed.

In chapter 7 the work is summarised and recommendations for further investigations are made.

With the contribution and collaboration of many people this work is realised. For that reason I would like to thank prof. Dr.-Ing. L.M.F. Kaufmann for giving me the opportunity to realise this work and for stimulating of contacts with other researchers. I also acknowledge dr. F. Karouta and dr. ir. Th.G. van de Roer for fruitful discussions during the work and preparation of this thesis and my second promoter prof. dr. M. van Rossum and prof. dr. P. van Daele for critical reviewing this work. In particular I would like to thank some people from the physics department of the EUT: P.A.M. Nouwens for performing the Hall measurements, ir. C.M. van Es for discussions, W.C. van der Vleuten for having grown the epitaxial layer structures (division of Solid State Physics) and dr. L.J. van IJzendoorn (division of Particle Physics) for measuring and interpretation of the RBS and ERD measurements. I wish to acknowledge ing. J.J.M. Kwaspen and ir. H.C. Heyker for measuring the high frequency characteristics. I appreciate the collaboration and technical assistance of drs. E. Smalbrugge, B.H. van Roy, ing. J.J.A. Stegeman, H.P.J.C. Rooijakkers, dr. A. Kalfane, dr. Y. Zhu, J.H. Maahury and the other members of the group. Finally I will not forget my family for their support and especially Réjane and Vicky for their patience during the work and preparation of this thesis.

CHAPTER I

GaAs-based field-effect transistors.

1.1 Introduction.

GaAs-based field-effect transistors are widely used in integrated circuits such as oscillators, amplifiers and mixers. MEtal Semiconductor Field-Effect Transistors (MESFETs) and Heterostructure Field-Effect Transistors (HFETs) are commonly the devices on which this integration is based. The heterostructure configuration is known under different names. Beside HFET also MOdulation Doped Field-Effect Transistor (MODFET), Two-dimensional Electron Gas Field-Effect Transistor (TEGFET or 2DEGFET), High Electron Mobility Transistor (HEMT) and Selectively Doped Heterostructure Transistor (SDHT) are frequently used. Here the term HFET will be used. The advantages of these HFETs over MESFETs are its lower power dissipation, lower noise and the fast response times. The fast response times can be ascribed to the high electron mobility and saturation velocity in these semiconductor materials.

In a MESFET the current flows through a normally n-doped layer. This current is controlled by a Schottky diode. Because of the presence of both the donor atoms and the electrons in the same layer the mobility as well as the response time are reduced in these structures. According to Hilsum [1] the mobility μ decreases with increasing donor concentration N_d. This reduction is due to an increase of the Coulomb scattering. See equation 1.1.

$$\mu = \frac{10^4 cm^2/Vs}{1+\sqrt{\dfrac{N_d}{10^{17} cm^{-3}}}} \tag{1.1}$$

In a heterostructure field-effect transistor the electrons are spatially separated from their donor atoms. The electrons are transferred from the higher bandgap doped material to the lower bandgap undoped material. The electrons in the lower bandgap material are confined in the vicinity of the interface in a Two-Dimensional Electron Gas (2-DEG). The Coulomb scattering is minimised by this separation which leads to an increased mobility especially at low temperatures. This can be enhanced if the lower bandgap material has improved electron velocity saturation properties. In this way superior device performances are obtained.

In the present work a technology for the fabrication of different types of compound semiconductor transistors had to be developed first. This was the base from which further investigations proceeded.

This chapter describes the wet chemical processes developed for GaAs-based transistors. With this technology GaAs MESFETs, AlGaAs/GaAs and AlGaAs/InGaAs/GaAs HFETs have been made and characterised. The principles of operation of MESFETs and HFETs are discussed in paragraph 1.2. The mask layout, the fabrication and optimisation of the process are described in paragraph 1.3 and 1.4 respectively. Paragraph 1.5 describes the electrical measurements used to characterise the transistors. The transistors are characterised by direct current and high frequency measurements at room temperature. Paragraph 1.6 lists the results obtained on wet chemically processed MESFETs, AlGaAs/GaAs and AlGaAs/InGaAs/GaAs HFETs. Here the structures and the data obtained with DC and microwave measurements are shown. Finally the results are compared to literature.

1.2 Transistors.

1.2.1 MESFETs

A typical schematic cross section of a MESFET is shown in Figure 1.1. The epitaxial structure consists of 2 µm undoped GaAs buffer layer, a 200 nm thick n-GaAs active layer ($3\cdot10^{17}$ cm^{-3}) and a 20 nm highly silicon doped ($2\cdot10^{18}$ cm^{-3}) n$^+$-GaAs top or contactlayer. The electron transport is carried within the active layer. The structure is grown on a semi-insulating GaAs substrate.

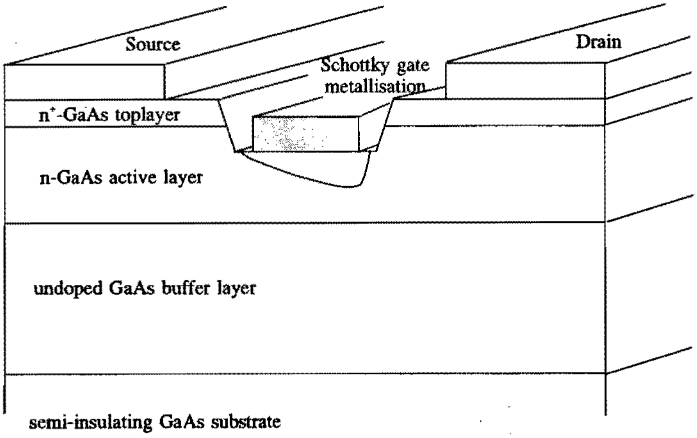
Source
Schottky gate metallisation
Drain
n$^+$-GaAs toplayer
n-GaAs active layer
undoped GaAs buffer layer
semi-insulating GaAs substrate

Figure 1.1, Schematic cross section of the layer structure of a MESFET.

The structures are grown with Molecular Beam Epitaxy (MBE). The semi-insulating substrates were produced using the Liquid Encapsulated Czochralski (LEC) technique.
With the Schottky gate metallisation between the ohmic contacts (see Figure 1.1) the channel conductivity can be modulated by applying a negative bias to this gate with respect to the source. If a voltage is applied between the drain and the source a current according to equation 1.2 will flow in the active GaAs layer.

$$I_{ds} = q\cdot W\cdot N_d\cdot[A-A_d(x)]\cdot v(x) \tag{1.2}$$

Here I_{ds} is the current between the drain and the source, q the electron charge, W is the width of the transistor, x the coordinate along the channel, A the thickness of the active layer under the gate, $A_d(x)$ the depletion depth and v(x) the electron velocity. For small voltages the electron velocity is linear to the longitudinal electric field E(x).

$$v(x) = \mu\cdot E(x)=\mu\frac{dV(x)}{dx} \tag{1.3}$$

with V(x) the potential along the channel. According to the abrupt junction depletion approximation and the one dimensional Poisson equation the depth of the depletion region under the gate $A_d(x)$ can be written as:

$$A_d(x) = \left[\frac{2\epsilon\cdot\{V(x)+V_{bi}-V_g]}{q\cdot N_d}\right]^{\frac{1}{2}} \tag{1.4}$$

Here ϵ is the dielectric permittivity of GaAs, V_{bi} the built in voltage of the Schottky barrier and V_g the gate voltage.
In figure 1.1 it is shown that the depletion region extends further into the active GaAs layer at the drain side of the gate. This occurs due to the higher reverse bias across the drain-gate diode as compared to the source-gate diode.
Substituting equation 3 and 4 in equation 2 and integrating over x along the channel from the source side to the drain side of the gate gives the fundamental equation of field-effect transistors [2].

However if the electrical field under the gate is greater than the critical electric field E_c the electron velocity saturates [3]. This can be modelled by dividing the region under the gate in two regions [4,5]. A region where the electron velocity is linear with the electric field and a region with constant electron velocity.

$$v = \begin{cases} \mu \cdot E(x) & \text{for } E < E_c \\ v_s & \text{for } E > E_c \end{cases} \tag{1.5}$$

In this case the saturation current $(I_{ds})_{sat}$ of a transistor can be expressed as:

$$(I_{ds})_{sat} = \beta \cdot (V_g - V_T)^2 \tag{1.6}$$

where the threshold voltage V_T is the gate-source voltage needed to deplete the channel at the drain side of the gate. The factor β can be written as [2]:

$$\beta = \frac{2 \epsilon \mu v_s W}{A \cdot (\mu V_{po} + 3 v_s L)} \tag{1.7}$$

with $V_{po} = V_{bi} - V_T$ the pinch off voltage and L the gate length. It can be seen that the DC saturation characteristics, according to equation 1.6 and 1.7, have a more or less linear dependence on the electron mobility. The voltage drops across the drain and the source resistances are however not included in this model. The influence of these resistances on the performance of the transistors will be treated later in this chapter.
As stated in the introduction the mobility decreases with increasing donor concentration. This holds certainly for MESFETs. In HFETs this effect is reduced because the donors are spatially separated from the 2-DEG that forms the transistor channel.

1.2.2 AlGaAs/GaAs HFETs

Figure 1.2 shows schematically a cross section of an AlGaAs/GaAs HFET structure and its band structure at the semiconductor interface. On the semi-insulating GaAs substrate an undoped GaAs buffer layer is grown. Subsequently a few nanometer thick undoped AlGaAs spacer and a n^+-AlGaAs donor layer are grown. On the top there is a n^+-GaAs caplayer. The thickness of the spacer layer is typically between 2 and 5 nanometer in HFET structures. This shows the importance of epitaxial techniques with atomic resolution.

The highly doped GaAs toplayer prevents the AlGaAs layer from surface oxidation and so from surface depletion due to this oxidation. This layer also facilitates the formation of ohmic contacts.

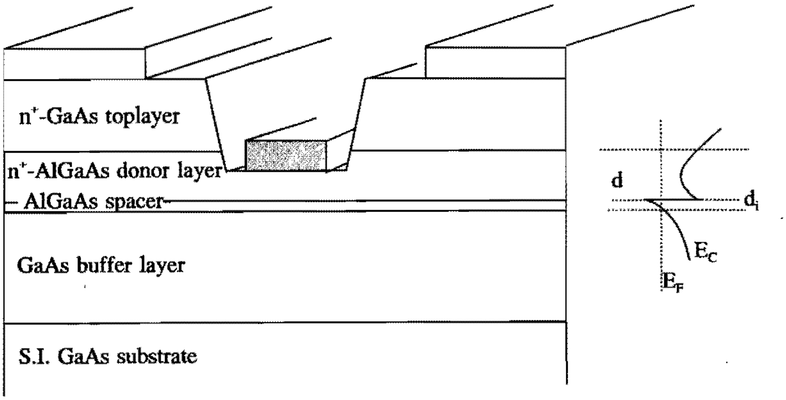

Figure 1.2, The cross section of the structure used in an AlGaAs/GaAs HFET. On the right side the AlGaAs-GaAs conduction band discontinuity is shown.

Between the n^+-AlGaAs donor layer and the GaAs buffer layer discontinuities in the valence and conduction bands occur due to the difference in bandgap of these materials. This is shown in the right hand side of figure 1.2 and in figure 1.3. The band discontinuity ΔEg between GaAs and $Al_yGa_{1-y}As$ for an aluminium concentration less than 45 percent can be written as [6]:

$$\Delta Eg = 1.247 \cdot Y \qquad \text{for } Y < 0.45 \tag{1.8}$$

This bandgap difference leads to discontinuities in the conduction band ΔE_c and the valence band ΔE_v which nowadays are generally accepted to be about [7]:

$$\begin{aligned} &\Delta E_c = 0.67 \cdot \Delta Eg \\ \text{and} \qquad & \qquad\qquad\qquad \text{for } Y < 0.45 \\ &\Delta E_v = 0.33 \cdot \Delta Eg \end{aligned} \tag{1.9}$$

Although in the past different figures have been used [8]. Due to these discontinuities the electrons of the AlGaAs layer are transferred into an approximately triangular potential well on the GaAs side of the interface. There the electrons are accumulated in a two-dimensional electron gas. The electron energies are quantised in this well. The concentration in the 2-DEG can be calculated by self-consistently solving the Schrödinger (1.10) and Poisson equations (1.11) [9,10]

$$\frac{(h/2\pi)^2}{2m} \cdot \frac{d^2\phi_i(z)}{dz^2} + [E_i - V(z)]\phi_i(z) = 0 \tag{1.10}$$

$$\frac{d^2 V}{dz^2} = \frac{q\rho(z)}{\epsilon} \tag{1.11}$$

where z is the coordinate perpendicular to the epitaxial layers, h is the Plancks constant, $\phi_i(z)$ the electron wave function, $\rho(z)$ the space charge density, m the electron mass and E_i the ith subband energy level. The electron potential energy in GaAs perpendicular to the interface can be found with help from the Poisson equation and:

$$-\rho(z) = q \cdot \sum_i n_i |\phi_i|^2(z) \tag{1.12}$$

Here the charge density due to donor and acceptor impurities in GaAs are neglected. Using the Fermi-Dirac distribution function, the electron concentration in the ith subband can be expressed as:

$$n_i = D\frac{kT}{q}\cdot\ln[1+\exp^{\frac{E_F-E_i}{k_bT}}] \tag{1.13}$$

with $D=4\pi qm/h^2$ the density of states for a two dimensional electron gas. An analytical approximation of the energy of the ith subband can be represented as [11]:

$$E_i = [\frac{(h/2\pi)^2}{2m}]^{\frac{1}{3}}\cdot[\frac{3}{2}qE_s\pi(i+\frac{3}{4})]^{\frac{2}{3}} \tag{1.14}$$

The surface electric field E_s can be related to the 2-DEG charge density by solving the Poisson equation over the depletion region which gives $\epsilon\cdot E_s = q\cdot n_s$. Combining with equation 1.14 the energy of the subbands can be related to the 2-DEG sheet density n_s:

$$E_1 = \zeta_1\cdot n_s^{\frac{2}{3}}$$

$$E_o = \zeta_o\cdot n_s^{\frac{2}{3}} \tag{1.15}$$

Here ζ_i are parameters which can be adjusted to fit experimental results. When using the Fermi-Dirac statistics the 2-DEG sheet charge concentration can be given as function of the Fermi level position [11,12]:

$$n_s = D(\frac{kT}{q})\cdot\ln[(1+e^{q\frac{(E_F-E_o)}{k_bT}})(1+e^{q\frac{(E_F-E_1)}{k_bT}})] \tag{1.16}$$

It is assumed that only the first two subbands are occupied. Electron transport in a HFET is in the lateral direction through the 2-DEG. The separation of the ionised donors in the donor layer and the electrons of the 2-DEG reduces the Coulomb scattering. In this way the mobility is increased compared to the mobility of a MESFET. This improved mobility was observed for the first time by Dingle et al. [13]. In spite of this separation the electrostatic Coulomb interaction is still present. For this reason an undoped AlGaAs spacer is introduced in the layer structure to increase the spatial separation. Intense research has been performed on the influence of the spacer thickness on the electron mobility and the 2-DEG sheet density. The influence of the spacer is investigated mainly at low temperatures since the effects are more pronounced in that regime. In general the mobility increases and the 2-DEG sheet concentration decreases with increasing spacer thickness [14,15]. The mobility also increases with increasing electron density in the 2-DEG until the electrons start to fill the first subband. Then the mobility is reduced by inter subband scattering. In a HFET it is preferred to have a high sheet concentration and a high electron mobility. The thickness of the AlGaAs spacer is typically between 2 and 5 nanometer to satisfy both conditions.

The band discontinuity and the donor density in the AlGaAs layer also have an influence on the 2-DEG sheet concentration. The aluminium content in the donor layer needs to be high to improve the band discontinuity at the interface and to improve the Schottky barrier height (equation 1.8). Also a high (Si) donor density in the AlGaAs layer is preferred for creating a high 2-DEG sheet concentration and to reduce the distance between the gate and the 2-DEG. However having as well a high aluminium concentration and a high donor concentration leads to the formation of deep centres in the donor layer [16]. These centres, named DX centres, occur if the aluminium content increases beyond 25 percent. Due to these DX centres transistors suffer from persistent photoconductivity, shifts in the threshold voltage and a collapse of the drain-source I-V characteristics, especially at low temperatures [17]. Another difficulty is that at band discontinuities of > 0.3 eV carrier transfer to higher valleys in the conduction band of GaAs can occur. This leads to a degradation of the mobility and the saturation velocity. For these reasons the aluminium content that will be used is below 30 percent.

The sheet density in the 2-DEG is controlled by a Schottky diode between the ohmic contacts. For an effective control of the electron density in the channel it is necessary to place the gate electrode below the highly doped toplayer in the AlGaAs donor layer. This is achieved by a gate recess which is usually done wet chemically or by a dry plasma etch process. By the gate recess it is possible to obtain different threshold voltages for the HFETs. In this way enhancement (normally off: positive threshold voltage) and depletion (normally on) mode field-effect transistors can be made. In depletion mode FETs the depletion by the gate built-in voltage extends just to the interface depletion. In normally off FETs a smaller AlGaAs donor layer is present and the depletion of the gate extends to the electron gas.
The depth of the gate recess is important since parallel conduction through the AlGaAs donor layer occurs if the recess is not performed adequately [18].
By increasing the gate bias in the positive direction the sheet density of the 2-DEG increases to its maximum value n_{s0}. A further increase of the voltage also leads to a conduction in the AlGaAs donor layer in parallel to the current transport in the 2-DEG. The performance of a HFET decreases as a consequence of this parasitic MESFET behaviour.
Considerations on the doping level, the spacer thickness and the thickness of the AlGaAs donor layer are given by Das et al. [19].

The 2-DEG sheet concentration can be written as a function of the gate voltage according to equation 1.17 [6,20].

$$q \cdot n_s = c_o \cdot [V_{gs} - V_T] \tag{1.17}$$

with c_o the gate to the 2-dimensional electron gas capacitance.

$$c_o = \frac{\epsilon}{d + d_i + \Delta d} \tag{1.18}$$

where d is the distance between the gate electrode and the AlGaAs spacer layer, d_i is the thickness of the spacer and Δd is the distance of the 2-DEG to the AlGaAs/GaAs interface. Applying a drain-source voltage gives an additional -V(x) term within the brackets of equation 1.17. Then the sheet density varies in the lateral direction and the I-V characteristics can be calculated.

1.2.3 Pseudomorphic AlGaAs/InGaAs/GaAs HFETs

The performances of HFETs can be improved by growing a thin InGaAs layer below the AlGaAs spacer through which the current transport takes place. InGaAs is known as having a higher electron saturation velocity compared to GaAs. Ketterson et al. [21] clearly showed the influence of an increasing indium content on the direct current and high frequency characteristics of these transistors.
The bandgap discontinuity and so the conduction band discontinuity between AlGaAs and InGaAs increases with respect to the AlGaAs/GaAs heterostructure. Figure 1.3 shows the band diagrams for an AlGaAs/GaAs and an AlGaAs/InGaAs/GaAs heterostructure. The band gap difference between $In_xGa_{1-x}As$ and $Al_yGa_{1-y}As$ can be defined as [6]:

$$\Delta E_g = 1.247 \cdot Y + 1.5 \cdot X - 0.4 \cdot Y^2 \qquad \text{for } Y < 0.45 \qquad (1.19)$$

and the discontinuities in the valence and conduction band are respectively accepted to be:

$$\begin{array}{ll} & \Delta E_c = 0.6 \cdot \Delta Eg \\ \text{and} & \qquad\qquad\qquad \text{for } Y < 0.45 \qquad (1.20) \\ & \Delta E_v = 0.4 \cdot \Delta Eg \end{array}$$

Beside better transport properties of electrons in InGaAs, the increased bandgap allows a higher sheet density, a greater carrier confinement and the upper valleys are farther away than in GaAs. The aluminium content of the spacer and donor layer can be reduced in this structure to avoid DX centre related problems. Due to a lattice mismatch of about 1 percent between InGaAs and the AlGaAs and GaAs the thickness of the InGaAs layer needs to be less than its critical thickness. Above the critical thickness misfit dislocations occur during the epitaxial growth which degrade the performance of transistors. Below the critical thickness the InGaAs accommodates to the lattice of GaAs with a certain strain. The critical thickness of InGaAs decreases with increasing Indium content. For this reason the amount of indium in pseudomorphic transistors is not allowed to exceed 35 percent, although degradation of the characteristics is often observed at indium contents higher than 25 percent [9].

A further improvement in HFETs can be obtained by adding a Si δ-doped layer or pulse doped layer between the AlGaAs spacer and donor layer [22]. The advantages of this Si δ-doped layer are a larger gate-voltage swing and a reduction of traps associated with the dopant atoms in uniformly doped AlGaAs layers. Extended discussions of this and other kind of structures can be found in references 6 and 20.

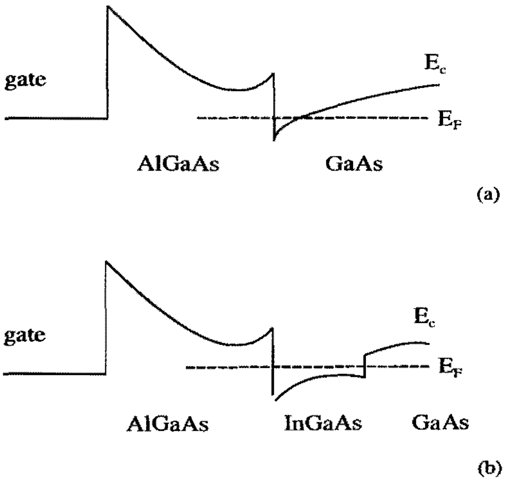
gate
E_c
E_F
AlGaAs
GaAs
(a)
gate
E_c
E_F
AlGaAs
InGaAs
GaAs
(b)

Figure 1.3, The conduction band diagram for an AlGaAs/GaAs heterostructure is shown in (a) The AlGaAs/InGaAs/GaAs heterostructure band diagram in (b).

1.3 Mask layout.

In collaboration with the University of Duisburg (Germany) a mask set has been developed for the fabrication of transistors. Beside transistors, control structures to measure the contact resistance and diodes are present on the mask. An extended discussion of the layout and the design rules concerning the alignment marks and the overlap between the different masks is given by Bertenburg [23]. Here only the main features of the mask will be mentioned.
The mask set consist of six different masks which need to be processed subsequently to obtain complete transistors. The first four masks are used in our processes, because the fabrication of air bridges (last 2 masks) has not been implemented. The different process steps will be treated in paragraph 1.4.
Each mask is divided in unity cells of 4 * 4 mm^2. which is repeated over a 3 inch circle. Each unity cell contains:

- Different transistor layouts (single-finger end-gate FETs, T-gate FETs, π-gate FETs and multiple-finger gate FETs) with gate lengths varying from 4 μm down to 0.6 μm. The width of the transistors varies from 200 μm down to 40 μm. Figure 1.4 shows a schematic layout of some different transistors. The shaded squares represent air bridges. The transistors have a Cascade layout necessary for on wafer high frequency characterisation.

- A transmission line pattern (TLM) to extract and to optimise the ohmic contact resistance. The transmission line pattern consists of six 200 μm width contacts separated from each other by increasing distances (2.5, 5, 10, 20 and 40 μm). A short discussion of the extraction of the contact resistance is given in paragraph 1.4.3.

- A 200 * 200 μm^2 Schottky diode surrounded by an ohmic contact to determine the diode characteristics like barrier height, leakage current and ideality factor.

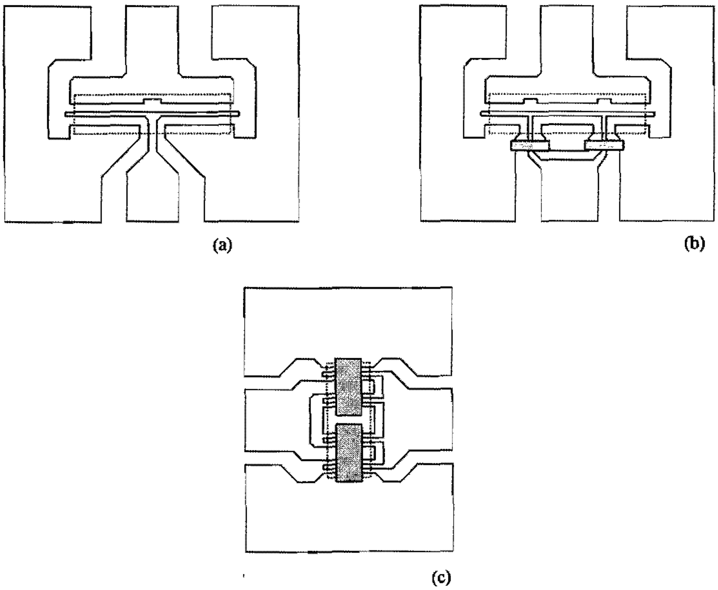

Figure 1.4, Schematically a T-gate (a), a π-gate (b) and a multiple finger (c) field-effect transistor is shown. The dashed squares represent air bridges.

1.4 The fabrication process.

1.4.1 Introduction

In this paragraph the different process steps necessary to obtain devices will be treated. All the processes are based on optical lithography. This restricts the minimum feature size to 0.8 µm. The four main processing steps necessary for the fabrication of a transistor are:

- Mesa isolation etch.
- Drain and source ohmic contact metallisation.
- Gate recess and metallisation.
- Contact paths (Cascade overlay metallisation).

The different process steps will be discussed below. A detailed description of the different processes is written in Appendix A.

1.4.2 Mesa etch.

Figure 1.5 shows the isolation of an active area of a T-gate FET. The etch is performed wet chemically in a $H_2SO_4:H_2O_2:H_2O$ solution at room temperature. The etch is through the active layer into the semi-insulating buffer layer. This etch separates the devices electrically from each other and confines the current flow to a certain area.

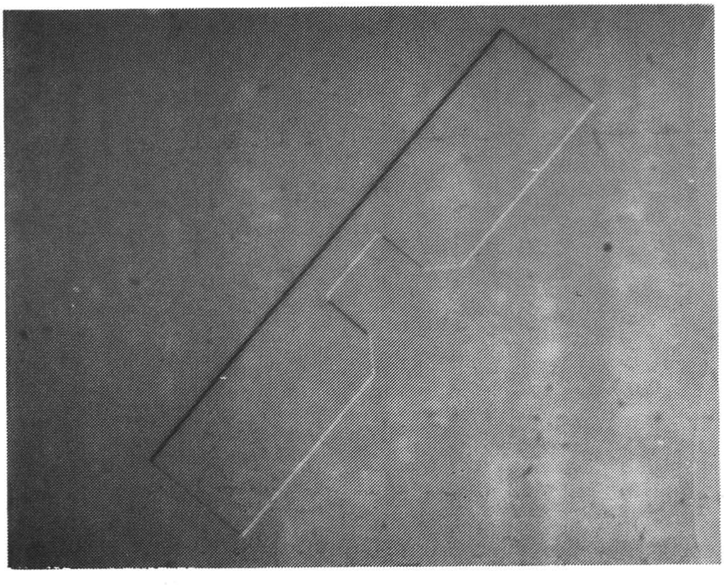

Figure 1.5, The mesa of a T-gate field-effect transistor with a width of 150 µm.

1.4.3 Ohmic contact formation.

The ohmic drain and source contacts are processed by a lift-off technique. This process leaves the metallisation that is on the GaAs surface and lifts the metal which is on the resist when the resist is dissolved in acetone (see also Appendix A). After lift-off the metallisation is annealed to obtain an ohmic contact. This annealing is necessary to obtain a low voltage drop over the contacts compared to the voltage drop in the active region under the gate. The annealing process is optimised with respect to the surface morphology of the metallisation, the ohmic contact resistance and the edges of the metallisation. Apart from the influence of annealing on the smoothness of the metallisation edges, the quality of the edges is very sensitive to the profile obtained in the patterned resist. An undercut resist profile as shown in [23] is desirable in this case.

To obtain good ohmic contacts a number of different metallisations and fabrication techniques have been described in literature [24,25]. These metallisations have to be annealed generally between 300 and 600 °C [25,26]. In our process the metallisation is evaporated by an e-beam process in the Leybold (L 560 UV) evaporator. The base pressure of this system is $3 \cdot 10^{-8}$ mbar. The distance between the sample and the e-gun is 50 cm to minimise heating up of the resist which facilitates the lift off process. The metallisation used for the ohmic contacts is germanium, nickel and gold (20 nm/15 nm/200 nm).

During annealing the germanium diffuses into the GaAs whereas gallium diffuses towards the metallisation. The purpose of the nickel is to prevent the metallisation from boiling up and to enhance the diffusion process. It is believed that grains of NiAs(Ge) are formed on the GaAs side of the interface below an AuGa intermixing layer [27,28,29]. Beside the vertical direction of the alloy it also extends in the lateral direction [30,31]. Since germanium is known as a n-dopant of GaAs, the GaAs surface layer becomes highly doped. This highly doped surface concentration causes an extremely narrow potential barrier. The energy band diagram of an ohmic contact is shown in Figure 1.6.

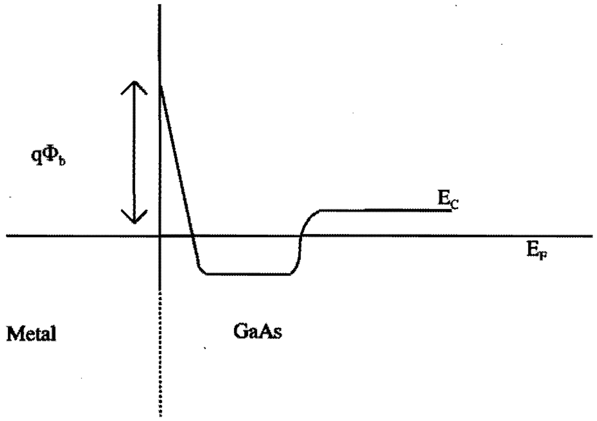

Figure 1.6, The band diagram of an ohmic contact after annealing.

Due to this narrow barrier the probability of tunnelling from the metallisation to the GaAs is increased and the transport mechanism of the ohmic contact works mainly due to this tunnelling effect.

The annealing process is optimised with respect to the annealing temperature and time. The minimal contact resistance observed as function of these two parameters is ascribed to the size of the grains formed [28]. Annealing is performed in a rapid thermal annealer (AST SHS 100) in a hydrogen and nitrogen ambient. In the RTA the sample is situated on a graphite plate in a quartz tube. With halogen lamps on both sides of the quartz chamber it is possible to increase the temperature of the sample very fast. The actual temperature is controlled by a thermocouple connected to the graphite plate. A detailed description of the annealing process is described in Appendix B. The contact resistance is determined from measurements on the transmission line which has been described in paragraph 1.3. The mesa restricts the current flow across the contact of width W. Then the contact resistance can be defined as [32]:

$$R = 2 \cdot R_c + \frac{R_{sh}}{W} \cdot L_c \tag{1.21}$$

where R_c is the contact resistance, R_{sh} is the sheet resistance of the GaAs layer, L_c the distance between the ohmic contacts and R the measured resistance. It is assumed that the sheet resistance under the contacts equals the sheet resistance between the contacts.

The contact resistance was measured using a four probe method. Plotting the measured resistances as function of the distance between the ohmic contacts gives $2R_c$ as an intercept with the Y-axis. This resistance is usually expressed in Ω-mm. The slope of the line reveals the sheet resistance divided by the width of the contact. These values are extracted with a least squares line fit.

To optimise the contacts with respect to the criteria mentioned above the annealing time and temperature are varied respectively. The ohmic contacts are optimised on the MESFET layer described in paragraph 1.2.1. The MESFET structure has a highly doped toplayer since the contact resistance decreases with increasing donor concentration [29,32]. Figure 1.7 shows the contact resistance as a function of annealing temperature for 1 minute processes. The contact resistance decreases rapidly from 380 to 400 °C. At 420 °C the spreading in the resistance increases, the edges of the ohmic contacts become rough and the surface morphology deteriorates. As an example figure 1.8 shows a photograph of an ohmic contact annealed at 440 °C for 1 minute. A part of the spreading, observed at all temperatures, can be explained by the temperature overshoot of about 10 % which sometimes occurs between the ramp-up from 100 to 400 °C and the stable 400 °C period. See also appendix B.

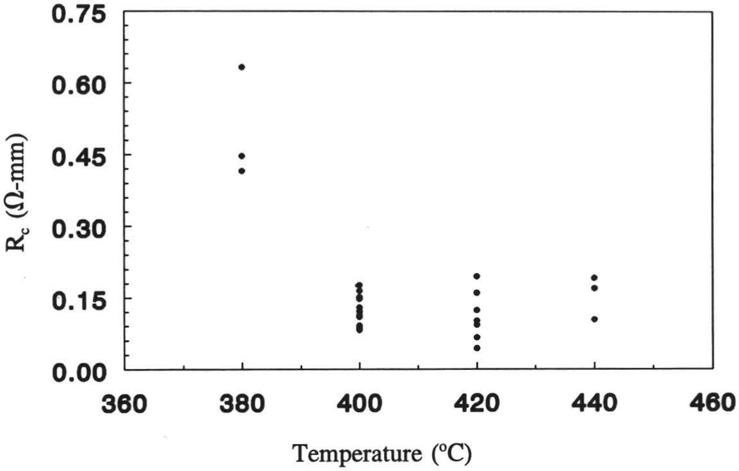

Figure 1.7, The contact resistance on a MESFET structure as a function of the RTA anneal temperature. The annealing time is kept constant at 60 seconds.

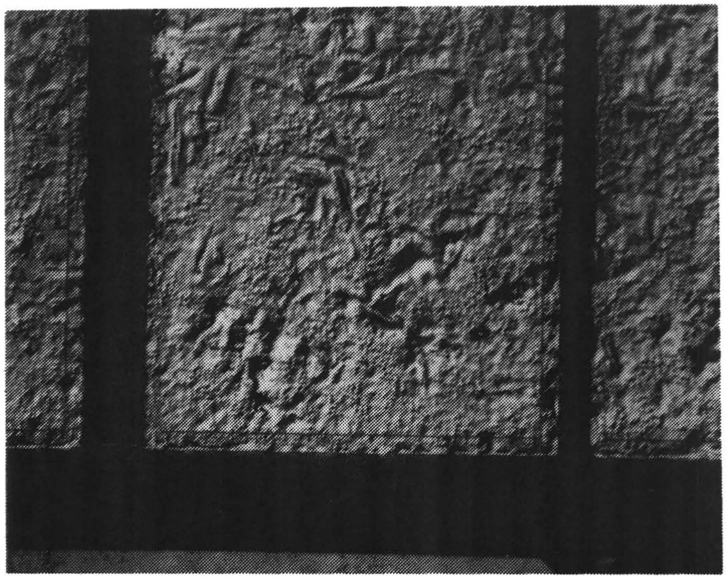

Figure 1.8, A photograph of the surface morphology of an ohmic contact annealed at 440 °C for 1 minute.

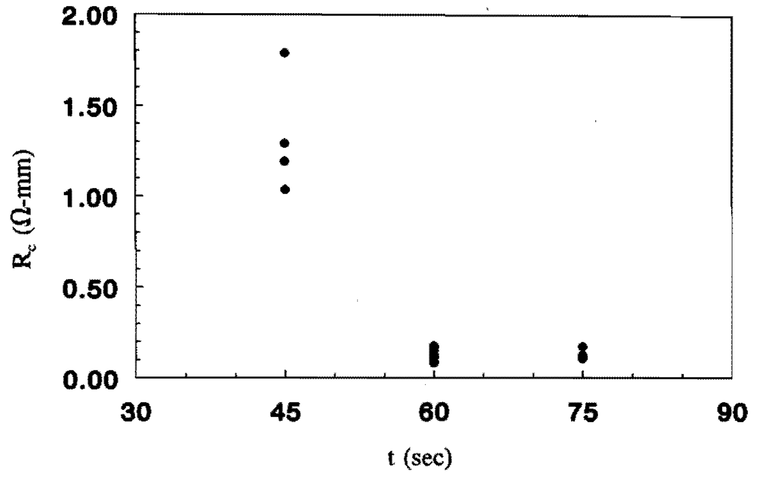

Figure 1.9, The optimisation of the contact resistance as a function of the annealing time. The temperature is kept constant at 400 °C.

Figure 1.9 shows the extracted contact resistance after annealing at 400 °C as function of increasing annealing time. The resistance rapidly decreases if the time is increased from 45 to 60 seconds. At 75 seconds the value of the contact resistance is still low. At this time however a degradation of the surface morphology occurs. The standard annealing process used in the fabrication of the transistors is according to these experiments performed at 400 °C for 1 minute. This annealing leads to a contact resistance of 0.12 Ω-mm which is good compared to those in the literature [33]. Figure 1.10 shows a photograph of the source and drain ohmic contacts after annealing.

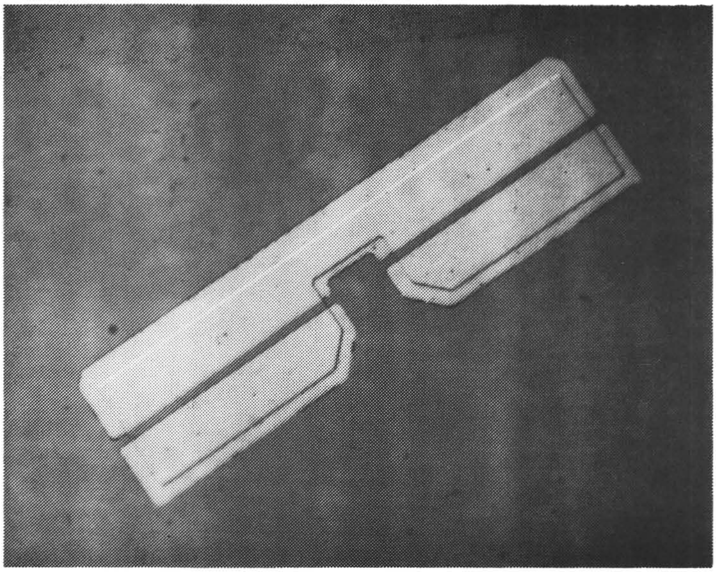

Figure 1.10, The ohmic drain and source contacts after the lift off process and annealing. The mesa is still visible.

1.4.4 The gate metallisation.

The process for the gate metallisation is comparable to the lift off process used for the ohmic contacts. The difference is the gate recess. After defining the gate pattern in the resist between the drain and the source and before the evaporation of the Schottky metallisation the recess etch is performed. The recess is done wet chemically in a NH_4OH : H_2O_2 : H_2O solution at room temperature. In later chapters processes will be described for dry etching of the recess. The importance of the gate recess is already mentioned in the theoretical discussion on the transistors. The etch is performed by subsequently etching and measuring the drain source saturation current. This is continued until an adequate saturation current is reached. In this way it is possible to fabricate enhancement and depletion mode transistors.
After the gate recess a titanium, platinum, gold (50 nm/20 nm/150 nm) Schottky metallisation is evaporated in the Leybold evaporator. The results after lift-off are shown in figures 1.11 and 1.12.

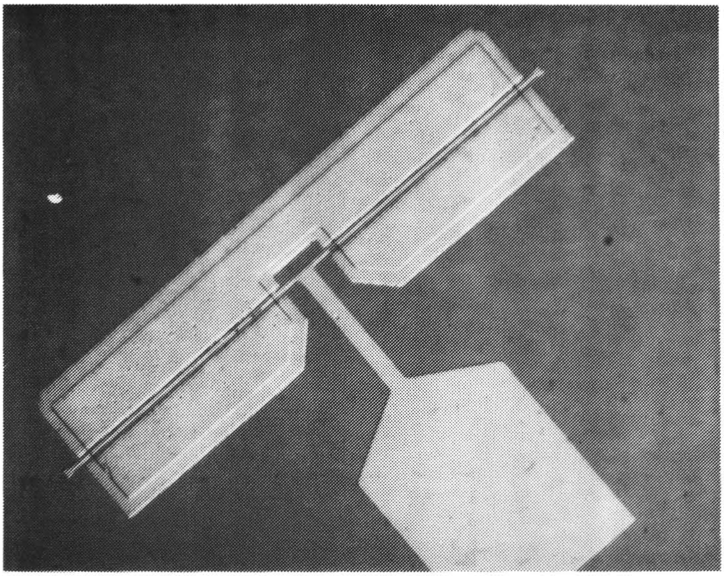

Figure 1.11, The 1 μm gate metallisation.

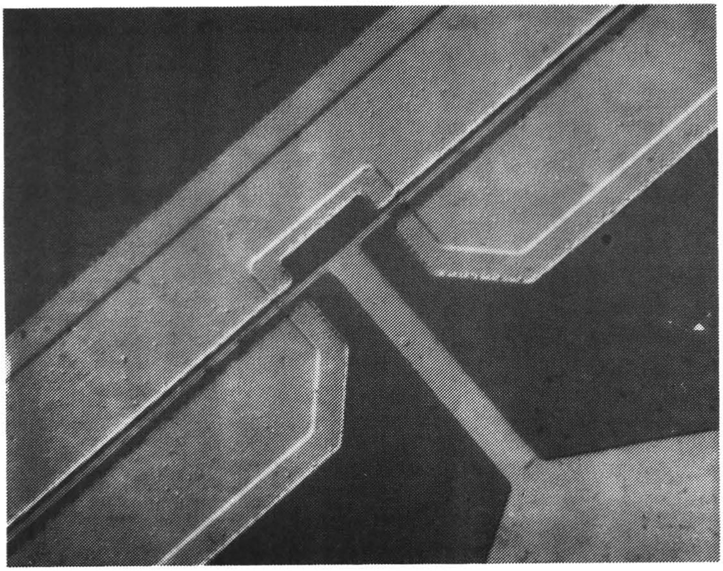

Figure 1.12, A detail photograph of the T-gate metallisation.

1.4.5 Cascade overlay metallisation.

The contact or overlay metallisation is made by a lift off technique. This metallisation is intended for contact paths necessary for the on-wafer high frequency measurements and the DC characterisation. The metallisation sequence is the same as used for the gate. Figure 1.13 shows the Cascade contacts and the completed transistor after processing of the fourth mask.

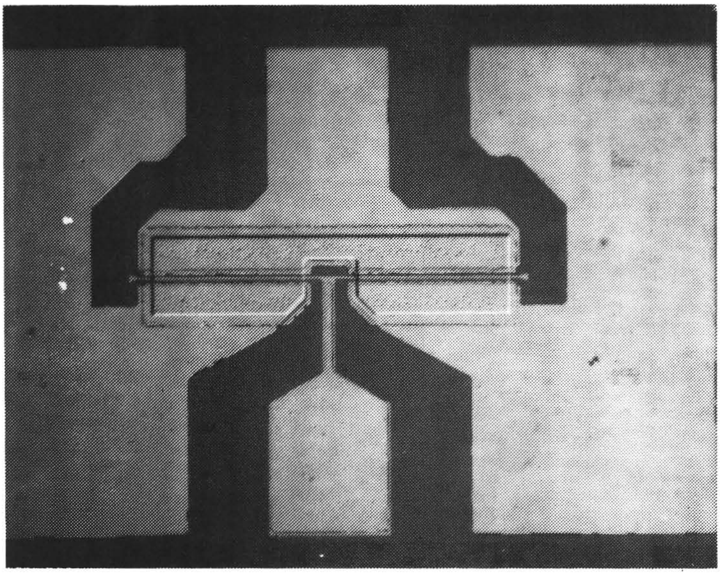

Figure 1.13, The completed transistor.

1.5 Electrical characterisation.

1.5.1 DC characterisation

As already mentioned, the drain to source current of field-effect transistors can be modulated by applying a DC bias to the gate with respect to the source. By decreasing the gate voltage of a MESFET the depletion layer extends more into the active layer and the conductivity of the current carrier layer is modulated. In a HFET the sheet charge density is modulated by the gate voltage. In both cases the drain to source saturation current changes. The variation in this saturation current as a function of a change in the gate voltage is expressed by the transconductance (See figure 1.14 and 1.15). The transconductance g_m is defined as:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{1.22}$$

The transconductance is usually expressed in mmho/mm or mS/mm and increases with decreasing gate length. The transconductances observed for HFETs are usually higher than those of MESFETs. This is because the HFETs have a better carrier confinement and the distance between the gate and the 2-DEG is strongly reduced.

The source resistance of a transistor has a significant influence on the external measured transconductance. The source resistance is defined as the sum of the contact resistance R_c and the resistance of the GaAs path between the source and the channel R_s. The source resistance causes a negative feedback whose influence on the transconductance can be written as:

$$g_{m_{extern}} = \frac{g_{m_{intern}}}{1 + R_s \cdot g_{m_{intern}}} \tag{1.23}$$

The resistance can be minimised by a short gate-to-source distance and an adequate technology for ohmic contacts with low resistivity. The optimisation of the ohmic contact is already treated in paragraph 1.4.3. Another parameter which is often referred to is the output conductance g_d. This is the slope of the drain-to-source saturation current at a constant gate voltage with respect to V_{ds} (see also figure 1.14).

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}} \tag{1.24}$$

At the end of the chapter these parameters will be compared to those in literature.

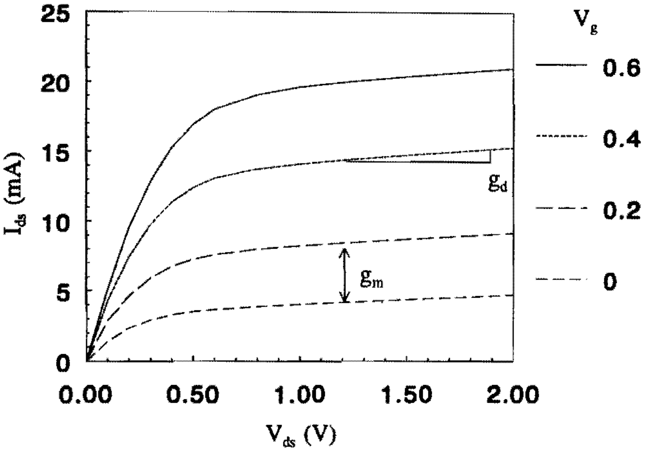

Figure 1.14, The drain-source current as a function of the drain-source voltage V_{ds} at different gate voltages V_g for a pseudomorphic HFET. The HFET has a gate length of 1 μm and a width of 100 μm. The transconductance g_m and the output conductance g_d are shown schematically.

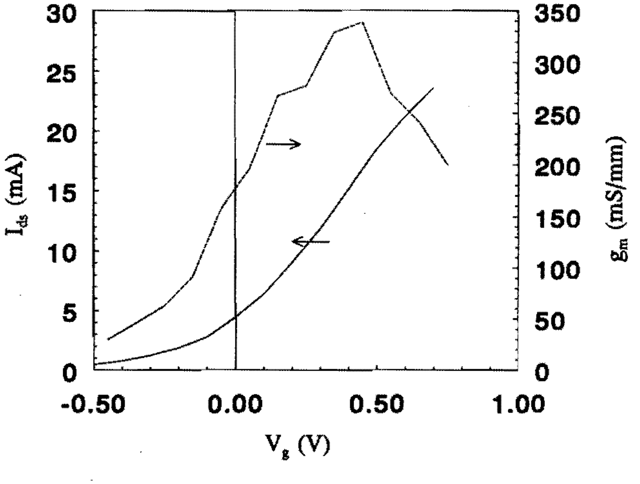

Figure 1.15, The transconductance g_m and the drain-source current I_{ds} as a function of the gate voltage V_g for the pseudomorphic HFET mentioned above (V_{ds} = 2 V).

1.5.2 High frequency measurements.

1.5.2.1 S-parameters

The performance of the transistors is characterised at microwave frequencies ranging from 45 MHz to 40 GHz. The S-parameters or scattering parameters represent the reflection and the transmission coefficients. This is shown schematically in figure 1.16. S_{11} and S_{22} represent the reflection coefficients at the input and output respectively. S_{12} and S_{21} represent the transmission coefficients. They are measured on wafer with a HP 8510 network analyzer and represented in polar plots and Smith charts. For a wet chemically processed pseudomorphic HFET with gate length of 1 μm and width 100 μm figure 1.17 shows an example of these measurements.

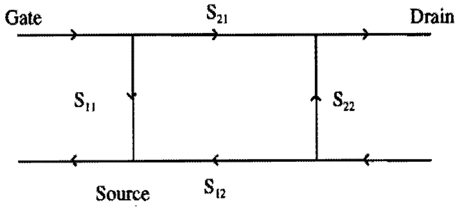

Figure 1.16, The microwave representation of the transistor twoport and the explanation of the different S-parameters.

From these measurements other parameters can be derived such as:

- The Maximum Available Gain (MAG):	is the gain if the transistor is unconditional stable.
- The Maximum Stable Gain (MSG):	is the gain if the transistor is not unconditional stable. The transition between these two parameters is determined by the k-factor which can be deduced from the measurements.
- f_t : the cut off frequency	is the frequency of unity current gain.
- f_{max} :	is the maximum frequency of oscillation or unity power gain frequency.

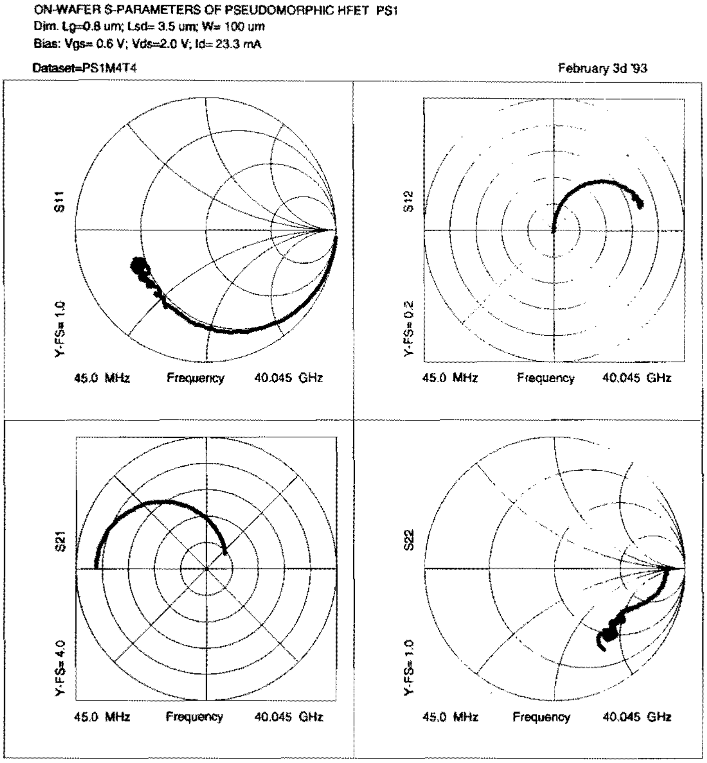

Figure 1.17, The different S-parameters in polar plots and Smith charts for a 1 * 100 µm pseudomorphic HFET as function of the frequency. S_{11} and S_{22} represent the reflection coefficients at the input and output respectively. S_{12} and S_{21} represent the transmission coefficients

From these S-parameters the parameters of a small-signal equivalent circuit can be extracted. An example of such a circuit is shown in figure 1.18.

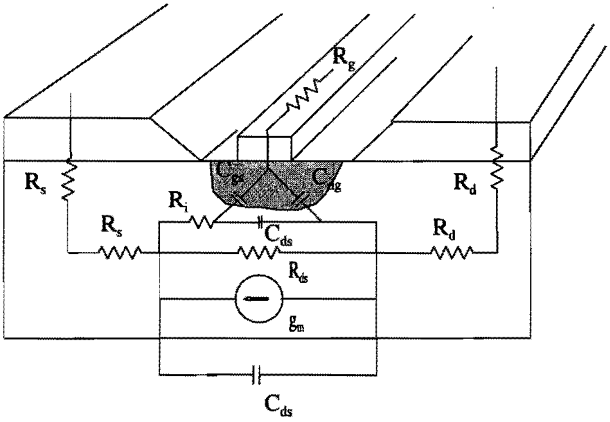

Figure 1.18, The small signal equivalent circuit of a MESFET.

For the 1 * 100 μm wet chemically processed pseudomorphic HFET the maximal stable and maximal available gain are shown in figure 1.19. Figure 1.20 shows the unilateral power gain and the current gain from which the maximum frequency of oscillation f_{max} and the frequency of unity current gain f_t are extracted. The cut off frequency, measured for a conventional AlGaAs/GaAs HFET, is generally lower than for the pseudomorphic HFET. This is explained by a lower modulation efficiency [34] and a lower electron saturation velocity under the gate in the conventional HFET. The cut off frequency depends on the average electron velocity v_{avg} as $v_{avg}/2\pi \cdot L$. Beside the influence of the average velocity the cut off frequency increases with decreasing gate lengths [35,36].

The parameters extracted for the equivalent circuit of this HFET are listed in figure 1.21. The DC characteristics have been shown in Figure 1.14 and 1.15 in the previous paragraph.

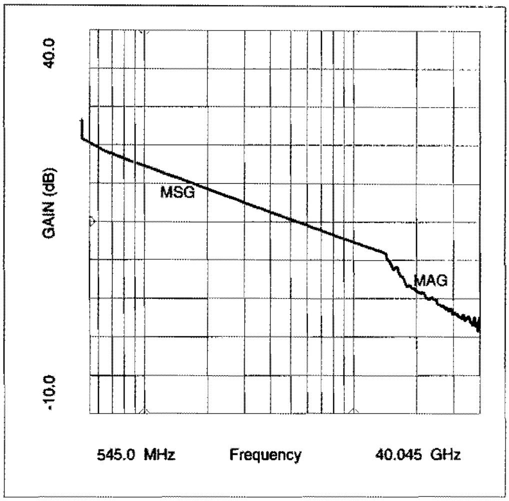

Figure 1.19, The maximum stable gain (MSG) and the maximum available gain (MAG) as function of the frequency for a 1 * 100 μm pseudomorphic HFET.

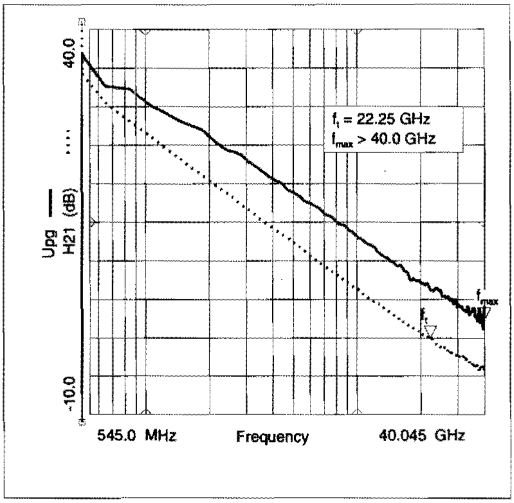

Figure 1.20, The current gain H_{21} and the unilateral power gain U_{pg} from which the frequency of unity current gain f_t and the maximum frequency of oscillation f_{max} are determined.

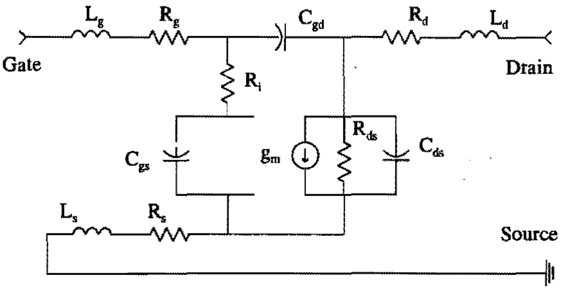
L_g
R_g
C_{gd}
R_d
L_d
Gate
Drain
R_i
C_{gs}
g_m
R_{ds}
C_{ds}
L_s
R_s
Source

Figure 1.21, The small signal equivalent circuit for the above mentioned pseudomorphic HFET. The extracted parameters from the simulation are listed below.

The extracted S-parameters are:

W = 100 µm,
L = 1 µm,

R_g = 7.1 Ω,
R_s = 0.5 Ω,
R_d = 0.5 Ω,
R_i = 6 Ω,
R_{ds} = 750 Ω,

g_m = 36.4 mS,
τ_{delay} = 3.0 ps,
Angle = 0 degree,

L_g = 1.2 pH,
L_s = 6.7 pH,
L_d = 10.0 pH,

C_{gs} = 260 fF,
C_{gd} = 34 fF,
C_{ds} = 16 fF.

1.5.2.2 Noise Figure (NF).

The Noise Figure (NF) represents the noise performance of a transistor. It corresponds to the signal to noise ratio of the input signal divided by the signal to noise ratio of the output signal. The noise factor is usually expressed in dB and is defined as:

$$NF = \frac{(\frac{signal}{noise})_{inp}}{(\frac{signal}{noise})_{out}} \tag{1.25}$$

The noise figure is a function of the measurement frequency, the applied DC bias voltages and the matching. Obtaining the minimal noise figure NF_o requires the optimisation of these parameters. According to Fukui the minimal noise figure can be defined as [37]:

$$NF_o = 1+2\pi \cdot K_f\, f\, C_{gs} \cdot \sqrt{\frac{(R_s+R_g)}{g_m}} \cdot 10^{-3} \tag{1.26}$$

Here K_f is a material and frequency dependent constant, f the frequency in GHz and C_{gs} the gate to source capacitance in pF. The source resistance needs to be minimised to obtain a low noise figure. This resistance can be improved by a short gate to source distance, to minimise the resistance in the GaAs path, and in a second way by optimising the contact resistance between the ohmic metallisation and the active GaAs layer. Further more the noise can be reduced by decreasing the gate length though its influence on the gate to source capacitance.

Some measurements have been made on the noise performance of MESFETs and pseudomorphic HFETs. The results of these measurements will be presented at the end of this chapter.

1.6 Results.

The next pages show some typical results obtained on MESFETs, AlGaAs/GaAs HFETs and pseudomorphic AlGaAs/InGaAs/GaAs HFETs. First the layer structure will be shown, then the parameters extracted from the DC and microwave measurements. The contact resistances are measured with the transmission line method. Finally the noise figures of typical MESFETs will be compared to those of pseudomorphic HFETs.

1.6.1 MESFETs.

wafer number : W314 E3 FET

layer structure:

caplayer	$2\cdot10^{18}$	cm^{-3} (Si)	20	nm	n^+-GaAs,
active layer	$3\cdot10^{17}$	cm^{-3} (Si)	200	nm	n-GaAs,
buffer layer	undoped		2	µm	GaAs,

S.I. GaAs substrate.

Fet 9 M4T1:

DC characterisation

L	gate length			1	µm,
L_{ds}	drain-source separation			4	µm,
W	gate width			150	µm,
$I_{ds,sat}$	$V_g = 0$ V,	$V_{ds} = 2.0$ V		33.2	mA,
g_m	$V_g = 0$ V,	$V_{ds} = 2.0$ V		176	mS/mm,
$g_{m,max}$	$V_g = 0.25$ V,	$V_{ds} = 2.0$ V		190	„
g_d	$V_g = 0$ V,	$V_{ds} = 2.0$ V		6.7	mS/mm,
V_T				-2.0	V.

TLM measurement

R_c	0.12	Ω-mm

HF characterisation

measured at $V_{ds} = 2.0$ V, $V_g = +0.25$ V and $I_{ds} = 38.03$ mA.

f_t	16.8	GHz,
f_{max}	35.4	GHz.

1.6.2 AlGaAs/GaAs HFETs.

wafer number : MO383-3*

layer structure:

caplayer	$3.5\cdot10^{18}$	cm^{-3} (Si)	90	nm	n^+-GaAs,
donor layer	$1.5\cdot10^{18}$	cm^{-3} (Si)	50	nm	n-$Al_{0.23}Ga_{0.77}As$,
spacer	undoped		2	nm	$Al_{0.23}Ga_{0.77}As$,
buffer layer	undoped		0.8	µm	GaAs,

S.I. GaAs substrate.

HW1 M4T2:

DC characterisation

L	gate length	0.8	µm,
L_{ds}	drain-source separation	3.5	µm,
W	gate width	150	µm,
$I_{ds,sat}$	$V_g = 0$ V, $V_{ds} = 2.0$ V	39.8	mA,
g_m	$V_g = 0$ V, $V_{ds} = 2.0$ V	175	mS/mm,
$g_{m,max}$	$V_g = -0.5$ V, $V_{ds} = 2.0$ V	224	mS/mm,
g_d	$V_g = 0$ V, $V_{ds} = 2.0$ V	20.9	mS/mm,
V_T		-1.83	V,

TLM measurement

R_c < 0.1 Ω-mm.

HF characterisation

measured at $V_{ds} = 2.0$ V, $V_g = -0.50$ V and $I_{ds} = 17.80$ mA.

f_t	22.3	GHz,
f_{max}	36.1	GHz.

---

* This layer structure is grown at the Walter Schottky Institute of the Technical University of Munich.

1.6.3 AlGaAs/InGaAs/GaAs HFETs.

wafer number : W385 H79

layer structure:

caplayer	$2.0\cdot10^{18}$	cm^{-3} (Si)	70	nm	n^+-GaAs,
donor layer	$1.5\cdot10^{18}$	cm^{-3} (Si)	50	nm	n-$Al_{0.20}Ga_{0.80}As$,
spacer	undoped		3	nm	$Al_{0.20}Ga_{0.80}As$,
pseudo morphic lay.	undoped		15	nm	$In_{0.15}Ga_{0.85}As$,
buffer layer	undoped		1.5	μm	GaAs,
S.I. GaAs substrate.					

PS1 M4T4:

DC characterisation

L	gate length		0.8	μm,
L_{ds}	drain-source separation		3.5	μm,
W	gate width		100	μm,
$I_{ds,sat}$	$V_g = 0$ V,	$V_{ds} = 2.0$ V	4.42	mA,
g_m	$V_g = 0$ V,	$V_{ds} = 2.0$ V	158	mS/mm,
$g_{m,max}$	$V_g = 0.5$ V,	$V_{ds} = 2.0$ V	340	mS/mm,
g_d	$V_g = 0$ V,	$V_{ds} = 2.0$ V	6.8	mS/mm,
V_T			-0.64	V,

TLM measurement

R_c	< 0.1	Ω-mm

HF characterisation

measured at $V_{ds} = 2.0$ V, $V_g = +0.5$ V and $I_{ds} = 18.50$ mA.

f_t	22.4	GHz
f_{max}	≥ 45	GHz

1.6.4 The Noise Figure (NF).

The noise Figures of 1.2 * 200 μm^2 MESFETs and pseudomorphic HFETs have been measured at a frequency of 1 GHz. The MESFET (FET6 M1T10) is biased with a drain source voltage of 2 Volt and a gate to source voltage of -0.6 Volt. The drain source current at this bias levels is 20.0 mA. The measured noise figure was 2.4 dB with an associated gain of 13.7 dB. This is a representative value for the different MESFETs measured. The bias conditions for the pseudomorphic HFET are respectively V_{ds} = 2.0 V, V_{gs} = + 0.3 V and an I_{ds} of 20.0 mA. The noise figure observed for the pseudomorphic HFET was 1.5 dB with an associated gain of 18.1 dB. The measured noise figures and gains are respectively lower and higher for the pseudomorphic HFET. This can be dedicated to the spatial separation of the electrons and the donors atoms in the HFET structure. These measured noise figures can not be interpreted as the real minimal noise figure since no correction of the tuner losses and no output tuner is used.

1.7 Discussion.

In this paragraph the results obtained on wet chemically processed MESFETs as well as conventional and pseudomorphic HFETs are compared to those mentioned in literature.
The results obtained on the contact resistance are in good agreement with the literature. The contact resistance of 0.12 Ω-mm is obtained after annealing at a temperature of 400 °C for 1 minute. The importance of this low values for the measured external transconductance and noise figure has already been mentioned previously.
For MESFETs the transconductances are typically between 190 and 200 mS/mm. The obtained transconductances are comparable to literature for 1 μm gate length transistors. Golio [38] plotted the transconductances as function of the gate length for 137 values, reported in literature. Compared to these values the obtained transconductances are good. For the conventional and the pseudomorphic HFETs the transconductances are compared to those listed in references 6, 21 and 36. Ketterson [21] showed an increase of the transconductance with increasing indium content in the strained InGaAs layer. The transconductance increased from 253 to 310 mS/mm for an increase in indium concentration from 5 to 20 percent. This was measured for a 1 μm gate length transistor. The increase is comparable to our observed transconductances for AlGaAs/GaAs conventional and AlGaAs/InGaAs/GaAs pseudomorphic HFETs which were 220 and 340 mS/mm respectively.
The maximum frequency of oscillation and the cut-off frequency observed for MESFETs (typically 35 and 17 GHz respectively) are comparable to those listed by Golio [38]. The f_t and f_{max} for both types of HFETs are compared to those of Ketterson [21], Cheng [6] and Nguyen [36]. Cheng lists typical a f_t and f_{max} of 24.5 and 40 GHz for 1 μm gate pseudomorphic HFETs. Nguyen lists a f_t for conventional and strained HFETs of respectively 15 and 22 GHz. The observed values as function of the indium content, as measured by Ketterson, are listed in table 1.1.

	In 0 %	In 5 %	In 10 %	In 15 %	In 20 %
f_t (GHz)	12.0	19.0	18.5	21.5	24.5
f_{max} (GHz)	30.5	36	34.5	37	40
g_m (mS/mm)	-	253	234	270	310

Table 1.1, The cut off frequency, maximum frequency of oscillation and transconductances reported by Ketterson [21] for different indium contents of the strained InGaAs layer in pseudomorphic HFETs.

There is an increase in both frequencies from conventional to the pseudomorphic HFET. Although our results show an increase in the measured f_{max} only a small increase was observed in the cut-off frequency. The cut off frequency and the maximum frequency of oscillation for the conventional HFET were 22 and 36 GHz respectively. The pseudomorphic HFET showed an identical f_t but f_{max} was ≥ 45 GHz. The results are however comparable to those obtained in literature.

It is difficult to compare the noise figures with literature since these are normally measured at higher frequencies. At the moment our noise measurements are limited to a frequency of 1.6 GHz. It is however clear that the observed noise figures are high. These high values can be explained by a high gate resistance. The influence of this resistance on the noise figure is stated in the Fukui equation 1.26. The high gate resistance is due to a thin (150 nm) gate metallisation. For this reason a T-gate technology is often used in submicron field-effect transistors.

In general it can be concluded that the wet chemical technology, developed for GaAs-based field-effect transistors, is able to produce transistors with good performances. The DC and high frequency measurements show results which are in agreement with the literature for 1 μm gate length transistors. In later chapters these results will be used for comparison to dry processed transistors

1.8 References

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CHAPTER II

The influence of argon cleaning on GaAs-based Schottky diodes and MESFETs.

2.1 Introduction.

Ion-milling (or etching) can be used for pattern transfer or in-situ cleaning prior to an evaporation. During the milling process atoms are removed mechanically from the target. This is performed by bombardment with ions or neutral atoms with a certain energy. It is however required that minimal crystal damage will be introduced by this bombardment. This can be realised with ions/atoms having low bombardment energy. The damage, which is even introduced at low energies, can be recovered during a heat treatment. Such a heat treatment is however not desirable.

Much research has been done on the damage introduced in GaAs by ion milling. This damage has been analysed by many different techniques like Transmission Electron Microscopy [1] (TEM), Deep Level Transient Spectroscopy [2,3,4] (DLTS), Rutherford Backscattering Spectrometry [5] (RBS), Photo-Luminiscence [6] (PL) and electrical characterisation of electronic components [6-11]. With the last technique mainly Schottky diodes are evaluated by I-V and C-V measurements.
There is little known about the projected range of the damage in literature. The damage is often related to point defects, such as vacancies or interstitials, which can extend to a high degree of crystal disorder. The extension of the damage observed in GaAs ranges between less than 10 nm to 100 nm [1,6,10,12]. Although it is clear that the near-surface region is strongly disordered some damage extends deeper into the material. The amount of damage also depends on the mass of the ions/atoms used [6]. Heavy ions like xenon have a smaller penetration depth and produce less damage than light atoms like neon. Reduction of the damage is also improved by adding a reactive gas like chlorine (Cl_2) near to the sample. In this case the etch is partial chemical and this kind of milling is known as Chemical Assisted Ion Beam Etching CAIBE.

In this chapter the influence of ion etching/cleaning with neutral and ionised argon species is investigated on the electrical behaviour of practical GaAs devices. The effects of argon cleaning on GaAs Schottky diodes and MESFETs are described. These experiments are done to determine if it is preferable to introduce an additional process step to obtain a clean GaAs surface before evaporation of the Schottky metallisation in transistor fabrication. The diodes and MESFETs are fabricated using the structure mentioned in the previous chapter.
After defining the resist pattern for the gates of a MESFET and the diodes, the highly

doped toplayer is removed wet chemically in a diluted ammonia-hydrogenperoxide ($NH_4OH:H_2O_2:H_2O$) solution at room temperature. Before evaporation of the Ti/Pt/Au Schottky metallisation the GaAs surface is cleaned in-situ with an argon beam. The experiments are done with neutralised and ionised argon beams at different energies. The diodes are characterised by I-V and C-V measurements and the MESFETs by I-V and high frequency S-parameter measurements. The results of these measurements are compared to a device whose toplayer was removed wet chemically. The recovery of the damage, introduced by this process, is studied as function of the annealing temperature.
The first part of the chapter will deal with the experiments with a neutralised argon beam. First the characteristics of the ion source and some additional theory on Schottky diodes will be described. Paragraphs 2.5 and 2.6 deal with the influence of argon cleaning with a neutralised beam on diodes and transistors respectively. Paragraph 2.7 describes identical measurements with an ionised argon beam. Finally the results will be discussed in paragraph 2.8.

2.2 The characteristics of the ion-gun.

The plasma of the ion-gun, a Leybold IQ 70, is maintained in a quartz cylinder. This cylinder is surrounded by a RF induction coil which is necessary to maintain the plasma. The RF power is supplied at a frequency of 13.56 MHz and the power ranges up to 700 W. Matching of the reflected RF power is done automatically. The plasma is ignited by an argon purge while the RF is already on. Beside argon it is also possible to use oxygen. The Ar ions are extracted from the plasma by three aluminium-oxide grids. The first grid (positively biased), which is nearest to the plasma, determines the energy of the ions. This energy can be varied between 50 and 2000 eV. Between the first and the second grid (negatively biased) the ions are accelerated. The third grid (earth) is needed to set the energy of the ions back to their initial value of the first grid. Above the grids there is a tungsten filament to neutralise the beam. The beam diameter is 70 mm. The ion current can be measured with a Faraday cup located between the ion gun and the target.

Figure 2.1 shows the extracted argon ion current as function of the voltage on the second grid. This is shown for different beam energies. The extracted beam current increases with increasing voltage on the second grid until saturation of the ion current occurs. This experiment is performed at a RF power of 270 Watt and a chamber pressure of $1.9 \cdot 10^{-4}$ mbar, initiated by an argon flow of 4 sccm. A 1000 to 1500 Volt difference between the first and the second grid is optimal. This is to minimise the current through the second grid which is necessary to prolong the lifetime, before maintenance, of the ion source.
Figure 2.2 shows the influence of the RF power on the extracted ion current. The increase is not as pronounced as the influence of the second grid. In this case the current on the second grid increases linearly with the RF power. For this reason a RF power of 270 Watt is chosen in the standard process.
No significant influence of the argon flow (4-25 sccm) on the extracted current could be observed. It needs to be mentioned that the measured current density is very sensitive on the condition of the grids. The extracted current rapidly decreases with contamination, resulting from the beam, on the grids.

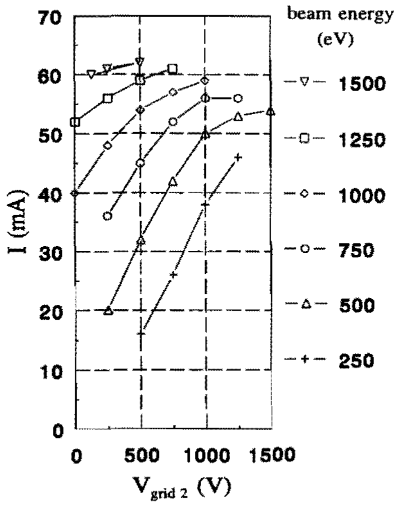

Figure 2.1, The argon ion current as function of the voltage on the second grid as measured by a Faraday cup. This is shown for different argon ion energies. The RF power is 270 Watt and the pressure is $1.9 \cdot 10^{-4}$ mbar.

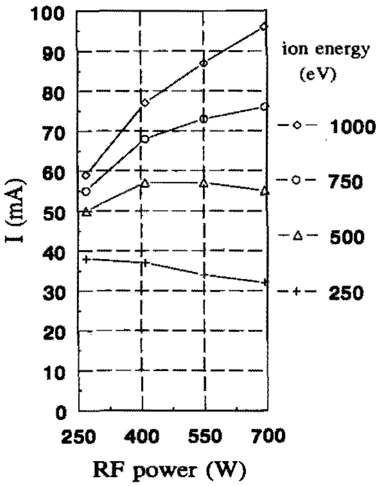

Figure 2.2, The influence of the RF power on the extracted ion current. This is shown for different ion energies. The voltage on the second grid was 1000 Volt and the pressure was $1.9 \cdot 10^{-4}$ mbar.

The parameters used during the experiments are given below. Table 2.1 lists the extracted current densities and the normalised etch rates of GaAs at different argon energies. These etch rates are obtained with a neutralised beam. The etch rates are normalised to the extracted current density. These etch rates appear to be consistent with previously reported values [1,5].

Resist masks are not resistant to long exposure times. Even at the lower argon energies the resist carbonises. Since the source is dedicated for short cleaning processes no problems occur with the compatibility of the argon cleaning process and the lift off process. After ion milling the GaAs surface appeared very smooth in the Scanning Electron Microscope (SEM). GaAs seems to be little sensitive to a preferential sputtering of arsene. This is due to a small mass difference between the gallium and arsine atoms. In the case of InP preferential sputtering of phosphor leads to the formation of indium droplets remaining on the surface [1]. During the fabrication of the GaAs MESFETs and diodes the time of the cleaning (etch) step at different energies was kept constant. The samples were cleaned for 10 seconds.

Process parameters:			
	- chamber pressure	$1.8 \cdot 10^{-4}$	mbar,
	- argon flow	4	sccm,
	- beam diameter	70	mm,
	- RF power	270	Watt.

energy (eV)	current density (mA cm^{-2})	normalized etch rate (nm s^{-1} mA^{-1} cm^{-2})
50	0.62	1.1
125	0.81	1.2
250	0.99	1.8
500	1.17	2.3
750	1.25	2.9

Table 2.1, The dependence of the current density and the normalised etch rate on the ion energy. The etch rates are obtained with a neutralised argon beam.

2.3 Theory of Schottky diodes.

In addition to the theory of Schottky diodes in chapter 1 this paragraph describes the theory on the origin of the depletion layer in the semiconductor and the mechanisms behind the rectifying behaviour. Figure 2.3 shows the band diagram of an ideal metal-semiconductor Schottky contact. To obtain a constant Fermi level a charge exchange between the metal and semiconductor occurs. Due to this exchange there is a depletion of carriers in the semiconductor and a potential barrier is formed at the GaAs side of the interface. The barrier height $q\Phi_b$ is the difference between the metal work function $q\Phi_m$ and the electron affinity $q\chi$ of the semiconductor,

$$q\phi_b = q(\phi_m - \chi) \tag{2.1}$$

The metal work function is the energy difference between the Fermi level E_F and the vacuum. The electron affinity is the energy difference between the conduction band edge and the vacuum in the semiconductor. See also figure 2.3.

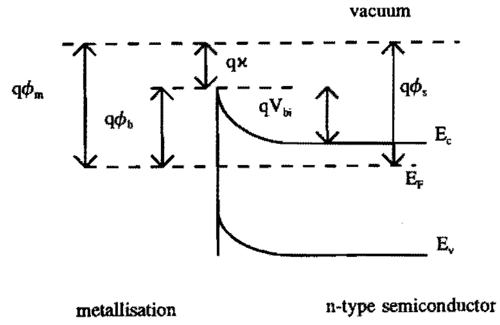

Figure 2.3, The band diagram of a metal-semiconductor Schottky contact.

The built in voltage V_{bi} can be written as in equation 2.2. The built-in voltage is only dependent on the difference in work function between the metal and the semiconductor.

$$q \cdot V_{bi} = q \cdot (\phi_m - \phi_s) \tag{2.2}$$

In reality the built-in voltage does not scale as mentioned in equation 2.2. This is due to a large number of surface states, located in the bandgap at the interface, that have an influence on the actual barrier height. Pinning of the Fermi level is caused by these interface states and they determine the actual barrier height. Walukiewicz [13] explains the Fermi level pinning by defects which change their electrical characteristics depending on the position of the Fermi level (amphoteric native defects). He mainly considers Ga rich surfaces by which a $(V_{Ga} + As_{As})^{3-} \leftrightarrow (As_{Ga} + V_{As})^{3+}$ transition is responsible for pinning the Fermi level between 0.5 and 0.7 eV above the valence band. Here V_{Ga} is a gallium vacancy and the As_{Ga} antisite is an arsenic atom on the gallium site. A similar approach can be obtained for arsenic rich surfaces. The As_{Ga} antisite is also considered by others as a cause of Fermi level pinning [14].

The ion source is meant for preparing a clean semiconductor surface to prevent residual oxide and to minimize defects at the metal semiconductor interface. Kellner [15] describes the influence of these surface states on the behaviour of the metal-semiconductor Schottky contacts.

The rectifying behaviour in the I-V characteristics of these contacts is described by Sze [16]. According to the Schottky diode equation the current can be written as:

$$I = I_s\left(e^{q \cdot \frac{(V - IR_s)}{n k_b T}} - 1\right) \tag{2.3}$$

with

$$I_s = A^{**} T^2 e^{-q \frac{\phi_b}{k_b T}} \tag{2.4}$$

In these formulas IR_s is the voltage drop due to the series resistance R_s, k_b is the Boltzmann constant, A^{**} is the Richardson constant for free electrons, I_s the saturation or leakage current and n the ideality factor.

With these formulas the ideality factor n, the barrier height ϕ_b and the saturation current I_s are determined from the forward I-V characteristics. In the case of an ideal Schottky contact the ideality factor is equal to 1. The parameter extraction is done in the voltage range where the local ideality factor n^* is nearly constant. The local ideality factor is given by,

$$n^* = \frac{k_b T}{q} * \frac{\delta V}{\delta \ln(I)} \tag{2.5}$$

This is clarified with help of figure 2.4 where the forward I-V characteristic of a reference diode is shown. The extracted local ideality factor of the I-V curve is shown with the open markers. It is clear that within a certain voltage range the local ideality factor remains constant.

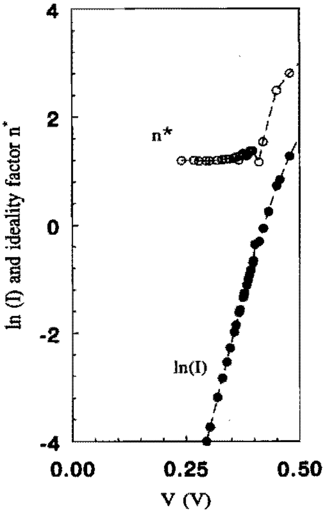

Figure 2.4, The forward I-V characteristics of a control diode. For every bias point the local ideality factor n^* is determined. This local ideality factor is shown with the open markers.

2.4 Fabrication technology.

The Schottky diode as well as the MESFETs have been processed using the MBE structure as described in chapter 1. The layer structure consists of:

20	nm	n^+-GaAs	$2 \cdot 10^{18} cm^{-2}$	top or contactlayer.
200	nm	n-GaAs	$3 \cdot 10^{17} cm^{-2}$	active layer.
2	μm	GaAs	undoped	buffer layer
semi-insulating GaAs substrate.				

Figure 2.5 shows schematically the diode. The Schottky diode (200*200 μm^2), situated in the active layer, is surrounded by an ohmic contact.

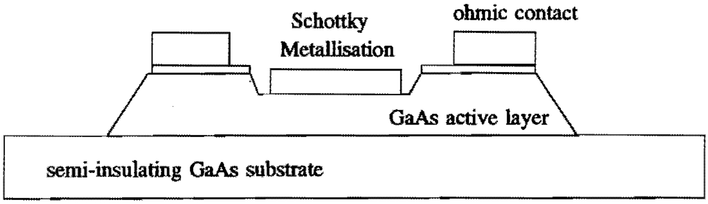

Figure 2.5, Schematic cross section of a 200 * 200 μm^2 diode which is surrounded by an ohmic contact. The gate metallisation is below the highly doped toplayer in the active GaAs layer.

First the mesa is defined and the ohmic contacts are evaporated and annealed. After defining the Schottky diodes in the resist the GaAs toplayer is removed wet chemically. Before loading the sample in the evaporator the GaAs surface is cleaned in diluted ammonia to remove any residual oxide from the surface. In the evaporator the GaAs surface is cleaned with a neutralised argon ion beam at energies ranging from 50 to 500 eV for 10 seconds. In-situ a Ti/Pt/Au Schottky metallisation is evaporated. After lift off the diodes and the MESFETs are completed. A detailed description of the manufacturing process of diodes is given in Appendix A.

2.5 The effect of Ar cleaning on diodes.

The reverse and forward I-V characteristics of diodes processed at energies from 50 to 250 eV with a neutralised argon beam are shown in figures 2.6 and 2.7 respectively. These characteristics are obtained prior to any heat treatment. The samples are compared to those which were cleaned in an ammonia solution. In both directions (forward and reverse) the performance degrades with higher argon energy.

Table 2.2 lists the parameters extracted from I-V and C-V measurements of the in-situ cleaned diodes. The parameters are compared to a wet chemically cleaned diode. In comparison with the wet chemical cleaned diodes the ideality factor (n) of the argon cleaned diodes are higher while the barrier heights (ϕ_b) are lower. The barrier heights listed in table 2.2 are extracted from the I-V characteristics. The leakage current I_s increases with increasing argon energy and is higher than that of the control sample.
The C-V measurements are performed using a HP 4280A at a frequency of 1 MHz in reverse bias. The C-V curves could not be measured satisfactory as function of the applied voltage due to a high leakage current in these diodes. The zero voltage capacitances, given in table 2.2 increase if the GaAs is cleaned with argon.
The breakdown voltage is defined as the voltage in reverse bias where the leakage current is 100 μA. This voltage decreases (becomes less negative) with increasing energy and is much lower than the breakdown voltage of the control diode. From table 2.2 it is clear that argon cleaning, even at low energies, introduces much damage to the GaAs active layer.

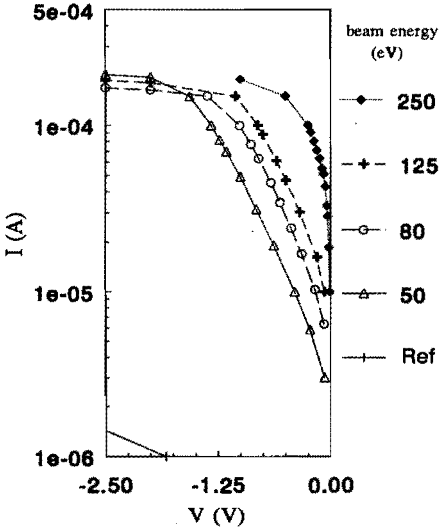

Figure 2.6, The reverse I-V characteristics of the diodes cleaned with a neutralised argon beam at different energies.

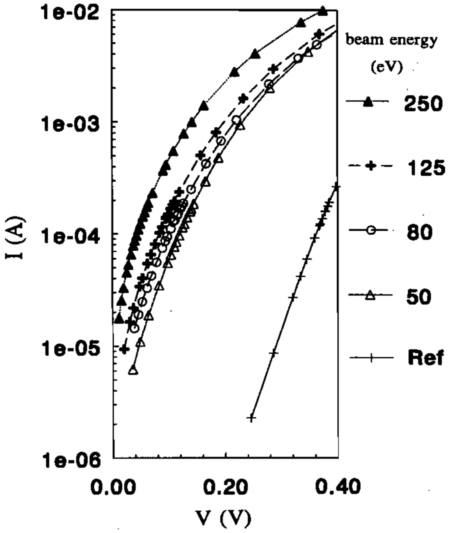

Figure 2.7, The forward I-V characteristics for diodes cleaned with a neutralised argon beam at energies up to 250 eV compared to a reference diode.

energy (eV)	ideality factor n	barrier height ϕ_b (V)	leakage current I_s (A)	capacitance C_o (pF)	breakdown voltage V_{br} (V)
Reference	1.22	0.72	$9*10^{-10}$	74	<-8
50	1.57	0.52	$4.8*10^{-6}$	83	-1.31
80	1.47	0.51	$6.8*10^{-6}$	85	-1.03
125	1.38	0.50	$8.9*10^{-6}$	86	-0.75
250	1.42	0.47	$3.1*10^{-5}$	93	-0.25
500	1.55	0.48	$2.0*10^{-5}$	86	-0.37

Table 2.2, The parameters extracted from the I-V and C-V measurements on the diodes (200 * 200 μm^2) cleaned with a neutralised argon beam at different energies before annealing. The results are compared to a wet chemically cleaned control diode.

A heat treatment is performed to determine if this damage could be recovered. The diodes are treated at temperatures ranging from 200 to 300 °C for 24 hours in a nitrogen ambient. Above 300 °C the surface of the diodes and the Ge/Ni/Au ohmic contacts became rough. Annealing at a temperature equal or less to 200 °C did not show any influence on the I-V characteristics.
Figure 2.8 to 2.11 show the influence of annealing on The I-V characteristics of diodes cleaned at 50, 80 and 250 eV. The legends show respectively the energy of the neutralised argon beam and the annealing temperature. For 50 and 80 eV the diodes show an improvement in the forward and reverse characteristics with increasing annealing temperature. This is also observed using an energy of 125 eV. The recovery is most remarkable on diodes cleaned at 50 eV and annealed at a temperature of 300 °C. In this case the saturation current decreases nearly 4 decades and is even lower than the unannealed control diode. The result is comparable to the control sample after having a heat treatment at 250 °C. No further improvement was observed for the control diode treated at 300 °C.

The reverse characteristics of diodes cleaned with argon with an energy less or equal to 125 eV also improve with a heat treatment. The characteristics, even at the lowest energy of 50 eV, are still worse than those of the control diode. This can be demonstrated by the breakdown voltage which is less negative for the cleaned diode at 50 eV compared to the reference diode.

The forward and reverse I-V characteristics at energies of 80 and 125 eV show the same tendency as the samples treated at 50 eV although the recovery is less pronounced. Table 2.3 shows the influence of a heat treatment on the ideality factor, the saturation current and the barrier height for 50, 80 and 125 eV compared to the reference diode.
The ideality factor and the barrier height only have a significant change after processing at an energy of 50 eV. Despite the argon cleaning no improved behaviour could be observed after cleaning and annealing compared to the annealed reference diode.
At the lowest possible energy (50 eV) the cleaning time was varied in 10, 20 and 40 seconds in order to determine the dependence of the cleaning time. In comparison with the 10 seconds cleaning step the I-V characteristics and the extracted parameters did not change with the cleaning time.

The influence of a heat treatment on the diodes cleaned at higher energies is different from those cleaned with an energy less than 125 eV. Figure 2.11 shows the forward and the reverse I-V characteristics of a diode cleaned at 250 eV. After annealing for 24 hours at 200 °C the characteristics are nearly ohmic for low bias voltages. The reverse characteristics degrade clearly with respect to the leakage current. This means that at higher energies it is not possible to restore the damage created by the argon cleaning.
It is therefore concluded that at higher energies the introduced damage becomes irreversible.

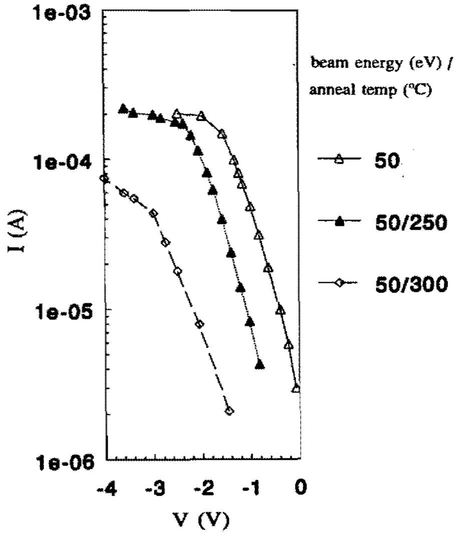

Figure 2.8, The reverse I-V characteristics of a diode cleaned with a neutralised argon ion beam at 50 eV annealed at different temperatures for 24 hours.

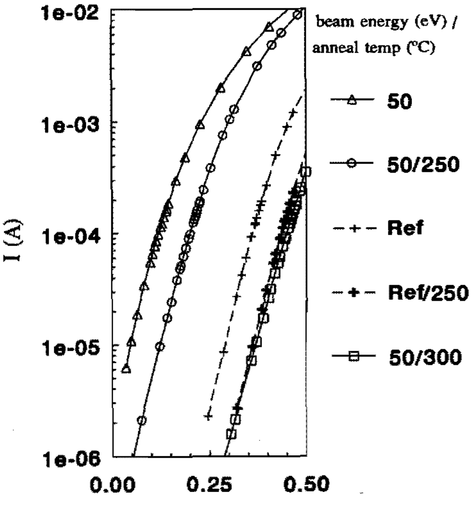

Figure 2.9, The forward I-V characteristics of a diode cleaned with a neutralised argon beam at 50 eV. The characteristics, annealed at different temperatures, are compared to a reference diode.

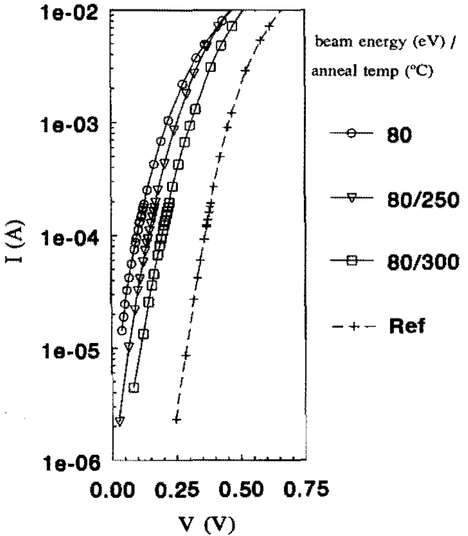

Figure 2.10, The forward I-V characteristics of a diode cleaned at 80 eV annealed at different temperatures for 24 hours. The characteristics are compared to a reference diode.

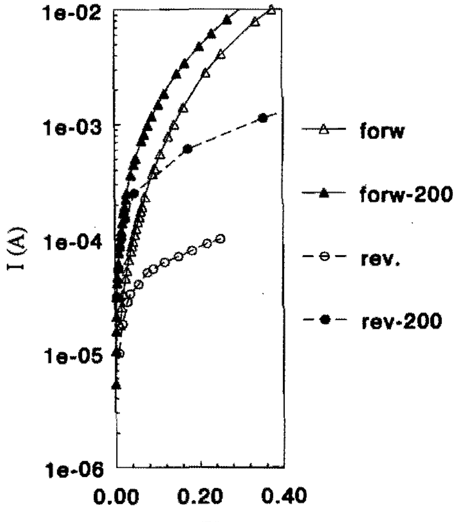

Figure 2.11, The forward and the reverse I-V characteristics of a diode cleaned at 250 eV with a neutralised argon beam. The characteristics are shown before and after annealing at 200 °C for 24 hours.

	50 eV heat treatment °C			80 eV heat treatment °C			125 eV heat treat. °C		control heat treatm. °C	
	-	250	300	-	250	300	-	300	-	250
n	1.57	1.45	1.47	1.48	1.47	1.47	1.37	1.58	1.22	1.27
I_s (A)	$4.8*10^{-6}$	$4.1*10^{-7}$	$5.0*10^{-10}$	$6.8*10^{-6}$	$2.0*10^{-6}$	$5.1*10^{-7}$	$8.9*10^{-6}$	$9.2*10^{-7}$	$9.0*10^{-10}$	$1.2*10^{-10}$
ϕ_b (V)	0.52	0.58	0.75	0.51	0.54	0.58	0.50	0.56	0.72	0.79

Table 2.3, The influence of a heat treatment on the ideality factor n, the saturation current I_s and the barrier height ϕ_b of Schottky diodes. The diodes are cleaned with a neutralised argon beam and annealed at different temperatures for 24 hours in a nitrogen ambient. These parameters are compared to a reference diode.

2.6 The influence of in-situ argon cleaning on MESFETs.

In addition to the influence of argon cleaning at different energies on Schottky diodes the influence on the I-V characteristics and the S-parameters of MESFETs is determined. Before evaporation of the Schottky gate metallisation the GaAs surface is cleaned in-situ with a 50 eV neutralised argon beam. Figure 2.12 shows the I_{ds}-V_{gs} and the transconductance g_m of a MESFET with a gate length of 1.2 μm and a gate width of 200 μm.

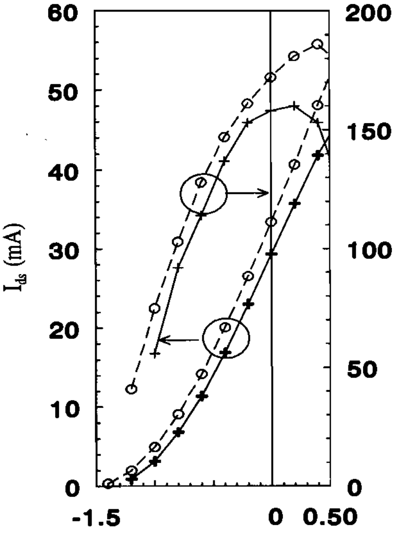

Figure 2.12, The influence of argon cleaning with a neutralised beam at 50 eV on the I_{ds}-V_{gs} characteristics and the transconductance of a 1.2 * 200 μm MESFET before (+) and after annealing (o) at 300 °C for 24 hours.

The strongest influence is at a positive gate bias. The transconductance increases remarkable after annealing at 300 °C. This improvement of the transconductance is typical for all energies used during these experiments, even those energies at which the diodes become very leaky after a heat treatment. This probably means that the improvement is mainly initiated by a recovery of the active GaAs layer. Also the channel current increases which probably indicates a removal of an electron trapping mechanism. The threshold voltage increases. All the MESFETs measured showed the same behaviour following ion cleaning and annealing.

Table 2.4 shows the gate current of a 1 * 100 μm MESFET cleaned at 50 eV, before and after the heat treatment at different positive gate biases. The gate current decreases after the heat treatment

V_{gs} (V)	I_g (mA) before	I_g (mA) after
0.2	0.02	0.004
0.4	0.12	0.03
0.6	0.46	0.18

Table 2.4, The influence of annealing at 300 °C for 24 hours on the gate current of a MESFET with a gate of 1 * 100 μm.

S-parameters are measured on wafer between 45 MHz and 40 GHz. The DC characteristics of this MESFET are shown in figure 2.12. The gate length is 1.2 μm and the width 200 μm. For the high frequency measurements the influence on the S-parameters is mainly observed for positive gate biases $V_g > 0.3$ V. The changes in the S-parameters occur at the input reflection coefficient S_{11} and the transmission coefficient from input to the output S_{21}.

The gain at low frequencies is increased from 8.1 to 10.6 dB as a consequence of annealing. The frequency of unity current gain f_t is increased from 7.3 to 9.4 GHz. This is measured at a gate voltage of 0.6 Volt. Below a gate voltage of + 0.4 V no difference in f_t was observed.

A circuit parameter extraction has been performed to study the influence of the argon treatment and annealing. This parameter extraction fits well with the measured S-parameters by introducing a resistance R_{gs} parallel to the input capacitance C_{gs}. This extra resistance is not necessary to fit a normally processed MESFET. In that case the resistance can be neglected because of its high value. The small-signal equivalent circuit used for the parameter extraction is already discussed in chapter 1. Table 2.5 shows some extracted parameters at different gate biases. The components at the gate input and those which change in a pronounced way are presented in this table.

	R_{gs} (Ω)		C_{gs} (pF)		R_i (Ω)	
V_g (V)	before	after	before	after	before	after
+ 0.6	44.9	222.1	0.90	0.85	7.5	3.4
+ 0.4	749	3060	0.56	0.61	7.0	6.0
+ 0.2	6790	6960	0.51	0.57	7.0	7.3
0	$15.6 \cdot 10^3$	$21.3 \cdot 10^3$	0.47	0.49	7.3	6.8
ref. 0.25	$1 \cdot 10^7$		0.29		7.2	

	g_m (mS)		R_{ds} (Ω)	
V_g (V)	before	after	before	after
+ 0.6	45.8	48.02	537	349
+ 0.4	39.83	41.65	445	360
+ 0.2	38.93	39.66	451	398
0	37.19	37.22	449	384
ref. 0.25	33.04		338	

Table 2.5, The circuit parameters extracted from the S-parameters before and after annealing at 300 °C for 24 hours as a function of the gate bias. The results are compared to a reference sample.

The influence of annealing at 300 °C on the channel resistance R_{ds} and on the parallel input resistance R_{gs} is very high. The parallel input resistance is very low compared to an identical MESFET fabricated without an argon cleaning process. The control MESFET is measured at a gate voltage of + 0.25 V.

The transconductance g_m is high in comparison to the DC measured transconductance. However by forcing the transconductance to a realistic value the fit to the S-parameters becomes worse. These measurements confirm that cleaning with a neutralised argon beam is not satisfactory for obtaining better device characteristics.

2.7 The influence of Ar^+ ion cleaning on Schottky diodes and MESFETs

The experiments are repeated on the same structure however now with an ionised argon beam. The normalised etch rates and the current densities as function of the argon energy are listed in table 2.6. The etch rates are much lower compared to the etch rates with a neutralised argon beam and are not comparable to etch rates listed in literature. The reason for these low etch rates is unknown.

In the Leybold evaporator the surface is cleaned with argon ions for 4 minutes at energies ranging from 50 to 750 eV. This process did not give problems of carbonised resist, even for the higher argon energies and for long exposure times.

energy (eV)	etch rate (nm min^{-1} mA^{-1} cm^{-2})	current density (mA cm^{-2})
50		0.52
125		0.78
250	~ 1	0.92
375		1.04
500	~ 1.1	1.07
750	~ 1.6	1.25

Table 2.6, The dependence of the GaAs etch rates and the current density on the energy of the argon ions. The etch rates are normalised to the extracted ion current.

Since it is required to remove a small oxide layer from the GaAs surface the influence on the Schottky diode behaviour is investigated. Figure 2.13 shows the influence of ion cleaning on the forward I-V characteristics of Schottky diodes. A linear fit to the measured characteristics is also shown. From these fits the different diode parameters are extracted with help of the Schottky diode equation. In contrast to the results observed with a neutralised beam the saturation current I_s increases with decreasing argon energy. Table 2.7 shows the dependence of the ideality factor n, the breakdown voltage V_{br}, the saturation current I_s and the barrier height ϕ_b as function of the ion energy. These results are obtained before annealing of the samples.

The ideality factor increases with increasing energy. At 750 eV the ideality factor is greater than 2 which is an indication of trap induced tunnelling effects at the interface. The barrier height of the cleaned samples is much lower compared to a reference sample. The breakdown voltage slightly increases (becomes more negative) with increasing argon energy. Although there is a certain lack of reproducibility in these experiments there is a tendency of a decreasing leakage current as well as an increasing ideality factor and breakdown voltage with increasing ion energy.

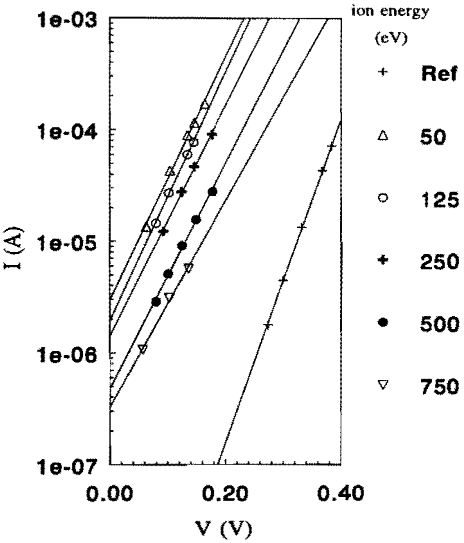

Figure 2.13, The dependence of the forward I-V diode characteristics on the ionised argon cleaning energy before annealing.

energy (eV)	ideality factor n	barrier height ϕ_b (V)	saturation current I_s (A)	V_{br} (V) (100 μA)
-	1.22	0.72	$9.0*10^{-10}$	<- 8.0
50	1.59	0.53	$3.2*10^{-6}$	- 1.25
125	1.60	0.55	$1.5*10^{-6}$	- 1.35
250	1.65	0.55	$1.3*10^{-6}$	- 1.44
375	1.54	0.56	$8.5*10^{-7}$	--
500	1.64	0.58	$6.6*10^{-7}$	- 1.57
750	2.1	0.58	$3.9*10^{-7}$	--

Table 2.7, The dependence of the from the forward I-V characteristics extracted parameters as a function of the ion energy compared to a reference diode.

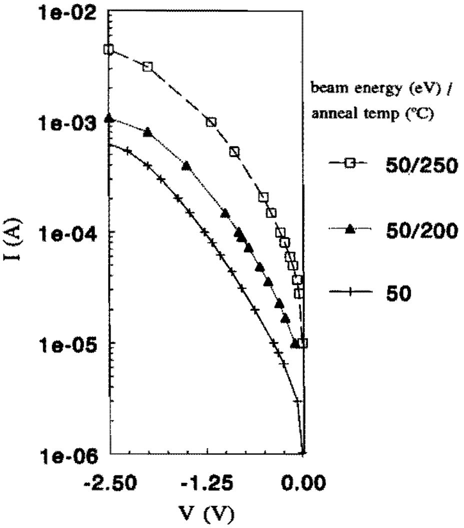

Figure 2.14, The reverse I-V diode characteristics after cleaning at 50 eV with an ionised argon beam before and after annealing at different temperatures for 24 hours.

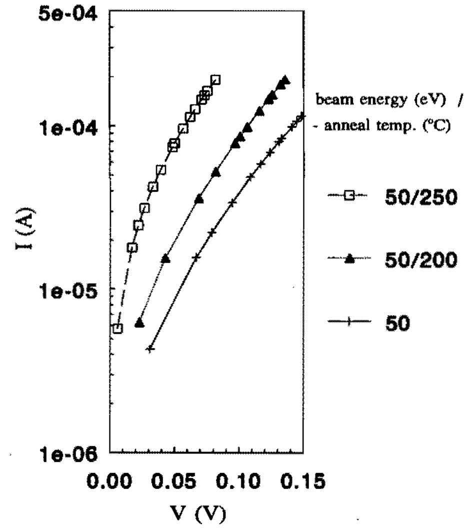

Figure 2.15, The influence of annealing for 24 hours on the forward I-V characteristics of a diode cleaned at 50 eV with an ionised argon beam.

A heat treatment is performed at temperatures of 200 and 250 °C for 24 hours. The influence of annealing on the forward and reverse characteristics is shown in figure 2.14 and 2.15 respectively. This is shown for a diode cleaned at 50 eV. The legends show respectively the ion energy and the annealing temperature. In contrast to the results observed with a neutralised beam the characteristics of the diode degrade upon annealing. This degradation occurs also for the higher argon energies. These results are unexpected since the effect of the ionised particles is expected to be the same as in the case of a neutralised beam.

MESFETs are also characterised during these experiments. Figure 2.16 shows the influence of annealing at 250 °C on a MESFET cleaned at 50 eV for 4 minutes. The curves with the open markers are the characteristics after annealing. Despite the degradation of the Schottky diodes after annealing the characteristics of the transistors are improved due to a recovery of damage in the active GaAs layer. At higher temperatures (300 °C) the characteristics improve further approaching the behaviour of a control transistor. In addition to the influence on the transconductance, the threshold voltage shifts towards the negative direction.
It is observed that the maximum in transconductance shifts to lower gate voltages with increasing ion energies. This can be explained by an extended degradation of the GaAs material. The threshold voltage also becomes more negative with increasing beam energy.

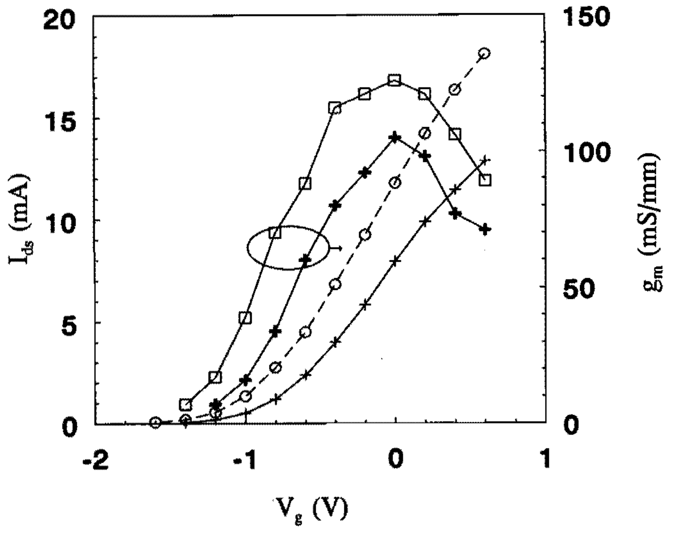

Figure 2.16, The influence of annealing at 250 °C for 24 hours on the I_{ds}-V_{gs} characteristics and the transconductance of a 1*100 μm MESFET. The open markers show the results after annealing.

2.8 Conclusions.

Our results with the neutralised beam are comparable to those mentioned in literature. Improvement of the results is probably obtained at lower argon energies. The minimum ion energy which could be obtained with the Leybold ion source (IQ 70) is 50 eV. The results obtained with the ion beam are not comparable to those in literature [5,11]. The results mentioned in literature with an ionised beam are for this reason compared to our experiments with a neutralised argon beam. The I-V characteristics of Schottky diodes, after cleaning with a neutralised argon beam, show a strong influence on the forward and reverse characteristics. The degradation is more pronounced at higher argon energies. Kwan et al. [10] obtained similar results on GaAs Schottky diodes. They explained the degradation by a preferential sputtering of arsenic atoms from the surface during argon cleaning. This arsenic depletion extends further into the material with higher energies. Full recovery of the diodes could not be achieved due to a gallium rich surface. At low energies the disordered surface recovers and the I-V characteristics improved after a heat treatment. At higher energies the defects are distributed upon annealing and a high degree of disorder occurs which makes the I-V characteristics worse. This is comparable to our results. At 50 eV the diodes are nearly full recovered. At 80 and 125 eV the diodes recover only partially and above 125 eV the rectifying behaviour nearly disappears. Identical results are also obtained by Pearton [1]. Neffati [9] showed by Schottky capacitance measurements that at low energies some additional interfacial states appeared. The shape of the barrier is greatly affected by the introduction of this interface charge. He observed that the ideality factor was closer to 1 than a wet chemical cleaned control diode for energies up to 150 eV. However the barrier height was reduced and could not be fully recovered. Good results are obtained by Hasni [7]. After cleaning at energies between 20-200 eV and annealing for 24 hours at 200 °C the ideality factor was improved, with respect to a control diode, for energies up to 125 eV. The leakage current was less or comparable to a control sample up to 100 eV and the barrier height was comparable to the control diode for energies up to 40 eV.

Compared to a wet chemically cleaned MESFET the I-V and microwave characteristics of a transistor treated with argon are worse. With respect to direct current measurements the transconductance and the gate leakage current at positive gate bias become lower and higher respectively. This after performing a heat treatment. After annealing the channel current increases which probably indicates a removal of an enhanced electron trapping and consequently a reduction in the drain source series resistance. This increase of channel current in MESFETs is comparable with the results of Chang [8]. The S-parameters showed a change in the input reflection coefficient (S_{11}) and the transmission coefficient from input to the output (S_{21}). A parameter extraction with the small equivalent circuit could only be fitted if an additional series resistance is included parallel to the gate input capacitance. In MESFETs fabricated without argon cleaning this resistance can be neglected because of its high value. Comparing the extracted circuit before and after annealing the strongest influence is observed in the channel resistance and the parallel input resistance. It is clear that most of the damage is introduced beneath the gate in the GaAs. This is expected since the GaAs surface was only cleaned at the gate region. Finally it can be concluded that it is not useful to add an argon beam cleaning step prior to the diode evaporation to improve the GaAs surface of the semiconductor.

2.9 References

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CHAPTER III

Metal Organic Electron-Cyclotron Resonance
Reactive Ion Etching.

3.1 Introduction

Dry etching offers many advantages over wet etching in the III-V semiconductor technology. General a better uniformity and reproducibility is obtained. Besides it is compatible with cluster tool systems. Dry processes often have a reactive or chemical and a physical or sputter component. The chemical element commonly gives a more isotropic profile than the sputter component. Usually gallium and aluminium containing semiconductors are processed in chlorine based chemistries whereas indium containing materials are etched in methane-hydrogen based plasmas.

There is an increasing interest in CH_4/H_2 plasma etching of III-V semiconductors after Niggebrügge et al. used this gas mixture in 1985 for InP [1]. This is because the alternative use of chlorinated gas mixtures like silicon tetrachloride ($SiCl_4$), chlorine (Cl_2) and boron trichloride (BCl_3) [2,3,4] have the disadvantages of being very corrosive and toxic. The alternative use of CCl_2F_2 [5,6,7] (Freon 12) minimises these problems however this gas is subjected to restrictions on its use because of environmental reasons, especially its effect on the ozone layer surrounding the earth. The advantages of $SiCl_4$, Cl_2 and BCl_3 is their low selectivity between GaAs and AlGaAs. They provide smooth surface morphologies. $SiCl_4$ also etches highly anisotropic whereas Cl_2 and BCl_3 show a greater degree of chemical etching. The addition of SF_6 to a $SiCl_4$ plasma process gives a high selectivity of AlGaAs with respect to GaAs. CCl_2F_2 also shows a selectivity up to 1000 between these semiconductor compounds [8]. This is commonly explained by the formation of an AlF_3 etch stop layer on the aluminium containing surface [6].

CH_4/H_2 has proven to be a good plasma etchant with a high selectivity for etching III-V semiconductors with respect to mask materials. This noncorrosive gas mixture is intensively studied after it was proposed by Niggebrügge in Reactive Ion Etching (RIE) [1]. Since several years Electron Cyclotron Resonance (ECR) discharges have been the subject of intense research because of their possible advantages over RF based plasmas. ECR plasmas provide a high degree of ionisation at low pressures and the discharge is generated remote and independent from the substrate stage. The substrate does not suffer from excessive ion bombardment since it is possible to work with low DC biases. This is essential for devices whose electrical or optical characteristics degrade due to their sensitivity to this bombardment [9,10,11,12]. Also the radiation damage is believed to be reduced because the substrate is not in the direct vicinity of the plasma. This in contrast to RIE where RF power on the substrate is used to ignite and maintain the plasma and providing the DC bias necessary for etching.

There has been much research on the Metal Organic ECR etching of III-V semiconductors. Regardless of differences in system configurations the etch rate increases with the content of CH_4 in hydrogen. It is not possible to increase the methane flow indefinitely. At a certain concentration of methane in hydrogen deposition of polymers is taking place.
The etch rate increases with RF power (DC bias) supplied to the substrate, microwave power and decreasing pressure [11]. In this chapter the etch characteristics of $CH_4/H_2/Ar$ electron cyclotron resonance plasma etching on GaAs and AlGaAs are described. Few experiments have been done on InGaAs and InP.
Paragraph 3.2 of this chapter describes the reactor, the basic concepts of ECR etching and the reaction mechanisms. Paragraph 3.3 describes the etch characteristics (average etch rates) on GaAs as a function of the CH_4 content and the additional RF power on the substrate. Also the influence of different mask materials will be mentioned. Paragraph 3.4 deals with the behaviour of $CH_4/H_2/Ar$ ECR plasma etching on InP.

3.2 MOECR plasma etching

3.2.1 The Reactor

The reactor is part of a cluster tool made by Oxford Plasma Technology. The cluster tool consists of a load lock connected to a transfer chamber which gives the possibility to enter in three different process chambers (stations). The whole system can be managed by a microprocessor as already described in the introduction.
The fourth station is the III-V semiconductor plasma etch chamber. This chamber is shown schematically in figure 3.1. The configuration of this chamber is the same as for the dielectric etch chamber (station 1).
The vacuum is created by a magnetically levitated 1000 ls^{-1} (N_2) turbo molecular pump (Seiko Seiki) which is supported by a rotary dry pump (Edwards DP 80). The base pressure obtained is $6 \cdot 10^{-6}$ Torr. The gases are exhausted via a dry scrubber (Plasma Products) to neutralise possible toxic gas emissions. The microwave power is introduced through a waveguide into the top of the vacuum chamber. Tuning of the reflected power is accomplished by two motor driven tuning stubs on the waveguide. During the experiments the microwave power was varied from 400 to 600 Watt. Two magnets produce the magnetic fields necessary for the cyclotron resonance condition. This condition will be treated later in this paragraph. The substrate table is located downstream of the microwave discharge zone. On the substrate table additional RF power, at a frequency of 13.56 MHz, can be supplied to obtain a certain DC bias level. This RF power is varied from 18 to 96 Watt. These powers lead to a DC bias of -20 and -120 Volt respectively. The table temperature is controlled with a heater/chiller and the table can be moved with respect to the plasma region. It is possible to introduce the gas mixtures at two different places. In the top of the chamber, adjacent to the upper magnet, it is possible to introduce the process gases CH_4, H_2 and Ar. The flow is regulated by mass flow controllers.

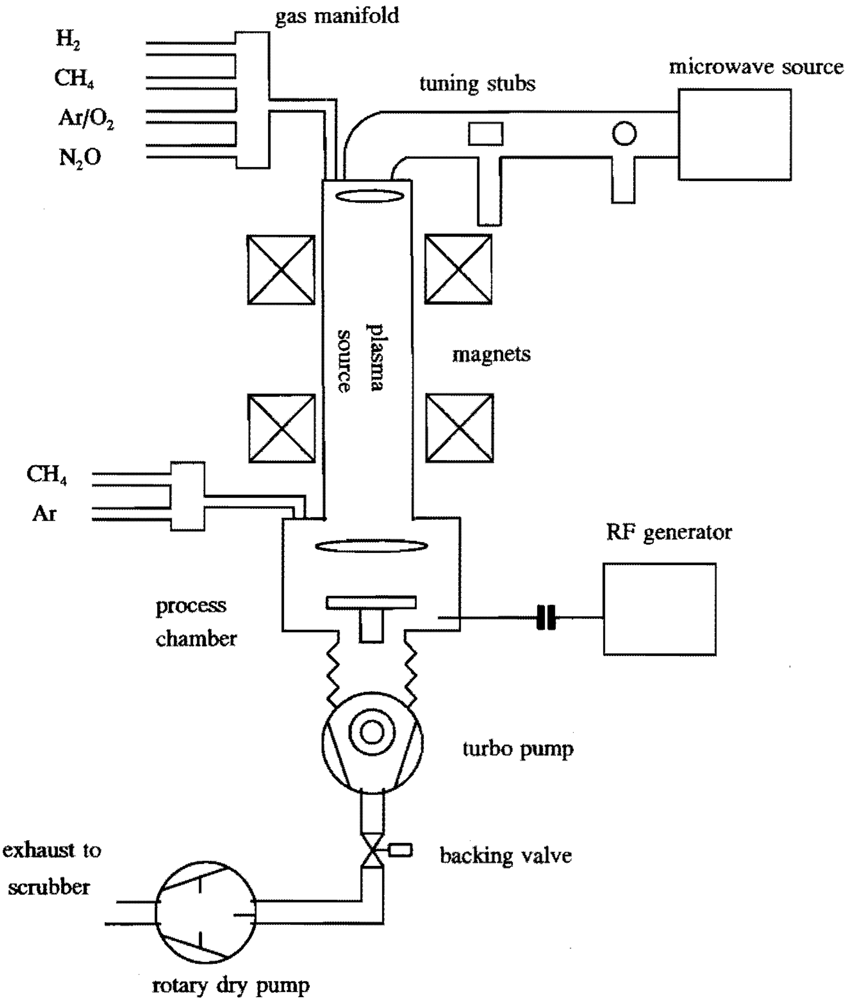
gas manifold
H_2
CH_4
Ar/O_2
N_2O
tuning stubs
microwave source
plasma source
magnets
CH_4
Ar
RF generator
process chamber
turbo pump
backing valve
exhaust to scrubber
rotary dry pump

Figure 3.1, The configuration of the ECR plasma etch chamber.

At this gas inlet ring also N_2O and O_2 can be introduced for chamber cleaning and substrate descumming purposes. The gases, introduced via the top manifold, pass through the ECR discharge zone. CH_4 and Ar can also be injected into the substrate chamber by a second gas distribution ring. These gases are introduced in the vicinity of the substrate. The pressure can be controlled by a VAT valve and an automatic pressure controller. The chamber walls are covered with aluminium oxide to minimise plasma interactions and to reduce contamination released from the walls during processing.

3.2.2 The ECR discharge

A plasma consists of positive ions and negative charged particles embedded in a sea of neutral species. The total number of these charged particles is the same since a discharge has to be electrically neutral. Charged particles are continuously created by dissociation and ionisation. This sustaining of the discharge is mainly initiated by electron impact ionisation. Beside the creation of charged particles always recombination takes place.

In ECR discharges the plasma is initiated when microwave energy is absorbed by the particles in the presence of a magnetic field [13]. This occurs when the electron cyclotron resonance frequency ω_c equals the microwave excitation frequency ω.

$$\omega_c = \frac{e.B}{m_e} = \omega \tag{3.1}$$

where e is the electron charge, m_e the mass of the electron and B the strength of the magnetic field. Since the microwave excitation frequency is 2.45 GHz the magnets have to produce a static magnetic field of 0.0875 Tesla to satisfy resonance within the source. The place where this condition is met is called the ECR zone.

The magnets help to sustain the plasma by giving the electrons an outward spiralling motion in the downstream direction. The residence time of the electrons in the plasma is prolonged and so the chance of electron impact ionisation increases. This additional residence is necessary because outside the ECR zone little microwave energy is coupled to the electrons. The magnets act like magnetic mirrors and the strength of their field determines the shape of the plasma. This is shown is figure 3.2.

Downstream the plasma, in the process chamber, only little RF power is needed to obtain a certain DC bias for processing. This is due to a independent control over the generation of the reactive species and the magnitude of the energy of the ions. This energy is controlled by adjusting the RF power. With Reactive Ion Etching (RIE) in a parallel plate reactor higher RF power levels are needed for both: maintaining the plasma and providing a DC substrate bias.

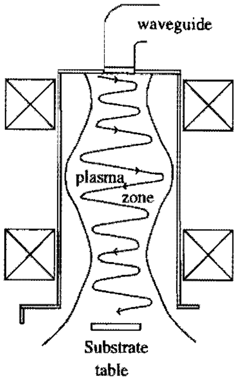

Figure 3.2, The shape of the plasma caused by the magnetic mirrors and the spiralling motion of the electrons.

There are several different reactor configurations possible to obtain a microwave discharge. Asmussen [13] compares and describes those different ECR plasma reactors.

Plasma discharges can be used for deposition and etching. Reactive radicals created in the plasma are normally adsorbed by the surface and a reaction product with the surface is established. After this product has been formed desorption takes place and etching results. It is also possible that different reactive species combine on the surface of the substrate, under certain conditions, which leads to deposition. Substrate temperature is for example such a condition.
The basic chemical reaction on the GaAs surface on which the $CH_4/H_2/Ar$ plasma is based can be written as:

$$3\, CH_4 + GaAs \xrightarrow[H_2]{} Ga(CH_3)_3 + AsH_3$$

The group III lattice constituent is removed in the form of trimethylgallium. The group V element is removed as a group V hydride: arsine. However the identification of the metalorganic group III product has been difficult to prove, its existence has been confirmed by secondary ion mass spectroscopy [14,15]. The group V product was much easier to observe [14]. The influence of argon will be described in paragraph 3.3.

3.2.3 Sample and reactor preparation

Before etching the chamber is prepared for ten minutes with a hydrogen plasma to reduce any residual oxygen present in the vacuum chamber. After cleaning the pressure is in the high 10^{-7} Torr region. The cleaning process uses a hydrogen flow of 50 sccm which leads to a pressure of 2.4 mTorr. The microwave power is 400 Watt and the upper and lower magnet have currents of 140 and 80 Ampère respectively. On the substrate there is a DC bias of -20 Volt induced by 10 Watt RF power. The aluminium substrate holder is loaded into the chamber during this cleaning process.

The average etch rates are determined on undoped GaAs substrates covered with a silicon oxide or resist mask. The sample size was about 1 cm^2 and covered for 80 percent by the mask. Before etching, the GaAs surface is cleaned in a diluted ammonia solution (NH_4OH:H_2O, 1:10) to remove native oxide from the surface. The average etch time was 20 minutes except at processes which gave low etch rates. In those cases the time is prolonged to a total of 40 minutes. The resist used (AZ 1505) is not known as plasma resistant. It is however chosen because it is used in the processing of a transistor gate since small features can be defined accurately with this type of resist. The average etch depth is measured with a Tencor Alpha step 200. The results will be compared to those mentioned in literature.

Since many process parameters are involved (microwave power, magnets, RF power, pressure, table height and gas mixture) it is difficult to optimise the process with respect to all parameters. The influence of the most important parameters will be described. It is also expected that some process parameters can not be controlled during the experiments. For example the temperature of the substrate and the deposition of polymers on the reactor walls could not be controlled accurately. Despite the presence of table cooling it was observed that the temperature of the substrate holder and the sample increased during processes. This was dedicated to a poor thermal contact between the table and the holder. Polymer deposition is also dependent on the temperature [16]. The polymer deposition is facilitated at higher temperatures. All these parameters will be ignored except when it can be shown that they have a strong influence on the results.

3.3 Results

Figure 3.3 shows the influence of increasing methane flow on the average etch rates of GaAs for fixed hydrogen flows. Argon is not used because it is thought to behave as a physical chemical inert component which enhances the etch rate and reduces the amount of polymer formation on the mask and the GaAs surface. The pressure varied from about 1 mTorr at a hydrogen flow of 20 sccm to 2.5 mTorr at 50 sccm. The DC bias is kept constant at -80 Volt, induced by a RF power between 45 and 57 Watt. The microwave power is 600 Watt. The upper and the lower magnet currents are 140 and 80 Ampère respectively. The etch rates increase with increasing methane flow until deposition of polymer on the GaAs appears. This polymer is initiated at a methane flow which is about 30 % of the hydrogen flow. However, polymer formation on the resist mask starts at a much lower methane content. The results are comparable to the experiments mentioned in literature [17,18].

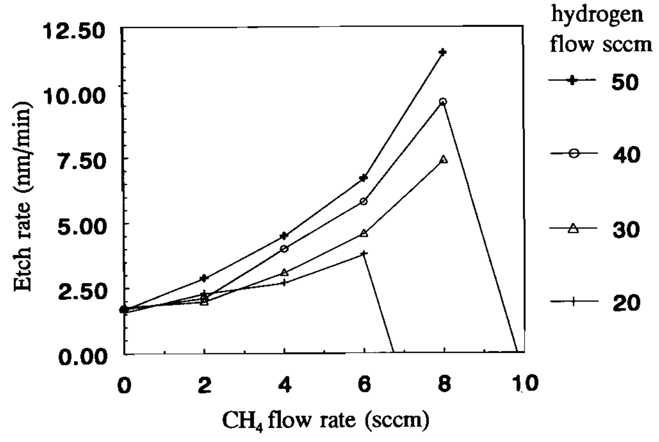

Figure 3.3, The etch rate on GaAs as a function of the methane flow for different hydrogen flows at a DC bias of - 80 Volt.

The experiments are also performed at DC biases of -20 and -40 Volt. For these lower biases the polymer starts to deposit at lower methane/hydrogen ratios. At a bias of -20 Volt the deposition on the GaAs surface is already initiated at a methane/hydrogen ratio of 10 percent. This is probably due to a reduced physical sputtering at these lower bias levels. At a constant methane flow the derivative of the etch rate to the hydrogen flow δ(rate) first increases with increasing hydrogen flow and later decreases. This effect can be the best observed at the methane flows of 4 and 6 sccm. The first increase in the δ(rate) is probably due to a competition between the deposition of polymers and the plasma etching. This competition reduces in favour of etching as the hydrogen flow increases. The addition of more hydrogen does not increase the amount of active methane species which are mainly responsible for the etch process. The etch rate increases only by the sputtering component of hydrogen.

The addition of the chemical inactive argon to this process is to reduce the polymer formation on the substrate and to enhance the etch rate. Figure 3.4 shows the effect of the average etch rate as a function of increasing argon flow. These experiments were done at a DC bias of -40 V and a methane and hydrogen flow of respectively 20 and 4 sccm. A remarkable dip in the etch rate at an argon flow of 10 sccm was observed. The etch rate increased from 1.8 to 10.8 nm/min if 4 sccm argon was supplied but decreased to 6.1 nm/min at a argon flow of 10 sccm. We assume that increasing the argon flow to 4 sccm increases the desorption of reaction products from the surface which leads to an improved etch rate. A further increase of the argon flow causes the etch to become adsorption limited. From 10 to 20 sccm the increase in etch rate is mainly initiated by argon sputtering. Based on the experiments an argon flow of 4 sccm, together with the above mentioned hydrogen and methane flows, was chosen for further experiments.

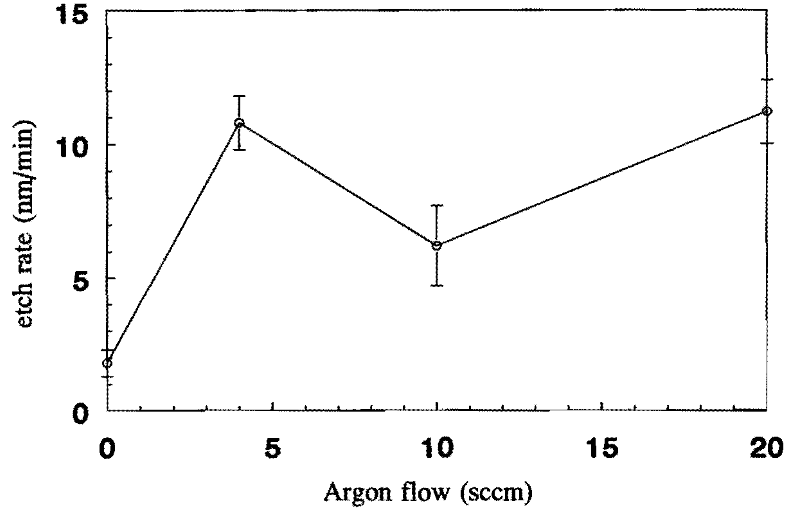

Figure 3.4, The etch rate of GaAs as a function of the argon flow at a DC bias of -40 Volt. The dip in the etch rate is caused by a change from a desorption to an adsorption limited process mechanism.

Variation of the microwave power from 400 Watt to 600 Watt does not show any significant changes on the average etch rate. This probably means that the density of reactive radicals is not significantly increased. However at lower microwave powers the polymer deposition appears at much lower methane/hydrogen ratios. At a bias voltage of -80 Volt and 600 Watt microwave power the polymer deposition is initiated at a methane/hydrogen ratio of 30 percent whereas at 400 Watt microwave power the deposition is initiated at 10 percent of methane with respect to hydrogen. For this reason a microwave power of 600 Watt is chosen which gives the opportunity to etch at lower DC substrate biases.

The etch rate is also dependent on the mask material which is used. The etch rate with a silicon oxide mask is about 30 percent lower than with a resist mask. This effect is also observed by others [15,19] and is more pronounced at lower RF power levels. The enhanced etch rate with a resist mask is due to a release or sputtering of hydrocarbons from the resist which effectively increase the amount of methane. In this way the resist takes part in the reaction mechanism. An advantage of a silicon oxide mask is that it appears to have a much lower degree of polymer deposition during etching [20]. For a resist mask this deposition can however be used as a natural protection. The disadvantage of this protection is that small openings in the resist (typical up to 1.5 μm) will be overgrown by polymers. Lowering the methane flow causes the resist to take a carbonized appearance. If methane was excluded from the process the resist appeared to be normal after etching. This is an indication that the methane reacts with the resist mask.

Increasing the table height increases the etch rate. If the substrate table is raised 10 cm, towards the plasma, the etch rate increases more than 50 percent. At a higher table position the substrate is closer to the reactive species and the ECR source. The amount of reactive species decreases with distance from the ECR source due to recombination. This explains the increase in etch rate.

The etch rate decreases with increasing pressure because the ion energy effectively reduces due to the presence of more collisions. There is also an increase in recombination of the charged particles. For this reason the pressure that is chosen for our standard process is only determined by the flows of the gases and is not controlled by the VAT valve and the automatic pressure controller.

Based on all the experiments a standard process is chosen which is listed below:

Standard process conditions:

top manifold,	H_2	20	sccm.
	CH_4	2	sccm.
	Ar	4	sccm.

lower manifold, no gases.

Top magnet	140	Ampère.
Bottom magnet	80	Ampère.
Microwave power	600	Watt.
RF power	16 to 66	Watt.
DC bias	-20 to -80	Volt.
pressure	1.2	mTorr.
Table height (with respect to reference)	157.0	mm.

Figure 3.6 and 3.7 shows two Scanning Electron Microscope (SEM) photographs of a GaAs etch performed with a silicon dioxide mask. The mask is still present on the GaAs surface. The plasma etch is performed with the standard process at a DC bias of -80 Volt (RF power of 66 Watt). The GaAs surface appears to be very smooth and the walls have an angle of 55 degrees with the horizontal. Figure 3.6 shows a detailed picture of the walls. The roughness (ribbles), visible on these walls, are already present in the silicon oxide mask. This silicon oxide mask is used during long processes because the substrate is strongly heated and the resist mask suffers from erosion. Also polymer deposition on the silicon oxide mask is lower. At lower RF powers the angle becomes a little bit steeper but it was not possible to obtain angles greater than 65 degrees.

Figure 3.7 and table 3.1 show the influence of the RF power (DC bias) on the etch rate of GaAs, AlGaAs and InGaAs. There are two different AlGaAs structures with aluminium content of 25 and 50 percent respectively. The InGaAs has an indium content of 53 percent. The methane flow during processing is increased with the DC bias to maintain a high reactive gas component and to prevent the process becoming to physical.
The rate exhibits a first order dependence on the applied DC bias and the etch rate is linear in time. No etch delay was observed at the beginning of the etch. Variation of etch rate with substrate temperature could not be observed.
Especially for AlGaAs it was necessary to remove the residual oxygen from the surface prior to loading in the system. If the surface is oxygen rich no etch could be performed.

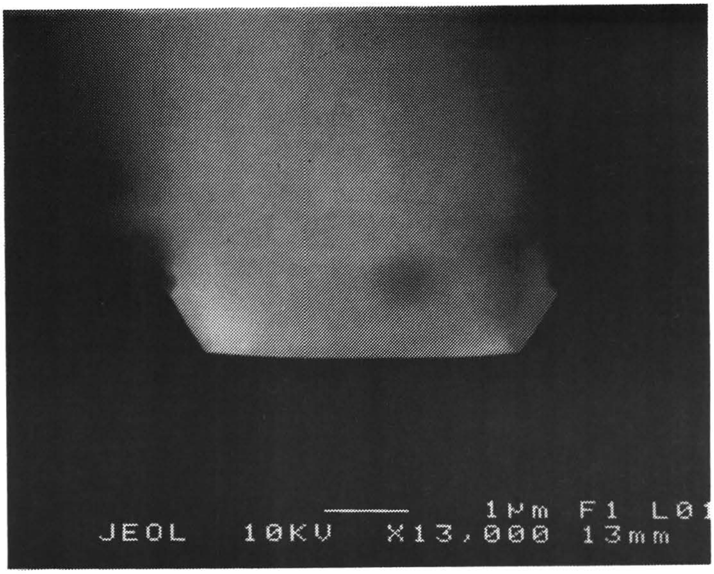
1μm F1 L0
JEOL 10KV X13,000 13mm

Figure 3.5, MOECR ($CH_4/H_2/Ar$) plasma etch of GaAs at a bias voltage of -80 Volt. The walls make an angle of 55 degrees with the bottom of the etch. The silicon oxide mask is still present.

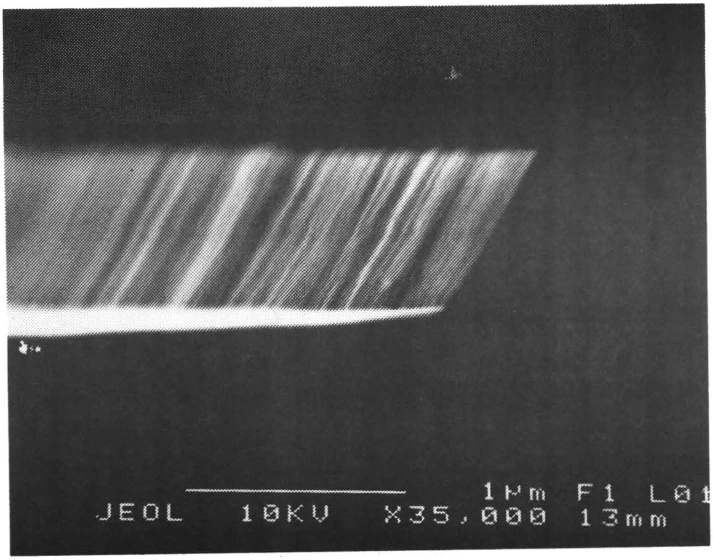
1μm F1 L0
JEOL 10KV X35,000 13mm

Figure 3.6, MOECR plasma etch of GaAs with the standard process at a bias voltage of -80 Volt.

DC bias RF power	- 20 Volt (18 Watt) nm/min	- 40 Volt (38 Watt) nm/min	- 60 Volt (57 Watt) nm/min	- 80 Volt (66 Watt) nm/min	- 120 Volt (96 Watt) nm/min
$Al_{0.5}GaAs$		4.2		14.2	
$Al_{0.25}GaAs$		5.6		15.3	27.7
GaAs	3.1	10.8	14.8	22.3	30.1
$In_{0.53}GaAs$		10.0		30.3	42.6

Table 3.1, The average etch rate in nm/min at DC biases ranging from -20 to -120 Volt for different III-V materials.

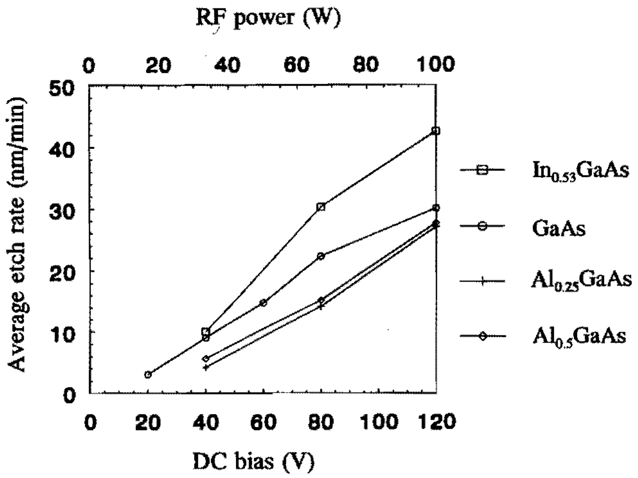

Figure 3.7, The average etch rate as function of DC bias (RF power) for $Al_{0.25}Ga_{0.75}As$, $Al_{0.5}Ga_{0.5}As$, GaAs and $In_{0.53}Ga_{0.47}As$.

As stated by V.J. Law [16] the average etch rates scale with the periodic number of the group III metals (aluminium < gallium < indium). The differences in etch rate is also related to the bond strengths of the metalorganic product formed during etching. These metalorganic compounds have been identified as reaction products during etching [14].

$Al(CH_3)_3$	trimethylaluminium	2.7 eV.
$Ga(CH_3)_3$	trimethylgallium	2.5 eV.
$In(CH_3)_3$	trimethylindium	1.8 eV.

The results concerning the etch rates are comparable to those mentioned in the literature [11,17,21]. At a DC bias voltage of -40 Volt the selectivity between GaAs and $Al_{0.25}Ga_{0.75}As$ is nearly 1:2. This selectivity at a bias voltage of -120 Volt is reduced to 1:1. This is due to enhanced physical process at higher biases. The same relation is visible at an aluminium content of 50 percent.

3.4 InP MOECR plasma etching.

Few experiments have been done on InP. From literature it is known that it is difficult to obtain smooth surfaces with methane hydrogen ECR plasmas [22]. The experiments were done to get an impression of the possibilities of the system. The material used for etching is a highly sulphur doped ($1 \cdot 10^{19}$ cm^{-3}) InP substrate.
The first tests are performed with the standard process in the ECR mode. The etch rate increased from 17.4 nm/min at a DC bias of -40 Volt (38 Watt RF power) to 146.3 nm/min at -120 Volt DC bias (96 Watt RF power). Figure 3.8 and 3.9 show two SEM photographs of the InP surface. It is clear that the surface is very rough due to the formation of indium droplets on the surface. These droplets are formed as a consequence of a preferential removal of phosphor molecules from the surface in the form of phosphine (PH_3). In the literature this roughness is well known as a consequence of etching InP with Metal Organic ECR plasma [11,17,23].

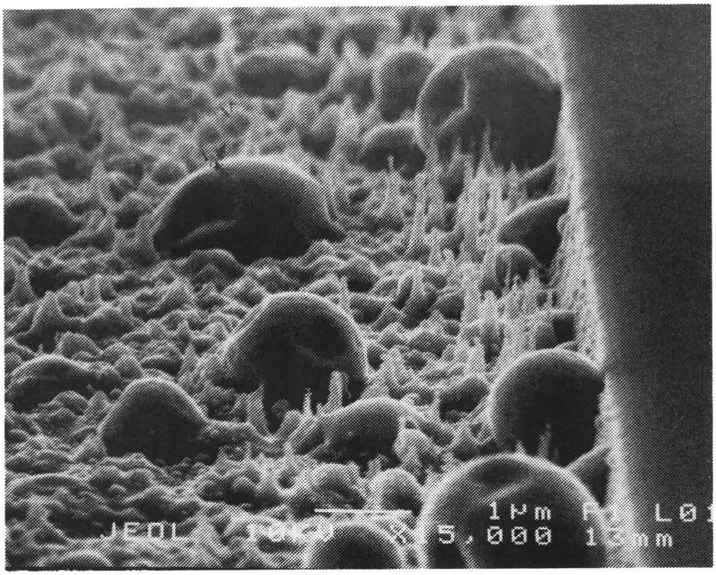

Figure 3.8, The InP surface after a MOECR standard etch process. The indium droplets are caused by a preferential removal of phosphor. The silicon oxide mask is still present.

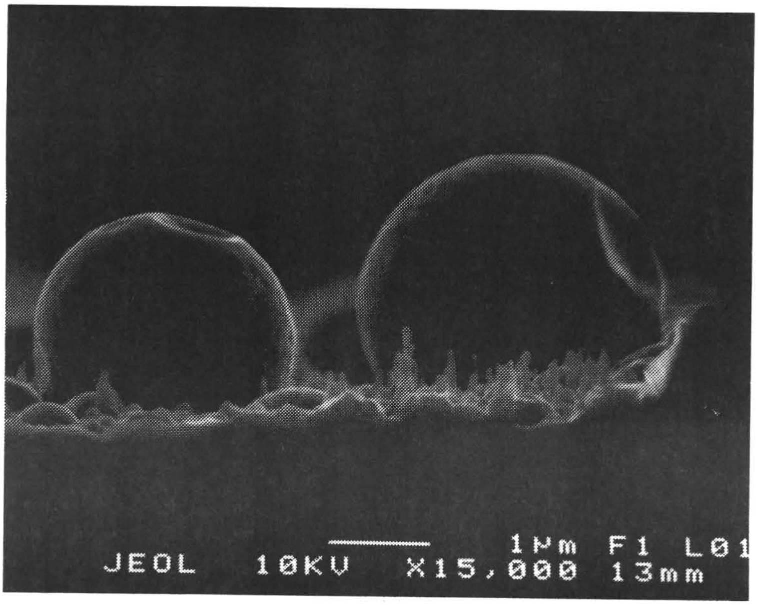

Figure 3.9, InP MOECR plasma etch. The size of the indium droplets compared to the etch depth.

The second test sequence is performed in a metal organic reactive ion etching (MORIE) mode. The magnets and the microwave power are not used during these experiments. With MORIE good results have been obtained on InP.
The pressure is increased to 40 mTorr by adding a hydrogen and methane flow of 70 and 12 sccm respectively. The pressure is maintained by an automatic pressure controller and a VAT valve. A RF power of 100 Watt is supplied to the substrate table to ignite and maintain the plasma. The DC bias induced by this RF power is -340 Volt. The average etch rates of GaAs and InP under these process conditions are 6 and 21 nm/min respectively. The resist remains undamaged in the process.
Figure 3.10 shows a SEM photograph of the InP surface. The peaks visible on the surface are probably due to the high sulphor doping concentration present in the InP. Redeposition on the InP surface of aluminium sputtered from the substrate holder can also be an explanation. This effect is known as micromasking. If the process is performed for a longer time the surface becomes rough due to the formation of indium droplets. This is initiated by an increase in substrate temperature during the etch process. No further optimisation is performed with respect to the different process parameters.

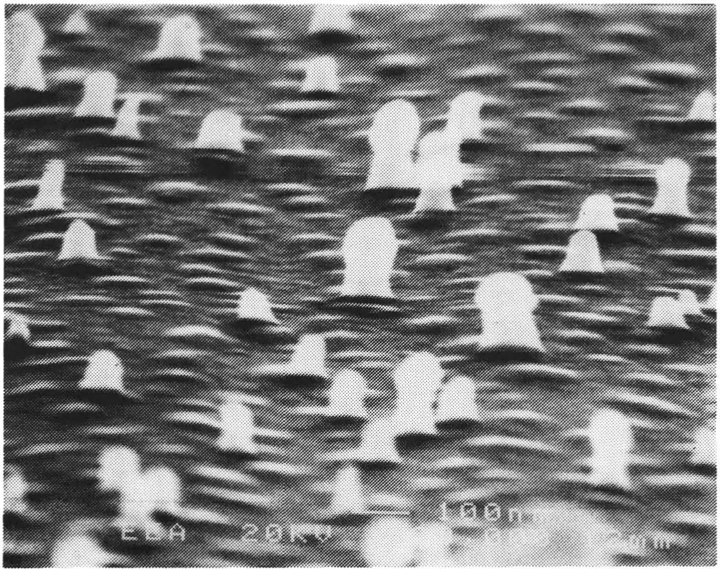

Figure 3.10, InP etch in the CH_4/H_2 RIE mode. The peaks which appear on the surface are probably introduced by the high doping or by micromasking.

The third test sequence is performed in an ECR-RIE mode. In contrast to the standard process only little microwave power is used and the RF power is increased. This according to processes described by Pearton et al. [22,24]. The process conditions are given below.
At a microwave power of 150 Watt and an additional RF power of 22 Watt (-105 V DC bias) the etch rate is 3.7 nm/min for a process of 15 minutes. For longer processes the etch rate increases to 4.6 nm/min. This is probably due to an increase in substrate temperature. If the RF power is increased from 38 Watt (-150 Volt) to 65 Watt (-210 Volt) the etch rate of InP increases from 7.5 to 10.3 nm/min. These etch rates are comparable to those measured by Pearton [22,24]. Figure 3.11 and 3.12 show some SEM photographs of these etches. The etch walls are nearly vertical and the surface is reasonably smooth. Pearton [24] ascribes the improvements of surface morphology to an absence of the imbalance between active hydrogen species and methyl radicals. At higher microwave powers the dissociation of hydrogen increases. So the lower microwave power prevents the InP from a preferential removal of phosphor over indium. Although the surface is reasonable smooth there is an excess of indium on the surface. This is concluded from the fact that at the moment the surface is exposed to the air, indium oxide is formed, which prevents the layer from further plasma etching.

Process conditions for InP:

top manifold,	H_2	20	sccm.
	CH_4	4	sccm.
	Ar	4	sccm.

lower manifold, no gases.

Top magnet	140	Ampère.
Bottom magnet	80	Ampère.
Microwave power	150	Watt.
RF power	22	Watt.
DC bias	-105	Volt.
pressure	1.3	mTorr.
Table height	157.0	mm.

Increasing the methane flow slightly improves the surface morphology. Also the etch rate increases slightly, although the sidewalls remain rough. This could be improved by introducing intermediate oxygen plasmas in the standard process for InP. This alternating process sequences probably removes some polymers from the sidewalls which are partially responsible for the roughness. The sidewall roughness also results from a replication of the mask. The type of mask seems also very important as mentioned in literature [25]. However further investigation is necessary to improve the results on InP.
Increasing the table height did not reveal an increase in the etch rate. This is because the process is forced in the direction of reactive ion etching. This is confirmed by a dark shield which is present above the substrate table.

According to the literature the smoothness of the surface can further be improved by adding Cl_2 [26,27] or PCl_3 [20,24] to the process. PCl_3 provides an overpressure of phosphor during the etch and the indium is removed as $InCl_3$. It is however required that the substrate temperature is increased to 150 °C. The etch rate also increases by adding some chlorine. This is preferred for laser processing where mesa's of a few micron are required. The slope of the sidewalls can be manipulated slightly from negative to positive by increasing the methane flow.
It is possible to etch InP by ECR using Cl_2 or BCl_2 but then substrate temperatures over 200 °C are needed to remove indium as $InCl_3$ [4,28,29]. In spite of the higher temperatures the InP surfaces remain indium rich [28].

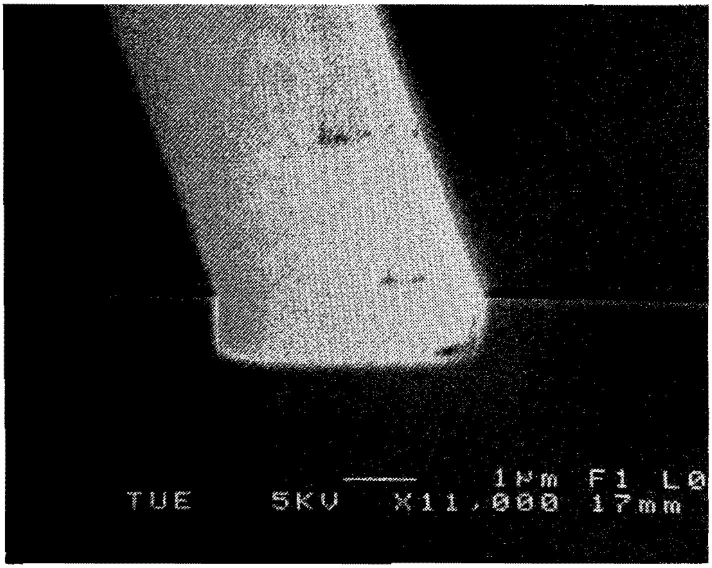
1μm F1 L0
TUE 5KV X11,000 17mm

Figure 3.11, InP $CH_4/H_2/Ar$ MOECR etch at low microwave power. The sidewalls are nearly vertical. The silicon oxide mask is still present on the surface.

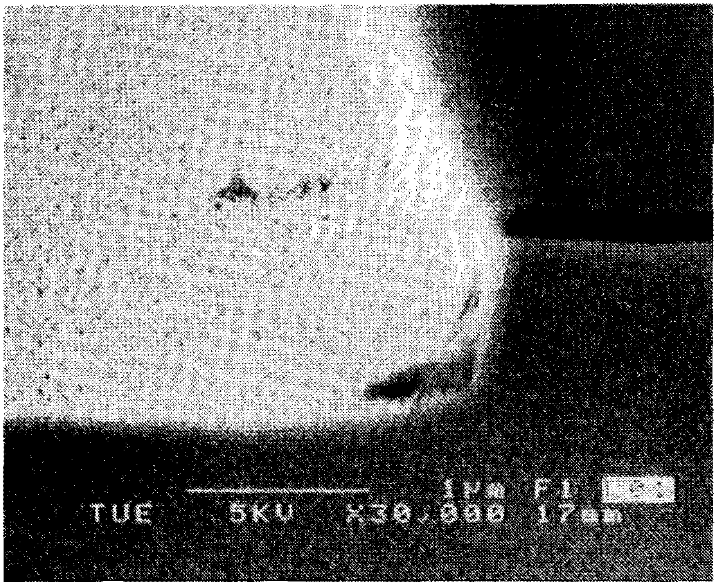
1μm F1
TUE 5KV X30,000 17mm

Figure 3.12, The InP surface after a MOECR plasma etch. The walls are nearly vertical and the surface is reasonable smooth.

3.5 Conclusions

A standard process is found for metal organic ECR plasma etching of GaAs. The influence of different process parameters has been studied intensively, although it can not be concluded that every parameter is fully optimised. The etch rates on the different III-V semiconductors are comparable with those in the literature. Although the etch rate is to low for mesa processing of lasers it can be used for gate recessing of GaAs-based field-effect transistors.

For InP the microwave power needed to be reduced to 150 W to prevent a preferential removal of phosphor from the surface. This process needs however to be optimised to improve the surface morphology and the sidewalls.

The loading effect [19] which certainly occurs during the processes is not taken into account. So the uniformity of the average etch rate over a wafer is not measured.

remark

During time the DC bias varied somewhat at the same process conditions. The reason for this drifting DC bias is probably the polymer contamination introduced on the walls of the chamber. This is also observed by others for CH_4/H_2 based plasma's [30]. The average etch rate as a function of RF power showed less change in time.

3.6 References

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CHAPTER IV

The influence of $CH_4/H_2/Ar$ ECR plasma etching on GaAs.

4.1 Introduction.

Argon ion cleaning with a neutralised beam, as already shown in chapter 2, leads to structural damage to GaAs. This damage could be partially removed by annealing at temperatures between 250 and 300 °C for 24 hours. This was concluded from Schottky diode measurements which showed a degradation of the breakdown voltage and the ideality factor compared to a reference diode. Modification of the GaAs surface due to ECR plasma etching is for this reason also expected. In this chapter the influence of $CH_4/H_2/Ar$ plasma etching on GaAs is studied. The process is meant for producing the gate recess. Its advantage in device fabrication should be the increased uniformity of the recess compared to a wet chemical etch. It is expected that less damage will be introduced by this $CH_4/H_2/Ar$ plasma process than by argon cleaning because it is possible to work at low particle energies. For the MOECR etching a process has been found at a substrate bias of -20 Volt. The etch rate obtained at this bias (about 3 nm/min.) is satisfactory for the gate recess. A minimal ion energy of 50 eV had to be used during the argon ion cleaning. Compared to the energies used in reactive ion etching (generally -300 Volt) also a reduced damage is expected.
Since the $CH_4/H_2/Ar$ etch process is known to be partially chemical due to the methane component in the gas chemistry also a reduction in damage is expected from this point of view. A clear evidence of the chemical nature of the process is given by the influence of increasing argon flow on the etch rates observed on GaAs (See chapter 3 figure 3.4). Whereas a linear increase in the GaAs etch rate is expected for an increasing argon flow, there was a dip in the etch rate at an argon flow of 10 sccm. This was explained by a transition from a desorption to an adsorption limited process mechanism.

Beside the physical damage, a loss of electrical activity of the silicon donor atoms is generally observed. This is explained by the formation of a neutral silicon-hydrogen complex due to the penetration of hydrogen in GaAs. In the next section of this chapter the neutralisation depth or passivation depth is investigated as function of GaAs doping concentration and the substrate bias used during processing. Recovery of the electrical activity of the silicon donors is obtained after annealing. This recovery is shown as function of annealing temperature. The passivation depth and recovery is measured by C-V measurements on Ti/Pt/Au Schottky diodes.

Section 4.3 deals with the degradation of the I-V characteristics of these Schottky diodes and the recovery upon annealing at different temperatures in the rapid thermal annealer. The results are compared to a wet chemical processed reference diode. Finally the influence of the plasma process on the Hall mobility and sheet density of AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures will be investigated. The Hall mobility and sheet density are measured as function of temperature (5-300 K). This is done for different annealing temperatures. The Hall mobility and the sheet density are compared to a reference sample. The influence of an additional Si δ-doped layer with respect to the damage is investigated. Before discussing these experiments the scattering mechanisms limiting the mobility will be mentioned. A mask is designed for fabrication of the Hall Bars. The layout of the mask set and the measurement set up will be discussed.

4.2 Passivation or neutralisation.

4.2.1 Introduction

The first evidence for a loss of electrical activity in silicon doped GaAs, caused by the introduction of hydrogen, was observed by Chevallier et al. [1]. This loss of electrical activity or reduction of carrier concentration is called donor neutralisation or passivation. By capacitance-voltage measurements Chevallier observed that the passivation or hydrogen penetration depth was inversely dependent on the silicon doping level. This suggests that the hydrogen is trapped by the silicon atoms to form a Si-H complex. This bond uses the free electron from the donor to form a neutral complex which leads to a loss of electrical activity of the n-doped GaAs layer. This is confirmed by a correlation of the passivation depth measured with C-V measurements and the depth in deuterated samples as measured with Secondary Ion Mass Spectroscopy (SIMS) [2]. Deuterium is used instead of hydrogen since deuterium can be more accurately detected by SIMS. It is also observed that the passivation depth increases with increasing substrate temperature during processing [3,4]. Recovery of the electrical activity can be done by annealing. Chevallier et al. [1] obtained a recovery of 95 percent of the silicon donors after annealing for 5 minutes at a temperature of 385 °C [1]. Experiments on deuterated samples and SIMS show that, although the electrical activity reappears after annealing, deuterium is still present in the GaAs. It is thought that the Si-H bonds are broken and that deuterium molecules D_2 are formed [5]. At higher annealing temperatures (600 °C) there is a total disappearance of deuterium. In this case the deuterium diffuses out and probably deep inside the GaAs.

Pearton [5] observed neutralisation, due to hydrogen incorporation, in GaAs doped with different donor atoms. Neutralisation was observed in Si, Ge, Sn (donors occupying Ga site) and S, Se and Te (donors occupying As site) doped GaAs whereas shallow acceptors like Be, Mg, Zn and Cd remained almost unaffected after hydrogen exposure. However Johnson [6] showed that passivation also occurred for shallow Zn doped p-type GaAs.

Due to the neutralisation an increase in resistivity, mobility and carrier lifetime is observed in n-doped GaAs [1,7,8,9,10]. The increase in resistivity is caused by a decrease in the free carrier concentration whereas the increase in the electron mobility is due to a reduction of the ionised impurity scattering by the silicon donors. This observation supports the formation of neutral Si-H complexes.

A strong reduction in the free carrier concentration and an increase in the electron mobility is also observed in uniform doped $Al_yGa_{1-y}As$ layers [8]. Beside the neutralisation of the silicon donors also the D-X centre related deep donors are passivated. Whereas the shallow silicon donors recover at annealing temperatures around 400 °C a complete recovery of the D-X centres is established at temperatures above 470 °C [11]. This is measured with Deep Level Transient Spectroscopy (DLTS).

The properties of hydrogen in Si-doped GaAs have been examined by Pavesi et al. [12,13]. He determined the lowest energy sites for the hydrogen by the local density pseudopotential approximation method in n and p-doped GaAs. In the case of a silicon impurity on the gallium site (Si_{Ga} donor) the stable configuration of the Si-H complex is the antibonding Si site. For Si incorporated on the arsenic site (Si_{As} acceptor) the stable configuration of the Si-H complex is along the Si_{As}-Ga bond. In this case the hydrogen forms a three centre bond with the silicon and gallium atoms. In both cases the existence of the Si-H complex have been confirmed by the measurement of the localised vibrational modes with far infrared transmission spectroscopy. An overview of these measurements is given by Pearton [14].

The effect of passivation and the loss of electrical activity is used in the fabrication of lasers and transistors. Plasma hydrogenation is successfully used to obtain current confinement in $Al_yGa_{1-y}As$-GaAs gain guided quantum well heterostructure lasers [15], high power gain guided AlGaAs-GaAs coupled-strip quantum well laser arrays [16] and InP based buried ridge structure lasers [17]. For field-effect transistors the exposure of the active gate region to a hydrogen plasma has been investigated. Due to an increase in the electron mobility an improvement of the performance is expected [18].

Hydrogen can be introduced in semiconductors by a number of methods. Beside the introduction by a hydrogen containing plasma it can be inserted by implantation and with a two electrode electrochemical cell. In the last case an acid solution such as HCl, H_3PO_4 or H_2SO_4 is used. The amount of passivation and surface damage depends strongly on the manner hydrogenation is performed [19]. In our experiments hydrogen is used as diluting gas in the $CH_4/H_2/Ar$ MOECR process to prevent polymer deposition. Since the argon and methane gas flows are relatively low compared to the hydrogen flow passivation is likely to occur. In this section the passivation depth as a function of the doping level and the process substrate bias is determined with Schottky diodes. The recovery of the passivation upon annealing is also studied.

4.2.2 Determination of the passivation depth by C-V measurements.

The passivation depth is measured with C-V measurements on Ti/Pt/Au Schottky diodes. A structure with different Si-doped GaAs bulk layers respectively 1,8 μm $1.5 \cdot 10^{15}$ cm^{-3}, 1 μm $1.5 \cdot 10^{16} cm^{-3}$ and 0.8 μm $3.0 \cdot 10^{17} cm^{-3}$ grown by MBE on a highly doped GaAs substrate have been used for these experiments. On the backside of the substrate Ge/Ni/Au ohmic contacts were evaporated whereas the layers are removed wet chemically to obtain Schottky diodes on the different doping levels. This etch is performed in a $NH_4OH:H_2O_2:H_2O$ (1:1:50) solution at room temperature. This solution has an etch rate of 0.57 μm/min [20]. The experimental set up and the layer structure are shown schematically in figure 4.1. After the samples are exposed to the standard MOECR processes a Ti/Pt/Au Schottky contact is evaporated onto the etched surface. The C-V measurements are performed with a HP 4280A at a frequency of 1 MHz in reverse bias. The carrier density can be extracted from these measurements by [21,22]:

$$N(W_{dep}) = \frac{-C^3}{\epsilon\epsilon_o q O^2} \cdot \left(\frac{dC}{dV}\right)^{-1} \tag{4.1}$$

where C is the measured capacitance, O the area of the diode and W the depletion depth of the diode. The depletion depth can be determined with:

$$W_{dep} = \frac{\epsilon\epsilon_o}{C} \cdot O \cdot 10^{-4} \tag{4.2}$$

with W expressed in μm. The maximum profile depth by these C-V measurements is restricted by the reverse breakdown voltage of the Schottky diode. Due to this restriction it is possible to determine a depletion depth up to about 20 μm for a 10^{15} cm^{-3} doped semiconductor and to 0.02 μm for a highly doped 10^{18} cm^{-3} semiconductor [22]. This depth is however dependent on the quality of the diodes.

The depth resolution is limited by the Debye length L_d. At the depletion edge the change in the doping concentration is characterised by the Debye length due to the diffusion of free carriers at the edge over a few Debye lengths. The Debye length is defined as:

$$L_D = \left(\frac{\epsilon\epsilon_o k_b T}{q^2 N_d}\right)^{\frac{1}{2}} \tag{4.3}$$

This equation clearly shows that the resolution improves with increasing donor concentration.

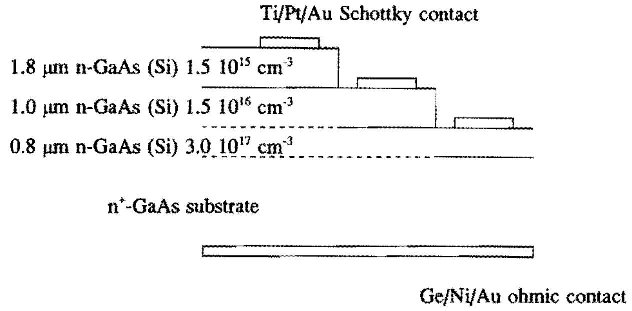
Ti/Pt/Au Schottky contact
1.8 μm n-GaAs (Si) 1.5 10^15 cm^-3
1.0 μm n-GaAs (Si) 1.5 10^16 cm^-3
0.8 μm n-GaAs (Si) 3.0 10^17 cm^-3
n^+-GaAs substrate
Ge/Ni/Au ohmic contact

Figure 4.1, The experimental set up and the layer structure used for the measurements concerning the passivation depth.

4.2.3 The passivation depth.

The passivation depth is determined after 10 minutes processing at a substrate bias of -20 Volt with the MOECR standard process as described in paragraph 3.3. The results for this depth as a function of initial doping density are shown in figure 4.2. The results are compared to a reference sample. The magnitude of the donor concentration close to the surface can not be determined due to the depletion width already present at zero applied voltage. It is clear that the depletion width is reduced with increasing doping concentration. Whereas the passivation depth at a carrier concentration of $1.5 \cdot 10^{15}$ cm^{-3} is over 1.5 μm this depth is reduced to about 0.35 μm at an initial concentration of $3.0 \cdot 10^{17}$ cm^{-3}. At the lowest doping concentration the interface between the different doping levels of the structure is visible at about 1.8 μm. The control sample doped at $3.0 \cdot 10^{17}$ cm^{-3} shows the small range of depth profiling by C-V measurements.

Figure 4.3 shows the passivation depth as function of the applied substrate bias for a $2.0 \cdot 10^{17}$ cm^{-3} Si doped layer. The process time for these experiments was 7 minutes. The passivation depth extends deeper into the GaAs with increasing bias. The depth increases in spite of the increased etch depth at a bias of -80 Volt. A possible explanation could be the substrate temperature that increases at higher substrate voltages which, according to literature, leads to an increased passivation depth.

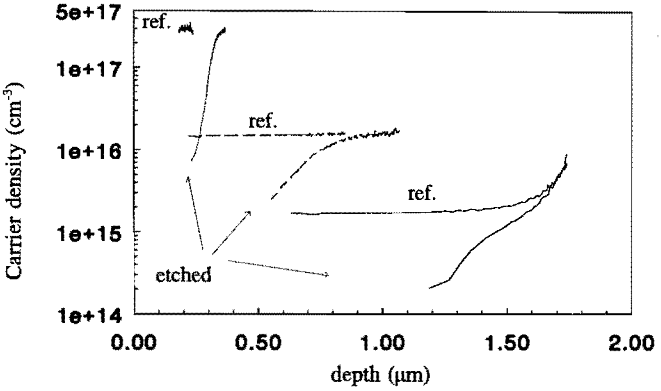

Figure 4.2, The passivation or neutralisation depth determined by C-V measurements at 1 MHz as function of doping concentration ranging from $1.5 \cdot 10^{15}$ to $3.0 \cdot 10^{17}$ cm^{-3}. The initial donor concentration is also shown. The MOECR plasma etch process is performed at a DC substrate bias of -20 Volt for 10 minutes.

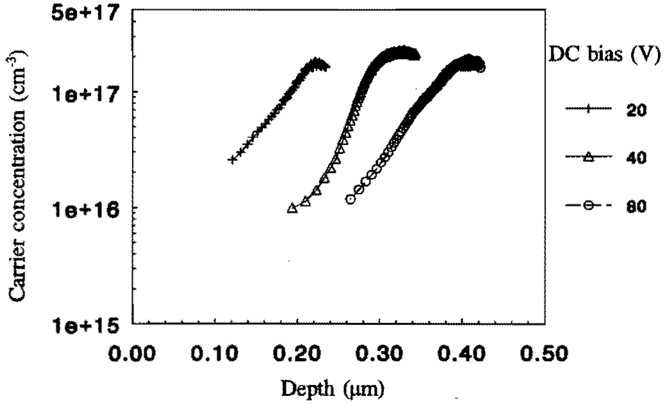

Figure 4.3, The passivation depth for a $2.0 \cdot 10^{17}$ cm^{-3} silicon doped n-type GaAs as function of applied substrate bias (-20, -40 and -80 Volt). The passivation depth increases with increasing MOECR substrate bias.

4.2.4 Recovery of the passivation

The recovery of the carrier density is studied after annealing for 1 minute at different temperatures in the rapid thermal annealer. This is done in a nitrogen ambient. Pearton [1] proposed a mechanism for the Si-H bound dissociation described by:

$$N/N_o = \exp - [\nu t \cdot \exp(-E_D / k_b T)] \qquad (4.4)$$

where N/N_o is the fraction of neutralised silicon remaining, ν is the dissociation attempt frequency and E_D is the activation energy. The annealing temperature T is expressed in Kelvin. The dissociation attempt frequency is generally taken as 10^{14} s^{-1} and the activation energy as 1.2 eV. Figure 4.4 shows the fraction of neutralised silicon remaining as function of the annealing temperature and for different annealing times according to equation 4.4. There is a rapid decrease between 350 and 425 °C.

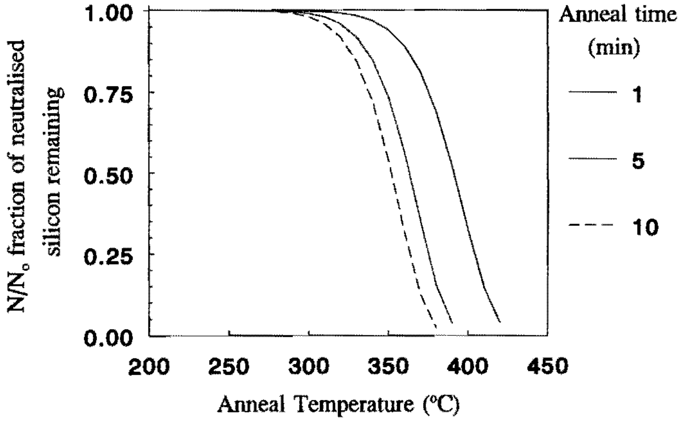

Figure 4.4, The neutralised silicon remaining after a heat treatment at different temperatures for different annealing times. This figure is after Pearton [1].

Figure 4.5 shows the recovery of the carrier concentration after exposing a $3 \cdot 10^{17}$ cm^{-3} silicon doped layer to a $CH_4/H_2/Ar$ plasma for 7 minutes at a DC bias of -20 Volt. Subsequently the structure is annealed at different temperatures for 1 minute. After annealing at 375 °C the carrier density is nearly full recovered and little increase is observed at higher temperatures. Identical behaviour is observed for layers treated at a DC bias of -40 and -80 Volt.

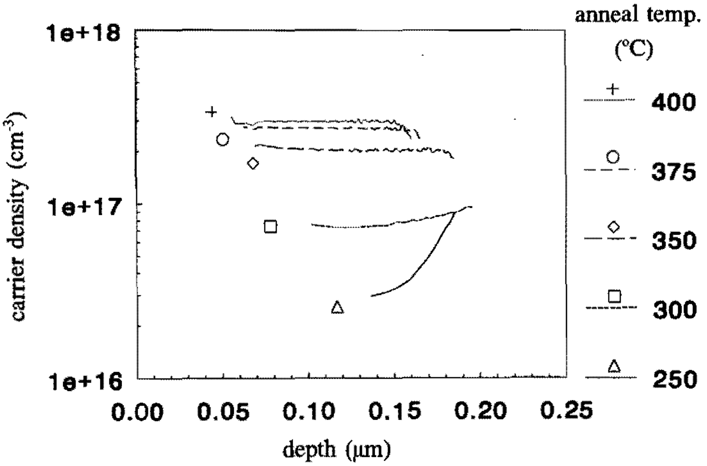

Figure 4.5, The recovery of the carrier concentration after annealing for 1 minute at different temperatures in a nitrogen ambient. The layer was exposed for 7 minutes to a $CH_4/H_2/Ar$ plasma at a DC bias of -20 Volt. The original carrier concentration before processing was $3 \cdot 10^{17}$ cm^{-3}.

4.3 Schottky diodes.

4.3.1 Introduction.

A clean GaAs surface is an important factor for obtaining good diode performance as already mentioned in chapter 2. The Schottky diode characteristics degrade due to interface states between the metal and semiconductor. The pinning of the Fermi level at the interface, as a consequence of these states, is dominant in the formation of the barrier height. This was explained by amphoteric native defects which occurs at gallium or arsenic rich surfaces [23,24]. Processing with a methane-hydrogen plasma by reactive ion etching generally reveals a gallium rich GaAs surface [11,25]. In these studies the surface elemental composition is measured by X-ray Photoelectron Spectroscopy (XPS). By measurements on AlGaAs and AlAs an increased oxygen content on the surface is observed due to a preferential removal of the arsenic and in a lesser extent of gallium atoms compared to aluminium [25]. The arsenic deficiency causes also an increase of gallium dangling bonds [26]. These defects are responsible for pinning of the Fermi level. In contrast to the arsenic deficiency caused by reactive ion etching no arsenic depletion was observed in $CH_4/H_2/Ar$ ECR plasma etching [27]. Even at substrate biases of -50 Volt no preferential arsenic loss could be detected.
In this section the influence of MOECR plasma etching on Ti/Pt/Au Schottky diodes is investigated by C-V and I-V measurements. The behaviour of the diodes is studied with respect to the barrier height, the saturation current and the ideality factor. This is done for different process bias conditions (-20, -40 and -80 Volt) and upon annealing to recover the electrical activity of the donors and to partially restore the structural damage introduced during the process.

4.3.2 The influence of MOECR plasma etching on Schottky diodes.

The Schottky diodes are made on an identical structure as the MESFET mentioned in chapter 1. This layer structure (W456 E7) consists of a 20 nm $2\cdot10^{18}$ cm^{-3} doped n-GaAs toplayer and a 200 nm $3.0\cdot10^{17}$ cm^{-3} doped n-GaAs active layer on a 2 μm undoped GaAs buffer layer. The ideality factor n, the leakage current I_s and the barrier height Φ_b are determined from I-V measurements. Alternatively the barrier height is extracted from the C-V measurements. Here the barrier height can be calculated from the horizontal voltage intercept V_i of the $1/C^2$ vs. V characteristics. The barrier height is defined as [28]:

$$\phi_b = V_i + V_n + \frac{k_b T}{q} \tag{4.5}$$

where V_n is the depth of the Fermi level below the conduction band. After etching 100 nm with the plasma a Ti/Pt/Au Schottky diode is evaporated. Figure 4.6 and 4.7 show the results of the barrier height, the saturation current and the ideality factor as function of the annealing temperature. The values are compared to a wet chemically etched reference diode.

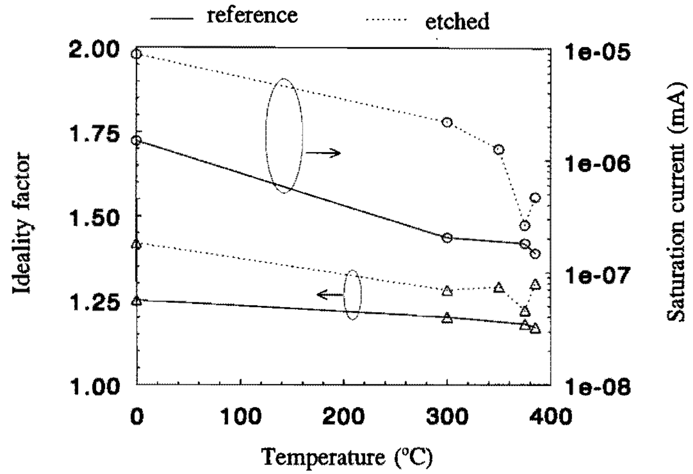

Figure 4.6, The saturation current (○) and the ideality factor (△) as function of annealing temperature for a diode etched at a DC bias of -20 Volt. The characteristics are compared to a wet chemically etched reference diode.

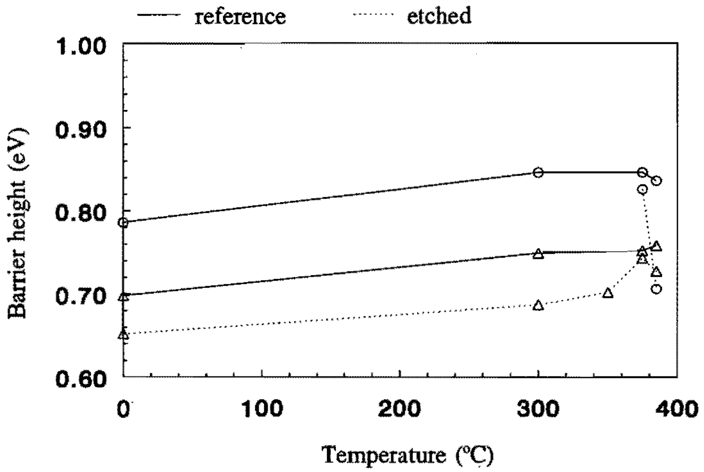

Figure 4.7, The barrier height extracted from I-V (△) and C-V (○) measurements for a diode etched at a DC bias of -20 Volt compared to a reference diode.

The plasma etch is performed at a -20 Volt DC substrate bias. Subsequent annealing is performed in the rapid thermal annealer (RTA) for 1 minute in a nitrogen ambient. 300 °C is lowest temperature used during these experiments because no recovery of the electrical activity of the silicon donors was observed at lower annealing temperatures.
The ideality factor decreases with increasing anneal temperature and equals that of the reference diode after annealing at 375 °C. Generally a degraded performance is obtained for heat treatments at temperatures above 375 °C. This is probably due to an indiffusion of the Schottky metallisation into the GaAs. Identical behaviour is observed for diodes processed at -40 and -80 Volt. Beside the ideality factor, the optimum for the saturation current is also obtained at 375 °C.
By C-V measurements it was difficult to extract the barrier height for diodes annealed at temperatures below the optimum. This is probably due to the amount of neutralised silicon donor atoms at the lower annealing temperatures.
It is clear that the barrier height extracted from the C-V measurements is estimated higher than the barrier height determined from I-V measurements. This is explained by atomair inhomogenities at the depletion interface causing local variations in the barrier height [29]. In C-V measurements (measured in reverse bias) the diode can be treated as parallel plate capacitor from which the extracted barrier height is a mean value. The C-V measured barrier height is defined by the band bending. In I-V measurements the current in forward bias is exponential dependent on the barrier height and in this way more sensitive to fluctuations in this barrier height. The current transport is influenced by the interface states, residual oxide and deep levels. The current flows preferentially through the barrier minima.

	n	Φ_b (V)	I_s (mA)
reference	1.25	0.68	$1.5 \cdot 10^{-6}$
reference (375°C)	1.18	0.74	$1.8 \cdot 10^{-7}$
- 20 V	1.22	0.73	$3.6 \cdot 10^{-7}$
- 40 V	1.24	0.74	$6.4 \cdot 10^{-7}$
- 80 V	1.30	0.68	$2.3 \cdot 10^{-6}$

Table 4.1, The influence of $CH_4/H_2/Ar$ ECR plasma etching on the barrier height Φ_b, the ideality factor n and the saturation current I_s of Schottky diodes. The results are compared to a wet chemical etched reference diode. The etch depth remained constant during the experiments.

Table 4.1 shows the from I-V measurements extracted barrier height ϕ_b, ideality factor n and saturation current I_s as function of the DC bias. This after annealing at 375 °C for 1 minute. The etch depth remained constant during these experiments. The characteristics slightly degrade with increasing substrate bias but are comparable to the unannealed reference diode. This is expected since processing at higher substrate biases introduces more damage.

Compared to the annealed reference diode little degradation is observed. No remarkable degradation in the reverse breakdown voltages was observed at the different energies.
The results are comparable to those obtained in literature [11,30]. Perreira [11] investigated the diode characteristics after CH_4/H_2 reactive ion etching as function of the aluminium content in AlGaAs (0 to 25 percent Al.). Generally he observed an increase in the ideality factor and the barrier height. The effect was more pronounced for higher aluminium content. This was explained by the formation of an acceptorlike surface layer caused by an arsenic surface depletion after RIE processing. In comparison to our results the changes in the ideality factor and the barrier height are not so pronounced. This is probably due to a less preferential removal of arsenic in the ECR processes compared to RIE.

4.4 The influence of MOECR plasma etching on GaAs-based heterostructures.

4.4.1 Introduction.

The influence of plasma etching on the electrical characteristics of heterostructures has been investigated for many different processes. The Hall mobility and the electron density of the 2-dimensional electron gas is very sensitive to damage created within the structure. The effect is more pronounced at low measurements temperatures.
Joseph et al. [31] observed a degradation in the mobility and carrier density after removing the GaAs caplayer of an AlGaAs/GaAs heterostructure in a CCl_2F_2 plasma. A 11 percent degradation of the Hall mobility was observed at a DC process bias of -30 Volt. No degradation in the carrier density was measured. The measurements were performed at 15 Kelvin. The damage increased with increasing substrate bias and at a bias of -80 Volt a strong reduction in the carrier density and a 40 percent degradation of the mobility was observed. This was measured without an post annealing step.
Guggina et al. [32,33,34] performed identical experiment with reactive ion etching in a $SiF_4/SiCl_4$ plasma. They observed a 10 percent reduction in the sheet density and a 32 percent reduction of the mobility at a temperature of 77 Kelvin. This degradation was mainly initiated in the first minute of overetching at a DC bias of -60 Volt. Overetching is possible since this gas mixture is very selective due to the formation of AlF_3 on the AlGaAs surface. They also observed a strong degradation with increasing process bias. The reduction of the mobility at low temperatures was dedicated to an increase in remote and background impurity scattering whereas the reduction in carrier concentration was explained by the introduction of electron traps within the AlGaAs donor layer.
Good results were obtained by Watanabe [35]. No degradation was observed in the mobility and carrier density in an AlGaAs/GaAs heterostructure with an Electron Beam (EB) assisted dry etch process with Cl_2 and SF_6 plasma. The measurements were done at a temperature of 20 Kelvin.

The influence introduced by CH_4/H_2 reactive ion etching on AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures has been investigated by Van Es and Pereira [11,36]. They measured the optical and transport properties of these heterostructures. Upon annealing they obtained full recovery of the 2-DEG electron density and 60% recovery of the Hall mobility in the AlGaAs/GaAs heterostructures. With an additional silicon δ-doped layer 75% recovery of the Hall mobility was obtained. From their experiments it was suggested that an additional Si δ-doped layer could prevent the mobility degradation. The Hall mobility in a pseudomorphic AlGaAs/InGaAs/GaAs structure with an additional silicon δ-doped layer fully recovered. Agarwala et al. [37] also demonstrated that an additional δ-doped layer in an AlGaAs/GaAs heterostructure reduced the damage with respect to the transport properties after plasma processing. They used a selective RIE process with $SiCl_4$ and SiF_4. They observed that δ-doped heterostructures showed a smaller change in the sheet density at 300 K and the mobility at 77 K compared to conventional doped heterostructures. The effect was more pronounced with increasing bias voltages and overetch time.
In this paragraph the influence of a silicon δ-doped layer in AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures is studied. Hall measurements are performed on the same structure (W24) as used by van Es and Pereira. This gives the opportunity to compare

the damage obtained by metal organic reactive ion etching and electron cyclotron plasma etching. The reactive ion etching was performed at IMEC Leuven (Belgium) in a parallel plate Plasmalab µP system from Plasma Technology. A standard process of 15 percent methane in hydrogen at a total flow of 75 sccm was used. An additional DC bias of -310 Volt initiated by a RF power of 0.33 W/cm^2 at a pressure of 37 mTorr gave an average etch rate of about 10 nm/min. This etch rate is comparable to our process at a DC bias of -40 Volt. Because ECR works at much lower substrate biases less damage is expected from the ECR system.

For these experiments a mask set was designed for the Hall patterns. The theory and the mask layout will be discussed briefly. Before describing the results, the scattering mechanisms limiting the mobility in a heterostructure will be mentioned.

4.4.2 The Hall effect.

Figure 4.8 shows the design of the Hall bar used for the Hall measurements. On top, the mesa and the ohmic contacts are shown. The width of the bar is 130 µm and the distance between the ohmic contacts is 250 µm. The ohmic contacts have a size of 200 * 300 µm^2. Below the gate pattern is displayed. The width of the gate is 150 µm to overlap the Hall bar. The gate pattern can be used to prevent parallel conduction in the AlGaAs donor layer. This gate pattern is not used during the experiments. Additional two 5 * 5 mm^2 squares for Van der Pauw measurements are made on the mask. These patterns are not shown.

During Hall measurements a current flows between the outer ohmic contacts through the Hall bar. Due to a magnetic field, perpendicular to the Hall bar, a Hall voltage is developed across the bar. According to this a Hall coefficient R_H can be defined as:

$$R_H = \frac{E_y}{J_x \cdot B} \tag{4.6}$$

where B is the magnetic field and J_x the current density. During the measurements a magnetic field of 0.5 Tesla and a current of 10 µA is used. The electric field is determined by measuring the voltage across the Hall bar between an upper and lower contact.

With the conductivity σ the Hall mobility is defined as:

$$\mu_H = R_H \cdot \sigma \tag{4.7}$$

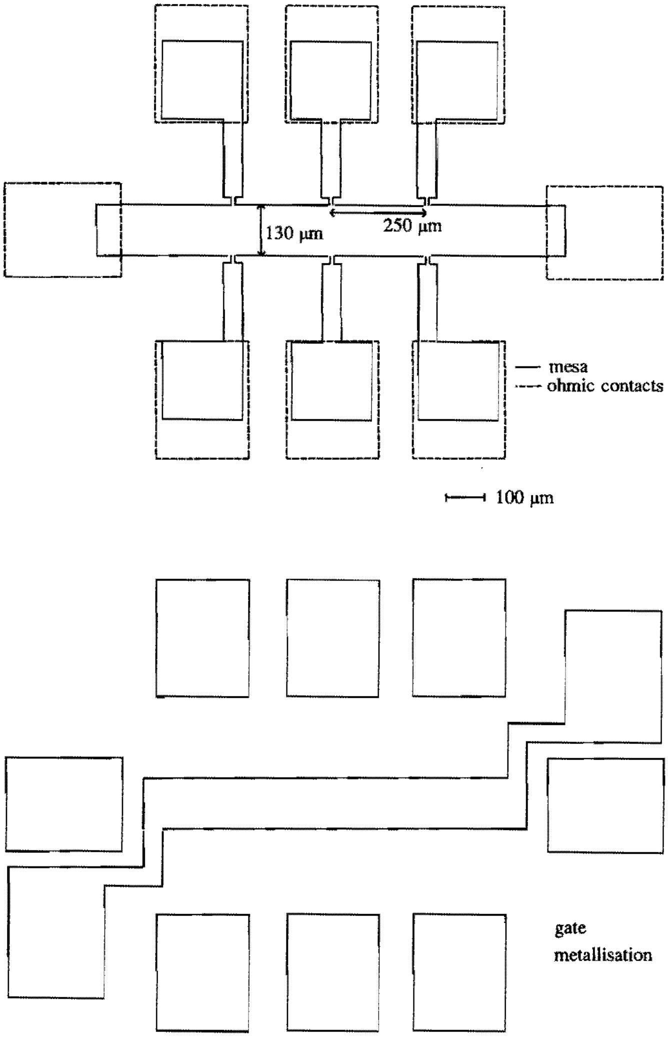
130 µm
250 µm
— mesa
---- ohmic contacts
100 µm
gate
metallisation

Figure 4.8, The Hall bar used for the determination of the sheet density and the Hall mobility of the electrons in the AlGaAs/GaAs heterostructure. On top the mesa and the pattern for the ohmic contacts is shown. The width of the bar is 130 µm and the distance between the contacts is 250 µm. Below the gate pattern is shown.

and the electron sheet density can be calculated with:

$$n_s = -\frac{r_h}{q \cdot R_H} \tag{4.8}$$

where r_h is the Hall factor which depends on the temperature, the doping level and the magnetic field. Generally the Hall factor is close to 1.

4.4.3 2-DEG Hall mobility

As mentioned in chapter 1 the electrons in an AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructure are confined within a potential well located at the interface of the lower bandgap material. The motion of the electrons is restricted parallel to the interface. The electron mobility in this 2-DEG is limited by different scattering mechanisms. At higher temperatures the restriction in the mobility is mainly caused by polar optical phonon scattering. In the lower temperature regime the mobility is limited by remote and background impurities, interface roughness and deformation potential scattering [38,39]. Although the influence of the background impurities and the interface roughness is minimised with the improved epitaxial techniques. Compared to the electron transport in doped GaAs [40] the influence of the ionised impurity scattering is reduced. This is improved by an additional AlGaAs spacer layer. The different scattering mechanisms limiting the mobility for an AlGaAs/GaAs heterostructure are shown in figure 4.9. This figure is after Walukiewicz [39] and shows the mechanisms below a temperature of 300 K. The calculated curves are for a sheet density of $3 \cdot 10^{11}$ cm^{-2} and a remote ionised impurity concentration of $8.6 \cdot 10^{16}$ cm^{-3}. It is clear that above 100 K the optical phonon scattering is the major mechanism in restricting the electron mobility. Below 100 K the deformation potential and the remote impurities play an important role. More about the origin and influence of the different scattering mechanisms can be found in literature [41,42].
For pseudomorphic structures an additional scattering mechanism is the alloy scattering initiated by a random distribution of gallium and indium atoms [43] or cluster scattering due to compositional disorder [44]. At higher sheet densities also intervalley scattering is more probable to occur.

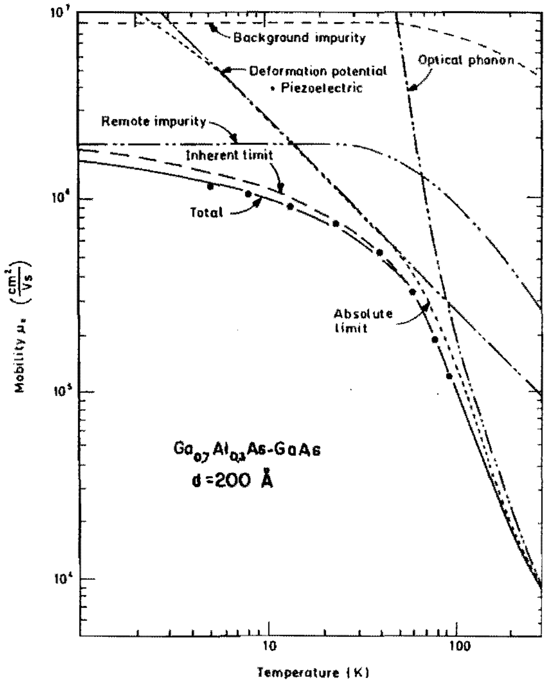

Figure 4.9 The temperature dependent mobility limiting scattering mechanisms in an AlGaAs/GaAs heterostructure [39]. The experimental data are obtained from Hiyamizu [45]. The influence of the optical phonon scattering at higher temperatures and the remote impurities at the lower temperatures is shown.

4.4.4. Experimental results.

4.4.4.1 Influence on AlGaAs/GaAs heterostructures.

Two different MBE grown AlGaAs/GaAs structures have been used for these experiments. The first structure (W24) consists of a 4 μm undoped GaAs buffer layer, a 20 nm $Al_{0.33}Ga_{0.67}As$ undoped spacer, a 38 nm $Al_{0.33}Ga_{0.67}As$ $1 \cdot 10^{18}$ cm^{-3} (Si) donor layer and a 17 nm undoped GaAs toplayer grown on a semi-insulating GaAs substrate. In the second structure a $5 \cdot 10^{12}$ cm^{-2} Si δ-doped layer was incorporated on top of the AlGaAs spacer (W482). These structures are the same as used in the reactive ion etching experiments of Pereira [11].
The GaAs toplayer of both structures is removed by an ECR plasma under standard ECR plasma conditions at different biases. This was done after defining the mesa of the Hall bars by optical lithography and wet etching, and Ge/Ni/Au ohmic contact evaporation and annealing. The applied process bias was increased from -20 to -40 and -80 Volt.
Hall measurements are performed as function of temperature (5-300 K) to obtain the Hall mobility and the 2-DEG sheet density. This is done for annealing temperatures between 325 and 450 °C. Below 325 °C no measurements could be made. From the reference structure the GaAs toplayer was removed wet chemically in a $NH_4OH:H_2O_2:H_2O$ solution at room temperature.
Figure 4.10 and 4.11 show respectively the sheet density and the Hall mobility as function of the temperature after removing the GaAs toplayer in a MOECR plasma at a DC bias of -40 Volt. The curves are displayed for different annealing temperatures. Whereas the sheet density recovers after annealing at 400 °C the Hall mobility does not recover completely compared to the reference Hall bar. This is comparable to the observations done by van Es and Pereira [11,36].

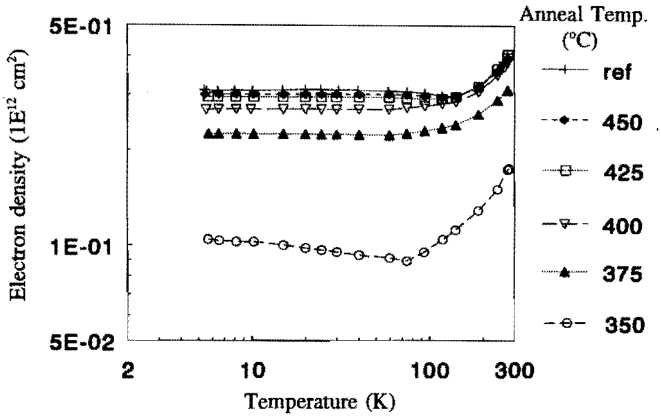

Figure 4.10, The recovery of the sheet density after annealing at temperatures between 350 and 450 °C for 1 minute. This after removing the GaAs toplayer of an AlGaAs/GaAs heterostructure at a DC bias of -40 Volt.

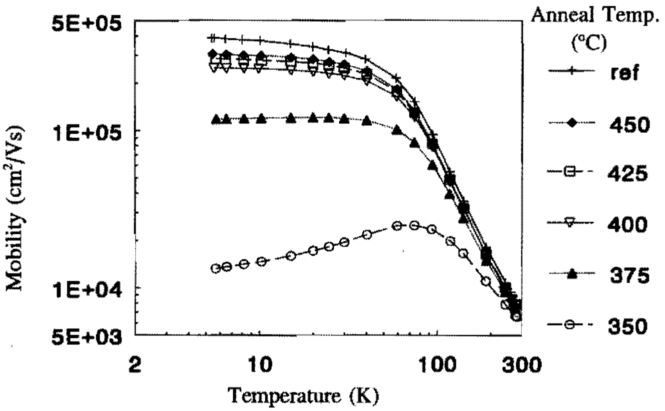

Figure 4.11, The Hall mobility of an AlGaAs/GaAs heterostructure as function of the annealing temperature after removing the GaAs toplayer at -40 Volt DC bias in a MOECR plasma. Compared to the reference Hall bar, the mobility does not completely recover.

Figure 4.12 and 4.13 show identical results of the Hall measurements for the structure with an additional silicon δ-doped layer. Here the Hall mobility and the sheet density recover almost completely after annealing at 400 °C. Table 4.2 lists the Hall mobility and the sheet density of both structures after annealing. The measurements are shown for a temperature of 5.6 K and the results obtained at different substrate biases are compared to a wet chemically etched reference sample.

		- 20 V.	-40 V.	-80 V.	reference
W24	n_s (10^{11} cm^{-2})	-	3.00	2.70	3.10
	μ (10^5 cm^2/Vs)	-	3.07	2.05	3.88
W482 δ-dope	n_s (10^{11} cm^{-2})	3.56	3.78	3.62	3.51
	μ (10^5 cm^2/Vs)	2.85	5.81	5.13	6.16

Table 4.2, The measured Hall mobility and sheet density as function of different applied substrate biases after annealing at 425 °C for 1 minute, compared to a reference sample. The Hall measurements are performed at a temperature of 5.6 K.

The measurements clearly show the influence of the silicon δ-doped layer. The bad results obtained at a DC bias of -20 Volt on both structures could not be explained. The structure without a δ-doped layer could not be measured after annealing. The best results are obtained at a DC bias of -40 Volt. This is in contrast to the results observed on the Schottky diodes where a minimal damage was observed at a DC bias of -20 Volt. Whereas the sheet density in both structures recover the Hall mobility recovered for 74 percent at a DC bias of -40 Volt in the structure without an additional δ-doped layer. With the additional layer the Hall mobility recovered for 94 percent. These results, obtained with ECR, are better than those obtained by methane hydrogen reactive ion etching by Pereira where a recovery of 60 and 75 percent was observed respectively.

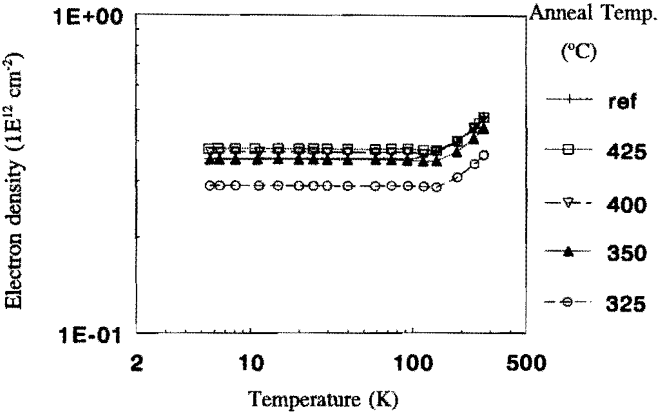

Figure 4.12, The recovery of the sheet density after annealing at temperatures between 325 and 425 °C for 1 minute. This after removing the GaAs toplayer of an AlGaAs/GaAs heterostructure with an additional δ-doped layer at a DC bias of -40 Volt.

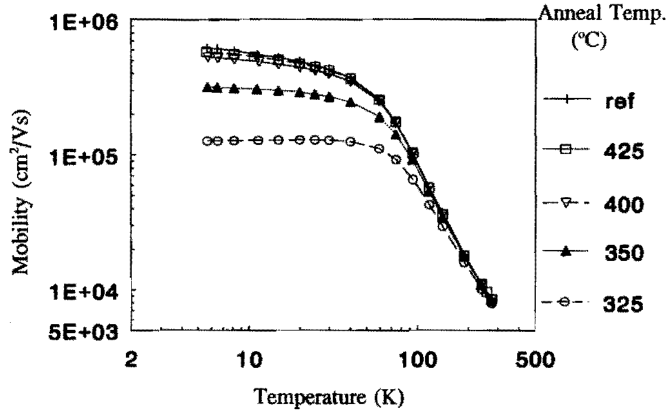

Figure 4.13, The Hall mobility of a AlGaAs/GaAs heterostructure as function of annealing temperature after removing the GaAs toplayer at -40 Volt DC bias. The mobility recovers upon annealing at 400 °C due to the presence of an additional δ-doped layer in the AlGaAs/GaAs heterostructure.

4.4.4.2 Influence on AlGaAs/InGaAs/GaAs heterostructures

Identical experiments have been done on AlGaAs/InGaAs/GaAs pseudomorphic heterostructures. Two structures have been grown by MBE. The first structure (W484) consists of an undoped GaAs buffer layer, a 13 nm undoped $In_{0.15}Ga_{0.85}As$ channel, a 5 nm undoped $Al_{0.25}Ga_{0.75}As$ spacer, a 30 nm $1\cdot10^{18}$ cm^{-3} silicon doped $Al_{0.25}Ga_{0.75}As$ donor layer and a 40 nm highly doped ($2.0\cdot10^{18}$ cm^{-3}) GaAs toplayer. In the second structure (W483) a $5\cdot10^{12}$ cm^{-2} silicon δ-doped layer was additionally incorporated on top of the AlGaAs spacer. The experiments are performed in an identical way as the AlGaAs/GaAs heterostructures. The toplayer was removed in the plasma at different DC biases (-20, -40 and -80 Volt) and the Hall measurements are compared to a wet chemically etched reference structure. The reference structure without a δ-doped layer showed a Hall mobility of $3.07\cdot10^4$ cm^2/Vs and a sheet density of $1.09\cdot10^{12}$ cm^{-2} at a temperature of 6.4 Kelvin. However, after removing the GaAs toplayer by the plasma no Hall measurements could be performed as function of the measurement and annealing temperature, even after annealing at 425 °C for 4 minutes. This was independent of the plasma energies used. A second test sequence and samples processed at IMEC Leuven with CH_4/H_2 reactive ion etching showed identical behaviour.
With the additional δ-doped layer the structures could be measured. Table 4.3 shows the measured Hall mobility and sheet density as function of DC bias and after annealing at 425 °C for 1 minute. The data is shown for a temperature of 5.6 Kelvin.

		- 20 V	- 40 V	- 80 V	reference
W483	n_s (10^{12} cm^{-2})	1.72	1.60	1.62	1.90
	μ (10^4 cm^2/Vs)	2.49	2.52	2.79	3.16

Table 4.3, The recovery of the Hall mobility and the sheet density of the pseudomorphic heterostructure with a δ-doped layer after annealing for 1 minute at 425 °C compared to a wet chemical etched reference Hall bar.

In contrast to the experiments done with the AlGaAs/GaAs heterostructures the carrier concentration is decreased at all substrate biases. The best recovery is obtained at a DC bias of -80 Volt where the Hall mobility is recovered for 88 percent and the carrier density for 85 percent. No experiments have been done at higher DC biases. Compared to reactive ion etching similar results are obtained. For samples processed at IMEC with RIE a 91 percent recovery of the Hall mobility and sheet density was measured.
The experiments on the structure without a silicon δ-doped layer suggests that an enormous damage is created within the structure as a consequence of methane hydrogen RIE and ECR based processes. Identical observations have been made during the fabrication of pseudomorphic HFETs as will be discussed in chapter 6.

4.5 Discussion and conclusions

The experiments reveal that the passivation depth increases with decreasing donor concentration in silicon doped GaAs. The passivation depth also increases with the applied DC bias for a constant process time. Recovery of the electrical activity of the passivated donor atoms is obtained after annealing for 1 minute at 375 °C. Annealing is performed in the rapid thermal annealer in a nitrogen ambient. Above this temperature only a slight improvement is observed.

Annealing of Schottky diodes and different heterostructures show that the characteristics recover at temperatures between 375 °C and 425 °C. Upon annealing the diodes recover and the characteristics are comparable to a reference diode. For temperatures higher than 380 °C an interdiffusion of the Schottky metallisation and the GaAs occurs which degrade the performances of the diodes. A slight degradation is observed with increasing substrate bias with respect to the barrier height, ideality factor and the leakage current compared to wet chemically processed diodes.

The electron density of a 2-dimensional electron gas in an AlGaAs/GaAs heterostructure recovered after annealing at 400 °C, whereas the Hall mobility recovered for 74 percent as measured at a temperature of 5.6 Kelvin. If a silicon δ-doped layer is introduced in the heterostructure the Hall mobility recovered for 94 percent after annealing. This is compared to a structure which toplayer was removed wet chemically. The best results are obtained at a DC bias of -40 Volt. Improvement is observed with respect to CH_4/H_2 reactive ion etching performed on the same structures at IMEC Leuven. They obtained a recovery of 60 and 75 percent for the Hall mobility on the structures without and with a δ-doped layer, respectively. However compared to chlorine based processes, as discussed in paragraph 4.3.1 additional process steps are necessary to obtain these results. For the pseudomorphic AlGaAs/InGaAs/GaAs heterostructure the best results are obtained at a DC bias of -80 Volt. This concerning the structure with an additional silicon δ-doped layer. Further improvement is expected at higher DC biases. For the structure without a δ-doped layer no recovery could be obtained. This suggests that an enhanced electron trapping mechanism or an interface degradation is introduced by the $CH_4/H_2/Ar$ ECR plasma. This probably also explains the experiments on the AlGaAs/GaAs heterostructure processed at a DC bias of -20 Volt. However further investigation is necessary to determine the origin of the damage.

For the conventional and pseudomorphic heterostructures a minimal damage is observed at different process conditions. This suggests that the process needs to be optimised with respect to the structure used. It is believed that this optimum is created by two mechanisms. On one hand the plasma exposure time needs to be minimised, which can be achieved by increasing the substrate bias. The etch time for removing the GaAs toplayer at a DC bias of - 20 Volt is at least 3 times as long as in the case of - 40 Volt. On the other hand it is necessary to minimise the DC bias to reduce the amount of physical or structural damage introduced in the surface and within the layers.

It seems that an additional silicon δ-doped layer behaves as a shield or buffer for further introduction of hydrogen or damage in the AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures. This is in agreement with the suggestion given by Van Es [36]. For this reason it is preferable to introduce a silicon δ-doped layer in heterostructure for field-effect transistors.

4.6 References

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CHAPTER V

Microwave downstream plasma enhanced chemical vapour deposition of silicon oxide and silicon nitride.

5.1 Introduction.

Dielectric layers like silicon oxide (SiO_2) and silicon nitride (Si_3N_4) are used in the semiconductor technology as passivation, protection or as mask during different process steps. Chemical vapour deposition (CVD) is well known as a technique providing high quality dielectric layers. The deposition is based on reactions on a heated substrate with a gas mixture. Generally elevated substrate temperatures (> 450 °C) are necessary to obtain good film properties and reasonable deposition rates [1]. However, processing at these temperatures can be detrimental for compound semiconductor devices. For this reason plasma's are used since it allows reaction kinetics at much lower substrate temperatures. Plasma based chemistry for dielectric deposition is known as Plasma Enhanced Chemical Vapour Deposition (PECVD). Even in PECVD it is still preferable to deposit above room temperature in order to reduce the incorporation of contaminations and to improve the density and the structure of the deposited layers. For plasma assisted deposition processes different types of reactors are used. Among these are the capacitively coupled parallel plate reactors and ECR based reactors. Processes in RF powered parallel plate reactors is also referred to as Direct Plasma Enhanced Chemical Vapour Deposition (DPECVD). In this chapter the quality of silicon oxide and silicon nitride films are investigated. The films are deposited in a microwave downstream PECVD system. This process is also known as Remote or indirect PECVD. One of the first experiments on RPECVD was done by Meiners for silicon oxide deposition [2]. In these systems the plasma is created remote and independent from a heated substrate table.

The quality of a dielectric film can be measured with many different techniques like Auger Electron Spectroscopy (AES), X-ray Photoelectron Spectroscopy (XPS), Rutherford Backscattering Spectrometry (RBS), Infrared Spectroscopy (IRS) and Elastic Recoil Detection Analysis (ERDA) [3,4,5,6,7]. AES, XPS and RBS are used for determination of the elemental composition and the incorporation of impurities. With infrared spectroscopy the absorption bands for the Si-N and Si-O bonds are used for the compositional analysis whereas the absorption bands for bounded hydrogen are used for determination of the amount of hydrogen incorporation. ERD is also used to determine the hydrogen incorporation [8,9]. For plasma deposited layers the amount of hydrogen can be as high as 30 percent.
Beside the composition the mechanical properties like stress and density are important since the layers need to act as barriers to the contamination from outside. Layers with an excess

of stress tend to crack, especially during process treatments. In this chapter the compositional quality of RPECVD silicon oxide and silicon nitride is investigated as a function of changes in the process parameters. In this work a dielectric layer is necessary as mask during the gate recessing of a field-effect transistor since thin resist layers are not resistant to the $CH_4/H_2/Ar$ ECR plasma and subsequent lift off processes. Fabrication of Schottky diodes, as discussed in the previous chapter, revealed less problems since thicker resists could be used.
The compositional analysis is done by RBS and ERD. The refractive index, the etch rate in diluted HF for silicon oxide and buffered HF for silicon nitride and the deposition rates are also studied as a function of the process parameters. The refractive index obtained from ellipsometric measurements can be related to the variation of stoichiometry of the films. The etch rate together with the deposition rate qualitatively gives some information on the film density. The measured data will be compared to literature on direct and remote deposited PECVD films. After describing the reactor layout, the deposition mechanisms and the experimental set up the results obtained on silicon oxide and nitride films will be discussed.

5.2 Silicon oxide and silicon nitride deposition

5.2.1 Deposition Mechanism

In plasma enhanced chemical vapour deposition of silicon oxide and nitride generally silane (SiH_4) is used as a supplier of the silicon. For silicon oxide nitrous oxide (N_2O) or oxygen (O_2) is used as a precursor gas to provide the oxygen. For silicon nitride deposition the nitrous oxide or oxygen is replaced by ammonia (NH_3) or nitrogen (N_2). As a diluent gas in these processes generally nitrogen, helium or argon is used.
The reactive species are created in the plasma by ionisation and dissociation. The radicals participate directly in the deposition. However gas phase reactions create precursor molecules which indirectly participate in the deposition. Hydrogen is eliminated by cross linking. The amount of hydrogen incorporation depends on the extent of ion bombardment and the deposition temperature. For this reason a higher hydrogen concentration is expected at lower deposition temperatures.
Figure 5.1 shows the reaction pathways for silicon oxide deposition after Smith et al. [10]. The gases used are nitrous oxide and silane. In RF based plasma's it is observed that the main plasma constituents for nitrous oxide are N_2 and O_2 molecules and $^{\cdot}O$ and $^{\cdot}NO$ radicals as measured with Fourier Transform InfraRed (FTIR) absorption measurements [11]. Since generally low amounts of nitrogen incorporation are observed in plasma deposited silicon oxide layers it is believed that the oxygen atoms are the main precursors for SiO_2 deposition. $^{\cdot}NO$ is assumed to be relatively unreactive. Together with the silane radicals ($^{\cdot}SiH_n$, $n = 1,2,3$) silicon oxide is deposited and hydrogen is released from the surface. See figure 5.1. A second reaction pathway is created by the formation of various silanols ($Si_mH_n(OH)_p$) due to the consumption of silane radicals by the reactive oxygen. These silanols are observed by mass spectrometry where a largest peak is observed for the $Si(OH)_3$ radicals [10]. These precursors participate in the silicon oxide deposition. It is possible that the silanols cluster together into particles which can be observed as a white powder [10]. Such a powder is also observed in the exhaust of our deposition chamber.

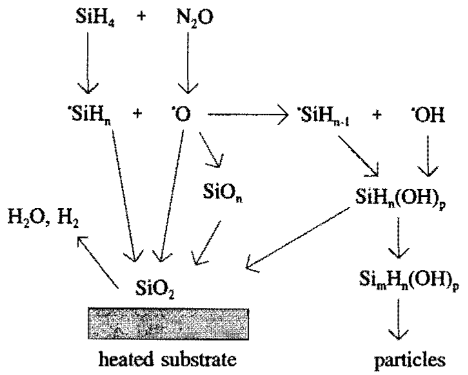

Figure 5.1, The reaction pathways of SiO_2 deposition with N_2O and SiH_4 as source gases. after Smith [10].

Smith [10] also states that higher silane flows which generally results in higher deposition rates can be tolerated without film degradation as long as the amount of oxygen is sufficient for SiO_2 deposition.

Deposition of silicon nitride with silane and ammonia has the same reaction mechanisms as in the case of silicon oxide. Beside the direct deposition from the radicals in the indirect reaction pathway aminosilanes (SiN_nH_m) are created instead of silanols [12]. These aminosilanes are thought to be the principal precursors for silicon nitride deposition. For silicon oxide deposition the difference in participation between the direct pathway of oxygen and silane radicals and the silanols is less clear [10,12]. Equation 5.1 and 5.2 show the precursor forming reaction of aminosilanes and the surface reaction for stoichiometric silicon nitride deposition (Si_3N_4).

$$SiH_4 + 4\,NH_3 \xrightarrow{\text{plasma}} Si(NH_2)_4 + 4\,H_2 \tag{5.1}$$

$$3\,Si(NH_2)_4 \xrightarrow{\text{heat}} Si_3N_4 + 8\,NH_3\uparrow \tag{5.2}$$

5.2.2 The Reactor

The reactor is part of the Oxford Plasma Technology cluster tool as described in the introduction. Figure 5.2 shows schematically the reactor layout used for microwave downstream deposition of silicon oxide and silicon nitride. The vacuum is created by a single stage Edwards roots blower (EH 250) which is supported by a rotary dry pump (Edwards DP 80) which gives a base pressure of a few mTorrs. The gases are exhausted via a dry scrubber. It is possible to introduce the gases N_2O, N_2 and NH_3 through a gas ring in the top of the microwave cavity. These gases flow through a quartz tube. Silane and nitrogen are introduced in the vicinity of the heated substrate table via a second gas distribution ring. The gas flows are regulated by mass flow controllers. A CF_4/O_2 mixture, which can be supplied in the top of the cavity as well, is used for chamber cleaning purposes. A gate valve is used for adjusting the process pressure. The substrate is located downstream from the microwave cavity on a heated table. The table temperature can be varied between room temperature and 400 °C.

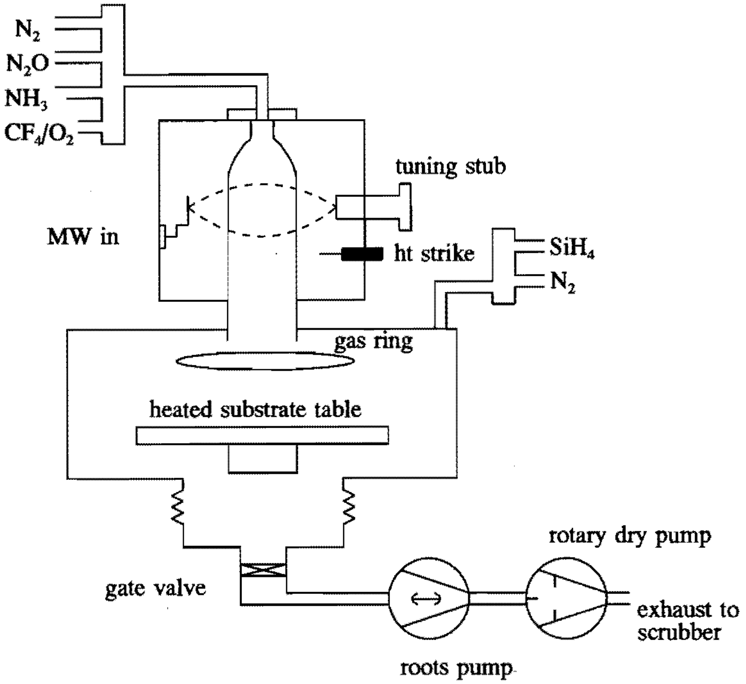

Figure 5.2, Schematic layout of the microwave downstream PECVD reactor used for silicon oxide and silicon nitride deposition.

The table height is adjustable with respect to the discharge cavity. No additional RF power can be supplied at the table. In this way less damage to the semiconductor surface is expected since the surface is prevented from excessive ion bombardment. In the cavity microwave power is emitted from an aerial located outside the quartz tube within the cavity. The microwave power is supplied at a frequency of 2.45 GHz with an Astex microwave power generator (S-250) with a range of 0 to 250 Watt. On the other side of the resonance cavity there is a manual tuning stub to reduce the reflected power. By adjusting the tuning stub to half of one wavelength which is approximately 60 mm minimal reflection is obtained. This is schematically indicated in figure 5.2. A high tension strike (ht) is connected to the resonance cavity to ignite the plasma. Through diffusion and pumping the reactive species flow downstream to the substrate chamber where deposition is initiated on the heated substrate. Due to the presence of the reactive species created in the microwave cavity, deposition is possible at much lower substrate temperatures, (< 400 °C) as already mentioned. This is in contrast with chemical vapour deposition where the temperatures need to be sufficiently high (typically ~ 700 °C) to crack the molecules in order to create these reactive species.

5.3 Experimental

5.3.1 Introduction

During the silicon oxide and silicon nitride deposition experiments a standard process was chosen and one parameter was varied while the others were kept constant. For silicon oxide deposition the deposition temperature, the silane and nitrous oxide flows, the pressure and the nitrogen flow were varied. For silicon nitride deposition the nitrous oxide is replaced by ammonia. Instead of nitrous oxide the ammonia flow was varied in the experiments for silicon nitride deposition. Typically 150 nm thick layers were investigated. Subsequently the refractive index, the etch rate and the deposition rate were investigated as function of the process parameters. Compositional analysis was done by Rutherford backscattering spectrometry and elastic recoil detection by L.J van IJzendoorn at the Particle Physics group of the Physics department of the Technical University of Eindhoven. The hydrogen content, as measured by elastic recoil detection, is measured without post deposition annealing which is often used to reduce the hydrogen incorporation.

5.3.2 Refractive index, etch rate and deposition rate

The refractive index was measured with a Rudolph Research (RR100) ellipsometer at a wavelength of 546.1 nm and an angle of incidence of 70 degrees with respect to the normal of the substrate. Generally the refractive index is a guide for determining whether a silicon oxide or nitride layer is silicon rich. Details will be described in the subsequent paragraphs on silicon oxide and nitride deposition.

For silicon dioxide the etch rate of the layers is measured in diluted hydrofluoric acid at room temperature (HF(40%) : H_2O = 1 : 50) whereas the silicon nitride films are etched in a buffered HF solution. The etch rates will be compared to those obtained on thermally deposited dielectric layers as described in literature. In combination with the deposition rate the etch rate gives a qualitative indication about the density of the deposited layers. If the deposition rate and the etch rate increase it can be concluded that the density of the layer is reduced. The deposition rate is deduced from the layer thickness as measured with a Tencor α-step 200, after removing the layer partially. This thickness is compared to the thickness obtained from the ellipsometric measurements.

5.3.3 Compositional analysis.

5.3.3.1 Rutherford Backscattering Spectrometry

Rutherford Backscattering Spectrometry (RBS) is well known as an ion beam analysis technique for the compositional analysis of thin films. Beside quantitative information on the elemental composition also depth profiling can be performed without the need of sputtering the film. In RBS an energetic ion beam is directed to the film with an energy of typically 2 MeV. The technique is based on the detection of the ions backscattered by the nuclei of the target. The kinetic energy of the backscattered ions is related to the mass of the target atoms and the scattering angle and is used to identify the elements of the target. With incident helium ions of 2 MeV Rutherford cross-sections can be used to quantify the RBS spectra. Depth resolution is obtained since helium atoms which travel deeper into the film, before scattering occurs, loose energy due to interaction with the electrons in the target and subsequently will occur at a lower energy in the RBS spectrum.

In our experiments a 4 MeV He^+ beam of ~100-200 nA from the 3-30 MeV AVF-cyclotron at the Physics Department of the Eindhoven University is used. The angle of incidence of the beam with the substrate is 20° and the RBS detector is at an angle of 165° with the direction of the incoming beam. A 4 MeV beam implies the application of non Rutherford cross-sections to quantify the RBS spectra [13,14,15,16]. Quantification of the RBS spectra is carried out using the computer programm RUMP. The sensitivity of the measurements on low Z elements (carbon, oxygen and nitrogen) is increased, due to the enhanced scattering cross-sections at 4 MeV, compared to the Rutherford cross-sections. The quantification procedure was verified with a Low Pressure Chemical Vapour Deposition (LPCVD) grown silicon nitride layer with accurately known elemental composition [9].

Figure 5.3 shows a RBS spectrum of the LPCVD grown silicon nitride and a microwave downstream deposited silicon oxide layer. The position of the RBS detector in the experiment is clarified in the insert of figure 5.3. The arrows indicate the energy of the He ions scattered at the surface on carbon (C), nitrogen (N), oxygen (O) and silicon (Si). The carbon peaks on the surface of the dielectric layers are caused by the deposition from residual gases in the vacuum system during the RBS measurements. The oscillation in the RBS yield, near channel 335, is due to a change in scattering cross-section of the silicon atoms at helium energies around 3.7 MeV [13]. The width and the area of the peaks can be related to the film thickness.

Backscattering spectrometry is restricted to target elements whose mass is greater than the mass of the incoming helium. For this reason it is not possible to measure the amount of hydrogen incorporation by RBS. Elastic recoil detection which will be discussed in paragraph 5.3.3.2 gives the possibility to detected the hydrogen recoiled from the target. As a final remark it is important to know that high energy ion scattering techniques do not give any information about the chemical nature of the bondings.

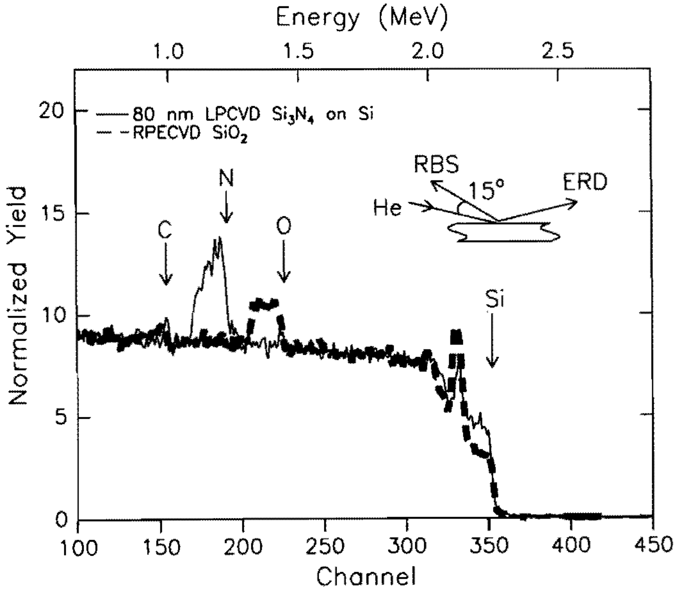

Figure 5.3, A RBS spectrum of the reference LPCVD deposited Si_3N_4 and a microwave downstream deposited SiO_2 layer. The arrows indicate the energies of the He ions scattered at the surface on C, N, O and Si.

5.3.3.2 Elastic Recoil Detection

As mentioned earlier plasma deposited dielectric films contain hydrogen concentrations up to 30 percent. Since the hydrogen plays an important role in the properties of PECVD grown dielectric films, it is necessary to obtain more information about the hydrogen incorporation. This can be done by IR spectroscopy which measures the chemical nature of different bonds by determining the absorptions peaks in the infrared spectrum. In this way the vibrational, stretching and bending absorption frequencies of Si-H, O-H and N-H can be measured to quantify the amount of hydrogen incorporation.

Since RBS is not able to detect hydrogen atoms Elastic Recoil Detection (ERD) is used. Elastic recoil detection is based on the measurement of the hydrogen atoms recoiled out of the film by the incoming helium ions. This means that ERD and RBS measurements can be performed simultaneously. In these experiments the ERD detector is located at an angle of 30° with respect to the direction of the incoming beam. A low angle of incidence is necessary for elastic recoil detection. The recoiled protons traverse the applied Mylar foil of 16.8 μm, located in front of the detector. This foil is required to stop the forward scattered Helium ions. Apart from the amount of hydrogen incorporation an incident beam of 4 MeV allows simultaneous detection of nitrogen incorporation by Nuclear Reaction Analysis (NRA) through the $^{14}N(\alpha,p)O^{17}$ reaction [17,18]. Because the oxygen is created in either the ground state or an excited state protons will be detected at two different energies (p_0 and p_1). In case of the $^{14}N(\alpha,p_1)O^{17}$ reaction the excited oxygen nucleus undergoes a transition to its ground level with emission of a gamma quant.

The proton energies at a scattering angle of 30° due to the He(α,p_o) and He(α,p_1) reaction are 2.355 MeV and 0.9404 MeV respectively. These energies are well above and below the energy of an elastically recoiled proton (1.920 MeV) for 150 nm thick films. The hydrogen content of the LPCVD grown silicon nitride layer was known and used to quantify the ERD measurements [9]. Figure 5.4 shows a typical ERD spectrum for the LPCVD grown silicon nitride and a microwave downstream deposited silicon oxide. The protons detected from the $^{14}N(\alpha,p_0)^{17}O$ and $^{14}N(\alpha,p_1)^{17}O$ reactions of the silicon nitride film are clearly observed. The position of the ERD detector in the experiment is clarified in the insert of figure 5.4. No distinction however can be made by ERD if the hydrogen in the silicon nitride films originates from the silane or ammonia. However experiments have been reported using ND_3 instead of NH_3 by which the origin of the hydrogen can be revealed [19].

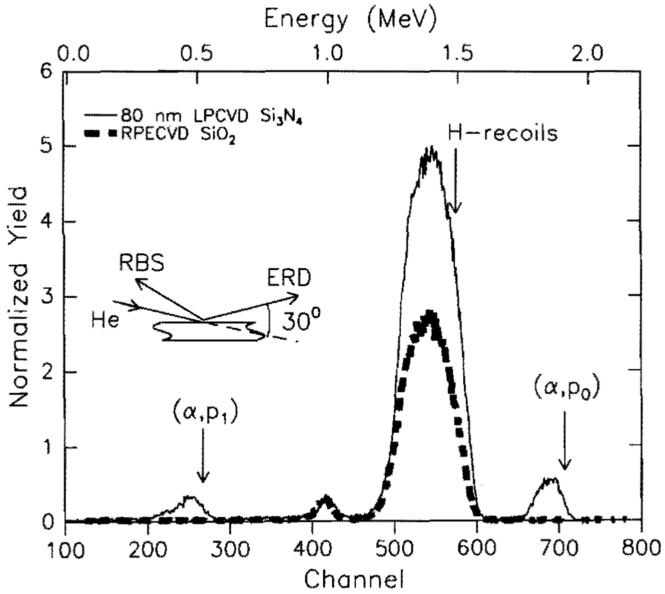

Figure 5.4, Elastic recoil detection spectrum of the reference LPCVD grown Si_3N_4 layer compared to remote PECVD SiO_2. The little peaks on both side of the recoiled hydrogen are due to the $^{14}N(\alpha,p_0)^{17}O$ and $^{14}N(\alpha,p_1)^{17}O$ reaction of silicon nitride.

5.4 Silicon oxide deposition.

5.4.1 Introduction

In the case of silicon oxide deposition one process parameter was varied while the others were kept constant. The initial process conditions are a 40 sccm N_2O gas flow diluted in 90 sccm N_2 in the top of the microwave cavity while in the chamber a SiH_4 and N_2 flow of 4 and 30 sccm, respectively are used. The microwave power is 200 W, the table temperature 300 °C and the process pressure is 100 mTorr. These process conditions give a refractive index of 1.50 and a deposition rate of about 60 nm/min. Stoichiometric SiO_2 films have a refractive index of 1.46. The layers are deposited on silicon substrates. Typically 150 nm thick silicon oxide layers were investigated. The variations in the process conditions are respectively 100 to 400 °C for the deposition temperature, 0-40 sccm for the N_2O flow, 4-8 sccm for the SiH_4 flow and the pressure was varied between 100-300 mTorr. The influence of the microwave power is not investigated since a minimum power of 200 Watt was necessary to obtain a stable plasma.

5.4.2 The influence of the deposition temperature

The deposition temperature was varied between 100 and 400 °C. Figure 5.5 shows the refractive index and the deposition rate while figure 5.6 shows the hydrogen content and the etch rate in diluted HF. The hydrogen content decreases from 2.5 at% at 100 °C to 1.3 at% at 400 °C. At 200 and 300 °C the hydrogen contents are 2.2 and 1.9 at% respectively. Figure 5.7 shows the ERD spectra at different deposition temperatures. The decrease in hydrogen incorporation as function of deposition temperature is clearly demonstrated. A reduction in hydrogen concentration with increasing process temperature is commonly observed in plasma deposited silicon oxide layers since the hydrogen bonds break easier at higher substrate temperatures [3,20,21]. The amount of hydrogen incorporation is comparable to remote PECVD deposited silicon oxide layers in literature [22,23,24].

The refractive index and the deposition rate increase with increasing table temperature. This is also observed by Adams [3] with a N_2O, SiH_4, Ar gas mixture in a parallel plate reactor and Herak [22] using an ECR reactor with identical gas mixture. Herak ascribed the increase in deposition rate to an increase in the thermally activated reactions at the surface. He also observed that the deposition rate decreases with increasing temperature if the substrate was placed in direct contact with the plasma instead of located in the plasma afterglow. Remarkable is the transition in etch rate at a deposition temperature of 200 °C. Generally a decrease in etch rate is observed due to a density increase as function of temperature [21,25].

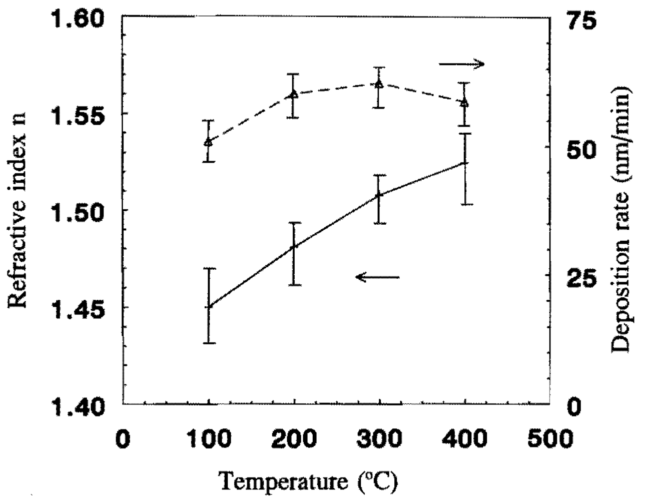

Figure 5.5, The deposition rate and the refractive index as function of the deposition temperature of microwave downstream deposited silicon oxide.

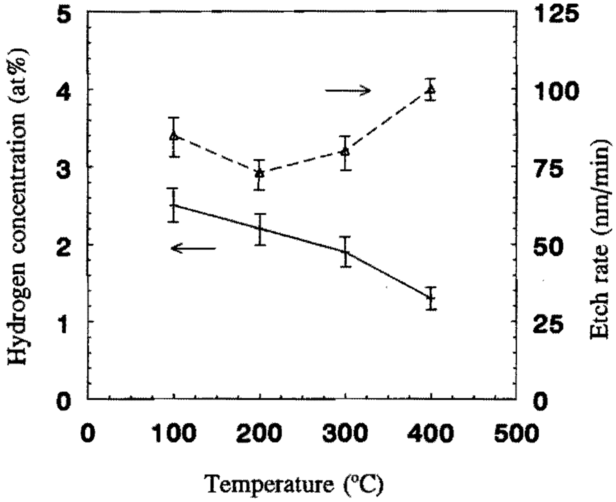

Figure 5.6, The hydrogen content as measured by ERD and the etch rate in diluted HF as function of the deposition temperature for microwave downstream deposited silicon oxide.

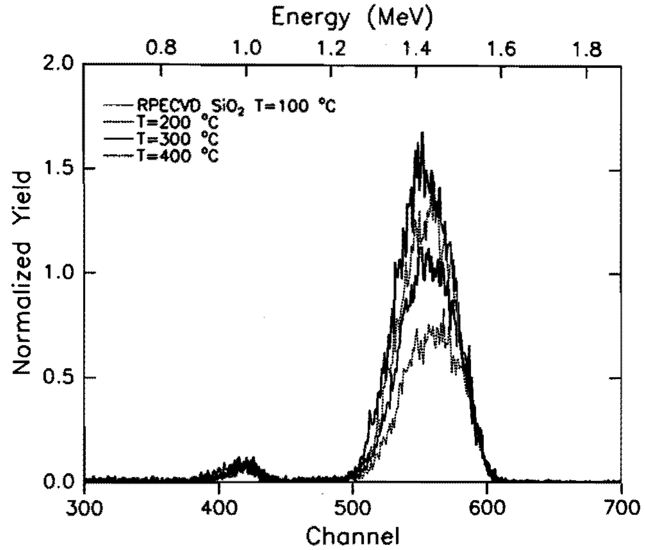

Figure 5.7, The ERD measurements showing the decrease in hydrogen content as function of increasing substrate temperature of RPECVD silicon oxide.

The etch rates are comparable to PECVD deposited silicon oxide layers and about 8 to 10 times faster than those of thermal oxides [3]. The RBS spectra showed a stoichiometric composition at all temperatures. No nitrogen incorporation was observed (< 0.4 at%). It is assumed that changes in the refractive index and etch rates originate from changes in the film structure and density. This is also mentioned in literature [25,26].

5.4.3 The influence of the silane and the nitrous oxide flow

Generally changes in composition are induced by variations in the silane (SiH_4) or nitrous oxide (N_2O) flow. In literature a strong increase in the refractive index is observed with an increase of silicon incorporation [26]. In our experiments the silane flow was varied in 4, 6 and 8 sccm and the nitrous oxide flow was decreased from 40 to 20 in steps of 10 sccm. Figure 5.8 shows that the refractive index increases in both experiments with the N_2O/SiH_4 ratio. This ratio was varied between 5 and 10. However no compositional changes could be observed by the RBS measurements. Increasing the silane flow from 4 to 8 sccm increased the deposition rate from 60 to 120 nm/min whereas no change in etch rate was observed. This increase in deposition rate can be ascribed to the presence of more active silane and the presence of sufficient active oxygen. The hydrogen incorporation decreased with increasing silane flow from 1.9 to 1.4 at%. Reduction of the N_2O flow from 40 to 20 sccm caused a slight reduction in the deposition rate whereas again no change in the etch rate was observed. The low change in deposition rate indicates that the nitrous oxide is effectively excited and enough reactive oxygen is supplied. At zero N_2O flow still a deposition rate of a few nm/min was observed. No further investigation was performed on this layer. It is likely to be a hydrogenated amorphous silicon film (a-Si:H) [27].

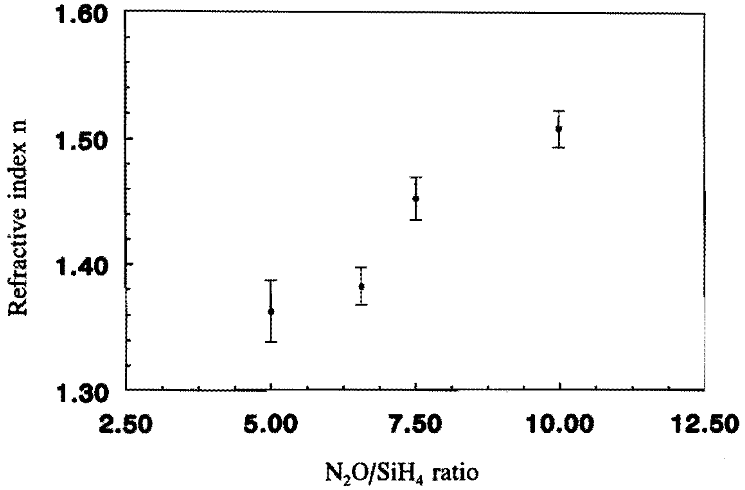

Figure 5.8, The refractive index as function of the N_2O/SiH_4 ratio of microwave downstream deposited silicon oxide.

5.4.4 The influence of the pressure, the table height and the nitrogen flow.

When increasing the pressure to 300 mTorr a strong reduction in the deposition and etch rate is measured. The deposition rate reduces from about 60 to 35 nm/min with pressures of 100 and 300 mTorr respectively, whereas the etch rate decreases by a factor of 2. This suggests an increase in film density of the silicon oxide layer. The refractive index decreases slightly with increasing pressure. The uniformity however degrades with increasing pressure. For this reason the pressure was not further increased. Beside a low pressure, an increase of the distance between the substrate table and the excitation source improved the uniformity. Increasing the distance effectively reduces the amount of active species and is comparable to a pressure reduction. A deviation of film thickness across a 3 inch wafer was found to be ± 6%. The uniformity was asymmetric over the wafer.
The amount of nitrogen flow did not show any influence on the characteristics of the layers. A certain nitrogen flow is necessary for maintaining the plasma in the excitation cavity and to improve the uniformity by diluting the silane.

5.4.5 Summary

No stoichiometric variation is observed in microwave downstream PECVD deposited silicon oxide layers upon changes in deposition temperature, pressure, gas flows and pressure. A hydrogen incorporation between 1.4 and 1.9 at% is measured by ERD. The absence of nitrogen contamination suggests a much stronger interaction between the silicon and oxygen than that of silicon with nitrogen radicals. As a function of deposition temperature a clear decrease in hydrogen incorporation was observed. The refractive index increased as function of the N_2O:SiH_4 ratio, which was varied between 5 and 10. Because no stoichiometric variation is observed which is in accordance with the small change in etch rate, it is suggested that the variation is caused by structural and density variations within the silicon oxide layer. It seems that the specific silicon oxide characteristics depend on the reaction kinetics at the substrate surface and the process conditions.

5.5 Silicon nitride deposition

5.5.1 Introduction

In plasma deposited silicon nitride films a percentage up to 35 % hydrogen can be incorporated [28]. Because hydrogen is incorporated, plasma deposited silicon nitride is often written as SiN_xH_y.
The physical properties like the refractive index, density and etch rate in buffered HF depend on the silicon to nitrogen ratio and the amount of hydrogen incorporation. Incorporation of oxygen from rest gases also affects these characteristics. Samuelson [29] showed that the refractive index correlated linearly with the Si-H/N-H ratio. Claasen et al. [30] described the refractive index as a linear function of the Si/N ratio as shown in equation 5.3,

$$n = 0.7 * Si/N + 1.39 \tag{5.3}$$

High refractive indexes were obtained in silicon rich layers by these authors. Their experiments were done in a parallel plate reactor using SiH_4 and NH_3 diluted with either nitrogen, argon or hydrogen. The authors observed that nearly all hydrogen was bond to silicon in silicon rich layers and that the amount of N-H bonds increased with decreasing silicon incorporation. This explained the observations made by Samuelson. The total amount of hydrogen remained nearly constant during their experiments and only a shift of the type of bond was observed. They observed a hydrogen content of 23 at% at a deposition temperature of 300 °C.
The etch rate in a buffered HF solution also depends on the Si/N ratio and generally increases with decreasing ratio. Apart from the Si/N ratio, the etch rate of silicon nitride films depends on the density and the dilution gas used [30]. The density decreases with the increase of silicon incorporation due to the difference in atomic size between silicon and nitrogen. A decrease in film density is generally also associated with a higher refractive index [30]. About the correlation between the etch rate and the amount of hydrogen incorporation much disagreement exists in literature [30,31,32].
During the silicon nitride deposition one process parameter was varied while the others were kept constant. The initial process conditions are a 50 sccm NH_3 gas flow diluted by 100 sccm N_2 in the top of the microwave cavity and a SiH_4 and N_2 flow of 3 and 50 sccm respectively, in the chamber. The microwave power is 150 W, the table temperature 300 °C and the process pressure is 100 mTorr. The plasma was stable at lower microwave powers. These process conditions give a refractive index of 1.79 and a deposition rate of 20 nm/min. Stoichiometric Si_3N_4 films have a refractive index of 2.05 [33]. The layers are deposited on silicon substrates. Typically 150 nm thick silicon nitride layers were investigated. The variations in process conditions are 100 to 400 °C for the deposition temperature, 3-20 sccm for the SiH_4 flow, 25-75 sccm for the NH_3 flow and the nitrogen in the chamber was varied between 0-100 sccm. The microwave power and the pressure were varied from 150 to 250 Watt and from 100 to 250 mTorr respectively. Because the chamber was dedicated for a long period to silicon oxide deposition the chamber was cleaned for 10 minutes in a CF_2/O_2 plasma and subsequently 3 times 10 minutes the standard process of silicon nitride was performed.

5.5.2 The influence of the deposition temperature

Figure 5.9 shows the silicon to nitrogen ratio and the amount of oxygen and hydrogen incorporation as measured by RBS and ERD for microwave downstream deposited silicon nitride as function of the temperature. Figure 5.10 shows the refractive index and the etch rate in buffered HF as function of the deposition temperature. The etch rate decreases remarkable by increasing the table temperature from 100 to 200 °C. A decrease of etch rate with temperature is commonly observed for PECVD deposited silicon nitride films [31,34,35]. This is probably due to an enormous densification of the silicon nitride film since its composition only slightly changes. The deposition rate decreases from 24 to 20 nm/min at temperatures of 100 and 400 °C respectively. The oxygen incorporation is between 4 and 8 at% which is likely to originate from residual gases in the reactor or from oxygen sputtered from the aluminium oxide reactor walls. The oxygen is incorporated due to the high reactivity between oxygen and silane. On increasing the temperature from 200 to 400 °C the hydrogen incorporation decreases from 23 to 18 at% whereas the silicon to nitrogen ratio slowly approaches the stoichiometric value of 0.75. Generally a more pronounced decrease in hydrogen incorporation is observed with increasing deposition temperature [28,35,36]. The amount of hydrogen incorporation is however comparable to PECVD deposited silicon nitride layers [28,37,38]. The excess of nitrogen is slightly reduced with increasing deposition temperature which is in accordance with the increase of the refractive index [34,39].

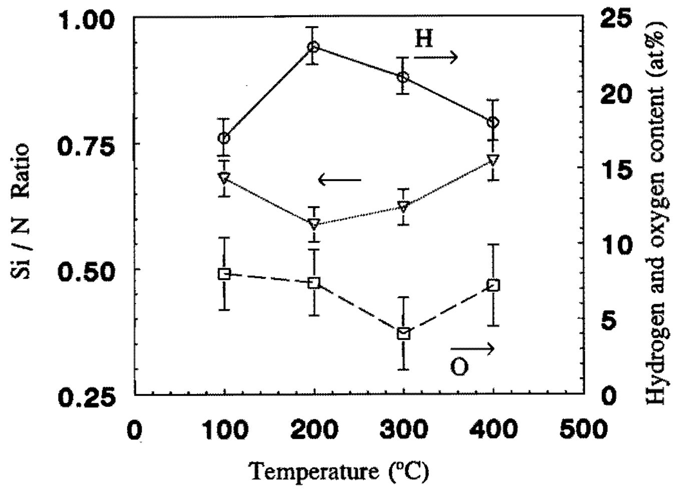

Figure 5.9, The influence of the deposition temperature on the composition of microwave downstream deposited silicon nitride.

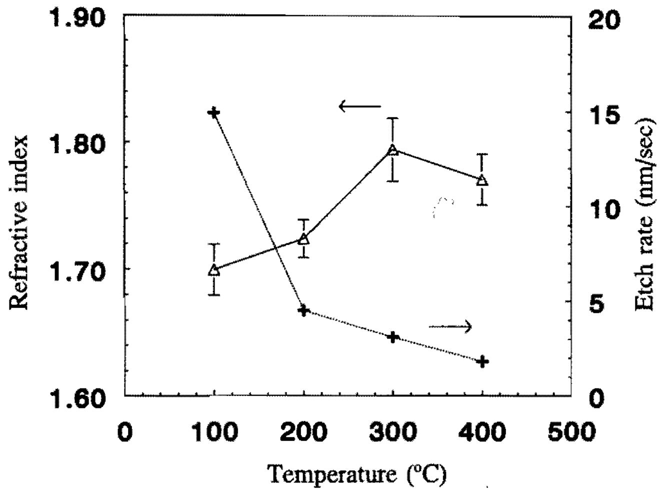

Figure 5.10, The refractive index and the etch rate in buffered HF of microwave downstream deposited silicon nitride as function of the deposition temperature.

5.5.3 The influence of the silane flow.

The silane flow was increased from 3 to 20 sccm. Figure 5.11 shows the hydrogen incorporation and the silicon to nitrogen ratio as function of the NH_3/SiH_4 gas flow ratio. Whereas at a silane flow of 3 sccm (NH_3/SiH_4 = 16.7) an amount of 4 at% oxygen was incorporated, no oxygen could be measured by RBS at higher silane flows. Figure 5.12 shows the refractive index and the etch rate as function of the NH_3/SiH_4 gas ratio and figure 5.13 shows the measured deposition rate.

The hydrogen incorporation (Figure 5.11) remained nearly constant whereas the silicon nitride film changes from silicon rich to nitrogen rich with increasing NH_3/SiH_4 gas ratio. Stoichiometric silicon nitride is obtained for a gas ratio between 5 and 7. The refractive index increases with increasing silicon incorporation but is still below the refractive index of thermally deposited silicon nitride which contains only little H incorporation. This lower refractive index is often ascribed to the amount of hydrogen incorporation. The etch rate also increases with silicon incorporation which is in accordance with literature [31]. The deposition rate increases with decreasing NH_3/SiH_4 gas ratio which can be ascribed to the increase in silicon incorporation and the formation of films with lower densities. In spite of the difference in system configuration Piccirilio et al. [39] obtained similar results as function of the NH_3/SiH_4 gas ratio on the silicon nitride films. They measured the Si/N ratio, the refractive index, the etch and deposition rates and the hydrogen content as function of the temperature, gas ratio and RF power. Their experiments were performed in a capacitively coupled parallel plate PECVD reactor at 13.56 MHZ using silane and ammonia.

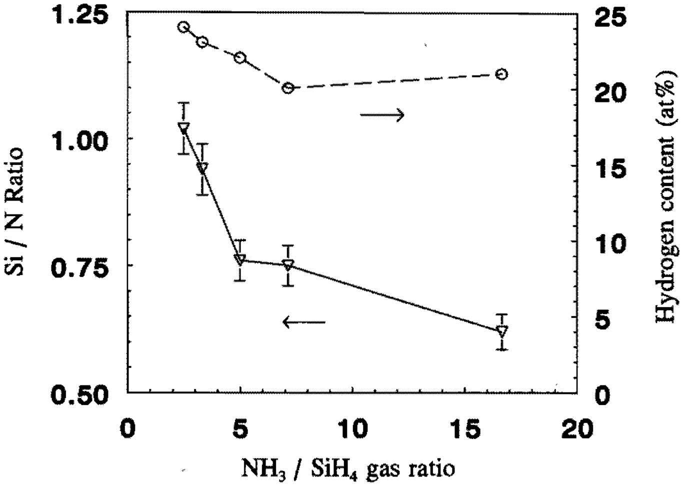

Figure 5.11, The Si/N ratio and the hydrogen incorporation as measured by RBS and ERD of microwave downstream deposited silicon nitride layers as function of the NH_3/SiH_4 gas flow ratio.

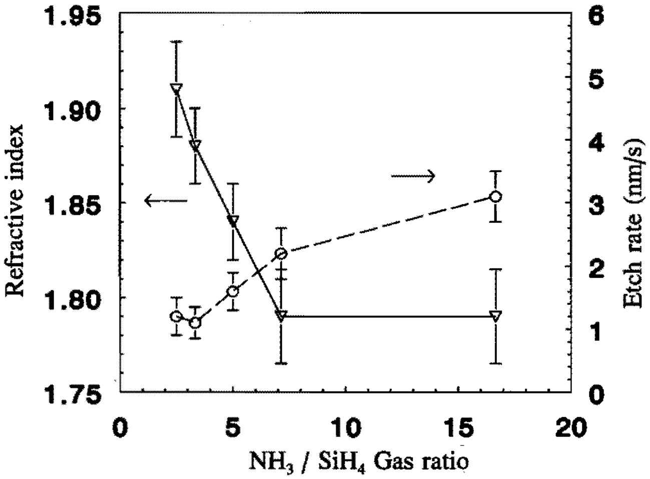

Figure 5.12, The refractive index and the etch rate in buffered HF of silicon nitride films as function of the NH_3/SiH_4 gas flow ratio.

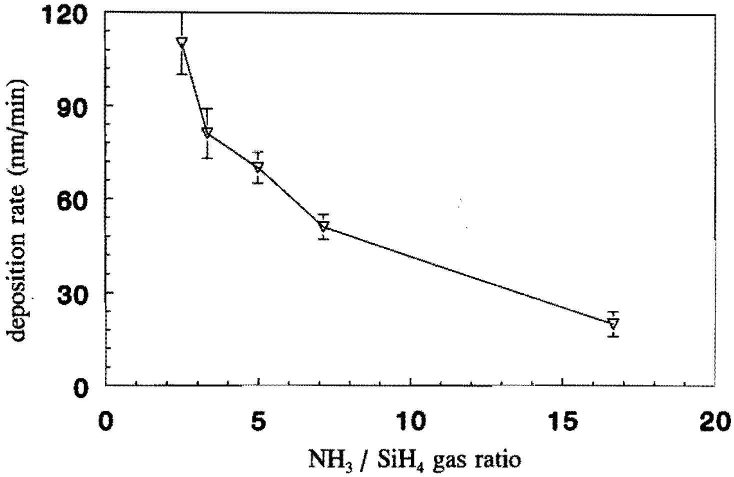

Figure 5.13, The deposition rate as function of the NH$_3$/SiH$_4$ gas flow ratio of remote PECVD deposited silicon nitride.

5.5.4 The influence of the NH$_3$ flow and the microwave power

Whereas in the standard process at an NH$_3$ flow of 50 sccm an oxygen incorporation of 4 at% was measured no oxygen incorporation was observed at an ammonia flow of 75 sccm. At a NH$_3$ flow of 25 sccm however 23 at% oxygen was incorporated and even 4 at% carbon was measured in the silicon nitride film. The origin of the amount of oxygen and carbon incorporation in this film was unclear. The refractive index increased from 1.69 to 1.79 and 1.82 and the etch rate decreased from 25 to 3 and 1.2 nm/s for ammonia flows of 25, 50 and 75 sccm respectively. This increase in refractive index and decrease in etch rate is in agreement with an increasing oxygen incorporation. The deposition rate decreased from 25 to 18 nm/min for an ammonia flow of 25 and 75 sccm respectively.

Identical results were obtained when the microwave power was increased to 250 Watt. Here also an incorporation of 4 at% carbon and 23 at% oxygen was observed. The refractive index and the etch rate showed similar behaviour as the experiment using 25 sccm ammonia. The films deposited before and after the layers where a carbon and large oxygen incorporation was observed, did not show any of these elements. This suggests that in both cases the contamination depends on the process conditions.

5.5.5 The influence of the process pressure

Increasing the pressure to 250 mTorr degraded the uniformity of the silicon nitride film. The Si/N ratio however became stoichiometric and the hydrogen incorporation decreased from 21 to 16 at%. No oxygen incorporation could be measured. The deposition rate increased to 34 nm/min due to an increase in reactants whereas the etch rate decreased to 0.75 nm/s. The refractive index was 2.04 which is close to thermally deposited silicon nitride. In addition to the pressure also the table height improved the uniformity if the distance to the microwave cavity is increased. A variation of film thickness of ± 3% can be obtained across a 3 inch wafer. The variation for silicon nitride is concentric in contrast to the asymmetric deviation observed for silicon oxide.

5.5.6 The influence of the nitrogen flow

Finally the nitrogen flow in the chamber was varied between 0 and 100 sccm. No changes in the deposition rate and the refractive index were observed. An oxygen incorporation between 1.8 and 6.4 at% is observed which is in agreement with the standard process performed at 300°C in the beginning of the test sequence. The Si/N ratio however changed to 0.70 which suggest a slight change in the deposition characteristics over all the layers grown. At higher nitrogen flows the hydrogen incorporation decreases slightly.

5.5.7 Summary

Silicon nitride layers have been grown by microwave PECVD and the composition strongly depends on the process conditions. Near stoichiometric composition was obtained at a NH_3/SiH_4 gas ratio between 5 and 7. The refractive indexes obtained at these ratios is in between 1.79 and 1.84 which is well below the refractive index of stoichiometric silicon nitride. The hydrogen incorporation of the investigated layers is about 20 at% and is almost independent of the process conditions. This is comparable to other plasma enhanced CVD processes [28,37,38] although in literature much lower hydrogen incorporation is reported in remote PECVD systems [36,40,41].

5.6 Microwave downstream PECVD

Silicon oxide and silicon nitride layers have been grown by remote plasma enhanced chemical vapour deposition. For silicon oxide deposition no compositional changes could be observed as function of process variations. The refractive index was near stoichiometric at a N_2O/SiH_4 gas ratio of 6.5. The hydrogen incorporation in these layers was low and typically between 1.4 and 1.9 at% at a deposition temperature of 300°C.
Silicon nitride showed strong compositional changes upon process variations. Increasing the NH_3/SiH_4 gas ratio increased the amount of silicon incorporation. The hydrogen incorporation was between 15 and 23 at% which is comparable to other PECVD deposited silicon nitride films, although better results are described in literature. Near stoichiometric layers were obtained if the NH_3/SiH_4 gas ratio was between 5 and 7. For both layers also near stoichiometric layers were obtained at higher pressures although the uniformity across the layers decreased with pressure. It is believed that the density of both types of films increases with increasing pressure. The deposition rate of silicon oxide and silicon nitride was sufficient to control the thickness of the layers. The films are free of cracks although the silicon nitride films, deposited with the standard process, cracked when the layer was annealed at temperatures above 200 °C in the rapid thermal annealer. The silicon nitride was resistant to annealing if the layer thickness was less than 250 nm. The layer probably cracks due to stress incorporated in the films. For this reason silicon oxide was chosen for further processes.

5.7 References

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CHAPTER VI

Dry processed GaAs-based MESFETs and pseudomorphic HFETs

6.1 Introduction.

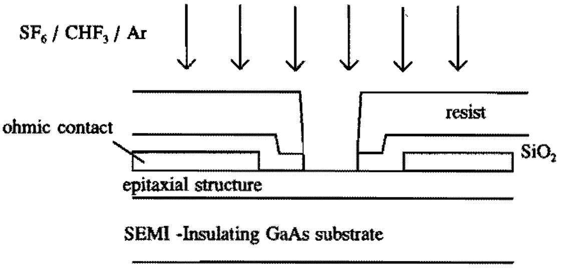
The gate recess, as already mentioned in chapter 1, is critical in the fabrication of field-effect transistors. Dry recess processes are primarily used for their uniformity and reproducibility. Often the uniformity is enhanced by using an additional etch stop layer in the structure. In RIE and ECR etch processes for transistor fabrication generally $SiCl_4$ ($+SF_6$), CCl_2F_2 or CH_4/H_2 gas mixtures are used [1-6]. For GaAs-based transistors an AlAs etch stop layer is often incorporated in the layer structure, and is used in the above mentioned gas mixtures. Although there is a tendency of a decreasing etch rate for the $CH_4/H_2/Ar$ ECR plasma with increasing aluminium content in AlGaAs layers, no additional etch stop layers have been used in the present work.

In this chapter the results obtained on dry recessed MESFETs and pseudomorphic HFETs will be discussed. The DC characteristics of MESFETs and the DC and high frequency characteristics of pseudomorphic HFETs will be compared to those of wet chemically processed transistors. The MESFETs are recessed at a substrate bias of -20 V whereas the pseudomorphic HFETs are processed at a DC bias of -40 Volt. Additional process steps, necessary for fabrication, and their influence will be discussed briefly. Finally the results obtained on a pseudomorphic HFET with an additional δ-doped layer on top of the AlGaAs spacer will be mentioned.

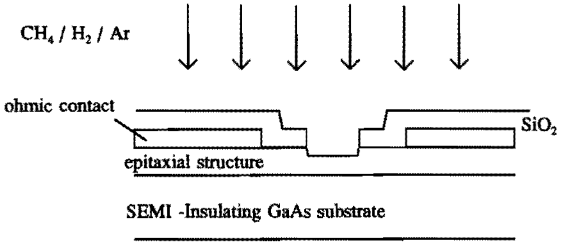
6.2 Fabrication of transistors

6.2.1 Fabrication process

Figure 6.1 shows the additional process steps necessary for the fabrication of the dry recessed transistors. The additional process steps were necessary since the resist, used to define the gate patterns, was not resistant to the $CH_4/H_2/Ar$ ECR plasma and no Schottky metallisation was available which was resistant to annealing temperatures above 375 °C. Often a $Ti_{10}W$ metallisation is used which is known to be resistant to temperatures up to 600 °C without degradation of the diode characteristics.


SF_6 / CHF_3 / Ar
resist
ohmic contact
SiO_2
epitaxial structure
SEMI -Insulating GaAs substrate

(a) SiO_2 etch


CH_4 / H_2 / Ar
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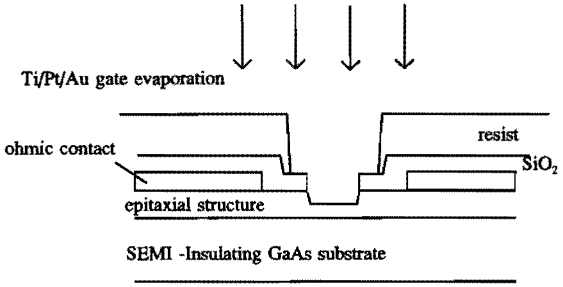
SEMI -Insulating GaAs substrate

(b) Gate recess


Ti/Pt/Au gate evaporation
resist
ohmic contact
SiO_2
epitaxial structure
SEMI -Insulating GaAs substrate

(c) Gate evaporation

Figure 6.1, Schematic overview of the process used for fabrication of a dry recessed transistor. The SiO_2 dielectric ECR etch (a), the dry gate recess (b) and the gate evaporation using a second gate resist mask (c) are shown.

After the mesa etch, evaporation of the Ge/Ni/Au ohmic contacts and subsequent annealing, a 250 nm silicon oxide layer is deposited over the whole sample at a temperature of 300 °C. Generally silicon nitride is used in transistor fabrication instead of silicon oxide. However for technological reasons and because the nitride films had a tendency to crack during annealing, silicon oxide was chosen in our experiments. The influence of a silicon oxide deposition on an AlGaAs/GaAs heterostructure will be discussed briefly in paragraph 6.2.2.
After defining the gate pattern a hard bake was performed for 10 minutes at 115 °C and subsequently the silicon oxide was opened in an ECR plasma using SF_6, CHF_3 and Ar (See figure 6.1a). The process conditions are a flow of 10, 2 and 2 sccm for SF_6, CHF_3 and Ar respectively, a microwave power of 400 W, a process pressure of 0.6 mTorr and a current of 140 and 80 Ampère through the upper and bottom magnet respectively. No additional substrate bias is used since the plasma initiates a DC self-bias of -24 Volt. The etch rate for silicon oxide is 20 nm/min which is a factor two slower than for silicon nitride. The selectivity between the resist and the silicon oxide in this process is about 1 to 1. No etch rate on GaAs is measured with the $SF_6/CHF_3/Ar$ ECR plasma. After defining the opening in the silicon oxide, the resist was removed in aceton. The sample was annealed after the dielectric etch at 400 °C for 1 minute to recover the damage introduced by this plasma. A start is made to investigate the influence of the dielectric etch on an AlGaAs/GaAs heterostructure. The first results will be discussed briefly in paragraph 6.2.3. After annealing the gate recess is performed by the $CH_4/H_2/Ar$ ECR plasma using the process conditions mentioned in chapter 3. The MESFETs are recessed at a substrate bias of -20 V whereas the pseudomorphic HFETs are processed at a DC bias of -40 Volt. After the gate recess and annealing at 400 °C to recover the damage a second gate lithography was made with a little overexposure to facilitate the mask alignment. Subsequently a Ti/Pt/Au Schottky metallisation was evaporated and lift off was accomplished.

6.2.2 The influence of SiO_2 deposition on an AlGaAs/GaAs heterostructure

The influence of a 200 nm thick silicon dioxide layer on the mobility (μ) and the sheet density (n_s) of an AlGaAs/GaAs heterostructure is investigated. The structure (W482) is the same as used in chapter 4 and consists of a 4 μm undoped GaAs buffer layer, a 20 nm $Al_{0.33}Ga_{0.67}As$ undoped spacer, a $5 \cdot 10^{12}$ cm^{-2} Si δ-doped layer, a 38 nm $Al_{0.33}Ga_{0.67}As$ $1 \cdot 10^{18}$ cm^{-3} (Si) donor layer and a 17 nm undoped GaAs toplayer. The structure is grown on a semi-insulating GaAs substrate. Electron transport in a 2-DEG is very sensitive to plasma radiation and ion bombardment. The presence of hydrogen in the plasma, originating from the silane, can introduce passivation of the silicon donor atoms. However, as function of the measurement temperature (5-300K) no influence was observed on the Hall mobility and sheet density of the 2-DEG. This means that no damage is expected from the silicon oxide deposition process.

6.2.3 The influence of a $SF_6/CHF_3/Ar$ ECR plasma on an AlGaAs/GaAs heterostructure

If the silicon oxide dielectric film, mentioned in the previous paragraph, was removed by a $SF_6/CHF_3/Ar$ ECR plasma at a DC bias of -24 Volt a strong degradation in the Hall mobility was observed. Table 6.1 lists the results on the Hall mobility and sheet density before and after annealing at 425 °C for 1 minute, compared to the measurements on a reference Hall bar. The measurements are shown for a temperature of 6.4 K. After removing the silicon oxide no Hall measurements could be performed. After a subsequent annealing step at 425 °C for 1 minute the density fully recovered whereas the Hall mobility recovered partially. This behaviour is identical as observed for the $CH_4/H_2/Ar$ ECR plasma except that the additional Si δ-doped layer does not prevent the degradation of the mobility. The reason for the degradation is unknown and further investigation of the influence of the $SF_6/CHF_3/Ar$ ECR plasma as function of additional substrate bias is necessary to minimise the damage. No experiments were done on uniformly doped GaAs layers as used in MESFET fabrication.

(W482)	μ (10^5 cm^2/Vs)	n_s (10^{11} cm^{-2})
Reference	7.97	3.80
etched	not measurable	
etched + 425 °C	5.48	3.70

Table 6.1, The influence of a dielectric plasma etch on the Hall mobility and sheet density of an AlGaAs/GaAs heterostructure with an additional Si δ-doped layer before and after annealing at 425 °C, compared to the Hall mobility and sheet density of a reference Hall bar. The measurements are shown for a temperature of 6.4 K.

6.3 Device performance

6.3.1 MESFETs

Typical data obtained on dry and wet etched MESFETs are compared in table 6.2. The transconductance (g_m), output conductance (g_d) and the contact resistance (R_c) of a 1*100 μm^2 gate MESFET are shown. Dry processing is performed at a DC bias of -20 V. Dry processed MESFETs show a better output conductance whereas a degradation in the transconductance is observed. The decrease in transconductance can be partially ascribed to the increased contact resistance. This is due to a not optimised processing since the structure is annealed a few times at 400 °C. A second reason is that passivation of GaAs by a dielectric layer can result in excessive stress of the dielectric layer by which interface states between the dielectric layer and the GaAs surface occurs. These interface states are responsible for shifts in threshold voltage, drain source saturation current and transconductance. The changes in MESFET parameters also depend on the orientation of the gate towards the crystal direction, the gate length, the dielectric thickness and the kind of stress (tensile or compressive) [7,8,9]. This is observed for silicon nitride and silicon oxide passivation layers. The amount of charges within the dielectric layer as well as the effect of the silicon oxide etch on the epitaxial structure is not known. For this reason much more investigation is required to minimise the influence of the different process steps on the GaAs epitaxial layers and devices.

	wet etched	dry etched
g_m (mS/mm)	220	160
g_d (mS/mm)	5.8	2.8
R_c (Ω-mm)	0.12	0.48

Table 6.2, Typical data of the transconductance (g_m), output conductance (g_d) and the contact resistance (R_c) of a wet recessed 1*100 μm^2 MESFET compared to a dry recessed.

6.3.2 Pseudomorphic HFETs

The $CH_4/H_2/Ar$ ECR plasma process is used in Pseudomorphic AlGaAs/InGaAs/GaAs Heterostructure Field Effect Transistor (PMHFET) gate recess fabrication. The PMHFET were characterised by direct current and on wafer high frequencies measurements($\leq$ 40 GHz). The results were compared to those obtained with wet chemical etched PMHFETs. The structure (W385) is grown by MBE on a semi-insulating substrate and consists of a 1.5 μm undoped GaAs buffer layer, a 15 nm undoped $In_{0.15}Ga_{0.85}As$ pseudomorphic layer, a 3 nm undoped $Al_{0.2}Ga_{0.8}As$ spacer, a 50 nm $1.5 \cdot 10^{18}$ cm^{-3} (Si) doped $Al_{0.2}Ga_{0.8}As$ donor layer and a 70 nm $2 \cdot 10^{18}$ cm^{-3} (Si) doped GaAs toplayer. The recess is performed at a DC bias of -40 V to a depth of approximately 85 nm. The transistors have a gate length and width of 1 and 100 μm respectively. Table 6.3 gives the transconductance (g_m), output conductance (g_d), drain source saturation current (I_{dss}), threshold voltage (V_t), transition frequency (f_T) and the maximum frequency of oscillation (f_{max}) of dry processed PMHFETs. The results are compared to those of a wet etched pseudomorphic HFET on the same epitaxial structure. Little influence on the DC characteristics was observed whereas the high frequency characteristics were slightly degraded. The degradation can probably be ascribed to the silicon oxide layer in combination with the input gate source capacitance. Additional capacitances due to the presence of silicon oxide reduces the unity current gain cut-off frequency. This frequency is inversely dependent on the gate-source capacitance. The changes in the S-parameters mainly occurred in the input reflection coefficient.

	wet	dry
$g_{m,max}$ (mS/mm)	340	370
g_d (mS/mm)	6.8	5.6
I_{dss} (V_{gs}=0V) (mA)	4.42	4.66
V_T (V)	-0.64	-0.53
f_t (GHz)	22.4	20.6
f_{max} (GHz)	>45	38

Table 6.3, The parameters extracted from DC and microwave measurements of a dry processed pseudomorphic 1*100 μm^2 HFET compared to a wet chemically etched transistor.

To obtain these results a few annealing steps at a temperature of 400 °C for 1 minute had to be introduced during the gate recess. The heat treatment was performed in the rapid thermal annealer. By this alternating process sequence the electrical activity of the silicon donor atoms was restored to act as a shield for the $CH_4/H_2/Ar$ ECR plasma. It was observed that without these intermediate annealing steps (also after the dielectric etch) the performance of the devices strongly degraded. After etching 40 nm of the 70 nm thick GaAs toplayer only little current remained, even after annealing a few minutes at 400 °C. The same observations have been described in chapter 4 on the AlGaAs/InGaAs/GaAs heterostructure without an additional silicon δ-doped layer. No recovery of the carrier concentration and Hall mobility could be obtained. Characterising 1*100 μm^2 gate length pseudomorphic HFETs gave transconductances of about 200 mS/mm. Also the high frequency measurements showed degraded performances. This suggests that a parallel MESFET is measured. As described in chapter 4, it seems that an enhanced trapping mechanism or a degradation of the AlGaAs/InGaAs interface, created by the $CH_4/H_2/Ar$ ECR process, is responsible for the effect observed. These results however show that the $CH_4/H_2/Ar$ ECR process is able to produce HFETs with good characteristics.

6.3.3 Pseudomorphic HFETs with additional δ-doped layer

Pseudomorphic HFETs have also been fabricated on identical structures as mentioned in the previous paragraph, however now a $5 \cdot 10^{12}$ cm^{-2} Si δ-doped layer is incorporated on top of the AlGaAs spacer (W540). No intermediate annealing steps were performed during the gate recess, although the structure was still annealed after the dielectric etch. Figure 6.2 shows the transconductance (g_m) and the drain source current (I_{ds}) as function of the gate source voltage (V_{gs}) for two samples. The gate recess is done with the ECR plasma at a DC bias of -40 V. The etch time was varied for both samples in respectively 8.5 (W540d2) and 10 (W540d1) minutes. The estimated recess depth is 85 and 100 nm respectively. The shift in threshold voltage and the gate voltage for the maximum transconductance is clearly observed in figure 6.2. For 1*100 μm^2 gate length transistors comparable f_T and f_{max} are obtained as for the structure without additional δ-doped layer. The uniformity across the samples (1.5 *1.5 cm^2) was good. No statistical evaluation has been done on the uniformity since the mask was not appropriate due to its great variety of different transistors.

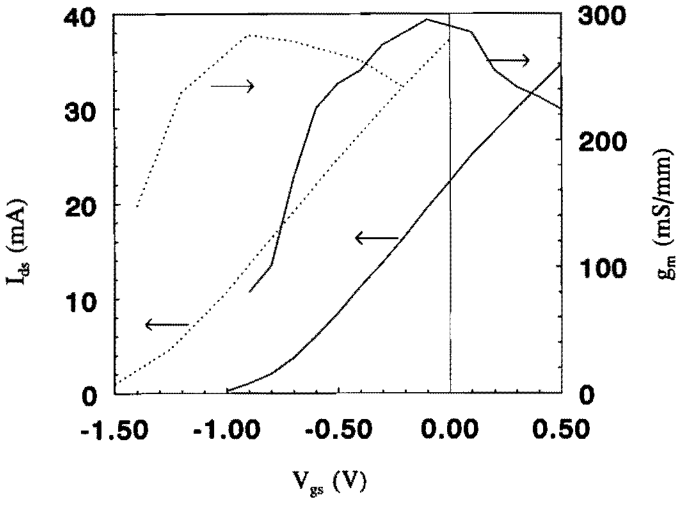


Figure 6.2, The drain source current (I_{ds}) and the transconductance (g_m) as function of the gate voltage (V_{gs}) for a pseudomorphic HFET with an additional Si δ-doped layer etched with the $CH_4/H_2/Ar$ ECR plasma for different etching times (recess depths). W540d1 (10 minutes etch) is represented by the full line.

6.4 Conclusions

Dry etched MESFETs and pseudomorphic HFETs with and without Si δ-doped layer have been processed using a $CH_4/H_2/Ar$ ECR plasma etch for the gate recess. The characteristics have been compared to wet chemical etched transistors. Dry etched MESFETs show a degradation in the transconductance whereas the pseudomorphic HFETs show results similar to wet chemically etched HFETs. This applies to both the high frequency and the DC characteristics. However additional annealing steps had to be introduced if no silicon δ-doped layer was present in the structure. This in contrast to chlorine based processes where no annealing is necessary to obtain good characteristics for HFETs [10].
The influence of the silicon oxide plasma etch has to be investigated more extensively. It can be concluded that the $CH_4/H_2/Ar$ ECR etch process is suitable for fabrication of heterostructure field effect transistors.

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CHAPTER VII

Conclusions and Recommendations.

7.1 Conclusions.

In this work the influence of using a $CH_4/H_2/Ar$ ECR plasma for the gate recess in GaAs based FETs has been investigated. The DC and HF characteristics of these dry processed transistors are compared to those of wet chemical etched transistors. To obtain these results a wet chemical technology has been developed first for field-effect transistors which is described in chapter 1. Ohmic contacts were optimised and give a contact resistance of about 0.1 Ω-mm at an annealing temperature of 400 °C for 1 minute. Wet chemically processed MESFETs, AlGaAs/GaAs and AlGaAs/InGaAs/GaAs HFETs showed good performances for 1 μm gate length transistors.

Subsequently different dry process steps have been studied and their influence on GaAs-based Schottky diodes and transistors have been measured and compared to the results obtained on wet chemical processed devices. The effect of in-situ argon ion cleaning before Schottky diode evaporation, the influence of $CH_4/H_2/Ar$ ECR plasma etching on Schottky diodes, AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures, and the comparison between wet and dry processed transistors is the main part of this work. To obtain these results a closer investigation was necessary on dielectric silicon oxide and silicon nitride deposition, used as mask during the fabrication of transistors, and the characteristics of $CH_4/H_2/Ar$ ECR plasma etching as a function of different process parameters.

Cleaning the GaAs surface with an argon ion beam and subsequent in-situ evaporation of the Schottky diodes did not improve the characteristics of the diodes compared to wet chemically cleaned diodes. This is described in chapter 2. The energy of the argon beam was varied between 50 and 750 eV and least damage is observed at the lowest energy with a neutralised beam. This after annealing at 300 °C for 24 hours. Despite the low energies, structural damage is incorporated and no improved behaviour is observed with respect to an annealed control diode. Also the transistor characteristics degrade after an argon cleaning step. It is expected that improvement can be obtained at lower energies than 50 eV. Consequently the energy range of the ion gun is too high to include this process as an additional process step in transistor fabrication.

Chapter 3 describes the etch characteristics of the $CH_4/H_2/Ar$ ECR plasma on different III-V semiconductors as a function of different process parameters. Most attention was dedicated to GaAs. Standard processes were obtained with etch rates satisfactory for gate recessing. The

standard process uses a microwave power of 600 Watt. The additional RF power (DC bias) on the substrate was kept low to minimise the amount of structural damage. At RF powers of 18 and 66 Watt a DC bias of -20 and -80 Volt is obtained respectively. Dependent on the RF power the methane to hydrogen gas flow ratio was changed to prevent polymer formation on the GaAs surface. At the lowest RF power a methane flow of 2 sccm was used whereas at 66 Watt the methane flow was increased to 6 sccm both diluted in 20 sccm hydrogen. Remarkable was the influence of additional argon. A dip in the etch rate was observed at an argon flow of 10 sccm. This was ascribed to a change from a desorption-limited to an adsorption-limited process mechanism. For GaAs an etch rate of 10 nm/min was obtained at a DC bias of -40 Volt, which is a satisfactory rate for gate recessing. The etch rate decreased with increasing aluminium content. At an aluminum content of 50% a selectivity of 1:2 was obtained with respect to GaAs, at a DC bias of -40 Volt. The selectivity decreased with increasing substrate bias due to a greater physical component in the process. For InGaAs higher etch rates are observed compared to GaAs.
For InP the process condition needed to be changed to prevent a preferential removal of the phosphorus and the formation of indium droplets. By reducing the microwave power to 150 Watt and increasing the DC bias to -150 Volt (38 Watt) reasonable smooth InP surfaces were obtained with vertical sidewalls. This process is however not further optimised with respect to the gas flows and microwave power.

In spite of the chemical nature of the $CH_4/H_2/Ar$ ECR plasma process physical damage will be introduced due to the presence of little additional DC bias. The influence and amount of damage is described in chapter 4. In addition to the structural damage also passivation occurs due to the presence of hydrogen. Passivation is due to the formation of Si-H complexes and gives a loss of electrical activity. The passivation can be recovered during a heat treatment. By C-V measurements it is observed that the passivation depth increases with decreasing silicon donor concentration and increasing process bias. The passivation was restored after a heat treatment at 375 °C during 1 minute in a nitrogen ambient.
I-V measurements on Schottky diodes on n-GaAs were used to determine the ideality factor, saturation current and the barrier height. It was observed that these parameters slightly degraded with increasing substrate biases. The characteristics are nevertheless comparable to wet chemically etched diodes.
For AlGaAs/GaAs and AlGaAs/InGaAs/GaAs heterostructures the influence of removing the GaAs caplayer by the $CH_4/H_2/Ar$ ECR plasma process on the sheet density and the Hall mobility is investigated as a function of temperature, at different DC biases. Upon annealing full recovery of the sheet density was obtained whereas the mobility in the AlGaAs/GaAs heterostructure only recovered for 74%. This was compared to a wet etched reference Hall bar. An additional silicon δ-doped layer, introduced in the structure, behaved as a shield and prevented further introduction of damage. Nearly full recovery of the Hall mobility was obtained. For the AlGaAs/InGaAs/GaAs heterostructure no measurements could be performed after removing the GaAs toplayer at different DC biases and subsequent annealing. This suggests the introduction of an enhanced electron trapping mechanism or an interface degradation due to the plasma. Identical behaviour is observed during the fabrication of pseudomorphic HFETs. With an additional silicon δ-doped layer the best recovery is obtained after etching at a DC bias of -80 Volt. This in contrast to the AlGaAs/GaAs heterostructures where a minimal damage was observed at a DC bias of -40 Volt. The minimal damage for

both structures is observed at different process biases. This suggest that the extent of damage is also dependent on the epitaxial structure. It is believed that this optimum is created by minimising the plasma exposure time, which is obtained by increasing the substrate bias, and on the other hand, a reduction of this bias is necessary to reduce the amount of structural damage. Compared to identical experiments with CH_4/H_2 reactive ion etching on the same AlGaAs/GaAs heterostructures, improved results are obtained.

Chapter 5 describes the deposition of silicon oxide and silicon nitride films as a function of the process conditions. The composition of the films is measured by Rutherford Backscattering Spectrometry (RBS) using 4 MeV Helium ions. Simultaneously the hydrogen and nitrogen incorporation is measured by Elastic Recoil Detection Analysis (ERDA). Furthermore the refractive index, deposition rate and etch rate have been determined and compared to the results obtained with the compositional analysis. For both type of films near stoichiometric composition is obtained. The silicon oxide films show no compositional changes upon process variations. Variations in the refractive index are for this reason ascribed to deviations in the density of the layers. The hydrogen incorporation was typically between 1.4 and 1.9 at% at a deposition temperature of 300 °C. In contrast to silicon oxide silicon nitride showed a strong variation in composition with changes in process gases. With increasing silane flow the amount of silicon incorporation increased. The refractive index and the etch rate in buffered HF respectively increased and decreased with the silicon incorporation, which is comparable to observations in literature. The refractive index was below the value for stoichiometric silicon nitride which can probably be ascribed to the amount of hydrogen incorporation. The hydrogen incorporation in silicon nitride varied between 15 and 23 at%. The uniformity of silicon nitride and silicon oxide layer over a three inch wafer can be controlled reasonable although no explanation is found for the asymmetric non-uniformity of silicon oxide in contrast to the concentric one for silicon nitride.

Chapter 6 compares the results obtained on dry processed MESFETs and pseudomorphic HFETs with wet chemical processed transistors. For MESFETs a degradation in performance of the DC characteristics was observed. For the pseudomorphic HFETs however identical results in DC characteristics for the wet and dry processed transistors were obtained. The high frequency behaviour of the dry processed PMHFET was somewhat below the wet etched. This can probably be explained by the presence of an additional silicon oxide layer in the dry processed transistors. Also PMHFETs with an additional silicon δ-doped layer have been processed showing good DC and HF performances. The $CH_4/H_2/Ar$ ECR plasma process is for this reason suitable for transistor fabrication with good reproducibility.

7.2 Recommendations.

Although the results obtained on the dry processed pseudomorphic HFETs are very promising still further investigation is necessary to improve the quality of the processes and to obtain more physical information on the influence of plasma processing on different layer structures. For this reason some work is initiated and suggestions are made for further investigations.

1. The ion gun described in chapter 2 was not successful in improving the GaAs surface to obtain better Schottky contacts. Nevertheless it is useful to investigate the influence of an in-situ cleaning step on the contact resistance of n-type Ge/Ni/Au and p-type Ti/Pt/Au ohmic contacts. Both material systems are present in the Leybold evaporator. Due to the formation of an amorphous or disordered semiconductor surface by the ion bombardment a large number of interfacial states and traps in the bandgap will be introduced which facilitates the electron transport [1]. This especially holds for the formation of p-type contacts since generally it is more difficult to obtain very good contact resistances of this type with Ti/Pt/Au. Improvement of the contact resistance on n-GaAs Ni-AuGe-Ni contacts after sputter cleaning is already observed by others [2,3,4].

2. Concerning the $CH_4/H_2/Ar$ ECR plasma process much more investigation is necessary to obtain smooth surfaces on InP and also information involving the origin and type of physical damage to different epitaxial structures.

    - In case of InP the most important parameters to be optimised are the microwave power and the amount of methane used in the process. The methane, responsible for the removal of indium, can be increased since the 150 Watt process result in higher DC biases. This should be investigated in combination with the additional RF power used. Also the surface preparation, the type of mask and the amount of argon may have their influence on the results. Performing intermediate oxygen plasma's probably will also improve the smoothness and the sidewall roughness. More experiments in the RIE mode will give additional information in this area of research.

    - Much more information is required about the role of a silicon δ-doped layer in improving the epitaxial structures of HFETs. A silicon δ-doped layer in a uniformly doped layer can reveal if this layer act as a diffusion barrier for hydrogen incorporation. In C-V measurements a discontinuity will appear in the uniform carrier density. Photoluminescence spectra can give additional information about the depth of the damage if multiple quantum wells are used. Also information can be obtained on the effect of the plasma on the interface of a heterostructure.

3. Whereas silicon oxide showed a very stable composition and was easily to handle in further processing, the composition of silicon nitride changed remarkably as function of the process conditions. Silicon nitride films showed a reduced compatibility with further processing and annealing. This is probably due to the amount of stress present

in the silicon nitride layers. Because silicon nitride is preferably used as capping layer in transistor fabrication more research is necessary on the quality and especially on the stress developed in the silicon nitride films. An option to reduce the stress is to supply additional RF power to the substrate during deposition. Additional RF power will induce more damage to the layer, although a reduction of hydrogen incorporation is expected. Exposing the surface to an ion bombardment is often correlated to variations in the stress [5,6]. Claasen et al [6] obtained silicon nitride films with compressive stress which reduced with higher pressures, higher temperatures and higher frequency of the RF power. With the last two the stress even shifted from compressive to tensile. They ascribed the shift to a reduction in hydrogen incorporation due to higher temperatures and a change in the ion bombardment as function of the frequency. At higher temperature silicon nitride also is improved due to additional cross-linking.

4. In this work little attention was paid to the uniformity of the wet chemically etched transistors . A selective wet chemical etch was developed by Youcai Zhu [7] to have the possibility of selective etching a GaAs toplayer with respect to the AlGaAs donor layer in a heterostructure. The etch was based on a solution of citric acid and hydrogenperoxide (4:1). The citric acid was obtained by dissolving 100 gram citric solid ($C_6H_8O_7$) in 83 ml water. At room temperature a selectivity of 1 to 36 for $Al_{0.25}Ga_{0.75}As$ with respect to GaAs is obtained. The etch rates were respectively 10 nm/min and 0.36 µm/min. The selectivity and the etch rates are sufficient to accurately control the gate recess, although overetching will result in a large underetch. Beside this chemical solution it is useful to perform experiments on selective etching with the $CH_4/H_2/Ar$ ECR plasma by using an AlAs stop layer. In both circumstances however the epitaxial layer has to be defined very accurately.

   The characteristics of field effect transistors improve with the reduction of the gate length. After N.Moll et al. [8] a process was further developed by Anisha Kalfane [9] to reduce the size of the gate length, using optical lithography, and to make the process more compatible with the dry etching. The process is defined in figure 7.1. After evaporating and alloying the ohmic contact a silicon oxide layer is deposited over the whole structure. A 1 µm gate is defined and aluminium is evaporated under a certain angle. This aluminium serves as a mask during the etch of the silicon oxide film in the $SF_6/CHF_3/Ar$ ECR plasma. By varying the angle of evaporation the size of the gate can be defined as shown in figure 7.2. This mask system is more compatible with the $CH_4/H_2/Ar$ ECR plasma. The length of the gate could be defined very accurately and reproducible in this way. After gate recessing a TiW sputter deposition is necessary for the additional annealing step. This shadow evaporation also can be used in a direct lift off process to reduce the size of the gate.

5. Also more information is necessary on the damage created by the $SF_6/CHF_3/Ar$ ECR plasma required for dielectric etching. As a function of the bias voltage an optimum must be determined to reduce the damage. Since the plasma does not etch GaAs this can also be investigated as function of overetch time. It can be done in an identical way as the for $CH_4/H_2/Ar$ ECR plasma as described in chapter 4.

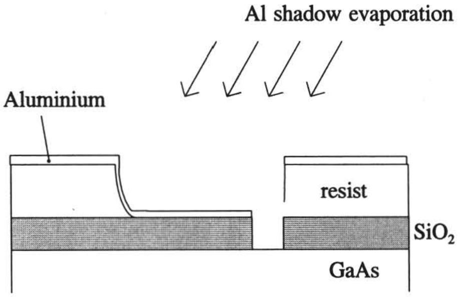
Al shadow evaporation
Aluminium
resist
SiO_2
GaAs

Figure 7.1, Schematic layout of the process which is more compatible with the $CH_4/H_2/Ar$ ECR process and with gives reduced gate lengths.

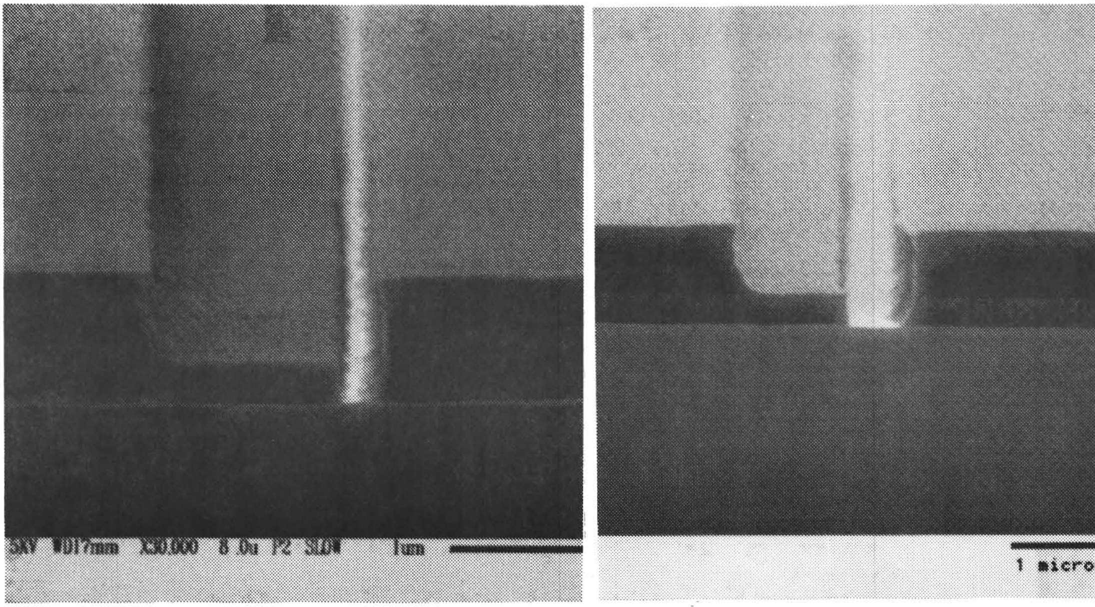
5kV WD17mm X30,000 8.0u P2 SLOW 1um
1 micro

Figure 7.2, The result of the process which can be used for reducing the gate lengths and is more compatible with the $CH_4/H_2/Ar$ ECR plasma.

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Appendix A

The processes used during the fabrication of GaAs-based field effect transistors and diodes are summarised in this appendix. The lithography is performed on a mask aligner (Karl Suss MJB 3) using UV 300 and UV 400 filters. Visual inspection is done with a Polyvar microscope.

Frequently used process steps

Cleaning step:
- Aceton dip for 1 min,
- Isopropanol dip for 1 min,
- Boiling chloroform 2 min,
- Hot plate 5 min. 105 °C.

Water rinse:
- Rinse for 20 sec in R.O. water,
- Rinse for 2 min in D.I. water,
- Nitrogen blow dry.

Lift off:
- Boiling aceton for 5 min,
- If necessary ultra sonic for a few minutes,
- Nitrogen blow dry.

Process technology for transistor fabrication

1. Mesa isolation etch:
   - Cleaning step,
   - Spinning of the resist AZ 5214, 5000 rpm, 30 sec,
   - Softbake 5 min 95 °C,
   - Exposure 5.5 sec, UV 400,
   - Development AZ developer:water 1:1, 20 °C, 1.5 min,
   - Water rinse,
   - Mesa etch in H_2SO_4:H_2O_2:H_2O solution (1:1:60) at 20 °C, 4 min, etchrate 75 nm / min,
   - Water rinse,
   - Resist strip in aceton,
   - Water rinse,
   - Visual inspection.
   - Mesa depth measurement with Tencor Alpha Step 200.

2. Ohmic contact formation:
   - Cleaning step,
   - Spinning of the resist AZ 5214, 5000 rpm, 30 sec,
   - Softbake 5 min 95 °C,
   - Flood exposure 1.5 sec, UV 300, without mask,
   - Postbake 3 min 105 °C,
   - Exposure 4.5 sec, UV 400,
   - Development AZ developer:water 1:1, 20 °C, 1.5 min, with stirring,
   - Water rinse,
   - Visual inspection,
   - Surface cleaning 30 sec in NH_4OH:H_2O solution (1:10) at 20 °C,
   - Ohmic contact evaporation in Leybold L560UV, Ge/Ni/Au (20/15/200 nm),
   - Lift off,
   - Cleaning step,
   - Visual inspection,
   - Annealing in rapid themal annealer 400 °C for 1 min in N_2:H_2 (2:1) ambient, See also appendix B,
   - Visual inspection,
   - Probe tester.

3. Gate formation:
   - Cleaning step,
   - Spinning of the resist AZ 1505, 5000 rpm, 30 sec,
   - Softbake 3.5 min 95 °C,
   - Exposure 4 sec, UV 400,
   - Development AZ developer:water 1:1, 20 °C, 30 sec,
   - Water rinse,
   - Gate recess in NH_4OH:H_2O_2:H_2O solution (1:1:150) at 20 °C, etchrate about 100 nm/min, intermediate control of the gate recess with the probe tester,
   - Water rinse,
   - Surface cleaning 30 sec in NH_4OH:H_2O solution (1:10) at 20 °C,
   - Evaporation of gate metallisation in Leybold L560UV, Ti/Pt/Au (50/20/200 nm),
   - Lift off,
   - Cleaning step,
   - Visual inspection,
   - Probe tester.

4. Overlay metallisation:
   - Cleaning step,
   - Spinning of the resist AZ 5214, 5000 rpm, 30 sec,
   - Softbake 5 min 95 °C,
   - Flood exposure 1.5 sec, UV 300, without mask,
   - Postbake 3 min 105 °C,
   - Exposure 5 sec, UV 400,
   - Development AZ developer:water 1:1, 20 °C, 1.5 min, with stirring,
   - Water rinse,
   - Visual inspection,
   - Surface cleaning 30 sec in NH_4OH:H_2O solution (1:10) at 20 °C,
   - Evaporation of overlay metallisation in Leybold L560UV, Ti/Pt/Au (50/20/200 nm),
   - Lift off,
   - Cleaning step,
   - Visual inspection,
   - Characterisation.

Appendix B

In this appendix a short description is given of the process used during annealing of the ohmic contacts. The process consist of 9 different steps as shown in figure a.

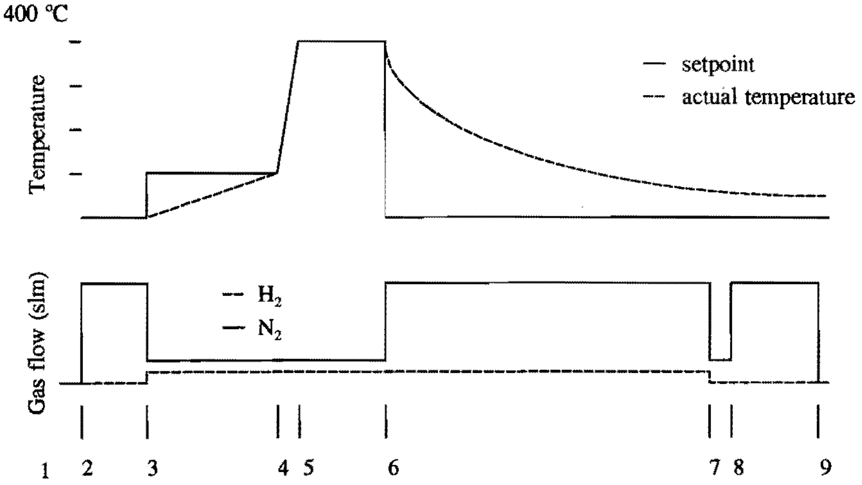

Figure a, Schematic overview of the process used during annealing of the ohmic contacts.

Annealing process:

1. Chamber evacuation 15 sec.
2. Nitrogen purge: 15 slm 30 sec.
3. N_2/H_2 preheat: setpoint 100 °C, N_2 flow = 1 slm and H_2 flow = 0.5 slm, 90 sec. This is a conditional step: if T = 100 °C within 90 sec then next step.
4. Rampup from 100 to 400 °C, N_2 flow = 1 slm and H_2 flow = 0.5 slm, 10 sec.
5. Stable at 400 °C, N_2 flow = 1 slm and H_2 flow = 0.5 slm, 60 sec.
6. Rampdown: setpoint 0 °C, N_2 flow = 1 slm and H_2 flow = 0.5 slm, 240 sec.
7. Evacuation 15 sec.
8. Purge: N_2 15 slm, 90 sec.
9. End 3 sec.

Summary

Field-effect transistors (FETs) are important devices for monolithic integration in opto-electronic circuits. Plasma processes are preferable in the fabrication of these transistors since they offer a better uniformity and reproducibility compared to a wet chemical technology. It is however desirable that damage introduced by these plasma processes will be minimal. Within the frame of this work different plasma etch- and deposition processes have been characterised and optimised. The influence of a few of these processes has been investigated on gallium-arsenide (GaAs) based Schottky diodes and field-effect transistors. For comparison wet chemically processed MEtal-Semiconductor Field-Effect Transistors (MESFETs), AlGaAs/GaAs and AlGaAs/InGaAs/GaAs (pseudomorphic) Heterostructure Field-Effect Transistors (HFETs) have been fabricated and characterised on wafer, using Direct Current (DC) and high frequency ($\leq$ 40 GHz) measurements. On wet chemically processed transistors these measurements showed good performances for 1 μm gate length transistors. The layer structures were grown by molecular beam epitaxy.

The influence of an in-situ argon cleaning step prior to the Schottky diode evaporation is studied by I-V measurements. The best results were obtained with a neutralised beam at an energy of 50 eV. Although improvement of the diode characteristics was expected only a marginal difference was observed compared to wet chemically cleaned diodes.

Electron Cyclotron Resonance (ECR) plasma etch processes using methane, hydrogen and argon are optimised for different III-V semiconductors. The influence of a number of process parameters, such as the gas flows and the RF power (DC bias), on the average etch rate is studied. The etch rates were sufficient to control accurately the gate recess.
In spite of the chemical nature of the process physical damage will be introduced. Beside the physical damage also passivation of the donor atoms occurs due to the presence of hydrogen in the plasma. By C-V measurements on Schottky diodes the passivation depth is investigated as a function of the initial donor concentration and as a function of the process bias. The passivation could be recovered by a heat treatment.
By I-V measurements on these diodes it was observed that the characteristics slightly degraded with increasing substrate bias but were nevertheless comparable to those of wet chemically processed diodes.
The influence of this plasma on the sheet density and the Hall mobility of a two-dimensional electron gas is studied as function of the process bias. For an AlGaAs/GaAs heterostructure the sheet density fully recovered whereas the Hall mobility only partially recovered after annealing. These measurements were done at a temperature of 5.6 Kelvin. The effect of the plasma on an AlGaAs/InGaAs/GaAs pseudomorphic heterostructure was deleterious. No measurements could be performed, even after annealing. Introduction of an additional silicon δ-doped layer in the structure behaved as a shield or buffer for the plasma and improved transport characteristics for both types of heterostructures were obtained. Compared to reactive

ion etching with a methane/hydrogen plasma also better results are obtained on the AlGaAs/GaAs heterostructures.

To successfully implement the ECR plasma process in the transistor fabrication it was necessary to use a silicon oxide or silicon nitride mask since thin resist layers were not resistant to the plasma exposure. For this reason and since little was known about the quality, compositional analysis is performed on these microwave downstream plasma enhanced chemical vapour deposition layers. This is done as function of process variations. The elemental composition is determined by Rutherford backscattering spectrometry whereas the hydrogen content is measured with elastic recoil detection. Furthermore the refractive index, the deposition rate and the etch rate in acid solutions is determined. Silicon oxide showed to be much more stable upon changes in the process conditions than silicon nitride whose composition and impurity incorporation strongly variated. Nevertheless for both types of layers process conditions have been found for near stoichiometric layers. For silicon oxide only a few atomic percent hydrogen was incorporated in contrast to the silicon nitride layers where the hydrogen content was about 20 percent. For technological reasons silicon oxide was chosen for the transistor fabrication.

Finally dry processed GaAs MESFETs and pseudomorphic HFETs are compared to wet chemically processed transistors. Whereas the dry processed MESFETs showed a degraded performance in the DC characteristics, the DC and high frequency characteristics of the pseudomorphic HFETs were comparable to those of wet chemically processed transistors. It can be concluded that the methane/hydrogen/argon ECR process is successfully implemented in the fabrication of field-effect transistors.

Samenvatting

Veldeffecttransistoren (FETs) zijn belangrijke bouwstenen bij monolithische integratie van opto-elektronische circuits. Plasma processen zijn gewenst bij de fabricage van dergelijke circuits en bouwstenen aangezien hiermee een betere uniformiteit en reproduceerbaarheid bereikt kan worden in vergelijking tot nat chemische processen. Van groot belang hierbij is dat de schade ten gevolge van deze plasma processen minimaal is. In het kader van dit werk zijn verscheidene plasma-ets en -depositie processen gekarakteriseerd en geoptimaliseerd. De invloed van een aantal van deze processen is bestudeerd op gallium-arseen (GaAs) gebaseerde Schottky diodes en transistoren. Als vergelijkend materiaal zijn nat-chemisch geëtste metaal-halfgeleider FETs, AlGaAs/GaAs en pseudomorphe AlGaAs/InGaAs/GaAs Heterostruktuur veldeffecttransistoren (HFETs) vervaardigd en zowel met behulp van DC en hoogfrequent metingen (< 40 GHz) gekarakteriseerd. Deze metingen toonden aan dat de eigenschappen van deze nat chemisch gefabriceerde transistoren met 1 µm gate lengte goed waren. De gebruikte lagen waren gegroeid met moleculaire bundel epitaxy.

De invloed van het in-situ schoonmaken met een argon ionen bundel van het GaAs oppervlak, voor het opdampen van een Schottky diode, is onderzocht met behulp van I-V metingen. De beste resultaten zijn behaald met een geneutraliseerde bundel bij de laagste energie van 50 eV. Deze zijn bereikt na een additionele temperatuurbehandeling. Hoewel er een verbetering van de diode karakteristieken werd verwacht ten gevolge van deze additionele stap was het verschil met een nat-chemisch schoongemaakte Schottky diode marginaal.

Elektron Cyclotron Resonantie (ECR) etsprocessen met een methaan/waterstof/argon plasma zijn geoptimaliseerd voor verscheidene III-V halfgeleider materialen. Hierbij is de invloed van verschillende proces parameters, zoals de gas toevoer en het RF vermogen (DC spanning) op de etssnelheid onderzocht. De verkregen etssnelheden zijn geschikt voor het uitvoeren van de gate ets.
Ondanks het chemische karakter van dit proces wordt er structurele schade geïntroduceerd. Daarnaast worden silicium donoren gepassiveerd ten gevolge van de aanwezigheid van waterstof in het plasma. De diepte van deze passivatie is bestudeerd als functie van de donor concentratie en de additionele proces spanning met behulp van C-V metingen. De passivatie kan echter hersteld worden door een temperatuurbehandeling. Stroom-spannings metingen toonden aan dat de diode karakteristieken langzaam verslechterden met toenemende proces spanning. Niettemin waren ze vergelijkbaar met die van nat chemisch gefabriceerde diodes. De invloed van het plasma op de elektronen concentratie en de Hall mobiliteit van een twee-dimensionaal elektronen gas is onderzocht als functie van de proces spanning. Voor een AlGaAs/GaAs heterostruktuur herstelde de elektronen concentratie zich geheel terwijl de Hall mobiliteit maar gedeeltelijk terugkwam na een temperatuurbehandeling. Deze metingen zijn uitgevoerd op een temperatuur van 5.6 Kelvin. Het plasma was funest voor een pseudomorphe AlGaAs/InGaAs/GaAs heterostruktuur. Zelfs na een temperatuurbehandeling konden geen

metingen worden uitgevoerd. Na het toevoegen van een additionele silicium δ-gedoteerde laag in de struktuur werden voor beide structuren betere resultaten verkregen. In vergelijking met reactief ionen etsen met een methaan/waterstof plasma zijn eveneens betere resultaten verkregen op een AlGaAs/GaAs heterostruktuur.

Om het bovenstaande proces succesvol te implementeren in de fabricage van veldeffecttransistoren was het noodzakelijk om een silicium-oxide of silicium nitride masker te gebruiken aangezien dunne laklagen niet bestand zijn tegen het plasma. Om deze reden en vanwege het feit dat er weinig bekend was over de kwaliteit van de lagen is de compositie hiervan onderzocht als functie van de verschillende proces parameters. De samenstelling van de plasma gedeponeerde silicium-oxide en -nitride lagen is onderzocht met behulp van "Rutherford backscattering spectrometry" terwijl de waterstof inhoud is bepaald met "elastic recoil detection". Verder is de brekingsindex, de depositiesnelheid en etssnelheid van deze lagen bepaald. De compositie van silicium oxide was erg stabiel in tegenstelling tot die van silicium nitride waarvan de samenstelling en de hoeveelheid ingebouwde verontreinigingen sterk varieerde bij variaties van de proces condities. Terwijl de waterstof inhoud van silicium oxide zeer gering was lag deze voor silicium nitride in de buurt van de 20 atoom procent. Voor beide lagen zijn echter proces condities gevonden die stoïchiometrische lagen opleverden. Om technologische redenen is silicium oxide gebruikt in de fabricage van veldeffectransistoren.

Tenslotte zijn de karakteristieken van plasma geëtste MESFETs en pseudomorphe veldeffecttransistoren vergeleken met die van nat chemisch vervaardigde transistoren. De MESFETs vertoonden slechtere DC karakteristieken, terwijl de DC en hoogfrequent eigenschappen van de pseudomorphe heterostruktuur veldeffecttransistoren gelijkwaardig waren aan die van nat geëtste transistoren. Hieruit kan worden geconcludeerd dat het ECR plasma proces succesvol is geïmplementeerd in de vervaardiging van veldeffecttransistoren.

List of symbols

Symbol	Comment	Unity
A	Thickness of the active layer	m
A^{**}	Richardson constant	$A/m^2/K^2$
A_d	Depletion width	m
B	Magnetic field strength	T
C	Capacitance	F
C_{ds}	Drain-source capacitance	F
C_{gd}	Gate-drain capacitance	F
C_{gs}	Gate-source capacitance	F
C_o	Zero voltage capacitance	F
d	Donor layer thickness	m
d_i	Spacer layer thickness	m
Δd	Distance between 2-DEG and interface	m
e	Electron charge	C
E	Longitudinal electric field	V/m
E_c	Critical electric field	V/m
ΔE_c	Conduction band gap difference	V
E_d	Activation energy	V
E_F	Fermi level energy	V
ΔE_g	Band gap potential difference	V
E_i	i^{th} subband energy	V
E_v	Valence bandgap difference	V
f_t	Cut off frequency	s^{-1}
f_{max}	Maximum frequency of oscillation	s^{-1}
g_m	Transconductance	S
g_d	Output conductance	S
$g_{m,max}$	Maximal transconductance	S
h	Planck constant	Js

I_{ds}	Drain-source current	A
$I_{ds,sat}$	Drain-source saturation current	A
I_g	Gate current	A
I_s	Diode leakage current	A
k	Boltzmann constant	J/K
L	gate length	m
L_c	Distance between ohmic contacts	m
L_d	Drain inductance	H
L_D	Debeye length	m
L_{ds}	Drain-source separation	m
L_g	Gate inductance	H
L_s	Source inductance	H
m	Electron mass	kg
MAG	Maximal available gain	dB
MSG	Maximal stable gain	dB
n	Ideality factor	
n^*	Local ideality factor	
N_d	Donor concentration	m^{-3}
n_i	ith subband electron concentration	m^{-2}
n_{ref}	Refractive index	
n_s	2-DEG sheet density	m^{-2}
n_{so}	Maximum 2-DEG density	m^{-2}
O	Area	m^2
q	Electron charge	C
R	Resistance	Ω
R_c	Contact resistance	Ω-m
R_d	Drain resistance	Ω
R_{ds}	Drain-source resistance	Ω
R_g	Gate resistance	Ω
r_H	Hall factor	
R_H	Hall coefficient	
R_{sh}	Sheet resistance	Ω
S_{11},S_{22}	Reflection coefficients	
S_{12},S_{21}	Transmission coefficients	
T	Temperature	K

v	Electron velocity	m/s
V	Channel potential	V
V_{bi}	Built-in voltage	V
V_{br}	Breakdown voltage	V
V_g	Gate voltage	V
V_{gs}	Gate-source voltage	V
V_{po}	Pinch off voltage	V
V_T	Threshold voltage	V
v_s	Saturation velocity	m/s
W	Gate width	m
W_{dep}	Depletion depth	m
ϵ	Dielectric permittivity	F/m
ϵ_o	Vacuum dielectric permittivity	F/m
ϵ_r	Relative dielectric constant	
μ	Hall mobility	m^2/Vs
μ_H	Electron mobility	m^2/Vs
σ	Conductivity	S/m
ϕ_b	Barrier height	V
ϕ_i	ith electron wave function	
ϕ_m	Metal potential	V
χ	Electron affinity	V
ω	Microwave excitation frequency	s^{-1}
ω_c	Cyclotron resonance frequency	s^{-1}
υ	Dissociation attempt frequency	s^{-1}

Other symbols are locally defined

CURRICULUM VITAE

Jan van Hassel was born on October 18, 1965 in Eindhoven the Netherlands.

He graduated in 1984 at the Anton van Duinkerkencollege (Atheneum) in Veldhoven.

In 1984 he started his study at the Delft University of Technology at the faculty of Technical Physics. In 1990 the academic degree was obtained in the division of Solid State Physics on the subject of weak links in YBaCuO films.

In January 1991 he started as a PhD student at the Eindhoven University of Technology in the division of Electronic devices of the Electronic Engineering department. He worked in the project on the fabrication of GaAs-based field-effect transistors necessary for opto-electronic circuits. He also participated actively in the start up and the maintenance of technological equipment of the III-V laboratory and in the development of processes.

Stellingen

behorende bij het proefschrift

Dry processing of GaAs-based MESFETs and pseudomorphic HFETs

door

Jan Gerard van Hassel

dinsdag 2 mei 1995

VII

Het is aanbevelingswaardig wegbedekking van Zeer Open Asfalt Beton (ZOAB) uit te rusten met verwarmingselementen.

VIII

Door het regelmatig falen van de moderne techniek in nieuwe systemen geïntroduceerd in het wegverkeer, is het noodzakelijk dat er tijdens de opleiding tot agent een hogere prioriteit wordt gegeven aan de verkeersregulatie.

IX

Het exploiteren van kassen ten bate van de softdrugsteelt door de overheid en het verplicht laten afnemen van deze produkten door coffeeshops vormt een effectief middel in de bestrijding van de illegale handel.

- *Volkskrant dd. 21 januari 1995 p. 1 & 17.*

X

Het invoeren van koffiejuffrouwen bevordert de werkgelegenheid en stimuleert de arbeidsproduktiviteit. In het kader van het emancipatiebeleid zouden juffrouwen hier ook zeer zeker vervangen kunnen worden door heren.

XI

De eenwording van Europa wordt al belemmerd door de grote verscheidenheid in eetgewoonten. Deze blijft hardnekkig voortbestaan ondanks de introductie van een grote diversiteit aan keukens uit verschillende culturen.

I

Om meer inzicht te verkrijgen in de schade toegebracht door plasma processen aan halfgeleiderstrukturen is het noodzakelijk fundamenteel inzicht te verkrijgen in de microscopische en structurele oorsprong van deze schade.

- *Hoofdstuk 4, dit proefschrift.*

II

Het gebruik van software ter ondersteuning van het verloop van een carrière is niet zinvol.

- *N.L.Mills and P.R. McCright, "Choosing the Ph.D. Path: A Multi-Criteria Model for Career Decisions." J. Engineering Education, Vol. 82 No. 2, pp. 109-117 (1993).*

III

De specifieke eigenschappen van bronwater dienen intensiever onderzocht te worden in nat-chemische etsprocessen.

- *S. Adachi, "Chemical Etching of (100)GaAs in volcanic Mineral Water." J. Elec. Soc., Vol 138 No. 12, pp. 3714-3716 (1991).*

IV

Semi-geautomatiseerde apparatuur in een technologisch laboratorium verhoogd de kans op toeval in de experimenten.

V

Cluster tool systemen kunnen zich alleen bewijzen indien alle deelprocessen uitvoerig en volledig gekarakteriseerd zijn.

VI

Hoewel er geen verklaring bestaat voor het feit dat de kans op een geslaagde borstkanker operatie afhankelijk is van het moment waarop geopereerd wordt en de menstruatie cyclus van een vrouw, dient dit meegewogen te worden in de bepaling van het moment waarop geopereerd wordt.

- *Volkskrant dd. 25 juni 1994 p. 17.*