Towards Spatial Multiplexing in Wireless Networks within Computing Packages

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ABSTRACT

Wireless Networks-on-Chip (WNoCs) are regarded as a disruptive alternative to conventional interconnection networks at the chip scale, yet limited by the relatively low aggregate bandwidth of such wireless networks. Hence, any method to increase the amount of concurrent channels in this scenario is of high value. In this direction, and since WNoC implies close integration of multiple antennas on a chip anyway, in this paper we present a feasibility study of compact monopole antenna arrays in a flip-chip environment at millimeter-wave and sub-terahertz frequencies. By means of a full-wave solver, we evaluate the feasibility to create, at will, concentrations of field in different spots of the chip. This way, we set the steps towards spatial multiplexing that enables concurrent multicast communications and also increases the aggregate bandwidth of the wireless network. Our results at 60 GHz show two clearly separable parallel channels that radiate simultaneously from two opposite corners of the chip, achieving a Signal-to-Interference Ratio (SIR) of around 40 dB, which proves that the channels are independent of each other even in such an enclosed environment. Further, we see potential to expand our approach to three or more concurrent channels, and to frequencies beyond 100 GHz.

CCS CONCEPTS

• **Hardware → Radio frequency and wireless interconnect**.

KEYWORDS

Wireless Network-on-Chip; Flip-chip; Antenna Arrays; Spatial multiplexing; Beamforming

1 INTRODUCTION

The Network-on-Chip (NoC) paradigm and, more recently, its analogous Network-in-Package (NiP) have become the de facto standard for the interconnection of cores in multicore processors. However, as we enter the hyperscaling era [21], the communication requirements increase up to a point where conventional NoCs and NiPs alone may not suffice. Their limited scalability is in fact turning communication into the performance bottleneck of manycore systems, thus calling for new solutions at the interconnect level [7, 12].

Advances in integrated antennas and transceivers have led to the proposal of Wireless Network-on-Chip (WNoC) as a complement of or alternative to existing NoCs. WNoCs basically consist of the co-integration of RF front-ends with cores or clusters of cores [15]. Radio waves propagate through the package at nearly the speed of light until reaching the intended destinations, also located within the same package, as shown in Figure 1. At the receivers, signals are then demodulated and deserialized [22]. Since intermediate router hops are avoided, WNoC reduces the latency of long-range and broadcast communications by an order of magnitude. On the downside, wireless bandwidth is limited and needs to be shared among the cores. As a result, Medium Access Control (MAC) protocols or multiplexing methods are required to avoid collisions and interference in the WNoC. However, this approach has important limitations because the number of non-overlapping frequency, code, or time slotted channels achievable in this resource-constrained scenario is relatively small [3, 14]. A large number of channels increases the complexity of hardware in frequency multiplexing or synchronization components in code multiplexing.

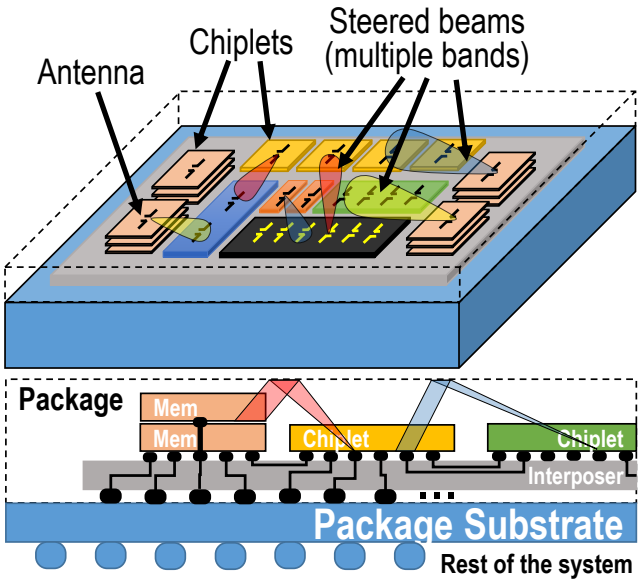

Figure 1: Schematic diagram of a System-in-Package (SiP) hosting a heterogeneous set of chiplets. The interconnect fabric is composed of a silicon interposer Network-in-Package (NiP) augmented, as proposed in this paper, with multiple concurrent spatial wireless links.

An alternative or complement to the multiplexing schemes mentioned above would be spatial multiplexing as proposed in the authors' prior work [1] and pictorially represented in Figure 1. Although the creation of multiple concurrent spatial channels comes with a loss of the broadcast nature of wireless communications, which is very much appreciated by computer architects [11], there are several applications that require multicast and can still benefit from having multiple spatial channels [2]. In any case, such an approach requires the use of antennas with a relatively large aperture, which may be complex to integrate with on-chip environments.

Indeed, to implement the on-chip array, the flip-chip package does not leave much space for the antennas. Due to the presence of solder bumps, antennas cannot be implemented in the first metal layer [24]. Alternatively, designers have to use the metal layers closer to the silicon, where patch antennas and printed dipoles might be implemented. However, the proximity to the virtual ground plane formed by the array of micro-bumps reduces their efficiency, whereas co-planarity between antennas further increases losses; also, as we are in heavily area constrained scenario one must be cautious with the use of available space [23]. Finally, as proposed recently, one could fabricate Through-Silicon Via (TSV) to implement vertical monopoles [19, 23], an approach followed by us. Due to the stringent area constraints of the scenario, directional antennas and MIMO arrays are generally prohibitive [22].

Even so, for the evaluation of feasibility of MIMO channels and near field communications, a statistical characterization of a 2×2 MIMO wireless link operated in a mode-stirred cavity is carried out in [16]. The authors obtained two parallel channels within the confined space for different conditions of the mode-stirred enclosure. They provide a characterization of a complex MIMO channel in highly reflective propagation environments.

In [20], the possibility of improving the performance of wireless RF interconnect in the near field is studied. The paper presents a design to get multi-channel communications between antennas in their mutual near field. This approach is useful for applications such as on-chip and chip-to-chip wireless communications.

Further, to increase communication distance and capacity in the THz band, the concept of Ultra-Massive MIMO is introduced in [4]. The authors propose the design of graphene-based plasmonic nano-antenna arrays composed of thousands of elements comprised in a few square millimiters. They contemplate reception, transmission, beamforming, spatial multiplexing and multi-band communication schemes as applications for the resulting array. Although the previously mentioned papers provide points to consider in our work, the proposed arrays and MIMO characterizations done by them do not precisely occur in a chip environment.

In [5, 6], a four element array for beam switching in chip-to-chip communications in a multi-chip system at 60 GHz is proposed. Pattern changes are achieved by switching the elements on and off. However, their package scenario is different than the one we use. Narde *et al.* [17, 18] evaluates the beamforming and transmission capabilities of on-chip arrays for intra-chip and inter-chip communications in multi-chip systems. They use a four zigzag antenna element phased array at 60GHz to study static beamsteering in specific directions. In their simulations, they arranged the four elements with a spacing of 0.75 mm which might imply problems with the use of available space in the chip. Moreover, the array is not reconfigurable. The previously cited papers mainly contemplate planar antennas in a chip environment different from the one we use and that we will describe in the next section.

In this paper, we attempt to create spatial channels or field distributions concentrated in different parts of the chip, by building 4×4 monopole antenna arrays in a flip-chip package and exploring different phase distributions. Hence, our strategy relies on having reconfiguration abilities at the transmitter and receiver antennas, which is in contrast to recent proposals using near-passive programmable reflectarrays at the boundaries of the environment to somehow re-structure the reverberant behavior of the channel (an idea proposed for indoor communications [9] and recently ported to the on-chip domain [13]).

In our proposed approach, we take advantage of the high permittivity of the bulk silicon layer used in the chip to create compact arrays with vertical monopoles. Also, the silicon high losses prove to be useful to attenuate waves that can interfere in adjacent channels and to place antennas close together without much coupling. Towards that goal, we conducted simulations to assess the appropriate distance among the antennas of the array and achieved compact 4×4 arrays at 60 GHz approximately 1 mm^2 and less than -10 dB coupling among adjacent antennas. Further, with the adjusting of excitation phases, we got two parallel channels, which we demonstrated along two different directions within the computing package. The antenna arrays radiate simultaneously with little interference with each other, achieving a very large Signal-to-Interference Ratio (SIR) of around 40 dB. Moreover, the results seem to be extendable to more channels and more frequency bands, as we show.

The remainder of this paper is organized as follows. In Section 2, we describe the simulation methodology and the antennas used in this work. In Section 3, we explain the criteria followed to design of the array and show the results obtained via full-wave simulations. Section 4 outlines the post-processing steps carried out to evaluate spatial multiplexing. In Section 5, the paper is concluded.

2 BACKGROUND

Here, we first depict the simulation environment in Section 2.1, to then describe the steps followed to design the vertical monopole that serves as the basis of our arrays in Section 2.2.

2.1 Environment Description

The environment structure is a flip-chip package as shown in Figure 2. In this configuration, the chips are turned over and connected to the system substrate through a set of solder bumps. The packaged chip therefore has the silicon substrate on top, which is in turn interfaced by the spreader material and system heat sink on top. The insulator and metal stack are placed at the bottom, interfaced by the solder bumps that connect it to the system [10, 23].

The layers are described from top to bottom as summarized in Table 1. On top the heat spreader, modeled as Aluminum Nitride, dissipates the heat out of the silicon since it has good thermal conductivity; with ε_r=8.6 and ρ=0.0003. The insulator is silicon dioxide with ε_r=3.9 and ρ=0.025. The silicon die, made of bulk silicon, serves as the foundation of the transistors. This layer has ε_r=11.9 and low resistivity (10 Ω·cm), which is convenient for the operation of transistors, but not for electromagnetic propagation

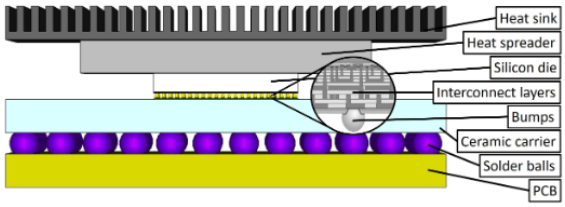

Figure 2: Schematic of the layers of a flip-chip package.

Table 1: Package parameters.

Parameter	Thickness	Materials	Units
Heat Spreader	0.5	Aluminum Nitride	mm
Silicon die	0.5	Bulk Silicon	mm
Lateral Space	0.5	Vacuum	mm
Chiplet insulator	0.01	SiO2	mm
Bumps	0.0875	Copper	mm
Frequency	60	-	GHz

since it attenuates the signal. Finally, we simulate the interconnects and the bumps as one solid layer of copper [23]. Our chip has a size of 10x10 mm^2 and is to be studied at a frequency of 60 GHz in a full-wave solver. The solver allows us to perform phase sweeps on the excitation of each antenna of the array, obtain the S-parameters to assess the coupling between antennas and to study the field distribution for those phase changes. Our choice of solver for this work is CST Microwave Studio [8].

2.2 Single Antenna Design

Due to its good *a priori* lateral coupling and opportunistic compatibility with conventional chip pacakge designs, we have chosen a vertical monopole antenna as baseline for our study. The monopole antenna is modeled as a thin and long cylindrical metallic structure, placed vertically passing through the silicon and fed from the first metal layers. Practically, this can be implemented by fabricating TSVs that emerge from the metallization layers and prematurely stopping the fabrication before reaching the heat spreader. Since the bumps layer is seen as a solid metallic block of metal at 60 GHz, due to the small bump pitch, this layer acts as a sort of ground plane for the monopole, increasing the effective antenna length due to image theory [23]. Hence, we initially set the monopole length L to

$$L = \frac{\lambda}{4} = \frac{v_p}{4 \cdot f} = \frac{c_0}{4 \cdot \sqrt{\varepsilon_{Si}} \cdot f} \quad (1)$$

where c_0 is the speed of light, $f = 60$ GHz is the target frequency, and ε_{Si} is the permittivity of silicon in that frequency region.

While the monopole fits entirely within the silicon layer, its proximity to the interface with the heat spreader material with a different permittivity may lead to a shift in the resonance. Taking this into account, to adjust the dimensions of our antenna we first model a simple scenario with a quarter-wave monopole sized using Equation (1). Afterwards we introduced the monopole in the chip environment and we fine-tuned the length to get a good reflection coefficient close to 60 GHz. Figure 3 shows the reflection coefficient of the monopole working at 60 GHz in the flip-chip environment.

Figure 4 shows two monopoles placed diagonally on the chip and radiating at the same time. Some phase sweeps were made to

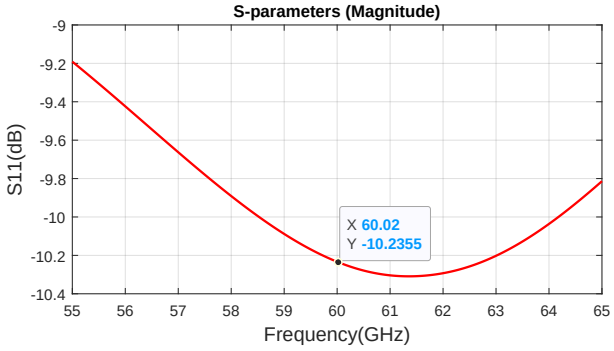

Figure 3: S11 of the monopole within a flip-chip environment.

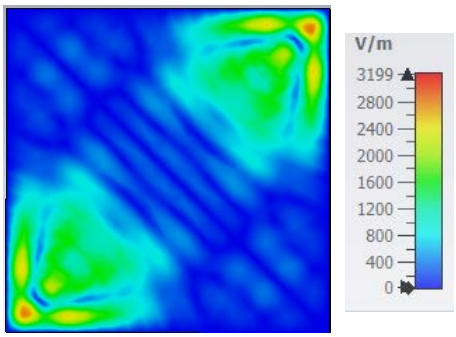

Figure 4: Electric field generated by two monopole antennas placed in opposite corners and transmitting at the same time.

the antennas excitation to attempt to create a sort of *beam* or field concentration in any part of the chip. However, as expected, none of the sweeps yield any controllability or appreciable differences in the field concentration for that matter. In fact, the beam-like distribution pointing to the center of the chip is due to the proximity of vertical walls at the lateral limits of the chip. Therefore, to be able to direct the beam or create concentration of energy in any part of the chip, we will need to use antenna arrays.

3 ANTENNA ARRAYS WITHIN A COMPUTING PACKAGE

3.1 Mutual Coupling

To get a better grasp of the behavior of the antennas in the flip-chip package, the scenario was simplified. Tests were made with only upper and lower boundaries of the chip, without any lateral vacuum spacers. We also experimented with distance between antennas, number of elements and their position on the chip to get to our final design. We will be using monopoles with a length of 0.475 mm and a radius of 0.005 mm, as discussed in Section 2.

Although the bulk silicon permittivity allows us to create a compact array, we need to make sure that the distance between elements will not lead to losses due to mutual coupling. Such a coupling issue was studied placing two monopoles in the corner of the chip forming a small array, then exciting them with the same phase at

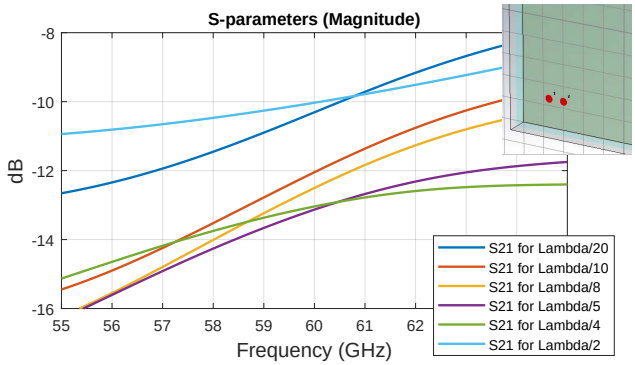

Figure 5: Landscape used for the coupling assessment and results at different distances between two antennas.

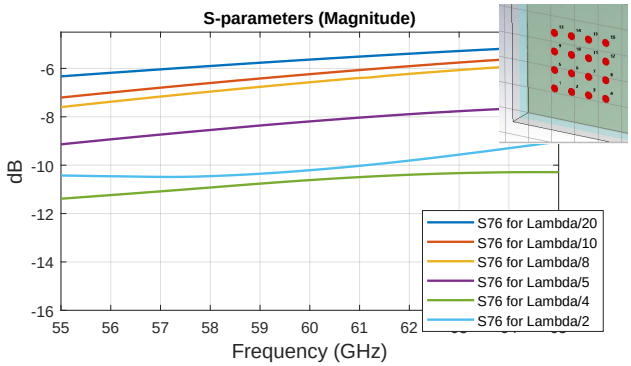

Figure 6: Landscape of the array and test coupling results for different distances among the elements.

the same time, and finally monitoring the S-parameters to evaluate the coupling in each case. We simulate $\lambda/20$, $\lambda/10$, $\lambda/8$, $\lambda/5$, $\lambda/4$ and $\lambda/2$ where $\lambda = \frac{c_0}{\sqrt{\varepsilon_{Si}} \cdot f}$ is the wavelength in silicon.

Figure 5 presents the distance dependency for the S-parameters and demonstrates that even for minimum distances between elements the coupling seems to remain very low; so we should be able to form arrays with short distances among antennas. However, because we are aiming for an array, we test the coupling issue at the mentioned distances for a 16-element array configured in a 4×4 manner. Then, we use two antennas in the center of the array to check the accumulated influence of the surrounding elements. In our configuration, these were antennas 6 and 7. In Figure 6 we observe the harmful effects of adding more antennas and lowering the distance among them, leading to an inter-element coupling worse than -10 dB when the distance is smaller than $\lambda/4$.

In the tests carried out, when using distances like $\lambda/2$, we obtained interesting field concentrations plots. However, as we are working on the chip scale, one must be cautious with the use of available space. Also, some phase combinations that prove to create a clear *beam* for smaller distances, at $\lambda/2$ start to lose shape. For the smallest distances, namely $\lambda/20$, $\lambda/10$, $\lambda/8$, although we can create and direct the beam using a correct combination of excitation phases, we face with the undesired coupling issue. For $\lambda/20$, in addition to the coupling effects, fabricating TSVs with the required pitch is difficult and expensive. With these results, the best compromise is to explore the energy concentration with a 16-element array with distances of $\lambda/4$ among each other. As a result, the evaluated array occupies a chip area of approximately 1.18 mm^2; which represents 1.18% of the 100 mm^2 chip and even less in larger dies.

3.2 Field Distribution

Finding a combination of phases for the array that give us a clear beam and certain controllability is complex in this scenario. Instead of using an analytic approach we use the post-processing combine results tool offered by CST, to get changes in the energy patterns. This means that after we run the simulation of our environment, we applied a macro that made a sweep of excitation phases re-using and combining the fields provided by the solver's field monitor at 60 GHz. This method allows us to obtain more results in less time, to experiment with different phase changes dynamically and without much computational cost. Such an approximation is valid since the

Table 2: Phase values leading to the field shown in Figure 7.

Vertical Beam								
Port	1	2	3	4	5	6	7	8
Phase	90	120	150	180	0	30	60	90
Port	9	10	11	12	13	14	15	16
Phase	-90	-60	-30	0	-180	-150	-120	-90
Horizontal Beam								
Port	1	2	3	4	5	6	7	8
Phase	0	-330	-300	-270	-150	-120	-90	-60
Port	9	10	11	12	13	14	15	16
Phase	60	90	120	150	270	300	330	0

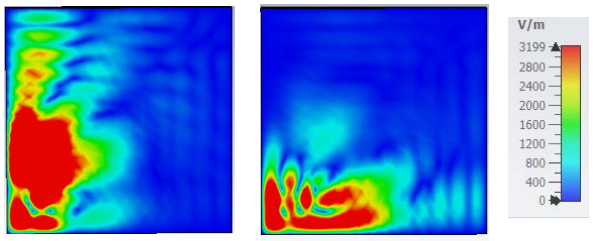

Figure 7: Field distributions of a phased array with configurations to steer the field along (a) the Y axis and (b) the X axis of the coordinate system.

coupling among the different elements is below -10 dB, as we have shown in Figure 6. Also, we made a smaller environment with one monopole. Using array theory and the array factor tool offered by CST, we manipulated the radiation pattern of the antenna creating a virtual array and the best results were used to compose the beams in the flip chip scenario. We gradually increased the difficulty of the simulations. First stimulating a single element and adding more as we became acquainted with the changes that certain phases caused in its field pattern until we reached the array of 16 elements.

Table 2 shows a summary of the final excitation phases used on each antenna to obtain parallel channels. In Figure 7, we see the results of such a phase profile combination. The 4×4 array (array 1) is placed on the bottom left corner of the chip and radiates towards its opposite corners with a clear and well shaped beam.

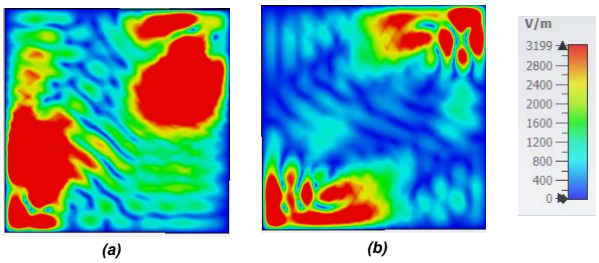

Figure 8: Field distributions of two phased arrays with configurations to steer the field towards the opposite corner along (a) the Y axis and (b) the X axis of the coordinate system.

Our next step is to come up with a combination that holds two parallel channels radiating at the same time without interfering with each other. To do this, we place an identical array in the upper right corner (array 2), we perform a phase sweep procedure as described above. This sweep is based on the results obtained with the array factor in the one monopole scenario.

Figure 8 presents the results of our simulations. At first sight it seems that we manage to create two parallel concentrations of energy that radiate at the same time, in principle without interfering with each other. This already proves one of our main goals, which was to create beams inside a chip using antenna arrays.

4 EVALUATION OF IN-PACKAGE SPATIAL CHANNELS

To verify that the channels obtained in the previous section radiate as independently as they appear to do, another post-processing step is performed by using the resulting fields of the phase manipulation. In Section 4.1, we outline the method and assess our basline case of two channels at 60 GHz. Then, we show the results of scaling the system to 110 GHz in Section 4.2 and of scaling the number of intended spatial channels to at least three in Section 4.3.

4.1 Baseline: Two Spatial Channels at 60 GHz

The post-processing made to further validate the beams along the Y axis is seen in Figure 9a. We take the field created when only the array on the bottom left corner (array 1) radiates and subtract from it the field produced when both arrays radiate. This gives us the level of interference on array 1 when array 2 radiates. From the image, it is observed that the space where array 1 dominates is clearly along its Y axis, with bright colors, whereas the other side of the chip clearly shows dominance from array 2. Overall, both channels are separated by way more than 20 dB of interference, hence they are isolated from each other. The SIR gives us a measure of the reliability of the channel in this case. From the image we see that the radiation from array 1 arrives to the intended opposite corner with a SIR of more than 40 dB, meaning that the interference level is very low when both arrays radiate simultaneously.

4.2 Scaling the Frequency

In the WNoC use case, it is desirable to achieve diversity both on frequency and space for multi-channel communications. For this, we contemplate to open spatial channels in frequencies other than 60 GHz. To evaluate this, we assume the same landscape and antennas at 60 GHz and simulate it at 110 GHz to consider that the monopole is working close to a harmonic of the original 60 GHz tone. In our simulations, the S11 parameter of the monopole drops to -10.3dB, but still it can be considered that monopole resonates so we can use it for our purposes. Figure 9b shows the interference field and the SIR relationship of the scenario at hand, but at 110 GHz. For this frequency, we also achieved two well-defined independent channels, hence opening the door to joint space-frequency multiplexing to maximize the channel creation within the package.

4.3 Scaling the Number of Channels

Next, we simulate the case of the arrays being placed closer to each other to see whether the scenario is compatible with more than two parallel spatial channels. In the new scenario, instead of two arrays on diagonal opposite corners of the chip, there is an array on the bottom left corner (array 1) and the other placed laterally and closer to the first one, as shown in Figure 10.

In this configuration, also two horizontal parallel channels seem plausible, yet with the interference taking a slightly different shape than in previous evaluations. Here, we see that array 1 (bottom-left corner) also produces interference along the Y-axis which hinders the error-free transmission from array 2. However, the achievement of good SIR even if the arrays are now closer is of high relevance in this scenario, because it could enable the integration of a third spatial channel in this hypothetical scenario.

5 CONCLUSION

In this paper, we made an analysis of the integration of a monopole antennas in an enclosed package to achieve concurrent multicast channels, which can be reconfigured by changing the excitation phases of the antenna elements. Understanding that it is not possible to direct and control the electromagnetic field by changing the phase of a single monopole, we considered antenna arrays. A review of the coupling issue among nearby antennas was performed to understand the tradeoff between undesired element coupling and compactness of the array. The first take away of our research is the confirmation of our ability to create, direct and somehow control the field distribution inside the chip with compact arrays of 1.18 mm^2 at 60 GHz. Albeit considering a few idealities, especially in the phase shift of the excitation, we have shown that two and even three simultaneously radiating channels can be created with good values of SIR (beyond 20 dB). We approach to the possibility of scaling in frequency and in number of channel with some success, which opens the way towards spatial multiplexing and frequency diversity of the channels in on-chip environments.

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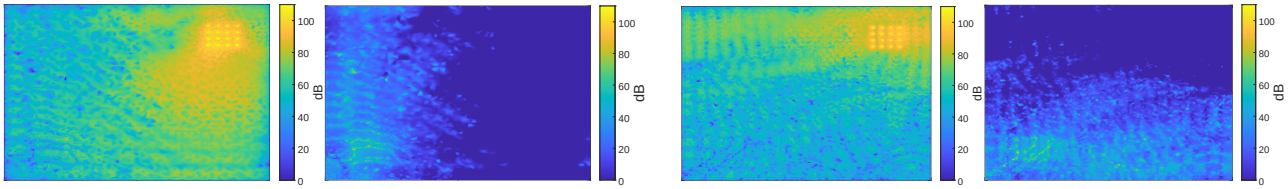
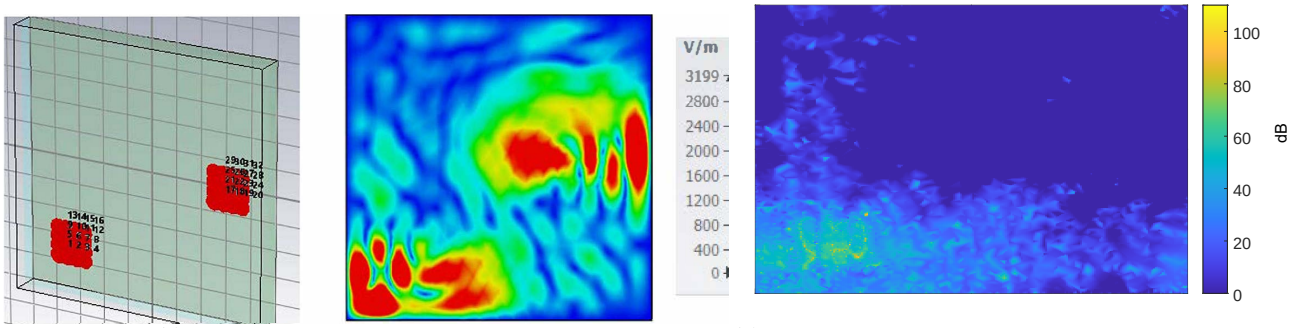


(a) Multiple channels along the X axis at 60 GHz. (b) Multiple channels along the Y axis at 110 GHz.

Figure 9: Interference field (left) and Signal-to-Interference Ratio (SIR, right) in two different cases.



(a) Array positions and field distribution. (b) Signal-to-Interference Ratio from the bottom-left array.

Figure 10: Evaluation of an array system with nearby and potentially interferent arrays compatible with three spatial channels.

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