AC Fault Ride Through in MMC-based HVDC Systems

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***Abstract*—VSC-HVDC systems are being increasingly employed in the power systems. The recently installed HVDC systems have a power capacity similar to traditional power plants. Hence, they are expected to have a similar behaviour as traditional synchronous generators during faults in AC grid, within their limits of course. Recent grid codes require HVDC converter stations to incorporate fault ride-through (FRT) capabilities in order to avoid HVDC converter station disconnection from AC grid for certain fault characteristics. In this paper, two FRT mechanisms are suggested for the two converter stations of an HVDC system. One FRT mechanism is added to the DC voltage control loop of the master converter station, while the other FRT mechanism is added to the active power control loop of the slave converter station. The objective is to ensure the stable operation of the HVDC system during faults that may occur in AC grids located on both sides of the HVDC system. The performance and stability of the suggested FRT mechanisms are tested considering the pre-fault power flow direction and all possible types of balanced and unbalanced faults. Simulation results confirm the effectiveness of the FRT mechanisms and revealed the critical modes during FRT operation.**

***Index Terms*—HVDC, MMC, faults, fault ride through, stability.**

I. Introduction

High voltage direct current (HVDC) transmission system based on modular multilevel converter (MMC) technology is the preferred solution for interconnection of distant power systems with overhead lines or submarine/underground cables. This can be applied to non-synchronous systems interconnection (with the same or different frequency), embedded transmission system in an AC grid, or connection of remote loads or generation plants [1]. This study is specifically focused on the application of HVDC link for interconnection of two AC grids. Such interconnector consists of two converter stations (referred to as MMC 1 and MMC 2 in this work) which interconnects two AC grids (referred to as grid 1 and grid 2) via HVDC cable.

On the grid fault occurrence, a severe voltage dip appears at the point of common connection (PCC) between the faulty AC grid and MMC terminals. This sudden reduction in AC voltage causes a sudden drop in the output power of the MMC. While one MMC is unable to exchange power with the faulty AC grid, the other MMC located on the other side of the HVDC link continues to exchange power with the AC grid, which leads to a power imbalance in the HVDC link [2]. Depending on the pre-fault power direction (from MMC 1 to MMC 2, or reverse) and the location of the fault (grid 1 or grid 2), the capacitance of the DC cable is continuously charged or discharged, leading to the rise or drop of DC voltage to an unacceptable level if it is not properly controlled during the fault. This puts additional stress on the HVDC equipment and may lead to the premature disconnection of the converter station from AC grid due to protection devices tripping [3]. Recent grid codes require HVDC converter station to stay connected to the grid and continue stable operation in such PCC voltage conditions to secure the best possible grid support. This objective is fulfilled via fault ride-through (FRT) capabilities of HVDC converter station [4].

Various FRT methods have been suggested to maintain DC voltage within permissible range during grid faults. The majority of them, however, deal with the offshore wind integration in which a fault occurs on the onshore AC grid and the surplus power coming from offshore wind farm causes a DC over voltage. Based on how this surplus power is handled, the FRT methods can be classified as follows:

(i) *Dissipation*: in this method, the surplus power during short period of fault is dissipated in a full-scale DC chopper with a resistive load that is installed on the DC link [5], [6].
(ii) *Storage*: the surplus power is transformed into kinetic energy and stored in the wind turbine rotor (if available) [7], or in a dedicated flywheel [8].
(iii) *Power reduction*: the surplus power in HVDC link is reduced via:
  (a) power curtailment of individual offshore wind turbines during onshore fault [9],
  (b) reducing the AC voltage of the wind farm by the offshore MMC [10],
  (c) increasing the frequency of AC voltage by the offshore MMC, which in turn, causes reduction in wind farm power [11].

However, the case of two AC grids interconnection is particularly different from wind integration application for the purpose of FRT design, since the fault may occur in either AC grid 1 or 2, and the pre-fault power flow direction can be positive or negative. Hence, both DC under and over voltage may appear in the DC link. Note that, while DC over voltage has impact on the insulation level of HVDC equipment and converter components, DC under voltage can lead to modulation issues [1], [3]. Moreover, the overall dynamics of the HVDC system are affected differently by the faults in AC grid 1 and AC grid 2, since the control modes of

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MMCs 1 and 2 are different. Typically, master MMC (called here MMC 1) operates in DC voltage regulation, while slave MMC (called here MMC 2) controls the active power flow [12]. Thus, different FRT mechanisms are needed for two MMCs to stabilize DC voltage during fault.

Focusing on the application of two AC grids interconnection, some of the suggested FRT approaches rely on a communication link. Such as the study conducted in [13], where the active power setpoint of the slave converter station is a function of the measured PCC voltages of both sides of HVDC link. As a result, the generated active power reference is automatically reduced in case of a voltage dip occurrence on the either sides of the HVDC link. Commonly, with the adoption of a communication network, a good DC voltage performance can be achieved, but additional investment is needed and there is a potential risk of communication failure. Another class of FRT approaches is based on the simple fact that the role of DC voltage regulation can be temporarily switched between master and slave stations. These approaches require minimal or no communication between two converter stations. In this regard, the concept of *voltage margin control* has been introduced in [14]. Once the master converter station can no longer maintain DC voltage within the given margins due to disturbances in AC grid, the slave converter station detects the DC voltage abnormal condition and switch from active power control to DC voltage control until the system is back to the normal operation. This concept has been further developed for a multiterminal HVDC grid in [15], [16]. Both studies share the same idea of using two PI controllers in the slave converter station: one for DC voltage regulation, the other for power regulation, and the switching between these two PI controllers depends on the defined DC voltage margin. In [3], the slow dynamics of the voltage margin control, which is due to the time delay from the detection of the DC voltage deviation in the master converter to the control action taken by the slave converter, is addressed. The DC power cable is used for obtaining an indirect communication between two converter stations. The DC voltage reference of the master station is decreased on the fault occurrence in order to inform the slave station about the abnormal situation. So, slave station will reduce the active power rapidly to avoid DC over voltage. As a modification to the voltage margin control with PI controller, DC voltage droop control has been discussed in [17], where a droop controller is used for DC voltage regulation during fault.

However, the majority of studies in this filed only discuss the static terminal behaviours of master and slave converter stations without offering a detailed engineering solution to realize them, which commonly involves the timings and detailed procedure of switching between normal operation and FRT operation. This is particularly important since the transition from normal operation to FRT operation has to be carried out in few tens of milliseconds before DC voltage rises/drops to an unacceptable value.

DC voltage regulation during the fault is not the only concern in an MMC-based HVDC system. Unlike two-level voltage source converter, an MMC requires an additional control action for internal energy balancing to assure stability of HVDC system [18], [19]. In particular, the capacitor voltages of the upper and lower arms may become unbalance during asymmetrical faults, which leads to internal energy imbalance of the MMC [20], [21]. Therefore, during AC grid fault, not only DC link voltage has to be regulated, but also the internal energy of both MMCs have to be kept balanced.

In this paper, the aforementioned challenges are addressed via two FRT mechanisms. One is employed in the DC voltage control loop of MMC 1, and the other is used in the active power loop of MMC 2. The suggested FRT mechanisms do not require a DC chopper or a long-distance communication link. They only rely on the local measurements of the DC and AC voltages to ensure a stable operation of the HVDC system and an adequate performance of the DC voltage and internal energy of the MMCs during multiple grid fault scenarios. In particular, the effectiveness of the suggested FRT mechanisms is investigated for 28 possible fault scenarios that are categorized as the fault types (symmetrical and asymmetrical), fault locations (AC grid 1 and 2), and pre-fault power flow direction (positive and negative).

II. Fault Ride Through Requirement

In this section, the requirements for FRT capabilities of HVDC converter stations provided by the EU ENTSO-E grid code (see [4]) are briefly discussed.

The voltage-time profile at the PCC during fault conditions is shown in Fig. 1. Under the conditions given by the dark gray region, the HVDC converter station shall be capable of staying connected to the AC grid, remaining in a stable operation after the power system has recovered following fault clearance. If the PCC voltage (v_{pcc}) enters the light gray region, the HVDC converter station is allowed to be disconnected (activation of the under-voltage protection) from the AC grid. It is assumed that the fault occurs at time zero, and it is cleared at t_{clear}. The retained PCC voltage during fault is given by U_{ret}. The pairs of parameters (t_{rec1}, U_{rec1}) and (t_{rec2}, U_{rec2}) indicate the lower limits of the voltage recovery following the fault clearance.

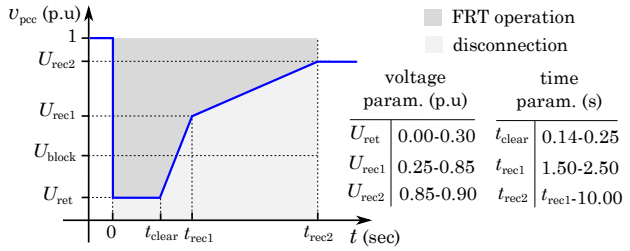

Fig. 1. Voltage profile at PCC during fault based on ENTSO-E grid code

Each Transmission System Operator (TSO) determines whether active power contribution or reactive power contribution shall have priority during FRT operation. In case of the reactive power contribution, it is achieved via regulating the reactive component of the grid current reference (i_s^{d*}). As shown in Fig. 2, during normal operation in which v_{pcc} is within the deadband from U_{min} to U_{max}, i_s^{d*} is based on the default setpoint of reactive power (normal conditions). However, once v_{pcc} falls below U_{min}, i_s^{d*} is increased proportionally to the

magnitude of v_{pcc}. For the voltage level from 110 kV up to 300 kV, the deadband is defined for [0.85 1.18] p.u, and for the voltage level from 300 kV up to 400 kV, it is defined for [0.85 1.05] p.u of the nominal AC voltage. Once v_{pcc} goes lower than 0.85 p.u, fault condition is detected and the FRT operation is activated. Subsequently, reactive current, proportional to the magnitude of v_{pcc}, is injected into the AC grid. Meanwhile, the active current reference (i_s^{q*}) has to be decreased to avoid overcurrent condition. In fact, converter injects reactive current into the faulty grid to support AC voltage recovery, and the remaining capacity of the converter is used to inject active current. However, the grid current magnitude is monitored to avoid exceeding the current limit of the converter given by

$$I_{max} = \sqrt{(i_s^{q*})^2 + (i_s^{d*})^2} \tag{1}$$

where I_{max} is the maximum permissible current magnitude of the converter (commonly 1 p.u). If v_{pcc} is as low as 0.5 p.u (each TSO may define another value), the entire capacity of converter is used to inject reactive current; therefore, i_s^{d*} reaches to 1 p.u and i_s^{q*} becomes zero. The characteristics of i_s^{d*} and i_s^{q*} during FRT operation are shown in Fig. 2.

Moreover, referring to Fig. 1, if v_{pcc} becomes lower than U_{block}, the HVDC converter station remains connected to the AC grid without active and reactive power contribution, i.e., the phase-locked loop (PLL) continues operating to keep the converter synchronized with the AC grid, but the active and reactive current references are set to zero (see Fig. 2). Such operation mode is often called blocking operation. The exact value of U_{block} for blocking operation is defined by the relevant TSO.

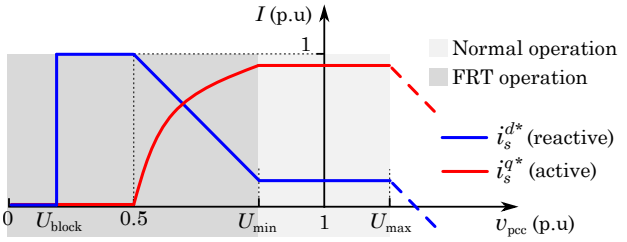

Fig. 2. Reactive and active current references in normal and FRT operation

An effective FRT mechanism has to deal with multiple fault scenarios:

- *Fault types*: Both symmetrical and asymmetrical faults can cause a major PCC voltage dip. Seven types of voltage dips, classified based on the symmetrical components of v_{pcc}, are sketched in Fig. 3 [22]. The pre-fault voltage and fault voltage are denoted by E and V, respectively. The voltage dip type A is caused by a three-phase fault. The type B is only caused by a single-line-to-ground (SLG) fault. Also, types C and D are the results of either SLG or line-to-line (LL) fault. Finally, types E, F, and G are only expected if the fault is double-line-to-ground (LLG).
- *Fault location*: Faults may occur in AC grid 1 or 2, and therefore, both MMCs are needed to be equipped with an adequate FRT mechanism.
- *Pre-fault power flow direction*: The direction of the pre-fault power flow through the HVDC link has an impact on the dynamics of the FRT mechanism. The pre-fault power flow direction can be positive or negative. Here, the positive power flow direction is assumed to be from MMC 1 to MMC 2. If a fault occurs in AC grid 1 and the pre-fault power flow direction is positive, the lack of power in DC link causes DC under voltage; whereas, if the power flow is negative, the surplus power in the DC link leads to DC over voltage. Similar observation can be made for faults in AC grid 2. Thus, both pre-fault power flow directions have to be considered during FRT design.

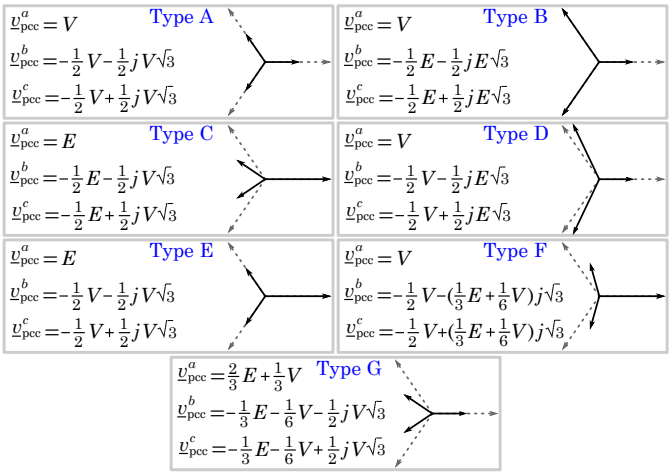

Fig. 3. Seven types of PCC voltage dip as caused by symmetrical and asymmetrical faults

In summary, the effectiveness of the FRT mechanism should be tested for 28 different fault scenarios ($7 \times 2 \times 2$). The primary objective of the FRT control is to ensure that the control systems of MMC 1 and 2 remain stable for the large disturbance imposed by v_{pcc} during all 28 fault scenarios. In addition to stability, the transient responses of DC voltage, grid current, and internal energy of MMCs should not exhibit large under/overshoots at the time of the fault occurrence and during transitions from normal operation to FRT operation. To this end, two FRT mechanisms are suggested for the DC voltage control loop of MMC 1 and the active power control loop of MMC 2, which are discussed in the following section.

III. MMC Control Strategy with FRT Capabilities

The topology of a grid-connected MMC is shown in Fig. 4. The MMC has six arms, each of them consisting of N_{arm} half-bridge submodules with a capacitor C_{SM} and a series arm reactor. The submodules (SM) can be controlled individually to either insert their capacitors in the circuit or bypass it. The voltages of the six arms can be controlled to achieve the desired power exchange between DC and AC sides. The overall control systems of MMCs 1 and 2, including the suggested FRT mechanisms, are detailed in Fig. 5. In the following sections, the three main control divisions are discussed. Note that the variables related to MMCs 1 and 2 are denoted by subscripts 1 and 2, respectively.

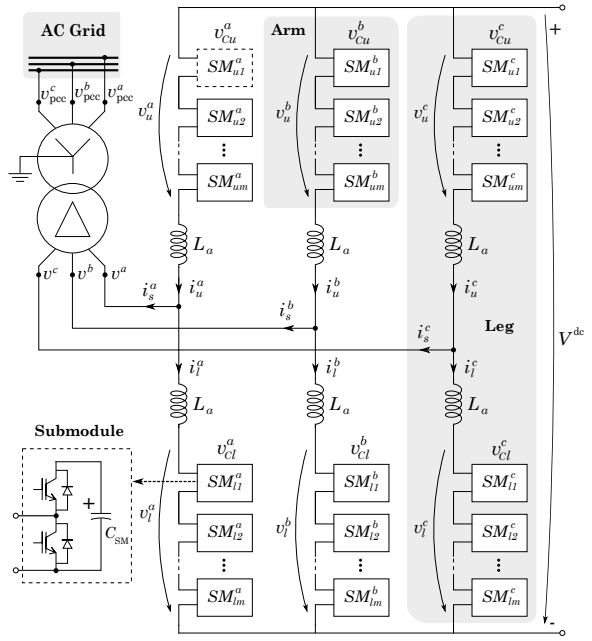

Fig. 4. Structure of a grid-connected MMC

A. Internal Energy Control

Generally, there are two distinctive methods for internal energy control of an MMC, namely voltage-based control (also referred to as direct control), and energy-based control (indirect control) [23]. Depending on the application and the control objectives, one of them may be preferred over the other one. For the purpose of FRT operation, however, it has been shown that the energy-based control is a more effective control method [3], [20]. This is mainly due to the unique ability of the energy-based control in fully decoupling the AC-side and DC-side dynamics of an MMC. More specifically, unlike the voltage-based control, the dynamics of the SM capacitor voltages are not directly imposed on the dynamics of the DC link voltage in energy-based control methods. This brings a clear advantage for the FRT operation: the double-line frequency oscillations, which are caused by asymmetrical faults, are inherently avoided in the energy-based control approaches [3]. Nonetheless, the implementation of energy-based control is more complicated than voltage-based control, since it requires six dedicated energy control loops to ensure stable operation [24].

In this study, the internal energy controls of MMC 1 and 2 are adopted from the energy-based control approach that is developed in [24]. Since both MMCs have similar internal energy control, we briefly describe the general concept and omit the subscript 1 and 2 for variables.

Referring to the given arms' variables in Fig. 4, it is common to define the following variable changes for the purpose of energy control design,

$$\begin{cases} v^j_{\text{diff}} \triangleq \dfrac{1}{2}\big(-v^j_u + v^j_l\big) \\ v^j_{\text{sum}} \triangleq v^j_u + v^j_l \\ i^j_{\text{sum}} \triangleq \dfrac{1}{2}\big(i^j_u + i^j_l\big) \end{cases} \qquad \begin{cases} R \triangleq \dfrac{R_a}{2} + R_s \\ L \triangleq \dfrac{L_a}{2} + L_s \end{cases} \tag{2}$$

where v^j_{diff}, v^j_{sum}, and i^j_{sum}, are, respectively, differential voltage, additive voltage, and additive current of phase j, ($j = a, b, c$). The MMC arm reactor has the inductance and resistance of L_a and R_a, respectively. The coupling power transformer is assumed to have the equivalent inductance and resistance of, respectively, L_s and R_s. The energy differences between two legs (W_{ab}, W_{ac}) and the energy differences between upper and lower arms of three legs (W_a, W_b, W_c) are maintained to zero by five control loops. One additional control loop is used to maintain the total stored energy (W_t) at the MMC rated energy level,

$$W^*_t = 6\frac{1}{2}\frac{C_{SM}}{N_{arm}}\,(V^{\text{dc}*})^2 \tag{3}$$

The outputs of the energy control loops are the DC power differences between two legs (P^*_{ab}, P^*_{ac}) and the upper and lower arms (P^*_a, P^*_b, P^*_c), and the total DC power of MMC (P^*_t). Here, a slight modification is made as compared to the original control scheme. A feed-forward from the positive sequence of the grid current reference (i^{q+*}_s) is used for the total power control loop. Such feed-forward improves the transient response of the total energy control loop, and its gain, g_e, is determined by

$$g_e = \frac{3}{2}U_N \tag{4}$$

where U_N is the rated voltage of the AC grid. The purpose of such gain is to scale up the dynamics of the grid current to power level. However, that is an initial value and is subject to slight changes after final parameter tuning.

Next, the DC powers are used to calculate the DC and AC terms of the additive current reference in $\alpha\beta$-frame ($i^{\alpha\beta 0\text{dc}*}_{\text{sum}}$ and $i^{\alpha\beta 0\text{ac}*}_{\text{sum}}$). The DC terms of additive current are given as

$$\begin{bmatrix} i^{\alpha\text{dc}^*}_{\text{sum}} \\ i^{\beta\text{dc}^*}_{\text{sum}} \\ i^{0\text{dc}^*}_{\text{sum}} \end{bmatrix} = \frac{1}{3\ V^{\text{dc}*}} \begin{bmatrix} 0 & 1 & 1 \\ 0 & \sqrt{3} & -\sqrt{3} \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} P^*_t \\ P^*_{ab} \\ P^*_{ac} \end{bmatrix} \tag{5}$$

The calculation of the AC terms is more complicated since it contains positive and negative sequence components. A detailed explanation on how to derive the AC terms of additive current are provided in [24].

B. Suggested FRT Mechanism for MMC 1

Referring to Fig. 5, MMC 1 regulates the DC voltage of the HVDC link (V^{dc}_1) in normal operation via a PI controller (PI_v). It is suggested to have a feed-forward from the zero sequence of the DC additive current (DC link current), $i^{0\text{dc}^*}_{\text{sum1}}$, with the gain of g_v, in order to improve the dynamics of the DC voltage at the presence of the fast transients on $i^{0\text{dc}*}_{\text{sum1}}$. The output of the DC voltage control loop is the q-axis reference of the grid positive-sequence current (i^{q+*}_{s1}).

A fault condition in AC grid 1 is detected by monitoring the magnitude of v_{pcc1}. As given by the grid codes [4] and in coordination with the corresponding TSO, if v_{pcc1} drops to lower than U_{min}, which is commonly 0.85 p.u, the FRT mechanism will be activated. This detection is carried out by an out-of-range condition control block. Once the binary signal

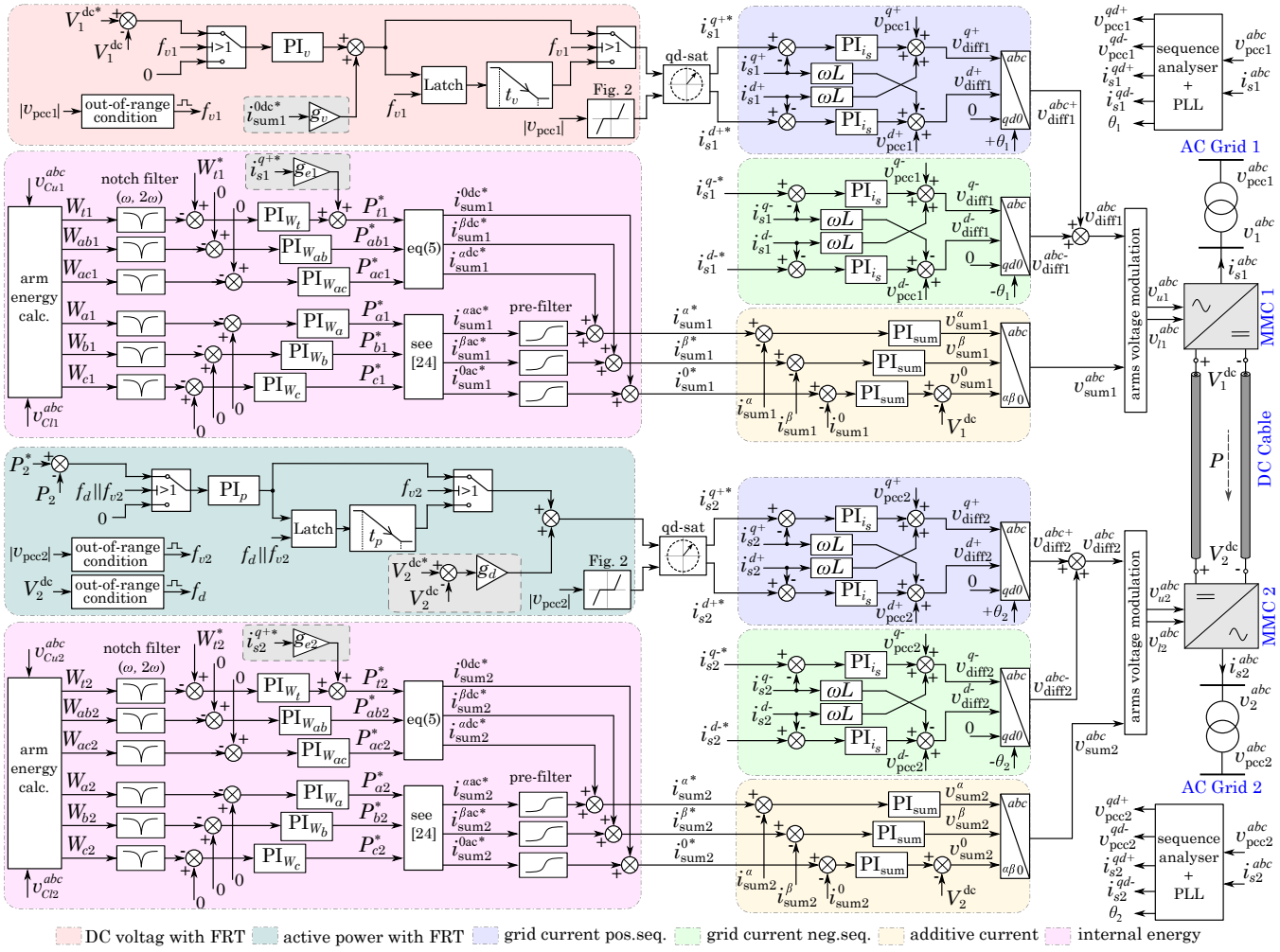

Fig. 5. The control systems of MMC 1 and MMC 2 equipped with FRT capabilities

f_{v1} changes from zero to one, the DC voltage control loop is bypassed to avoid high fault current injection to the grid by i_{s1}^{q+*}. Note that the DC voltage cannot be controlled via a PI controller during fault as it tries to increase i_{s1}^{q+*} until hits the upper limit (saturation).

By bypassing PI_v, DC voltage is no longer regulated in the HVDC link. At this moment, as we will discuss later, the FRT mechanism of MMC 2 takes the control over the DC voltage. This transition is communication free and requires only the local measurement of DC voltage. As V_1^{dc} is not being regulated by MMC 1, it starts drifting away from the permissible range. With a delay related to the time constant of the DC cable capacitance, V_2^{dc} at the DC terminal of MMC 2 also exceeds the limits, which activates the FRT mechanism on MMC 2. In order to avoid a sudden drop in V_1^{dc} due to the action of the bypass, and leave time for MMC 2 to react to the DC voltage changes, the pre-fault output value of PI_v, which is equal to i_{s1}^{q+*}, is latched and reduced by a ramp-down function to the value that is calculated by (1). The time duration of the ramp is t_v. It is suggested that t_v to be bigger than the time constant of DC cable capacitance. Also, if the relevant TSO defines specific active power contribution during fault, the ramp-down function may arrive at that certain value for i_{s1}^{q+*} to fulfil the requirement of the active power contribution.

With regard to the reactive current reference, i_{s1}^{d+*}, it is defined based on the curve given in Fig. 2. Once the positive-sequence qd current references are generated, they are passed through a standard qd current saturation block. Although the suggested FRT mechanism avoids overcurrent during faults by bypassing PI_v, this saturation block is used as a back-up control in case of FRT control failures. The saturation block also ensures that qd currents remain proportional even if saturation occurs [25]. The negative sequence of the grid current, i_{s1}^{qd-*}, is set to zero; however, it may have any value if requested by the corresponding TSO.

C. Suggested FRT Mechanism for MMC 2

As indicated in Fig. 5, MMC 2 controls the active power of the HVDC link in normal operation by a PI controller (PI_p). It is suggested to have a feed-forward from V_2^{dc} droop control (with the gain g_d) to the output of PI_p, which is primarily used to take the control of DC voltage during the time that MMC 1 can no longer regulate it (fault in AC grid 1). Nonetheless, this feed-forward remains active during normal operation of

the HVDC link. The gain g_d is selected as

$$g_d = \frac{P_N}{\Delta V^{\text{dc}} \times V_2^{\text{dc}*}} \times \frac{2}{3U_N} \tag{6}$$

where P_N and U_N are the rated power and rated AC voltage of the MMC, respectively. ΔV^{dc} is in percentage and denotes the maximum permissible DC voltage deviation, and V_2^{dc*} is the DC voltage reference. For a tight voltage regulation, ΔV^{dc} is set at 2%. The gain g_d has two terms: the term on the left is a standard droop gain and the term on the right is a scaling factor. Using g_d, the DC voltage is scaled down to i_{s2}^{q+*}. However, g_d is subject to slight changes after final parameter tuning. Worth mentioning that a droop controller is preferred over a PI controller since the transition from PI_v in MMC 1 to a droop controller in MMC 2 is significantly simpler than transition to another PI controller.

Two conditions will activate the FRT mechanism of MMC 2: (i) a fault in AC grid 2 and, therefore, out-of-range condition of v_{pcc2}, which has similar concept as the FRT mechanism of the DC voltage control, and (ii) the out-of-range condition of V_2^{dc} which is commonly due to a fault in AC grid 1. For these two conditions, the binary signals f_{v2} and f_d are constantly monitored for FRT activation. It is worth mentioning that if either conditions occurs, the active power loop has to be bypassed as the HVDC link can no longer operate in normal condition to transfer the rated active power (P_2^*).

The active current reference (i_{s2}^{q+*}) is the sum of the ramp-down function and the output of the droop controller, which is monitored not to exceed the converter limits as calculated by (1). The ramp-down function has a ramping time of t_p. It is suggested that t_p to be smaller than t_v to take the control of DC voltage before it drops to a very low value. The reactive current reference, i_{s2}^{d+*}, is based on the curve given in Fig. 2. Similar to the FRT control of MMC 1, the positive-sequence qd currents are passed through a saturation block before feeding to the inner current loops. The i_{s2}^{qd-*} is also set to zero.

The FRT mechanisms of MMC 1 and 2 are summarized as,

- For faults in AC grid 1, PI_v loop in MMC 1 is bypassed (f_{v1} becomes one). Also, due to DC voltage deviation, PI_p in MMC 2 is bypassed by f_d, but the droop feed-forward remains operational for DC voltage control.
- For faults in AC grid 2, PI_p in MMC 2 is bypassed (f_{v2} becomes one) but the droop feed-forward is still operational. MMC 1 continues DC voltage regulation via PI_v.

IV. FRT Parameters Tuning

In this section, the control parameters of both MMCs for an adequate FRT performance are tuned. Since the results of the tuning depend on the characteristics of the HVDC system, such as MMCs' parameters and DC cable length, the tuning is conducted on the example HVDC system that is introduced in the next section.

For the suggested FRT mechanism, there are several control parameters to be specified: (i) 4 feed-forward gains: g_v, g_{e1}, g_d, and g_{e2}, (ii) 2 time parameters: t_v and t_p, and (iii) 12 PI controllers per each MMC. The PLL is designed to have a time response of 25 ms, and the sequence analyzer is based on the signal-delay cancellation method [26]. Commonly, the PI controllers of the inner current loops (PI_{is} and PI_{sum} in Fig. 5) are defined based on the MMC impedance and the desired closed-loop time constant [24]. Here, we assume a time constant of τ=1 ms for both inner current loops with the following PI coefficients,

$$\text{PI}_{is}(s) = \frac{1}{\tau}(L + \frac{R}{s}) \tag{7}$$

$$\text{PI}_{\text{sum}}(s) = \frac{1}{\tau}(2L_a + \frac{2R_a}{s}) \tag{8}$$

The design procedure of the outer loops (PI controllers of the internal energy, DC voltage, and active power) can be defined depending on the specific control objectives. The following objectives are set in this study: (i) a closed-loop time constant that is about 10 times slower than the time constant of the inner current loops, (ii) the maximum over/undershoots of the system variables during the transition from normal operation to FRT operation are limited to 10% of the rated values. Note that the main disturbances to the closed-loop system are v_{pcc1} and v_{pcc2}. (iii) The closed-loop system should be stable during FRT operation.

A linear model of the system is required to obtain a control design that meets the aforementioned objectives. For this purpose, the linear model that has been developed in [27] is adopted. For the sake of brevity, only results are presented here. The PI coefficients and the feed-forward gains after tuning are given in Table I. Note that the 6 PI controllers (PI_{W_t}, $\text{PI}_{W_{ab}}$, $\text{PI}_{W_{ac}}$, PI_{W_a}, PI_{W_b}, and PI_{W_c}) of the internal energy loops have the same coefficients.

The sensitivities of the system eigenvalues to the variations of the feed-forward gains, g_v, g_{e1}, g_d, and g_{e2}, are shown in Fig. 6. For a better illustration, the gains are expressed in per unit values, and they varied from 0 p.u, i.e. no feed-forward conditions, to 2 p.u. Regarding to g_{e1} and g_{e2}, it is assumed that their base values are given by (4); the base value for g_d is given by (6), and g_v has a base value of 1. Referring to Fig. 6(b), if g_{e1} is zero, the overall stability of the system is seriously challenged as a pair of eigenvalues moves to the right-half plane. For the final design of the gains, a heuristic method is used to meet the aforementioned control objectives. The black circles in Fig. 6 indicate the eigenvalues of the system for the final selected gains which are also given in Table I.

The impact of the time parameter, t_v, which is related to the ramp-down operation of FRT in MMC 1, on the DC voltage dynamics is studied through simulation of a three-phase fault in AC grid 1. The voltage dip is of Type A, and v_{pcc1} drops from 1 p.u to 0.25 p.u as indicated in Fig. 7. The fault occurs at t=1.5 s and is cleared at t=2 s. Assuming t_v is equal to zero, once the magnitude of v_{pcc1} goes below 0.85 p.u, signal f_{v1} becomes one to declare fault condition. At this point, PI_v is immediately bypassed, and i_{s1}^{q+*} is set to zero. Hence, V_1^{dc} falls steeply and without control (gray area in Fig. 7) until MMC 2 detects major DC voltage drop via f_d, and takes the control of V_2^{dc} via droop control (green region in Fig. 7).

TABLE I
PARAMETERS OF CONTROL LOOPS

Coefficients		PI$_v$	PI$_p$	PI$_{W_t}$	PI$_{i_s}$	PI$_{\text{sum}}$	g_e	g_v	g_d
MMC 1	k_p	0.045	-	150	2.478e+02	3.098e+02	5.094e+05	1.1	-
	k_i	2.834	-	3750	3.114e+03	3.893e+03			
MMC 2	k_p	-	1.628e-06	87.50	2.478e+02	3.098e+02	2.743e+05	-	0.039
	k_i	-	2.626e-04	2187.50	3.114e+03	3.893e+03			

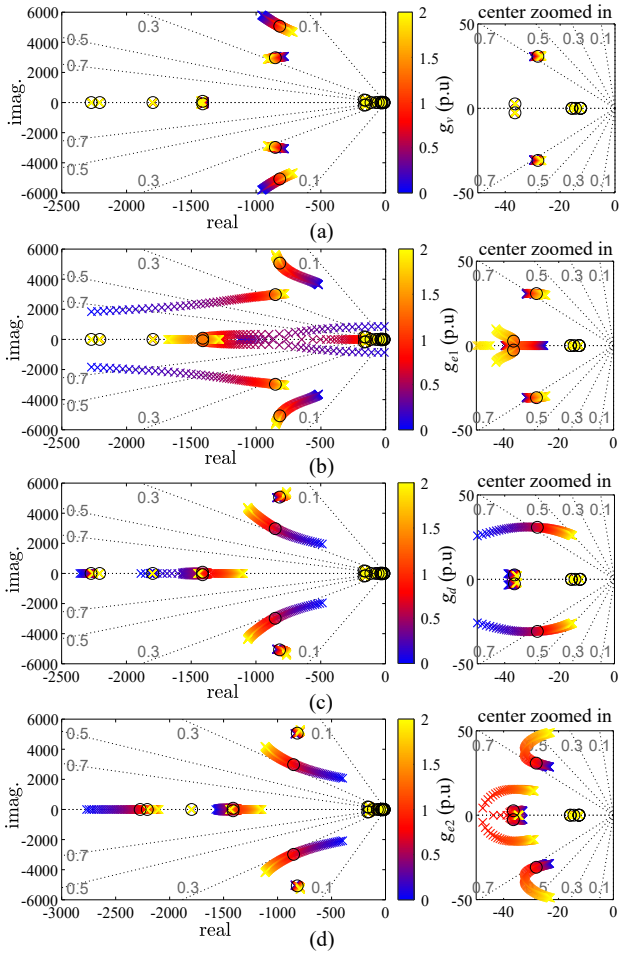

Fig. 6. Sensitivities of the system eigenvalues to the feed-forward gains, (a) g_v, (b) g_{e1}, (c) g_d, and (d) g_{e2}. The black circles indicate the eigenvalues of the system for the final selected gains.

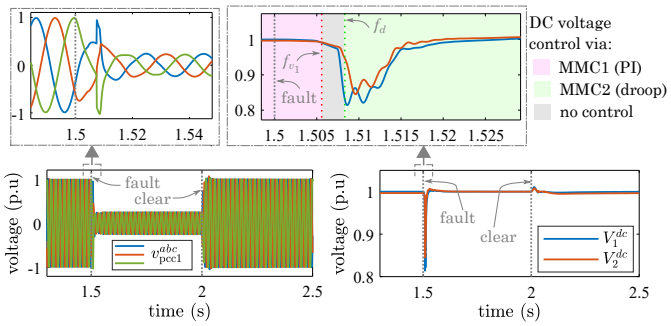

Fig. 7. Impact of t_v on DC voltage dynamics

Since it was assumed that t_v is zero, there has been a major DC voltage drop (as low as 0.8 p.u) during FRT operation. This can be effectively avoided by setting t_v to be higher than the decay rate of the DC voltage. Such decay rate is influenced by the time constants of the control loops, and the time constant of the DC cable. The closed-loop transfer function from $V_1^{\text{dc}*}$ to V_2^{dc} can be used to determined the decay rate of the DC voltage. Using the linear model developed in [27], such transfer function is derived and the maximum decay rate of the DC voltage is calculated as 39.6 ms. Hence, t_v=50 ms is selected in this study. It should be noted that if t_v is significantly larger than the decay rate of DC voltage, the speed of active current reduction becomes very slow. Meanwhile, the efforts of the MMC to inject reactive current into the AC grid may lead to temporary current saturation. Hence, t_v should be slightly larger than DC voltage decay rate and unnecessary high values have to be avoided. As it will be shown in the case study section, the DC under/over voltage is limited to less than 0.1 p.u with this strategy.

The tuning of the another time parameter, t_p, which is the ramp-down parameter of MMC 2, is less critical than t_v. Once the value of t_v is decided, t_p should be selected to be smaller than t_v. Here we assumed t_p is 25 ms, meaning that the DC voltage control is fully handed over to the droop control of MMC 2 once t_v reaches to its half value.

V. CASE STUDIES

In this section, three case studies are conducted in MATLAB software:

- Severe fault: the PCC voltage dip is 0.25 p.u, which is lower than the blocking voltage (U_{block}=0.3 pu), so MMC operates in the blocking conditions without reactive and active current contribution.
- Moderate fault: the PCC voltage dip is 0.7 p.u, which is higher than the blocking voltage. Therefore, MMC injects reactive and active currents into the AC grid during fault.
- Simultaneous fault: the PCC voltages of the AC grids 1 and 2 simultaneously drop to 0.25 p.u, meaning that both sides of the HVDC link experience fault conditions at the same time.

The MMCs of the HVDC system under study have the characteristics given by Table II. The length of the DC cable between two MMCs is 100 km, and it is modelled using a lumped parameters model relying on vector fitting [28].

A. Case Study 1: severe fault

The performance of the suggested FRT mechanisms is studied for all 28 fault scenarios. First, the detailed analysis of

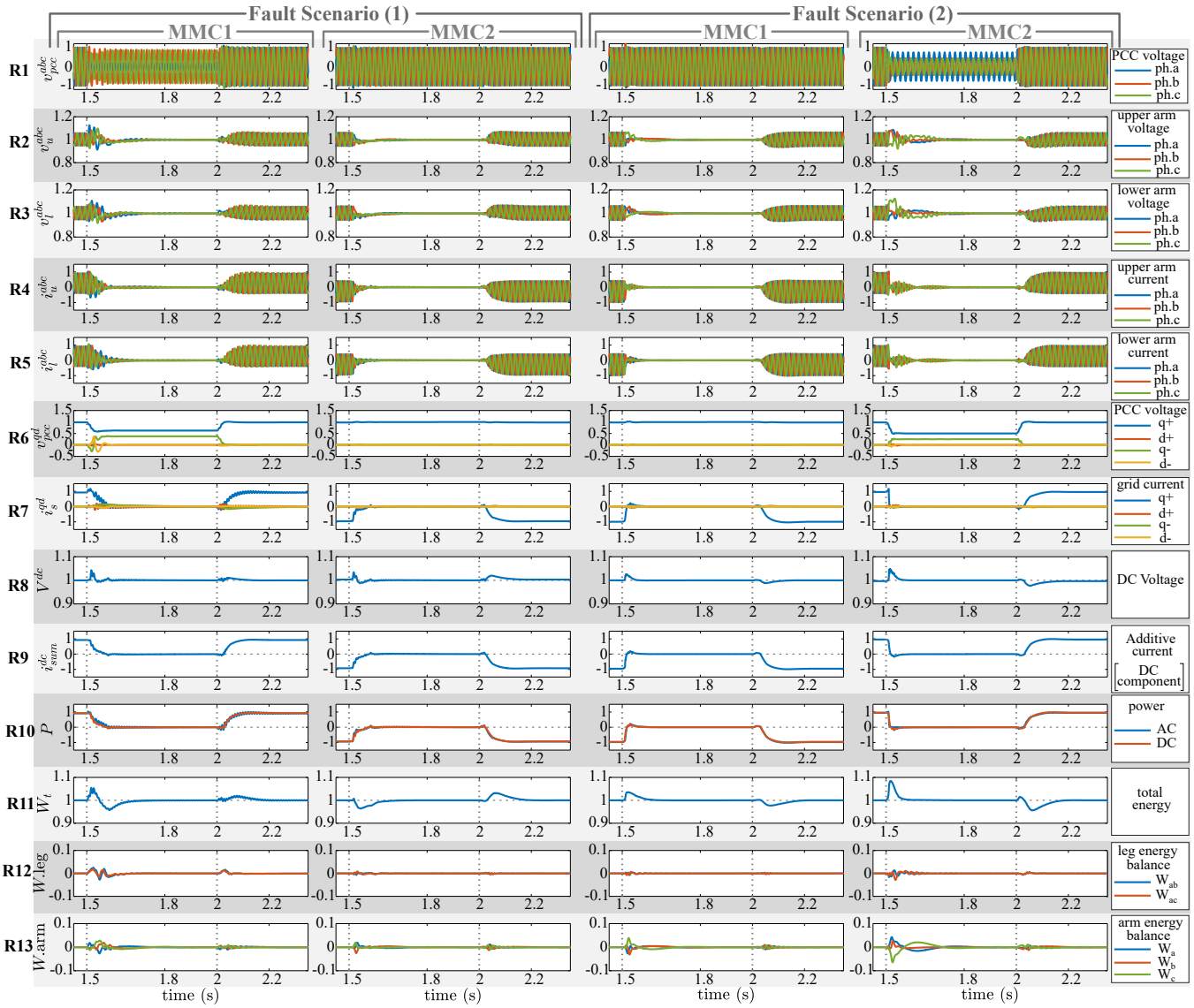

Fig. 8. case study 1: system variables for the fault scenarios 1 and 2

TABLE II
MMC PARAMETERS

Parameter	Symbol	Value	Units
Rated (base) active power	P_N	500	MW
Rated (base) AC-side voltage	U_N	320	kV
Rated (base) DC-side voltage	V_N^{dc}	640	kV
Grid short circuit ratio	SCR	10	-
Transformer impedance	R_s+jL_s	0.01+j0.2	pu
Arm reactor impedance	R_a+jL_a	0.01+j0.2	pu
Converter submodules per arm	N_{arm}	400	-
Average submodule voltage	V_{SM}	1.6	kV
Submodule capacitance	C_{SM}	8	mF

two selected fault scenarios are presented. Then, a summary of all fault scenarios are discussed.

1) Detailed analysis on two fault scenarios: Two particular fault scenarios are selected for the detailed analysis:

- Scenario 1: fault occurs in AC grid 1 at t=1.5 s and cleared at t=2 s. The pre-fault power direction is negative (from MMC 2 to MMC 1). The voltage dip is type D that is associated with SLG and LL faults.
- Scenario 2: fault occurs in AC grid 2 at t=1.5 s and cleared at t=2 s. The pre-fault power direction is positive (from MMC 1 to MMC 2). The voltage dip is type G that is associated with LLG faults.

The results of both fault scenarios are shown in Fig. 8. During FRT operation from t=1.5 s to 2 s, the DC voltage is properly regulated at 1 p.u as indicated in the row 8 (R8) of Fig. 8. Particularly, in the fault scenario 1, the ramp-down time (t_v) in MMC 1 leaves enough time for the droop controller of MMC 2 to take the control of DC voltage; hence the DC voltage over/undershoot remains within 10% of rated value.

Since fault voltage is 0.25 p.u (see R1), it is assumed that MMCs operate in blocking conditions without active or reactive power injection to the AC grid during FRT operation (see Fig. 2). Therefore, the references for the positive and negative sequences of the grid currents (i_s^{qd*}) are set to zero during FRT operation (see R7) to achieve zero power exchange

with the AC grid during the fault (see R10). Please note that PLL is fully functional and keeps the MMC synchronized to the AC grid. The performance of the internal energy balancing among MMC legs and upper and lower arms are indicated in, respectively, R12 and R13 of Fig. 8. While the energy differences are maintained at zero during fault, the total energy is regulated at 1 p.u (R11). Moreover, there is no voltage imbalance in the arm capacitor voltages due to the faults (see R2 and R3).

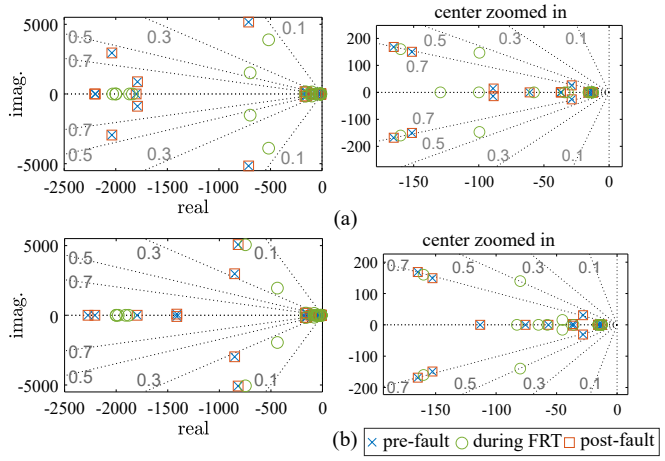

Fig. 9. Eigenvalues of the equilibrium points at pre-fault, during FRT, and post-fault operation, (a) fault scenario 1, and (b) fault scenario 2

In order to assure the stable operation of the system, the nonlinear model of the system is linearized at three equilibrium points for each fault scenario:

(i) Pre-fault steady-state operation at t=1.4 s
(ii) FRT steady-state operation at t=1.9 s
(iii) Post-fault steady-state operation at t=2.3 s

The linearization points of the linear models (i) and (ii) are influenced by the power direction. The linear model (iii) depends on the fault location. If fault is in AC grid 1, then DC voltage control loop of MMC 1 and active power loop of MMC 2 are removed from the linear model, but the droop feed-forward in MMC 2 remains in the model. On the contrary, if the fault occurs in AC grid 2, the active power loop and droop feed-forward in MMC 2 are removed from the linear model, but DC voltage control loop in MMC 1 remains activated. In either cases, the PLLs of MMC 1 and 2 are included in the linear model. The eigenvalues of these three linear models are shown in Fig. 9. As it can be seen, the FRT operation reaches to a stable equilibrium during faults as all eigenvalues have negative real part. Since the system has the same pre- and post-fault operating conditions in each fault scenario, the related eigenvalues are the same.

2) Summary of all fault scenarios: One of the objectives of the FRT parameter tuning (Section IV) is to make sure that no variable deviates (in sense of over/undershoot) more than 0.1 p.u from its rated value during transition from normal operation to FRT operation and vice versa. During this transition, the control systems of MMCs 1 and 2 should deal with the large disturbances of v_{pcc1} (for faults in AC grid 1) and v_{pcc2} (for faults in AC grid 2). To this end, the maximum deviation of all variables for 28 fault scenarios during the time period from t=1 to t=2.3 s have been recorded. Among all variables given in Fig. 8, only V^{dc}, W_t, i_s^{q+}, and arm capacitor voltages v_u and v_l are selected for presentation in Fig. 10. With regard to v_u and v_l, they are allowed to deviate up to 1 p.u from their nominal values. Note that the base voltage for arm capacitor voltages is equal to the rated DC voltage. However, arm capacitors are commonly designed to endure twice rated DC voltage [24].

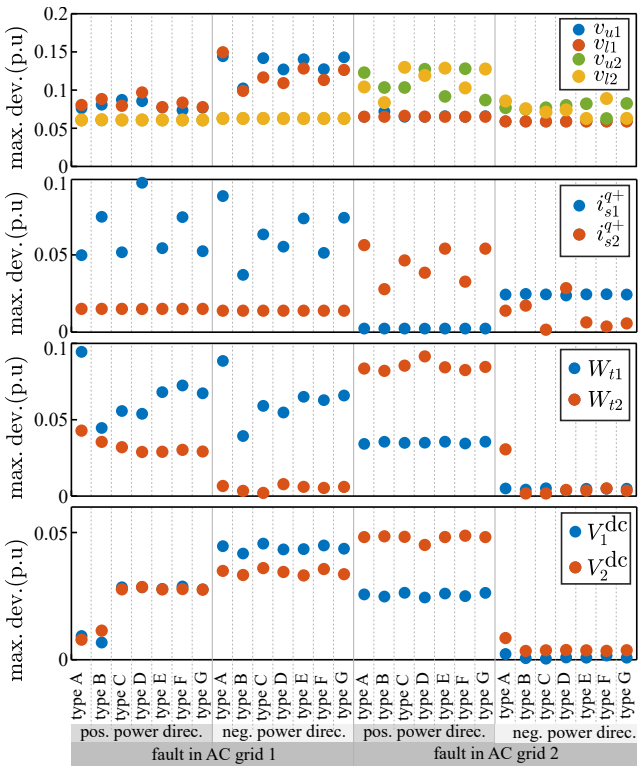

Fig. 10. Maximum deviation of the selected variables from the rated values for 28 fault scenarios

Referring to Fig. 10, although none of the variables violate the defined threshold, the impact of the pre-fault power direction on the maximum deviation is noticeable. For instance, the highest deviation in V_1^{dc} occurs for faults in AC grid 1 and negative pre-fault power direction, whereas, V_2^{dc} is more vulnerable to the faults in AC grid 2 and positive pre-fault power direction. As a general conclusion, the pre-fault power direction has to be considered as an influential parameters during FRT performance evaluation.

Next, the critical modes of the FRT operation for all fault scenarios are derived. For this purpose, the eigenvalues of the linear model (iii) are derived for all 28 fault scenarios. Then, the damping ratio for each eigenvalue is calculated. Using participation factor analysis, the state variables that contribute to the eigenvalues with low damping ratio are identified. As given in Table III, four critical modes with a damping ratio lower than 0.707 are identified. Overall, the high-frequency modes (3887 and 5058 rad/s) are excited by either V_1^{dc} or V_2^{dc}, and low-frequency modes (average 150 rad/s) are excited by the PI controllers of the PLLs in MMC 1 and 2. It is also noticeable that the least damped mode of the FRT operation

TABLE III
CRITICAL MODES OF THE FRT OPERATION

Fault location	Fault type	Mode 1			Mode 2			Mode 3			Mode 4		
		Damp.	Freq.	Excit.	Damp.	Freq.	Excit.	Damp.	Freq.	Excit.	Damp.	Freq.	Excit.
AC grid 1	A	0.132	3887.0	V_2^{dc}	0.353	105.8	PLL 1	0.417	1518.7	V_1^{dc}	0.707	160.0	PLL 2
	B				0.417	1518.8	V_1^{dc}	0.613	153.9	PLL 1			
	C							0.556	149.9	PLL 1			
	D							0.561	146.7	PLL 1			
	E							0.497	139.6	PLL 1			
	F							0.502	137.5	PLL 1			
	G							0.497	139.6	PLL 1			
AC grid 2	A	0.146	5058.0	V_1^{dc}	0.218	1949.3	V_2^{dc}	0.353	105.8	PLL 2	0.707	160.0	PLL 1
	B							0.613	153.9	PLL 2			
	C							0.556	149.9	PLL 2			
	D							0.561	146.7	PLL 2			
	E							0.497	139.6	PLL 2			
	F							0.502	137.5	PLL 2			
	G							0.497	139.6	PLL 2			

for faults in AC grid 1 belongs to the DC voltage of the other end of the HVDC link (V_2^{dc}). Similar situation exists for the faults in AC grid 2. Overall, regardless of the fault location and its type, the stability of the FRT mechanism is challenged by the four identified critical modes.

Before moving to the next case study, the performance of the FRT control is briefly evaluated in case the TSO requests to set U_{block} at 0 pu. The direct effect of such decision is that the MMC should inject 1 pu reactive current to the faulty AC grid. Obviously, the active current contribution would be zero (please see Fig. 2). The main purpose of this analysis is to assess the ability of FRT mechanism to supply 1 pu reactive current during severe fault in AC grid. In this scenario, a type A (symmetrical) fault occurs in AC grid 1, causing a voltage dip of nearly 0 pu. The timings of the events are the same as the previous case study. As it is shown in Fig. 11, MMC 1 injects 1 pu reactive current to the AC grid without causing any overcurrent conditions. The DC voltage is also stable and within the permissible range.

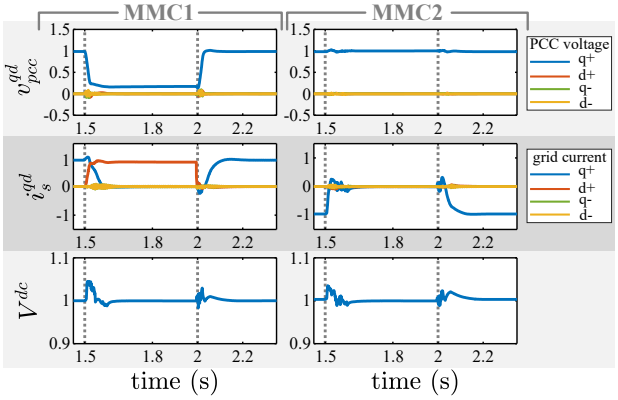

Fig. 11. 1 pu reactive current injection during symmetrical fault in AC grid

B. Case Study 2: moderate fault

In this case study, another fault scenario is conducted to evaluate the ability of the FRT mechanisms in providing reactive and active currents during FRT operation. Fault voltage is 0.7 p.u and it has the following characteristics:

- Scenario 3: fault occurs in AC grid 1 at t=1.5 s and cleared at t=2 s. The pre-fault power direction is negative (from MMC 2 to MMC 1). The voltage dip is type A that is associated with a three-phase fault (symmetrical).

The results of the fault scenario 3 are illustrated in Fig. 12. The system is stable during fault and the DC voltage is within permissible range (see R8). Different from the previous case study, MMC 1 injects 0.4 p.u reactive current (i_s^{d+} shown in R7) which is proportional to the voltage dip (according to Fig. 2). The remaining capacity of MMC 1, calculated by (1), is used to inject 0.91 p.u active current to the grid. The active current (and hence active power) that MMC 1 supplies to the faulty AC grid 1 is coming from MMC 2. The droop controller of MMC 2 automatically detects the DC voltage drop due to the lack of power in the DC link, and increases the active current set point to compensate for this lack of power. Please note that the MMC 1 regulates reactive power independently from MMC 2. Hence, the reactive current of MMC 2 is zero, while it is 0.4 p.u in MMC 1.

C. Case Study 3: simultaneous fault

In this case study, the fault scenario 3 is investigated. Fault voltage is 0.25 p.u and it has the following characteristics:

- Scenario 4: faults occur in both AC grids 1 and 2 simultaneously at t=1.5 s and cleared at t=2 s. The pre-fault power direction is positive (from MMC 1 to MMC 2). The voltage dip is type A that is associated with a symmetrical three-phase fault.

The purpose of such case study is to investigate FRT operation particularly for embedded HVDC links. In such application, the AC grids on the both sides of the HVDC link are interconnected, so that a fault occurrence causes voltage dip on the PCC voltages of the both sides of the HVDC link. The results of the fault scenario 4 is presented in Fig. 12. As it can be seen, the suggested FRT control is able to maintain stability of the system during the simultaneous fault condition.

VI. CONCLUSION

In this paper, two FRT mechanisms have been suggested for the DC voltage control loop of the master MMC (MMC 1)

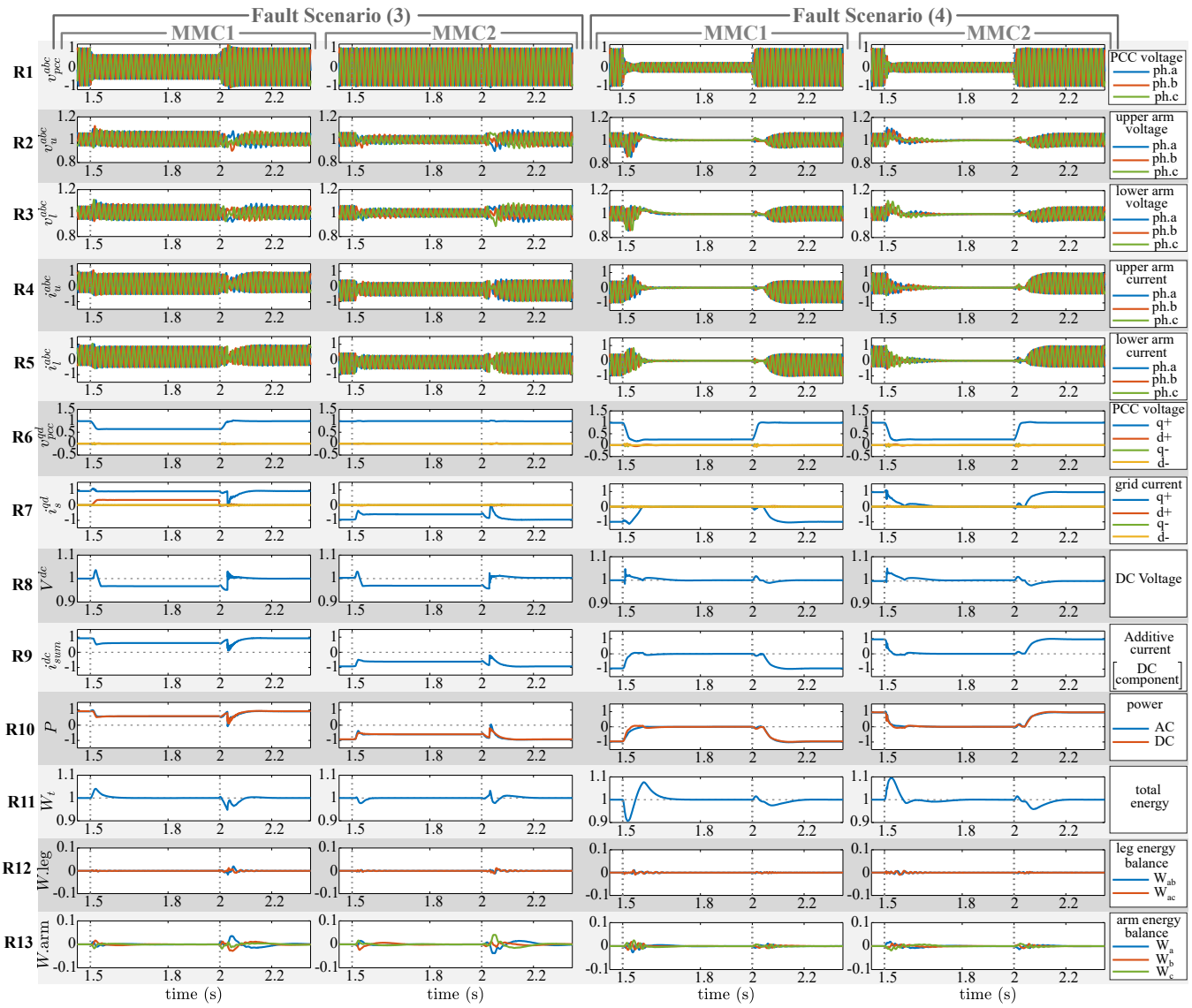

Fig. 12. Case study 2 and 3: system variables for the fault scenarios 3 and 4

and the active power loop of slave MMC (MMC 2). The main objective is to maintain the stable operation of the system and avoid system disconnection during faults in AC grids 1 and 2. While the DC voltage is regulated via PI controller of MMC 1 in normal conditions, it is controlled with the droop function of MMC 2 during faults in AC grid 1. This control transition is communication-less and a ramping function is used to facilitate this transition without major DC voltage drop/rise. The effectiveness of the FRT mechanisms have been tested for 28 fault scenarios that have been based on the fault types, fault locations, and pre-fault power flow direction. For every fault scenario, it has been shown that the HVDC link reaches to a stable equilibrium point during the fault conditions. DC voltage, internal energy, currents, and MMC arm capacitor voltages have been shown to have an adequate performance during transition between normal operation and FRT operation. It has been also revealed that four critical modes of the FRT operation with the least damping ratio are associated with the DC voltage variables and the PLLs of both MMCs.

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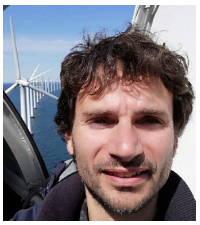

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