Control Method, Circuit Topology, and Power Architecture for High-performance AC–DC Converters

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Originality Statement

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Abstract

This thesis explores new approaches, including a new control method, a new power factor correction (PFC) front-end topology, and two power architectures to improve the performance of AC–DC power converters.

• Control method: A modulation and control method for an active-clamp flyback (ACF) converter is developed. It is first found that the internal clamping capacitor in the ACF converter can be used as an active buffer without any modifications on topology, by adopting the proposed modulation method. The clamping capacitor of the ACF converter can tolerate a much greater voltage swing than the buffer capacitor in a two-stage architecture, allowing for a single-stage adapter design with reduced capacitance requirements. A 100-W universal-input laboratory prototype is built, which achieves 94 % peak efficiency and up to 10x size reduction of the buffer capacitor.

• Circuit topology: A new topology for the PFC front end is developed, which enables simultaneous size reduction of both the inductor and the buffer capacitor by achieving zero-voltage-switching (ZVS) of all switches and active power buffering. An apple-to-apple experimental comparison is made between a typical critical-mode boost PFC and the proposed PFC front end. The prototype achieves a 47 % size reduction of the magnetics, a 21 % size reduction of the buffer capacitor, and an almost constant DC-link voltage while maintaining comparable efficiency performance.

• Power architecture ①: A stacked-switch PFC architecture is developed. The stacked-switch architecture allows all switches to achieve full-load-range ZVS at a universal input and under a constant switching frequency, which has not yet been demonstrated in any PFC applications before. This valuable property is achieved by simply removing the high-frequency diode in the two-stage architecture. Hence, higher power density can be achieved via high-frequency operations while requiring lower costs as the total component counts are

reduced. A 150-W universal-input prototype is built, which measures 92.9 % peak efficiency and 53.9 W/in^3 power density by box volume.

• Power architecture ②: A star PFC architecture is developed. It is first discovered that the current ripple in the second stage of a two-stage architecture can be used to 1) reduce the current ripple of the first boost PFC stage and to 2) assist full-range ZVS of the first PFC stage under a constant switching frequency. The star architecture thereby enables higher efficiency and smaller magnetics in the boost PFC front end while maintaining the performance of the second DC–DC stage, leading to a high-power-density and high-efficiency AC–DC converter. A 300-kHz, 240-W, 48-V-output, and universal input prototype is built, showcasing a high power factor, constant output voltage, 97.1 % full-load efficiency, and 55.6 W/in^3 power density by box volume. The star architecture is experimentally verified to achieve a 40 % loss reduction given the same power density compared to the two-stage architecture.

Acknowledgements

First, I want to thank my supervisor Prof. Weidong Xiao for his support. I found power electronics interesting and developed a strong passion for building hardware over the past five years, which would not be possible without his carefully prepared lectures and rigorous attitude toward teaching. He always opens his mind to my naive ideas and patiently corrects my understanding, which motivates me to think independently and develop my taste. Building hardware is never easy and sometimes heartbreaking, especially when watching your carefully designed circuits catch fire again and again. Without Prof. Xiao's encouragement and support, I can't imagine overcoming all the failures. I also learned a lot from his can-do attitude, which helped me stay positive against any challenges in life.

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CHAPTER 1

Introduction

AC–DC converters are widely used to transfer power from the utility grid to various DC load such as batteries, LEDs, computing devices, and so on [1]. The future trend of AC–DC converters is toward higher efficiency, higher power density, and lower cost to tackle the energy crisis, enable new applications, and reduce electronic waste. Among many solutions, a two-stage PFC architecture has been a dominant solution for AC–DC converters in commercial products over 75 W where power factor correction (PFC) is mandatory. The two-stage architecture generally consists of a boost PFC front end for sinusoidal input current and an isolated DC–DC back end for output voltage regulation, as shown in Fig. 1.1. The wide adoption of the two-stage architecture is mainly because multiple tasks in PFC applications can be divided and optimally addressed by each of the two stages, leading to high overall performance in efficiency, power density, operating range, design simplicity, and cost. Nevertheless, the performance of the two-stage architecture is increasingly challenged by the demand for lower cost, higher efficiency, and higher power density.

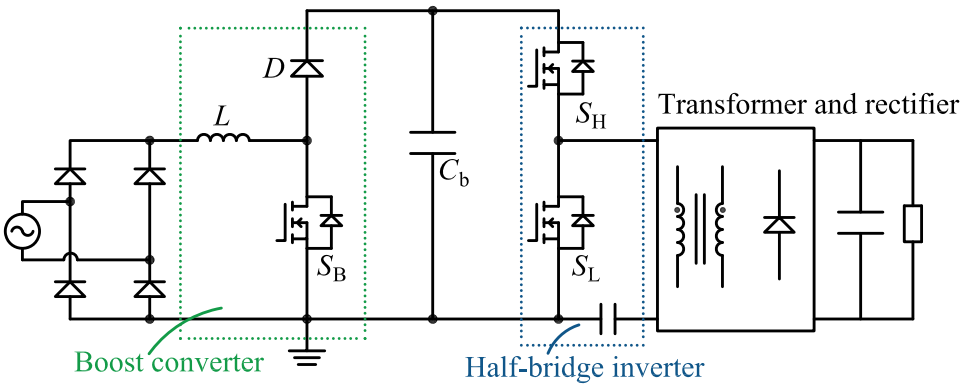

FIGURE 1.1: Two-stage PFC architecture.

This thesis takes the two-stage architecture as a benchmark and investigates new control methods, circuit topology, and power architectures to improve the performance of AC–DC converters. The key contributions are summarized as follows:

1. Control method:

   Single-stage active-clamp flyback (ACF) converter has been abandoned in PFC application due to the requirement of excessive output capacitance to reduce the double-line frequency ripple. This thesis finds a new method to control the ACF converter, enabling the clamping capacitor to be utilized as an active energy buffer without any modifications to the topology. As a result, lower buffer capacitance can be used without affecting the output voltage's ripple performance. With this new control method, it is demonstrated that up to 92 % size reduction of the buffer capacitor can be realized while achieving higher efficiency and lower component count than the two-stage solution [2].

2. Circuit topology:

   The boost PFC front end of the two-stage architecture suffers from hard switching, making it hard to reduce the size of inductor through high-frequency operations. In addition, high capacitance is required in the boost PFC front end to reduce the low-frequency ripple, leading to bulky buffer capacitors. This thesis introduces a new circuit topology for PFC front end applications. The new topology features ZVS across a universal input, ripple-free DC-link voltage, and reduced buffer capacitance, allowing for size reduction of both the inductor and the buffer capacitor. A 100-W universal input prototype is built, measuring a 96.7 % peak efficiency and 50.8 W/in^3 power density. Compared to a typical critical-mode (CRM) boost PFC front end, the prototype achieves a 47% size reduction of the magnetics, a 21% size reduction of the buffer capacitor, and an almost constant DC-link voltage while maintaining comparable efficiency performance [3].

3. Stacked-switch architecture:

   The author found that the above solutions have some issues that may hinder their practical applications, including losing ZVS at light-load conditions, requiring additional passive components, and varying switching frequencies. Motivated by

these issues, a stacked-switch PFC architecture is developed. The stacked-switch architecture has lower component counts and, thus, lower cost than the two-stage architecture. In addition, it is first demonstrated that full-range ZVS of all active switches can be achieved under a constant switching frequency in PFC applications, enabling higher power density than the two-stage architecture and simplifying the hardware design and implementation. It is also demonstrated that the stacked-switch architecture can directly take advantage of the existing control circuits for the two-stage architecture and a simple analog circuit is enough. A 150-W-universal-input prototype is built, measuring 92.9 % peak efficiency and 53.9 W/in^3 power density by box volume [4].

4. Star architecture:

   While high-frequency operations enable smaller magnetic components, the achievable power density is also constrained by the temperature rise, calling for solutions that can operate at a higher frequency while having higher efficiency. The author, therefore, tried to find a scaling law in magnetic components that may lead to higher efficiency at a higher frequency. Interestingly, one such scaling law is found — the inductor features lower root-mean-square (RMS) current and lower peak-to-peak flux density with the increase of switching frequency in continuous-conduction-mode (CCM) operations of the boost converter. However, it is hard to take advantage of this scaling law because the conventional CCM boost PFC converter is hard-switched, resulting in high switching loss if the switching frequency is increased. Targeting at 1) achieving CCM operations to take advantage of the scaling law and 2) achieving soft switching to unlock higher switching frequency, a star PFC architecture is developed, which only has one additional transistor compared to the two-stage architecture. With the star architecture, it is first found that the second stage's ripple current allows reduced current ripple in the first PFC stage and can assist full-range ZVS of the PFC stage even under CCM operations. The high performance of star architecture is enabled by realizing (i) continuous-conduction-mode (CCM) operation of the boost PFC stage and (ii) full-range zero-voltage-switching (ZVS) of all active switches. In addition, the star architecture can (i) operate at a

constant frequency via a proper selection of the circuit topology and modulation method and (ii) be controlled based on simple and low-cost analog electronic circuits. A 300-kHz, 240-W, 48-V-output, and universal-input prototype is built to verify the performance of the star architecture, showcasing high power factor, constant output voltage, 97.1 % full-load efficiency, 55.6 W/in^3 power density by box volume [5].

This thesis is organized as follows. Chapter two introduces the new control method for ACF converter. Chapter three introduces the new circuit topology for PFC front end. Chapter four introduces the stacked-switch architecture, and the star architecture is introduced in Chapter five. Finally, chapter six concludes this thesis.

CHAPTER 2

A Modulation Method for Capacitance Reduction in Active-clamp Flyback Converter

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2.1 Background

In an effort to promote consumer convenience and reduce electronic waste, the Universal Series Bus (USB), originally created in 1996 as a communication interface with only limited power delivery capabilities, has now become a primary method for powering and charging a wide range of electronics products [6]. The recently released USB Power Delivery 3.1 (USB-PD 3.1) has just pushed the power delivery profile to 240-W power range, making it possible to extend its applicability to an even greater number of application scenarios [7].

The increased power demand, however, poses great challenges to existing adapter design regarding system cost and power density, especially as the power level exceeds 75 W when power factor correction (PFC) becomes mandatory [8]. Conventional solutions in the above-75W range usually adopt a two-stage topology [9], consisting of an AC–DC stage for PFC followed by a DC–DC stage for output regulation and galvanic isolation, with a twice-line frequency buffer capacitor in between (see Fig. 2.1 (a)) [9]–[12]. On the one hand, a two-stage topology requires multiple switches, drivers, sensors, magnetics, auxiliary power supplies and control circuits, generally leading to complex and costly design. On the other hand, the buffer capacitor is a well-known bottleneck in realizing a high-density adapter design: its size is generally large as its energy storage requirement depends on the line frequency, thereby cannot be reduced by increasing the switching frequency [13]. Thus, to lower system cost and increase power density, it is highly desirable to develop single-stage isolated solutions with

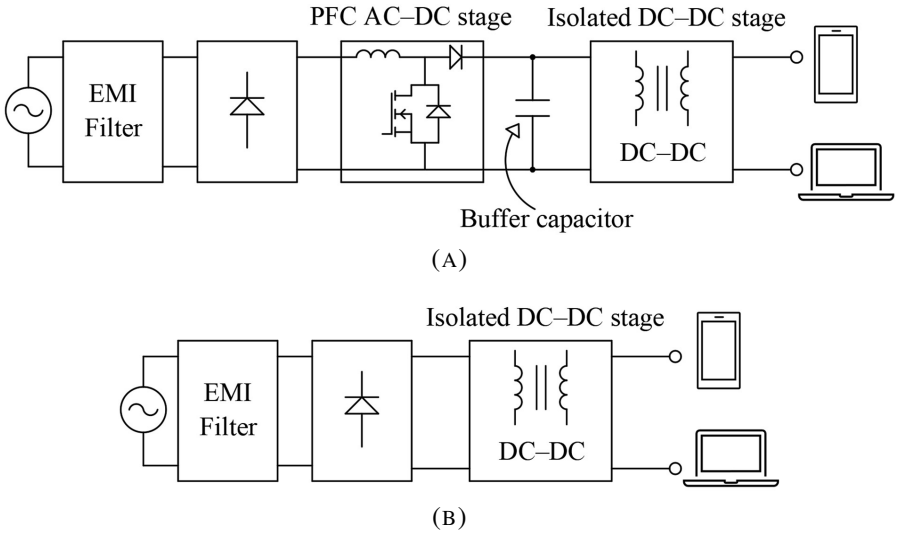


FIGURE 2.1: Architectures of adapters: (A) two-stage architecture typically used when high power factor is required (B) single-stage architecture.

reduced buffer capacitance requirement while being able to retain the conventional two-stage solutions' efficiency, PFC and galvanic isolation function (see Fig. 2.1 (b)).

Targeting the limitations of the two-stage solution, significant research efforts have focused either on single-stage isolated AC-DC power conversion [14]–[16] or buffer capacitance reduction [17]–[20] or both, through the development of advanced topology, modulation method and/or power devices. For those focusing only on single-stage isolated (or buffer capacitance reduction), the issues of large buffer capacitor (or high component count) remain unsolved. On the other hand, those focusing on both targets, in general, cannot outperform the conventional two-stage solutions. For example, [21] presents a hybrid converter that merges a two-stage converter into one stage and utilizes the intermediate capacitor as an active power buffer for capacitance reduction. However, the solution is based on hard switching and the leakage energy is lost per switching cycle, presenting high switching and leakage energy losses at the high operating frequency. A modified single-stage active-clamped flyback (ACF) converter is proposed in [22], effectively integrating the active power buffer function into the clamping capacitor. Buffer capacitance can be reduced, but the cost and losses are increased, as a tertiary winding and two extras secondary MOSFETs are needed and the two MOSFETs and output diodes are hard switched. A modified flyback-based solution is presented in [23].

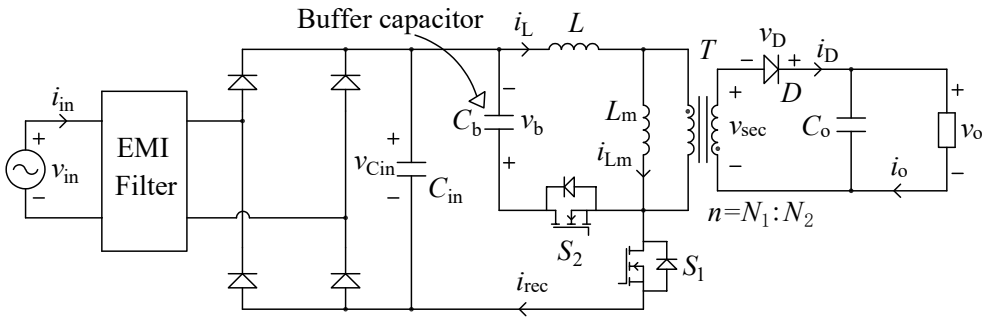


FIGURE 2.2: The topology of ACF converter.

Capacitance requirement is reduced by integrating the active power buffer into the system, but two additional switches and one tertiary winding are required while all switches are hard switched.

Focusing on single-stage power conversion and buffer capacitance reduction, this thesis discusses a new modulation method for ACF converter [24]. Without the need for hardware modifications, this modulation method enables ACF converter to achieve (i) PFC, (ii) active power buffering, (iii) zero-voltage-switching (ZVS) of active switches, (iv) zero-current-switching (ZCS) of output rectifier diode or synchronous rectifier (SR), (v) galvanic isolation, and (vi) leakage recycling, all in a single power-conversion stage. Although this approach requires a more elaborate control strategy than the conventional ACF control method, it provides an economically viable and technologically elegant solution to the problem of costly and bulky adapter design for high-power delivery.

2.2 Topology and Operating Principle

Fig. 2.2 illustrates the basic circuit of an ACF-based AC–DC adapter, consisting of an EMI filter, a diode bridge rectifier, a high frequency filter C_{in}, a half-bridge switch leg S_1 and S_2, a clamping and energy buffer capacitor C_b, a transformer T with a magnetizing inductance of L_m and a turns ratio of N_1:N_2, a resonant inductor L, an output rectifier D, and an output filter C_o. Here, L may be further integrated with T, and D replaced with an SR. To explain the proposed modulation method, the operation of the conventional continuous conduction mode ACF converter is briefly reviewed [25].

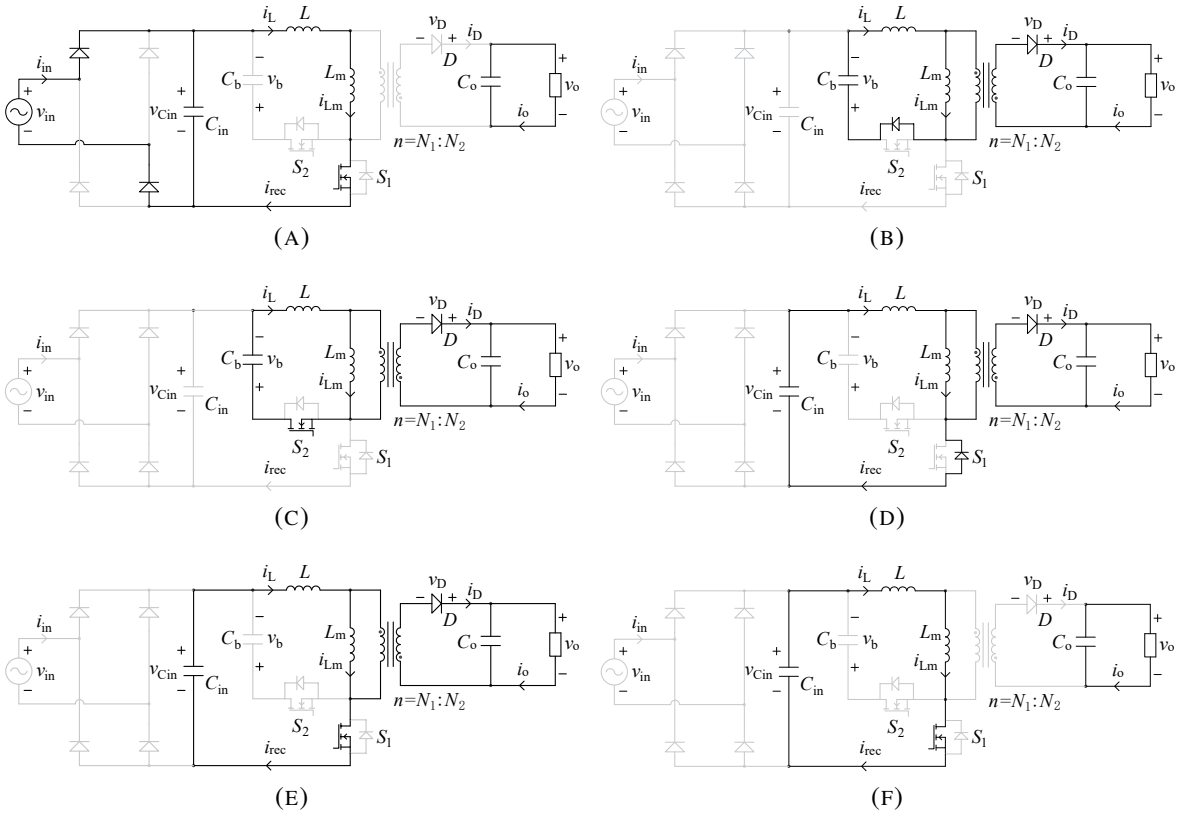


FIGURE 2.3: Operating states. (A) State I:[T_o–T_1]. (B) State II:[T_1–T_2]. (C) State III:[T_2–T_3]. (D) State IV:[T_3–T_4]. (E) State V:[T_4–T_5]. (F) State VI:[T_5–T_6].

2.2.1 Conventional Operating Method

The key operating waveforms of the conventional ACF converter are shown Fig. 2.4. Neglecting the deadtime, 6 operating states can be identified over one switching cycle.

State I [T_0–T_1]: i_L and i_{Lm} are linearly charged by v_{in} as shown in Fig. 2.3 (a) with a rising slope k_1 expressed by

$$k_1 = \frac{v_{in}}{L + L_m}. \tag{2.1}$$

The diode D is reverse-biased as the voltage across the secondary side of T, annotated as v_{sec} in Fig. 2.2, is negative. State I ends when S_1 is turned off at T_1.

State II [T_1–T_2]: L and L_m begin to resonate with the total output capacitances of S_1 and S_2. The resonance ends when the body diode of S_2 starts to conduct. State II ends when S_2 is

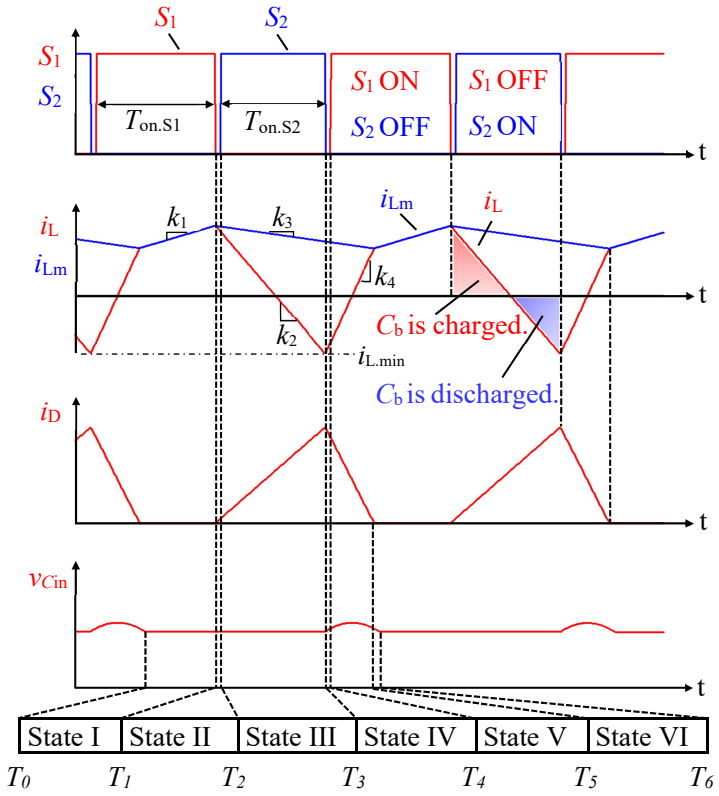


FIGURE 2.4: Operating waveforms.

turned on with ZVS at T_2. The condition, $v_b \geq N_1 v_o / N_2$, is essential to ensure a sufficient voltage across the secondary winding to turn on D so that energy can be transferred from the primary side to the secondary side.

State III [T_2–T_3]: S_1's drain–source voltage is clamped at (v_b + v_{Cin}) while i_L and i_{Lm} start to decrease. During this period, i_L and i_{Lm} become

$$i_L = i_{L.min} + k_2(t - T_3) \tag{2.2}$$

$$i_{Lm} = i_{L.min} + k_3(t - T_3) \tag{2.3}$$

where $i_{L.min}$ is the minimum i_L within each switching period and the expression of $i_{L.min}$ is derived in Appendix, k_2 is the slope of i_L in State III, and k_3 is the slope of i_{Lm} in State III. k_2 and k_3 can be derived as

$$k_2 = \frac{N_1 v_o - N_2 v_b}{N_2 L} \tag{2.4}$$

$$k_3 = -\frac{N_1 v_o}{N_2 L_m}. \tag{2.5}$$

In State III, C_b is first charged and then discharged by i_L as the polarity of i_L reverses (see Fig. 2.4). The amount of charge absorbed by and released from C_b are highlighted as red and blue areas in Fig. 2.4, respectively. With the conventional operation method, S_2 needs to be controlled to ensure the charges are balanced in C_b per switching period at a steady state. State III ends when S_2 is turned off at T_3.

State IV [T_3–T_4]: The reversed i_L discharges the output capacitance of S_1. The body diode of S_1 starts to conduct, and S_1 is ready for ZVS turn-on as shown in Fig. 2.3 (d). Since $i_L < i_{Lm}$, D continues to conduct, clamping the voltage of L_m at ($N_1 v_o / N_2$). Based on Kirchhoff's Voltage Law, the voltage across L is (v_{Cin} + $N_1 v_o / N_2$). i_L thus increases with a slope of

$$k_4 = \frac{N_1 v_o + N_2 v_{Cin}}{N_2 L_m}. \tag{2.6}$$

The current slope of i_{Lm} remain the same as k_3. State IV ends when S_1 is turned on with ZVS at T_4.

State V [T_4–T_5]: During this state, L resonates with C_{in}, causing $v_{Cin} > |v_{in}|$. Hence, the front-end bridge rectifier is reverse-biased. i_{Lm} continues to decrease with a slope of k_3, while i_L increases. Therefore, i_D gradually decreases. State V ends when i_D reaches zero, and D is turned off with ZCS at T_5.

State VI [T_5–T_6]: L continues to resonate with C_{in} as shown in Fig. 2.3 (f). The resonance ends at T_6 when v_{Cin} drops to $|v_{in}|$ and the front-end bridge rectifier starts to conduct and clamps v_{Cin} at $|v_{in}|$.

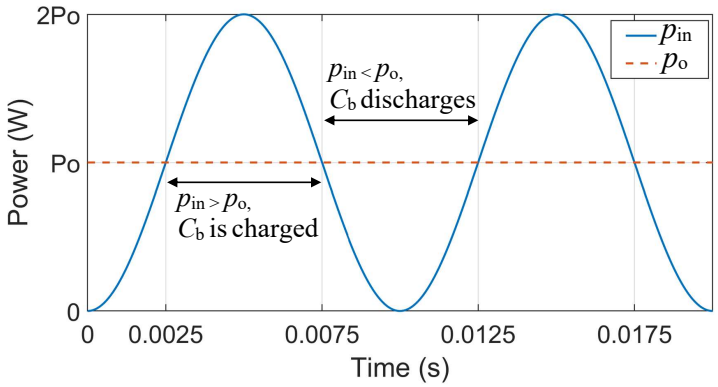
2.2.2 Proposed Operation

The proposed operating method is identical to the conventional one except for State III. According to the operating principles mentioned above, C_b is first charged and then discharged in State III when S_2 is maintained 'on'. As a result, the net charge per switching period can be controlled by the duration of State III (or S_2's on time). In other words, one may turn C_b into a twice-line frequency energy storage buffer (or an active power buffer) by actively controlling S_2's on time properly. In particular, when $p_{in} > p_o$, as shown in Fig. 2.5 (a), the turn on time of S_2, $T_{on.S2}$, needs to be reduced such that C_b is in effect absorbing power, as shown in Fig. 2.5 (b) where the red area is larger than the blue one. Similarly, when $p_{in} < p_o$, the turn on time of S_2 needs to be increased such that C_b is in effect releasing power, as shown in Fig. 2.5 (c) where the blue area is greater than the red one. The proposed converter operation is thus different from the conventional approach, which aims to achieve zero net charges in C_b per switching period. Thereby, C_b cannot offer low-frequency energy storage capability. This new approach indicates that one can integrate the active power buffering function into ACF circuit topology shown in Fig. 2.2 without modifying the hardware. Furthermore, all features of ACF are retained, including soft switching of S_1, S_2 and D, leakage inductor energy recycling, galvanic isolation, and active voltage clamping for S_1.

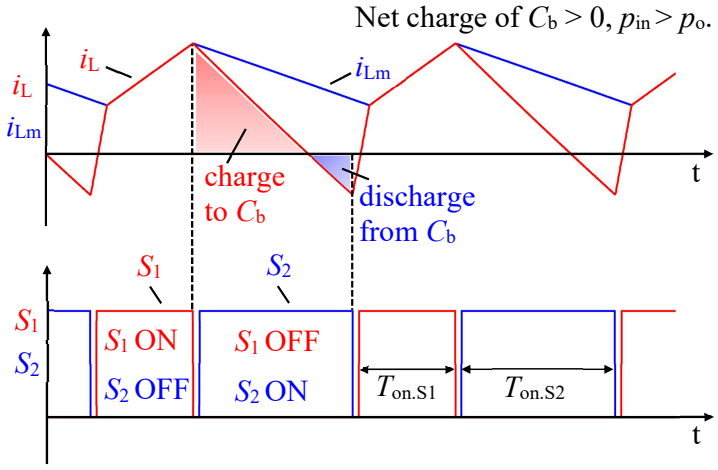
Table. 2.1 summarises the key differences between the conventional and the proposed operating methods of ACF converter. Although the PFC function can be achieved with ACF converters, most existing works only utilise the ACF converter for DC/DC conversions without performing the PFC function. The reason is that the conventional method of AC–DC ACF requires high capacitance of C_o to mitigate twice-line frequency ripples and maintain a low voltage ripple of the DC side.

2.3 Modulation and Control Method

The modulation and control schemes are newly developed and discussed in this section to support the proposed operation in Section 2.2.2.



(A)



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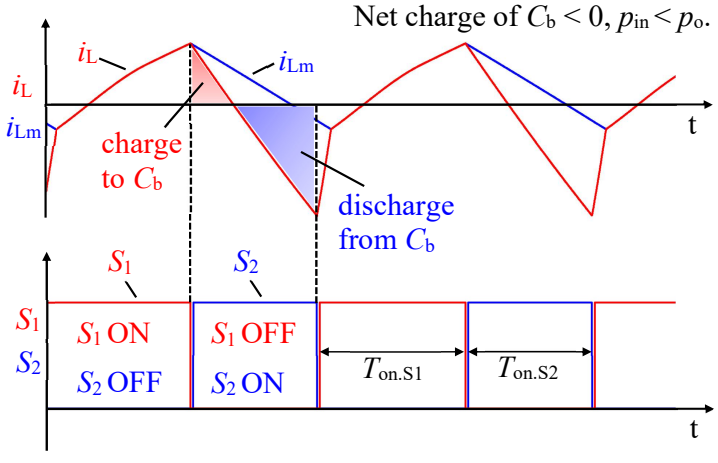


(C)

FIGURE 2.5: Charging and discharging phases of C_b: (A) power flows of input power p_{in} and output power p_o (B) charging phase (C) discharging phase.

TABLE 2.1: Comparison between the conventional operating methods and the proposed operating method.

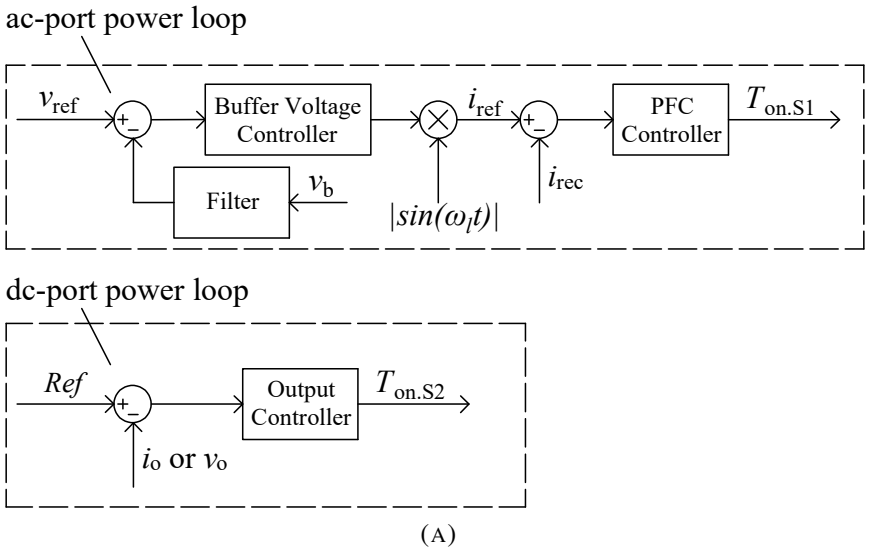
	Conventional Method of DC–DC ACF	Conventional Method of AC–DC ACF	Proposed Method of AC–DC ACF
Soft switching	$\surd$	$\surd$	$\surd$
Leakage recycling	$\surd$	$\surd$	$\surd$
PFC	$\times$	$\surd$	$\surd$
Active power buffering	$\times$	$\times$	$\surd$
Extra PFC Stage	Require	Not require	Not require
100/120 Hz buffer	C_{in}	C_o	C_b
Bias of buffer voltage	High ($> \lvert v_{in} \rvert$)	Small (= v_o)	Medium ($> N_1 v_o / N_2$)
Voltage swing of buffer	Small	Highly restricted	Large
Size of buffer capacitor	Medium	Large	Small

2.3.1 Dual On-time Modulation

According to Fig. 2.4, the current (or equivalently power) at the ac-port of ACF over one switching period is determined by the duration of the State I. Therefore, the ac-port current (or power), i_{in}, scales with the on-time of S_1, denoted as $T_{on.S1}$, which can be utilized as a control variable for ac-port current (power) regulation. On the other hand, according to Fig. 2.4, the current (power) at the dc-port, i_o, is determined by the duration of State III. In particular, the longer State III is, the more energy is to be released from C_b and the deeper L will be negatively charged, leading to an increased peak of secondary diode current and average dc current. Therefore, the dc-port current (power) scales with the on-time of S_2, denoted as $T_{on.S2}$, which can be utilized as a control variable for dc-port voltage (power) regulation. According to the automatic power decoupling control theory [26], and based on the two reasons mentioned above, $T_{on.S1}$ and $T_{on.S2}$ are chosen as modulation signals. Such a control method is named dual on-time modulation thereafter.

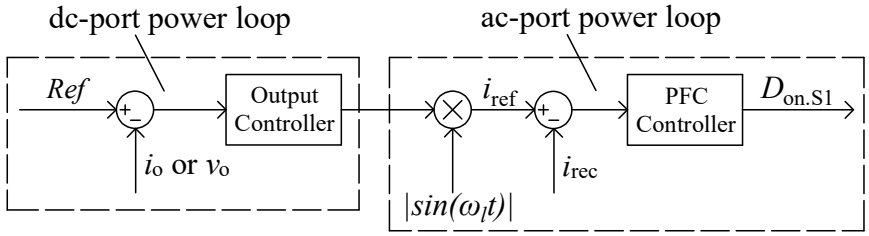
The architecture of the proposed dual on-time modulation is shown in Fig. 2.6 (a). The control scheme consists of an ac-port power loop and a dc-port power loop. For the ac-port, a PFC controller regulates i_{rec} to follow a rectified sinusoidal reference i_{ref} to achieve PFC function by adjusting $T_{on.S1}$, which is the on-state time of S_1. The amplitude of i_{ref} is obtained from the outer buffer voltage loop, which regulates the DC value of v_b at a predefined reference signal v_{ref}. The value of v_{ref} shall be properly specified to balance the current stress of C_b

Proposed control architecture:



(A)

Conventional control architecture:



(B)

FIGURE 2.6: (A) Proposed control architecture for the single-stage ACF PFC converter. (B) Conventional control architecture for the single-stage ACF PFC converter [14].

and the voltage stresses on S_1 and S_2. The value shall support a practical implementation using commonly rated power FETs and capacitors. The DC value of v_b can be extracted via a filter component. Depending on the application, either the output voltage (v_o) or current (i_o) can be regulated by the dc-port power loop, as shown in Fig. 2.6 (a). Ref is the reference for v_o or i_o. which shall be regulated by adjusting $T_{on.S2}$, which is the on-state time interval for S_2. When both ac-port and dc-port power are regulated at their respective reference values, their instantaneous power difference, which is pulsating at twice-line frequency shall be automatically balanced by the ripple-port without the need for a dedicated ripple-port controller.

For comparison, the conventional control architecture of AC–DC ACF converter is shown in Fig. 2.6 (b). In the control diagram, $D_{on.S1}$ is the duty cycle of S_1, v_{ref} is the reference for buffer's average voltage, i_{ref} is the reference for i_{rec}, and ω_l is the angular line frequency. Ref is the reference for v_o or i_o. Different from the proposed control architecture, the conventional control architecture directly regulates v_o or i_o through changing the amplitude of i_{in} via the duty cycle of S_1 [14]. Consequently, v_b is passively determined by the circuit parameters and the double-line frequency ripple is mainly buffered by C_o. Due to stringent ripple requirement on v_o, excessive C_o is mandatory with the conventional ACF control method, leading to the need for bulky buffer capacitors in the system and, thus, low power density.

2.3.2 Control Circuit Implementation

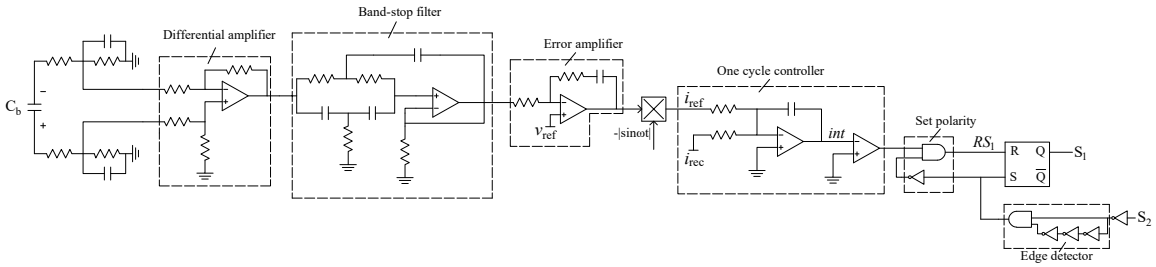


FIGURE 2.7: Analog circuit implementation of the ac-port power loop.

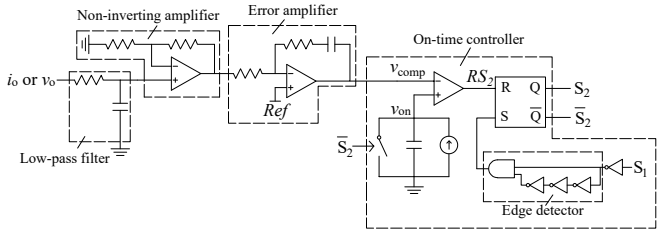


FIGURE 2.8: Analog circuit implementation of the dc-port power loop.

An analog control circuit is designed to execute the proposed dual on-time modulation control. Fig. 2.7 shows the control circuit for the ac-port power loop. The voltage across C_b is sensed by the voltage divider and differential amplifier. A band-stop filter is used to remove the double-line frequency ripple of the sensed signal to obtain the dc component of v_b. The buffer voltage controller, implemented as an error amplifier, compares the average value of v_b with v_{ref} to adjust the amplitude of i_{ref}, which is further multiplied by a rectified sinusoidal signal

to generate i_{ref}. A one-cycle controller, consisting of an error integrator and a comparator, is used as the PFC controller to adjust $T_{on.S1}$ for tracking i_{ref}. The output from the error integrator int is

$$int = \int (i_{ref} - i_{rec})\, dt. \tag{2.7}$$

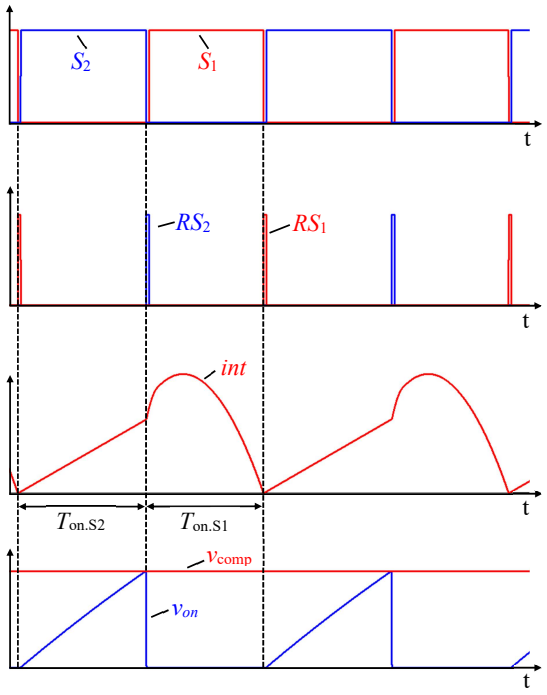


FIGURE 2.9: Detailed signals of the proposed control circuits.

A comparator resets the RS flip flop to turn off S_1 once int in (2.7) equals to zero, as shown in Fig. 2.9. This is when the average ac-port current over T_s equals to i_{ref} (assuming that v_{in} is piece-wise constant within T_s so that

$$\int_{StateIV}^{StateVI} i_L\, dt = 0. \tag{2.8}$$

Thus, the control scheme ensures fast and accurate ac reference current tracking in a cycle-by-cycle manner.

The implementation of the dc-port power loop is shown in Fig. 2.8. A filtered and amplified i_o (or v_o) signal is fed to the output controller, which is implemented by a second error amplifier to produce a control signal v_{comp}. An on-time controller then translates v_{comp} into $T_{on.S2}$ to

achieve on time modulation, where a higher v_{comp} means a longer $T_{on.S2}$. In particular, v_{on}, as defined in Fig. 2.9, starts to ramp up with a constant slew rate when S_2 is on and S_2 is turned off when v_{on} reaches v_{comp}, as shown in Fig. 2.9. The response of the dc-port loop depends on the second error amplifier design.

The switching deadtime should be selected short enough to minimize the deadtime loss and long enough to fully discharge the output capacitance of S_1 and S_2. In this study, the optimal value is fine-tuned following simulation and experiments and considering different operating conditions. The final value is determined by experimental tests to ensure full ZVS of S_1 and S_2 over the whole line cycle and the lowest switching loss.

The controller synthesis is based on the following procedure using the computer-aided design:

i. The small-signal model of the system is derived via the AC-sweeping method in the simulation environment.
ii. The control parameters are tuned to ensure sufficient stability margin and control bandwidth via the frequency-domain analysis.
iii. Iterative tuning is conducted to balance the system robustness and control performance, which is based on both simulation and experimental tests.

2.4 Design Consideration

This section describes the derivation of the circuit parameters to achieve practical voltage stress, full ZVS under the universal input, and high utilization of the buffer capacitor.

2.4.1 Design of Winding Turns Ratio n

The design principles of the winding turn ratio, n, are to comply with the circuit operating constraint mentioned in (2.9) and ensure secondary diode D's voltage stress is below a specified value $V_{D.max}$ (see (2.10)). The minimum value of v_b is defined as $V_{b.min}$. Thus,

$$V_{b.min} > \frac{n(L+L_m)v_o}{L_m} \approx nv_o. \tag{2.9}$$

should hold to make D forward-biased to deliver power. On the other hand, the voltage stress of D, v_D, can be calculated as below and should be smaller than $V_{D.max}$.

$$\begin{aligned} v_D &= \frac{V_{Cin.max}(L+L_m)}{nL_m} + v_o \\ &\approx \frac{V_{Cin.max}}{n} + v_o < V_{D.max}, \end{aligned} \tag{2.10}$$

where $V_{Cin.max}$ is the maximum value of v_{Cin}. From (2.9) and (2.10), the constraints of n is known by

$$\frac{V_{Cin.max} + nv_o}{V_{D.max}} < n < \frac{V_{b.min}}{v_o}. \tag{2.11}$$

2.4.2 Design of v_b and C_b

The design principles of C_b are to ensure the voltage stress of S_1 and S_2 below a specified value $V_{S.max}$ and reduce the energy storage requirements for C_b while leaving a sufficient operating margin. According to energy conservation, the power flow to C_b can be derived as

$$p_b = v_b C_b \frac{dv_b}{dt} = p_{in} - p_o. \tag{2.12}$$

Solving (2.12), the instantaneous v_b can be expressed as

$$v_b = \sqrt{V_b^2 - \frac{p_o}{\omega_l C_b} sin(2\omega_l t)}, \tag{2.13}$$

where V_b is a constant value representing the DC component in v_b. C_b can be calculated by rearranging (2.13) as

$$C_b = \frac{2P_o}{\omega_l \Delta V_b V_b^2 \sqrt{(4-\Delta V_b)^2}}, \tag{2.14}$$

where ΔV_b is the peak-to-peak ripple percentage of v_b.

According to (2.14), there are two design variables, ΔV_b and V_b, to determine C_b. To reduce the size of C_b, ΔV_b should be intentionally increased. Fig. 2.10 plots the waveforms of v_b under different C_b using (2.13). It can be seen that smaller C_b can be used if a higher voltage fluctuation of v_b is allowed. Hence, ΔV_b, can be selected first to properly size C_b. Then, V_b

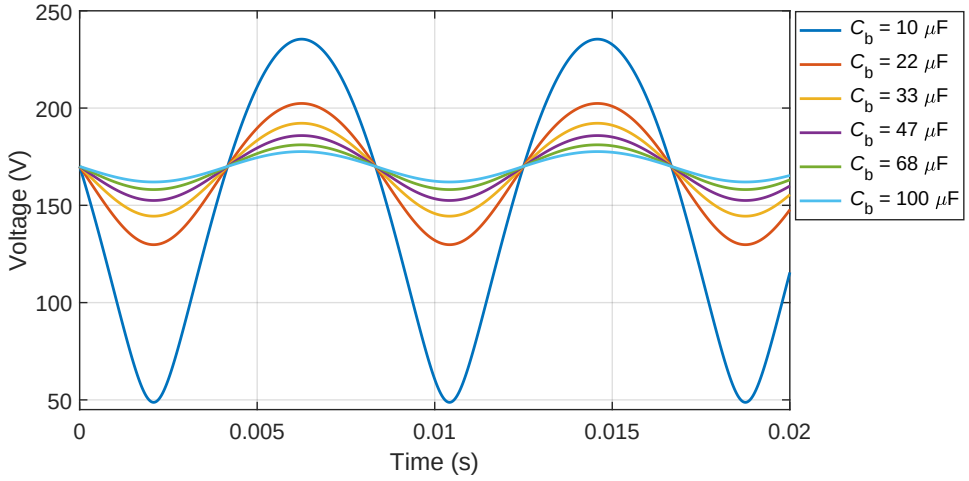


FIGURE 2.10: Effects of C_b on v_b. p_o = 100 W and V_b = 170 V.

can be determined based on the voltage stress requirements for S_1 and S_2. Finally, C_b can be determined by substituting the values of ΔV_b and V_b into (2.14).

2.4.3 Design of L_m and L

The design principles of L_m and L are to guarantee ZVS of S_1 and S_2 under the entire operating conditions, and to restrict the maximum f_{sw}. Further, the inductance of L shall be low to minimize the system cost or directly use the leakage inductance in the flyback transformer. Fig. 2.11 shows the equivalent circuit of S_1 and S_2 when the capacitances are discharged. Assuming the turn-on transient of S_1 is sufficiently fast such that v_b and v_{Cin} are regarded constant, the drain–source voltage of S_1 can be and S_2 can be expressed by (2.15) and (2.16), respectively. To ensure the ZVS of S_1 and S_2, the condition in (2.17) should be held.

$$\begin{aligned} v_{ds.S1} = v_{Cin} + v_b - i_{L.min}\sqrt{\frac{L}{2C_{oss}}}sin(\frac{1}{\sqrt{2LC_{oss}}}t) \\ + nv_o - nv_o cos(\frac{1}{\sqrt{2LC_{oss}}}t) \end{aligned} \tag{2.15}$$

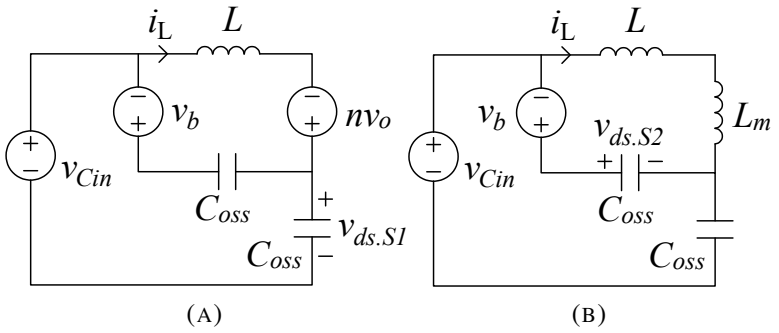


FIGURE 2.11: Equivalent resonant circuit during the ZVS of S_1 and S_2. (A) i_L is discharging the output capacitance of S_1. (B) i_L is discharging the output capacitance of S_2.

$$v_{ds.S2} = -(i_{L.min} - k_2 t_1)\sqrt{\frac{L+L_m}{2C_{oss}}}sin(\frac{1}{\sqrt{2(L+L_m)C_{oss}}}t) + v_{Cin} + v_b \tag{2.16}$$

$$\min(v_{ds.S1}) < 0 \quad \& \quad \min(v_{ds.S2}) < 0 \tag{2.17}$$

The switching frequency, f_{sw}, should be accordingly specified in the design stage. The detailed derivation of f_{sw} is provided in the Appendix. The expression of f_{sw} in terms of L and L_m is derived in (.7).

2.4.4 Concept Design

The circuit design follows a practical system, of which the specifications are shown in Table. 2.2. Following the design process in Section 2.4.1, the winding turns ratio should be defined by $3 < n < 7.5$. Hence, n = 5 is specified for the prototype design. A 20% peak-to-peak ripple is selected for v_b and $V_{b.max}$ is chosen to be 180 V to maintain a 90 V margin from the breakdown voltage of S_1 and S_2. Based on the proposed design in Section 2.4.2, the values of V_b and C_b are calculated to be 170 V and 47 μF, respectively. Therefore, an off-the-shelf 47 μF 250 V capacitor is selected. Table. 2.2 shows that the maximum f_{sw} shall be limited by 300 kHz. Following the design constraints in (2.17) and the maximum switching frequency requirement, the inductance values are determined as L = 60 μH and L_m = 260 μH. The system parameters are summarized in Table 2.3 for the prototype construction.

TABLE 2.2: Specifications of the prototype.

Specifications	Values
Input Voltage (v_{in})	100 $\sim$ 240 V AC 60 Hz
Output Rating (p_o, v_o, i_o)	100 W (20 V, 5 A)
Buffer Voltage (V_b)	170 V
Switching Frequency	60 $\sim$ 300 kHz
Voltage Stress of D ($V_{D.max}$)	150 V
Voltage Stress of S_1 and S_2	650 V
Voltage Ripple of C_b (ΔV_b)	20 %

TABLE 2.3: Designed parameters

Parameters	values
Magnetizing Inductance L_m	260 μH
Leakage Inductance L	60 μH
Winding Turns Ratio n	5
Buffer capacitance C_b	47 μF

TABLE 2.4: Bill of materials.

Components	Descriptions
Diode Bridge	RTBS40M M2G, 1000 V, 4 A
S_1, S_2	IPL60R285P7AUMA1, 600 V
Synchronous Rectifier	BSC093N15NS5ATMA1, 150 V
C_b	UCS2E470MHD1TO, 250 V, 47 μF
C_o	25SEPF330M * 2, 25 V, 330 μF
C_{in}	ECQ-E6123JF, 630 V, 12 nF
Transformer	RM 12, 35:7

2.5 Experimental Results and Evaluation

Following the concept design in Section 2.4.4, a prototype is built. The bill of materials are summarized in Table. 2.4. The buffer capacitor is the model, UCS2E470MHD1TO, rated as 47 μF and 250 V, which is small in size.

2.5.1 Verification

Fig. 2.12 shows the measured waveforms of v_{in}, i_{in}, v_b, and i_o when the AC power supply is rated for 110 V. The operating waveforms under 230 V AC are measured and shown in Fig. 2.13. The voltage ripple of v_b is measured to be 20%, which proves the design in 2.4.4.

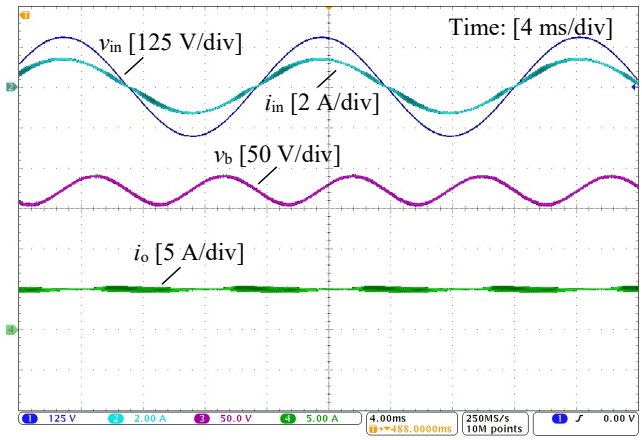


FIGURE 2.12: Operating waveforms of v_{in}, i_{in}, v_b, and i_o at 110 V AC.

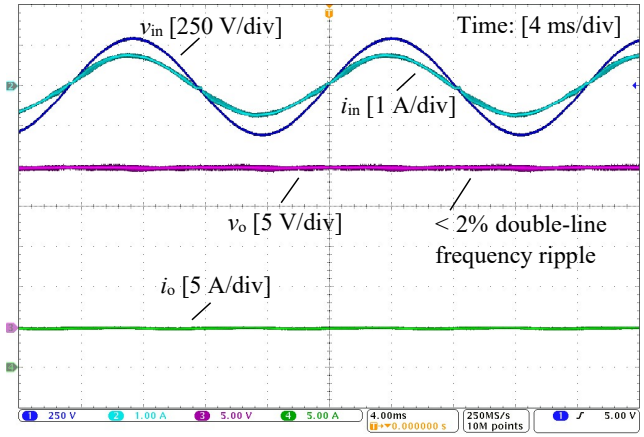


FIGURE 2.13: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 230 V AC.

Fig. 2.14 shows the waveform of v_{comp}, which is proportional to $T_{on.S2}$. As shown in Fig. 2.14, v_{comp} periodically varies to buffer the double-line frequency ripple while maintaining a constant output voltage. Particularly, a high level of v_{comp} is observed near the zero-crossing of v_{in} indicating that more power is released from C_b to the output. Meanwhile, a low level of v_{comp} is noticed near the peak of v_{in} indicating that more power is stored into C_b.

Fig. 2.15 demonstrates the resonating waveform of v_{Cin}. The amplitude of the resonance is well below the peak of v_{in}. The ZCS turn-off of the secondary synchronous rectifier is verified under 110 V and 230 V AC, as shown in Fig. 2.16 and Fig. 2.17, respectively. The ZVS turn-on operation of S_1 under 110 V and 230 V AC is verified and indicated in Fig. 2.18 and Fig. 2.19, respectively. The ZVS switching moment of S_1 is intentionally measured

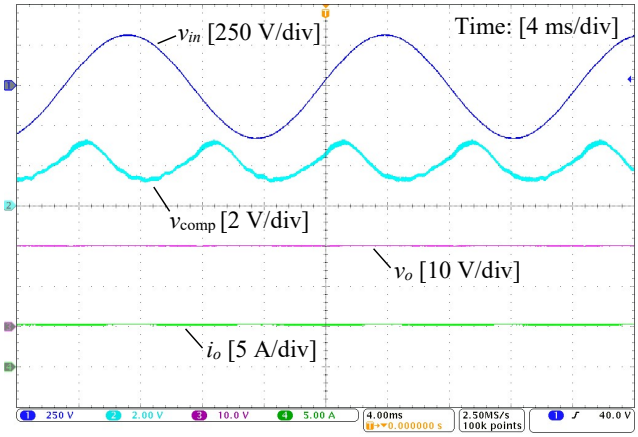


FIGURE 2.14: Operating waveform of v_{in}, v_{comp}, v_o, and i_o under 230 V AC

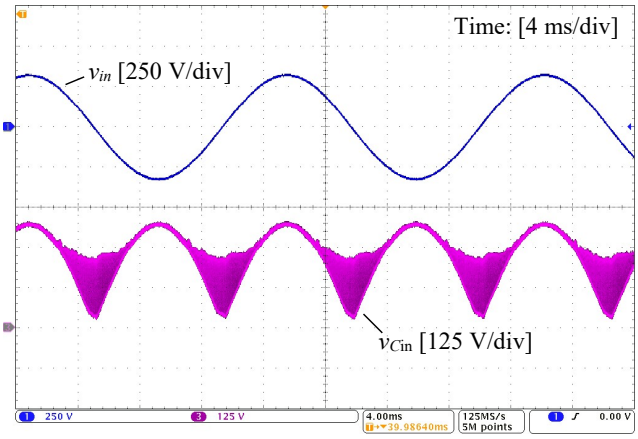


FIGURE 2.15: Operating waveform of v_{in} and $v_{C_{in}}$ under 230 V AC

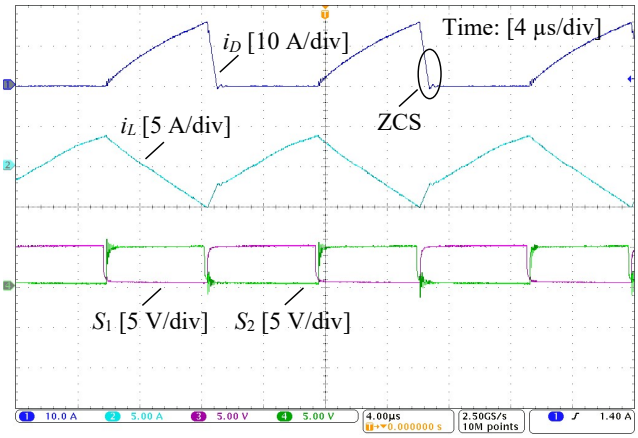


FIGURE 2.16: Operating waveform of i_D, i_L, logic signal to S_1, and logic signal to S_2 under 110 V AC

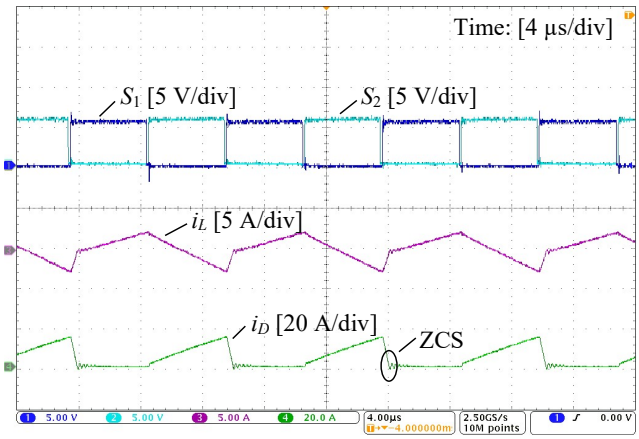


FIGURE 2.17: Operating waveform of i_D, i_L, logic signal to S_1, and logic signal to S_2 under 230 V AC

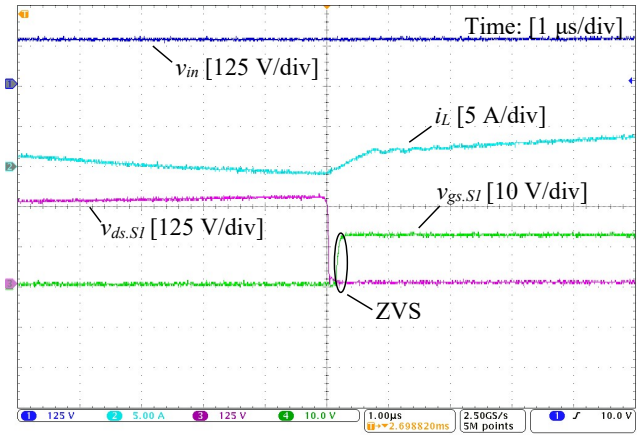


FIGURE 2.18: ZVS waveforms of S_1 under 110 V AC.

during the peak of v_{in} because the power released from C_b to achieve ZVS of S_1 is minimal at this interval. Similarly, the ZVS waveforms of S_2 are measured during the zero-crossing of v_{in} because the power from v_{in} to achieve ZVS of S_2 is minimal at this interval. Fig. 2.20 and Fig. 2.21 shows the ZVS switching-on operation of S_2 at the voltage levels of 110 V and 230 V, respectively. The experimental results show that the voltage stress of the proposed operation is identical to that of the conventional ACF converter. All measured waveforms match well with the previous analysis.

The experimental results demonstrate the proposed modulation method can achieve high power factor and constant output current with reduced buffer capacitance across a wide range of AC voltage in a single ACF stage. Fig. 2.22 shows that v_o can be regulated at 20 V under a

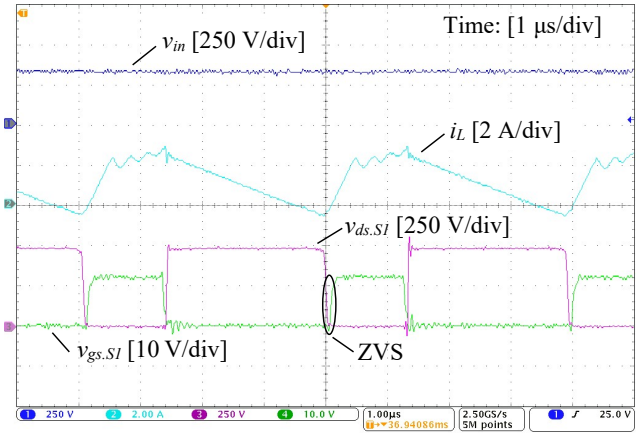


FIGURE 2.19: ZVS waveforms of S_1 under 230 V AC.

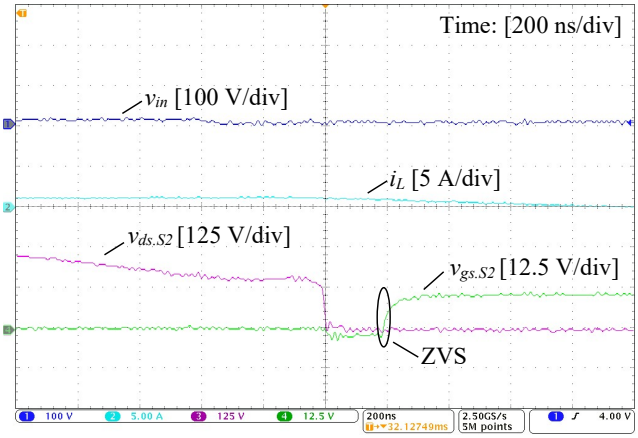


FIGURE 2.20: ZVS waveforms of S_2 under 110 V AC.

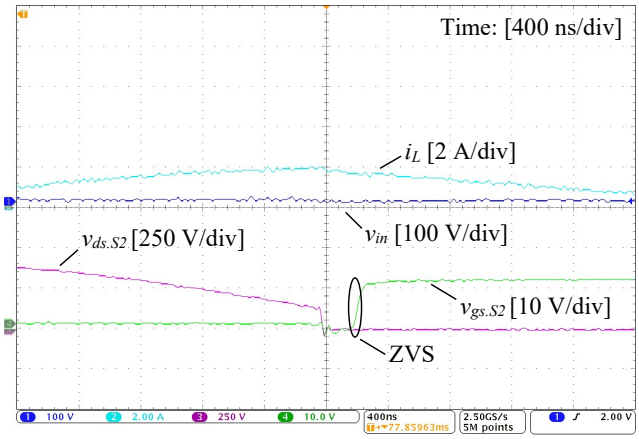


FIGURE 2.21: ZVS waveforms of S_2 under 230 V AC.

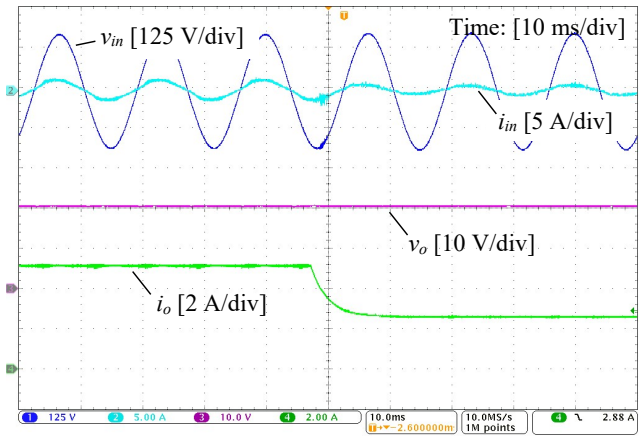


FIGURE 2.22: Transient waveforms with a load change from 100 W to 50 W.

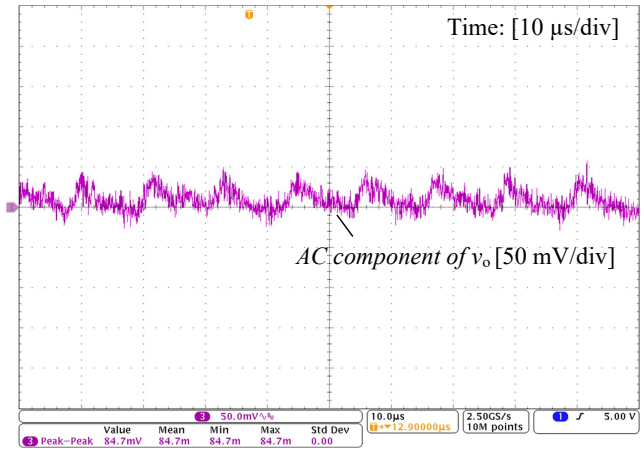


FIGURE 2.23: Plot to check the peak-to-peak ripple of v_o.

load change from 100 W to 50 W, which verifies the effectiveness of the proposed control circuit. The voltage ripple of v_o can be checked by the zoom-in plot, as shown Fig. 2.23. The peak-to-peak voltage ripple of v_o is measured to be 0.4 %, much lower than the 10 % requirements mandated by the standard of USB PD 3.1. Fig. 2.24 shows the plot of the total harmonic distortion of i_{in}. The experimental test reveals a lower THD value at higher input voltage, as shown in Fig. 2.24, which can be explained by (.7). The expression shows that the switching frequency becomes higher when the input voltage is increased. Thus, high-frequency harmonics are effectively suppressed by the existing filters. The power quality meets the IEC 61000-3-2 Class C standard, which is demonstrated in the spectrum plot, as shown in Fig. 2.25. A picture of the prototype is given in Fig. 2.26.

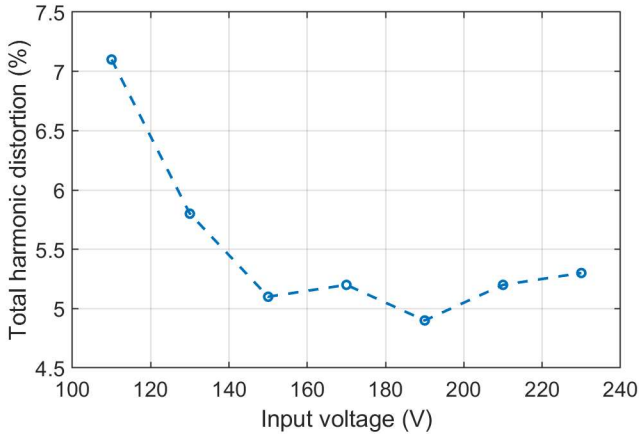


FIGURE 2.24: Total harmonic distortion of i_{in} versus input voltage.

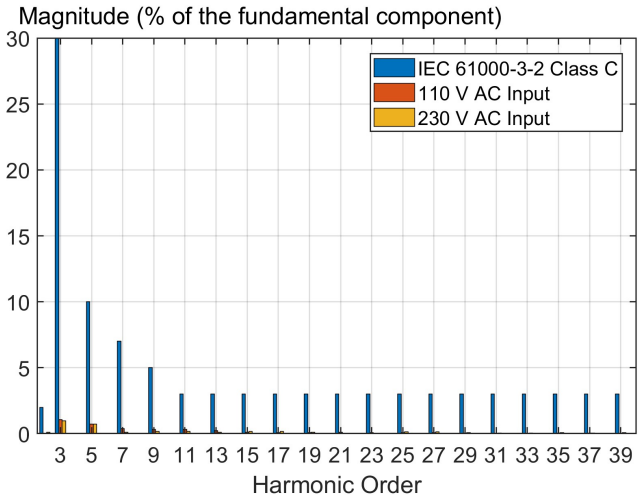


FIGURE 2.25: Harmonic spectrum of the prototype.

A thermal image was captured during a steady-state operation, as shown in Fig. 2.27. The test is based on natural ventilation without any active cooling means. The transformer temperature in the prototype is 62.3 °C and is lower than that of the conventional two-stage solution, which is tested to be higher than 80 °C presented in [27].

2.5.2 Comparison

The conventional single-stage and two-stage solutions are taken as benchmarks to compare the performance with the proposed solution. A recent reference design from the industry, a2-010047 [27], is used as the benchmark to represent the conventional two-stage solution.

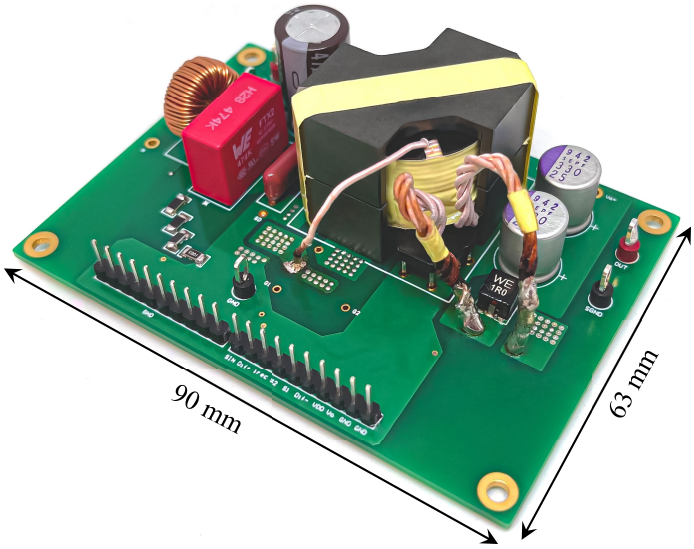


FIGURE 2.26: Hardware implementation. Dimensions: $90 \times 63 \times 26$ mm^3.

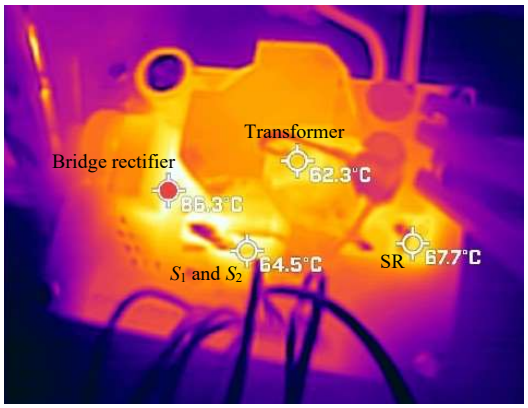


FIGURE 2.27: Thermal image under the steady-state condition of 110 V AC input, 20 V / 5 A output, and 23 °C room temperature.

Another prototype is constructed to represent the conventional single-stage solution. The prototype is reconfigured into the conventional single-stage solution by replacing C_b with a 470 nF film capacitor and increasing C_o by 13200 μF. The conventional and the proposed single-stage ACF solutions are designed for the same average switching frequency. All prototypes follow the same specifications for a fair comparison.

Fig. 2.28 demonstrates the side-by-side comparison of the buffer capacitors used in different solutions, showcasing the significant size reduction of buffer capacitors with the proposed

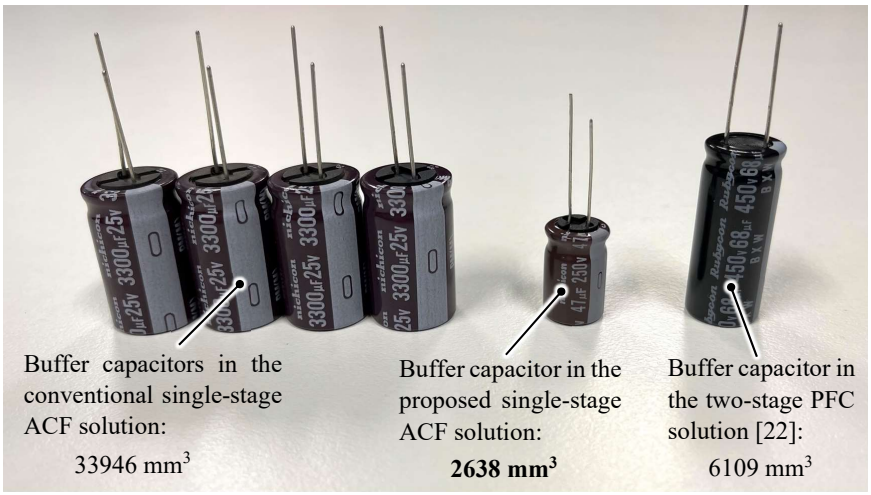


FIGURE 2.28: Comparison of buffer capacitors between the conventional single-stage ACF solution, the proposed solution, and the two-stage solution. Left: buffer capacitor used in the 100 W conventional single-stage ACF solution. Middle: buffer capacitor used in the proposed single-stage ACF solution. Right: buffer capacitor used in a typical 100 W two-stage solution[27].

solution. It should be noted that the output capacitor, C_o, is rated as 13.2 mF in the conventional single-stage solution, which is significantly higher than the capacitance for C_b used in the proposed topology. Fig. 2.29 measures the steady-state waveforms of the conventional single-stage ACF solution and shows that v_o in the conventional single-stage ACF solution contains higher double-line frequency ripple than the proposed solution even though larger buffer capacitors are employed. C_o can be further increased to reduce the double-line frequency ripple in v_o, but the volume of the buffer capacitors may be unpractical for adapter applications. Although the peak of i_D in the proposed ACF solution shows a slight twice-line-frequency ripple, the average value of i_D is constant in steady states.

The conversion efficiency is measured and shown in Fig. 2.30 for the three different solutions. It is shown that the proposed solution can achieve higher efficiency than the conventional two-stage and single-stage solutions over a wide load range. The proposed solution achieves full load efficiency of 92.9 % and 94 % under 110 V and 230 V, respectively. The proposed single-stage solution can achieve higher efficiency than the conventional single-stage topology because the double-line frequency ripple is effectively eliminated from the secondary side. It shows a 25.6 % reduction of RMS current of i_D at the secondary side, as shown in Fig. 2.31,

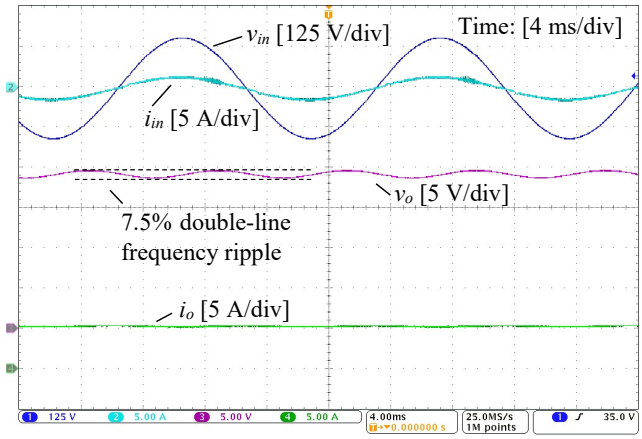


FIGURE 2.29: Steady state waveforms of the conventional single-stage ACF solution (C_o = 13860 μF, C_b = 470 nF).

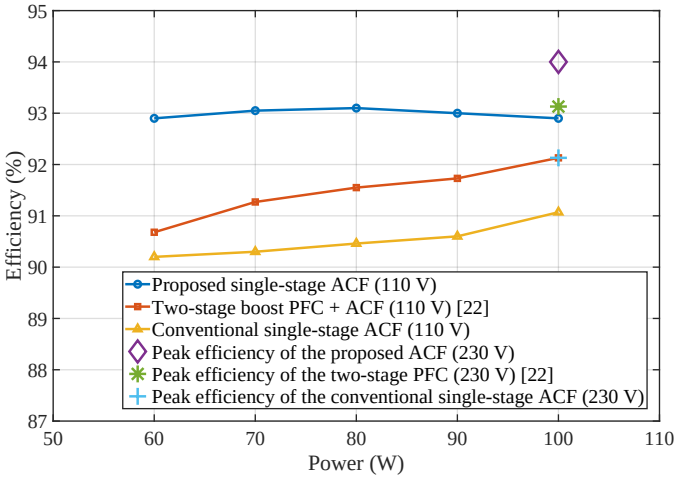


FIGURE 2.30: Efficiency curves.

which explains the efficiency improvement. Table 2.5 summarizes the comparison among the three solutions.

Compared to the conventional two-stage solution, both the proposed single-stage and two-stage solutions achieve the functions of ZCS switching for all diodes, PFC, and galvanic isolation with similar control complexity. However, the proposed solution shows the advantages of ZVS for all MOSFETs, fewer magnetic components, reduced magnetics' volume by 13 %, fewer power semiconductors, reduced buffer capacitor's voltage rating by 44 %, reduced buffer capacitor's energy storage requirement by 79 %, reduced buffer capacitor's

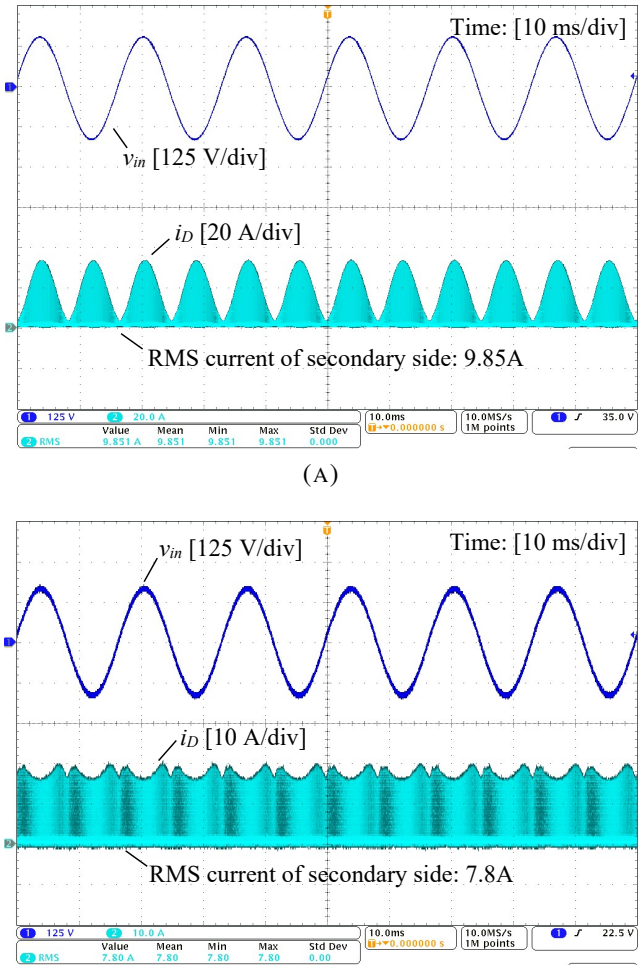


FIGURE 2.31: i_D in (A) the conventional single-stage ACF solution and (B) the proposed single-stage ACF solution.

volume by 57 %, and higher full-load efficiency at 110 V (by 0.8 %). Compared to the conventional single-stage solution, the proposed solution requires one extra controller and voltage sensor, but the proposed solution demonstrates the advantages of lower double-line frequency ripple in v_o, reduced buffer capacitor's energy storage requirement by 64 %, reduced buffer capacitor's volume by 92 %, and higher full-load efficiency at 110 V by 1.8 %.

TABLE 2.5: Comparison between the conventional two-stage solution (boost + ACF), the conventional single-stage solution, and the proposed single-stage ACF solution.

	Two-stage Boost + ACF [27]	Conventional single-stage ACF	Proposed single-stage ACF
Input voltage	$100 \sim 240$ V AC	$100 \sim 240$ V AC	$100 \sim 240$ V AC
Output power	100 W (20 V, 5 A)	100 W (20 V, 5 A)	100 W (20 V, 5 A)
PFC	$\surd$	$\surd$	$\surd$
Elimination of 100/120 Hz ripple	$\surd$	$\times$	$\surd$
Isolation	$\surd$	$\surd$	$\surd$
ZCS for all diodes or SRs	$\surd$	$\surd$	$\surd$
ZVS for all FETs	$\times$	$\surd$	$\surd$
Number of controllers	3	2	3
Number of sensed signals	3	2	3
Number of 650 V FET	3	2	2
Number of secondary diode or SR	1	1	1
Number of magnetics	RM 10×2	RM 12×1	RM 12×1
Volume of magnetics	16472 mm^3	14297 mm^3	14297 mm^3
Total power component count[a]	10	7	7
Voltage rating of buffer capacitor	450 V	25 V	250 V
Volatge ripple of buffer capacitor	2.5 %	7.5 %	20 %
Energy storage of buffer capacitor	6.885 J	4.125 J	1.469 J
Volume of buffer capacitor	6109 mm^3	33946 mm^3	2638 mm^3
Full-load efficiency at 110 V	92.1 %	91.1 %	92.9 %
Full-load efficiency at 230 V	93.1 %	92.1 %	94 %

[a]The EMI filters and the diode bridge are excluded.

2.6 Summary

In this chapter, a new modulation method is proposed for ACF converters in AC–DC adaptor applications. By actively controlling the on-time of both active switches, it has been found that both PFC and active power buffering function can be simultaneously realized without any modification on the topology, which leads to a new single-stage AC–DC solution with significant size reduction of buffer capacitor. The experimental evaluation demonstrates that the new single-stage solution can outperform the conventional two-stage and single-stage solutions in terms of cost, conversion efficiency, and power density.

CHAPTER 3

A High-density PFC Front End

3.1 Background

PFC front end is widely adopted in AC–DC applications to improve power quality. In many of these applications, high power density is desirable [28]–[30]. One of the most widely employed PFC front ends is the boost PFC front end shown in Fig. 3.1. Despite its low cost and high efficiency, the boost PFC front-end is increasingly challenged by the demand for higher power density. Most of its size is occupied by the boost inductor and the buffer capacitor.

To reduce the size of the boost inductor, a critical conduction mode (CRM) of operation is adopted. However, ZVS turn-on cannot be achieved across the universal range of AC voltage [31]. Without soft-switching capability, the efficiency of CRM boost converter can decrease significantly at high-frequency operation even with GaN devices [32]. Consequently, the conventional CRM boost front end typically switches at below 100 kHz, and the size of the boost inductor cannot be further reduced without compromising the efficiency. On the other hand, the buffer capacitor of the boost PFC front end functions as both the DC link and the double-line-frequency energy buffer. The size of the buffer capacitor is typically large due to the need to ensure a low DC-link voltage ripple for the cascading power-processing stage [33].

The totem-pole boost converter is an alternative solution to the PFC front end. Besides reducing the conduction loss of the diode bridge [34], a totem-pole PFC converter can operate efficiently at high frequency across a universal input by adopting ZVS extension control,

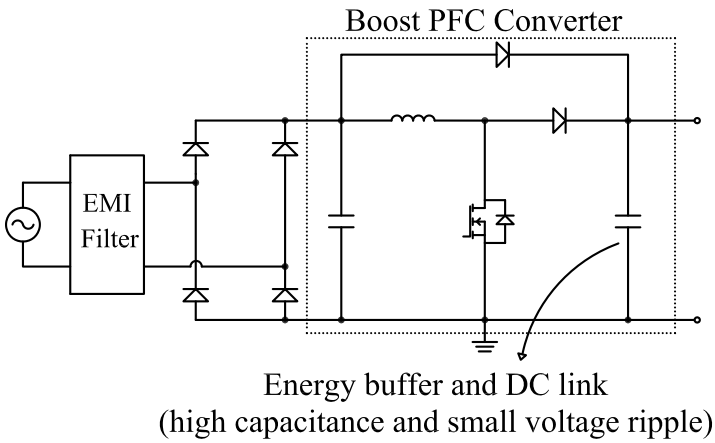


FIGURE 3.1: Conventional boost-based PFC front end

allowing for a much smaller boost inductor design [35]. However, the converter requires a high number of active switches. Extra sensing and control circuits are also needed to detect the zero-crossing of the inductor current and calculate the extended on-time, requiring a relatively expensive micro-controller [36]. Also, a large DC-link capacitor is still mandatory in the totem-pole PFC front end. As a result, the totem-pole PFC converter is usually used in high-power applications (kW-level), where efficiency is of primary concern.

Multilevel boost PFC front end can also reduce the size of the boost inductor by transferring the energy storage burden to the capacitors which usually have much higher energy density than inductors [37], [38]. But the number of switches in the multilevel converters increases proportionally with the voltage levels, leading to high costs. Hence, the multilevel boost PFC front end may not be suitable for low-power and cost-sensitive applications.

Besides reducing the size of the boost inductor, reducing the size of the buffer capacitor is also critical for higher power density in AC–DC systems. Active power buffering is one of the most widely used techniques to reduce the size of the buffer capacitor in an AC–DC system [21], [26], [39]. The idea is to employ a power buffering circuit to decouple the double-line-frequency power from the DC link while directing it to an external energy buffer that can tolerate a greater voltage ripple [40]–[44]. However, existing active power buffering solutions generally focus on capacitance reduction solely and, very often, require the augmentation of extra magnetic energy storage to the original PFC circuits [13]. The size of buffer capacitors

is reduced but at the expense of bigger magnetic components in total. Also, additional active switches are generally required to formulate an active buffer with these switches typically hard-switched, making it even harder to reduce the size of magnetics through high-frequency operation due to the increased power losses. Therefore, it is challenging to achieve simultaneous size reduction of both the magnetics and the buffer capacitor. For example, an extra bidirectional DC–DC converter is connected to the PFC circuit to reduce the buffer capacitance, but an additional inductor is required in the bidirectional power buffering converter, and the original PFC converter remains hard-switched [17], [18]. Similarly, the capacitance in a full-bridge PFC front end can be reduced by inserting an extra inductor and a capacitor into the circuit, adding additional size and cost to the original circuit [45].

In this chapter, a new PFC front-end converter is proposed to improve the power density of the boost PFC front end and achieve simultaneous size reductions of both the magnetics and the buffer capacitors. This is achieved via integrating an active buffering circuit into a conventional boost converter in a way that also allows the original circuit to be soft-switched, creating mutual benefits between the active buffering circuit and the original circuit. The advantages of the proposed converter are summarized as follows:

(1) All switches can achieve ZVS turn-on across the universal input range, allowing for a higher switching frequency operation and thus low magnetic demand in the system.

(2) Active power buffering is achieved, allowing for a smaller energy buffer and an almost constant DC-link voltage, which eases the design of the following power processing stages and mitigates the propagation of the double-line frequency ripple.

(3) Neither expensive MCU nor DSP is needed, and a low-cost analog control is sufficient to operate the proposed topology.

A 100-W universal input prototype is built, which achieves a 96.7% peak efficiency and a power density of 50.8 W/in^3. Compared to a typical CRM boost PFC front end, the prototype achieves a 47% size reduction of the magnetics and a 21% size reduction of the buffer capacitor with a comparable efficiency performance.

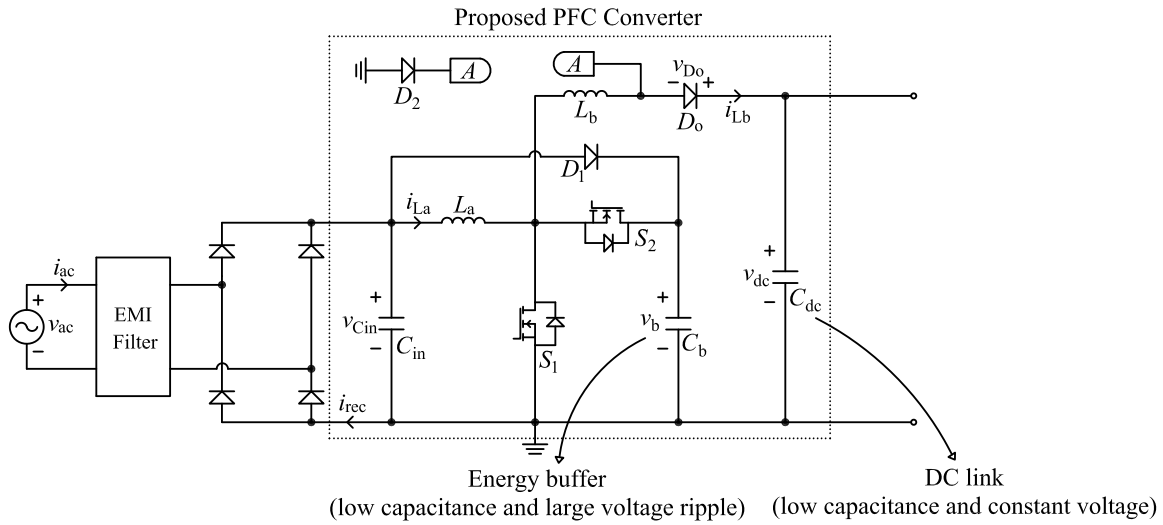


FIGURE 3.2: Proposed topology for PFC front end.

3.2 Topology and Operating Principle

This section presents the proposed topology and analyzes the steady-state operations.

3.2.1 Development of the Proposed Topology

The bulky buffer capacitor in the conventional boost PFC solution is the main constraint for size reduction. Another is the lack of soft switching to increase switching frequency. Thus, the proposed PFC converter is developed and shown in Fig. 3.2.

The proposed PFC converter consists of two inductors, L_a and L_b. S_1 provides input current shaping capability (i.e., input power regulation) similar to the low-side switch in a boost PFC converter. S_2 provides additional control freedom to regulate the DC-link voltage v_{dc} (i.e., output power regulation). Hence, the proposed topology can regulate both its input power and output power independently by controlling the switching actions of S_1 and S_2. As a result, C_b can be operated as an active energy buffer while C_{dc} only receives constant power without any double-line-frequency ripple power. Such a feature allows for an increased voltage ripple over v_b, leading to a reduced twice-line energy buffer's size while achieving a constant voltage for v_{dc}. It should be noted that this is impossible in the conventional boost

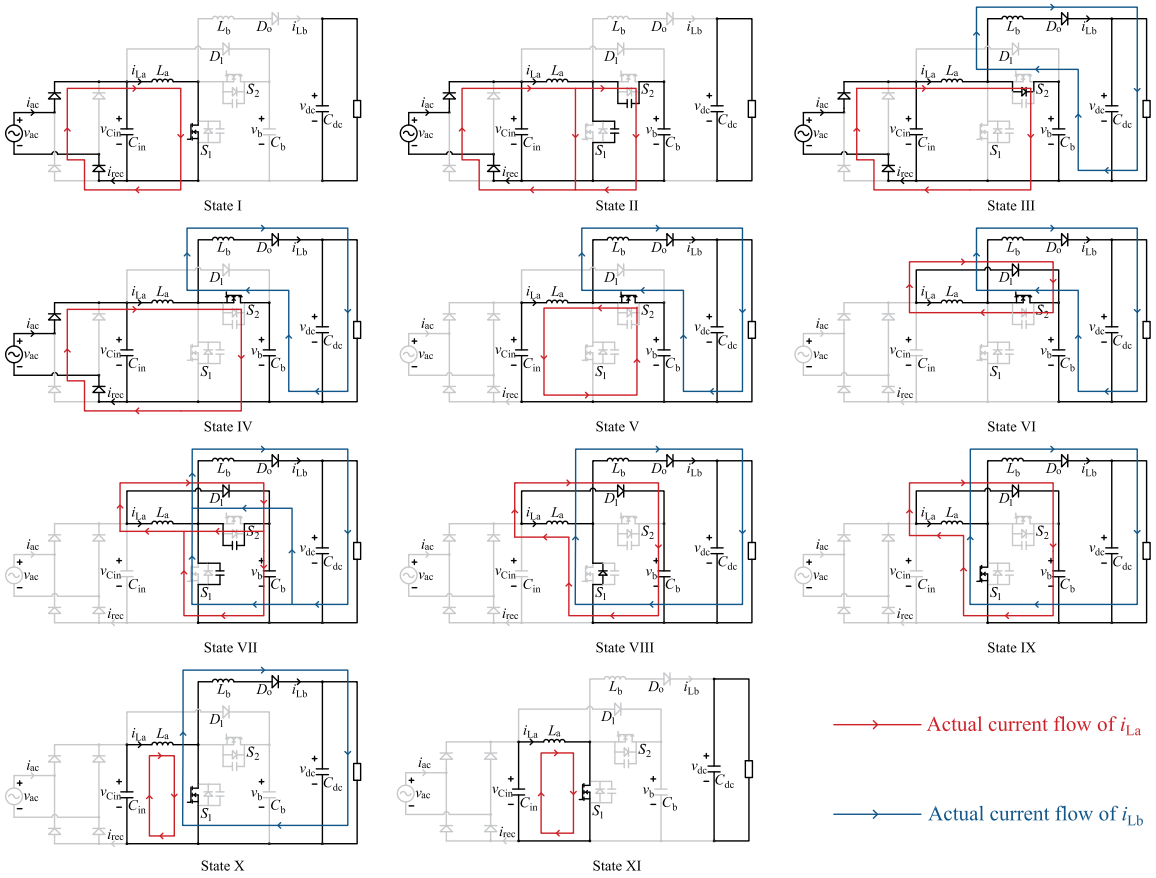


FIGURE 3.3: Operating states of the proposed converter.

PFC converter, where reducing buffer capacitance will compromise the DC-link voltage ripple. Meanwhile, the energy stored in L_b can be used to discharge the output capacitance of S_1, allowing universal-input-range ZVS and size reductions of magnetics through high-frequency operations. This is also impossible in the conventional CRM boost PFC converter, where ZVS is lost at high-line conditions. The output diode, D_o, is used to block the reversed power flow from C_{dc}. The auxiliary diode D_1 is included for inrush current bypassing and voltage clamping. Another auxiliary diode D_2 is adopted for voltage clamping.

3.2.2 Operating Principle

The steady-state operation includes 11 states, which can be identified by the equivalent circuit, as shown in Fig. 3.3. The definition follows the steady-state waveform in Fig. 3.4. The operation is elaborated as follows.

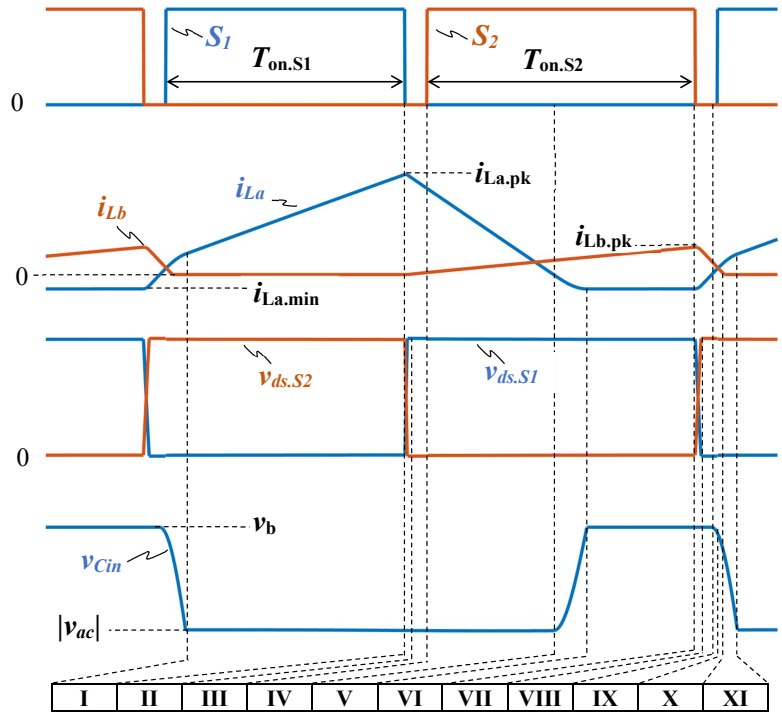


FIGURE 3.4: Detailed waveforms of the proposed converter. $v_{ds.S1}$ and $v_{ds.S2}$ are the drain-source voltage of S_1 and S_2.

State I: L_a is charged by $|v_{ac}|$ via the conduction of S_1 and a pair of diodes.

State II: S_1 is turned off and causes i_{La} to discharge the output capacitance of S_2 and to charge the output capacitance of S_1.

State III: The body diode of S_2 is forward-biased. S_2 is ready for the ZVS turn-on. L_b is charged by v_b, causing i_{Lb} to increase with a slope of (v_b-v_{dc})/L_b. Although the blue current is passing through the body diode of S_2 in a reversed direction, the net current passing through the body diode is still along its forward biasing direction because i_{La} is greater than i_{Lb} at this state.

State IV: S_2 turns on with ZVS. i_{La} decreases while i_{Lb} increases, and they cancel each other in S_2, which reduces the current stress of S_2.

State V: i_{La} reaches zero, and the diode bridge turns off with ZCS. i_{La} starts to flow reversely and charges C_{in}, resulting in a rising v_{Cin}.

State VI: The forward bias of D_1 clamps v_{Cin} at the level of v_b. The energy stored in C_{in}, $0.5C_{in}v_b^2$, can be controlled by designing C_{in}, and is released back to L_a to realize the ZVS turn-on of S_2 in State II. i_{La} circulates within the loop formed by L_a, D_1, and S_2. The minimum value of i_{La} in each switching state can be calculated by (3.1). Since the energy to achieve ZVS turn-on of S_1 is mainly from L_b rather than L_a, there is no need to have a dedicated controller to sense and control $i_{La.min}$, which allows a simple and cost-effective control scheme. It should be noted that many existing soft-switching PFC converters usually need expensive digital controllers and high-speed sensing circuits to adjust the switch timing and detect the zero-crossing of inductor current to achieve ZVS, which increases cost and complexity. Moreover, the energy to achieve ZVS turn-on of S_1 is mainly sourced from L_b rather than L_a. As a result, ZVS of S_1 can still be achieved at the peak of v_{ac} under the high-line condition as shown in the experimental section.

$$i_{La.min} = -\sqrt{\frac{C_{in}(v_b^2 - 2v_b|v_{ac}|)}{L_a}}. \tag{3.1}$$

State VII: S_2 is off. i_{La} and i_{Lb} discharge the output capacitance of S_1 together while charging the output capacitance of S_2.

State VIII: the body diode of S_1 conducts after the output capacitance of S_1 is fully discharged. S_1 is ready for ZVS turn-on.

State IX: S_1 turns on with ZVS. i_{La} starts to increase with a slope of (v_b/L_a) to approach the zero level. i_{Lb} decreases with a slope of $(-v_{dc}/L_b)$.

State X: When i_{La} reaches zero and turns positive, D_1 turns off with ZCS. C_{in} starts to charge L_a. Thus, the level of i_{La} continues to increase with a slope of (v_{Cin}/L_a). The diode bridge remains off until v_{Cin} is discharged to the level of $|v_{ac}|$. On the other hand, i_{Lb} decreases to approach the zero current level.

State XI: i_{Lb} reaches zero and D_o is off with ZCS. The DC-link voltage is maintained by C_{dc}. The bridge rectifier remains off until v_{Cin} reduces to $|v_{ac}|$. It marks the last state of the switching cycle. Then, the operation enters State I and repeats the 9 states.

3.2.3 Circuit Analysis

Mathematical expressions of key circuit parameters such the switching period T_{sw}, $T_{on.S2}$, $T_{on.S1}$, and peak inductor currents are derived to assist the design of the proposed converter. The dead-time and the parasitic capacitance are neglected to simplify the derivation. Assuming that C_{in} is zero, the peak inductor current of L_a can be calculated as

$$i_{La.pk} = \frac{|v_{ac}|T_{on.S1}}{L_a}, \tag{3.2}$$

where $T_{on.S1}$ refers to the on-time of S_1. Similarly, the peak inductor current of L_b can be calculated as

$$i_{Lb.pk} = \frac{(v_b - v_{dc})T_{on.S2}}{L_b}, \tag{3.3}$$

where $T_{on.S2}$ denotes the on-time of S_2. The time required to reset i_{La} and i_{Lb} from their peak values to zero can be calculated as

$$T_{down.La} = \frac{i_{La.pk}L_a}{v_b - |v_{ac}|} \tag{3.4}$$

and

$$T_{down.Lb} = \frac{i_{Lb.pk}L_b}{v_{dc}}, \tag{3.5}$$

respectively. The average values of i_{La} and i_{Lb} are the input and output current respectively, so we have the following two equations:

$$|i_{ac}| = \frac{i_{La.pk}(T_{on.S1} + T_{down.La})}{2T_{sw}} \tag{3.6}$$

and

$$i_{dc} = \frac{i_{Lb.pk}(T_{on.S2} + T_{down.Lb})}{2T_{sw}}, \tag{3.7}$$

where i_{dc} is the output current.

Combining (3.2), (3.3), (3.4), (3.5), (3.6), and (3.7), the analytical expressions of key circuit variables are derived as summarized as follows.

$$\begin{aligned} T_{sw} =& \frac{4\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}}{|v_{ac}|v_b^2(v_b-v_{dc})} \\ &- \frac{2|i_{ac}|L_av_b(|v_{ac}|-v_b)(v_b-v_{dc})+2L_bP_o|v_{ac}|v_b}{|v_{ac}|v_b^2(v_b-v_{dc})} \end{aligned} \tag{3.8}$$

$$T_{on.S1} = \frac{2(\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}-|i_{ac}|L_av_b(|v_{ac}|-v_b)(v_b-v_{dc}))}{|v_{ac}|v_b^2(v_b-v_{dc})} \tag{3.9}$$

$$T_{on.S2} = \frac{2\left(\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}+L_bP_o|v_{ac}|v_b\right)}{|v_{ac}|v_b^2(v_b-v_{dc})} \tag{3.10}$$

$$T_{down.La} = \frac{2\left(\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}-|i_{ac}|L_av_b(|v_{ac}|-v_b)(v_b-v_{dc})\right)}{v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})} \tag{3.11}$$

$$T_{down.Lb} = \frac{2\left(\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}+L_bP_o|v_{ac}|v_b\right)}{|v_{ac}|v_b^2v_{dc}} \tag{3.12}$$

$$i_{La.pk} = \frac{2|i_{ac}|L_bP_o|v_{ac}|(v_b-|v_{ac}|)}{\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}}+|i_{ac}|\left(2-\frac{2|v_{ac}|}{v_b}\right) \tag{3.13}$$

$$i_{Lb.pk} = \frac{2\left(\sqrt{|i_{ac}|L_aL_bP_o|v_{ac}|v_b^2(v_b-|v_{ac}|)(v_b-v_{dc})}+L_bP_o|v_{ac}|v_b\right)}{L_b|v_{ac}|v_b^2} \tag{3.14}$$

3.2.4 Impact of L_b on Power Density

While the proposed PFC front end can achieve soft switching across the universal range, the possible size reduction of magnetic components through high-frequency operation may be hindered by L_b, which is not presented in the conventional boost PFC front end. This section analyzes the impact of L_b on power density.

L_a works the same way as the inductor of the CRM/DCM boost converter and the magnetic energy storage of L_a can be calculated as

$$\begin{aligned} E_{boost} &= \frac{1}{2} L_a i_{La.pk}^2 \\ &= P_{boost} T_{sw} (1 - \frac{v_{in.boost}}{v_{o.boost}}), \end{aligned} \tag{3.15}$$

where $i_{La.pk}$ is the peak i_{La} per switching cycle, T_{sw} is the switching period, P_{boost} is the power handled by the boost converter, $v_{in.boost}$ is the input voltage of the boost converter (i.e., $|v_{ac}|$ in the proposed converter), and $v_{o.boost}$ is the output voltage of the boost converter (i.e., v_b in the proposed converter). In a universal AC–DC application, the maximum energy storage of L_a happens under the low-line condition and is calculated to be $1.39 P_o T_{sw}$.

The function of L_b in the proposed topology is equivalent to the conventional buck inductor operated by the DCM/CRM. Thus, its magnetic energy storage can be calculated as

$$\begin{aligned} E_{buck} &= \frac{1}{2} L_b i_{Lb.pk}^2 \\ &= P_{buck} T_{sw} (1 - \frac{v_{o.buck}}{v_{in.buck}}), \end{aligned} \tag{3.16}$$

where $i_{Lb.pk}$ is the peak i_{Lb} within each switching cycle, P_{buck} is the power handled by the buck converter, $v_{in.buck}$ is the input voltage of the buck converter (i.e., v_b in the proposed converter), and $v_{o.buck}$ is the output voltage of the buck converter (i.e., v_{dc} in the proposed converter and v_{dc} is designed at constant 380 V in this work). Detailed derivations of the maximum magnetic energy storage of boost and buck converters are in the Appendix.

The maximum energy storage of L_b, $E_{buck.max}$, occurs when v_b reaches the peak, which is around 410 V in our design, so $E_{buck.max}$ is calculated to be $0.07P_oT_{sw}$, which is low. The main reason for the low energy storage requirement of L_b is that v_b and v_{dc} are purposely designed at similar voltage levels. The ratio between the magnetic energy storage in the proposed PFC front end and the magnetic energy storage in the conventional boost PFC front end can therefore be calculated as

$$k_{mag} = \frac{E_{boost.max} + E_{buck.max}}{E_{boost.max}} \approx 1.05. \tag{3.17}$$

From (3.17), the proposed PFC front end requires 5 % more magnetic energy storage than the conventional boost PFC front end if both are working at the same frequency. This disadvantage can be easily offset by the universal-range ZVS feature of the proposed topology, which allows a much higher switching frequency than the convention boost PFC front end without compromising the switching loss. As a result, L_b will not be a barrier towards higher power density.

3.2.5 Comparison of Electrical Energy Storage

This subsection compares the electrical energy storage between the proposed converter and the conventional boost PFC converter to show the advantages of the proposed converter, including smaller DC-link voltage ripple and lower required electrical energy storage. The electrical energy storage of the proposed converter can be calculated as

$$E_{C.proposed} = E_{C_{dc}} + E_{C_b}, \tag{3.18}$$

where $E_{C_{dc}}$ is the electrical energy storage of C_{dc}, and E_{C_b} is the electrical energy storage of C_b. The function of C_{dc} of the proposed topology is to perform high-frequency filtering, limiting the high-frequency ripple to a given level. The required electrical energy storage of C_{dc} can be calculated as

$$\begin{aligned} E_{C_{dc}} &= \frac{1}{2} C_{dc} v_{dc}^2 \\ &= \frac{v_{dc} P_o T_{sw}}{2 \triangle v_{dc}} \end{aligned} \tag{3.19}$$

where T_{sw} is the switching period, P_o is the output power, and $\triangle v_{dc}$ is the voltage ripple on C_{dc}. C_b buffers the double-line-frequency ripple power, and the electrical energy storage of C_b can be calculated as

$$\begin{aligned} E_{C_b} &= \frac{1}{2} C_b V_{b.max}^2 \\ &= \frac{1}{2} C_b V_b^2 + \frac{P_o T_l}{4\pi}, \end{aligned} \tag{3.20}$$

where $V_{b.max}$ is the maximum value of v_b, V_b is the average voltage of v_b, and T_l is the line period.

The electrical energy storage of the conventional boost PFC converter can be calculated as

$$E_{C.boost} = \frac{1}{2} {C_b}^* {V_b^*}^2 + \frac{P_o T_l}{4\pi}, \tag{3.21}$$

where ${C_b}^*$ is the buffer capacitance of the conventional boost PFC converter, and ${V_b}^*$ is the average buffer voltage or DC-link voltage of the conventional boost PFC converter.

Assuming $v_{dc} = V_b^*$ = 380 V, V_b = 400 V, C_b = 33 μF, C_b^* = 68 μF, T_{sw} = 2.5 μs, P_o = 100 W, and $\triangle v_{dc}$ = 2 V, $E_{C.proposed}$ is calculated to be 2.79 J, and $E_{C.boost}$ is calculated to be 5.04 J. Thus, the ratio of electrical energy storage k_{cap} between the proposed converter and the conventional boost converter is

$$k_{cap} = \frac{E_{C.proposed}}{E_{C.boost}} \approx 0.55. \tag{3.22}$$

According to (3.22), the proposed PFC converter reduces the electrical energy storage by 45 % via reducing the buffer capacitance from 68 μF to 33 μF. Meanwhile, the proposed converter can also achieve 80 % less DC-link voltage ripple as shown in Fig. 3.5 despite the electrical energy storage is reduced in the proposed converter. The above analysis demonstrates that the

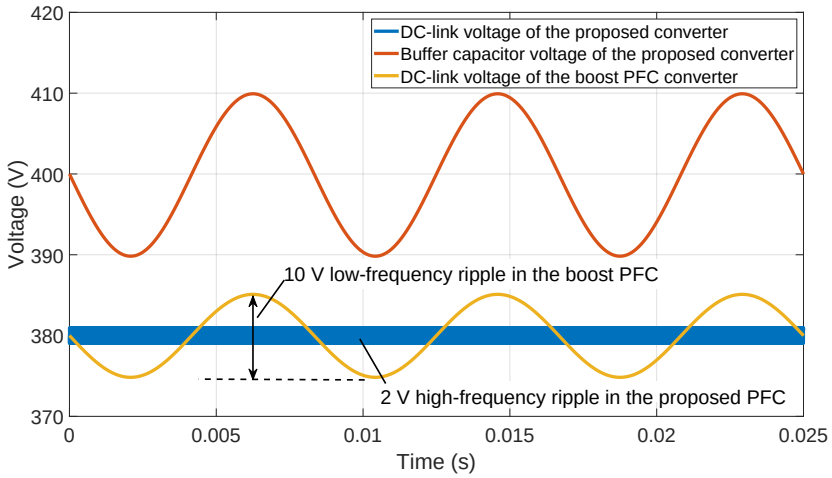


FIGURE 3.5: Waveforms of DC-link voltage in the proposed converter and the conventional boost PFC converter (C_b = 33 μF, C_b^* = 68 μF). The proposed converter can achieve a lower DC-link voltage ripple than the conventional boost PFC converter while requiring lower capacitance.

proposed converter can achieve lower DC-link ripple while requiring less electrical energy storage than the conventional boost PFC converter.

3.3 Design Considerations

This section discusses the practical design considering the effects of parasitics, circuit parameters design, ZVS range discussion, controller implementation, and common-mode noise.

3.3.1 Effects of Parasitic Capacitance and D_2

The auxiliary diode D_2 is ignored in the previous analysis, but D_2 is essential to clamp the voltage stress of D_o when the parasitic capacitance of D_o is considered. Fig. 3.6 illustrates the operating waveforms of i_{Lb} and v_{do} when the parasitic capacitance of D_o is 10 pF. Oscillations between the parasitic capacitance and L_b can be observed when D_2 is reverse-biased. The oscillations increase the voltage stress of D_o to over 600 V and introduce EMI noises. The feature of D_2 is to clamp the voltage stress of D_o at v_{dc}. Fig. 3.6 indicates that the oscillation is eliminated by D_2. It is noted that i_{Lb} can go negative due to the parasitic capacitance, and

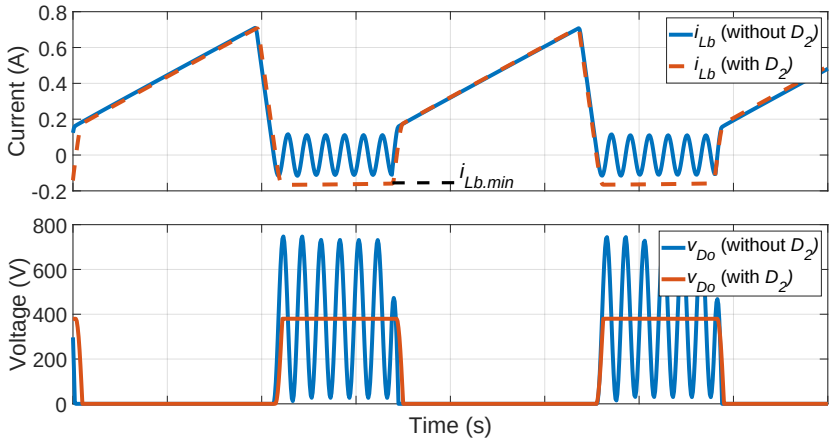


FIGURE 3.6: Operating waveforms with and without D_2 considering 10 pF parasitic capacitance of Do.

the minimum i_{Lb} can be calculated as

$$i_{Lb.min} = -v_{dc}\sqrt{\frac{C_{D_o} + C_{D_2}}{L_b}}, \tag{3.23}$$

where C_{D_o} and C_{D_2} are the parasitic capacitance of D_o and D_2. From (3.23), $i_{Lb.min}$ does not scale with the power level, which is not a barrier for higher power applications. The negative i_{Lb} will circulate within the loop formed by L_b, S_1, and D_2, leading to slightly increased conduction loss in D_2. Assuming 20 pF for $(C_{D_o} + C_{D_2})$, 380 V for v_{dc}, 100 μH for L_b, 1 V forward voltage for D_2, and $i_{Lb.min}$ continuously flows through D_2, the conduction loss of D_2 in the worst case is estimated to be 0.17 W based on (3.23), corresponding to a 0.17% efficiency reduction for a 100 W PFC converter. Thus, the effects of D_2 and parasitic capacitance on the system efficiency are negligible.

3.3.2 Design of C_b

The design target of the buffer capacitor is to reduce its size but maintain sufficient hold-up time. The average value of v_b is designed at 400 V to enable the converter to work across the universal input range. The minimum capacitance required can be calculated as

$$C_{b.min} = \frac{2P_oT_{hold}}{V_b^2 - V_{min}^2}, \tag{3.24}$$

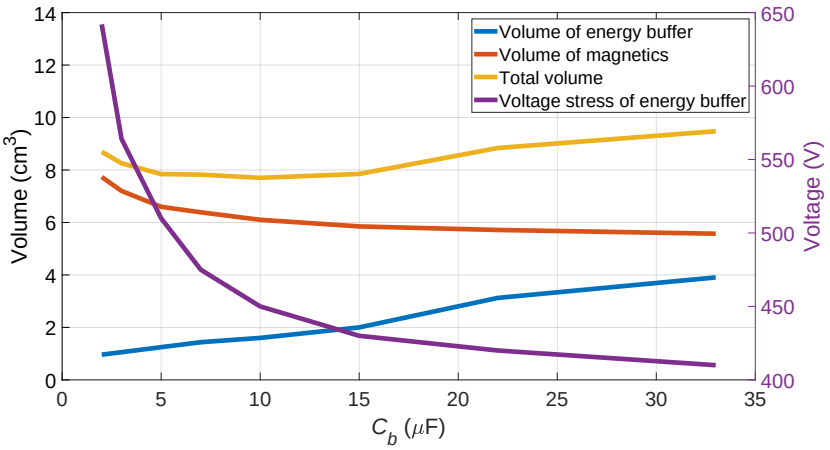


FIGURE 3.7: Volume of magnetics and energy buffer versus C_b for a 100-W prototype. Lower C_b leads to higher voltage stress, smaller energy buffer, and bigger magnetics. The volume of the energy buffer capacitor is calculated based on existing electrolytic capacitors from Rubycon. The volume of magnetics is calculated assuming 0.065 μJ/mm^3 energy density and 400 kHz switching frequency.

where T_{hold} is the hold-up time, V_b is the average voltage of C_b, and V_{min} is the minimum buffer voltage without interrupting the next stage. Furthermore, the minimum v_b, $V_{b.min}$, must be higher than v_{dc} to ensure the proper operation of the proposed circuit. $V_{b.min}$ can be calculated as

$$V_{b.min} = \sqrt{V_b^2 - \frac{P_o}{\omega_l C_b}}, \tag{3.25}$$

where ω_l is the angular frequency of the AC voltage, which is 100π rad/s for 50 Hz input and 120π rad/s for 60 Hz input. For 10-ms T_{hold}, 100-W P_o, 400-V V_b, 380-V v_{dc}, and 300-V V_{min}, $C_{b.min}$ is calculated to be 28 μF and an off-the-shelf 33 μF 450 V electrolytic capacitor is selected in the prototype.

It is noticed that C_{dc} can also be increased to provide the hold-up time. However, doing so will increase the volume of the overall system. Since C_b is the key energy storage component in the proposed system, C_b can be directly used to provide the hold-up energy required without increasing the system's volume.

If the hold-up time is not required, the buffer capacitor can be further shrunk by reducing C_b and increasing its voltage ripple. However, reducing C_b also leads to higher voltage stress of C_b and thus larger energy storage requirement of magnetics as per (3.15) and (3.16).

Therefore, there exists an optimal value of C_b that results in the highest power density. Fig. 3.7 estimates the size of magnetics and energy buffer under different C_b for a 100-W design, and the optimal C_b is found to be around 10 μF, corresponding to V_b = 423 V.

3.3.3 Design of L_a and L_b

The design targets of L_a and L_b are: 1. to reduce the size of magnetics by switching at a much higher frequency than the conventional CRM boost converter and 2. to improve the energy storage utilization of magnetics by ensuring L_a to work in DCM.

The design process starts with determining the switching frequency f_{sw} when v_{ac} reaches its peak under the low-line condition, and the maximum energy storage occurs. Then, L_a is designed to ensure its DCM operation at f_{sw}. The critical inductance to ensure DCM operation of L_a at f_{sw} can be calculated as

$$L_{a.crit} = \frac{V_{ac.min}^2(V_b - |V_{ac.min}|)}{4P_o f_{sw} V_b}, \tag{3.26}$$

where $V_{ac.min}$ is the minimum amplitude of v_{ac}. L_a should be designed smaller than $L_{a.crit}$ to guarantee DCM operation. After that, L_b can be calculated by substituting f_{sw} and L_a into (3.8). It should be noted that (3.8) is derived without considering the parasitics and power losses, and the design procedure above only leads to a preliminary design. Finally, L_b and L_a should be finely tuned based on simulations and experiments to match the design targets.

3.3.4 Design of C_{in}

The capacitance of C_{in} should be determined to allow S_2 to achieve ZVS even at the zero-crossing of v_{ac}. As analyzed above, i_{La} should be sufficiently high to achieve the ZVS turn-on of S_2. However, during the zero-crossing of v_{ac}, i_{La} is near zero since there is no power from v_{ac}, and S_2 will lose the ZVS turn-on. The capacitance of C_{in} should be designed to be sufficient to assist the ZVS turn-on of S_2 during the zero-crossing of v_{ac}. The energy stored in C_{in} is calculated as $0.5C_{in}v_b^2$, to charge L_a when S_1 is on and i_{La} should be high enough

to fully discharge the output capacitance of S_2. Assuming that all of the energy stored in C_{in} is transferred to L_a when S_1 is on and v_{ac} = 0 V, the energy balance is expressed by

$$\frac{1}{2}C_{in}v_b^2 = \frac{1}{2}L_a i_{La.max}^2, \tag{3.27}$$

where $i_{La.max}$ denotes the maximum i_{La} per switching cycle. A state-plane trajectory analysis may provide more accurate results than (3.27) [46], [47]. The minimum $v_{ds.S_2}$ should be lower than zero to guarantee the ZVS turn-on of S_2, so combining (3.30) and (3.27), the minimum capacitance of C_{in} can be calculated as

$$C_{in.min} = 2C_{oss}. \tag{3.28}$$

3.3.5 ZVS Range Analysis

This subsection analyzes the range of ZVS. The equivalent resonant circuits of ZVS transitions of S_1 and S_2 can be approximated as shown in Fig. 3.8 (a) and (b). The drain-source voltage of S_1 and S_2 can be derived accordingly as (3.29) and (3.30), respectively.

$$\begin{aligned} v_{ds.S_1} = &- i_{Lb.pk}\sqrt{\frac{L_b}{2C_{oss}}}sin\big(\frac{1}{\sqrt{2L_bC_{oss}}}t\big) + v_b \\ &+ v_{dc} - v_{dc}cos\big(\frac{1}{\sqrt{2L_bC_{oss}}}t\big) \end{aligned} \tag{3.29}$$

$$\begin{aligned} v_{ds.S_2} = &|v_{ac}|cos\big(\frac{1}{\sqrt{2L_aC_{oss}}}t\big) - |v_{ac}| + v_b \\ &- i_{La.pk}\sqrt{\frac{L_a}{2C_{oss}}}sin\big(\frac{1}{\sqrt{2L_aC_{oss}}}t\big) \end{aligned} \tag{3.30}$$

C_{oss} is the output capacitance of S_1 and S_2. The ZVS range can therefore be derived by checking the minimum values of $v_{ds.S1}$ and $v_{ds.S2}$ under different v_{ac}, v_b, and power level. A key fact from (3.29) and (3.30) is that the minimum drain-source voltages are mainly

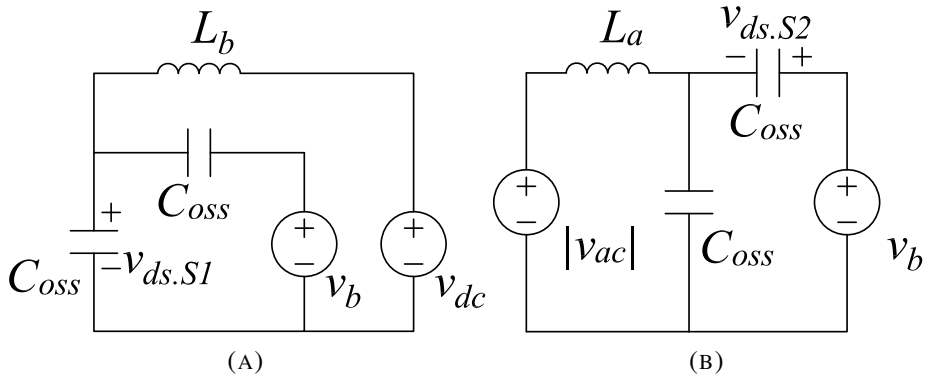
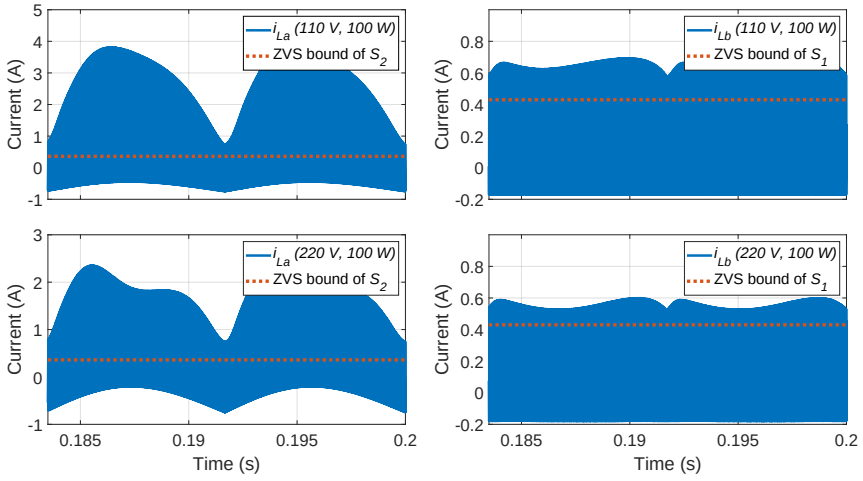


FIGURE 3.8: Approximate resonant circuit during the ZVS transition of S_1 and S_2. (A) i_{Lb} is discharging the output capacitance of S_1 while charging the output capacitance of S_2. (B) i_{La} is discharging the output capacitance of S_2 while charging the output capacitance of S_1.

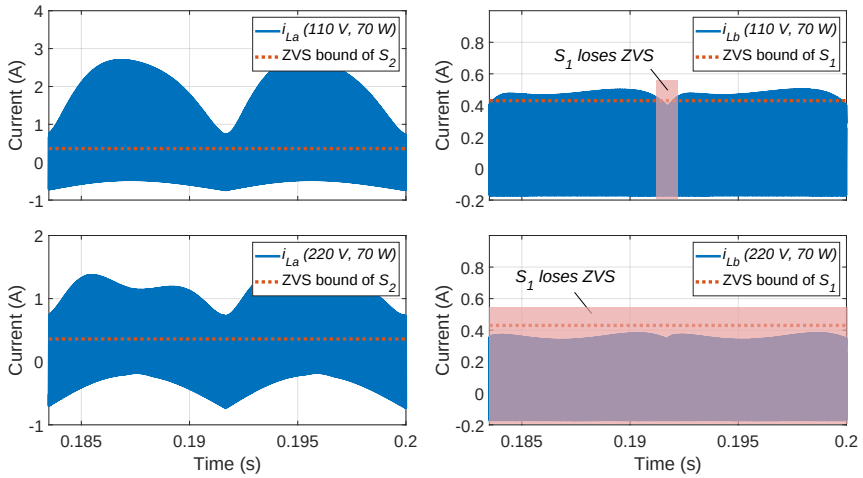
determined by the peak inductor currents, which reduce at a lighter load. Hence, ZVS can be lost under light-load operations, reducing the efficiency at lower power levels.

The ZVS ranges under different input voltage and load power are plotted in Fig. 3.9. Fig. 3.9 (a) shows that the proposed topology can achieve full-range ZVS at a universal input under the full-load condition. Particularly, the topology can achieve full-range ZVS at 100 W, as the peak currents of i_{La} and i_{Lb} are both greater than the minimum required current (i.e., around 0.4 A) to realize ZVS of S_1 and S_2 throughout the complete line period under both 110 V and 220 V AC input. However, S_1 starts to lose ZVS at around 70 W as there exists an interval where the peak of i_{Lb} becomes less than 0.4 A as shown in Fig. 3.9 (b), resulting in reduced efficiency at lower power levels. Another observation from Fig. 3.9 (b) shows that the proposed topology is prone to lose ZVS at high line conditions as the red region is larger under 220 V AC, which is similar to many other PFC converters, such as CRM boost converter or Totem-pole converters.

Possible solutions to extend the ZVS range of the proposed converter include (1) redesigning of the circuit parameters to ensure ZVS operation throughout the desired operating range and (2) burst mode operation. Fig. 3.10 presents the relationship between L_b and the ZVS range, showing that increasing L_b can extend the ZVS range. However, the trade-off between power density and the ZVS range should be considered. For example, to extend the ZVS boundary



(A)



(B)

FIGURE 3.9: ZVS range under different AC voltages and power levels. The regions where ZVS is lost are highlighted in red. L_a is 50 μH and L_b is 100 μH. (A) Simulated waveforms of i_{La} and i_{Lb} under 110 V and 220 V inputs at 100 W. ZVS of switches can be achieved as $i_{La.pk}$ and $i_{Lb.pk}$ are higher than the ZVS boundaries plotted in dashed lines. (B) Simulated waveforms of i_{La} and i_{Lb} under 110 V and 220 V inputs at 70 W. The ZVS of S_1 is lost when $i_{Lb.pk}$ is lower than the ZVS boundary of S_1.

from around 50 W to 20 W, a 5 times increase of the effective core area of L_b is required given the same window area, current density, and flux density, which may not be worthwhile considering its system-level benefits.

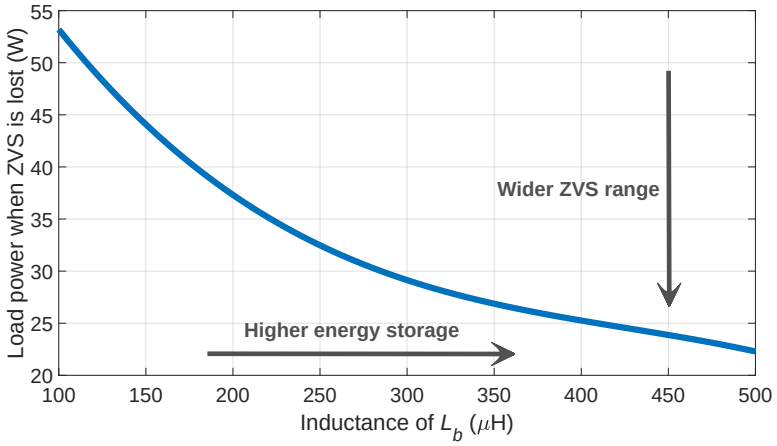


FIGURE 3.10: The relationship between L_b and ZVS range. The figure is plotted using the same specifications and circuit parameters as in Table. 3.1 and 3.2.

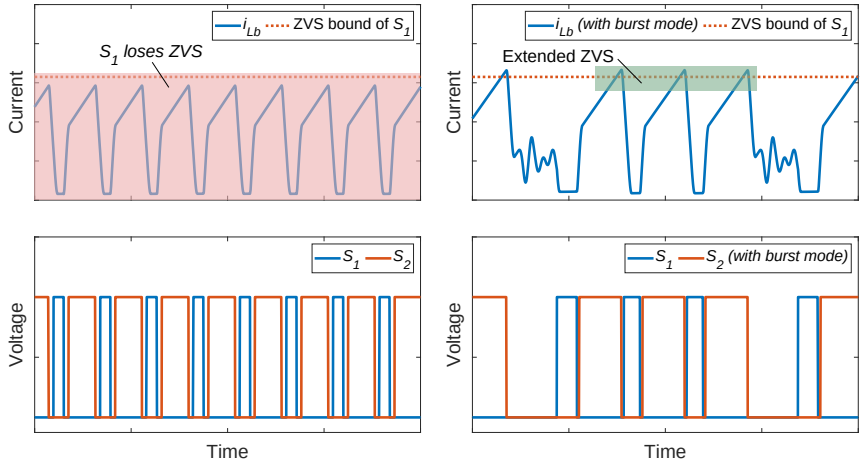


FIGURE 3.11: ZVS extension through the burst-mode operations. Left: simulated waveforms under the normal-mode operations. Right: simulated waveforms under the burst-mode operations. Both cases are measured at 220-V AC input and 70-W output, and the circuit parameters are the same as the hardware prototype in the experimental section.

For high power density, the design of circuit parameters should focus on optimizing the efficiency around the full-load condition at which the maximum power losses usually occur rather than solely focusing on the ZVS range under normal-mode operations, given that there exist many other approaches to improve light-load efficiency without greatly compromising power density. For example, burst-mode operations can also improve the light-load efficiency performance. Fig. 3.11 compares the operating waveforms of the proposed topology under normal-mode and burst-mode operations (where additional blank time is inserted between

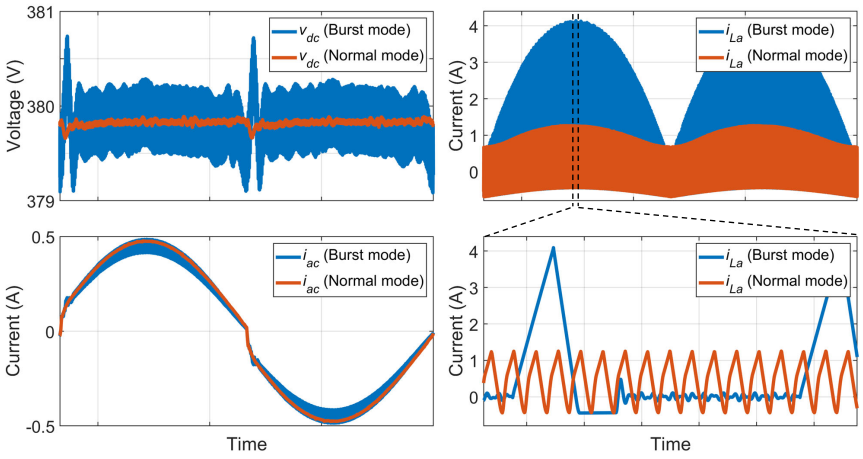


FIGURE 3.12: Comparison of waveforms between the normal-mode operations and burst-mode operations (30 W output, 110 V AC). The parameters used to simulate the waveforms are the same as the hardware prototype in the experimental section. The average switching frequency is reduced after using the burst mode operations. Higher ripple occurs as a trade-off for lower switching frequency and the corresponding switching-related losses.

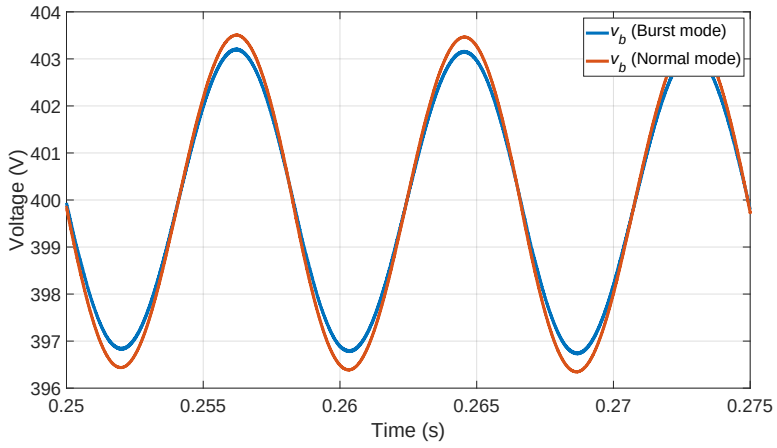


FIGURE 3.13: Comparison of v_b between the burst-mode operations and normal-mode operations (30 W output, 110 V AC). The ripple of v_b under burst-mode operations is lower than that under normal-mode operations because the burst-mode operations improve efficiency and reduce the 120 Hz ripple power.

every two groups of pulses), given identical circuit parameters and operating conditions. It can be seen that burst-mode operations can reduce the switching frequency and increase $i_{Lb.pk}$, effectively extending the ZVS range of the proposed system.

It should be noted that burst-mode operation may increase the output ripple and input current distortion due to reduced operating frequency, as shown in Fig. 3.12, which should be

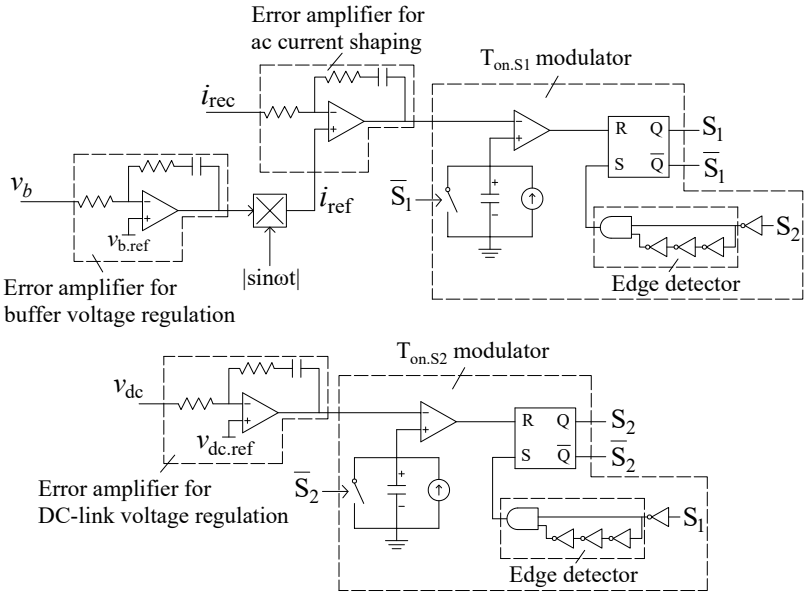


FIGURE 3.14: Implementation of the control circuit.

considered when sizing the filters [48], [49]. However, the ripples are still relatively low in the burst-mode operations even though the switching frequency is reduced by more than 10 times in Fig. 3.12. The reason is that the ripple power is inherently lower at light-load conditions, compensating for the increase of ripple due to the burst-mode operations. Also, it is found that burst-mode operations can even decrease the ripple of v_b as shown in Fig. 3.13 because the burst-mode operations improve efficiency and hence reduce the 100/120 Hz ripple power.

3.3.6 Control Circuit

Fig. 3.14 illustrates the control circuit, which is specially designed for the proposed topology. $T_{on.S1}$ is used to shape the AC current i_{rec} to follow a sinusoidal reference i_{ref}. The regulation of v_b is done by a dedicated error amplifier which adjusts the amplitude of i_{ref}. The voltage regulation of v_{dc} is achieved by modulating $T_{on.S2}$ so that v_{dc} follows the reference signal, $v_{dc.ref}$. The on-state of S_2 increases the level of v_{dc} while the off-state of S_2 prevents C_b from charging L_b and C_{dc}, so $T_{on.S2}$ can be used to regulate v_{dc}. The on/off switching of S_1 and S_2 is realized by their respective modulators, which ensure the complementary operations of S_1 and S_2 with enough dead-time.

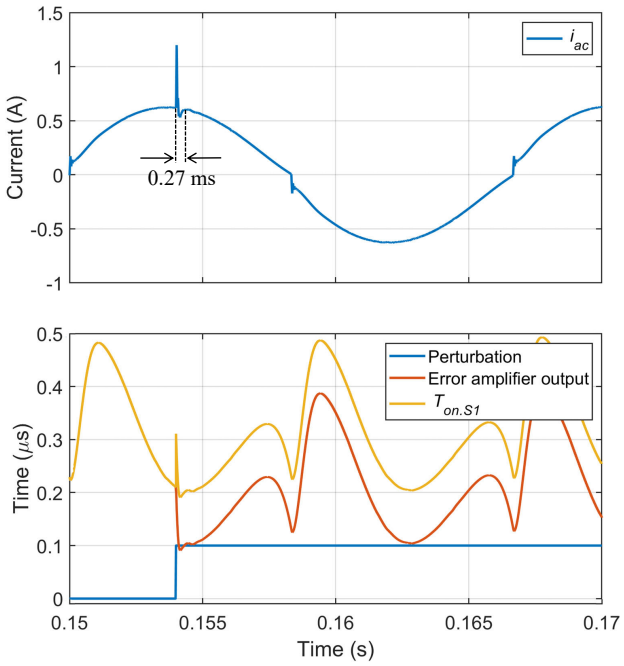


FIGURE 3.15: The effects of 100 ns perturbation of $T_{on.S1}$ on i_{ac}.

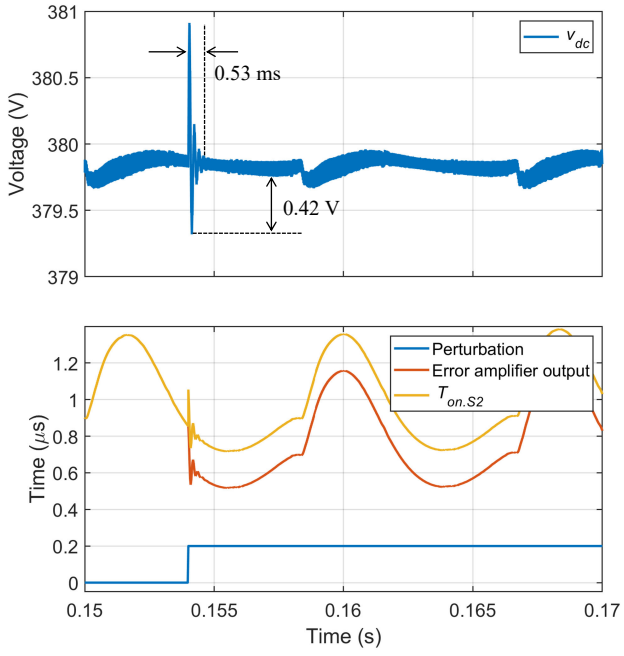


FIGURE 3.16: The effects of 200 ns perturbation of $T_{on.S2}$ on v_{dc}.

The on-time modulator is built with a comparator, a switch, a constant current source, and a capacitor. The capacitor is charged when either power switch is on until its voltage is higher than the voltage from the error amplifier. A higher voltage from the error amplifier leads to

longer on-time because it takes a longer time for the capacitor to be charged up to reset the SR latch and vice versa. In this way, the on-time modulator translates the voltage signal from the error amplifier to the amount of on-time for S_1 and S_2.

Three PI controllers are implemented as the error amplifiers in the proposed control circuits. The PI parameters are designed according to the frequency response analysis, where the open-loop frequency responses of the system are obtained through AC sweep method. The controllers are then designed accordingly to provide sufficient crossover frequency and phase margin. The crossover frequencies of the AC current loop and DC output voltage loop should be much higher than 120 Hz to compensate for the low-frequency harmonics caused by the AC input and are designed to be an order of magnitude lower than the switching frequency to reduce the sensitivity to the high-frequency switching noises. The crossover frequency of the buffer voltage loop is selected at around 10 Hz to regulate the DC voltage of C_b while avoiding the low-frequency noise of v_b to reduce the harmonic distortion of i_{ac}. Finally, the PI parameters are finely tuned based on simulation and experimental results to achieve desirable transient and steady-state performances.

A 100-ns perturbation, which is around 20 % of $T_{on.S1}$, is added into $T_{on.S1}$ to examine its effect on i_{ac}. The perturbation is intentionally added at the peak of v_{ac} and under full power to evaluate the proposed control strategy in the worst scenario. Fig. 3.15 shows that an increase of $T_{on.S1}$ leads to an increase of i_{rec}, testifying that $T_{on.S1}$ is a suitable control input for regulating i_{ac}. The proposed control circuit effectively regulates i_{ac} as the error amplifier quickly compensates the perturbation via reducing its output, and the steady state of i_{ac} is reached again in 0.27 ms with low undershoot.

Similarly, a 200-ns perturbation, which is around 20 % of $T_{on.S2}$, is added in to $T_{on.S2}$, as shown in Fig. 3.16, to verify the effects of $T_{on.S2}$ on v_{dc}. Fig. 3.16 confirms that v_{dc} increases with the increase of $T_{on.S2}$ and the perturbation in $T_{on.S2}$ can be compensated by the proposed control circuit with 0.53 ms settling time and 0.42 V undershoot.

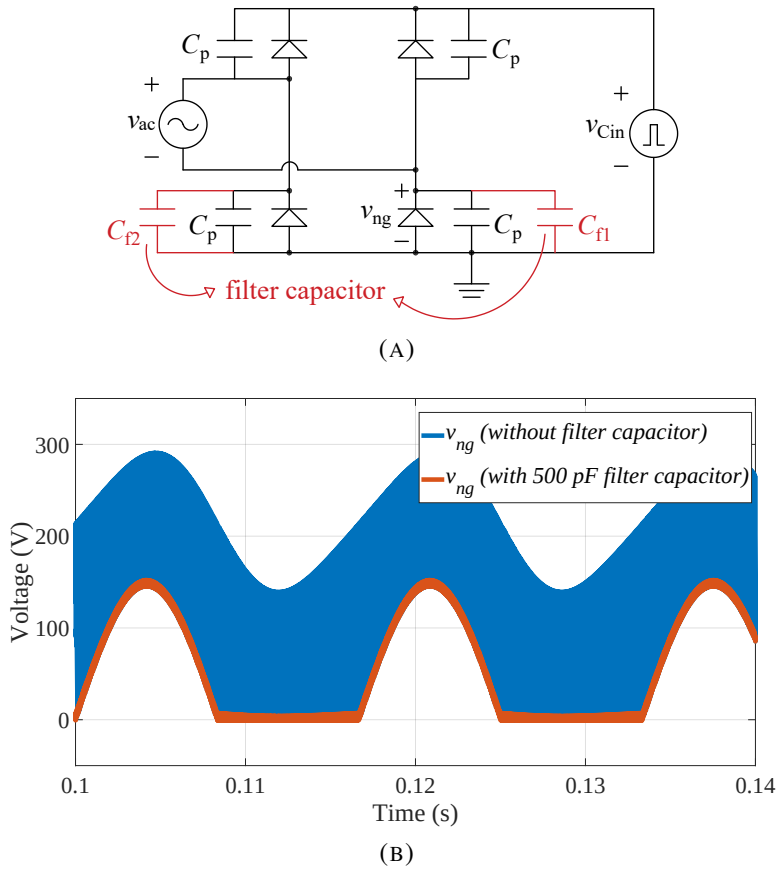


FIGURE 3.17: (A) Proposed filtering method to reduce the common-mode noise. C_p is the junction capacitance of the diodes. C_{f1} and C_{f2} are the added filter capacitors. (B) v_{ng} before and after adding the filter capacitors.

3.3.7 Common-mode Noise Reduction

In the proposed converter, v_{Cin} rises to v_b in each switching cycle. The parasitic capacitors, C_p, appear in the bridge rectifier as shown in Fig. 3.17 (a). Thus, v_{Cin} is divided by the parasitic capacitance of the bridge rectifier. Based on the voltage-dividing rules, the voltage between the neutral and ground is

$$v_{ng} = \frac{C_p v_{Cin}}{2C_p} \tag{3.31}$$

if the filter capacitors, C_{f1} and C_{f2}, are not added. From (3.31), half of the high-frequency components in v_{Cin} will appear in v_{ng}. The resulting waveform of pulsating v_{ng} is demonstrated in Fig. 3.17 (b). The phenomenon is undesirable from the EMI perspective because

TABLE 3.1: Specifications of the prototype.

Specifications	Value
Input Voltage (v_{ac})	Universal
Output Power	100 W
Buffer Voltage (V_b)	400 V
DC-link Voltage (v_{dc})	380 V
f_{sw}	400 kHz

the circuit ground usually shows higher parasitic capacitance to the earth than other nodes in the circuit.

A common-mode choke can suppress the common mode noise from v_{ng}. To improve the performance, a bigger choke is preferable, which is undesirable for high power density and cost-effectiveness. The proposed topology adds two small filter capacitors, C_{f1} and C_{f2}, as highlighted in Fig. 3.17 (a), to ease the issue. After adding the filter capacitors, v_{ng} can be calculated as

$$v_{ng} = \frac{C_p v_{Cin}}{2C_p + C_{f1}}. \tag{3.32}$$

The denominator of (3.32) is higher than that of (3.31). Therefore, the high-frequency components of v_{ng} can be effectively reduced by adding C_{f1}, as shown by the comparison in Fig. 3.17 (b). Hence, the size of the common-mode choke will not impede the improvements in power density.

3.4 Experimental Verification

A prototype rated for 100 W is constructed to evaluate the proposed topology and control scheme. The specifications and bill of materials are summarized in Table. 3.1 and Table. 3.2, respectively. The box volume of major passive components is also included in Table. 3.2. The system is designed and tested by the universal input. The prototype is shown in Fig. 3.18. The prototype achieves a power density of 50.8 W/in^3 by box volume. The size is measured to be 77 $\times$ 28 $\times$ 15 mm^3.

The steady-state waveforms of v_{ac}, i_{ac}, v_b, and v_o at 110 V AC and 220 V AC are measured and shown in Fig. 3.19 and Fig. 3.20, respectively. The waveforms verify that the proposed

TABLE 3.2: Bill of materials.

Components	Descriptions
Diode Bridge	IDDD04G65C6, 650 V, 4 A
S_1, S_2	NV6115, 650 V, 170 mΩ
D_o	C3D02065E, 650 V, 4A
C_b	450BXW33MEFR12.5X25, 450 V, 33 μF, 3906 mm^3
C_{dc}	ECW-FD2W474Q1, 450 V, 470 nF, 917 mm^3
C_{in}	C1206C560JBGACTU, 630 V, 56 pF
L_a	RM 7, 52 μH, 3994 mm^3, N49, 175/46 litz wire
L_b	RM 5, 100 μH, 1588 mm^3, N49, 100/46 litz wire
Op-amps	MCP6022
Nor gates	SN74HCS02QPWRQ1
Not gates	SN74HCS04PWR
And gates	SN74HCS08PWR
Multiplier	AD633JRZ
Analog switch	BSD235N
Comparator	TLV3202AIDR

PFC front end can achieve a high power factor and ripple-free DC-link voltage across a wide input voltage range. The waveform of v_b can accommodate a larger voltage ripple to improve C_b's utilization without affecting v_{dc}. Overviews of other key operating waveforms at different AC inputs are shown in Fig. 3.21 and Fig. 3.22. Detailed waveforms are illustrated in Fig. 3.23 and Fig. 3.24. All match well with the analysis and expectations above. The negative

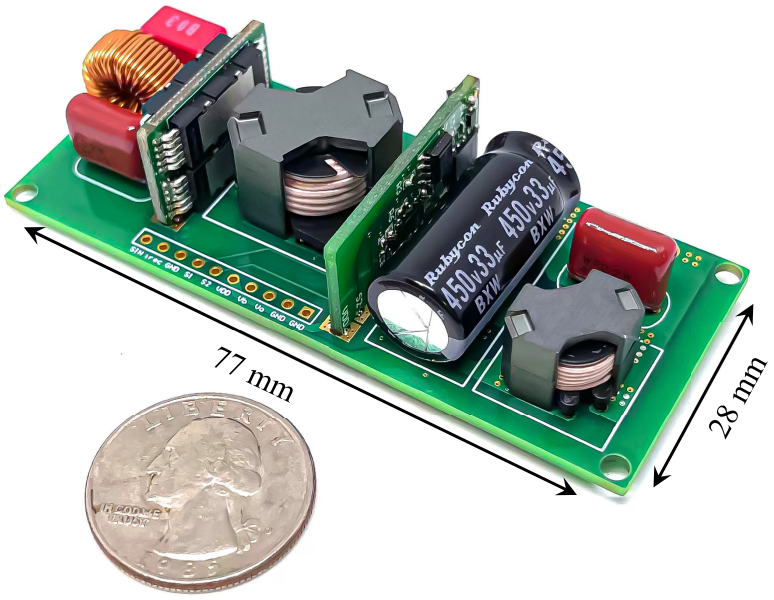


FIGURE 3.18: Photo of the 100 W-rated prototype measured as 77 $\times$ 28 $\times$ 15 mm^3.

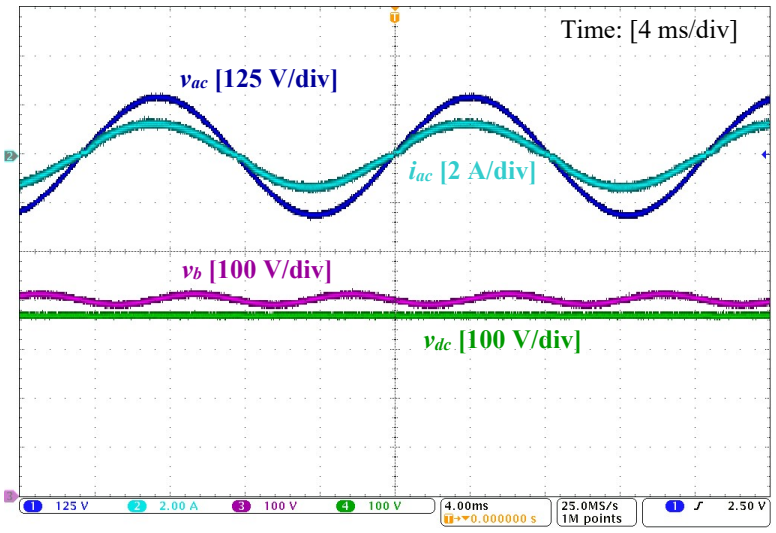


FIGURE 3.19: Waveforms of v_{ac}, i_{ac}, v_b, and v_{dc} at 110 V AC.

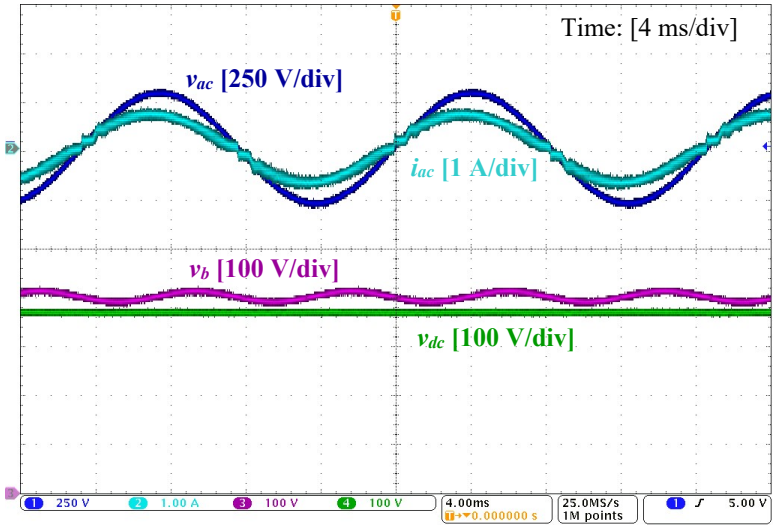


FIGURE 3.20: Waveforms of v_{ac}, i_{ac}, v_b, and v_{dc} at 220 V AC.

value of i_{Lb} reaches -0.2 A and lasts for merely around 10 % of a switching period. Thus, the loss caused by the negative current is small.

The ZVS waveforms of S_2 and S_1 are tested under different AC voltage and operating points as shown from Fig. 3.25 to Fig. 3.32, verifying the universal-range ZVS capability of the proposed topology. Fig. 3.33 shows the effectiveness of the proposed common-mode noise reduction method, as there is no high-frequency ripple in v_{ng}.

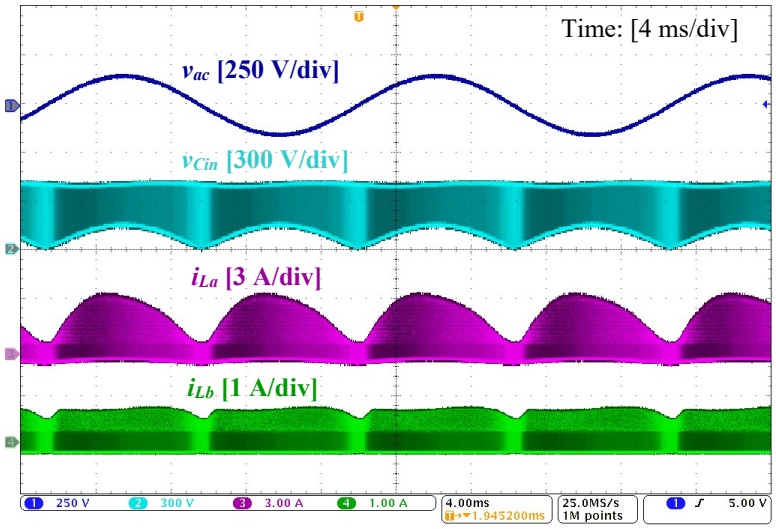


FIGURE 3.21: Waveforms of v_{ac}, v_{Cin}, i_{La}, and i_{Lb} at 110 V AC.

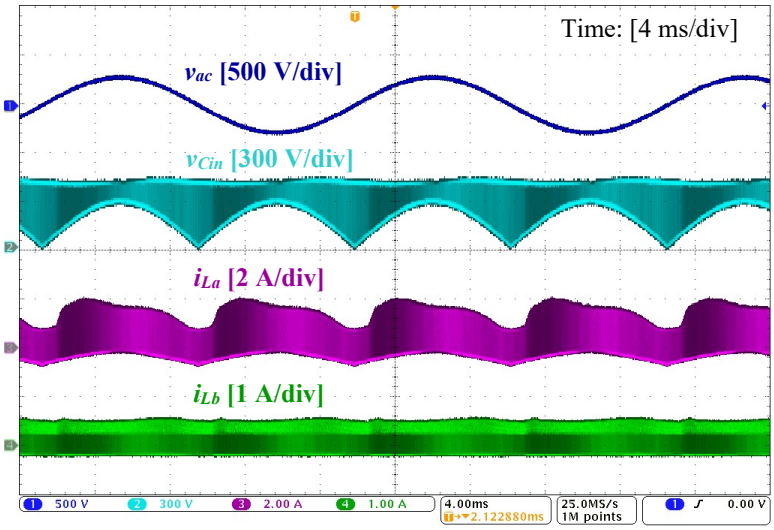


FIGURE 3.22: Waveforms of v_{ac}, v_{Cin}, i_{La}, and i_{Lb} at 220 V AC.

The waveforms under a shutdown process are shown in Fig. 3.34, and the prototype can hold v_{dc} above 300 V for 15.4 ms, which meets the design target and the 3 ms hold-up time requirement in USB PD 3.1. A start-up test is also performed to evaluate the transient performance of the proposed control method as shown in Fig. 3.35. Fig. 3.35 verifies that the circuit can reach the steady state with small overshoots on v_{dc} and v_b. Like the conventional boost converter, an inrush current occurs at the beginning to charge C_b via D_1. The dynamic waveforms under load step-down and step-up processes are shown in Fig. 3.36 and Fig. 3.37,

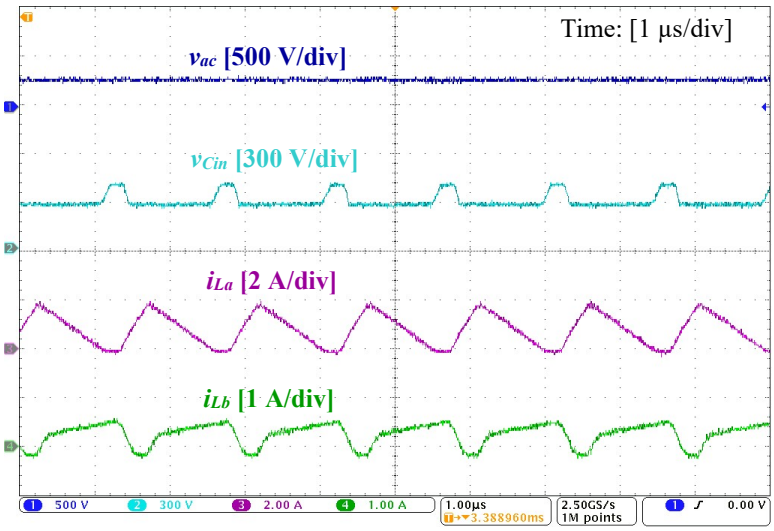


FIGURE 3.23: Detailed waveforms of v_{ac}, v_{Cin}, i_{La}, and i_{Lb} at 220 V AC.

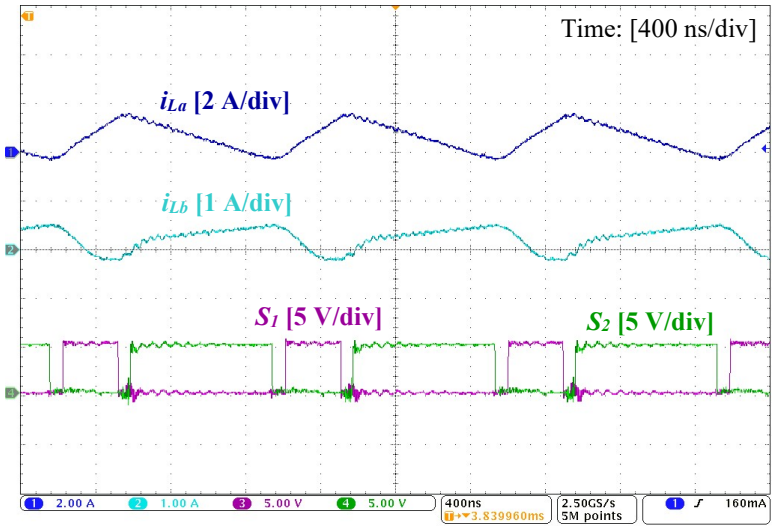


FIGURE 3.24: Detailed waveforms of i_{La}, i_{Lb}, logic signal to S_1, and logic signal to S_2 at 220 V AC.

respectively. The dynamic waveforms verify that the proposed control method can maintain nearly constant DC-link voltage and high-quality AC current under large load transient events. Also, the buffer voltage is well regulated below the 450-V rated voltage with around a 30-V safety margin during the step-down process.

The prototype is tested down to 20 % load power, and the operating waveforms at 20 % load condition are shown in Fig. 3.38, demonstrating a high power factor and constant DC-link voltage at light-load condition. The efficiency curves at different input voltages and power

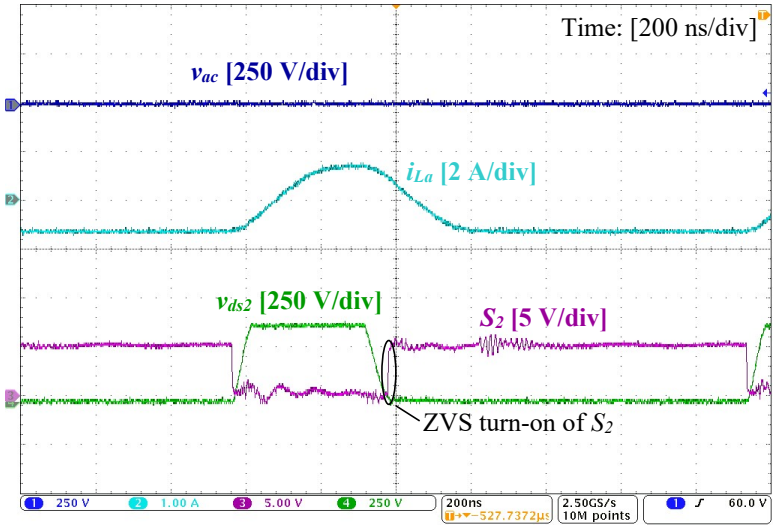


FIGURE 3.25: ZVS waveforms of S_2 at the zero-crossing of v_{ac} (220 V AC).

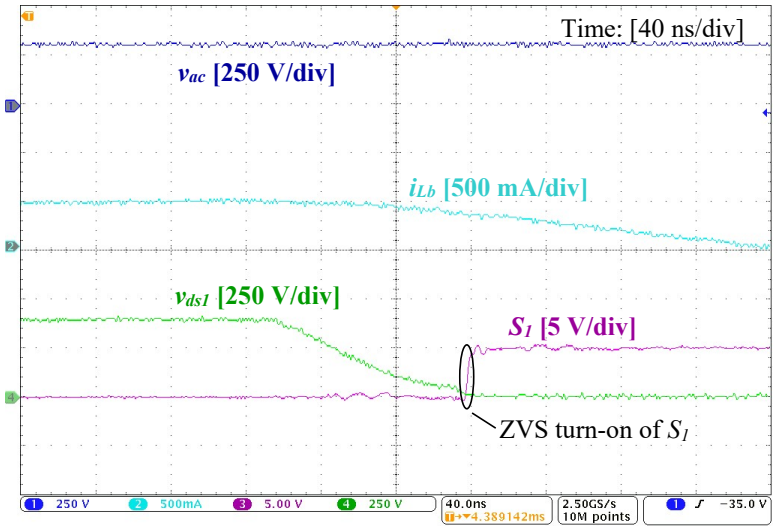


FIGURE 3.26: ZVS waveforms of S_1 at the peak of v_{ac} (220 V AC).

levels are measured and illustrated in Fig. 3.39. The prototype achieves a peak efficiency of 96.7 % at 220 V AC and maintains above 90 % efficiency for load power greater than 40 %. The prototype has higher peak efficiency at 220 V AC than 110 V AC because of the reduced conduction loss, especially in the diode bridge rectifier. However, the light-load efficiency at 220 V AC is slightly lower than that at 110 V AC because the converter loses ZVS earlier at 220 V AC and the switching frequency at 220 V AC is higher. The efficiency drops significantly below 40 W due to the loss of ZVS and increased switching frequency at

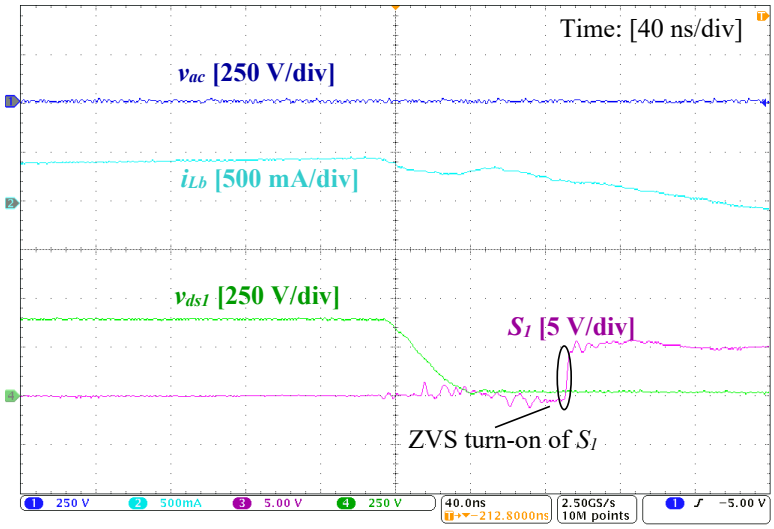


FIGURE 3.27: ZVS waveforms of S_1 at the zero-crossing of v_{ac} (220 V AC).

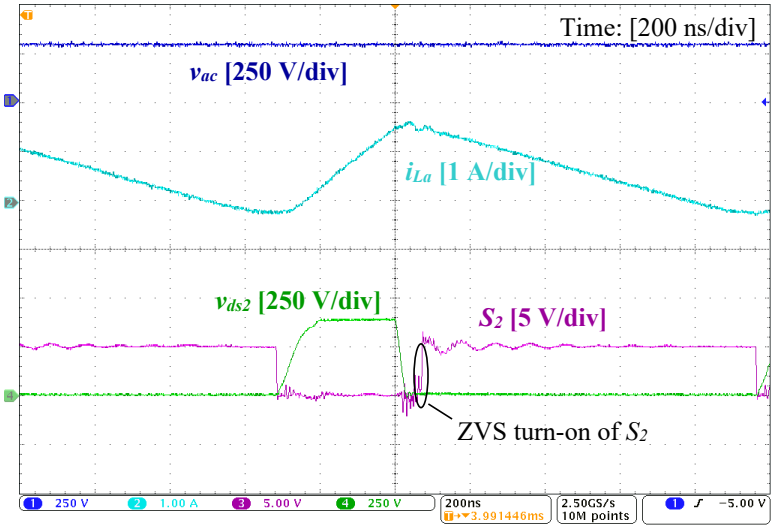


FIGURE 3.28: ZVS waveforms of S_2 at the peak of v_{ac} (220 V AC).

lighter load conditions. Existing light-load operating methods, such as burst-mode control, can be adopted to improve the light-load efficiency by reducing the switching frequency and extending the ZVS region. The loss breakdown of the prototype is shown in Fig. 3.40 and Fig. 3.41, evaluated under the full-load conditions of 110 V and 220 V AC, respectively. In both cases, the diode bridge and magnetics dominate the losses. The analysis indicates future work to improve the efficiency further. The power factor and total harmonic distortion under different AC voltage and power levels are measured in Fig. 3.42. The prototype achieves

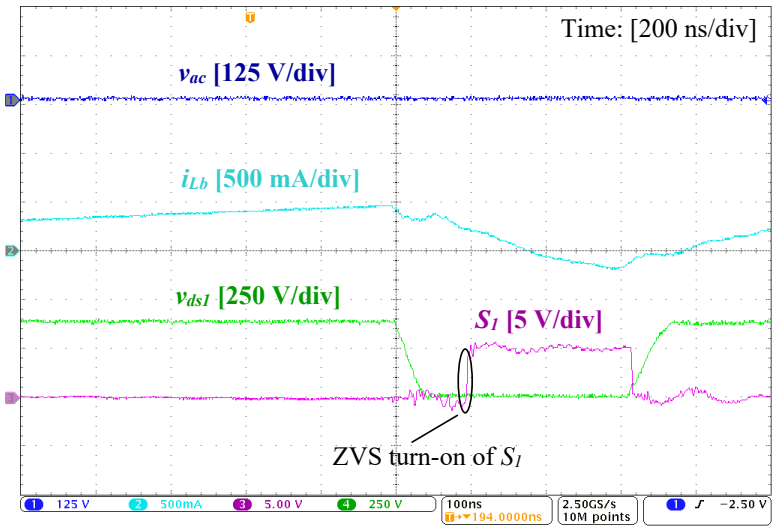


FIGURE 3.29: ZVS waveforms of S_1 at the zero-crossing of v_{ac} (110 V AC).

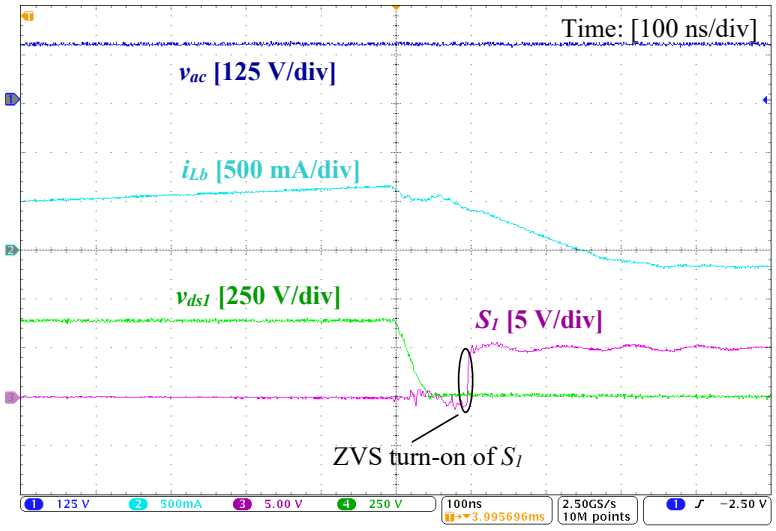


FIGURE 3.30: ZVS waveforms of S_1 at the peak of v_{ac} (110 V AC).

above 0.95 power factor across a wide range of AC voltage and under different load conditions. The prototype shows a higher power factor at low-line conditions because the reactive power caused by the input filter capacitor is reduced at lower AC voltage. The THD values are lower under the high-line condition because the converter works at a higher switching frequency at 220 V AC, and the high-frequency harmonics of i_{La} are better suppressed by the input filter.

A comparison between the proposed solution and the recent publications is summarized in Table. 3.3. The magnetic energy storage of the CRM boost PFC is taken as a benchmark

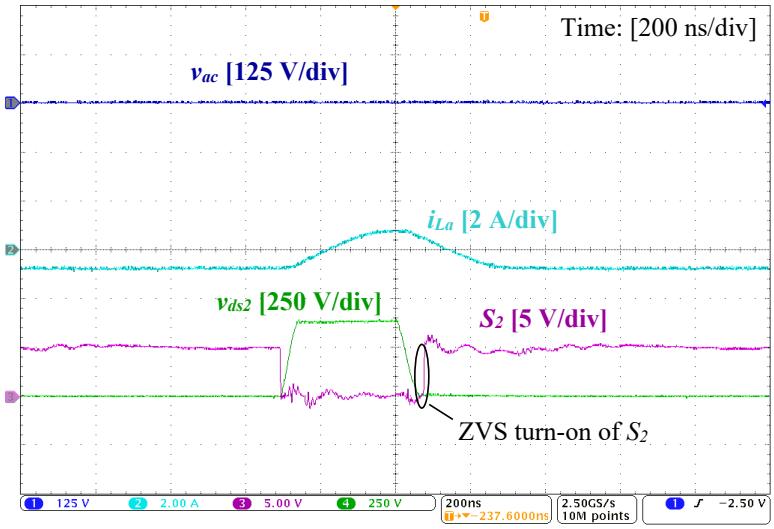


FIGURE 3.31: ZVS waveforms of S_2 at the zero-crossing of v_{ac} (110 V AC).

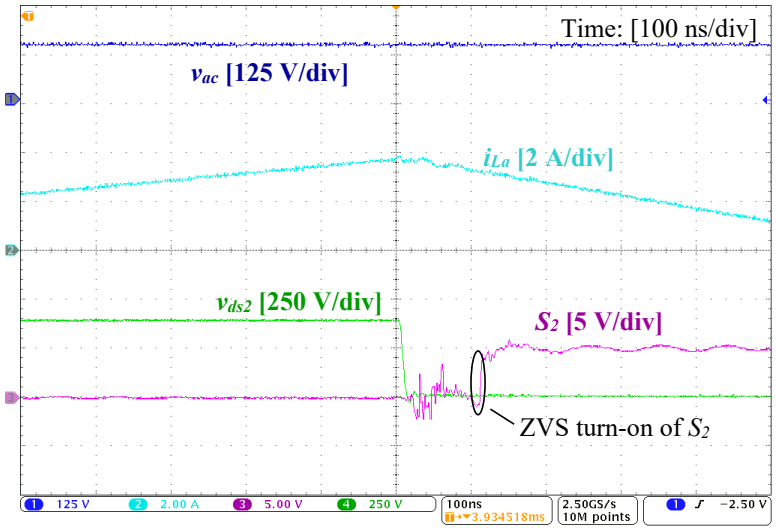


FIGURE 3.32: ZVS waveforms of S_2 at the peak of v_{ac} (110 V AC).

for comparison. By comparison, it is shown that the proposed solution demonstrates lower magnetic energy storage and requires fewer active switches than many other works. Also, the proposed solution is the only one that can achieve both universal-range ZVS of all switches and ripple-decoupled DC-link voltage, allowing for smaller magnetics through high-frequency operation and a smaller energy buffer through increasing its voltage ripple. In Table. 3.3, five solutions rely on digital control techniques. The proposed converter is based on the analog circuit, reducing the overall cost.

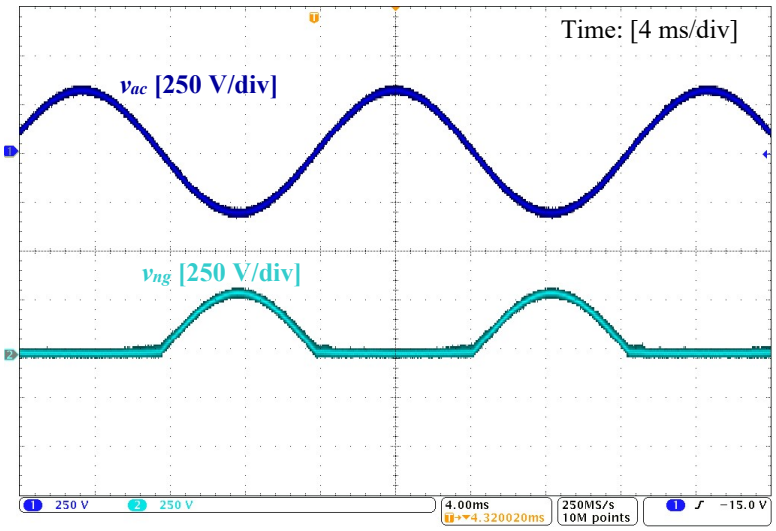


FIGURE 3.33: The voltage potential between the circuit ground and neutral.

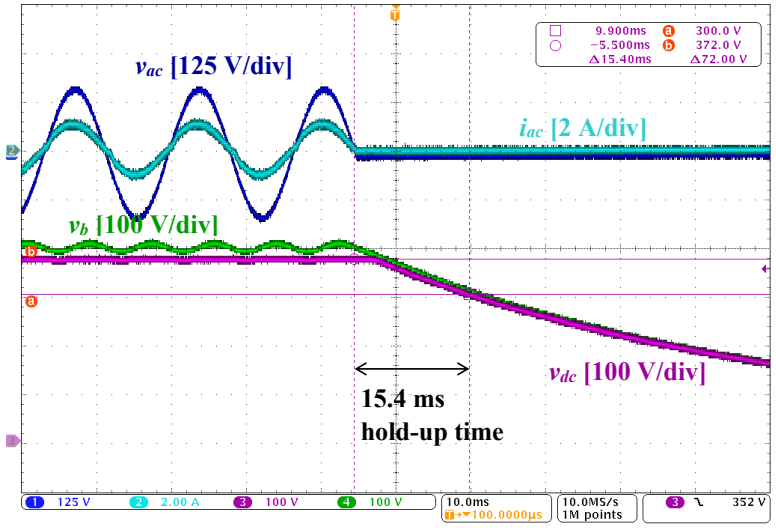


FIGURE 3.34: Waveforms of a shutdown process.

A comparison to the conventional 100 W CRM boost PFC front end is compared in detail and summarized in Table. 3.4. The volume of energy buffer takes both C_b and C_{dc} into account, and both L_a and L_b are considered in the volume of magnetics. The two designs follow similar specifications used in [27]. Although the proposed topology increases the component counts, it maintains a similar bill of material cost as the conventional CRM boost PFC. The proposed topology greatly reduces the size of the PFC front end at the power level, including a 51 % reduction in buffer capacitance, 21 % size reduction in energy buffer, and 47 % size

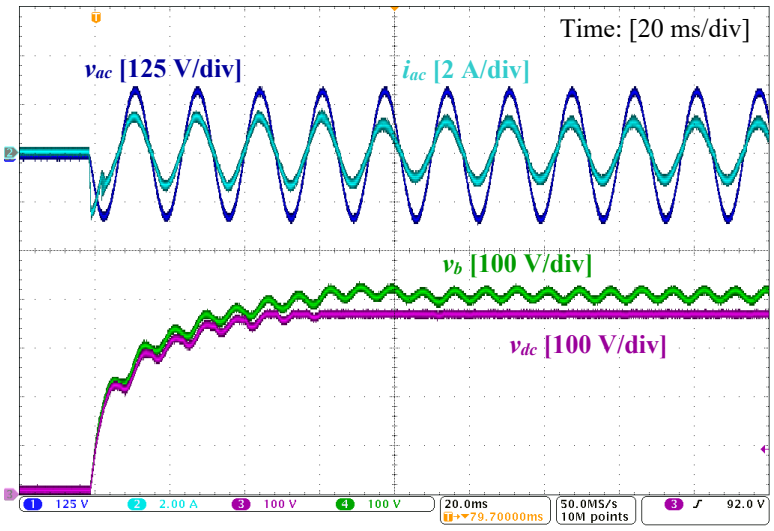


FIGURE 3.35: Waveforms of a startup process.

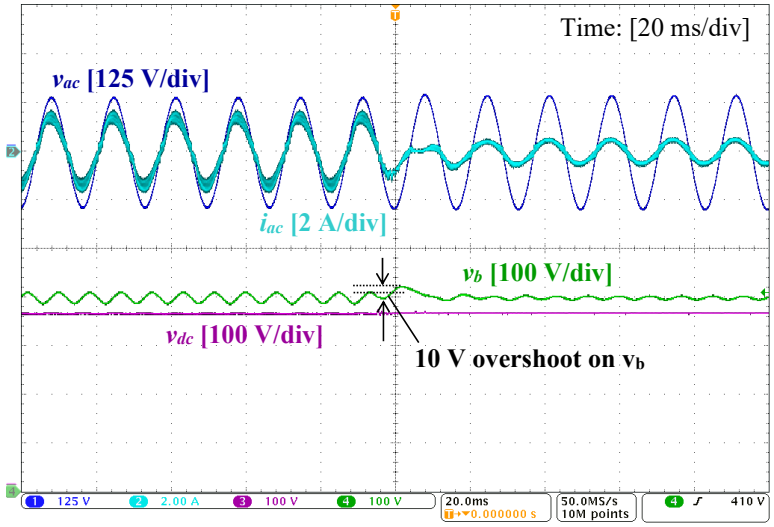


FIGURE 3.36: Waveforms of a load step-down process from 100 % to 20 % load power.

reduction in magnetics. The proposed topology also presents a ripple-free DC-link voltage while maintaining competitive efficiency. The size of magnetics in [27] may be reduced without compromising efficiency by using GaN devices and increasing switching frequency, but the possible switching frequency and, hence, the room for size reduction will still be limited by the switching loss due to hard-switching operations. Also, the trade-off between the size of the buffer capacitor and DC-link voltage ripple in the conventional CRM boost

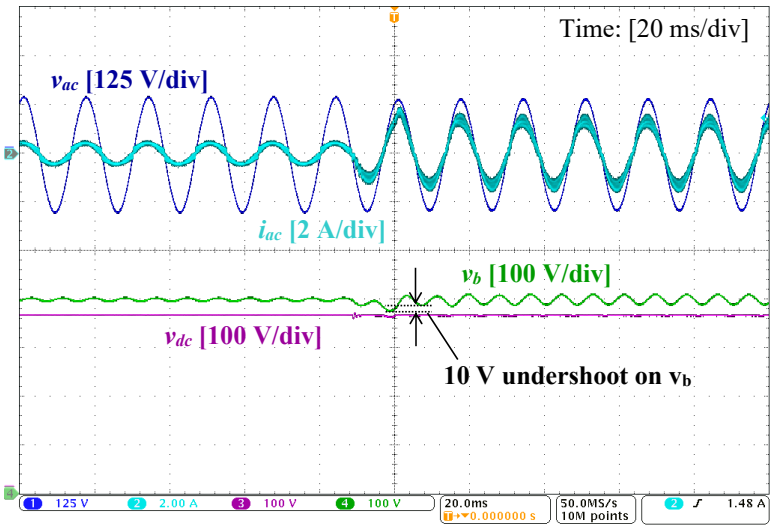


FIGURE 3.37: Waveforms of a load step-up process from 20 % to 100 % load power.

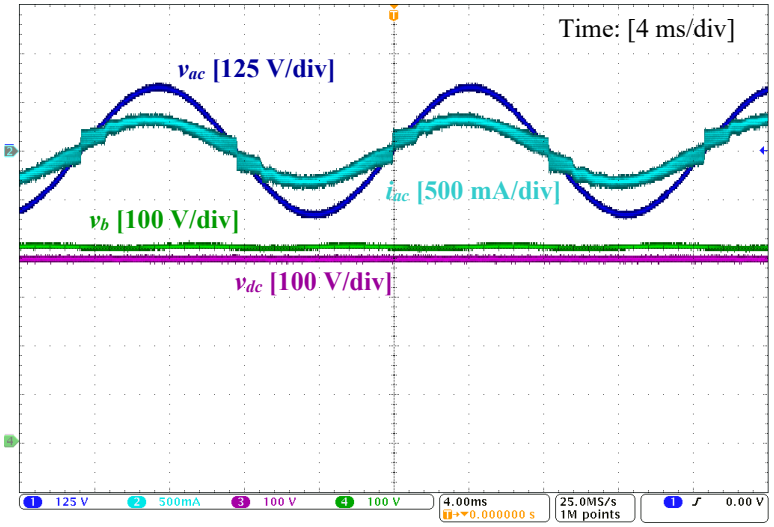


FIGURE 3.38: Waveforms of v_{ac}, i_{ac}, v_b, and v_{dc} at 20 W output.

converter remains unsolved, making it hard to shrink the buffer capacitor in [27] without compromising the following stages' performance.

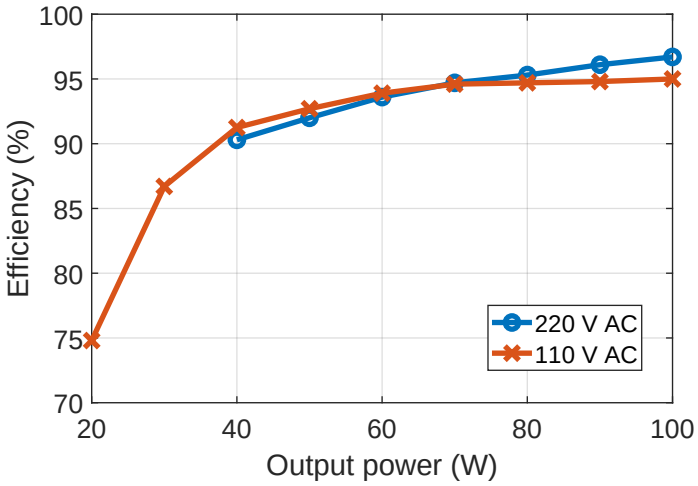


FIGURE 3.39: Efficiency curves of the prototype.

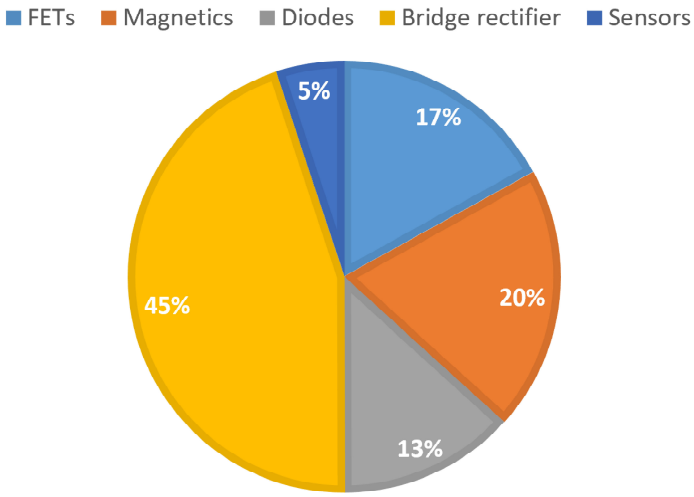


FIGURE 3.40: Loss breakdown under full-load output and 110 V AC input.

TABLE 3.3: Comparison between recently published PFC solutions.

Features	CRM Boost	Totem-pole Boost	[50]	[51]	[52]	[53]	[54]	This Work
Magnetic storage (pu)	1	1	2	0.79	2.4	2.5	1.7	1.05
Number of FETs	1	4	4	4	1	4	4	2
Bridgeless topology	×	√	√	×	×	√	√	×
Ripple-free DC link	×	×	√	×	√	√	×	√
ZVS of FETs	×	√	×	√	×	×	√	√
Controller type	Analog	Digital	Digital	Digital	Analog	Digital	Digital	Analog

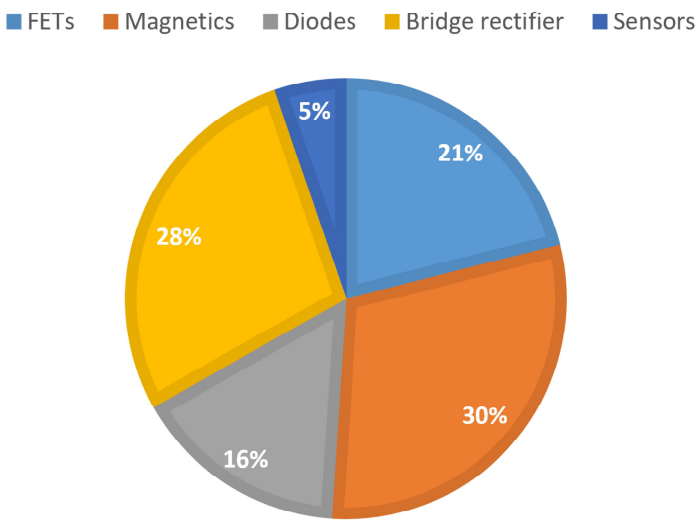


FIGURE 3.41: Loss breakdown under full-load output and 220 V AC input.

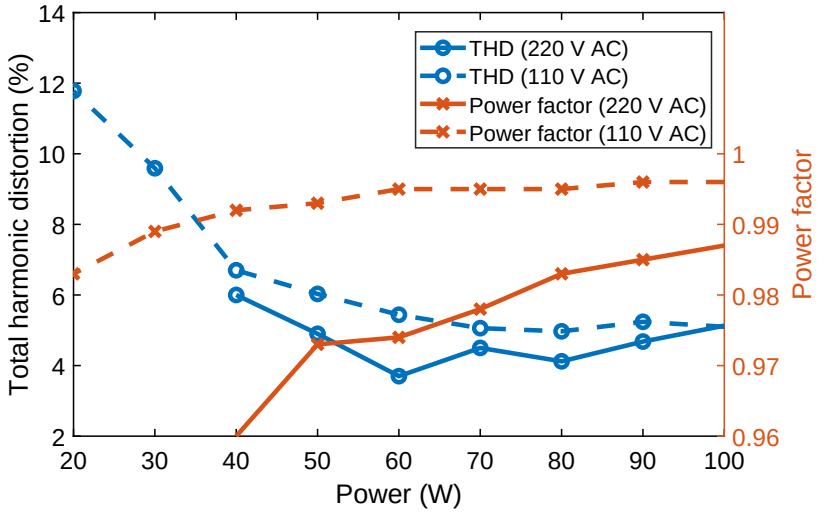


FIGURE 3.42: Measured power factor and total harmonic distortion under high-line and low-line conditions.

3.5 Summary

This chapter presents a new topology as the PFC front end, showing improvements regarding constant DC-link voltage, reduced buffer capacitance, and universal-input-range ZVS. A 100-W universal prototype is designed and constructed for performance evaluation. It achieves a 96.7% peak efficiency and a power density of 50.8 W/in^3. Compared to a typical CRM boost PFC front end at the same power level, the prototype achieves a 47% size reduction of the

TABLE 3.4: Comparison between the conventional CRM boost PFC front end and this work.

Performance	CRM Boost [27]	This work
Power factor	0.99	0.99
Controller type	Analog	Analog
Power level	100 W	100 W
Buffer voltage	400 V	400 V
Semiconductor technology	Si	GaN, SiC
Universal-range ZVS	$\times$	$\surd$
Minimum f_{sw}	45 kHz	400 kHz
Number of passive components	2	4
Rating of energy buffer	450 V, 68 μF	450 V, 33 μF
Volume of energy buffer	6109 mm^3	4823 mm^3
Peak voltage of energy buffer	405 V	410 V
Ripple of the energy buffer	2.5 %	5 %
Volume of magnetics	10518 mm^3	5582 mm^3
Cost of buffer capacitors	\$1.52	\$0.86
Cost of magnetics	\$2.13	\$3.16
Cost of FETs	\$3.59	\$3.92
Total cost [a]	\$7.24	\$7.94
DC-link low-frequency ripple	10 V	0 V
Peak efficiency	96.9 %	96.7 %

[a]Calculated based on the unit price of 1000 pieces from DigiKey.

magnetic components and a 21% size reduction of the buffer capacitor with a comparable efficiency performance. The proposed solution is also compared with the latest publications to show the advantages, including lower magnetic energy storage, fewer active switches, simpler control implementations, and a smaller energy buffer.

CHAPTER 4

Stacked-switch Power Factor Correction Architecture

4.1 Background

High power density is increasingly demanded in many AC–DC applications [21]. A two-stage power-factor-correction (PFC) architecture is widely adopted for AC–DC applications above 75 W. Fig. 4.1 shows a typical implementation of such an architecture, consisting of a boost PFC front end and a half-bridge isolated converter [55]. However, the conventional critical mode (CRM) boost PFC front end loses zero-voltage-switching (ZVS) at high-line conditions. Thus, its switching frequency is usually limited to below 100 kHz to reduce switching losses. Therefore, the size of the boost inductor and input EMI filters of the conventional two-stage PFC architecture are generally large, hindering a further improvement of the power density performance [32].

Recent research focusing on power density improvements of the two-stage architecture usually leads to higher cost and complexity [51]. The power density of the boost PFC front end can be greatly improved by replacing D with an active switch to assist the ZVS turn-on of S_B and operating the converter at a higher switching frequency [35], [36], [56]. As trade-offs, the cost increases, the switching frequency varies in a wide range, and complicated sensing and control circuits are usually required for high-speed zero-crossing detection and on-time calculations [57]. Multilevel PFC front ends are also effective in reducing the size of the boost inductor and EMI filters [37], [38], [58], but more switches are needed for the increased voltage levels, inevitably adding cost and complexity. Single-stage conversion has been explored. However, existing single-stage solutions have issues such as bulky buffer capacitor [59] and narrow soft-switching range [60], and further improvements are still necessary to achieve a comparative

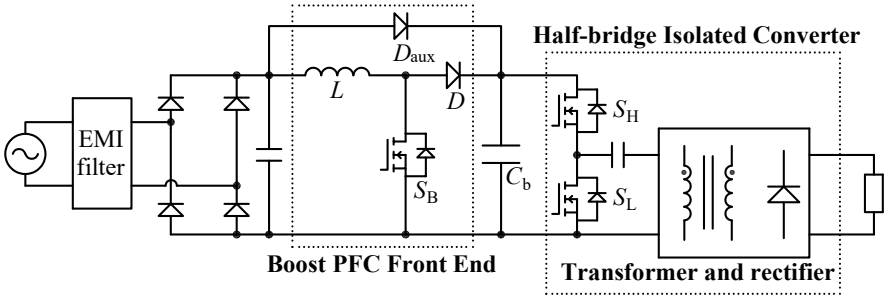


FIGURE 4.1: Two-stage PFC architecture.

full-load range efficiency with the two-stage solutions. Therefore, it would be highly desirable to find a solution that allows the boost PFC stage in the two-stage architecture to operate at a much higher switching frequency without causing troubles such as wide switching frequency range, increased component counts, high switching loss, complicated sensing and control, and narrow soft-switching range.

Recently, a stacked-switch structure has been developed in DC–DC applications to enable power transfer among multiple ports [61]. It is reported that the stacked-switch structure can improve the efficiency of LLC converter in applications requiring wide operating ranges [62]. Also, the stacked-switch structure can lower the component counts and realize ZVS by integrating a boost converter with a buck converter [63]. Nevertheless, using the stacked-switch structure in AC–DC applications has unique challenges compared to DC–DC applications mentioned above, including output regulation over a universal input, active current shaping, 100/120 Hz ripple buffering, and buffer voltage regulation, and its feasibility and performance in AC–DC applications have not been demonstrated yet.

This chapter investigates the use of the stacked-switch structure in AC–DC applications and proposes a stacked-switch PFC architecture to reduce the size and cost of the conventional two-stage PFC architecture. It is first demonstrated that the stacked-switch architecture can realize 1) full-load-range ZVS of all active switches, 2) unity power factor, 3) constant switching frequency, and 4) universal-input operations. This is achieved by simply removing D and re-positioning the three switches in the two-stage architecture. As a result, the size of passive components can be reduced by increasing the switching frequency, and higher power density can be achieved with lower component counts. It is also demonstrated that the

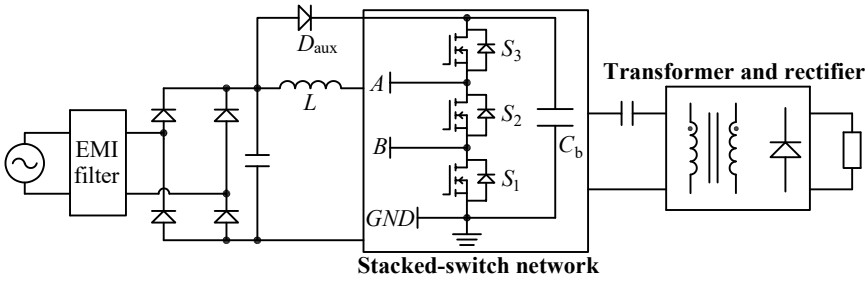


FIGURE 4.2: Stacked-switch PFC architecture.

stacked-switch PFC architecture can directly take advantage of the well-developed control methods in the conventional two-stage PFC architecture, allowing for a simple control design and reducing time to market. An analog control circuit is newly developed to facilitate a low-cost control implementation. A 150-W-universal-input prototype is built, which measures 92.9 % peak efficiency and 53.9 W/in^3 power density.

4.2 Stacked-switch PFC Architecture

4.2.1 Operating Principle

The proposed stacked-switched PFC architecture is shown in Fig. 4.2. The stacked-switch architecture merges the boost PFC stage and the isolated DC–DC stage into a stacked-switch switching network. Compared to the two-stage architecture, the stacked-switch architecture doesn't require D and reduces the component count. Similar to the two-stage architecture, the stacked-switch architecture uses three active switches, but the three switches are connected in a series-stacked manner, creating two switching nodes, i.e., A and B, and a ground node GND. Each of the two stages uses either two of the three nodes, resulting in different configurations. Configuration I is used to illustrate the fundamental operating principle.

In Configuration I, the boost stage is connected between nodes A and GND, and the isolated DC–DC stage is connected between nodes B and GND. Configuration I has three operating states, as shown in Fig. 4.3, and each state is elaborated as follows:

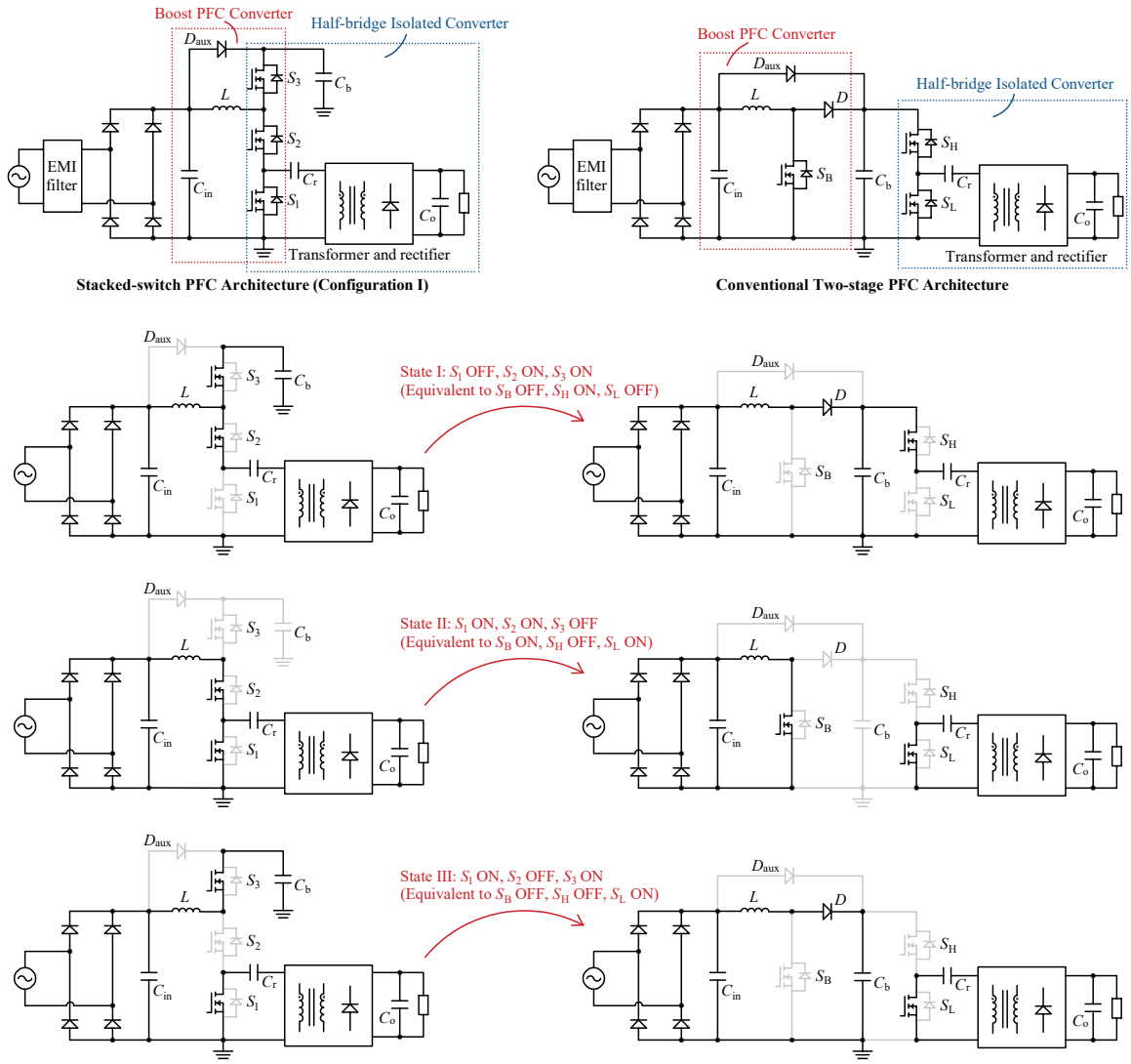


FIGURE 4.3: Operating principle of the stacked-switch PFC architecture.

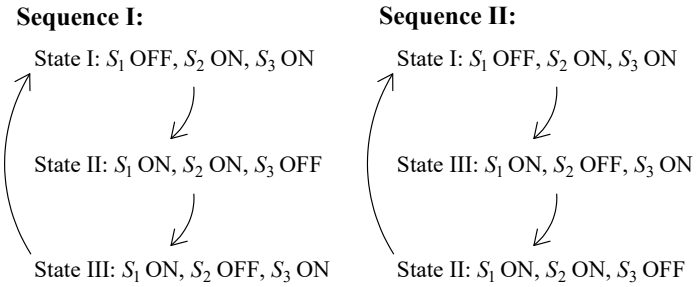


FIGURE 4.4: Two possible switching sequences in Configuration I of stacked-switch PFC architecture.

- State I: S_2 and S_3 are on, which is equivalent to turning off S_B and turning on S_H in the two-stage PFC architecture. L discharges its stored energy to the buffer capacitor C_b. Meanwhile, C_b charges the energy storage elements in the isolated DC-DC stage. This operating state is equivalent to the discharging state of boost PFC stage and the charging state of the isolated DC–DC stage.
- State II: S_1 and S_2 are on, equivalent to turning on S_B and S_L in the two-stage PFC architecture. The boost inductor L is charged by the AC source. The energy storage elements in the isolated stage release their stored energy to the load through the transformer and secondary rectifiers. This operating state is equivalent to the charging state of boost PFC stage and the discharging state of the isolated DC–DC stage.
- State III: S_1 and S_3 are on, equivalent to turning off S_B and turning on S_L in the two-stage PFC architecture. L releases it stored energy to C_b through S_3. The energy storage elements in the isolated stage continue discharging their stored energy. It is worth mentioning that the secondary side may not continuously receive energy in State II and III as some isolated topologies are designed to operate at resonant mode where the secondary current can reach zero before S_L is turned off. This operating state is equivalent to the discharging state of boost PFC stage and the discharging state of the isolated DC–DC stage.

In summary, the stacked-switch PFC architecture is capable of performing all necessary switching states in the two-stage PFC architecture, including the charging and discharging states of the boost PFC stage as well as the isolated DC–DC stage. The energy transfer mechanism of the stacked-switch architecture is identical to the two-stage architecture, except that the stacked-switch architecture saves one high-frequency diode and can achieve soft switching of all active switches. The ZVS realization of all switches is discussed in the following subsection.

TABLE 4.1: Comparison between the two-stage architecture and the stacked-switch PFC architecture.

Features	Two-stage PFC	Stacked-switch PFC
Number of FETs	3	3
Number of diodes	2	1
isolation	$\surd$	$\surd$
PFC	$\surd$	$\surd$
ZVS of all switches	$\times$	$\surd$

4.2.2 Switching Sequence and ZVS Realization

Configuration I of the stacked-switch architecture contains three switching states, leading to two possible switching sequences shown in Fig. 4.4. This section analyzes and compares how ZVS turn-on of the three switches is realized under different switching sequences, and a recommendation is made.

The ZVS realizations in Sequence I are analyzed as follows:

- State I to State II: S_3 is turned off, and the output capacitance of S_1 is being discharged by the transformer current, as shown in Fig. 4.5. The energy to realize the ZVS turn-on of S_1 is from resonant inductance, or leakage inductance, or magnetizing inductance, or their combinations of the isolated DC–DC stage depending on the topology selection. The turn-on process of S_1 is similar to that of S_H in the isolated DC–DC converters. It has been verified that many existing isolated DC–DC converters, such as LLC converters, can achieve full-load-range zero-voltage-switching. Therefore, ZVS turn-on of S_1 can also be achieved across the full-load range, as later proved in the experimental results.
- State II to State III: S_2 is turned off, and S_3's output capacitance is discharged by i_L, as shown in Fig. 4.6. It should be noted that i_L may not be high enough to fully discharge the output capacitance of S_3 at very light-load conditions because the input current is close to zero. However, converters don't usually operate at the normal mode under light-load conditions, and dedicated power-saving modes, such as pulse skipping or burst modes, are well developed to improve efficiency at light-load conditions. In fact, the ZVS turn-on of S_3 can be achieved across a nearly

full operating range, which is the same as the turn-on of D in the boost converter. It will also be demonstrated later that full-range ZVS of S_3 can be achieved via properly desiging C_{in}.

- State III to State I: S_1 is turned off, and the transformer current is discharging S_2's output capacitance as shown in Fig. 4.7. The turn-on process of S_2 is identical to that of S_H in the conventional isolated DC–DC converters, so S_2 can also achieve full-load-range ZVS turn-on.

The analysis shows that full-load-range ZVS turn-on of all switches can be achieved under Sequence I. However, Sequence II is hard to guarantee full-load-range soft switching for the following reasons. In Sequence II, when the operating state switches from State III to State II, the energy to discharge the output capacitance of S_2 is from L as shown in Fig. 4.8, and sufficient negative i_L is required to fully discharge S_2's output capacitance. Although extending the on-time of S_3 helps to increase the negative current of i_L, complicated sensing circuits and control algorithms are mandatory to avoid excessive conduction losses due to the increased current ripple on L. In addition, the switching frequency can vary widely throughout a line period, as in the critical-mode boost PFC converter. Thus, Sequence I is recommended. Table. 4.1 concludes the differences between the two-stage PFC architecture and the stacked-switch PFC architecture. The stacked-switch architecture has a lower component count than the two-stage architecture while being able to switch at a higher frequency thanks to the ZVS capability. Hence, the stacked-switch architecture is suitable for applications where cost-effectiveness and power density are of primary concern, such as power adapters, battery chargers, and LED drivers.

4.2.3 Comparison to Existing Single-stage PFC Solutions

Many single-stage solutions have been developed in the literature, generally focusing on reducing the number of active switches. One typical single-stage solution is shown in Fig. 4.9 [64], where S_B and S_L are merged into a single switch S_a so that the total number of switches can be reduced from 3 to 2 compared to the two-stage architecture. Reducing the number of switches sacrifices operating freedom. In the two-stage architecture, there are three control

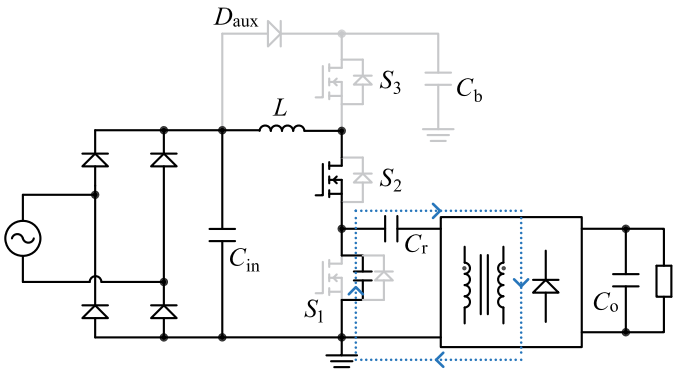


FIGURE 4.5: ZVS transition from State I to State II. S_1's output capacitance is discharged by the transformer current highlighted in blue. The charging/discharging effects of i_L on the output capacitance of S_1 is negligible because L is designed to work at discontinuous-conduction mode (DCM) in this thesis.

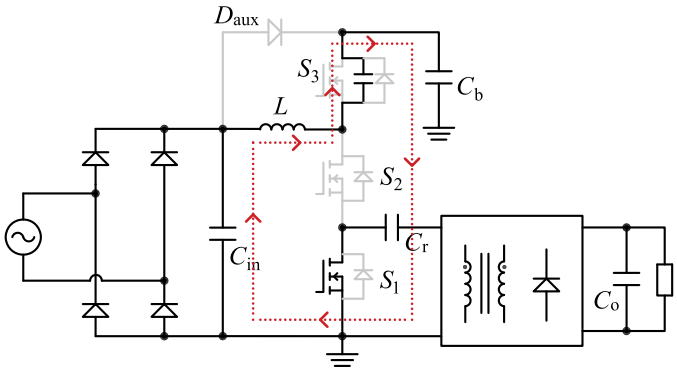


FIGURE 4.6: ZVS transition from State II to State III. S_3's output capacitance is discharged by the boost inductor current highlighted in red.

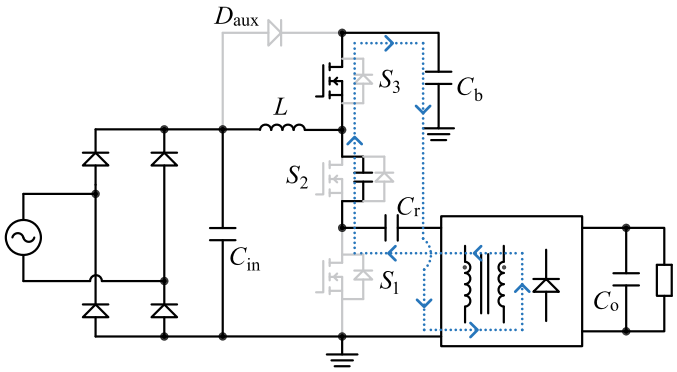


FIGURE 4.7: ZVS transition from State III to State I. S_2's output capacitance is discharged by the transformer current highlighted in blue.

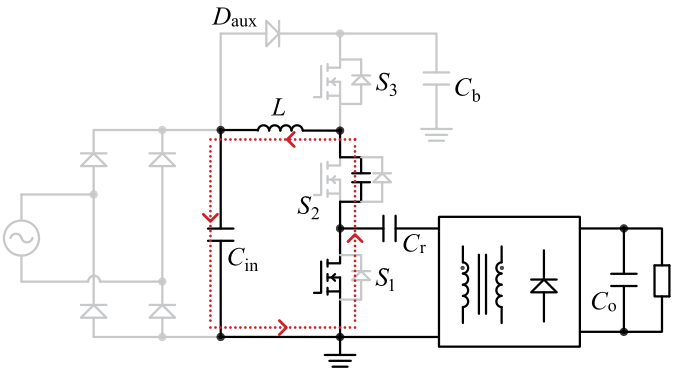


FIGURE 4.8: ZVS transition from State III to State II. S_2's output capacitance is discharged by the boost inductor current highlighted in red. Complicated digital calculations and high-speed current sensing are required to precisely regulate the negative current of i_L to guarantee ZVS without incurring excessive circulating power.

TABLE 4.2: Comparison with recently published single-stage PFC solutions

	[64]	[65]	[66]	[60]	[67]	[68]	[69]	Two-stage PFC	This work
Active input current shaping	×	×	√	√	×	×	×	√	√
Universal input	×	×	×	√	√	√	√	√	√
Regulated bus voltage	×	×	√	√	√	×	×	√	√
Low output ripple and buffer capacitance	×	√	√	√	×	×	×	√	√
Active ripple power buffering	×	√	√	√	√	×	√	√	√
Constant switching frequency	×	×	√	×	×	√	√	√	√
ZVS of all active switches	√	√	×	√	√	×	√	×	√

variables (i.e., the on-duration of S_B, S_L, and S_H). However, in the single-stage solution in Fig. 4.9, S_a and S_b must be switched complementarily to realize ZVS, leading to only two control variables (i.e., the on-duration of S_a and the on-duration of S_b). As per the minimum active switch theory [21], with two control variables, it is impossible to simultaneously realize active ripple power buffering and active current shaping at a constant switching frequency, making it hard for the single-stage solutions to replace the two-stage solutions in applications greater than 75 W.

For example, to achieve active current shaping and bus voltage regulation, the on-duration of S_a in Fig. 4.9 must be actively controlled and adjusted. Meanwhile, the on-duration of S_b must also be controlled to regulate the output voltage. Hence, if one wants to realize active current shaping, bus voltage regulation, and output voltage regulation simultaneously, the switching

period (i.e., the sum of the on-duration of S_a and S_b) must vary. The varying switching frequency imposes great challenges on the design of the isolated stage as the magnetizing inductance must be low enough to support ZVS under the highest switching frequency, resulting in excessive magnetic energy storage and bulky magnetics. Moreover, the switching frequency of single-stage solutions often increases significantly at light-load conditions because the required on-duration generally reduces at a lighter load. The significantly increased switching frequency at light-load conditions limits the frequency increase at the full-load condition due to challenges in control implementations and hinders the improvements of power density. Alternatively, if S_a is used to achieve output voltage regulation and S_b is used to maintain constant switching frequency, the circuit in Fig. 4.9 will lose active current shaping and bus voltage regulation, causing high harmonic distortion in the input current and high voltage stress on the buffer capacitor under some operating conditions.

These issues are also widely reported in other similar single-stage solutions that use only one or two switches. The lack of control freedom makes them hard to realize all the necessary functions mandated in PFC applications. Unlike the single-stage solutions focusing on reducing switches, the stacked-switch architecture aims at better utilizing the existing three switches in the two-stage architecture, enabling more functions without compromising the cost and complexity. In particular, there also exist three control variables (i.e., the on-duration of State I, State II, and State III) in the stacked-switch PFC architecture. While two of the three variables must be used to achieve active current shaping, buffer voltage regulation, and output voltage regulation, there still remains one free control variable, which enables constant switching frequency or other auxiliary functions, such as frequency dithering and circulating energy minimization, to ease the circuit design or optimize other performance merits. Table. 4.2 compares the stacked-switch architecture with recently published single-stage solutions. It is shown that the stacked-switch architecture is the only one that can achieve all the functions at the same time.

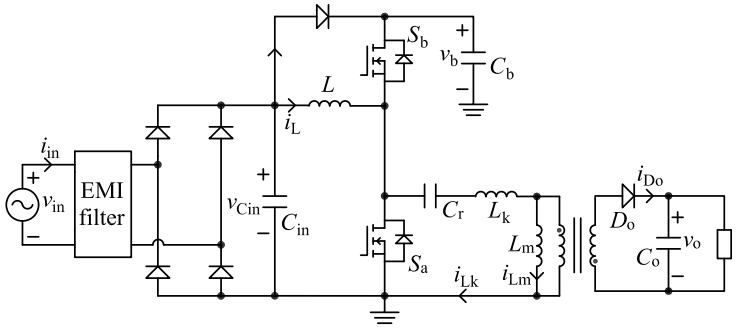


FIGURE 4.9: A single-stage PFC converter based on integration of boost and flyback converters [64].

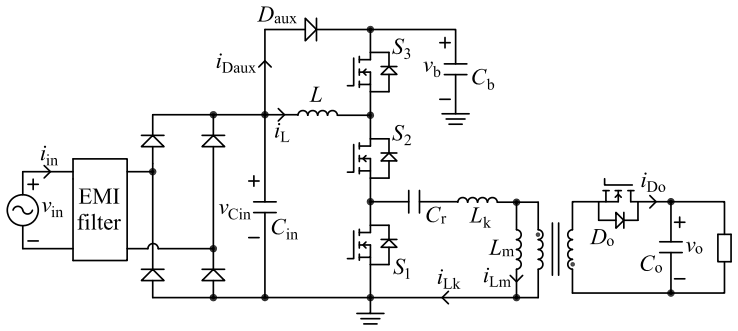


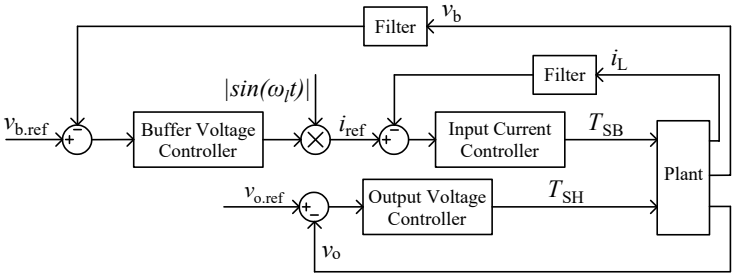
FIGURE 4.10: Schematic diagram of an implementation of the stacked-switch PFC architecture, where the asymmetrical half-bridge flyback converter is adopted as the isolated DC–DC stage and Configuration I is used. A synchronous rectifier is used to implement the secondary diode D_o.

4.3 Design Considerations

4.3.1 Modulation and Control

Fundamentally, the stacked-switch PFC architecture operates the same way as the two-stage architecture except that the switching realization is slightly different. Hence, the stacked-switch PFC architecture can take advantage of the well-developed control methods for the two-stage PFC architecture. The detailed modulation and control method can vary depending on the isolated topology. For example, pulse-width modulation is used for flyback converters, frequency modulation is used for LLC converters, and phase-shift modulation is used for dual-active-bridge converters. In this thesis, the author investigate the modulation and control method of the stacked-switch PFC architecture when the asymmetrical half-bridge (AHB) flyback converter is adopted as the isolated stage as shown in Fig. 4.10. The AHB flyback

Control Block Diagram for Two-stage Architecture:



Control Block Diagram for Stacked-switch Architecture:

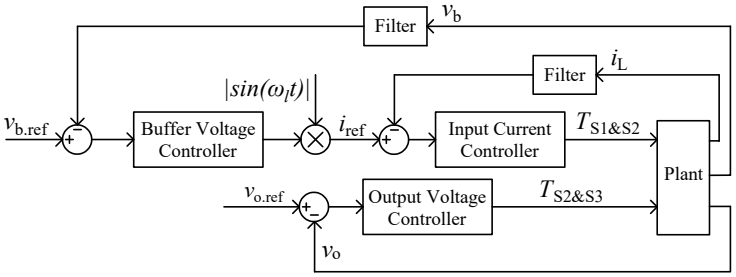


FIGURE 4.11: Control block diagrams for the two-stage PFC architecture and the stacked-switch PFC architecture. T_{SB} and T_{SH} refer to the on-time of S_B and S_H, respectively. $T_{S1\&S2}$ refers to the time duration when both S_1 and S_2 are turned on. $T_{S2\&S3}$ refers to the time duration when both S_2 and S_3 are turned on. ω_l is the angular line frequency.

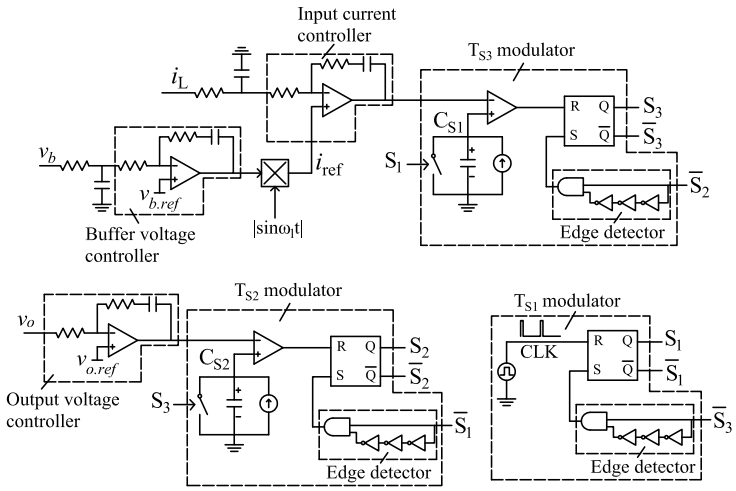


FIGURE 4.12: Control circuit implementation.

converter is chosen for its capabilities to achieve wide output voltage range, full-load-range ZVS, constant-frequency operation, and lower voltage stress than the active-clamp flyback converter.

The control block diagrams for the two-stage and stacked-switch PFC architectures are shown in Fig. 4.11. The stacked-switch architecture is controlled in a similar way as the two-stage architecture, and the main differences are the modulation variables. In the control diagram of the two-stage architecture, the on duration of S_B, T_{SB}, is modulated to shape the input current, and the off duration of S_B may be determined by the switching frequency or the zero-crossing of i_L. To realize the equivalent switching state, the stacked-switch architecture uses the time duration when both S_1 and S_2 are on, $T_{S1\&S2}$, as the modulation variable to shape the input current. The boost stage of the stacked-switch architecture is designed to operate in discontinuous-conduction mode (DCM) in this work, and the duty cycle of the boost stage can be calculated as

$$\begin{aligned} D &= \frac{T_{S1\&S2}}{T_s} \\ &= \sqrt{\frac{4P_oL(v_b - |v_{in}|)}{v_{in}^2 v_b T_s}}, \end{aligned} \tag{4.1}$$

where P_o is the output power and T_s is the switching period. From (4.1), D should vary with v_{in} to achieve sinusoidal input current, which is done by the input current controller in Fig. 4.11.

The two-stage architecture uses the on-time of S_H, T_{SH}, to control v_o, while the on-time of S_L is passively determined by the zero-crossing of i_{Lk} or the selected switching frequency. Similarly, the stacked-switch architecture uses the time duration when both S_2 and S_3 are on, $T_{S2\&S3}$, to emulate T_{SH}, and the time duration of State III is passively determined by the switching frequency. The duty cycle of the isolated stage (i.e., $\frac{T_{S2\&S3}}{T_s}$) is adjusted by the output voltage controller in Fig. 4.11 such that v_o remains constant at its reference value $v_{o.ref}$ regardless of the low-frequency ripple in v_b.

An analog circuit shown in Fig. 4.12 is designed to implement the control method for the stacked-switch architecture. The proposed control circuit is constructed with low-cost components such as logic gates, operational amplifiers, resistors, and capacitors, and no expensive micro-controller is needed. The switching frequency is determined by the frequency of the clock signal CLK. Detailed operating waveforms under the proposed modulation and

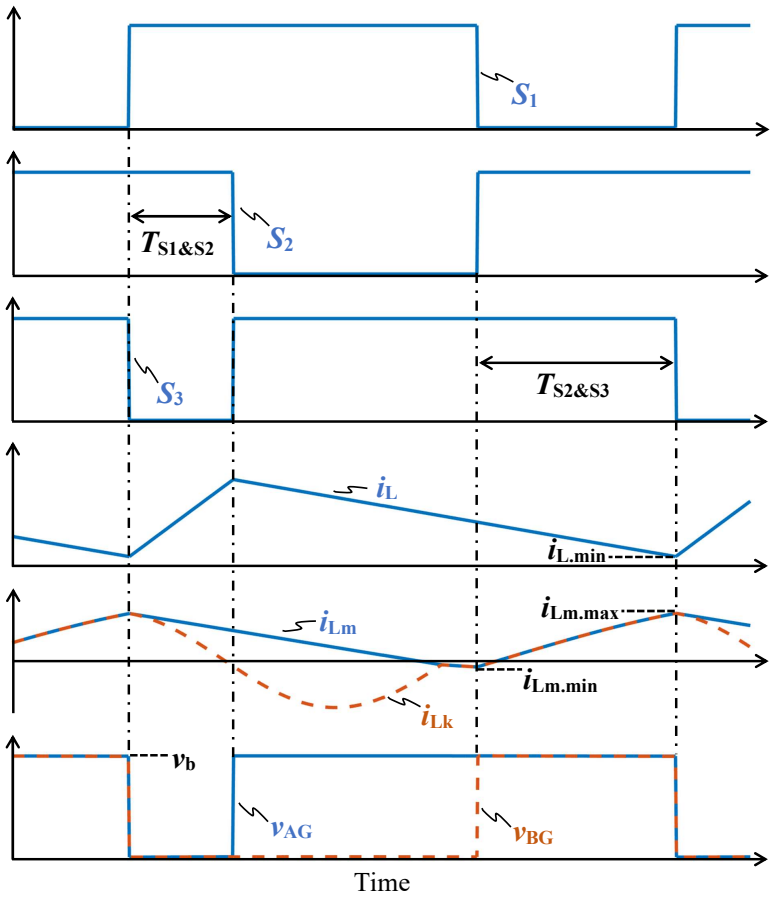


FIGURE 4.13: Operating waveforms under the proposed modulation and control method when the boost stage works in continuous-conduction mode and the AHB flyback stage works in resonant mode. v_{AG} is the switching node voltage of the boost stage and v_{BG} is the switching node voltage of the isolated stage.

control method are shown in Fig. 4.13. In the T_{S2} modulator, S_3 is used to reset the analog switch so that the C_{S2} only charges up when the circuits enter State II, allowing the output voltage controller to control $T_{S1\&S2}$. Similarly, S_1 is used to reset the T_{S3} modulator and C_{S1} is only charged when the circuit enters State I, allowing the input current controller to control $T_{S2\&S3}$.

4.3.2 Clamping State and Design of C_{in}

As with the existing ZVS boost PFC design, the C_{in} of the PFC front-end in the proposed architecture can be in the range of nF to provide a steady rectified sine-wave v_{Cin}. In this

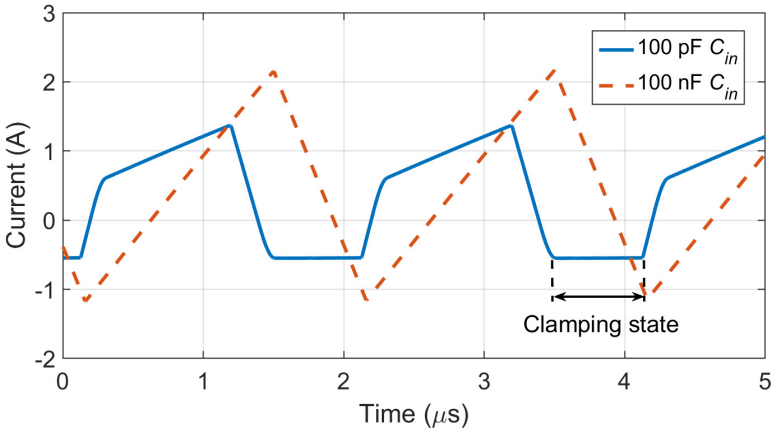


FIGURE 4.14: Operating waveforms of i_L under different C_{in} values. The waveforms are measured at 500 kHz switching frequency and 0.5 A average current.

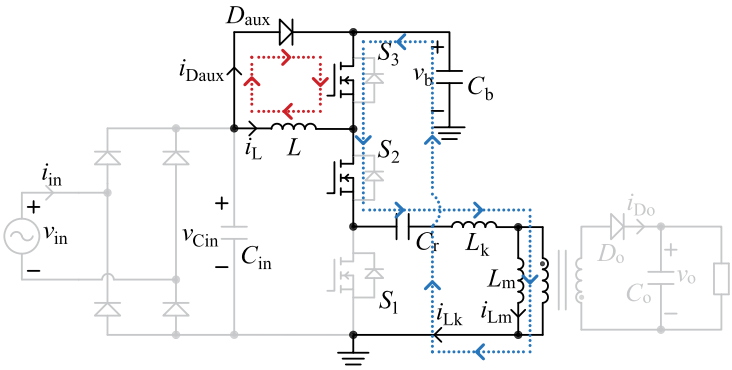


FIGURE 4.15: Clamping state. v_{Cin} is clamped at v_b and i_L remains unchanged during the clamping state. The current flow of i_L is highlighted in red and that of i_{Lk} is highlighted in blue.

thesis, it is found that reducing C_{in} can lead to several benefits including reduced inductor current ripple, reduced switching frequency, and minimized reversed energy to realize the ZVS turn-on of S_3. The waveforms of i_L under different C_{in} are compared in Fig. 4.14. A new operating state, which is termed clamping state as shown in Fig. 4.15, appears on top of the three operating states in Fig. 4.3 when C_{in} is reduced. The peak-to-peak ripple of i_L reduces from 3 A to 2 A when C_{in} is reduced from 100 nF to 100 pF. By comparison, it can be seen that smaller C_{in} enables the circuit to enter the clamping state earlier, leading to reduced current ripple under the same switching frequency or reduced switching frequency under the same current ripple. In the stacked-switch architecture, the energy to assist ZVS turn-on of S_1 and S_2 is from the isolated stage, and there is no need to control the negative

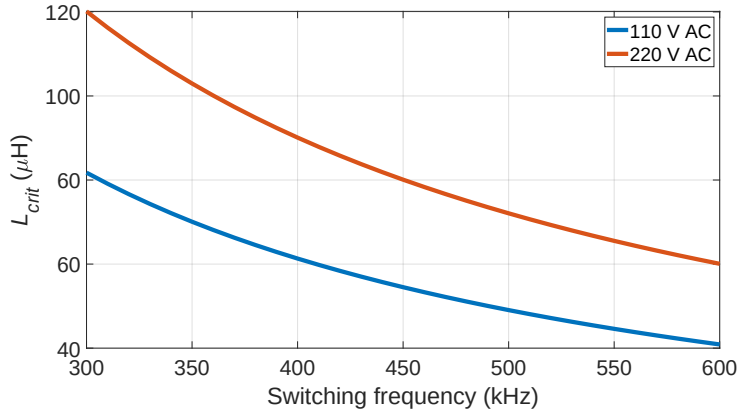


FIGURE 4.16: L_{crit} versus switching frequency under different AC voltage ($V_{b.max}$ = 400 V, P_o = 150 W).

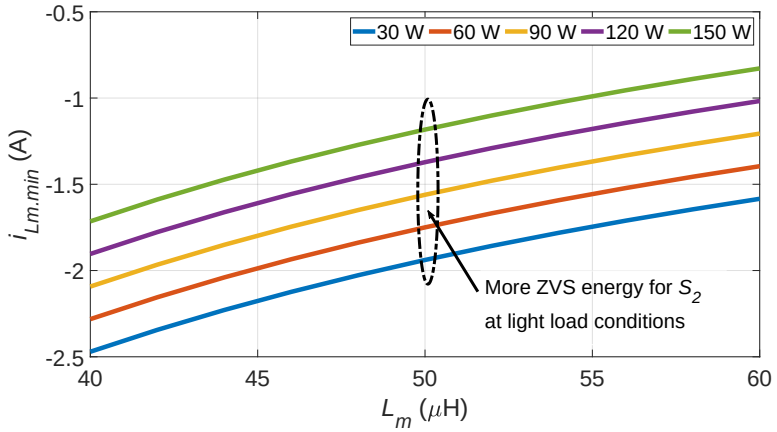


FIGURE 4.17: $i_{Lm.min}$ versus L_m under different power levels. The circuit parameters used to plot the figure are the same as Table. 4.3. There is more negative $i_{Lm.min}$ under lower L_m and lower power level.

current of i_L for ZVS, so reducing C_{in} to make the circuit enter the clamping state becomes a preferable design option. This is not possible with conventional ZVS boost converters, where the negative current must be adjusted to achieve ZVS, leading to variable switching frequency if the ZVS energy is minimized or high RMS current of i_L if the switching frequency is constant. Moreover, high-speed sensors and complicated calculations are not required in the stacked-switch architecture because the negative i_L is no longer a variable to be controlled.

During the clamping state, the maximum reversed energy stored in C_{in} is $0.5C_{in}v_b^2$, which only depends on C_{in} given that v_b is already designed. The energy will later be released back to L to discharge the output capacitance of S_3. Hence, one can easily minimize the reversed

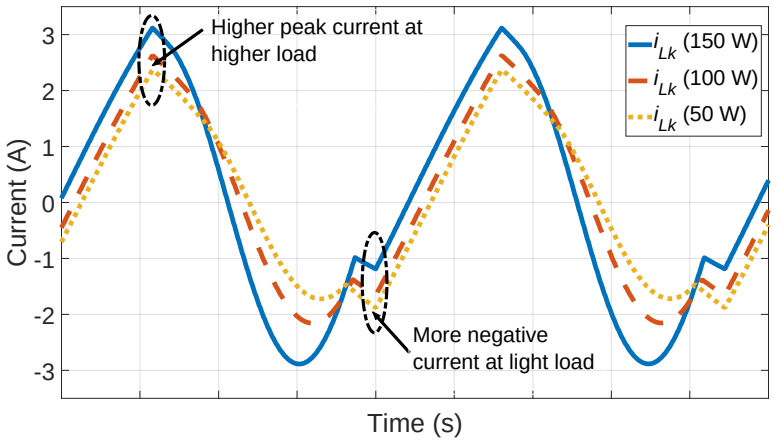


FIGURE 4.18: Waveforms of i_k under different power levels. The circuit parameters used to plot the figure are the same as Table. 4.3.

energy to C_{in} by minimizing C_{in}, and the minimal reversed energy should support the ZVS turn-on of S_3. The worst condition for the ZVS turn-on of S_3 is during the zero-crossing of v_{in} because i_L is theoretically zero, and the minimum C_{in} to guarantee the ZVS turn-on of S_3 during the zero-crossing of v_{in} can be calculated as

$$C_{in.min} = 2C_{oss}, \tag{4.2}$$

where C_{oss} is the output capacitance of S_1, S_2, and S_3.

4.3.3 Design of L

L works the same way as the boost inductor under constant-frequency operations. Higher L leads to lower ripple at the expense of larger core volume. The design target of L is to achieve high utilization of its energy storage while maintaining its ripple current as low as possible to maximise the efficiency performance. This can be done by designing L slightly lower than the critical inductance when L operates at continuous conduction mode. The critical inductance L_{crit} can be calculated as

$$L_{crit} = \frac{V_{ac.min}^2(V_{b.max} - |V_{ac.min}|)}{4P_o f_{sw} V_{b.max}}, \tag{4.3}$$

where $V_{ac.min}$ is the minimum amplitude of AC voltage, $V_{b.max}$ is the maximum buffer voltage, P_o is the output power, and f_{sw} is the switching frequency. The effects of switching frequency and AC voltage on L_{crit} are shown in Fig. 4.16. It is revealed that increasing switching frequency can effectively reduce L_{crit} so as the size of L.

4.3.4 Design of L_m

The design target of L_m is to have sufficient magnetizing current to fully discharge the output capacitance of S_2 when S_1 is turned off. Neglecting L_k, the minimum magnetizing current in each switching cycle, $i_{Lm.min}$, is

$$i_{Lm.min} = \frac{P_o}{nv_o} - \frac{(v_b - nv_o)nv_o}{2L_m v_b f_{sw}}, \tag{4.4}$$

where n is the winding turns ratio. From (4.4), reducing L_m leads to more negative magnetizing current to discharge the output capacitance and, hence, more margin to realize the ZVS turn-on of S_2, as shown in Fig. 4.17. Another observation from Fig. 4.17 is that $i_{Lm.min}$ is even lower when P_o is reduced, indicating that the worst-case scenario to realize ZVS of S_2 is at full-load rather than light-load conditions. This fact is also confirmed by the time-domain waveforms of i_{Lk} under different power levels, as plotted in Fig. 4.18. Therefore, the worst ZVS condition for S_1 is at the lightest load condition, and the worst ZVS condition for S_2 is at the full-load condition. In summary, our analysis shows that the AHB flyback converter can have full-range ZVS (i.e., S_1 and S_2 can achieve ZVS at their respective worst ZVS conditions) by designing a sufficiently small L_m under a constant switching frequency. To optimally design L_m, the switching frequency can be selected first. Then, L_m is gradually reduced until the ZVS turn-on of S_2 can be achieved at full-load conditions. Finally, L_m should be further slightly reduced to guarantee more ZVS margin to ensure more reliable operations with relatively low circulating power.

4.3.5 Design of Magnetics

The main purpose of magnetic design is to pursue high power density. The area product A_p mainly constrains the size of cores, and A_p can be calculated as

$$\begin{aligned} A_p &= A_w A_e \\ &= \frac{L I_{max}^2}{B_{max} J_{max} k_c}, \end{aligned} \tag{4.5}$$

where A_w is the core's window area, A_e is the effective area of the core, L is the inductance, I_{max} is the maximum inductor current, B_{max} is the maximum magnetic flux density, J_{max} is the maximum current density of the wire, and k_c is the copper fill factor. From (4.5), increasing switching frequency can reduce L and A_p, enabling the use of a smaller core without sacrificing I_{max}, I_{rms}, B_{max}, J_{max} and k_c. In this work, k_c is assumed to be 0.4, B_{max} is selected to be 200 mT, and J_{max} is 1000 A/cm^2. The design starts with selecting the magnetic core. Then, the switching frequency is increased to reduce L until the required A_p is lower than the area product of the selected core. After that, the number of turns is adjusted to reduce the magnetic flux density below B_{max}. Finally, the wire gauge is designed to occupy the core's window area as much as possible to improve the copper fill factor.

In addition to A_p, the dimensions of cores also affect the achievable power density. In this work, the dimensions of the cores are purposely designed to match other components' dimensions to enable high utilization of PCB space. In particular, the height of L and flyback transformer are similar for high utilization of the vertical space. The sum of the length of the two cores is designed similar to that of the electrolytic buffer capacitor, which eases the layout design and improves the power density. For better heat dissipation, planar cores are used due to their high area-to-volume ratios. After several iterations, EQ 20 and EQ-I 30 are selected for L and transformer, and the required switching frequency is calculated to be 450 kHz.

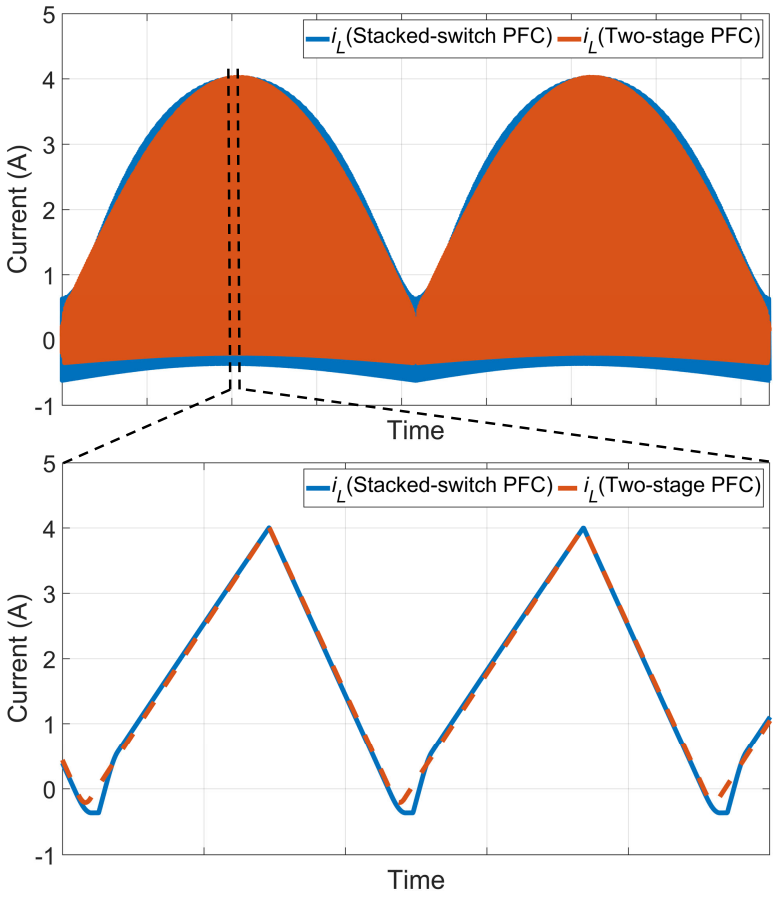


FIGURE 4.19: Comparison of boost inductor current waveforms between the two-stage architecture under CRM operations and the stacked-switch architecture under DCM operations (110 V AC, 150 W). The top figure shows the waveforms over a line period, and the bottom plot is a zoomed-in version of the top one.

4.3.6 Case Study

This subsection presents a case study to compare the performance between the stacked-switch architecture (Case I: DCM boost PFC converter and stacked-switch architecture with constant switching frequency) and the two-stage architecture (Case II: CRM boost PFC converter and two-stage architecture with variable switching frequency). The case study is on a 150-W, 28- V-output, and universal-input AC–DC application, and has the same specifications and components' parameters as the hardware prototype in the experimental verification. Both cases use GaN switch, NV6117, to implement all the switches at the primary side. Despite the varying switching frequency, CRM boost converter is selected for the two-stage architecture

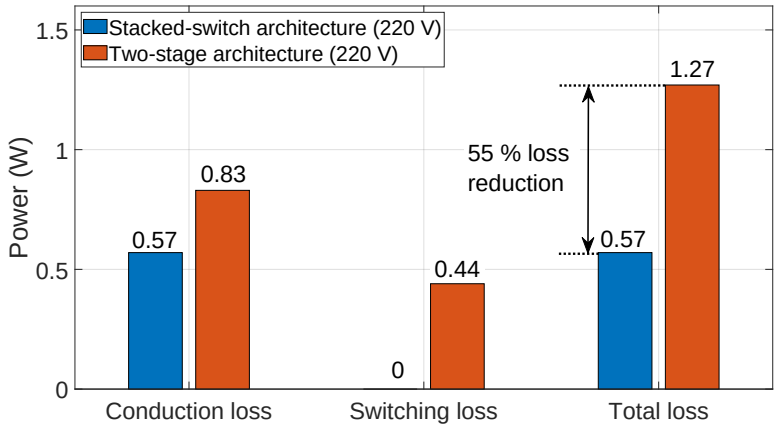


FIGURE 4.20: Comparison of power losses in the intermediate semiconductors between the two cases. (220 V AC, 150 W)

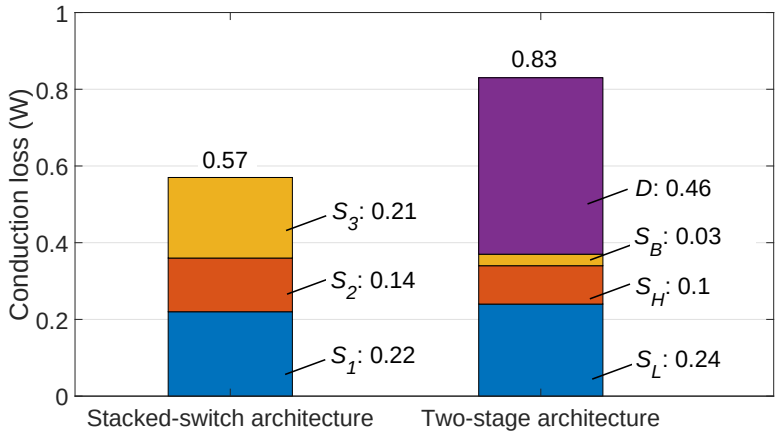


FIGURE 4.21: Breakdown of the conduction loss at 220 V AC and 150-W output.

because it achieves the lowest switching loss compared to DCM and CCM operations, which is essential for high-frequency operations. As the operating waveforms and power losses of the isolated transformer and secondary-side rectifier are the same in both cases, they are excluded from the comparison.

The comparison starts with the current waveforms of the boost inductor. The waveforms are measured at low-line conditions, where the maximum energy storage of L occurs, to compare the current ripple between the two cases in their worst conditions. The two cases are purposely designed to have the same peak current (at around 4 A) and maximum magnetic energy storage (i.e., $0.5Li_L^2$), as shown in Fig. 4.19. Although Case I has a higher inductor current ripple than Case II due to the constant frequency operations, the power losses of the

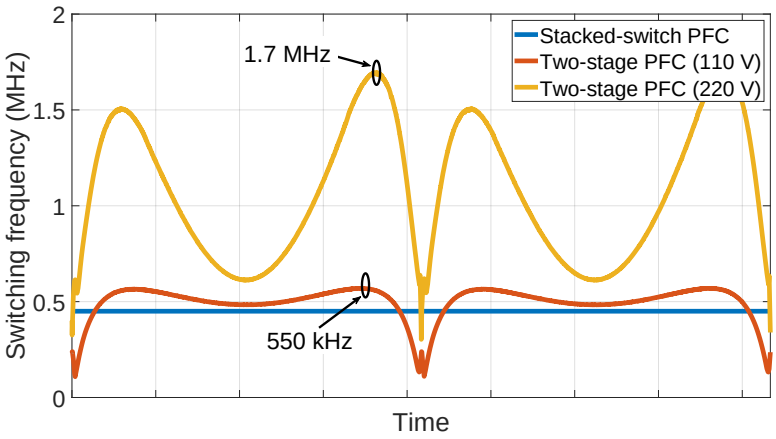


FIGURE 4.22: Comparison of the switching frequency of the boost PFC front end between the two-stage architecture and the stacked-switch architecture. The switching frequency of the CRM boost converter in the two-stage architecture increases at high-line conditions, and the maximum switching frequency is around 1.7 MHz. The stacked-switch architecture maintains a constant 450-kHz switching frequency under different AC voltages and power levels.

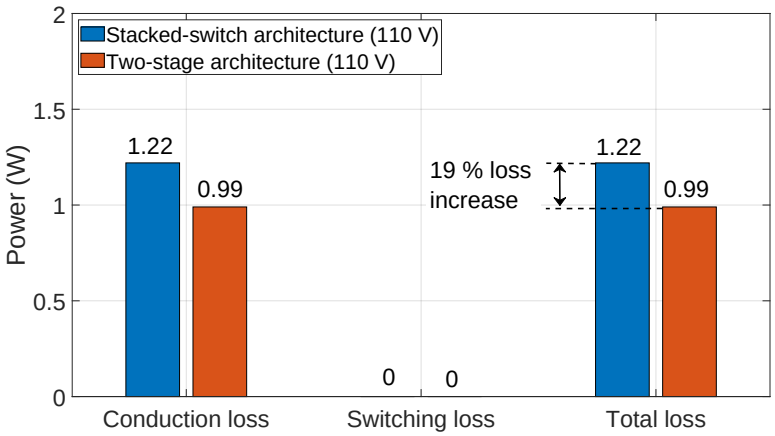


FIGURE 4.23: Comparison of power losses in the intermediate semiconductors between the two cases. (110 V AC, 150 W)

two cases are nearly the same because the RMS current of the stacked-switch architecture (1.66 A) is only 3 % higher than that of two-stage architecture (1.61 A).

The main difference in power losses between the two cases is in the intermediate semiconductors (i.e., S_1, S_2, and S_3 in Case I, and S_B, S_H, S_L, and D in Case II). The conduction loss and switching loss of these semiconductors are calculated in Fig. 4.20. It is found that the stacked-switch architecture has lower conduction loss and switching loss than the two-stage architecture at 220 V AC. In high-line conditions, the conduction loss is higher with

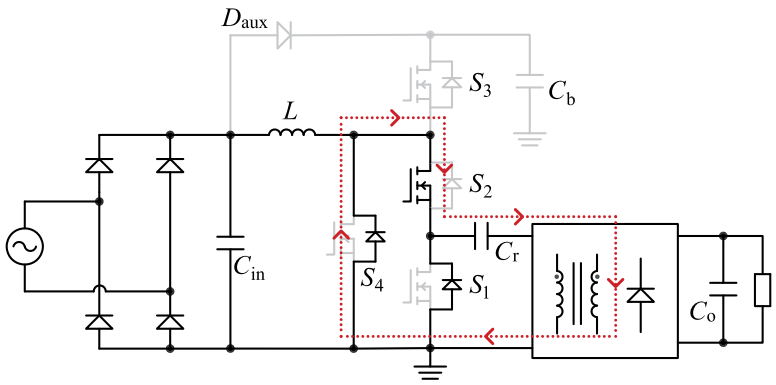


FIGURE 4.24: Proposed method of connecting S_4 in parallel with S_1 and S_2 to reduce the conduction loss. S_4 is turned on together with S_1 and turned off together with S_2 to reduce the current stress on S_1 and S_2. Similar to S_1, S_4 can realize ZVS by utilizing the transformer current highlighted in red to discharge its output capacitance.

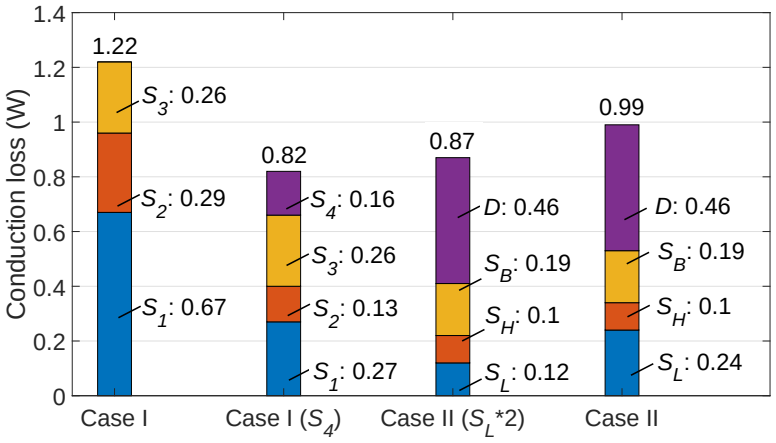


FIGURE 4.25: Breakdown of the conduction loss at 110 V AC and 150-W output. Paralleling S_4 helps Case I to achieve lower conduction loss than Case II using two switches in parallel to implement S_L.

the two-stage architecture as the two-stage architecture uses a D while the stacked-switch architecture replaces it with an active switch S_3, as demonstrated in Fig. 4.21. Meanwhile, the switching loss is higher with the two-stage architecture as (i) a CRM boost converter can only achieve valley switching of S_B in high-line conditions, while the stacked-switch architecture can realize full-range ZVS for all active switches and (ii) the switching frequency of a CRM boost converter increases in high-line conditions, which further increases the switching loss. For example, the maximum switching frequency can increase from around 550 kHz to around 1.7 MHz to realize the valley switching of S_B in Case II when the input voltage changes from

110 V to 220 V, as shown in Fig. 4.22. In comparison, the stacked-switch architecture utilizes i_{Lk}, whose value doesn't change with AC voltages, to discharge the output capacitance of S_1, enabling constant switching frequency under different AC voltages. It should be noted that the above analysis assumes that ideal valley switching is achieved in Case II, which is generally difficult in practical implementations due to the requirements of ultra-fast valley detection (e.g., reliable valley detection at 1.7 MHz).

However, in low-line conditions, Case I is shown to have higher losses than Case II, assuming both cases can achieve full-range ZVS of all active switches (i.e., zero switching losses), as shown in Fig. 4.23. The main reason is that both i_L and i_{Lk} flow through S_1 and S_2 in Case I, resulting in higher conduction loss than Case II in high current situations. Here, a method is proposed to reduce the conduction loss, as illustrated in Fig. 4.24, where a switch S_4 is connected in parallel with S_1 and S_2. The use of S_4 can reduce the current stress of two switches (i.e., S_1 and S_2), and S_4 itself can realize ZVS by utilizing the transformer current highlighted in Fig. 4.24. In contrast, directly paralleling a switch in the conventional two-stage architecture can only reduce the conduction loss of one switch and can increase switching loss if the switch is paralleled with S_B due to increased output capacitance and the potential hard-switching operations. Fig. 4.25 compares the conduction loss of both cases with and without the paralleled switch. It is found that Case I has lower conduction loss than Case II when both cases adopt a paralleled switch, which has been a standard engineering practice in high-current situations [70].

In summary, the case study shows that the stacked-switch architecture 1) has similar worst-case losses on L to the two-stage architecture (only 3 % higher RMS current), 2) is more efficient in high-frequency applications due to the full-range ZVS feature (55 % loss reduction at 220 V AC), and 3) is easier for practical implementations thanks to the constant-frequency operations (the maximum switching frequency is suppressed from 1.7 MHz to 450 kHz). The case study also finds that the stacked-switch architecture may have higher conduction loss than the two-stage architecture in high-current situations. However, it is demonstrated that this issue can be resolved with a paralleled switch and that paralleling a switch in the stacked-switch architecture can achieve more loss reduction than in the two-stage architecture.

TABLE 4.3: Parameters of the prototype.

Parameters	Values
Input voltage (v_{in})	Universal
Output rating (p_o, v_o)	150 W, 28 V
Buffer voltage (V_b)	400 V
Switching frequency	450 kHz
Winding turns ratio	17:3
Leakage inductance L_k	7 μH
Magnetizing inductance L_m	50 μH
Boost inductance L	45 μH
Resonant capacitance C_r	12 nF
Buffer capacitance C_b	68 μF
Input capacitance C_{in}	102 pF
Output capacitance C_o	660 μF

TABLE 4.4: Components of the prototype.

Components	Part number
Buffer capacitor	450BXW68MEFR12.5X45
EMI filter inductors	XGL4040-472
EMI filter capacitors	C2225C474MBRACTU
Diode bridge	C6D06065Q-TR
$S_1 \sim S_3$	NV6117
Synchrnous rectifier	EPC2034
Boost inductor L	EQ20
Transformer	EQ30 + I30
Output capacitor C_o	EEH-AZS1V331B

4.4 Experimental Results

A 150-W-universal-input prototype based on Fig. 4.10 is built to verify the stacked-switch architecture. The design parameters and components of the prototype are summarized in Table. 4.3 and 4.4, respectively. The switching frequency is designed at a constant 450 kHz to use smaller boost inductor and EMI filters than the two-stage architecture. D_o is replaced with a synchronous rectifier to reduce conduction loss. The winding ratio is designed to reduce the voltage stress of the synchronous rectifier below 150 V. L_k is measured after the transformer is built. Then, C_r is designed to resonate with L_k at the switching frequency to achieve zero-current turn-off of the synchronous rectifier. C_b is designed to buffer the twice-line ripple power with around 5 % voltage ripple, whose effects can be easily compensated by the AHB

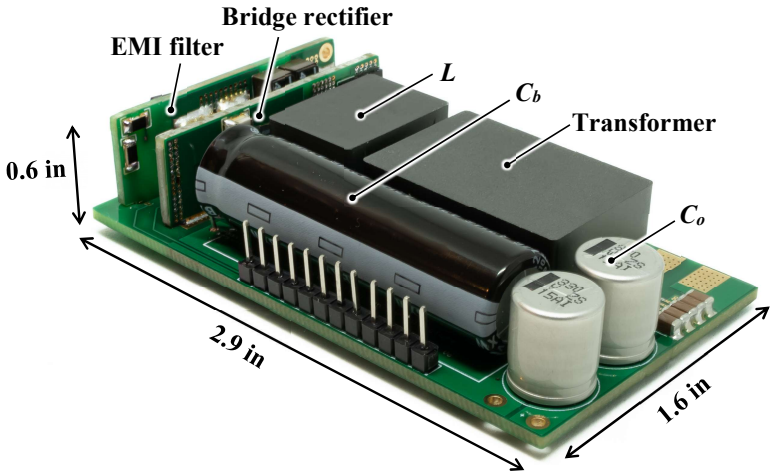


FIGURE 4.26: Hardware prototype. The prototype measures 53.9 W/in^3 power density by box volume.

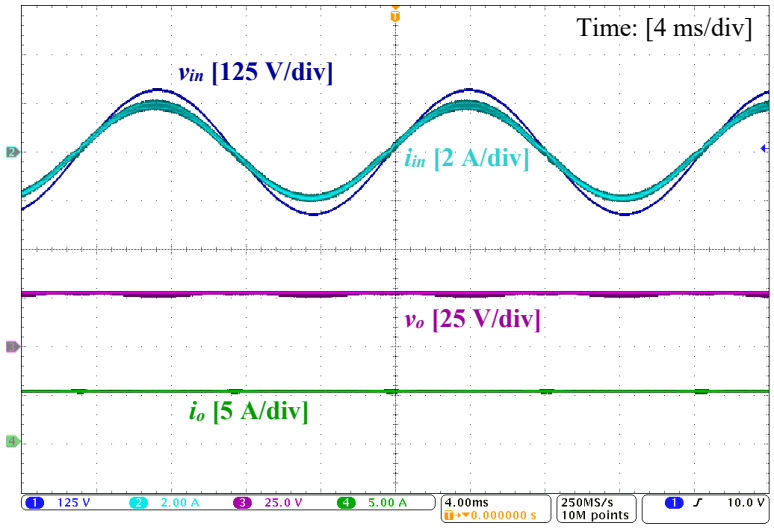


FIGURE 4.27: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 110 V AC and 150 W output.

flyback stage. The average voltage of C_b is designed at 400 V to cover the universal input voltage range. The prototype achieves 53.9 W/in^3 power density, as shown in Fig. 4.26.

The stacked-switch architecture, together with the proposed control scheme, can achieve high-quality-sinusoidal input current and constant output voltage under both high-line and low-line conditions, as demonstrated in Fig. 4.27 and 4.28. The ripple of v_o is measured to be 2 % as shown in Fig. 4.29 and there is nearly no double-line frequency component in v_o, meaning that the 120 Hz ripple is actively buffered into C_b. An overview of other waveforms,

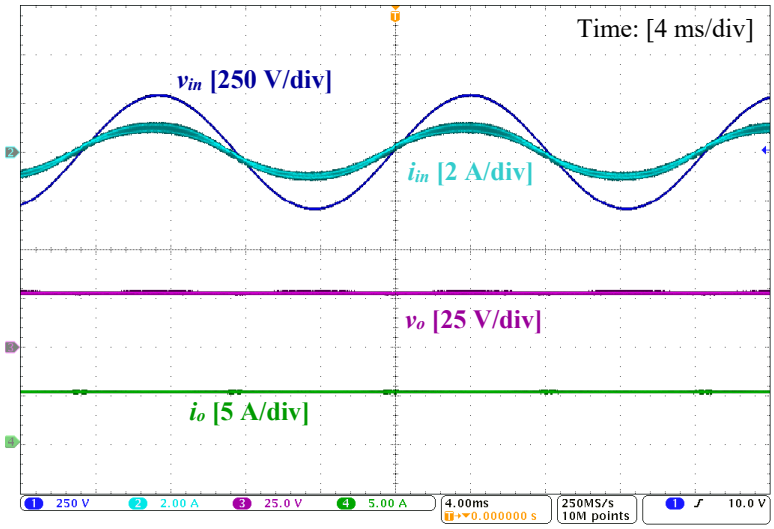


FIGURE 4.28: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 220 V AC and 150 W output.

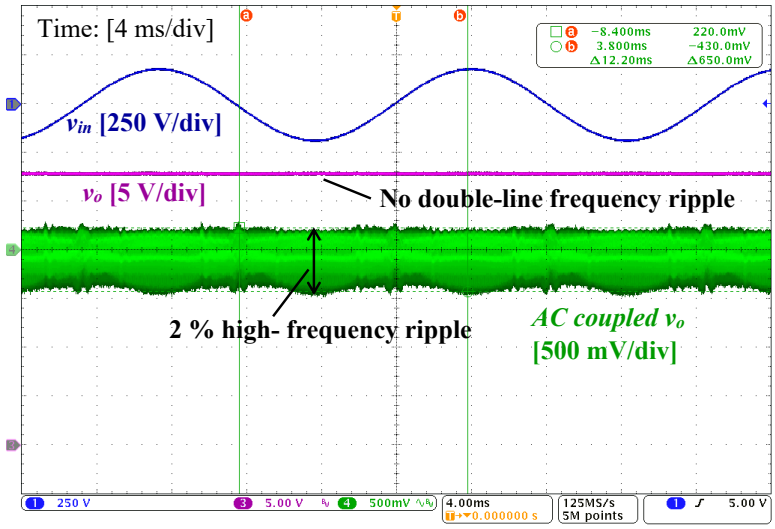


FIGURE 4.29: Measured output voltage ripple at full-load condition. The output voltage ripple is around 2 %.

including i_L, i_{Lk}, and v_b, is measured in Fig. 4.30. In particular, i_L operates at DCM to achieve high utilization of energy storage, and its minimum value is well clamped above -1 A by minimizing C_{in}. There is negligible double-line frequency ripple in i_{Lk}, which also verifies that most of the low-frequency ripple power is buffered into C_b and does not propagate to the load side under the proposed control scheme. v_b is well regulated at the designed reference value and contains a slight double-line frequency ripple, as expected.

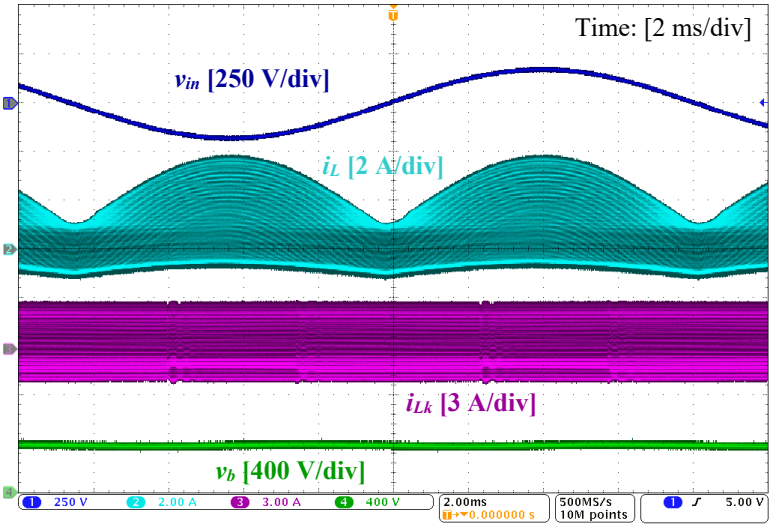


FIGURE 4.30: Overview of operating waveforms of v_{in}, i_L, i_{Lk}, and v_b at 110 V AC.

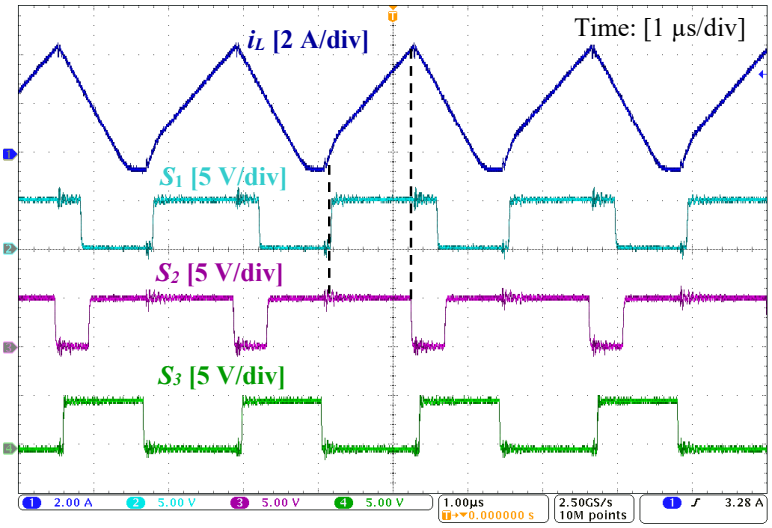


FIGURE 4.31: Detailed operating waveforms of i_L, S_1, S_2, and S_3.

Detailed operating waveforms are also measured to verify the operating principle. According to Fig. 4.31 and 4.32, i_L increases when both S_1 and S_2 are turned on, and the transformer is charged when both S_2 and S_3 are on, which complies with the operating principle. Fig, 4.33 demonstrates that i_{Do} resonates to zero before S_1 is off, enabling zero-current turn-off of the synchronous rectifier.

All switches can achieve ZVS at their worst ZVS conditions, as shown from Fig. 4.34 to Fig. 4.36, demonstrating full-range ZVS capability. The prototype achieves 92.9 % peak

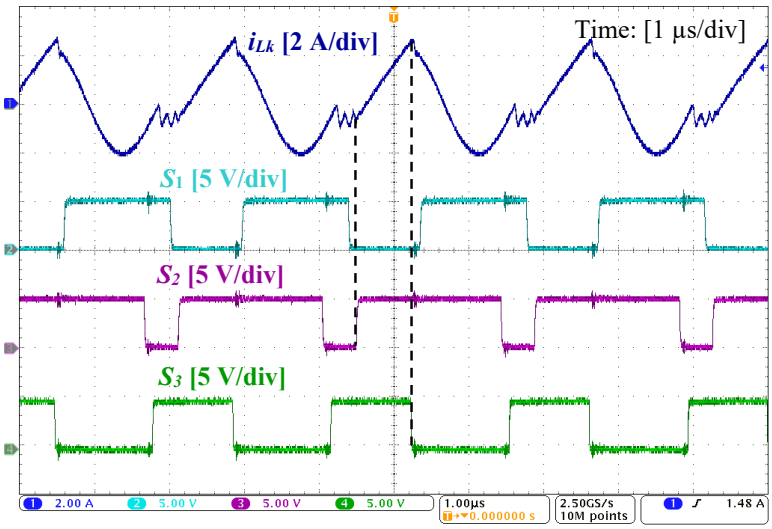


FIGURE 4.32: Detailed operating waveforms of i_{Lk}, S_1, S_2, and S_3.

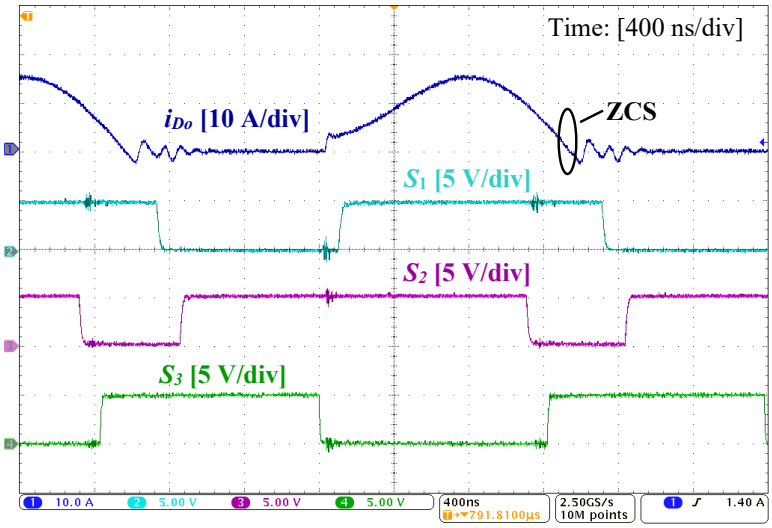


FIGURE 4.33: Detailed operating waveforms of i_{Do}, S_1, S_2, and S_3.

efficiency under 220 V AC and above 86 % efficiency at 30 % load as shown in Fig. 4.37. The magnetics are found to contribute to the majority of the losses, as shown in Fig. 4.40, which will be a barrier towards higher switching frequency. Another barrier toward higher frequency is delay and other constraints in the control circuit. At high switching frequencies, the on-duration of switches reduces and becomes close to the minimum on-time of the logic circuits, leading to challenges in designing a reliable control circuit. The deadtime loss will also be a problem as the duration of body diode conduction increases at higher switching

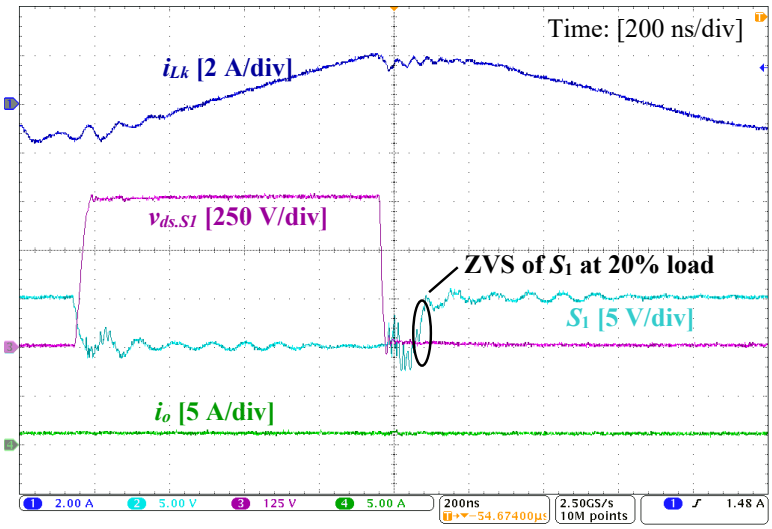


FIGURE 4.34: ZVS waveforms of S_1 under 20 % load condition (220 V AC). This is the worst condition for ZVS of S_1 as $i_{Lm.max}$ is minimal.

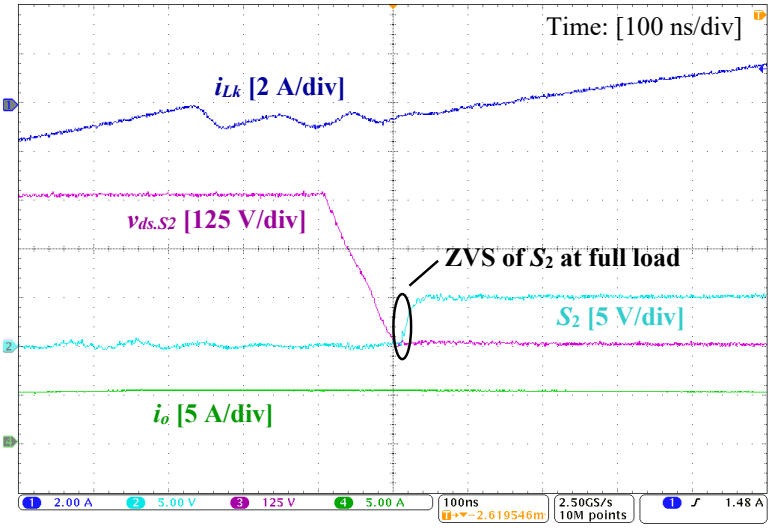


FIGURE 4.35: ZVS waveforms of S_2 under full load condition (220 V AC). This is the worst condition for ZVS of S_2 as $i_{Lm.min}$ is closest to zero.

frequency, especially for GaN devices due to their higher voltage drop (around 3 V) at reverse conduction than the Si counterparts (around 1 V).

C_{in} is increased from 102 pF to 1 nF to verify its effects, and it is found that increasing C_{in} does result in a higher ripple current on L as shown in Fig. 4.38 and Fig. 4.39, leading to reduced efficiency, especially at the light load conditions. There is more reversed energy back to C_{in} when C_{in} increases, and the reversed energy stored in C_{in} must be released such that

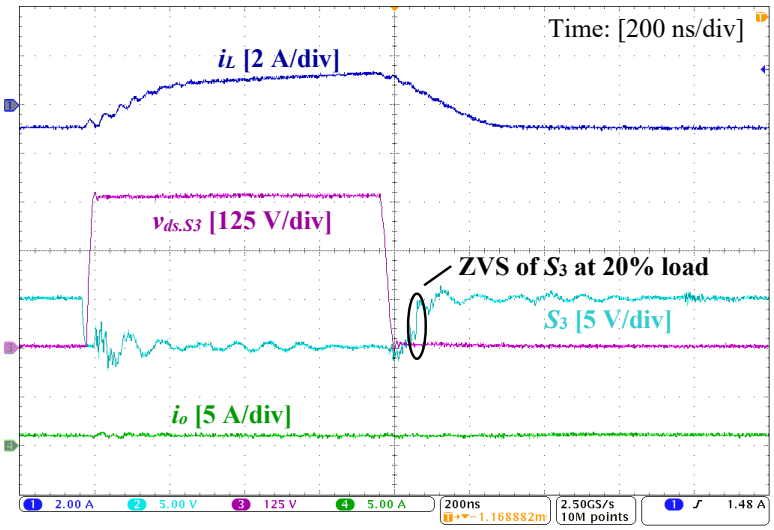


FIGURE 4.36: ZVS waveforms of S_3 under 20 % load condition and at the zero-crossing of v_{in} (220 V AC). This is the worst condition for ZVS of S_3 as the energy stored in i_L is minimal.

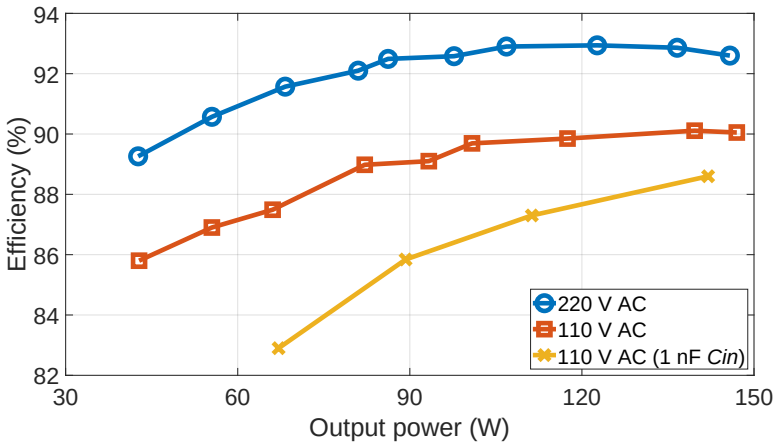


FIGURE 4.37: Measured efficiency curves under different AC voltages and output power.

the converter can drain power from the AC source to achieve sinusoidal input current. Hence, increasing C_{in} can result in increased circulating energy, causing higher current ripple in i_L and higher distortion in i_{in}. The increase of C_{in} may also cause a dead angle when C_{in} is so high that the reversed energy back to C_{in} cannot be fully released in a switching period. The total harmonic distortion (THD) of i_{in} and power factor are measured in Fig. 4.41. The prototype has above 0.9 power factor and below 7 % THD of i_{in} across a wide load range and input range, verifying that the input current is actively controlled and shaped to be sinusoidal.

TABLE 4.5: Comparison to recent publications with similar specifications

	[71]	[28]	[72]	[59]	[73]	[74]	This work
Year	2018	2019	2021	2021	2022	2022	2022
Number of magnetics	2	4	2	2	3	2	2
Number of FETs	4	10	4	8	6	7	4
ZVS of all FETs	×	×	×	√	×	×	√
Galvanic isolation	√	√	×	√	√	√	√
Constant switching frequency	×	×	√	√	√	×	√
Active 120/100 Hz ripple buffering	√	×	√	×	√	√	√
Control implementation	Analog	Digital	Digital	Digital	Digital	Analog	Analog
Output voltage (V)	20	12	100	20	28	28	28
Power (W)	100	150	100	330	170	140	150
Peak efficiency (%)	93.4	92	92.5	93.4	94.2	94.2	92.9
PFC stage switching frequency (kHz)	45	2000	50	400	60	108	450
Power density (W/in^3)	30	50	18.6	37.9	26.2	22.8	53.9

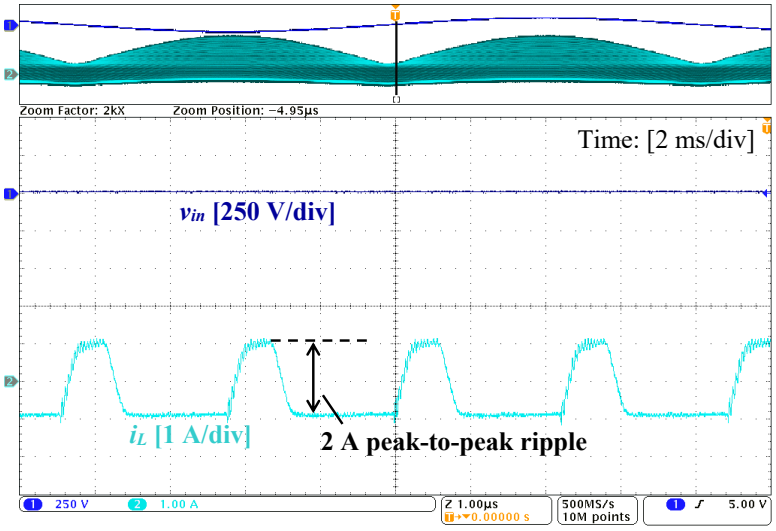


FIGURE 4.38: Operating waveform of i_{Lin} at the zero-crossing of v_{in} with 102 pF C_{in}

A comparison with other recently published PFC converters at similar power levels is summarized in Table. VI. The comparison shows the proposed solution has the highest power density and is the only one that achieves all the beneficial functions (i.e., ZVS of all switches, galvanic isolation, constant switching frequency, and active 100/120-Hz buffering). Meanwhile, the proposed solution uses the fewest number of magnetics and active switches and can be controlled with simple analog circuits. Although the proposed solution does not achieve

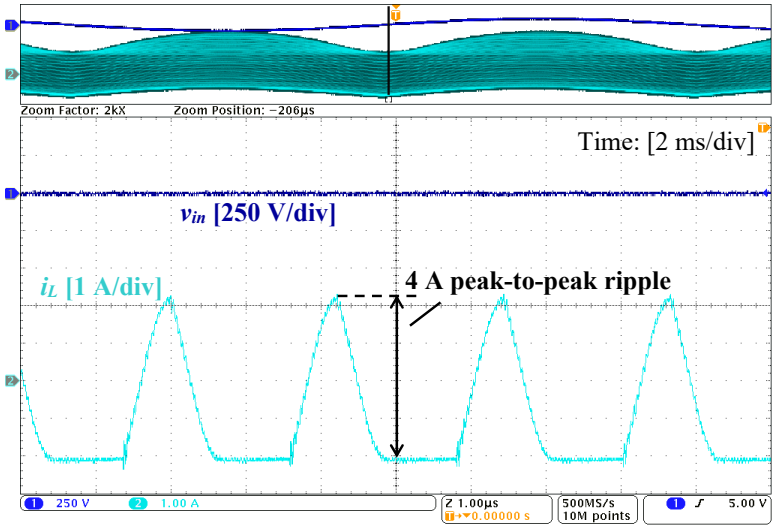


FIGURE 4.39: Operating waveform of i_{Lin} at the zero-crossing of v_{in} with 1000 pF C_{in}

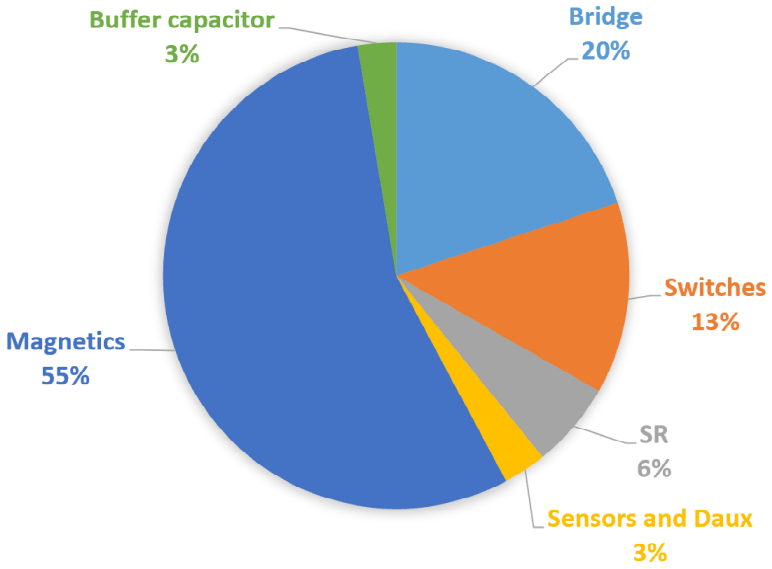


FIGURE 4.40: Loss distribution under 110 V AC and full-load output.

the highest efficiency among all solutions in Table. VI, its efficiency is comparable to (i.e., only 1.3 % lower than) the best-in-class solution in the industry [74], which is based on a bridge-less PFC converter and has been comprehensively optimized. To improve efficiency, future work may focus on 1) developing bridgeless versions of the stacked-switch architecture, 2) considering better magnetic design including material selection, winding layout, core geometry, and the number of turns, 3) optimizing the switching frequency and other circuit

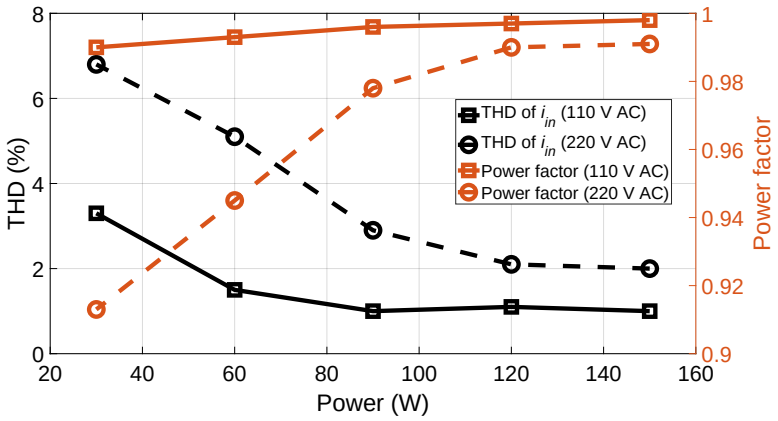


FIGURE 4.41: THD and power factor of the prototype under different input voltage and load conditions. The curves under 110 V and 220 V are plotted in solid lines and dashed lines, respectively.

parameters to achieve a better trade-off between efficiency and power density, and 4) using more efficient topologies, such as LLC converter, as the second stage.

4.5 Summary

A new PFC architecture is investigated in this chapter. The proposed stacked-switch PFC architecture requires fewer components than the conventional two-stage architecture while realizing full-load-range ZVS of all switches, leading to higher power density and lower cost. The stacked-switch architecture can directly utilize the well-developed control methods for the two-stage architecture, enabling simple control implementation with low-cost analog circuits and constant switching frequency. The performance of the stacked-switch PFC architecture is verified by a 150-W prototype, demonstrating a high power factor, constant output voltage, and full-range ZVS with 92.9 % peak efficiency and 53.9 W/in^3 power density.

CHAPTER 5

Star Power Factor Correction Architecture

5.1 Background

Single-phase universal-input AC–DC converters are widely adopted in many applications such as wall adapters and LED lighting. In these applications, it is highly desirable to achieve high efficiency, power density, and cost-effectiveness. A two-stage power-processing architecture is generally the de-facto solution in these applications where the power level is greater than 75 W (in which case power-factor-correction (PFC) is mandatory), with the first stage being a PFC converter (typically a boost converter) and the second stage an isolated DC–DC converter (such as a half-bridge based isolated converter), as shown in Fig. 5.1 [9]–[12].

Elevating the switching frequency is an effective method for reducing the volume of passive components and thereby increasing the overall system's power density. While a switching frequency from multi-kHz up to multi-MHz for the second DC–DC stage has been widely reported [75]–[77], that of the first boost PFC stage is generally limited to around 100 kHz range even when GaN devices are utilized [32], [78]. The challenge with increasing the switching frequency in the boost PFC stage is mainly threefold:

1) Challenges in full-range soft switching: Most boost PFC front end operates in the continuous-conduction-mode (CCM), critical-mode (CRM) or discontinuous-conduction-mode (DCM), or their combinations [79]. However, all three modes of operation cannot realize full-range ZVS [27], [73], leading to increased switching loss at high frequency;

2) Challenges in control electronics: CRM boost PFC converter generally requires peak current and zero-crossing detection circuits to realize valley switching [80], [81]. However,

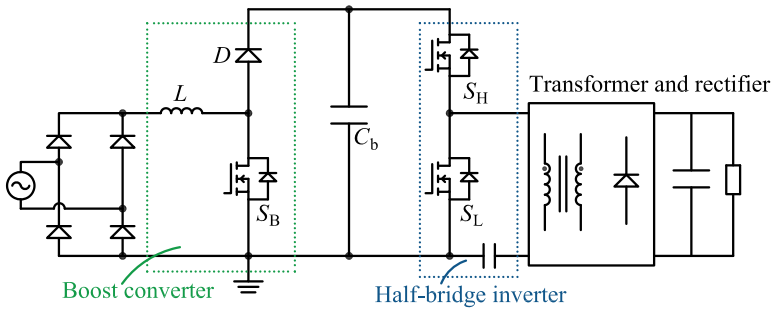


FIGURE 5.1: Two-stage PFC architecture based on boost PFC front end and half-bridge isolated DC–DC stage.

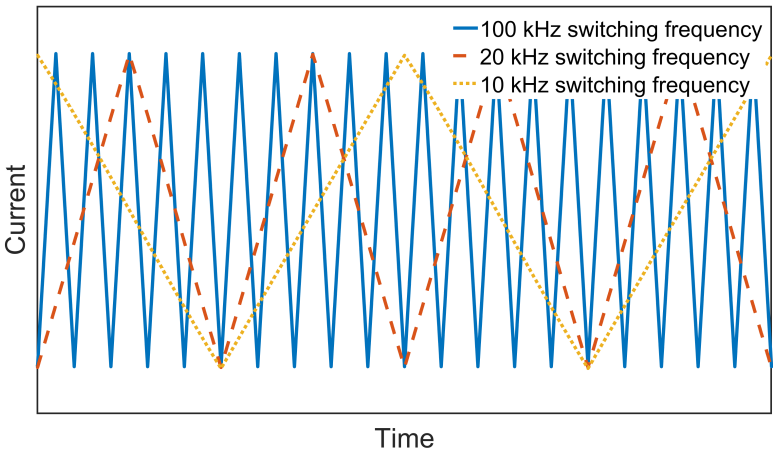


FIGURE 5.2: Inductor current waveforms of CRM operation at different switching frequencies. The current waveforms have the same average value. The current ripple doesn't change with the increase of switching frequency.

high-frequency operation demands high-bandwidth electronics (e.g., controllers, sensors, comparators), which are generally expensive and even challenging to design [82];

3) Challenges in magnetics: The inductor current in CRM or DCM boost PFC converters contains a high portion of high-frequency components, and the peak-to-peak inductor current ripple must be at least twice higher than the average inductor current. Given that (i) the amplitude of the high-frequency current components is basically invariant and that (ii) the rate of change of current increases at higher frequency (see Fig. 5.2), increasing the frequency will lead to higher AC losses in PFC inductor [83]. The high current ripple and the increased AC losses impose significant challenges on the inductor design at a higher switching frequency.

Extensive efforts have been made to solve the three challenges above. Among them, quasi-square-wave (QSW) boost converters are the best known solutions [34], [84]–[87]. While the challenges with full-range soft switching can be tackled through QSW operation and its variations [35], [36], [56], [88], those with the control electronics and magnetics remain unsolved. The reason is that high-speed peak/valley current control and additional digital calculations are needed for minimizing the root-mean-square (RMS) current to improve efficiency and that the inductor current ripple is even greater than that in CRM boost PFC converter.

Motivated by these challenges, this thesis presents a star PFC architecture to improve the power density and efficiency performance of single-phase universal input AC–DC converters. Instead of focusing on each stage of a PFC system independently, this architecture merges the two stages in a way that can overcome the challenges of the PFC stage while maintaining the performance of the second stage. In particular, by actively integrating the second stage's high-frequency transformer current into the first PFC stage, the star architecture can realize (i) CCM operation in the PFC inductor, leading to reduced current ripple and associated core and conduction losses, (ii) full-range ZVS of all active switches, leading to reduced switching losses, with (iii) simple and low-cost analog control circuits. With an appropriate selection of circuit topology, the star architecture can be further operated at a constant switching frequency, which is convenient for hardware design and implementation. These features of the star architecture, as summarized in Table. 5.1, fundamentally enable simultaneous performance improvement in efficiency and power density over existing two-stage architecture at high switching frequency ranges.

5.2 Operating Principle of Star Architecture

The star architecture is derived by adding an auxiliary S_A to the conventional two-stage architecture, as shown in Fig. 5.3. S_H in the star architecture has the same function as S_H in the two-stage architecture (i.e., controlling the amount of charge flowing out of C_b), so they have the same name despite that their positions are different. It is worth mentioning that the

TABLE 5.1: Comparison of boost PFC stage's performance between the star architecture and the two-stage architecture.

Architecture	Two-stage architecture			Star architecture
Operating mode	CCM	CRM	QSW	CCM
Current ripple on L	Small	Large	Largest	Small
Control complexity	Simple	Medium	Very complicated	Simple
Analog control	Yes	Yes	No	Yes
Expensive micro-controller	No	No	Yes	No
Switching frequency range	Constant	Wide variation	Wide variation	Constant
ZVS range	No ZVS	Partial ZVS	Full ZVS	Full ZVS
Possible switching frequency	Low	Medium	High	High
Power density	Low	Medium	High	High

total number of active switches is the same as that of the two-stage architecture based on the QSW boost PFC front end. The two stages in the star architecture feature a star connection of S_A, S_H, and D. This architecture is therefore named star PFC architecture.

Compared to the conventional two-stage solution where the operations of the first and the second stage are fundamentally decoupled, the star architecture provides the opportunity to integrate the two stages in a way that makes it possible to leverage the second stage's current to assist with the soft-switching of the first PFC stage. As shown in Fig. 5.4, by including S_A, the star architecture features a unique operating state where the second stage's primary transformer current, i_{pri}, can directly flow into the first stage and actively participate in the commutation process of S_B, i.e., the current through S_B, $i_{SB} = i_L - i_{pri}$. Due to the two degrees of freedom (i.e., i_L and i_{pri}) in determining i_{SB}, i_L does not needs to be bi-polar as CRM and QSW boost PFC do to realize the ZVS turn-on of S_B. In fact, so long as $i_{pri} > i_L$, $i_{SB} < 0$, resulting in ZVS condition, even if i_L is uni-polar. Therefore, simultaneous CCM operation of the boost inductor (with a uni-polar current profile) featuring reduced current ripple and ZVS of S_B are possible. Here, it should be highlighted that (i) the operation of the boost PFC stage is identical to the conventional CCM boost converter except for a short S_B's ZVS transition process, (ii) the second stage's operations remain unchanged, and (iii) constant operating frequency can be achieved by selecting a proper circuit topology and modulation method for the second stage.

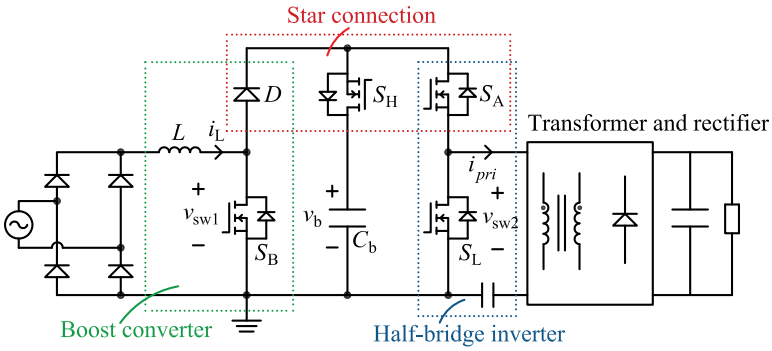


FIGURE 5.3: Star PFC architecture.

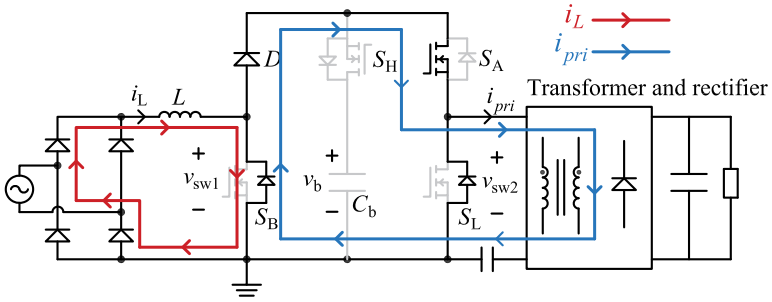


FIGURE 5.4: Key operating state of the star architecture enabling CCM operation and ZVS of S_B. The blue current path refers to the high-frequency transformer current in the isolated stage and the red path refers to the current flow of the boost inductor. The drain-source voltages of S_B and S_L can be discharged to zero if the blue current flow is greater than the red one.

Besides the advantages of CCM operations and ZVS of S_B, the star architecture also has the advantage of a low-cost control implementation over the two-stage architecture. The fundamental reason is that the ZVS of S_B is achieved through utilizing the transformer current of the second stage in the star architecture and the second stage is simply a DC–DC converter having a nearly constant input voltage rather than the wide varying sine-wave input seen by the boost stage, allowing full-range ZVS via simply designing its circuit parameters properly and without any active control. In contrast, the ZVS condition of S_B in the QSW boost converter varies in a wide range under different input voltages, making it hard to ensure ZVS via solely designing the circuit parameters properly and mandating the use of expensive digital controllers and high-speed current sensor to minimize the RMS current.

An example of constant-frequency-operated star architecture is discussed in more detail below. It is worth mentioning that conventional variable switching frequency modulation techniques

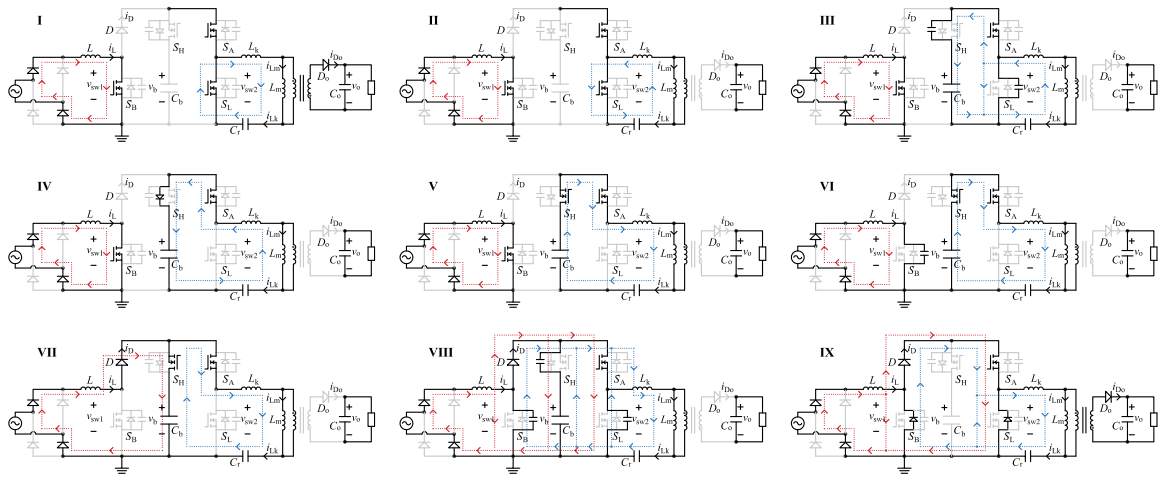


FIGURE 5.5: Operating states of the star architecture when the second stage is the asymmetrical half-bridge flyback and $T_{on.SB} \geq T_{on.SL}$. The current flows of i_L and i_{Lk} are highlighted in red and blue, respectively.

to improve the efficiency and/or EMI performances, as proven in commercial products, can also be applied [89], [90].

5.2.1 Examples of Star PFC Operations

The asymmetrical half-bridge (AHB) flyback converter is taken as an example for the isolated stage to illustrate the detailed operations of the star architecture. The operating states and detailed waveforms are shown from Fig. 5.5 to Fig. 5.8. In particular, when $T_{on.SB} \geq T_{on.SL}$, the system operates as Fig. 5.5 and Fig. 5.6; when $T_{on.SB} < T_{on.SL}$, the system operates as Fig. 5.7 and Fig. 5.8, where $T_{on.SB}$ and $T_{on.SL}$ denote the on-time of S_B and S_L. Generally, the operations of both the Boost PFC stage and the AHB stage in the proposed star architecture are basically identical to those in the conventional two-stage architecture, i.e., power transfer is done through changing the switching node voltages of the two stages (i.e., v_{sw1} and v_{sw2}) to switch between 0 and v_b independently to charge and discharge the energy storage elements to move energy from AC to DC end. For example, the boost inductor L is charged by the rectified AC source when S_B is on, and the transformer is charged by the buffer capacitor C_b when S_H and S_A are on. For this reason, the detailed circuit operation for each state is not exhausted. Interested readers are referred to [91] and [75] regarding the operation of boost and AHB converters.

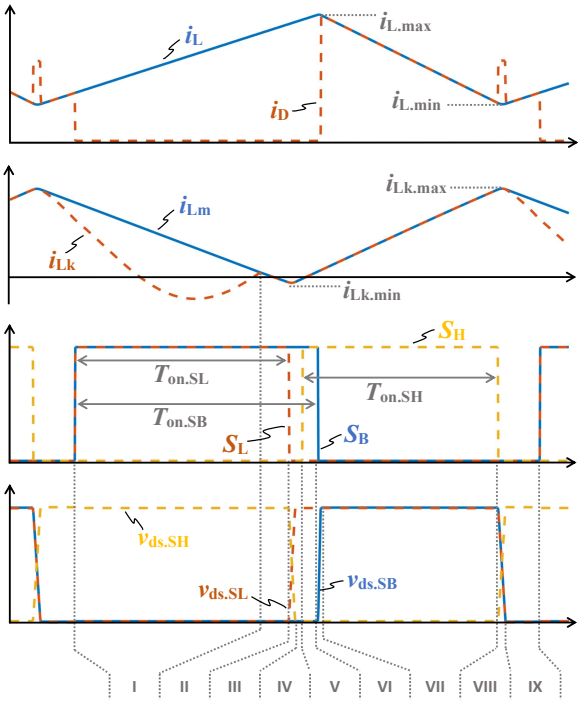


FIGURE 5.6: Operating waveforms when $T_{on.SB} \geq T_{on.SL}$. S_A is always on.

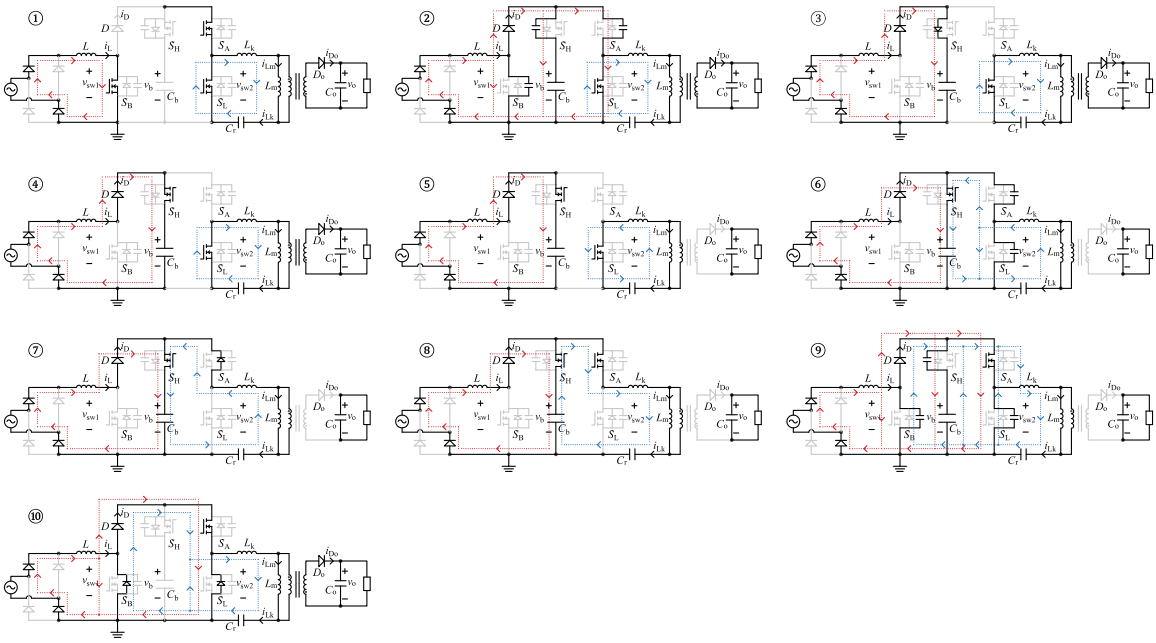


FIGURE 5.7: Operating states of the star architecture when the second stage is the asymmetrical half-bridge flyback and $T_{on.SB} < T_{on.SL}$. The current flows of i_L and i_{Lk} are highlighted in red and blue, respectively.

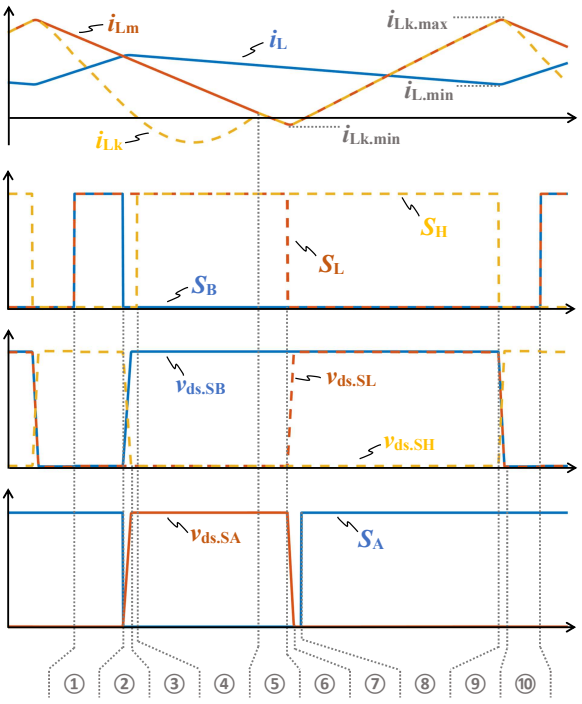


FIGURE 5.8: Operating waveforms when $T_{on.SB} < T_{on.SL}$. S_A is turned off when S_B is turned off, and S_A is turned on after S_L is turned off.

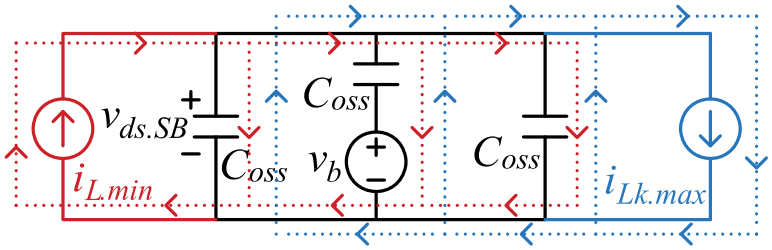


FIGURE 5.9: Equivalent circuit of the resonant process in State VIII and State ⑨. C_{oss} is the output capacitance of S_B, S_L, and S_A. The red and blue paths represent the current flows of i_L and i_{Lk}, respectively. The net current between i_L and i_{Lk} discharges the output capacitances of S_B and S_L to achieve ZVS under CCM.

The only difference in terms of operation between the proposed system and the conventional two-stage system based on a boost PFC stage and an AHB stage is an extra resonant process (State VIII for $T_{on.SB} \geq T_{on.SL}$ case, and State ⑨ for $T_{on.SB} < T_{on.SL}$ case) to assist soft-switching of S_B and S_L. S_A are controlled to integrate the second stage's transformer current into the boost PFC stage to enable the above resonant process.

To realize the above-mentioned operations, the switching logic needs a slight variation from the conventional two-stage architecture. In the conventional two-stage architecture, the control of i_L can be solely achieved by S_B and that of the output voltage v_o by the on duration of S_H. In the star architecture, however, the control of i_L are achieved by switching S_A and S_B collectively, and the control of v_o by the overlapping on duration of S_A and S_H. For example, L can be charged when S_B is turned on, but can only be discharged when both S_A and S_B are turned off in the $T_{on.SB} < T_{on.SL}$ case. Otherwise, if S_B is turned off and S_A remains on, i_L will be continuously charged by the rectified AC source through D, S_A, and S_L, losing the regulation capability of i_L. S_A can be constantly on in the $T_{on.SB} \geq T_{on.SL}$ case because solely turning off S_B can control i_L in this case. While there are some flexibility with the switching logic realization that can result in the same operating waveforms, here it is decided to operate S_A only when $T_{on.SB} < T_{on.SL}$ while keeping it constantly on when $T_{on.SB} \geq T_{on.SL}$ to enable the ZVS of S_B, simplify the controller implementation, and reduce the associated losses.

5.2.2 ZVS Realizations

As mentioned, the ZVS realization of S_B with $i_L > 0$ is attributed to a new resonant state (i.e., State VIII in Fig. 5.5 and State ⑨ in Fig. 5.7, both states have identical equivalent circuits) after S_H's turning off. In the new resonance state, i_L starts to charge the output capacitances of S_B and S_L while discharging the output capacitance of S_H. Meanwhile, i_{Lk} discharges the output capacitances of S_B and S_L and charges the output capacitance of S_H. The equivalent circuit during the resonance is shown in Fig. 5.9. Here, i_L and i_{Lk} are modelled as two constant current sources whose amplitudes are $i_{L.min}$ and $i_{Lk.max}$ as defined in Fig. 5.6 and Fig. 5.8. $i_{L.min}$ refers to the turn-on current of the boost front end. $i_{Lk.max}$ is the turn-off current of the isolated stage. During the resonance, the drain-source voltages of S_B and S_L are equal and can be calculated as

$$v_{ds.SB} = v_{ds.SL} = v_b - \int \frac{i_{Lk.max} - i_{L.min}}{3C_{oss}}\, dt \tag{5.1}$$

where C_{oss} is the output capacitance of S_A, S_B, and S_L, and $v_{ds.SB}$ and $v_{ds.SL}$ are the drain-source voltages of S_B and S_L, respectively. (5.1) shows that, in an ideal case, ZVS of S_B can be achieved as long as $i_{Lk.max} > i_{L.min}$. Practically, there are losses during the resonance process, and the resonant period may not be too long to approximate i_L and i_{Lk} as ideal current sources. Therefore, $i_{Lk.max} > i_{L.min}$ should be held with sufficient margin to ensure full-range ZVS of S_B. In universal-input applications, the minimal mismatch between $i_{Lk.max}$ and $i_{L.min}$, i.e., the most stringent condition for ZVS of S_B, is under the peak AC voltage of the low-line condition because $i_{L.min}$ is maximum in this condition while $i_{Lk.max}$ doesn't change with the AC inputs. The optimal design, i.e., the design with a minimal current ripple on L, can be found by reducing L until the ZVS of S_B and S_L can be marginally achieved in the most stringent condition. Another observation from (5.1) is that higher $i_{Lk.max}$ allows higher $i_{L.min}$ given the same ZVS margin. In other words, the higher the turn-off current of the isolated stage, the lower the current ripple of the boost inductor, bringing in a new opportunity to reduce the current ripple of L by leveraging the existing isolated stage with a relatively high turn-off current such as flyback converter and dual-active-bridge converter.

The resonant process ends when the body diodes of S_B and S_L conduct, and both S_B and S_L are ready for ZVS turn-on. Although the theoretical analysis shown in Fig. 5.5 and Fig. 5.7 assumes S_B and S_L are turned on simultaneously, it is recommended to turn on S_B slightly earlier than S_L by adjusting the dead-time in actual implementations. Otherwise, the turn-on of S_L may short the path of i_{Lk}, and there is no current to maintain the body diode conduction of S_B, leading to increased $v_{ds.SB}$ and loss of ZVS.

It is worth mentioning that the new resonance state also enables power transfer utilizing the output capacitance of S_B, which is not possible with the existing soft-switching boost converters. In star architecture, the energy stored within the output capacitance of S_B is charged by i_L in State VI or State ②, and is eventually discharged to the load rather than flowing back to L and the AC source as in the case of QSW operation, enabling lower circulating energy than QSW operation.

5.3 Comparison Between Star Architecture and Two-stage Architecture

5.3.1 Comparison of Power Loss

While including the additional switch S_A can reduce the switching loss of S_B and conduction loss of L by realizing ZVS and CCM operations thanks to the extra operating freedom provided by S_A, S_A itself, however, has additional conduction losses. Therefore, it is necessary to analyze whether the star architecture can eventually achieve higher overall efficiency than the conventional two-stage architecture. In this section, the following three case studies are conducted to compare the power loss performance:

- Case I: CCM boost and star architecture.
- Case II: CCM boost and two-stage architecture.
- Case III: QSW boost and two-stage architecture.

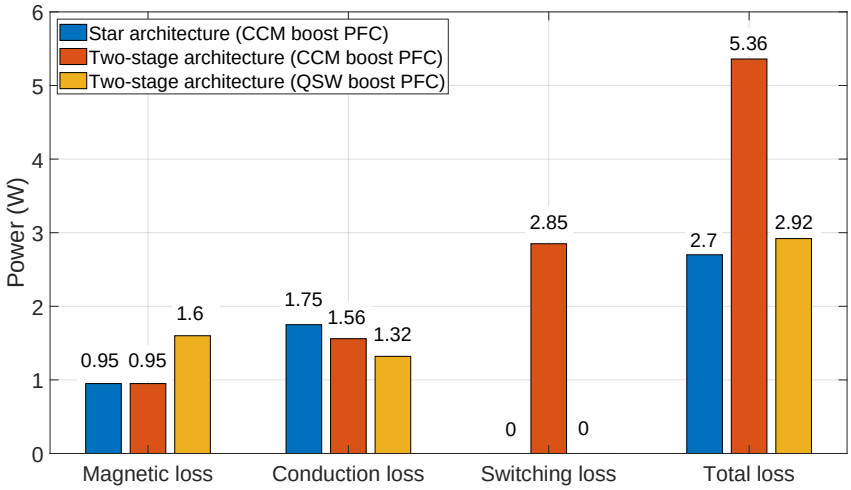


FIGURE 5.10: Loss comparison between star architecture and two-stage architecture under different modes of operations (110 V AC). The magnetic loss includes conduction loss and core loss of the boost inductor.

All three case studies are on a 240-W (48 V / 5 A) adapter design. 240 W is selected because it is the maximum output power in the latest USB PD 3.1 fast charging standard. For fair comparisons, circuit parameters and components for all three cases are identical except for

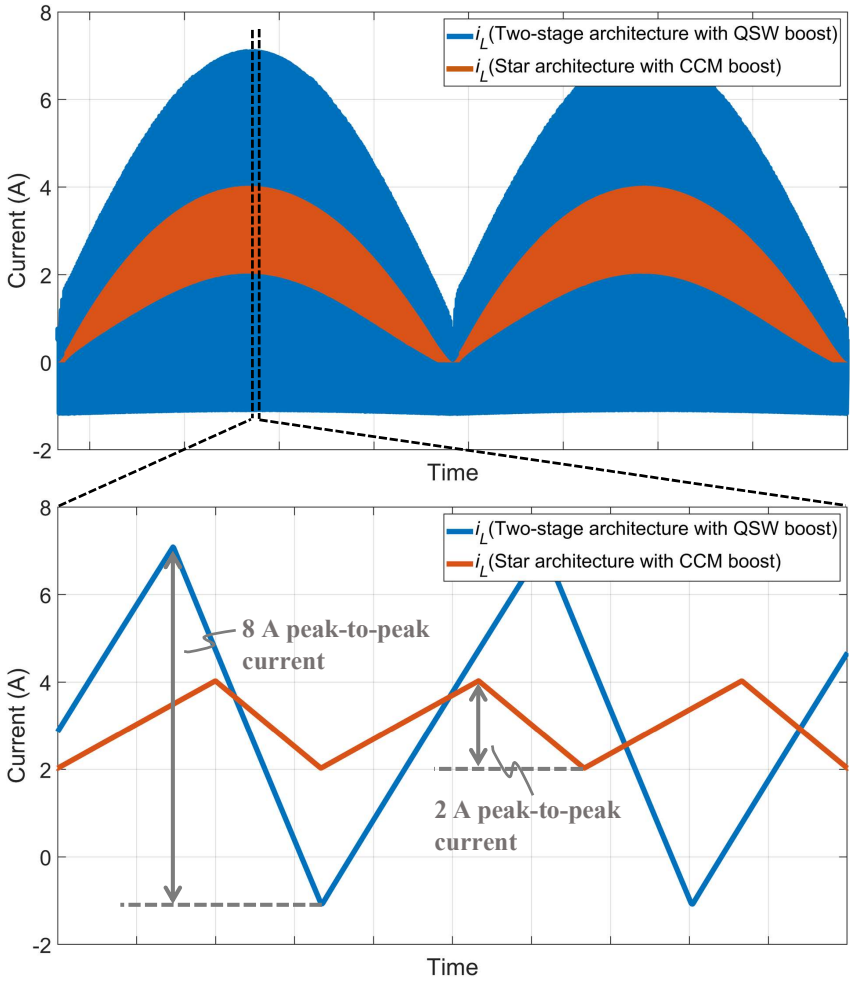


FIGURE 5.11: Comparison of inductor current ripple between CCM and QSW operations (110 V AC). The star architecture allows four times smaller current ripple than the two-stage architecture under QSW operations when the magnetic energy storage of both cases are the same.

the switching frequencies and the inductance used in the boost PFC stage. Particularly, the switching frequency of the CCM boost converter in Case I and II is selected as 300 kHz to keep up with the trend toward higher switching frequency and higher power density, while that of the QSW boost converter is from 118 to 242 kHz to maintain the same magnetic energy storage requirement (i.e., $0.5Li^2_{L.max}$) as the CCM boost converter. The boost inductors used in all three cases have the same core geometry, the number of turns, and wire gauge. Since S_B should handle the high current stress in low-line conditions to cover universal input, a device with lower on-state resistance and higher output capacitance is selected for S_B. Here, a GaN switch GS-065-030-2-L is used for S_B. On the other hand, the current stresses for S_H,

S_L, and S_A are relatively low, so devices with slightly higher on-state resistance and lower output capacitance are used for them to reduce the circulating energy. Here, GS-065-011-2-L is used for S_H, S_L, and S_A. The conduction loss and switching loss of the active switches are calculated using (5.2) and (5.3) below

$$P_{cond} = I_{rms}^2 R_{ds.on} \tag{5.2}$$

$$P_{switch} = \frac{C_{oss} v_b^2 f_{sw} + v_b I_{on} T_f f_{sw}}{2}, \tag{5.3}$$

where I_{rms} is the RMS current flowing through the switch in a line period, $R_{ds.on}$ is the on-state resistance of the switch, I_{on} is the average turn-on current of the switch over a line period, T_f is the falling time of the drain-source voltage during the turn-on process, and f_{sw} is the switching frequency. The core loss of magnetics is estimated using the Steinmetz equation, and the conduction loss of magnetics is approximated by the DC conduction loss. The transformer loss is excluded from the magnetic loss analysis because both architectures have the same loss on their transformers. Similarly, the power losses on the diode bridge, secondary side rectifier, and voltage sensors are also excluded because they are identical in all cases. The boost inductor used in the comparison follows the same design as specified in Table. 5.3 except that its air gap is reduced in the case of QSW boost converter until the magnetic energy storage of QSW boost converter becomes the same as that of the CCM cases.

The results of the comparison are shown in Fig. 5.10. Compared with Case II, the star architecture shows slightly higher conduction loss due to the additional loss on S_A, but has much lower switching loss thanks to the ZVS of S_B, eventually leading to higher overall efficiency than that of Case II. Compared with Case III, the star architecture also shows slightly higher conduction loss because D is replaced with an active switch in the QSW-based two-stage architecture. Nevertheless, the star architecture still has higher overall efficiency than that of Case III because of the substantially reduced inductor current ripple (by 75 % in the case study) and thus the corresponding magnetic loss (by around 40 %) thanks to the CCM operation as illustrated in Fig. 5.11. It should also be noted that the star architecture has a lower implementation cost than Case III, as the expensive micro-controller and high-speed zero-crossing detection mandated in Case III are not required in the star architecture.

The above analysis demonstrates that the star architecture can achieve higher overall efficiency than the two-stage architecture, especially in high-frequency designs. Also, it is concluded that ZVS is still necessary for higher efficiency even if better devices, such as GaN devices, are available.

5.3.2 Comparison of Current Stress on C_b

In addition to magnetics, C_b also occupies a significant amount of the system's size. C_b's size mainly depends on (i) the energy storage requirements for buffering the double-line frequency ripple power (i.e., $C_b = P_o/(2\pi f_l V_b \triangle V_b)$, where P_o is the output power, f_l is the line frequency, V_b is the average buffer voltage, and $\triangle V_b$ is the low-frequency voltage ripple) and (ii) the amount of ripple current passing through C_b. Regarding the energy storage requirement aspect, the star architecture and the conventional two-stage architecture will lead to identical C_b provided that f_l, V_b and $\triangle V_b$ are the same. Regarding the ripple current aspect, the star architecture has a lower or at least equal current stress on C_b compared with the two-stage architecture. A comparative study is conducted below to evaluate the ripple current of C_b in both architectures. In the conventional two-stage architecture, the PFC stage and the second DC–DC stage can be operated independently. The ripple current in C_b is thus a function of the relative phase shift between the two stages (i.e., the ON-instant of S_B and S_L). With the proposed star architecture, the operation of the two stages is coupled, resulting in the in-phase operation of the two stages (or synchronized turn-on of S_B and S_L). Thus, the ripple current of C_b with the star architecture is a special case of the conventional two-stage one. The RMS current of C_b under different phase shifts between S_B and S_L are measured in Fig. 5.12. It is found that C_b has the lowest current stress when the phase shift is zero, which is inherently achieved with the star architecture. The fundamental reason for the reduced current stress is that i_L and i_{Lk} cancel each other on C_b better when the two stages are perfectly synchronized. Ensuring zero phase shift between S_B and S_L can lead to up to 45 % reduction of RMS current in C_b, as shown in Fig. 5.13. The star architecture can thus achieve lower or at least equal RMS current into C_b compared with the two-stage architecture.

In summary, C_b's energy storage requirement and current stress are the same or smaller with the star architectures, leading to the same or smaller C_b's size.

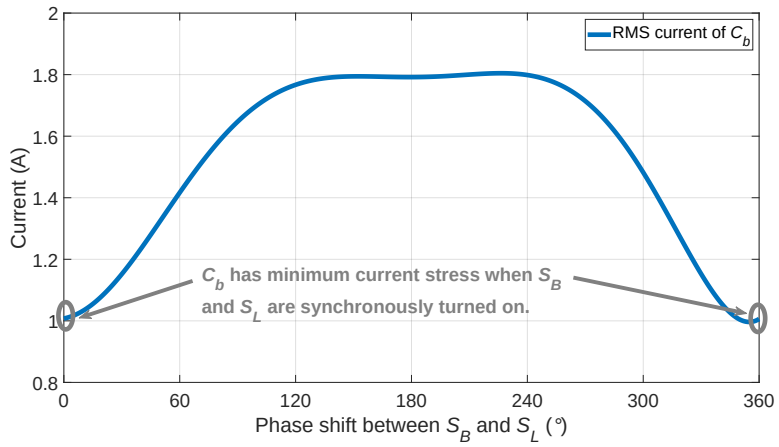


FIGURE 5.12: RMS current of C_b under different phase shift between S_B and S_L in the two-stage architecture (115 V, 240 W). The circuit parameters used to plot the figure are the same as the hardware prototype. The two stages have the same switching frequency. It is found that synchronously turning on S_B and S_L leads to the lowest RMS current in C_b, which is an inherent feature with the star architecture.

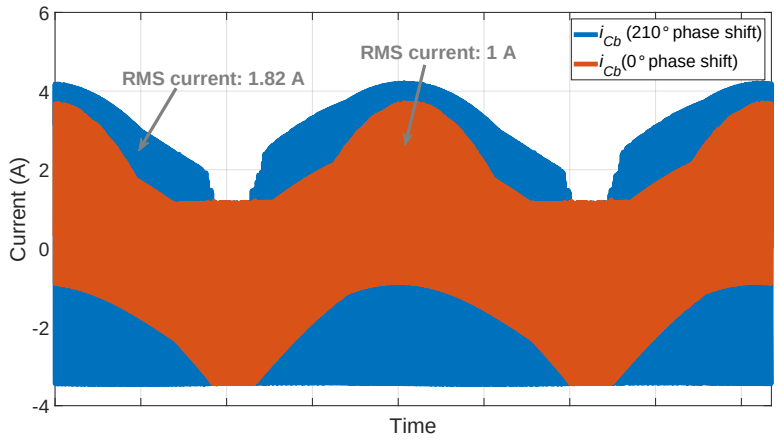


FIGURE 5.13: Comparsion of current flows in C_b, i_{Cb}, under different phase shift between S_B and S_L (115 V, 240 W). The star architecture has $0°$ phase shift between S_B and S_L by turning on S_B and S_L synchronously, enabling up to 45 % reductions of RMS current in C_b.

5.4 Control Circuit

An exemplary implementation of the control circuits for the star architecture is shown in Fig. 5.14. The added components to control S_A are highlighted in red. It is shown that the star architecture only requires two additional components (i.e., a delay block for the dead-time and a SR latch for the control logic) than the two-stage architecture, making the implementation very simple and low-cost. The added control circuit synchronously turns S_A off when S_B turns off, and turns S_A on when S_L is off, which executes the operations when $T_{on.SB} < T_{on.SL}$. The SR latch is configured to be set-prioritized so that S_A remains on when S_L is already off, effectively executing the operations when $T_{on.SB} \geq T_{on.SL}$. The other parts of the control circuit follow a standard control design for the two-stage architecture. Three controllers are used to perform input current shaping, buffer voltage regulation, and output voltage regulation. The output voltage v_o is sensed and compared with the reference $v_{o.ref}$ to determine the on-time of S_H, i.e, the duty cycle of the isolated stage, to achieve output voltage regulation. The buffer's voltage v_b is also compared with its reference signal $v_{b.ref}$ to adjust the amplitude of input current and the amplitude is multiplied with a rectified sinusoidal signal in phase with the AC input to generate the reference signal i_{ref} for the input current controller. The input current controller compares the errors between i_{ref} and filtered i_L and adjusts the on-time of S_B, i.e, the duty cycle of the boost stage, to shape the input current and achieve PFC. A clock signal CLK resets S_L periodically to determine the switching frequency.

It is worth mentioning that the control circuit is only based on simple analog circuits and basic logic gates. A key difference between the star architecture and existing ZVS boost converters is that the energy for ZVS of S_B is from the isolated stage rather than i_L. Therefore, precisely regulating i_L to ensure ZVS and low circulating energy is not needed in the star architecture, so the expensive high-speed sensors and complicated digital calculations in many existing QSW-based PFC solutions are not required.

The feasibility of the proposed control circuit is verified by a simulation study under a step change of load from 10 % to 100 %. The proposed control circuit allows i_{in}, v_b, and v_o to reach a steady state quickly with low undershoots after the step change of load, as shown in

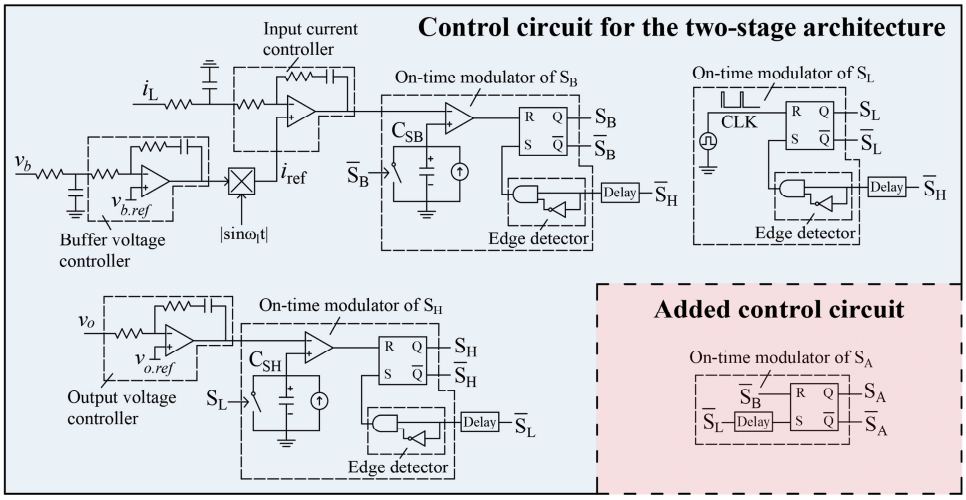


FIGURE 5.14: Control circuit. The control circuit in the two-stage architecture is blue-shaded, and the added control circuit is red-shaded. The star architecture only adds a delay block and an SR latch compared with the two-stage architecture. All of the SR latches are configured to be set-prioritized.

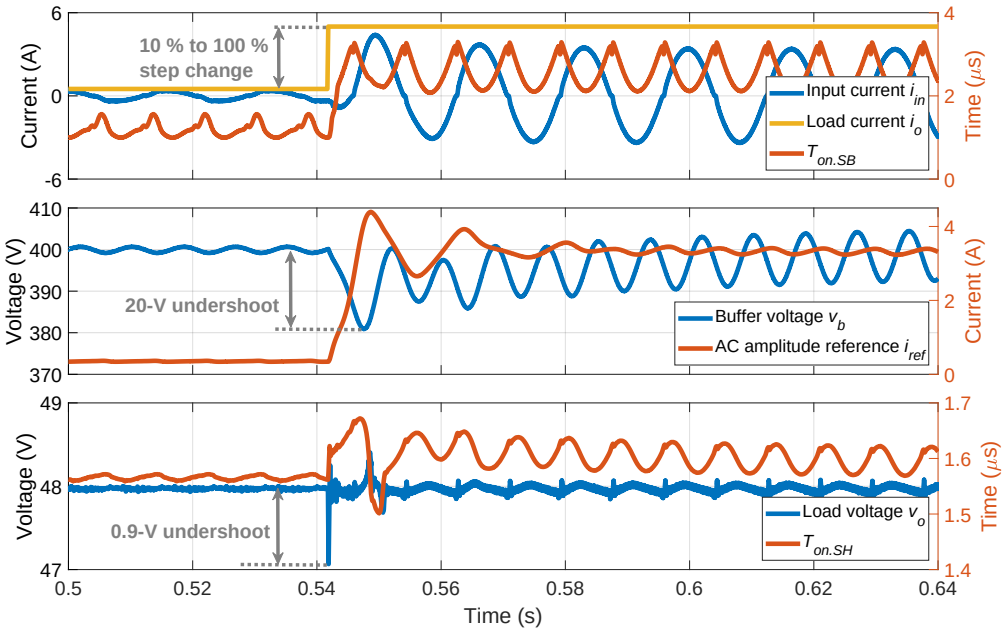


FIGURE 5.15: Transient waveforms under a step change of load from 10 % to 100 %. $T_{on.SB}$, i_{ref}, and $T_{on.SH}$ are actively controlled and increased during the step change to achieve sinusoidal i_{in}, balanced v_b, and constant v_o. The proposed control circuit allows i_{in}, v_b, and v_o to reach steady states with small undershoots after the transient event.

Fig. 5.15. During the transient event, $T_{on.SB}$, i_{ref}, and $T_{on.SH}$ are increased to regulate i_{in}, v_b, and v_o, which testifies to the operating principle. At the steady state, $T_{on.SB}$ is actively

varied according to v_{in} to achieve sinusoidal i_{in}, and $T_{on.SH}$ contains a double-line frequency component to compensate for the low-frequency ripple in v_b such that v_o remains constant.

5.5 Design

The main difference in the design of the star architecture is that the design should ensure the ZVS of S_B in the worst condition while keeping the current ripple on i_L as low as possible to optimally utilize the CCM capability. In the previous analysis, (5.1) is derived in an ideal case to help the readers quickly understand the key idea and illustrate the capability of ZVS and CCM operations leveraging i_{Lk}. More accurate modelling is conducted in this section to assist the actual design.

5.5.1 Design of The Isolated Stage

The design process starts from the isolated stage. The main design target of the isolated stage is to achieve i). full-range ZVS of S_A and S_H and ii.) practical voltage and current stresses on both sides of the transformer. The winding turns ratio n is designed first. n is designed such that the AHB flyback works at around 0.5 duty cycle to balance the current stress on the primary and secondary sides while having sufficient leeway to perform voltage regulation. n can be calculated as

$$n = \frac{Dv_b}{v_o}, \tag{5.4}$$

where D is the duty cycle selected for the isolated stage. After determining n, the switching frequency f_{sw} should be designed. While there is negligible switching loss with the star architecture, the main factor limiting f_{sw} is the trade-off between the size and power losses of the transformer. Fig. 5.16 compares the core loss and the size of the transformer under different switching frequencies. As with many other high-frequency converters, such as totem-pole PFC converters, the switching frequency can be further increased with the star architecture to use smaller magnetics (e.g., RM 8 core can be used if the switching frequency is pushed to 640kHz), but, in general, this will increase the core losses, as shown in Fig. 5.16. Therefore, the determination of the optimal switching frequency of the system requires

further engineering efforts. In this work, f_{sw} is selected at 300 kHz, which is around 5 times higher than the conventional design of a CCM boost converter, to prove the concept of high-frequency and efficient operation of the first PFC stage and showcase the performance improvements with the proposed architecture.

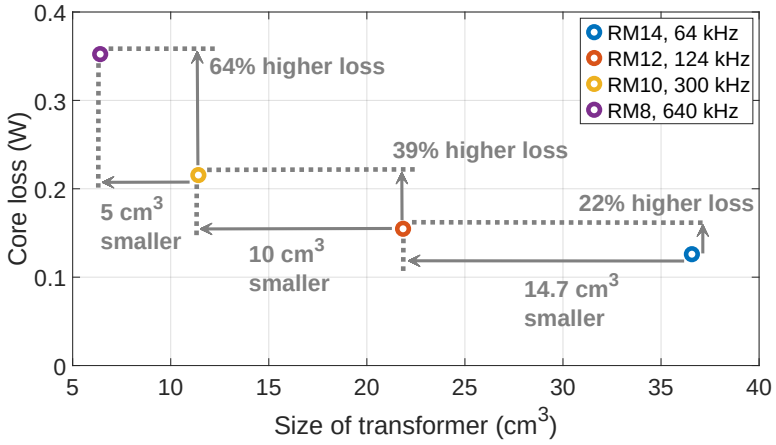


FIGURE 5.16: Trade-off between the size of transformer and core loss. All cases follow the same specifications as the hardware prototype in experimental verification and are designed to have the same flux density and current density. Higher switching frequency enables a smaller transformer at the expense of higher core loss. The loss penalty increases while the benefit of size reduction becomes marginal with the increase of switching frequency.

Then, L_m is designed to have sufficient negative magnetizing current to achieve ZVS of S_A and S_H. The maximum L_m to marginally achieve ZVS can be found by solving

$$\begin{aligned} min(v_b - Dv_b + Dv_b cos(\frac{t}{\sqrt{2L_m C_{oss}}}t) \\ - \sqrt{\frac{L_m}{2C_{oss}}} i_{Lk.min} sin(\frac{t}{\sqrt{2L_m C_{oss}}})) = 0, \end{aligned} \tag{5.5}$$

where $min(\cdot)$ is the minimum operator and $i_{Lk.min}$ is the minimum i_{Lk} is a switching cycle. $i_{Lk.min}$ is derived to be

$$i_{Lk.min} = \frac{P_o}{nv_o} - \frac{(v_b - nv_o)nv_o}{2L_m v_b f_{sw}}, \tag{5.6}$$

where P_o is the output power. L_m should be designed smaller than its maximum value calculated from (5.5) to ensure full-range ZVS of the second stage. The leakage inductance L_k should be designed as small as possible to reduce the voltage stress on the secondary diode or synchronous rectifier (SR).

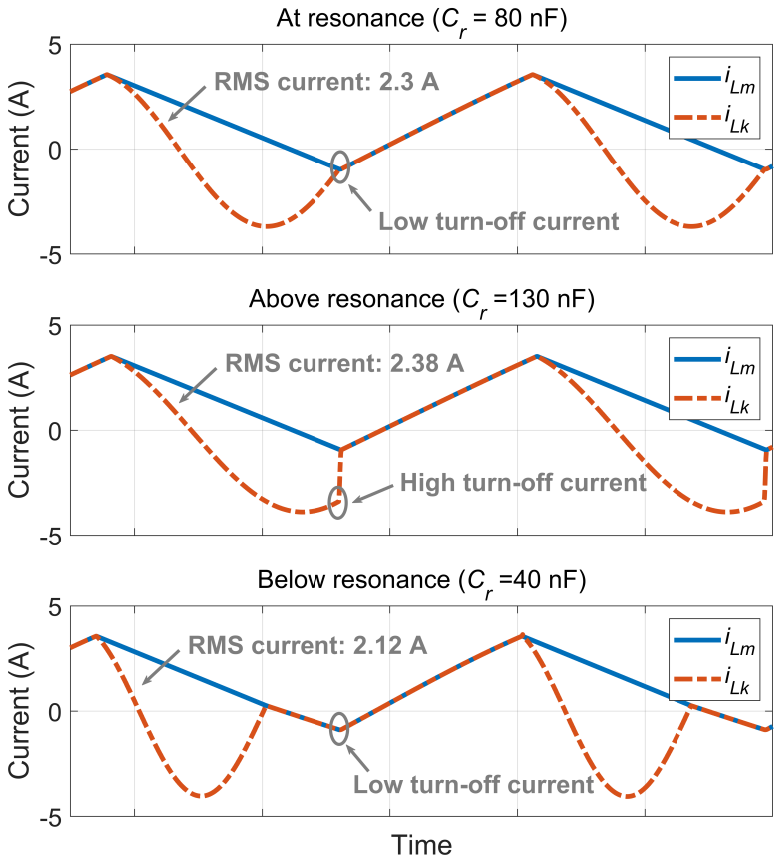


FIGURE 5.17: Waveforms of i_{Lk} and i_{Lm} under different C_r (240-W output). The parameters used to plot the figure are the same as the hardware prototype in experimental verification. Varying C_r changes the resonant frequency of the AHB flyback converter, leading to three operating modes (i.e., at, above, and below resonance). Reducing C_r helps to achieve a lower turn-off current of S_L and a lower RMS current on the primary side of the transformer.

L_k may be measured after the transformer is built. After L_k is determined, C_r is designed to resonate with L_k at the switching frequency so that the secondary-side diode can realize zero-current turn-off and S_L can be turned off with low current stress. Reducing C_r shifts the operations from "above resonance" to "below resonance", leading to a lower turn-off loss on S_L and lower conduction loss on the primary side, as shown in Fig. 5.17. On the secondary side of the transformer, reducing C_r reduces the reversed recovery loss of D_o at the expense of higher conduction loss, as shown in Fig. 5.18. Hence, it is desirable to tune C_r such that the converter operates near the "at resonance" region to achieve low switching and conduction losses.

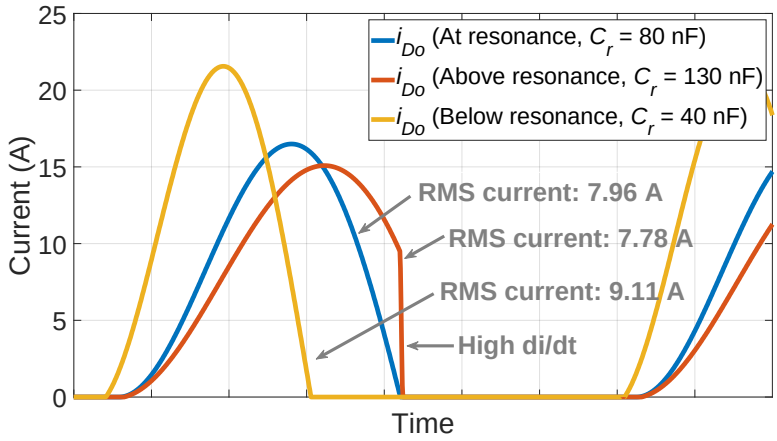


FIGURE 5.18: Waveforms of i_{Do} under different C_r (240-W output). The parameters used to plot the figure are the same as the hardware prototype in the experimental verification. All waveforms have the same average value at 5 A. Operating above resonance leads to lower current stress on the secondary side of the transformer but results in higher reversed recovery loss due to higher di/dt of i_{Do}.

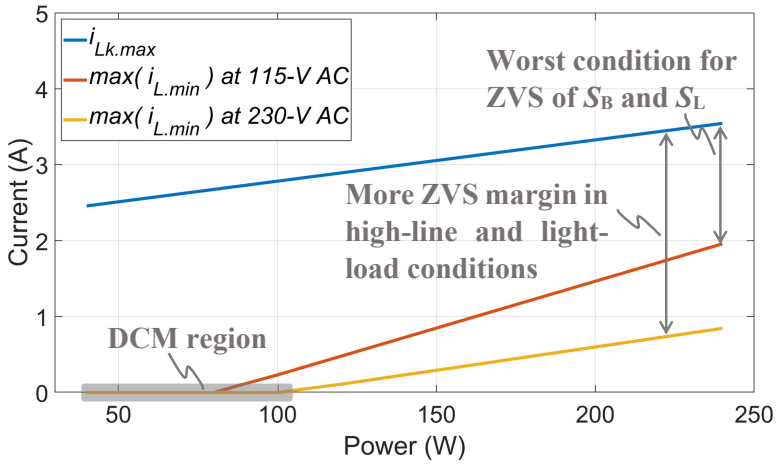


FIGURE 5.19: $i_{Lk.max}$ and $max(i_{L.min})$ under different AC input and load power. The circuit parameters used to plot the figure are the same as the hardware prototype in the experimental verification. The worst condition for ZVS, which is when the mismatch between $i_{Lk.max}$ and $max(i_{L.min})$ is minimal, is highlighted by the double arrow.

5.5.2 Design of The PFC Stage

The main design target of the PFC stage is to achieve i). full-range ZVS of S_L and S_B and ii.) minimized inductor current ripple.

After the design of the isolated stage, its turn-off current $i_{Lk.max}$ is determined and can be calculated as

$$i_{Lk.max} = \frac{P_o}{nv_o} - \frac{(v_b - nv_o)nv_o}{2L_m v_b f_{sw}} + \frac{D(v_b - Dv_b)}{f_{sw}L_m}. \tag{5.7}$$

$i_{Lk.max}$ determines how high $i_{L.min}$ can be and, hence, how low the current ripple of L can be. Lower current ripple indicates higher $i_{L.min}$ given the same average current of i_L. $i_{L.min}$ is calculated to be

$$i_{L.min} = \frac{|v_{ac}|^3 + 2f_{sw}Lp_{in}v_b - v_{ac}^2 v_b}{2f_{sw}L|v_{ac}|v_b}, \tag{5.8}$$

where p_{in} is the instantaneous input power and v_{ac} is the AC input voltage. The maximum L to ensure ZVS of S_B in the worst case can be determined by solving

$$max(i_{L.min}) = i_{Lk.max}, \tag{5.9}$$

where $max(\cdot)$ is the maximum operator. L should be selected slightly lower than its maximum value and further tuned based on hardware experiments for optimal performance. Fig. 5.19 shows $i_{Lk.max}$ and $max(i_{L.min})$ under different input voltage and power level. The most stringent condition for the ZVS of S_B and S_L is found to be at full-load and low-line conditions, and there will be more ZVS margin in high-line and light-load conditions.

5.6 Verification

A 300-kHz, 240-W (48 V / 5 A), and universal-input hardware prototype, as shown in Fig. 5.20, is built to verify the performance of the star architecture. The prototype has a power density of 55.6 W/in^3, and its bottom side is shown in Fig. 5.21. The specifications, circuit parameters, and components used are summarized in Table. 5.2 and Table. 5.3. The current stress and voltage stress of components are summarized in Table. 5.4 and Table. 5.5.

The experimental verification is to verify 1) the key functions required in the PFC applications, including universal-input PFC and output voltage regulation, 2) the operating principle of the star architecture, 3) the full-range ZVS capability of all switches, and 4) improvements over the two-stage architecture.

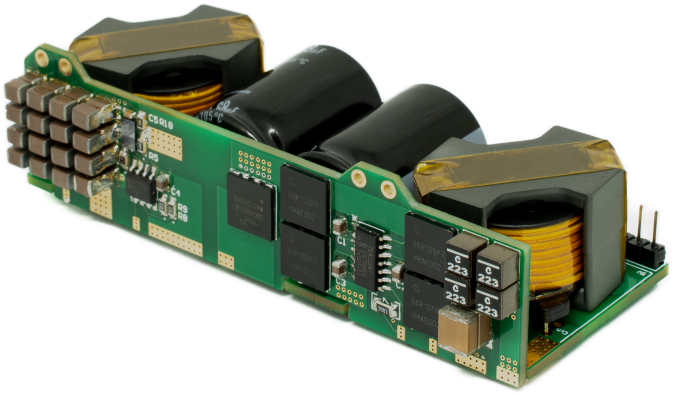


FIGURE 5.20: Hardware prototype. The size is 3.6 × 1.5 × 0.8 in^3 (length × width × height). The power density is 55.6 W/in^3.

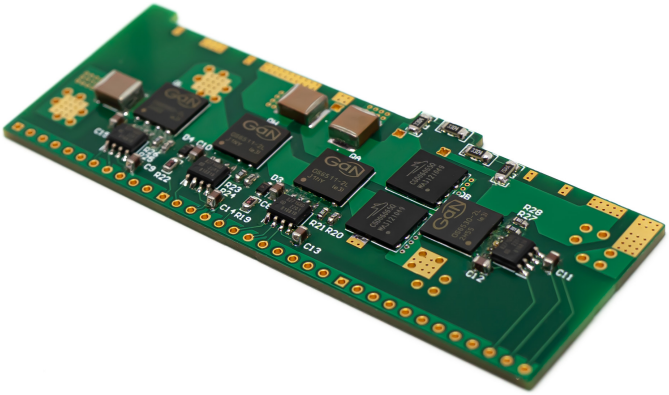


FIGURE 5.21: Bottom side of the prototype.

TABLE 5.2: Specifications of the prototype.

Specifications	Value
Input Voltage (v_{ac})	Universal
Output Power	240 W
Buffer Voltage (v_b)	400 V
Output Voltage (v_o)	48 V
f_{sw}	300 kHz

The experimental verification starts with the key functions of the star architecture. The star architecture can achieve high-quality sinusoidal input current in phase with the AC input and constant output voltage under both low-line and high-line conditions, as verified in Fig. 5.22 and Fig. 5.23. The operating waveforms at 20 % load condition are shown in Fig. 5.24,

TABLE 5.3: Bill of materials.

Components	Descriptions
EMI filter inductor	XGL4040-223MEC (22 μH) * 4
EMI filter capacitor	C2220X664KBRLCAUTO (630 V, 0.66 μF)
Bridge rectifier	IPL60R105P7AUMA1 (650 V, 105 mΩ) * 4
S_A, S_H	GS-065-011-2-L (650 V, 150 mΩ)
S_B, S_L	GS-065-030-2-L (650 V, 50 mΩ)
D	C6D06065Q (650 V, 6 A)
C_b	450TXW68MEFR18X25 (450 V, 68 μF) * 2
C_o	C3225X7R2A106K250AC (100 V, 10 μF) * 32
C_r	CKC21C823FWGACAUTO (650 V, 82 nF)
Synchronous rectifier	EPC2034 (200 V, 10 mΩ)
Boost inductor L	RM 10 (160 μH, N49)
Transformer	RM 10 (74-μH L_m, 2-μH L_k, n = 23:6, N49)

TABLE 5.4: Steady-state Current Stress of Components (115-V AC)

Components	Peak current (A)	RMS current (A)
S_B	4.3	2
S_A	3.7	1.35
S_H	4.3	1.05
S_L	3.7	1.59
D	4.3	1.38
C_b	4.3	1.05
C_o	13.3	6.71
Bridge rectifier	4.3	1.19
Synchronous rectifier	18.3	8.37
L	4.3	2.38
Primary side of transformer	3.7	2.14
Secondary side of transformer	18.3	8.37

TABLE 5.5: Steady-state Voltage Stress of Components

Components	Voltage stress (V)
S_B, S_A, S_H, S_L, D, and C_b	405
C_o	48
C_r	210
Bridge rectifier	340
Synchronous rectifier	150

demonstrating a high power factor and the regulated output voltage at light-load conditions. The zero-crossing distortion of i_{in} may be reduced by increasing the controller bandwidth or using feed-forward control [92].

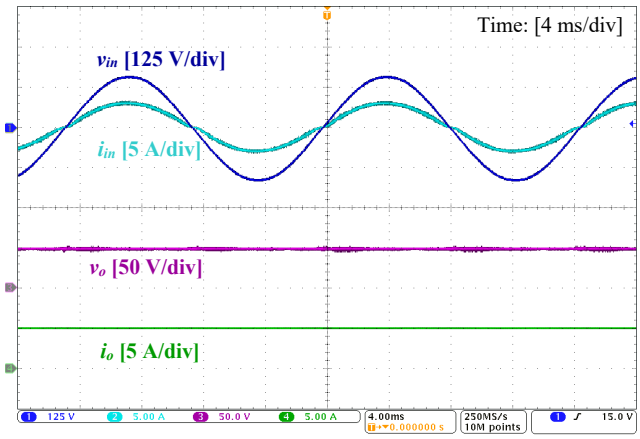


FIGURE 5.22: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 115-V input and 240-W output.

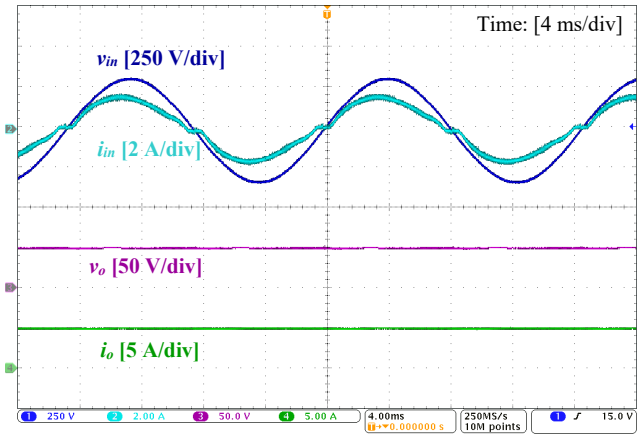


FIGURE 5.23: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 230-V input and 240-W output.

Then, the operating principle is verified by checking detailed switching waveforms. The detailed waveforms of i_L, S_B, S_L, and S_A when $T_{on.SB} > T_{on.SL}$ and when $T_{on.SB} < T_{on.SL}$ are recorded in Fig. 5.25 and Fig. 5.26, respectively. Fig. 5.25 verifies that the proposed control circuit functions properly as S_A is always on when $T_{on.SB} > T_{on.SL}$, and the charging and discharging of i_L can be effectively controlled by the on-off actions of S_B. Fig. 5.26 shows that S_A is synchronously turned off with S_B when $T_{on.SB} < T_{on.SL}$, which complies with the theoretical analysis. Fig. 5.27 shows that the S_H and S_L switch complementarily to charge and discharge the transformer, verifying the isolated stage in the star architecture works the same way as how it works independently. In particular, low circulating energy and ZCS turn-off of the SR are successfully achieved. Fig. 5.27 also shows that i_{Lk} increases

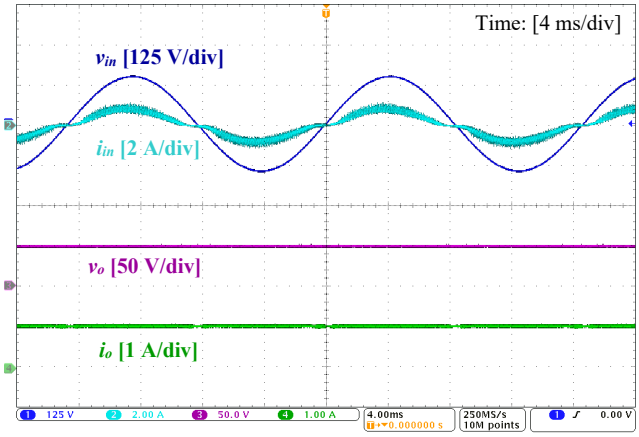


FIGURE 5.24: Operating waveforms of v_{in}, i_{in}, v_o, and i_o at 115-V input and 48-W output.

linearly at the full-load condition, verifying the transformer is not saturated at its worst operating condition. The CCM operations of i_L are verified under both low-line and high-line conditions, as shown in Fig. 5.28 and Fig. 5.29. It can be seen that CCM operations are achieved under both low-line and high-line conditions. Fig. 5.29 shows that the mismatch between $i_{L.min}$ and $i_{Lk.max}$ is larger under 230-V AC, so there is more ZVS margin for S_B under 230-V AC than 115-V AC, which coincides with the analysis carried out in Fig. 5.19. Fig. 5.28 and Fig. 5.29 also demonstrates that the average buffer voltage is well regulated at a constant 400 V across a wide range of AC input.

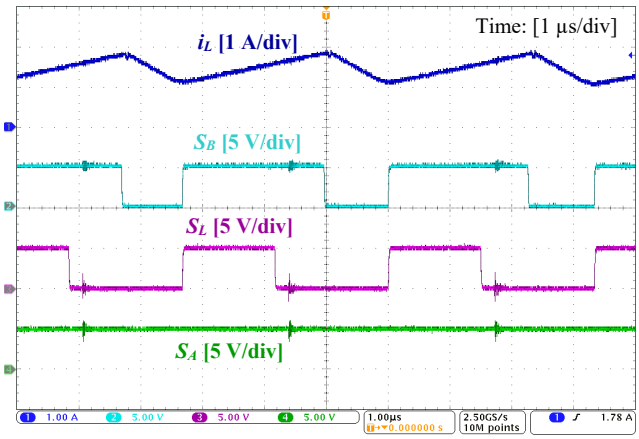


FIGURE 5.25: Operating waveforms of i_L, S_B, S_L, and S_A when $T_{on.SB} > T_{on.SL}$. S_A is always on in a switching period as designed. The switching frequency is constant at 300 kHz, as expected.

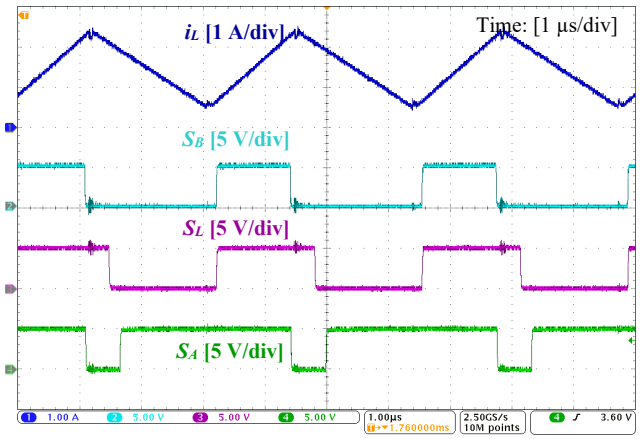


FIGURE 5.26: Operating waveforms of i_L, S_B, S_L, and S_A when $T_{on.SB} < T_{on.SL}$. Both S_A and S_B switch off to reduce i_L. The switching frequency is constant at 300 kHz, as expected.

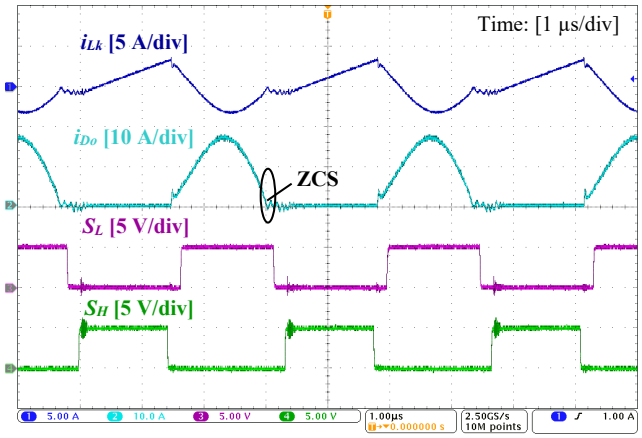


FIGURE 5.27: Operating waveforms of i_{Lk}, i_{Do}, S_L, and S_H at 240-W output. The circuit is finely tuned to achieve near zero circulating energy.

The ZVS waveforms of all switches are measured under their most stringent conditions to verify the full-range ZVS capability of the star architecture. For S_B and S_L, their most stringent ZVS condition is at the peak of AC input under low-line and full-load conditions, under which the mismatch between $i_{Lk.max}$ and $i_{L.min}$ is minimal as shown in Fig. 5.28. Fig. 5.30 proves that S_B and S_L can achieve ZVS under their most stringent condition, verifying that they can achieve full-range ZVS. During the resonance process, $v_{ds.SB}$ and $v_{ds.SL}$ are equal and slowly drop to zero even when i_L is still in CCM operation. The worst ZVS condition of S_A is when $i_{Lk.min}$ is closest to zero, which happens under the full-load condition. Fig. 5.31 verifies that S_A can achieve ZVS under the worst condition. The worst

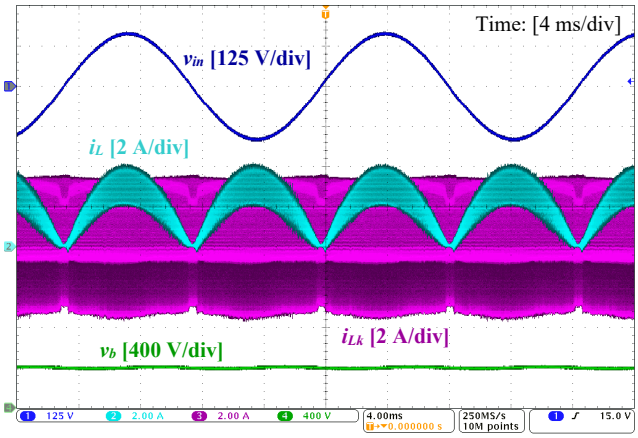


FIGURE 5.28: Operating waveforms of v_{in}, i_L, i_{Lk}, and v_b at 115-V input and 240-W output. $i_{L.min}$ is lower than $i_{Lk.pk}$ across the whole line period, enabling ZVS of S_L and S_B.

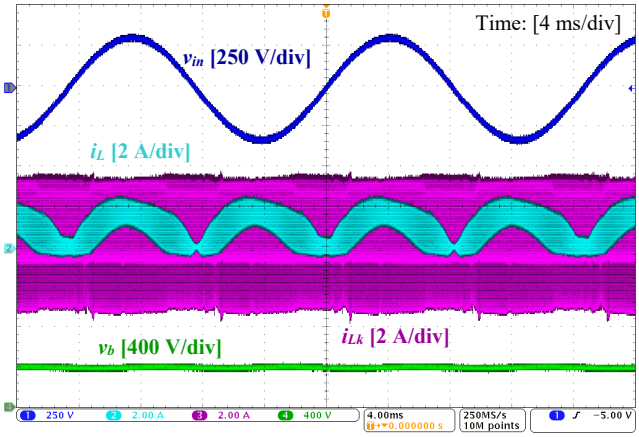


FIGURE 5.29: Operating waveforms of v_{in}, i_L, i_{Lk}, and v_b at 230-V input and 240-W output. There is more ZVS margin for S_L and S_B compared with that of 115-V input because the difference between $i_{L.min}$ and $i_{L.pk}$ is larger.

ZVS condition of S_H is when both $i_{Lk.min}$ and $i_{L.max}$ are closest to zero, which happens near the zero-crossing of AC input under the full-load condition. Fig. 5.32 demonstrates that S_H can also achieve ZVS under its worst condition.

The above verification confirms that the star architecture can perform the key functions required by a typical PFC rectifier and can achieve CCM operation and full-range ZVS of all switches simultaneously. Then, the prototype is re-configured into the two-stage architecture to make a fair comparison between the two architectures and verify the star architecture's performance improvements. The reconfiguration is done by directly soldering the drain and

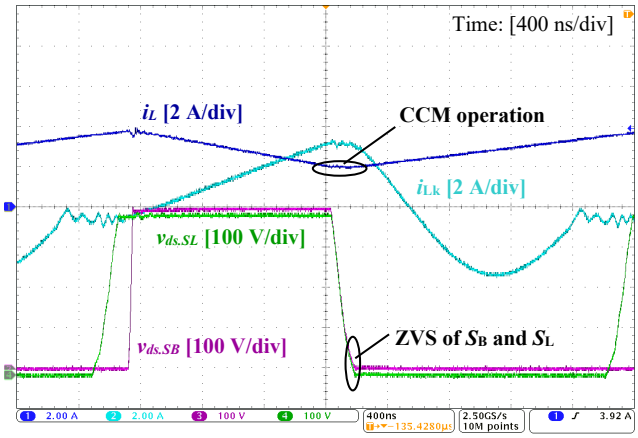


FIGURE 5.30: ZVS waveforms of S_L and S_B at the peak of 115-V input and 240-W output. This is the most stringent condition for the ZVS realizations of S_L and S_B as the mismatch between $i_{L.min}$ and $i_{Lk.pk}$ is minimal. ZVS of S_L and S_B as well as CCM operation of i_L are achieved.

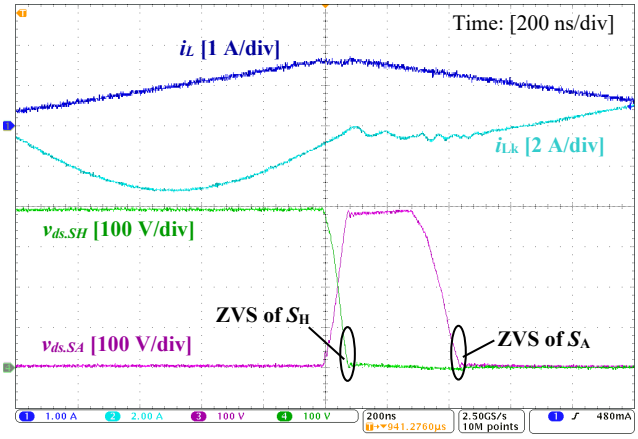


FIGURE 5.31: ZVS waveforms of S_A and S_H at 240-W output. This is the most stringent condition for the ZVS realization of S_A as $i_{Lk.min}$ is closest to zero.

source of S_H together and uses the logic signal of S_H to drive S_A. Other components in the prototype, including the inductor and transformer, remain the same. Fig. 5.33 shows the waveforms of losing ZVS in the two-stage architecture. In the two-stage architecture, $v_{ds.SL}$ and $v_{ds.SH}$ are no longer equal during their turn-on processes, and S_B is hard switched, causing a sharp falling edge of $v_{ds.SB}$ after the logic signal is turned high. Fig. 5.34 measures the efficiency of the two architectures at different AC voltage levels. The star architecture can maintain an efficiency greater than 96 % and achieve more than 2 % efficiency improvements than the two-stage architecture thanks to the ZVS capability, which testifies to the previous loss

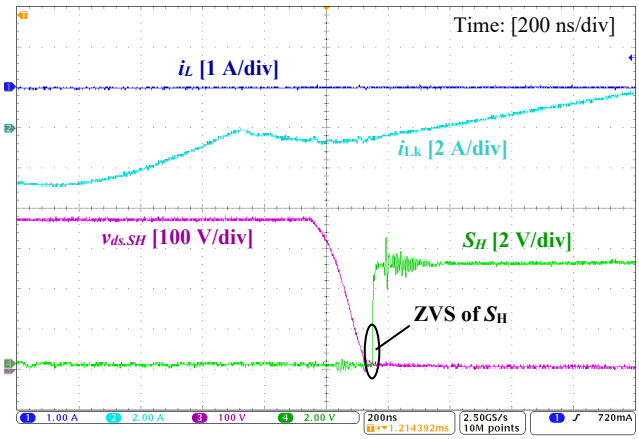


FIGURE 5.32: ZVS waveforms of S_H near the zero-crossing of 115-V input and at 240-W output. This is the most stringent condition for the ZVS realization of S_H as both $i_{L.max}$ and $i_{Lk.min}$ are closest to zero.

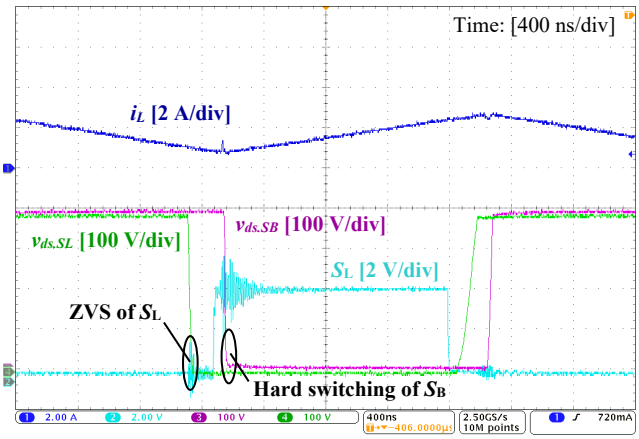


FIGURE 5.33: Loss of ZVS in the conventional two-stage architecture under CCM operation. S_L can still realize ZVS but S_B cannot. S_B (not shown in the figure) is turned on simultaneously with S_L to reduce the current stress of C_b.

analysis. The efficiency is also measured at different power levels in Fig. 5.35, which shows that the star architecture can have more efficiency improvements in light-load conditions because the switching loss, which is saved in the star architecture, is more dominant in light-load conditions. The prototype measures 97.1 % peak efficiency in full-load conditions and under 230-V input. The efficiency drops faster at light-load conditions due to the increased circulating power and AC losses in the AHB flyback stage. The above results conclude that the star architecture has higher efficiency than the two-stage architecture, given the same power density in high-frequency applications.

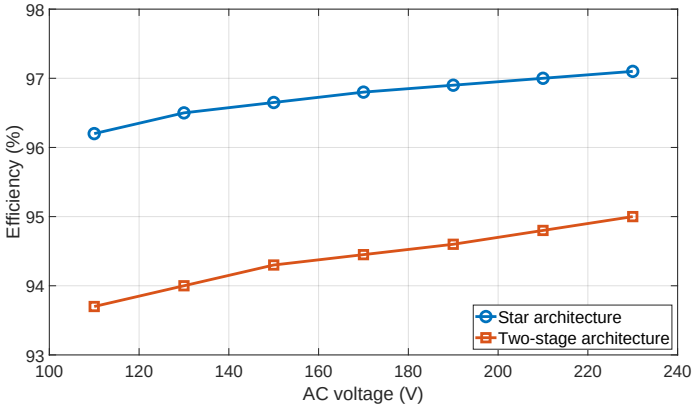


FIGURE 5.34: Efficiency curves of the star architecture and the two-stage architecture at 240-W output across different input voltage. The efficiency of the two-stage architecture is measured at the same prototype as the star architecture.

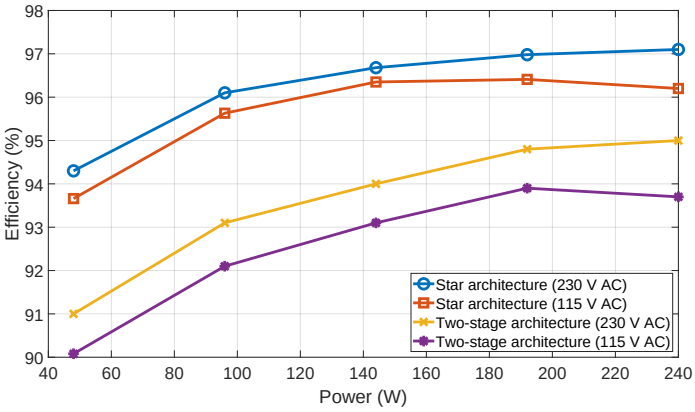


FIGURE 5.35: Efficiency curves of the star architecture and the two-stage architecture at different power levels.

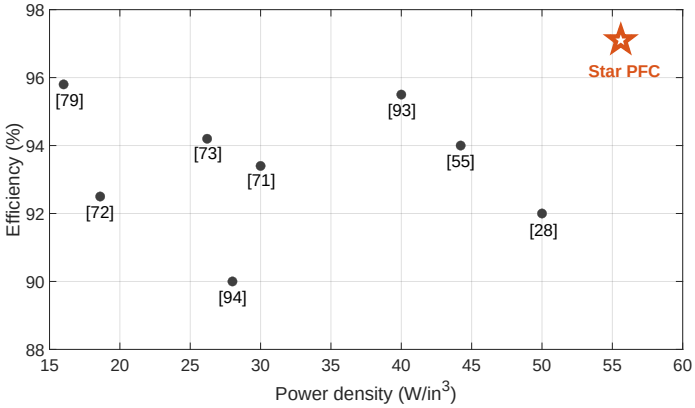


FIGURE 5.36: Comparison of efficiency and power density with recent works.

TABLE 5.6: Comparison between recent publications

	[28]	[55]	[93]	[71]	[94]	[73]	[72]	[79]	This work
Year	2019	2016	2019	2019	2018	2022	2022	2022	2022
Number of magnetics	4	2	1	2	3	3	2	2	2
Number of FETs	10	8	3	4	17	8	4	6	9
ZVS of all FETs	×	√	×	×	×	×	×	×	√
Control	Digital	Digital	Digital	Analog	Digital	Digital	Digital	Analog	Analog
Output voltage (V)	12	20	48	20	24	28–42	100	19	48
Maximum f_{sw} (kHz)	2000	1000	50	100	140	60	50	120	300
Power (W)	150	65	48	100	600	170	100	250	240
Full-load efficiency (%)	92	94	95.5	93.4	90	94.2	92.5	95.8	97.1
Power density (W/in^3)	50	44.22	40	30	28	26.2	18.6	16	55.6

The proposed architecture is also compared with other recent publications at similar power levels, as summarized in Table. 5.6. The comparison shows that the star architecture can outperform recently published solutions in efficiency, power density, and control simplicity.

5.7 Summary

This chapter presents a star architecture to achieve better trade-offs between power density and efficiency than the two-stage architecture by realizing CCM operations and full-range ZVS simultaneously. A 300-kHz, 240-W, 48-V-output, and universal-input prototype is built to verify the performance of the star architecture, demonstrating high power factor, constant output voltage, 97.1 % full-load efficiency, 55.6 W/in^3 power density by box volume, and more than 2 % efficiency improvements over the two-stage architecture. Compared to other recently published PFC solutions, the proposed solution shows improvements in control simplicity, conversion efficiency, and power density. The star architecture also implies that there can be more benefits by considering the operations and topologies of the two stages holistically rather than focusing on optimizing the performance of each stage.

CHAPTER 6

Conclusion

This thesis investigates new approaches, including a new control method, a new PFC front end, and two new power architectures, to improve the performance of single-phase AC–DC converters. It has been demonstrated that there exists plenty of room for performance improvements compared with state-of-the-art commercial practices. The improvements include (I) a 92 % size reduction of buffer capacitors and a reduced number of active switches and magnetics in the newly developed control method for the ACF converter, (II) a 47 % size reduction of magnetics and a 21 % size reduction of buffer capacitors in the new PFC front end, (III) full-range ZVS of all active switches under a constant switching frequency while saving one high-frequency diode as demonstrated in the stacked-switch architecture, and (IV) best-in-class power density (55.6 W/in^3) and efficiency (97.1 %) in a 240-W, universal-input, 48-V output PFC application as demonstrated in the star architecture.

1 Appendix

1.1 Derivations of f_{sw}

Neglecting the switching deadtime and assuming v_{Cin} is constant within T_s, the operating waveform of i_L can be approximated by a three-segment piecewise linear waveform per switching period shown in Fig. .1. Suppose that f_{sw} is sufficiently fast such that the average i_L and i_{Lm} over T_s can be regarded as constant, then voltage-second balance principle applies to L and L_m. Accordingly, we have (.1) and (.2). Meanwhile, by applying the charge balance principle to C_o, we have (.3).

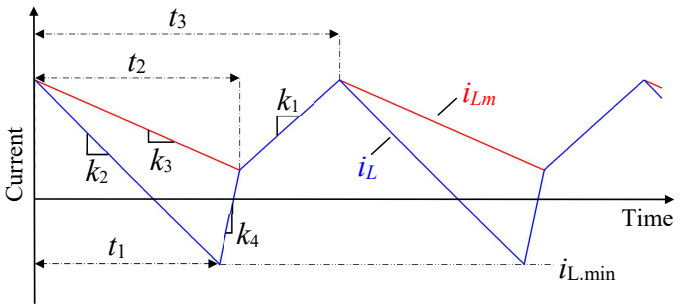


FIGURE .1: Detailed waveforms of i_L and i_{Lm}.

$$k_2 t_1 + k_4(t_2 - t_1) + k_1(t_3 - t_2) = 0 \tag{.1}$$

$$k_3 t_2 + k_1(t_3 - t_2) = 0 \tag{.2}$$

$$\int_0^{t_2} n v_o (i_{Lm} - i_L)\, dx = p_o t_3, \tag{.3}$$

where $t_1 - t_3$ are defined in Fig. .1. Solving (.1) – (.3) for $t_1 - t_3$, we have

$$t_1 = -\frac{2Lp_o(nv_o(L + L_m) + L_m v_{Cin})}{nv_{Cin}v_o(L_m v_b - nv_o(L + L_m))} \tag{.4}$$

$$t_2 = \frac{2LL_m p_o(v_b + v_{Cin})}{nv_{Cin}v_o(L_m v_b - nv_o(L + L_m))} \tag{.5}$$

$$t_3 = \frac{2Lp_o(v_b + v_{Cin})(nv_o(L + L_m) + L_m v_{Cin})}{nv_o v_{Cin}^2(L_m v_b - nv_o(L + L_m))}. \tag{.6}$$

f_{sw} is thus:

$$f_{sw} = \frac{1}{t_3} = \frac{nv_o v_{Cin}^2(L_m v_b - nv_o(L + L_m))}{2Lp_o(v_b + v_{Cin})(nv_o(L + L_m) + L_m v_{Cin})}. \tag{.7}$$

1.2 Derivations of $i_{L.min}$

The energy to C_b in each switching period can be calculated as

$$p_b t_3 = \int_0^{t_1} i_L v_b\, dt = \int_0^{t_1} (i_{L.min} - k_2 t_1 + k_1 t) v_b\, dt, \tag{.8}$$

where p_b refers to the instantaneous power to C_b. Solving (.8), we have

$$i_{L.min} = \frac{p_b T_3}{T_1 v_b} - \frac{T_1(v_b - nv_o)}{2L}. \tag{.9}$$

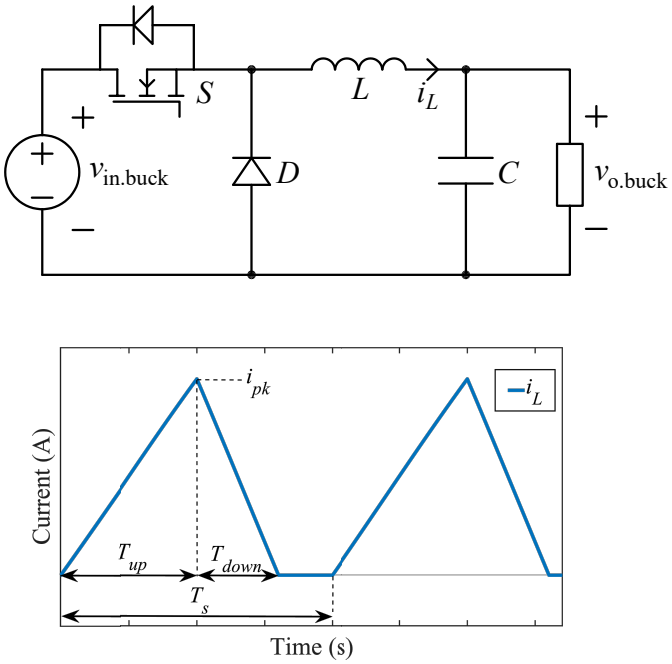


FIGURE .2: Topology and operating waveform of a buck converter.

1.3 Maximum Magnetic Energy Storage in Buck and Boost Converters

This section derives the maximum magnetic energy storage in DCM buck and boost converter and analyzes how it relates to the power level, switching period, and voltage ratio. Fig. .2 shows the buck topology and its typical waveforms under DCM operation. The maximum energy storage of L occurs when the inductor current reaches its peak, so E_{buck} can be calculated as

$$E_{buck} = \frac{L i_{pk}^2}{2} \tag{.10}$$

where i_{pk} is the peak i_L in a switching cycle.

T_{up} and T_{down} denote the rise time and fall time of i_L, respectively. T_{up} and T_{down} can be calculated as

$$T_{up} = \frac{i_{pk} L}{v_{in.buck} - v_{o.buck}} \tag{.11}$$

and

$$T_{down} = \frac{i_{pk} L}{v_{o.buck}}. \tag{.12}$$

In a switching cycle, the average i_L is the load current and can be calculated as the triangle area divided by the switching period, so we have

$$\frac{P_{buck}}{v_{o.buck}} = \frac{(T_{up} + T_{down})i_{pk}}{T_s}, \tag{.13}$$

where P_{buck} is the output power of the buck converter. The four equations, (.10) $\sim$ (.13), are a system of equations with four variables, T_{up}, T_{down}, i_{pk}, and E_{buck},. After solving the four equations, E_{buck} is calculate as

$$E_{buck} = P_{buck}T_s(1 - \frac{v_{o.buck}}{v_{in.buck}}). \tag{.14}$$

The boost converter operated in DCM has the same inductor current waveform as in Fig. .2. The maximum magnetic energy storage in the DCM boost converter, E_{boost}, can be calculated as

$$E_{boost} = \frac{L_{boost}i_{pk.boost}^2}{2}, \tag{.15}$$

where $i_{pk.boost}$ is the peak inductor current in the boost converter and L_{boost} is the inductance of the boost inductor. The rise time and fall time of inductor current in a boost converter can be calculated as

$$T_{up.boost} = \frac{i_{pk.boost}L_{boost}}{v_{in.boost}} \tag{.16}$$

and

$$T_{down.boost} = \frac{i_{pk.boost}L_{boost}}{v_{o.boost} - v_{in.boost}}, \tag{.17}$$

where $v_{o.boost}$ is the output voltage of the boost converter, and $v_{in.boost}$ is the input voltage of the boost converter. The average inductor current in the boost converter is essentially the input current, so we have

$$\frac{P_{boost}}{v_{in.boost}} = \frac{(T_{up} + T_{down})i_{pk.boost}}{T_s}, \tag{.18}$$

where P_{boost} is the output power of the boost converter. E_{boost} can be calculated by solving (.15) $\sim$ (.18) and is derived as

$$E_{boost} = P_{boost}T_s(1 - \frac{v_{in.boost}}{v_{o.boost}}). \tag{.19}$$

The above analysis shows that the magnetic energy storage of DCM buck and boost converters are proportional to the power and switching period, indicating that increasing switching frequency can effectively reduce the magnetic energy storage and size of inductors. Also, it is noticed that the voltage ratio determines the magnetic energy storage and the magnetic energy storage can be greatly reduced if the voltage ratio is close to 1.

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