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Demonstration of High-Temperature Operation of Beta-Gallium Oxide (β-Ga2O3) Metal-Oxide-Semiconductor Field Effect Transistors (MOSFET) with Electrostatic Model in COMSOL

Nicholas Paul Sepelak
Wright State University

DEMONSTRATION OF HIGH-TEMPERATURE OPERATION OF BETA-GALLIUM OXIDE (β-Ga_2O_3) METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTORS (MOSFET) WITH ELECTROSTATIC MODEL IN COMSOL

A thesis submitted in partial fulfillment of

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By

NICHOLAS PAUL SEPELAK

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I HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER MY SUPERVISION BY Nicholas Paul Sepelak ENTITLED Demonstration of High-Temperature Operation of Beta-Gallium Oxide (β-Ga_2O_3) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) with Electrostatic Model in COMSOL BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Master of Science in Mechanical Engineering.

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Hamed Attariani, Ph.D
Thesis Director

_____

Raghavan Srinivasan, Ph.D., PE.
Chair, Mechanical and Materials Engineering Department

Committee on Final Examination:

_____

Hamed Attariani, Ph.D

_____

Weisong Wang, Ph.D

_____

James Menart, Ph.D

_____

Shu Schiller, Ph.D.
Interim Dean of the Graduate School

Abstract

Sepelak, Nicholas Paul. M.S.M.E., Department of Mechanical and Materials Engineering, Wright State University 2022. Demonstration of High-Temperature Operation of Beta-Gallium Oxide (β-Ga2O3) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET) with Electrostatic Model in COMSOL

β-Ga_2O_3 is a robust semiconductor material set with a large band gap of ~4.8 eV, low intrinsic carrier concentration, and high melting point that offers a stable platform for operating electronic devices at high temperatures and extreme environments. The first half of this thesis will cover the fabrication of a fixture and packaging to test electronic components at high temperatures. Then it will highlight the characterization of β-Ga_2O_3 field effect transistors from room temperature (RT) up to 500 °C. The devices, fabricated with Ni/Au and Al_2O_3 gate metal-oxide-semiconductor (MOS), demonstrate stable operation up to 500 ^oC. The tested device shows no measured current degradation in the I_D-V_D characteristics up to 450 ^oC. Improvements to the drain current, I_D within this temperature range are due to activation carriers from dopants/traps and the negative push in threshold voltage, V_T. The device exhibits a drop in I_D at 500 °C; however, device characteristics recover once the device returns to RT. Even after 20 hours of device operation at 500 °C, the device shows negligible degradation. Device characteristics such as gate leakage, I_{ON}/I_{OFF} ratio, g_m, R_{on}, and contact resistance show monotonic variation with temperature. The experimental results suggest that an optimized choice of metals and gate dielectrics β-Ga_2O_3 will provide a platform for device operation at high temperatures and extreme environments. The second half of the thesis focuses on creating an electrostatic model of a metal-oxide-semiconductor field effect transistor with COMSOL finite element analysis software to understand the physics behind semiconductor technology.

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Acknowledgments

To my mother, thank you for pushing me to make this journey in my life. Your love and support were always a light in my life and are greatly missed. I know that you would be very proud of me.

To my father, for always having the advice that I need to hear even when I don't want to hear it.

To my children, I hope that observing me go back to school will help you understand the value of hard work as well as the importance of finding happiness and balance in your life. I know the last five years have been difficult at times, but the future is bright, and it is important to always look forward. To Angela, thank you for the love and support that you gave me while I pushed through difficult times to complete my degrees. It means the world to me to share these experiences with you.

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You can indeed achieve your goals when you put your mind and effort towards them, but it is a lot easier to accomplish them when you have the love and support that I have received from so many, Thank you.

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Chapter 1. Introduction to Beta-Gallium Oxide (β-Ga_2O_3)

1.1. Introduction

Beta-gallium oxide (β-Ga_2O_3) is an emerging semiconductor that has shown high promise for applications in power electronics [1]. With a wide band gap (WBG) of 4.6-4.9 eV, Ga_2O_3 also boasts a hefty critical field strength of 8 MV/cm along with decent transport properties of 100-150 $cm^2V^{-1} \cdot s^{-1}$[2]. Coupled with these values, Ga_2O_3 pushes its Baliga's figure of merit (BFOM) past those of silicon carbide (SiC) and gallium nitride (GaN) [3]. Intrinsically, carrier activation does not ramp up until after 900 °C in Ga_2O_3 making it a potential candidate for high-temperature electronics. From a cost perspective, Ga_2O_3 also has the potential to be very cost-effective, as Ga_2O_3 is the only ultra-wide band gap (UWB) semiconductor where melt–growth is possible with 100 mm wafers in production.

Despite these positives, Ga_2O_3 has very low thermal conductivity. Anisotropic in nature, the thermal conductive at its highest in the [010] plane is 22.8 $W/m \cdot K$ and as low as 9.5 $W/m \cdot K$ in the [100] plane [4]. This low thermal conductivity is undesirable when considering high-frequency RF performance in Ga_2O_3. Many studies have endeavored to model and explore many ways to remove heat from the channel. This includes backside thinning, flip chip integration to SiC, and diamond heterojunctions, just to name a few [5]. Ga_2O_3 may not be able to compete with GaN when it comes to RF performance, but its high breakdown field will push the limits when it comes to power-switching devices [6]. There may also be a place for Ga_2O_3 when considering high-temperature low frequency RF performance.

The purpose of this study is to explore the high-temperature viability of Ga_2O_3 transistors due to their wide band gap and high breakdown field. In this study, Ga_2O_3 metal-oxide field effect transistors, MOSFETs are tested with the use of a special fixture from room temperature up to 500

°C in ambient air to explore the effects of an oxidizing environment. Some of the challenges of fabricating a fixture to test electrical components at high temperatures will be addressed as well as, highlighting some of the challenges involved in fabricating a transistor that will operate at high temperatures. The second half of this study involves the creation of an electrostatic model of a Ga_2O_3 MOSFET to better understand semiconductor device physics.

1.2. Wide Band Gap Semiconductors

Silicon is the dominant semiconductor used today for most integrated circuit applications, it finds its limit when used for radio frequency (RF) and power switching applications. High current, power, and temperature environments which are typical to power switching and RF are particularly difficult for silicon and have left these applications open to other semiconductor types. Discrete or integrated devices are defined as power devices if they deliver more than 1 Watts to an electrical load, or they continuously operate at > 30 V [7].

The band gap of the material influences the number of intrinsic carriers that can be activated at a specific temperature and can be seen in Equation (1) [8].

$$n_i = \sqrt{N_C N_V} e^{-E_g/2K_bT}, \left[1/cm^3\right] \quad (1)$$

where N_C and N_V are the intrinsic density of states of the conduction and valence bands respectively, E_g is the bandgap, K_b is the Boltzmann constant, and T is the temperature in Kelvin. Silicon and gallium arsenide (GaAs) have bandgaps of ~1.1 and 1.4 respectively. Other compound semiconductors such as SiC with a bandgap of ~3.3 eV and gallium nitride GaN with a band gap of ~3.4 eV have filled in the void for most power electronics and RF devices. β-Ga_2O_3 has a bandgap of ~4.8 eV and requires a significant temperature to activate intrinsic carriers to the point where the device would cease to operate as a semiconductor. This happens when the intrinsic

carrier density approaches the conduction band density of states. The temperature dependence of the intrinsic carrier density can be seen in Figure 1.

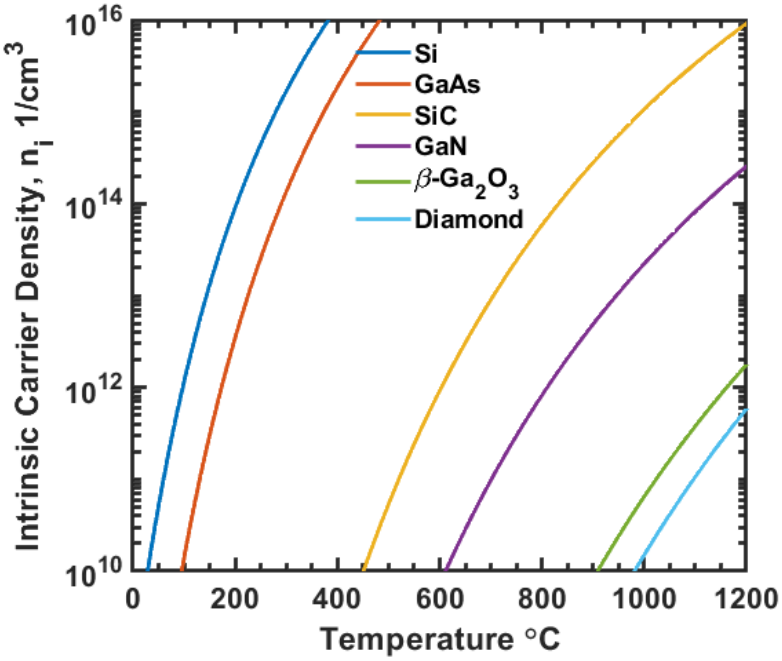

Figure 1: Intrinsic carrier density as a function of temperature.

As the band gap increases, the temperature required to activate intrinsic carriers increases intuitively. The band gap of a semiconductor material is also a function of temperature. Equation (2) shows the temperature dependence of the band gap. Eg (0) is the band gap at 0 K, T is the temperature in Kelvin, while α and β are fitting parameters.

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{(T+\beta)},\ [eV] \tag{2}$$

From this equation, it is important to realize that the band gap reduces as temperature increases. Figure 2 shows the reduction in the band gap of gallium oxide. Since the reduction is ~0.2 eV, the effect is minimal but still considered.

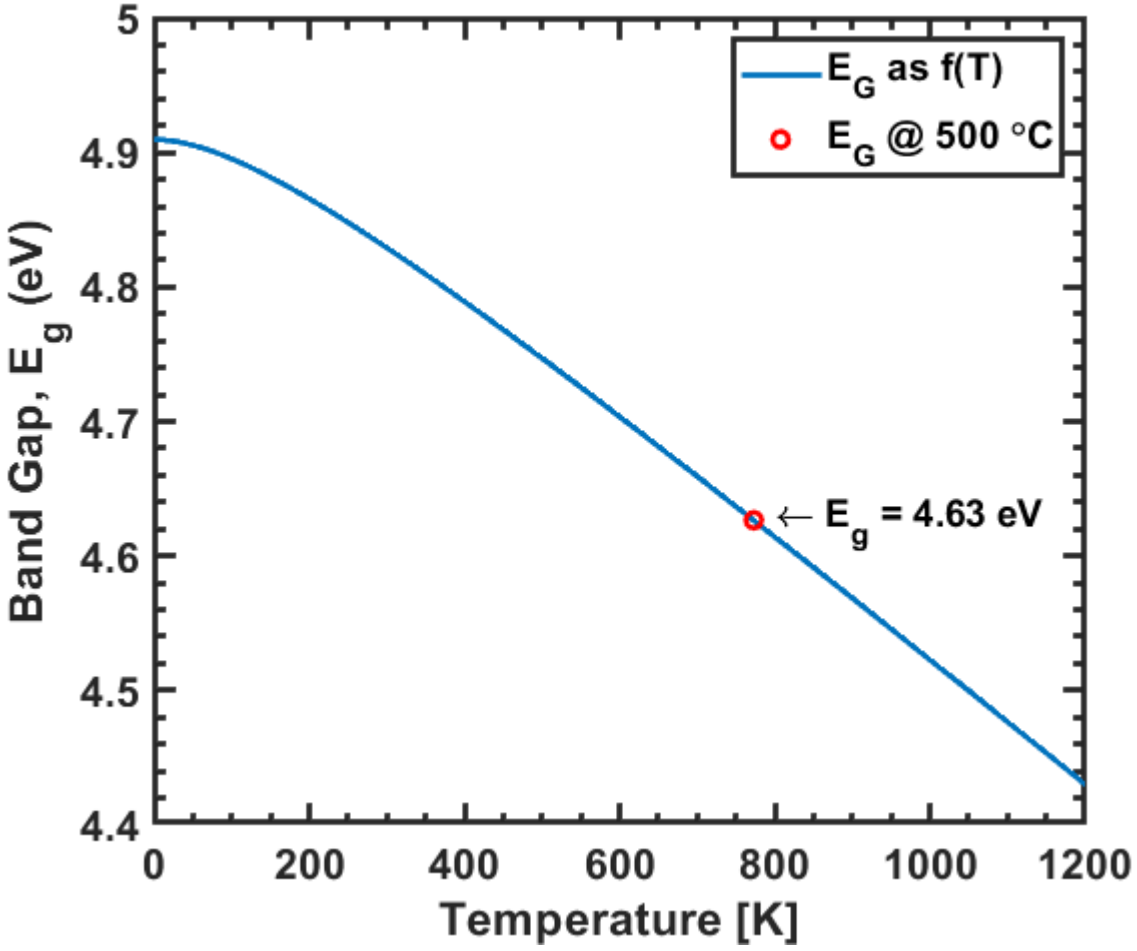

Figure 2: The band gap of β-Ga_2O_3 as a function of temperature. The band gap reduces from 4.82 eV at 25 °C to 4.63 eV at 500 °C

Since several WBG semiconductors are being used for power switching and RF applications, a way to classify their potential was needed. These classification merits are called figures of merits (FOMs). There are several FOMs used today to classify materials and benchmark devices. One of the first was Johnson's figure of merit (JFOM) which can be defined by,

$$JFOM = \frac{E_c v_{sat}}{2\pi} \tag{3}$$

In equation 3, E_c is the critical electric field and v_{sat} is the saturation velocity. Johnson's figure of merit is used to define the cut-off frequency and the maximum applied voltage to a device [9]. Another FOM that is used for device benchmarking is Baliga's figure of merit (BFOM) which is defined by,

$$BFOM = \varepsilon_r \mu E_c^3 \tag{4}$$

where ε_r is the relative dielectric constant of the material and μ is the bulk mobility of the material. The BFOM compares the on-resistance, R_{on} of a device to the breakdown voltage, V_{bk}. This is relatable in device design as it correlates that a device with a larger gate-to-drain length, $L_{GD,}$ should theoretically have a larger breakdown voltage as the on-resistance is higher. It is important to keep in mind that BFOM was derived with a vertical device in mind, so there are ambiguities and assumptions when applying it to a lateral device [10], [11].

Baliga also derived another FOM known as Baliga's high-frequency figure of merit (BHFFOM). It can be defined with the equation,

$$BHFFOM = \frac{1}{(R_{on,sp} C_{in,sp})} \tag{5}$$

In this equation, $R_{on,sp}$ is the specific on resistance and $C_{in,sp}$ is the input capacitance. BHFFOM was Baliga's way to account for switching loss in devices. In Table 1, the material properties of specific semiconductors along with FOMs are compared. The FOMs are normalized to silicon and all the materials are assumed n-type except for diamond as only p-type has been demonstrated in the literature [11].

Table 1: Material parameters and FOMs of different semiconductors. The figures of merits are normalized to silicon and are for n-type devices except for diamond [12].

Material	**Si** [12]	**GaAs** [12]	**4H-SiC** [12]	**GaN** [12]	**β-Ga_2O_3**	**Diamond** [13]
Band gap, E_g $(eV\ at\ 300\ K)$	1.12	1.43	3.2	3.4	4.8	5.5
Dielectric Constant, ε_r	11.9	13.0	10.0	9.5	10.2	5.5
Saturated Drift Velocity, v_{sat} $(\times 10^{17}\ cm/s)$	1.0	1.0	2.0	2.5	1.1-2.0	1.1
Critical Electric Field, E_c (MV/cm)	0.25	0.3	3.0-4.0	3.0	8.0	> 4.0
Thermal Conductivity, λ $(W/m \cdot K\ at\ 300\ K)$	150	50	300-400	130	10-23	2090
Bulk Mobility, μ $(cm^2/V \cdot s\ at\ 300\ K)$	1350	8500	950	1000	150-300	2000 [14]
Baliga's DC figure of merit, BFOM $(\mu\varepsilon E_c^3)$	1	12	1022-2422	1022	3120-6242	2804
Baliga's high-frequency figure of merit, BHFFOM (μE_c^2)	1	9	101-180	107	114-228	379
Johnson's figure of merit, JFOM $(v_{sat}E_c)$	1	1.2	24-32	30	35-64	17.6

1.3. Beta-Gallium Oxide Structure and Properties

Ga2O3 is relatively new to the field of power electronics with the first transistors being fabricated in 2006 [15], [16]. The compound itself has been known since 1875 when gallium was discovered and has been studied for other applications such as high-temperature oxygen sensing and solar blind photodiodes [17], [18]. Ga2O3 has five different polymorphs and of those five, three of which have a measurable bandgap. α-Ga203 has a bandgap higher than β-Ga2O3 at 5.5 eV and has been grown on sapphire substrates as it has a triagonal-corundum crystal structure [19]. The main issue with α-Ga203 is that it converts to β-Ga2O3 at high temperatures that are required for growth and fabrication [20]. Since the beta-phase is the most stable polymorph, most of the device research today is done on β-Ga2O3.

Another note about β-Ga2O3, it is the only WBG semiconductor that can be grown by melt. Other WBG semiconductors like SiC and GaN are grown by chemical vapor deposition (CVD). This makes the process of producing SiC and GaN expensive. There is potential for β-Ga2O3 to be grown at the size of Silicon boules today, which would drive costs down dramatically. Currently, four-inch (100mm) wafers are being produced commercially [1].

With a monoclinic crystal structure, β-Ga2O3 has lattice constants of a = 1.22 nm, b = 0.30, nm c = 0.58 nm with the β direction at 104 degrees and α and γ directions at 90 degrees. The crystal structure of β-Ga2O3 can be seen in figure 3a.

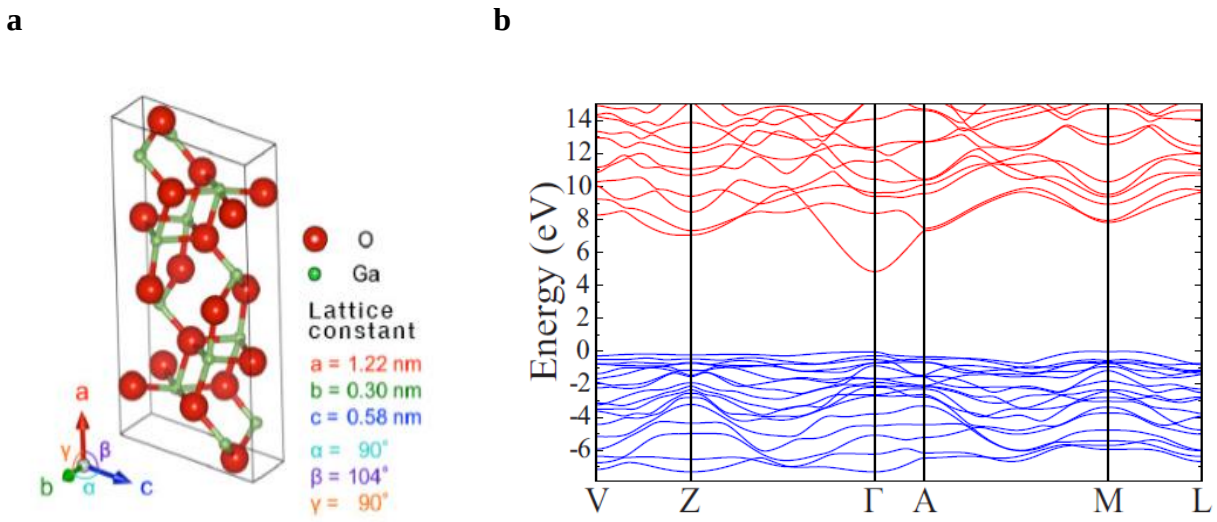

Figure 3: a) The monoclinic crystal structure of β-Ga_2O_3 [21]. **b)** The band structure plot for β-Ga_2O_3. The flat valence band suggests a large effective mass of holes [22].

Figure 3b show the energy band structure derived using density functional theory (DFT) [22]. The flatness of the valence band suggests a large effective mass of holes, $m_h = 40.0m_e$. The effective mass of electrons, m_c is measured at approximately, $0.28m_e$. The effective mass of electrons and hole are used to calculate the effective density of states,

$$N_x = 2\left(\frac{2\pi m_x k_b T}{h^2}\right)^{3/2},\ \left[1/cm^3\right] \quad (6)$$

In equation 6, N_x can represent either N_C or N_V, which is representative of the effective density of states of the conduction band and valence band respectively. The effective mass of electrons, m_c and the effective mass of holes, m_h would replace m_x in Eq. 6. It is important to note that β-Ga2O3 is an n-type material. Since the holes have a large effective mass, they do not move around and have very low mobility [22]. It is a general assumption with β-Ga2O3, that the dopant concentration, N, is,

$$N = N_d - N_a,\ \left[1/cm^3\right] \quad (7)$$

Where N_d is the donor concentration and N_a is the acceptor concentration, N_a is generally ignored and, N becomes,

$$N = N_d,\ \left[1/cm^3\right] \quad (8)$$

Some studies have shown that there are deep acceptors that may be activated and influence breakdown voltage [23].

1.4. MOSFETs

There are many types of transistors out there and too many to describe in the scope of this paper. This paper is going to focus on metal-oxide-semiconductor field effect transistors (MOSFETs). This implies that an oxide such as aluminum oxide (Al_2O_3) or silicon dioxide (SiO_2) is in between the gate metal-semiconductor junction. MOSFETs are the predominant type of transistor in power electronics. Like a MOSFET is a metal-insulator-semiconductor field effect transistor (MISFET) where the devices have a nitride between the metal-semiconductor junction such as silicon nitride (Si2N4) versus the oxide in MOSFETs. Since the current transport in MOSFETs is predominately

one charge (hence the notion that β-Ga2O3 is an n-type material), MOSFETs are unipolar devices [24]. MOSFETs can be designed to be either depletion mode, which is when the device is normally on and must be biased at the gate to turn the device off, or enhancement mode (E-mode), where a bias of the gate allows current to flow. The enhancement mode device is the most desirable for power electronics as the device is only on when you want it to be and for obvious safety reasons. The design methods for E-mode lateral devices include thinning the channel or fabricating Fin FETs [25], [26]. These designs are beyond the scope of this paper and only depletion mode devices will be studied. Figure 4 shows a typical cross-sectional schematic of a MOSFET studied in this paper.

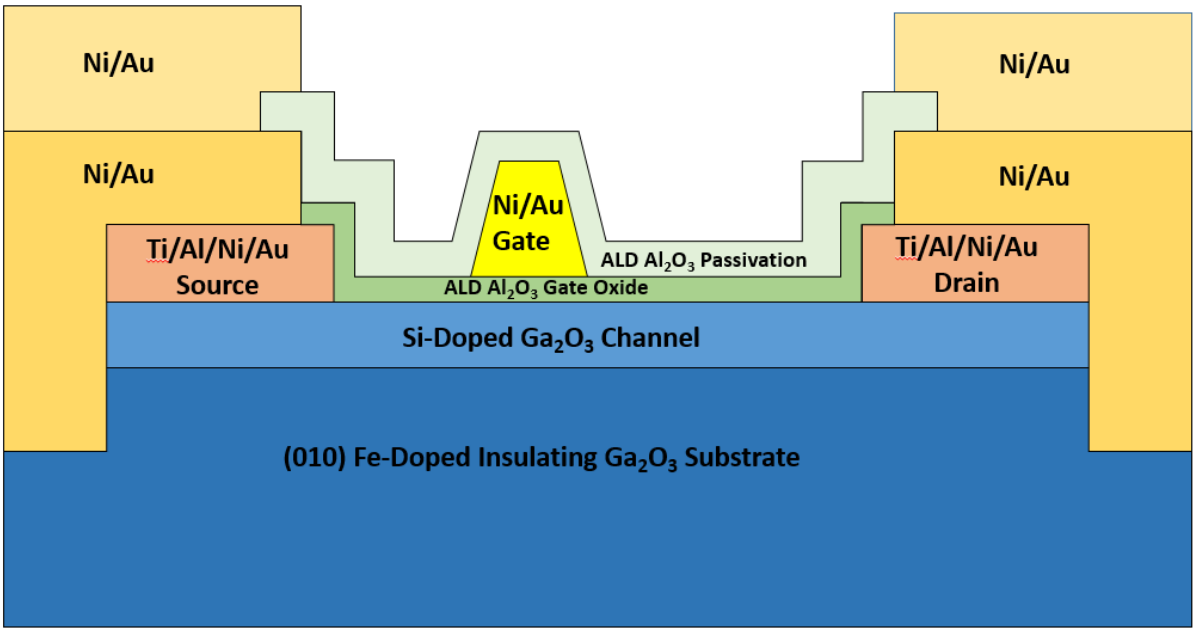

Figure 4: A typical cross-section of a MOSFET. The dielectric under the gate is what distinguished a MOSFET from a MESFET.

A typical fabrication process for a lateral device is as follows. An insulating substrate, typically Fe-doped, has an epitaxial layer of β-Ga2O3 grown on it either by molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD). During the deposition process the dopants, typically silicon, are added. The dopants are targeted to specific concentrations, typically in the 10^{17} $[1/cm^3]$ range but can vary depending on the design of the device. The desired epitaxy layer thickness can also vary on device design but for the sake of this paper, the desired thickness is 65 nm. Between each step of the process going forward, the wafer will be coated with a photoresist (PR). There is a mask design for each step of the process so that when the photoresist is exposed to ultraviolet (UV) light, the PR is developed away in the desired areas.

The first step in the process after the epi-layer deposition is the mesa/alignment key etch by inductively coupled plasma etching (ICP). This step isolates the conductive epi-layer in the areas where the device is to be fabricated as well as establishes an alignment key so the subsequent steps can be aligned to the correct locations. The next step in the process is to deposit the ohmic contacts. This is done by evaporating layers of Ti/Al/Ni/Au onto the wafer and then removing the excess metal by a lift-off method. This method uses two different photoresists so that the evaporated metal sticks to the wafer where you want it to and to the PR where you don't want it to. The metal is then peeled away with a special tape and recycled. After the ohmic contacts are deposited and the wafers are cleaned, the ohmic contacts are annealed in a rapid thermal annealing machine (RTA) up to 470 °C. After ohmic contacts, the next step of the process is to deposit the Al_2O_3 gate oxide. This is typically done as a blanket deposition by plasma-enhanced atomic layer deposition (ALD). Gate oxide thicknesses are usually targeted to be 20 nm or 30 nm depending on the device design. The unwanted oxide is etched away by reactive-ion etching (RIE). Once the gate oxide step is complete; the next steps are to add the first layer of Ni/Au pad metal and gates. The gates can be

written optically or by e-beam lithography and can vary in material and between which step of the process, they are deposited. After the first pad-metal layer and gates have been deposited, a passivation layer of o Al_2O_3 is deposited by ALD. This layer is usually thicker than the gate oxide. Last but not always, another layer of pad metal is evaporated. This extra layer of Ni/Au aids in wire bonding the devices as well as thermally.

1.5. High-Temperature Electronics

For many years, silicon has been the dominant semiconductor in almost every aspect of electronics. Silicon is unmatched in integrated circuits and is pushing the boundaries of Moore's law. It has become very cheap to manufacture as it can be fabricated on 12-inch wafers. The main downside to silicon for certain applications is that it requires active cooling as intrinsically, silicon ceases to function as a semiconductor at temperatures greater than 250 °C. This requires that silicon electronic components have active cooling. The problem that comes along with active cooling is the space and energy requirements to go along with it. There have been many interesting ways to help mitigate heat from electronics while also trying to save space and power. A few examples of these mitigation methods are heat pipes, and in the case of avionics, fuel thermal management systems where the aircraft fuel is used to draw thermal energy from the electronics and then dump it to the engine [27]–[29].

Another approach to high-temperature electronics is to design the devices so that active cooling is not needed at all. Researchers at NASA Glenn have been working with WBG semiconductor SiC for more than 20 years and have successfully demonstrated the stable operation of integrated circuits, ICs, at 500 °C for thousands of hours [30]. They have made this possible by taking a step-back approach by using junction field-effect transistors, JFETs which allows them to exploit the band gap of the semiconductor as the barrier height. The team at NASA Glenn has also built a test

chamber that allows them to test electronics at different simulated atmospheres and pressures named GEER, which stands for Glenn extreme environment rig, and has demonstrated the operation of electronic components for 60 days in a simulated Venus atmosphere [31]. SiC, while doing an excellent job in the high-temperature IC realm, has not yet been able to fill the role of power switching and RF in extreme environments.

The approach to the high-temperature operation of electronics without active cooling that NASA has pioneered could most certainly be applied to other technology sectors other than space exploration. For example, high-temperature capable electronics are highly desirable for use in hypersonic aircraft as well as for RF decoy drones that are deployed for electronic countermeasures. Both areas are examples where size and weight constraints apply. In the commercial sector, engine management sensors that can withstand extreme environments are highly desirable. Deep well drilling can benefit from the size and weight capabilities of high-temperature sensors.

Chapter 2. High-Temperature Demonstration of β-Ga_2O_3 MOSFETs

"I must not fear, fear is the mind-killer. Fear is the little-death that brings total obliteration."

-Princess Irulan [32]

"In transistors, heat is the little-death that brings total obliteration."

- Capt Jeremiah Williams, USSF

2.1. High-Temperature Air Ambient Testing Fixture

To test electronic devices at high temperatures, a special testing fixture had to be designed and fabricated. The High-Temperature Air-Ambient Testing Fixture is comprised of several components that work together to make the system operate. It consists of a box furnace, two Source Measurement Units (SMUs), a fixture to allow for connections to the device under test (DUT), and a computer to control the software. Figure 5 shows a schematic of the test setup highlighting the furnace, fixture, SMUs, and laptop.

The furnace is a ThermoFisher-Scientific BF51800 Series 1100 °C, Lindberg/Blue M, Moldatherm box furnace. It can control the temperature from 100 °C up to 1100 °C with a tolerance of ± 2 °C at 1100 °C. The furnace has a PID controller that is programmable with up to five programs with sixteen segments each. This means that the program can consist of eight temperature settings since one segment is needed for the ramp temperature set point and ramp rate and one segment is needed for the temperature soak setting and time. Internal temperature is controlled with a thermocouple that extends into the cavity. There is a 1-inch diameter vent port on the top of the oven which serves as access for the electrical connections to the fixture. One major limitation of this furnace is the inability to control and program the PID controller from an external source such as the laptop which will be explained in greater detail later in this report.

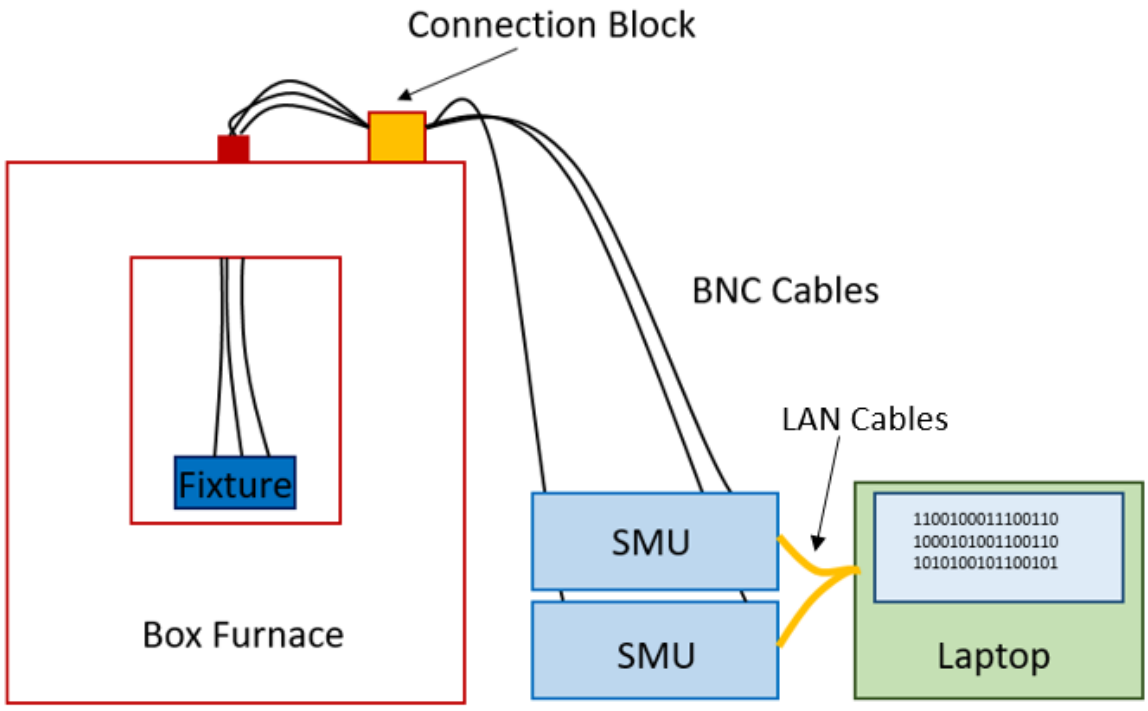

Figure 5: A schematic of the high-temperature testing setup. The fixture is connected through the top of the box furnace to source measure units which are controlled by a script on a laptop computer.

The SMUs used in this study are a pair of Keithley 2612 B Source Meter Units. Each unit has two nodes that can be used as a voltage or current source. The SMUs can measure current down to 10 pA and voltages in μV, and they can source up to 100 V and 1 A of current. In this study, the SMUs are used as voltage sources, and potentials are applied to the DUT's gate and drain. The SMUs measure the resulting current from the applied voltage drop. Each SMU has two channels or nodes. In this study, one SMU will be assigned to control and measure the DUT. The other SMU will be assigned to control the temperature sensor. The SMUs are controlled via LAN to a laptop computer which is running a program called Test Script Builder (TSB) which is free software that comes with the Keithley SMUs. TSB is a Lua-based programming code. The SMUs

can also be controlled via LabVIEW, MATLAB, and Python. In TSB, there are two scripts written to perform the tests highlighted in this study. The subscript is a sweeping script that controls the two channels of one SMU. One channel is dedicated to the gate and the other to the drain.

Three different characterization tests can be performed with the subscript. These tests are the I-V family of curves, gate diode test, and transfer characteristics. The I-V family of curves sets a specific gate voltage and sweeps the drain voltage. The sweep is repeated for subsequent sweeps as the gate voltage is increased until it reaches the final voltage. In this study the gate voltage is set to -8 V and the drain voltage is swept from 0 to +5 V at increments of 0.1 V. the gate voltage is then stepped at increments of +1 V until it reaches 0 V. For the gate diode test and transfer characteristics, the drain is set to a specific voltage and the gate is swept. The gate diode test consists of holding the drain at 0 V and sweeping the gate from -8 V to 0 V whereas, in the transfer characteristic test, the drain is held at 5 V. The gate diodes test is used to understand the amount of leakage current in the device when it is in the off state. The transfer characteristics can be used to understand the max current of the device, $I_{max,}$ and the threshold voltage V_{th}. If the derivative of the transfer curve is taken, the transconductance curve or G_m can be found. The max $G_{m,\ peak}$ is where the derivative goes to zero. The equation for G_m is,

$$G_m = {\Delta I_{DS}}/{\Delta V_{GS}} \tag{9}$$

where ΔI_{DS} is the change in drain current and ΔV_{GS} is the change in gate voltage. If the transfer and transconductance curves are imposed on the same x-axis, a vertical line can be drawn through the G_M curve at its maximum. Where this line intersects the transfer curve is the point where the slope of the transfer curve is constant. At this point, a line can be fitted to the linear region of the transfer curve, and where this line intersects the x-axis is a good estimation for the threshold

voltage, V_{th}. Figure 6 shows a representative transfer and G_M curve with the $G_{M,\,peak,}$ and estimated V_{th}.

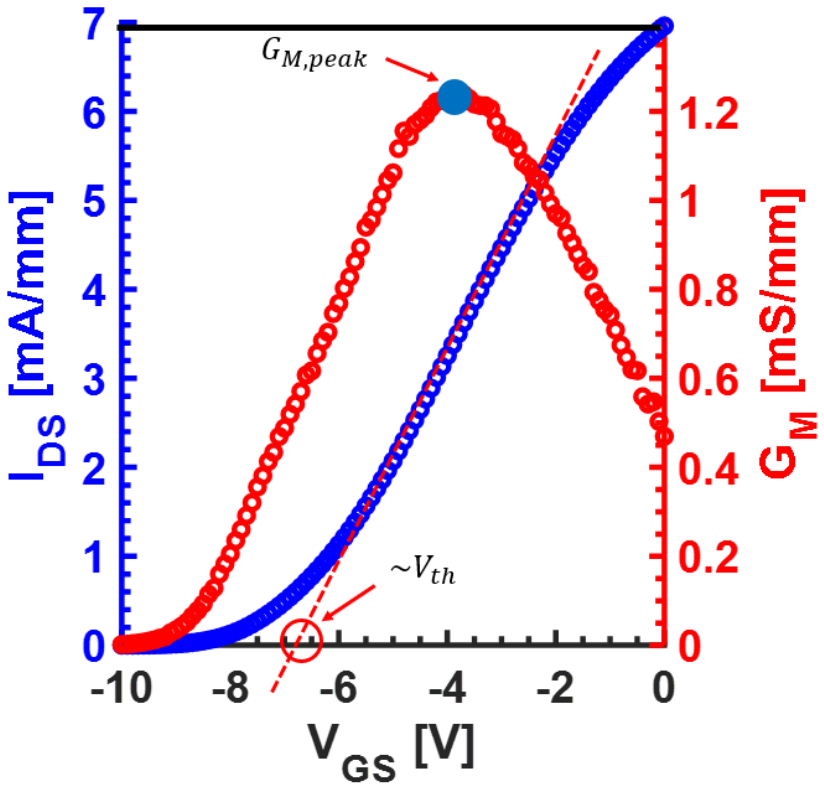

Figure 6: A representative ID-VG curve with GM. The GM is the derivative of the ID-VG curve and the GM, peak is the maximum. The threshold voltage can be estimated by drawing a line along the slope and Vth is approximately where the line crosses the x-axis.

If the y-axis of the transfer curve is plotted in log scale, the on/off ratio of the DUT can be estimated. The sub-threshold slope can be estimated from the slope of the linear region of the log scale transfer curve. To get a better comparison of the performance of the DUT, the measured current is always normalized to the gate width of the device and is typically presented in mA/mm of current or mS/mm for transconductance.

To connect the DUT to the SMUs, a special fixture had to be designed to allow for an electrical connection. The fixture needed to be able to withstand a high-temperature oxidizing environment as the tests were to be performed in an air-ambient atmosphere. The base of the fixture, rocker arms, and side plate supports was machined from a 66 mm thick plate of nickel. Nickel was chosen because of its cost and oxide properties. Nickel forms a stable oxide that does not continue to grow once it has been established [33]. The back plate of the fixture that holds the thermocouple connectors is made from stainless steel and is coated with an AlTiN coating that prevents corrosion. The set screws used in the fixture are also stainless steel and coated with the same coating. The side plates of the fixture support a Macor rod which suspends the rocker arms and allows them to be electrically isolated. Macor is a type of machinable ceramic [34]. Mini K-type ceramic thermocouple connectors allow for easy removal of the fixture from the furnace without having to fish wire in and out every time the fixture or DUT needs to be serviced. Wires run from the thermocouple connectors out of the furnace through a port in the top and connect to a connection block. From the connection block, BNC cables connect the DUT to the SMUs. A resistance temperature detector (RTD) is attached to a thermocouple connector and placed in the vicinity of the DUT. An RTD was chosen as the SMUs used in the study do not have a cold junction point. They do have the capability of attaching a 4-wire RTD to factor out the line resistance, however, when considering the number of wires that need to be run through the one-inch vent port, the 2-wire RTD was chosen. With line resistance a consideration, because any series resistance in the circuit with the RTD will affect the measurement, a silver wire was chosen as it has low resistivity for the length of wire needed. Originally, Ni-200 wire was used for all electrical connections. The nickel wire performed well, however; oxidation eventually played a factor in the wire needing to be replaced periodically. Observing that the silver wire to the RTD required less

maintenance, all the connection wires in the system were replaced with silver wire. Oxidation was no longer a factor as silver oxide decomposes at temperatures greater than 350 °C [35]. The Silver wire can be delicate to work with and care must be taken to not break the wire when servicing the fixture. Figure 7 shows a picture of the test fixture connected inside the box furnace.

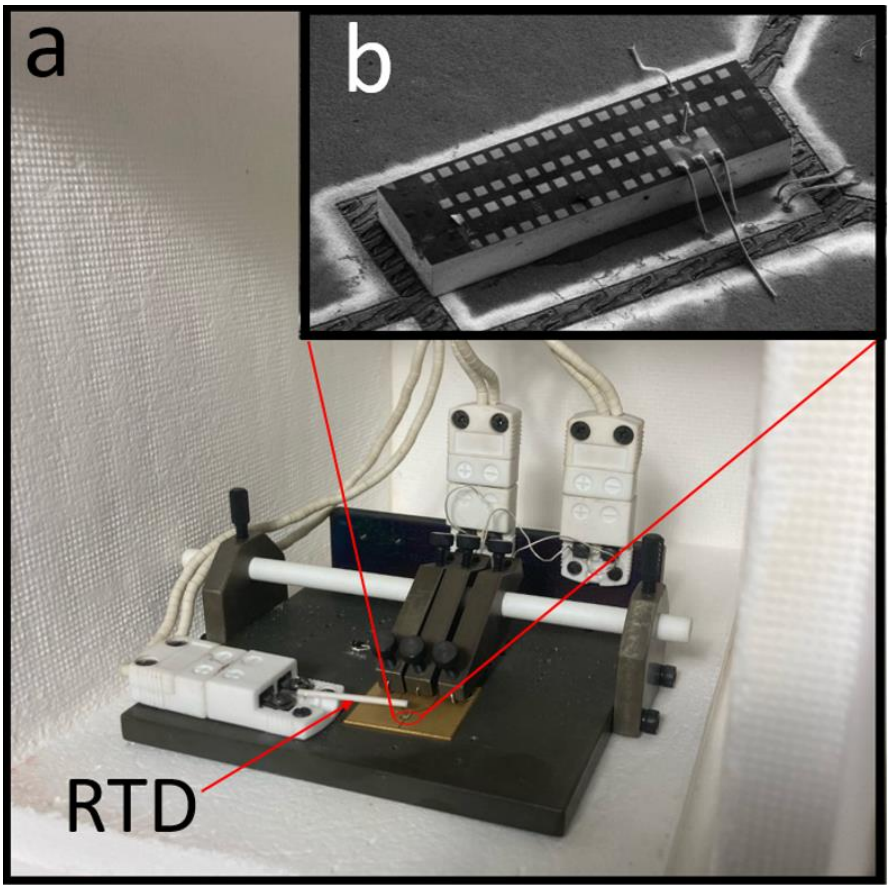

Figure 7: a) the fixture inside the box furnace with a connection that goes through the top of the furnace. The packaged part is connected via rocker arms that are mechanically pressed to the TiAu-plated package. An RTD is positioned close to the DUT to obtain an accurate reading of the temperature as close to the part as possible. **b)** An SEM image of the DUT wire bonded to the package. The three rocker arms correspond to the gate, source, and drain [36].

To connect the DUT electrically with the SMUs, the rocker arms needed a way of contacting the package. The initial thought was to use tungsten needle probes as the method of contact. In early

testing, it was quickly realized that the needle probes would not work for two reasons. First, the stress of the thermal cycling would cause the probe to "walk" and lose connectivity. Second, after two cycles of one hour at 500 °C, the probes would oxidize to the point that they would no longer conduct without removing the oxide form after each run. The next iteration was using some Pt/Ir tunneling microscopy probes. The Pt/Ir probes solved the oxidation problem but still suffer from probe walking. The final solution to the problem of contacting the package was bent around the front edge of the rocker arm and then mechanically depressed onto the package. Set screws on the rocker arms were tightened to fix the position on the Macor rod. Figure 8 shows a rendered CAD illustration of the rocker arm and how it is connected to the package.

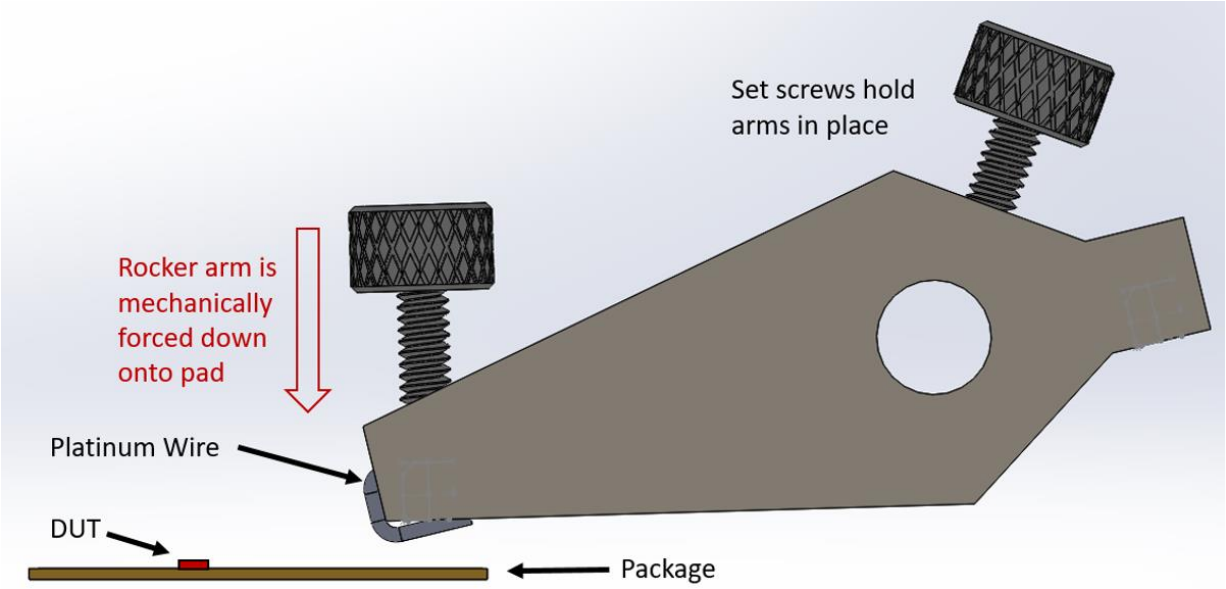

Figure 8: A CAD illustration of how the rocker arms make electrical contact with the packaged part.

The packaging of the device had to be taken into consideration as traditional packaging methods would not stand up to the oxidization and extreme temperature of the test. The next section will discuss packaging and some of the challenges involved.

2.2. Packaging for High-Temperature Electronic Testing

To test devices at high temperatures, it became very clear that it was going to be necessary to fabricate custom packages. The initial package that was used was a design made by Remtec that was used for other testing and was readily available. The packages were made from, 99.6% alumina with a copper thick-film coated with a layer of gold. Two problems quickly surfaced from the design of this package. First, it was clear that the pad size was too small for creating proper contact with needle probes, and quite often the probes would walk off on them during the thermal cycle. Second, the copper film would oxidize through the gold and result in a loss in connectivity.

The second generation of package design consisted of one 25 x 25 x 0.6 mm piece of alumina with 40 nm of Ti deposited by RF sputtering and 3 nm of Au by DC sputtering. Titanium is generally used as a sticking layer for the gold to adhere to. After the Ti/Au was sputtered on the package, an LPKF ProtoLaser, laser ablation tool was used to ablate the metal from the surface of the package to create three pad areas for electrical contact and a pad for the device to connect. This method for packaging devices for high-temperature testing worked effectively until the laser ablation tool went into disrepair and it was decided that the tool would not be fixed due to cost.

The third iteration of packing was now needed to make packages for high-temperature testing. Using lithography fabrication techniques, a third iteration of the high-temperature package was created. A 100 mm Alumina wafer was cleaned with an Acetone/Isopropyl Alcohol and subjected to a 4 min oxygen plasma ash. The wafers received 200/1500 A of Ti/AU for a seed layer. Using photolithography processes, the packaging pattern was developed on the wafer. Electro-plating was used to deposit a 3 μm thick layer of gold to allow for reliable wire bonding. The subsequent packages were diced from the wafer using a dicing saw. Figure 9 shows images of the second

iteration of the high-temperature package and a complete 100 mm alumina wafer before being diced.

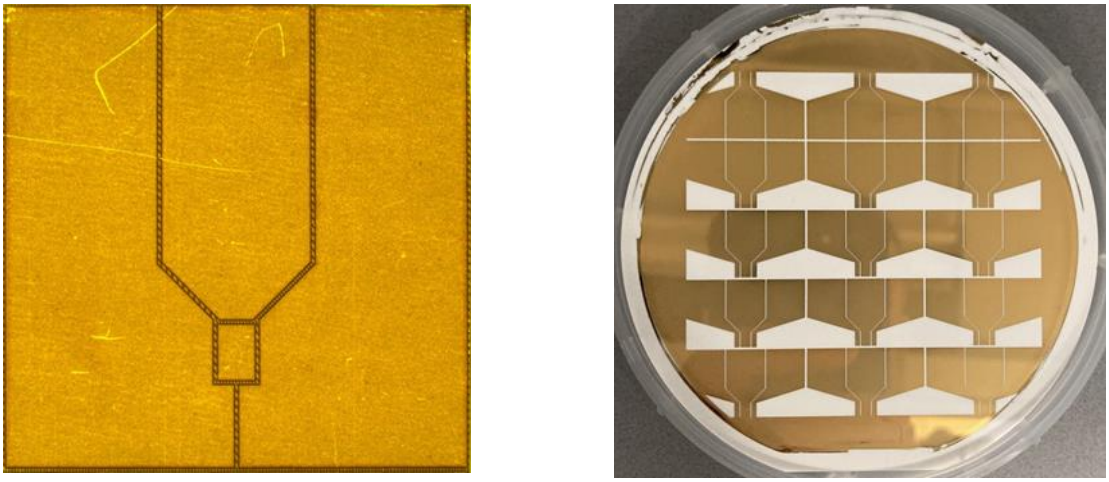

Figure 9: a) The first package design consists of a 1-inch square of alumina with TiAu sputtered on top and laser-ablated channels. **b)** The second package design was created using lithography and plating Au onto a TiAu seed layer on a 100 mm alumina wafer.

2.3. Device Fabrication

Fig. 1a shows a cross-sectional schematic of a MOSFET fabricated on a (010) Fe-doped Ga_2O_3 substrate using 65 nm, $3x10^{17}$ cm^{-3} Si-doped Ga_2O_3 channel grown by Molecular-Beam Epitaxy (MBE). The device mesa was defined using a BCL_3 inductively coupled plasma (ICP) mesa etch. Next the source and drain ohmic contacts were deposited using electron beam evaporation of Ti/Al/Ni/Au. The ohmic contacts were annealed at 470 ° in a rapid thermal annealing (RTA) tool. The devices had ~20 nm Al_2O_3 gate dielectric deposited using plasma-enhanced ALD. The gate was deposited using 20 nm of Ni and 380 nm of Au. The first metal interconnect layer was formed in the source/drain regions using evaporated Ni/Au. The devices were then passivated with 80 nm of Al_2O_3 by plasma-enhanced ALD. The second metal interconnect layer was deposited again using evaporated Ni/Au. Finally, roughly 4 µm of Au was deposited using electroplating to form the device contacts and complete device fabrication. Figure 10 shows a schematic of the device.

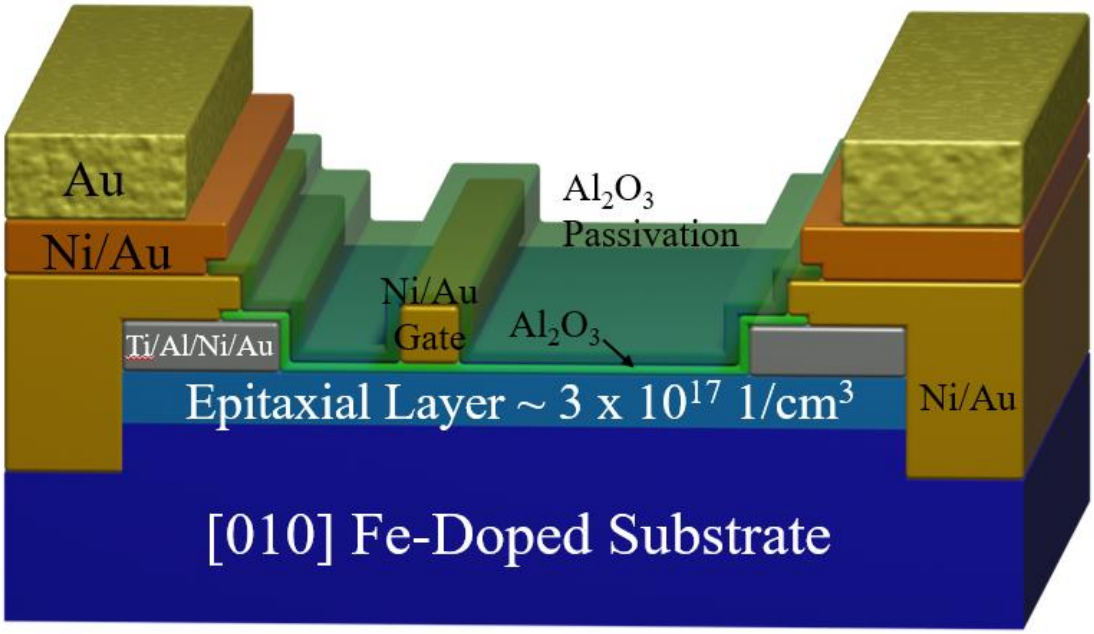

Figure 10: A schematic of the fabricated device. The gate metal is Ni/Au with Ti/Al/Ni/Au ohmic contacts and Al2O3 as the dielectric and passivation layers.

Fabricated devices were tested in air (using a box furnace that permits electrical connection capabilities using externally accessible, electromagnetically shielded wires). The device was targeted to have a source-drain spacing, L_{SD} of 7.75 µm, a source-gate, L_{SG} access region of 1.4 µm, and a ~ 0.7 µm gate length, L_G. Errors in the fabrication process such as misalignment, alignment tolerance, and development times contribute to differences in the dimensions of the device when compared to the mask vs fabricated device. Figure 11 shows an SEM image of a representative device with actual measurements after fabrication.

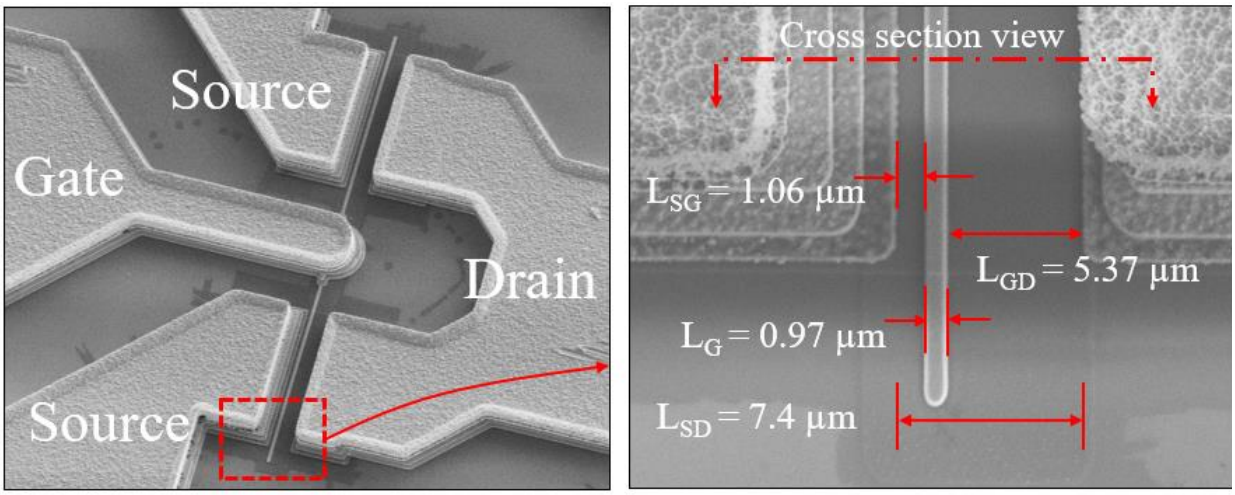

Figure 11: a) An SEM of the fabricated device. b) A close-up SEM of the gate region with measurements to show the differences between the mask versus after fabrication.

2.4. Testing Procedures

Devices in this study were tested inside a high-temperature box furnace that permits electrical connection capabilities using externally accessible, electromagnetically shielded wires. As reiterated in a previous section, the test intervals for I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics were every 100 C for the air ambient test. I_{DS}-V_{DS} sweeps consisted of sweeping the gate voltage, V_{GS} from -8 to 0 V at steps of +1 V. and sweeping V_{DS} from 0 to +5 V. I_{DS}-V_{GS} sweeps consisted of holding the drain at 0.1V and 5 V while sweeping the gate from -8 to 0 V. Figure 12 shows the representative initial I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics for the DUT. It is noteworthy that the Gm curve has a "belly" which can represent a secondary channel and is contaminated from the chemical mechanical polishing (CMP) that is performed on the topside of the wafer before epi growth [37].

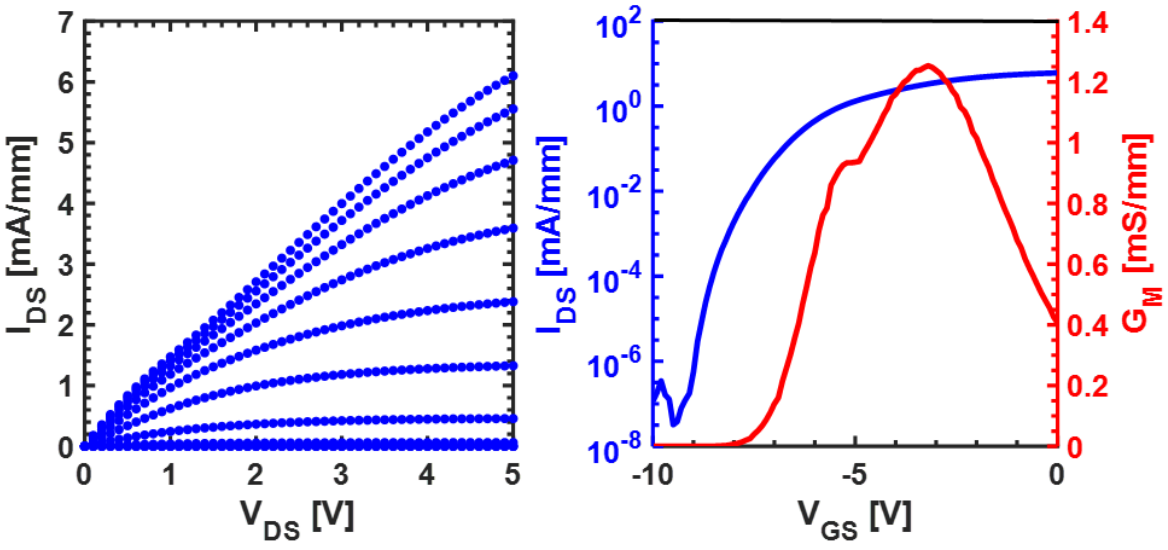

Figure 12: **a)** The initial as packaged IDS-VDS curves. **b)** The initial as packaged IDS-VGS on/off and GM curves [36].

2.5. High-Temperature Device Results

Figure 13 shows the I-V family (I_{DS}-V_{DS}) characteristics of a device measured at different temperatures from room temperature (RT) up to 500 °C.

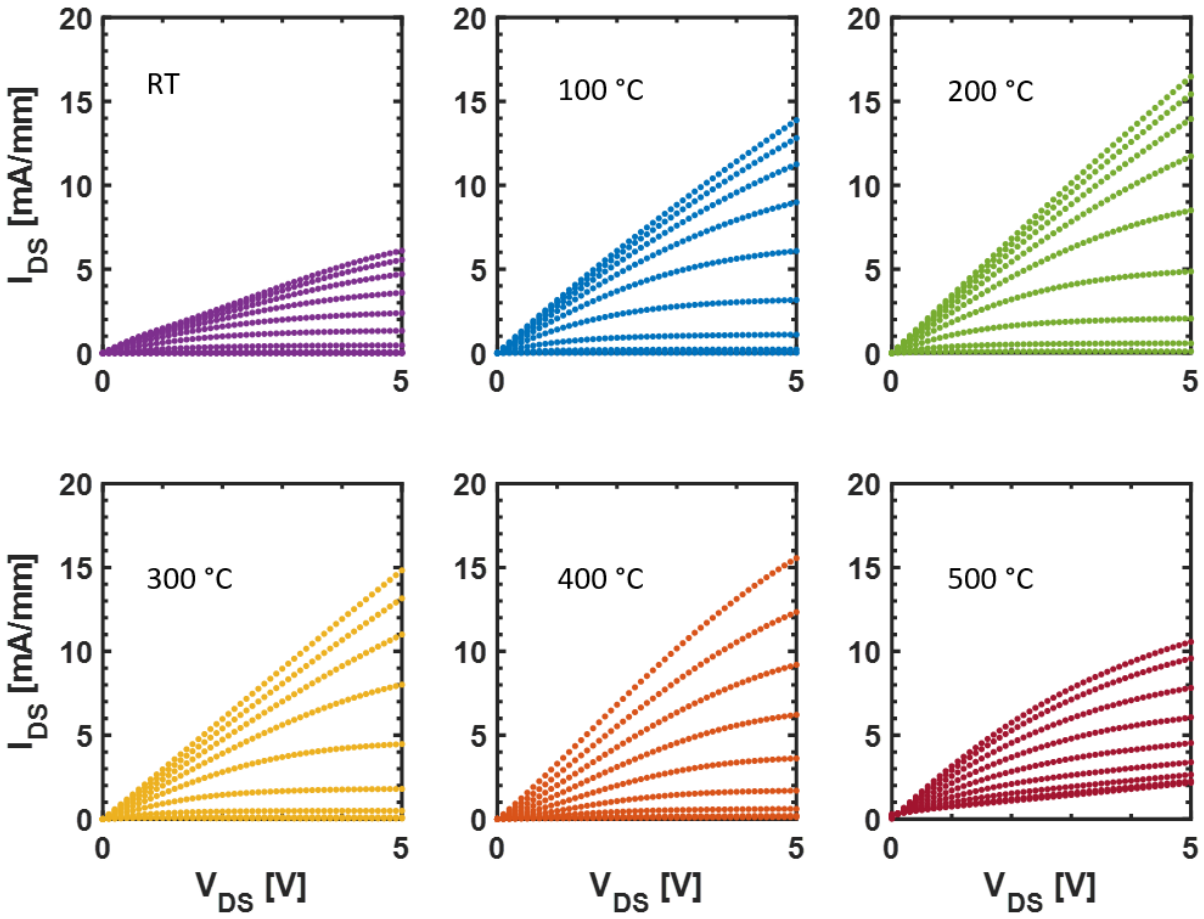

Figure 13: the respective IDS-VDS curves from room temperature (20 °C) up to 500 °C. the device are very stable up to and past 400 °C but the device is leaky in the off state at 500 °C [36].

An increase in current with temperature observed here is presumably due to activation carriers from dopants/traps in the device [23], [38]. The current increase in Ga_2O_3 as a function of temperature is interesting as in high-temperature testing of SiC shows a reduction in current as a function of temperature [39]. Using equilibrium Fermi Dirac statistics,

$$\frac{N_d^+}{N_d} = 1 - \frac{1}{1+\frac{1}{g}exp\left(\frac{E_d - E_{F,T}}{k_B T}\right)} \tag{10}$$

where E_d is the donor energy, g in the degeneracy, k_B is Boltzmann's constant in eV/K, and $E_{F,T}$ is the equilibrium Fermi energy and a particular temperature, the ratio of ionized donors can be estimated. From this, using a degeneracy of 1, it is estimated that the 30 meV donors are completely activated by 100 °C and the 120 meV unintentional donors would be completely activated by ~ 400 °C. Considering this and the observed data, the increase in current is concluded to be more likely due to the de-trapping of electrons from interface traps and defects as well as a negative push in threshold voltage, V_T as a function of temperature increasing the current density within the channel [40]. To support this, figure 14 shows the log scale transconductance as a function of temperature.

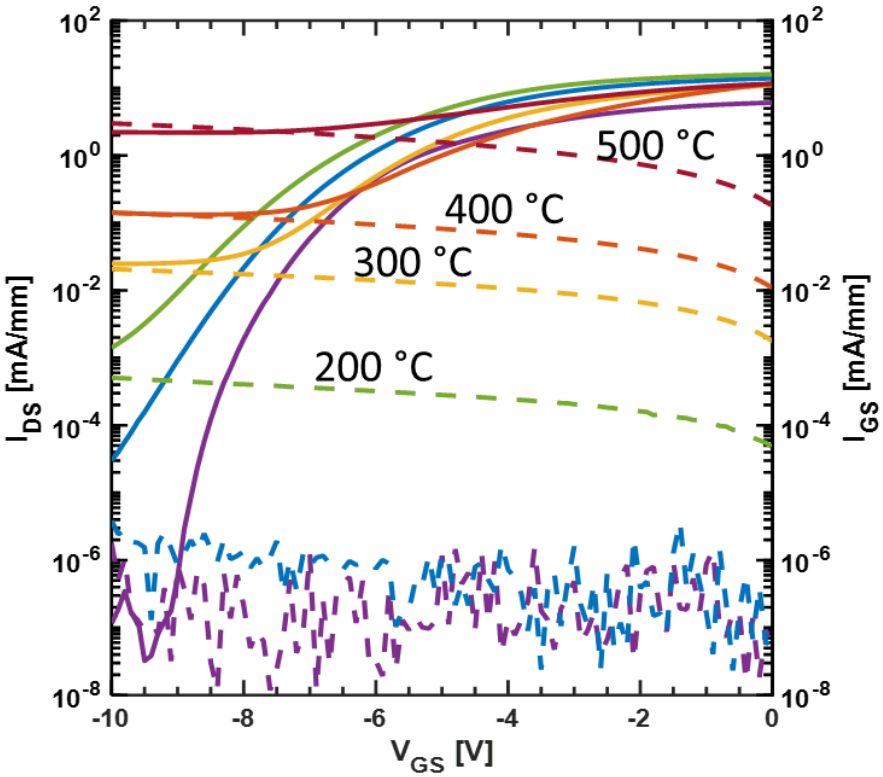

Figure 14: the log scale of the drain current, I_{DS}-V_{GS} curves (solid line) at temperatures from RT to 500 °C plotted with the gate leakage current, I_{GS}-V_{GS} (dashed line). The off-state drain current trends with the off-state gate current. RT and 100 °C are at the noise floor of the fixture [36].

It can be seen the on/off ratio of the device decreases as a function of temperature from ~ 10^7 down to ~10^1. Furthermore, figure 14 shows that the subthreshold slope decreases with increased temperature. This suggests that the field effect mobility is also decreasing as temperature increases. Coupled with this information and the conjecture can be made that the total increase of current in Ga_2O_3 is only partially due to the temperature activation of donors, but more likely due to trap/defect mechanisms [41]. Further analysis is needed to understand the source of these mechanisms.

When comparing Figures 13 and 14, it is important to notice that the device modulates at 500 °C but the device is unable to turn off and is leaky. This is due to the domination of gate current in the off-state. Figure 14 demonstrates this with the off-state gate current, I_{GS} in agreement with the transfer curve off-state. This is due to thermionic emissions over the gate [42]. Thermionic emission theory can be used to analyze the increase in gate current as a function of temperature [8]. The equation for gate current density is as follows,

$$J_G = \frac{4\pi q m^* (k_b T)^2}{h^3} exp\left[\frac{-q\left(\phi_B - \sqrt{\epsilon_{ox}/4\pi\varepsilon_{diel}}\right)}{k_b T}\right] \quad (11)$$

where q is the electron charge, m^* is the effective mass of electrons, h is Plank's constant, k_b is the Boltzmann constant, T is the temperature in Kelvin, ϕ_B is the barrier height, ϵ_{fld} is the electric field across the dielectric, and ε_{diel} is the dielectric/oxide permittivity. The unknown parameters are presented in Eq. 11, $\phi_B, \epsilon_{ox}, and\ T$. The temperature will be constant at a specific dwell point, 100 °C, 200 °C for example, ϵ_{ox} will be a function of the voltage bias applied to the gate, and ϕ_B will be a constant.

After the cycle up to 500 °C, the device returns to its normal operating state. The part was able to withstand 20 hours at 500 °C will little degradation other than a reduction in the on/off ratio and a negative push in the off-state voltage. Figure 15 shows the respective curves of the device from as packaged to after 20 hours.

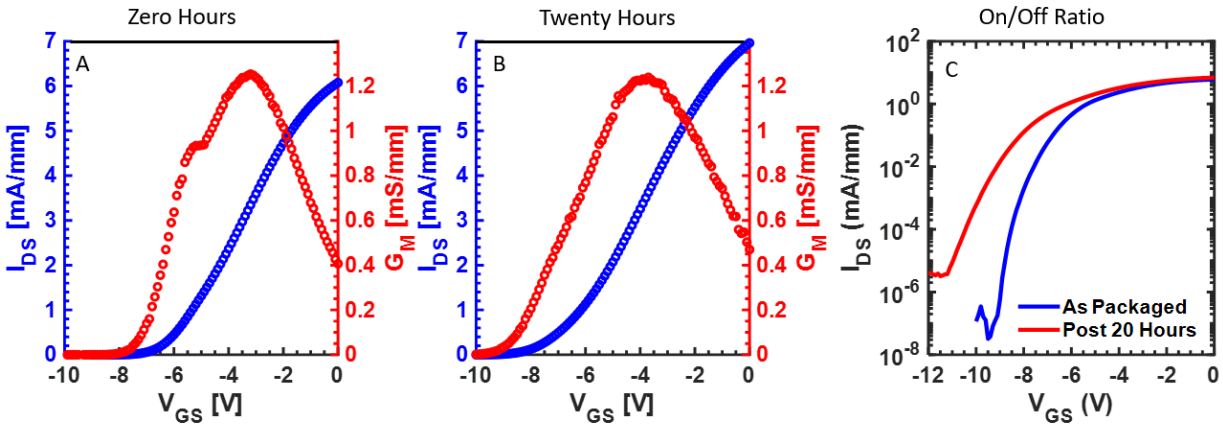

Figure 15: **a)** The transfer and GM curves taken at RT before the start of the test. **b)** The transfer and G_M curves were taken at RT after 20 hours at 500 °C. V_{off} has migrated approximately -1 V. **c)** the log scale transfer curve showing on/off ratio decreased by approximately two orders of magnitude [36].

After the DUT had been through 20 hours at 500 °C, the device was sent out for a transition electron microscopy (TEM) analysis. TEM is where a beam of electrons is transmitted through a very thin sample and can give high-resolution images of material interfaces. Figure 16 shows TEM images done on a representative unbaked device compared to the device that was tested at a high temperature for 20 hours.

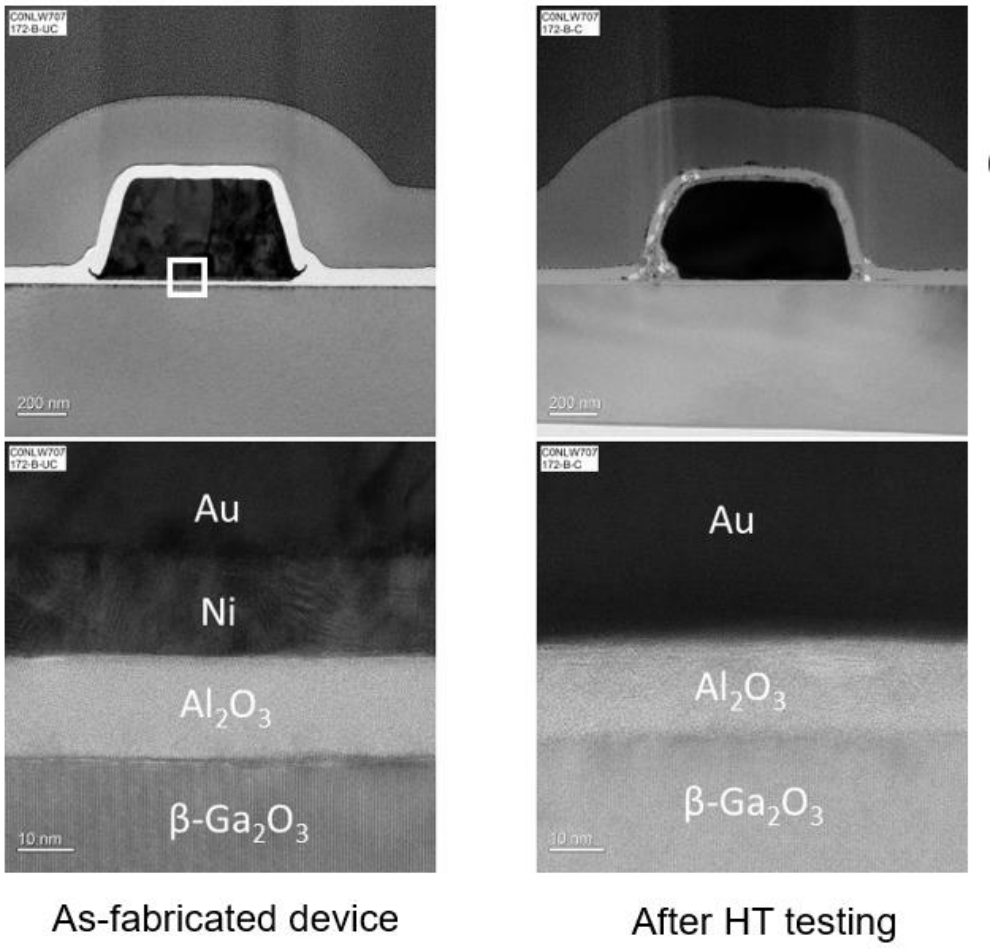

Figure 16: A TEM cross-sectional analysis of the gate. The as-fabricated metal-oxide-semiconductor (MOS) structure of the gate (left) and the gate MOS structure after 20 hours at 500 °C.

In figure 16, the Ni/Au boundary can be seen in the as-fabricated cross-section. After testing for 20 hours at 500 °C the Ni has alloyed with the Au which was expected [43]. What was not expected, was for the Ni/Au to intermingle with the Al2O3 dielectric and passivation. Figure 17 offers a close-up of the gate cross-section after the 20-hour test highlighting the damage to the dielectric and passivation layer due to diffusion and intermixing.

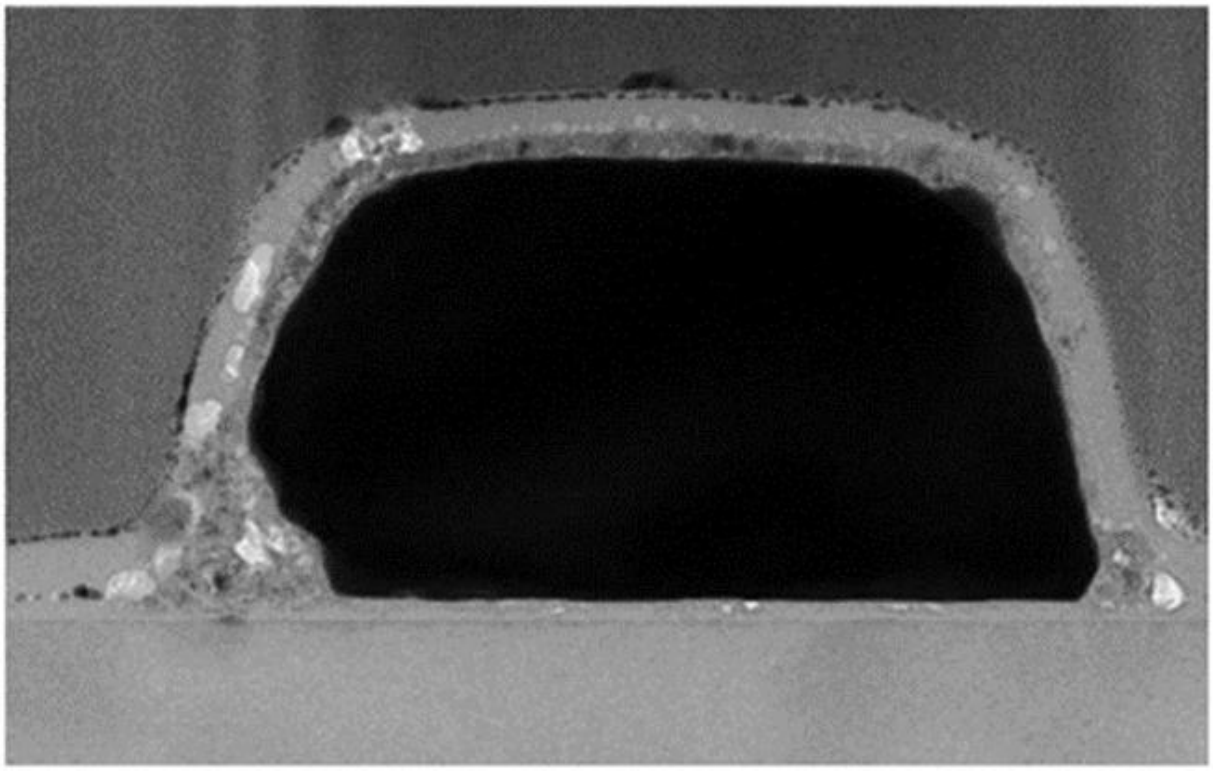

Figure 17: A cross-section of the gate after 20 hours at 500 °C highlighting the intermixing of the Ni/Au gate metal with the Al_2O_3 passivation and dielectric layers.

Considering the damage to the dielectric and passivation layers, it can be concluded that Ni/Au may not be the best choice for a long-term high-temperature device. An experiment into MOS structures will need to be performed to down-select choices for high-temperature gates. Once the choices have been selected, the device will need to be fabricated and tested at high temperatures.

Chapter 3. Modeling the Electrical Characteristics of MOSFETs

3.1. Material Constants and COMSOL Parameters

The first step to creating a model within COMSOL Multiphysics is to find the intrinsic material properties for β-Ga_2O_3. The COMSOL material library does not have β-Ga_2O_3 properties in the database, so a new material profile had to be created. Table 2 shows a list of the required material parameters needed to satisfy the equations within the solvers.

Table 2: All material constant and device dimensions are summarized.

COMSOL Semiconductor Module Parameter Inputs			
Property	**Variable**	**Value**	**Unit**
Band Gap	E_g	4.82	eV
Electron Affinity	χ_0	4	eV
Effective Density of States, Conduction Band	N_C	3.7034×10^{18}	$1/cm^3$
Effective Density of States, Valence Band	N_V	6.2897×10^{21}	$1/cm^3$
Electron Mobility	μ_n	0.00751	$m^2/V \cdot s$
Hole Mobility	μ_p	1×10^{-6} [44]	$m^2/V \cdot s$
Contact Resistivity	ρ_C	7.98×10^{-8}	$\Omega \cdot m^2$
Relative Permittivity, Ga_2O_3	ε_s	10	1
Relative Permittivity, Al_2O_3	ε_{ins}	8	1
Metal Work Function, Ni	ϕ_m	5.1	eV
Oxide thickness, Al_2O_3	d_{ins}	20	nm
Epitaxial Layer Thickness	d_{epi}	65	nm

Epitaxial Doping Density	N_d	3.1034×10^{17}	$1/cm^3$
Device Out of Plane Width	d_z	100	μm

The effective density of states for the conduction and valence band were calculated empirically using Eq. 6. Electron mobility, μ_n, and epitaxial doping density, N, all are obtained experimentally by taking hall measurements on the sample. Each reticle includes a Van der Pauw structure for taking these measurements across the wafer. Figure 18 shows the Van der Pauw structure and a sample of the data from the Hall measurements on different reticles.

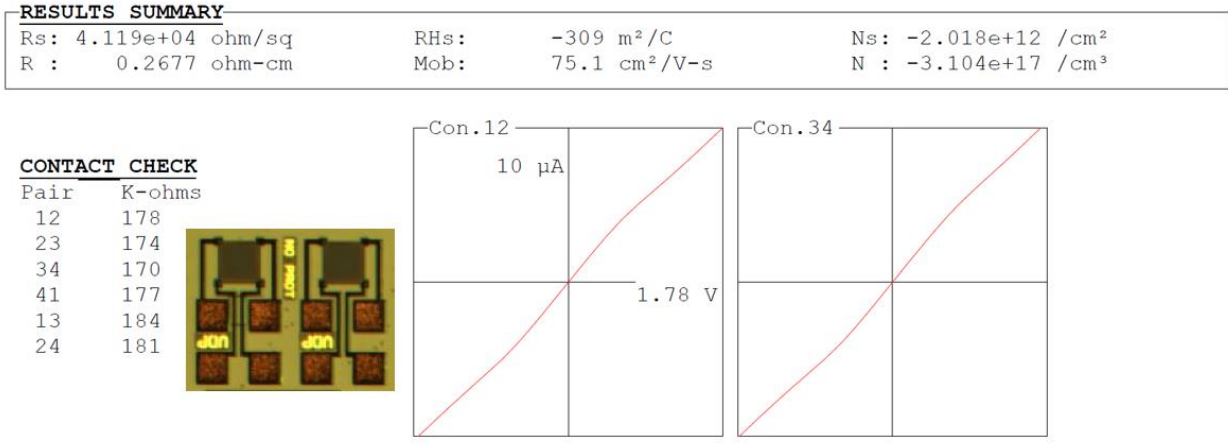

Figure 18: An Image of the hall measurement data with a small image of the Van der Pauw structure used to collect the data.

As concluded before, the valence band of β-Ga2O3 is very flat and the holes are very deep within the band gap [22], [44]. Considering this, hole mobility, μ_p is negligible and a very small number is entered into this parameter.

The relative permittivity, ε_{ins} of the Al_2O_3 deposited by plasma-enhance ALD is estimated through CV measurements [45]. The thickness, d_{ins} of the deposited Al_2O_3 is measured by an ellipsometer.

The Epitaxial thickness, d_{epi} is measured through secondary ion mass spectrometry (SIMS) and the doping density is measured from Hall measurement techniques. The gate metal work function can be found in literature and tables [46]. The contact resistivity, ρ_C must be calculated experimentally. The equation used to calculate contact resistivity is,

$$\rho_c = R_c L_T W_C \, [\Omega \cdot m^2] \tag{12}$$

where R_C is the contact resistance, L_T in the transfer length, and W_C is the TLM contact width. These parameters are found using the four-probe or van der Pauw method [47]. Transfer length method (TLM) test structures are created during the lithography process along with the transistors. TLMs are defined by a mesa etch and six ohmic pads spaced laterally apart in six different spacings from 5 to 30 µm. With four probes, two for current and two for voltage, 1 mA of current is pushed through each gap spacing and the voltage drop is measured. From the relationship, $V = IR$, the resistance of each gap is plotted. Figure 19a shows a typical TLM testing structure and figure 19b shows a plot of the resistance as a function of gap spacing.

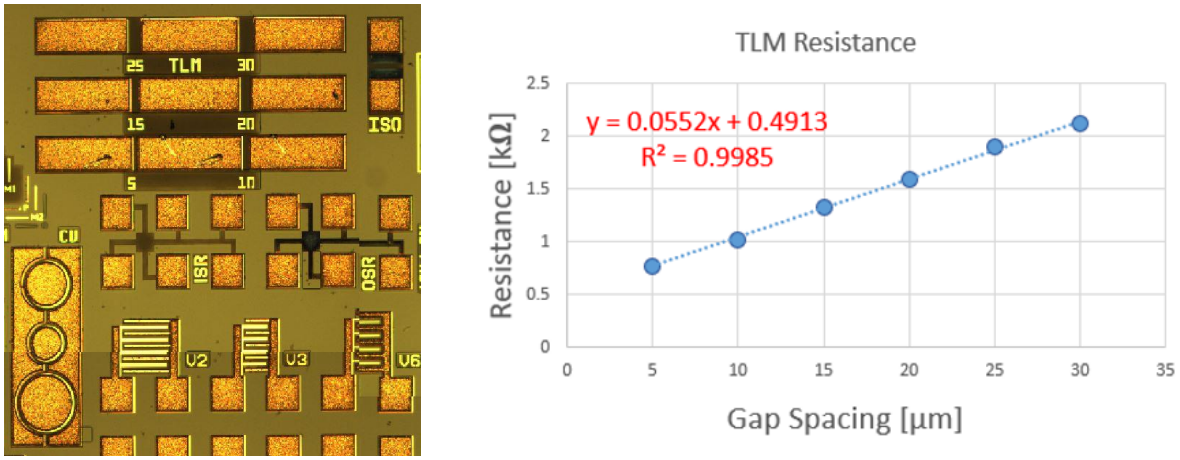

Figure 19: a) An image of TLM structures with spacings of 5 µm to 30 µm. **b**) A plot of the measured resistance as a function of the gap spacing. A linear fit is generated with an R^2 value. An R^2 value of 0.999 is desirable however, the measurement is highly dependent on geometry, and artifacts from the lithography process can influence the measurement.

A linear fit is applied to the data and outlying points are removed to achieve an R2 value of 0.99.

From this linear fit, we have the equation,

$$R[k\Omega] = 0.0552\,\frac{k\Omega}{\mu m} * L[\mu m] + 0.4913 k\Omega \tag{13}$$

If we set $L = 0$, the y-intercept will be equivalent to $2R_C$. Therefore, to calculate the contact resistance, the equation at $L = 0$ becomes,

$$R_c = \frac{0.4913}{2} = 2.457\ k\Omega \tag{14}$$

The transfer length, L_T is the length from the edge of the contact pad inward to which current flows. Current flow drops logarithmically from the leading edge of the contact to no current flow on the opposite edge. This effect is known as current crowding [47]. If the linear fit is extrapolated to where the line crosses the x-axis, the x-intercept will be equivalent to $-2L_T$. From this, the transfer length can be calculated by,

$$L_T = \frac{0.4913\ k\Omega}{2\left(0.0552 {}^{k\Omega}/_{\mu m}\right)} = 4.4502\ \mu m \left(\frac{1\times10^{-6} m}{1\ \mu m}\right) = 4.45 \times 10^{-6}\ m \tag{15}$$

Now that all the unknowns are solved and $W_C = 0.73 \times 10^{-4} m$, the contact resistivity, ρ_C can be solved using equation (6),

$$\rho_C = (0.2.457\ k\Omega)(4.45 \times 10^{-6} m)(0.73 \times 10^{-4} m)\left(\frac{1000\ \Omega}{k\Omega}\right) = 7.98 \times 10^{-8} \Omega \cdot m^2 \tag{16}$$

TLM testing is typically done by an automated testing system called PCM (Process Control Monitor) as it is very time-consuming to probe the TLM structures manually. The PCM is a series of test structures, i.e., TLM, Van Der Pauw, on each reticle to verify that the wafer being processed

is viable throughout the fabrication process. This ensures that the fabrication engineer does not spend a whole month or so processing a wafer that will not yield viable devices. The PCM system has special probes with six tips and can measure three TLM spacings at once. The system will take the measurements at each TLM structure and then step to the next reticle. Figure 20 shows a wafer plot of the contact and sheet resistance and how it can vary across the wafer. The sheet resistance is the slope of the line from equation (13) multiplied by the contact with, W_c.

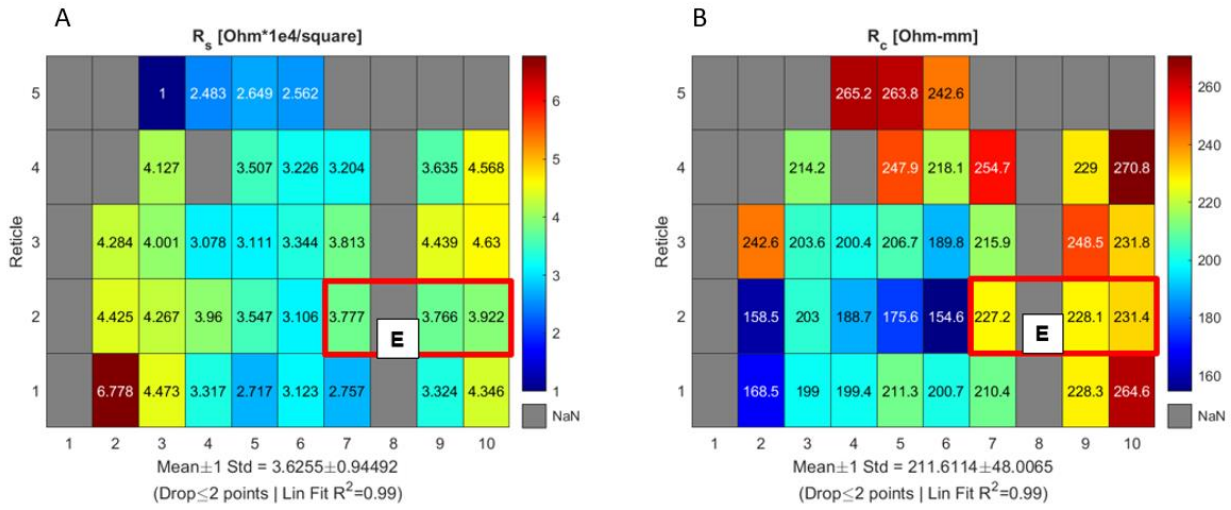

Figure 20: a) a wafer map of the sheet resistance of each reticle taken from the PCM structure **b)** A wafer map of the contact resistance of each reticle.

Now that all the parameters are known, the next step in creating the model is to define the device geometry.

3.2. Model Geometry and Assumptions

The general approach to creating a model of the device was to simplify it as much as possible since the main goal of the study was to look at channel temperatures inside the device. This means that only the epi-layer and mesa portion of the substrate will be looked at in the study. From the process

followers, the devices were built on a 65 nm epi-layer on a ~ 500 µm thick substrate. The mesa etch creates a total mesa height of 400 nm. Measured from the mask layouts, the source contact length, L_S is 22.25 µm, the drain contact length is $L_D$is 18 µm. The device being modeled has optical gates with a length, L_G of 0.7 µm. The source to drain length, L_{SD} of the device is 7.75 µm with a source-to-gate length, L_{SG} of 1.4 µm and a gate to drain length, L_{GD} of 7.05 µm. Since the device being modeled is a 2x50 µm device, the width of the gate, W_g is set to 100 µm. Figure 21a shows a sample of the CAD file with the mesa, ohmic, and gate layers active with dimensions. Figure 21b shows a cartoon with the dimensions of the modeled 2D device as modeled in COMSOL.

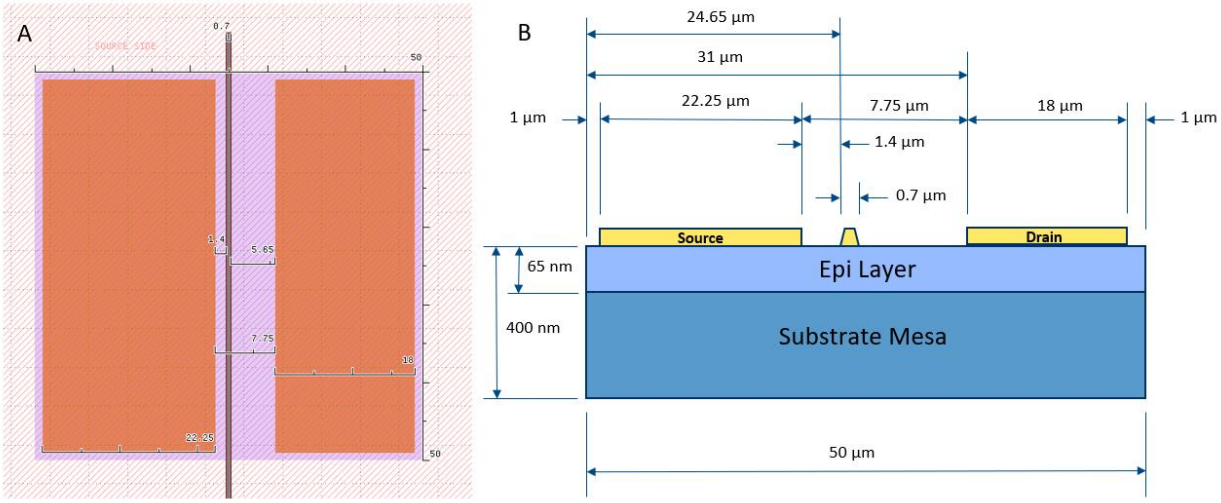

Figure 21: a) A CAD image of the mesa, ohmic, and gate masks with the respective dimension. **b)** A side illustration of the geometry of the model in COMSOL with dimensions.

To simplify the model, the interface between the epi-layer and the ohmic contacts are assumed to be an ideal ohmic boundary condition which assigns a local thermodynamic equilibrium at the contact [48]. This means that the hole and electron quasi-fermi levels are equal at the boundary. The contact resistivity, ρ_c is also applied in the ohmic metal contact assumption. For the gate, a

thin insulated gate assumption is chosen. This assumption requires a gate metal work function, Φ_m, insulator thickness,d_{ins} and oxide relative permittivity, ε_{ins}. For the epitaxial layer, an analytic doping model is applied along with the semiconductor material model properties. The semiconductor material properties and parameters will be discussed in the previous section. The analytic doping model requires a donor carrier density, N_d and requires the choice of complete or incomplete donor ionization. In this model, incomplete ionization is selected. Incomplete ionization requires a donor energy level below the conduction level which is 30 meV from the literature [23]. The Mesa has the semiconductor material model parameters applied to it, however, since the substrate is semi-insulating, the mobility of the electrons, μ_n is set to a small number, 1e-6.

3.3. Governing Equations

In COMSOL, the governing equations are organized in two ways. The equation either governs a domain or a boundary condition. For a domain condition, it is applied to an enclosed area or solid. The equation will usually have a gradient or divergence operator to denote the x, y, and z directions. Since the simulation is a 2D model, $\frac{\partial}{\partial z} = 0$, and the z direction is a constant multiple, which is the gate width or out-of-plane width, d_z in this case. Boundary conditions are applied to a specific boundary of the system and represent the in and out of the continuity of the system. Table 3 list the governing equations used with COMSOL and how they are applied to the system.

Table 3: The governing equations used in COMSOL with their respective boundary or domain conditions.

Equations Used in the COMSOL Electrostatic Model		
Equation	**Boundary/Domain Condition**	**#**
$\boldsymbol{\nabla \cdot (-\varepsilon_0 \varepsilon_r \nabla V) = \rho}$	**Semiconductor Domain**	**17**

$\rho^+ = q(p - n + N_d^+ - N_a^+)$	**Semiconductor Material Domain**	**18**
$\nabla \cdot J_n = 0$	**Semiconductor Material Domain**	**19**
$J_n = qn\mu_n \nabla E_c + qD_n \nabla n - qnD_n ln(N_c) + qnD_{n,th} \nabla ln(T)$	**Semiconductor Material Domain**	**20**
$D_n = \mu_n k_b T G(n/N_c)$	**Semiconductor Material Domain**	**21**
$E_c = -(V + \chi_0)$	**Semiconductor Material Domain**	**22**
$E_v = -(V + \chi_0 + E_g)$	**Semiconductor Material Domain**	**23**
$n - J_n = 0, \quad n \cdot D = 0$	**Insulator Boundary**	**24**
$V = V_{eq} + V_0 + \rho_c n \cdot J$	**Source, Drain, and Base Contact Boundary**	**25**
$n = \frac{1}{2}(N_d^+ - N_a^-) + \frac{1}{2}\sqrt{(N_d^+ - N_a^-)^2 + 4\gamma_n \gamma_p n_{i,eff}^2}$	**Source, Drain, and Base Contact Boundary**	**26**
$n \cdot D = \frac{\varepsilon_{ins}\varepsilon_0}{d_{ind}}(V + \phi - V_0 + V_{eq})$	**Thin Insulator Gate Boundary**	**27**
$n \cdot J_n = 0$	**Thin Insulator Gate Boundary**	**28**
$N_d = N_d^{prev} + N_{d0}$	**Analytic Doping Domain**	**29**
$n \cdot (D_1 - D_2) = \rho_s$	**Surface Charge Density, Boundary**	**30**

Equations (17) and (18) when set equal, make up Poisson's equation for electrostatics. Equation (19) is the continuity equation. Equation (20) is the current density equation for free electrons in the system whereas equation (21) is the electron diffusivity coefficient and Einstein's relationship which includes a generation term, G. $D_{n,th}$is the thermal electron diffusivity coefficient. Equation (22) and (23) defines the conduction and valence band relative to the applied voltage. Equation (24) is applied to any boundary that is not a contact, gate, or heterojunction. Equation (25) is the potential of the contact where V_{eq} is the voltage at which the vacuum level is constant and V_0 is the applied potential. Equation (26) is the carrier concentration at the contact. Equation (27) describes

the electrical displacement at the gate while equation (28) established continuity about the gate boundary. Equation (29) describes the activated doping concentrations of the doping model and equation (30) establishes the surface charge density at the gate interface. Figure 22 shows the geometry of the model in COMSOL with the boundary conditions highlighted and representative equation number.

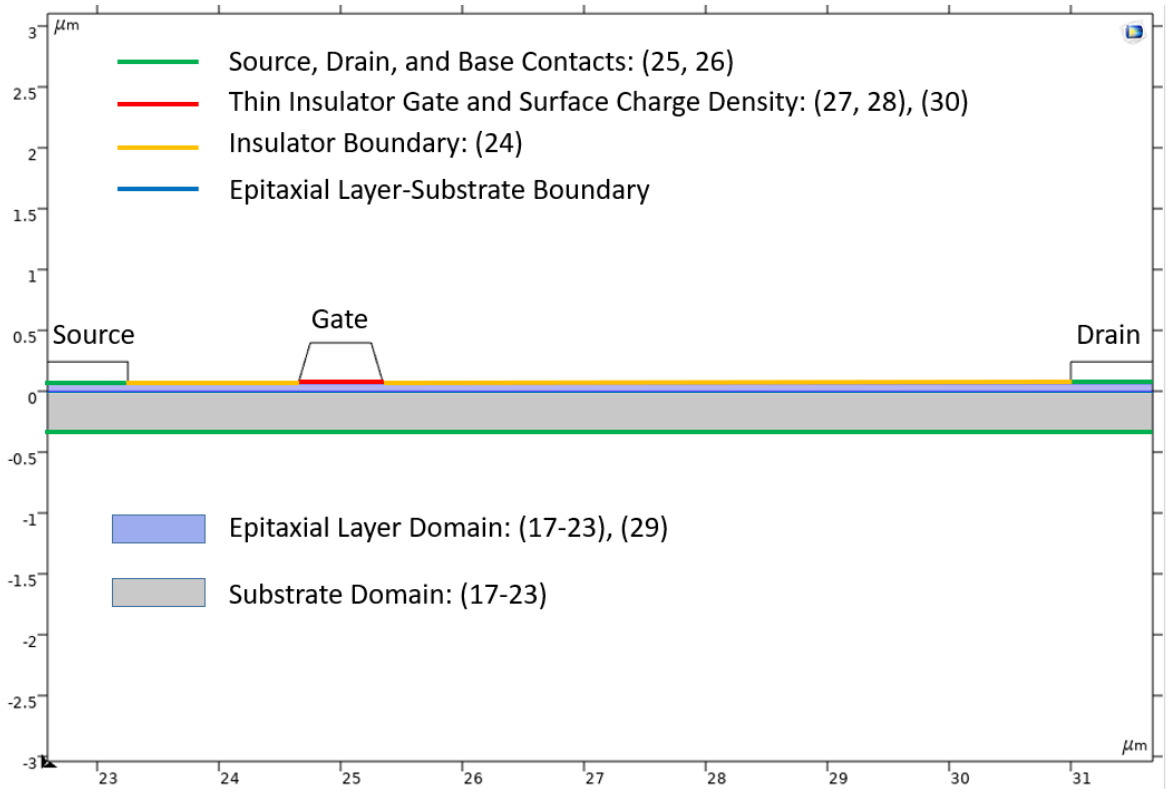

Figure 22: The model geometry in COMSOL with the boundary conditions highlighted with respective governing equation numbers.

3.4. Initial Model Results and Challenges

To model the electrostatics of a representative device, a device from the original fabricated data was chosen. As stated before, the device periphery was selected to be a 2x50 μm device. Figure

23a shows the Id-Vg data from the wafer and Figure 23b shows the representative device's experimental data.

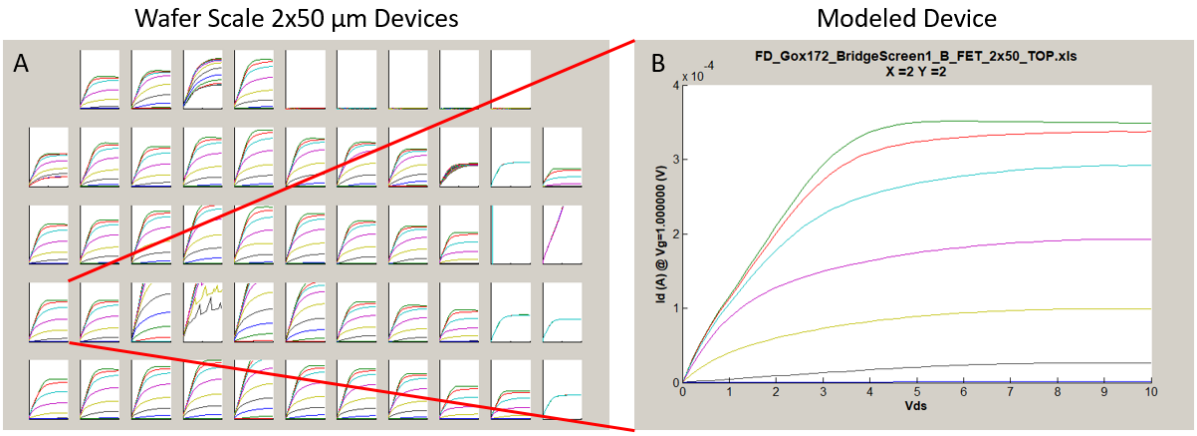

Figure 23: a) A wafer-scale plot of the 2x50 µm devices. **b)** The I-V data of the selected device to be modeled.

To keep the simulation like the experiment, the same test parameters were chosen for the simulation. As can be seen in Figure 23b, the test is sweeping the drain voltage from 0 to 10 V while stepping the gate bias from +1 V to -5 V, at –1 V per sweep. The device is fully off at –5 V on the gate with the off-state voltage (V_{off}) being somewhere between –4 and –5 V on the gate. The off-state voltage can be described as the gate voltage where there is minimal conduction between the source and the drain. If $Vg > V_{off}$, then the device will be in the on-state in a depletion mode device, whereas if $Vg < V_{off}$, then the device will be in the off-state. The initial simulation did not turn out as expected. While the max drain voltage was within a reasonable range, the simulated device was off when –1 V was applied to the drain. When simulations are run in COMSOL where the numbers are very small, the simulations tend to have convergence issues. Figure 24 shows the comparison of the simulated current at gates voltages of +1, 0, and –1 V. The

simulated device is off at –1 V on the gate so the off-state voltage is somewhere between 0 and –1 V.

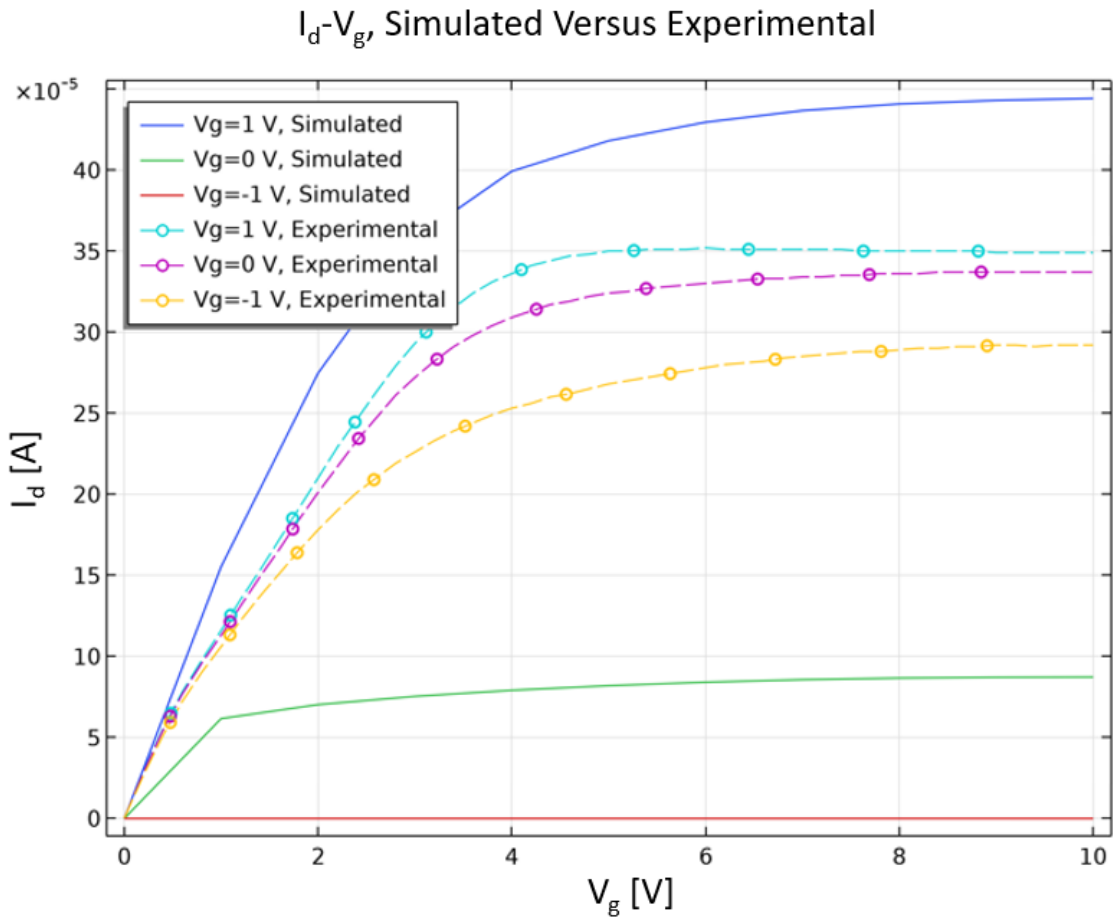

Figure 24: I-V curves of the simulated versus experiment data at 1, 0, and -1 V. The simulation is in the off state at -1 V on the gate where the experiment data is not.

The off-state voltage, V_{off} can be calculated with the equation,

$$V_{off} = V_{FB} - dqN_d\left(\frac{d}{2\varepsilon_s} + \frac{1}{C_{ox}}\right) \tag{31}$$

Where V_{off} is the flat-band voltage, d is the channel thickness, in this case, we will consider the thickness of the epitaxial layer, q is the charge of an electron, N_d is the doping density, ε_s is the relative permittivity of the semiconductor, and $C_{ox}$is the oxide capacitance per unit area.

V_{FB} is the flat-band voltage. The flat-band voltage is the applied voltage where there is no band bending across the gate metal-oxide-semiconductor (MOS) structure. The flat-band voltage is like the built-in voltage of a p/n junction [8]. Figure 25 shows the band diagram of the MOS structure at a gate bias and flat-band condition.

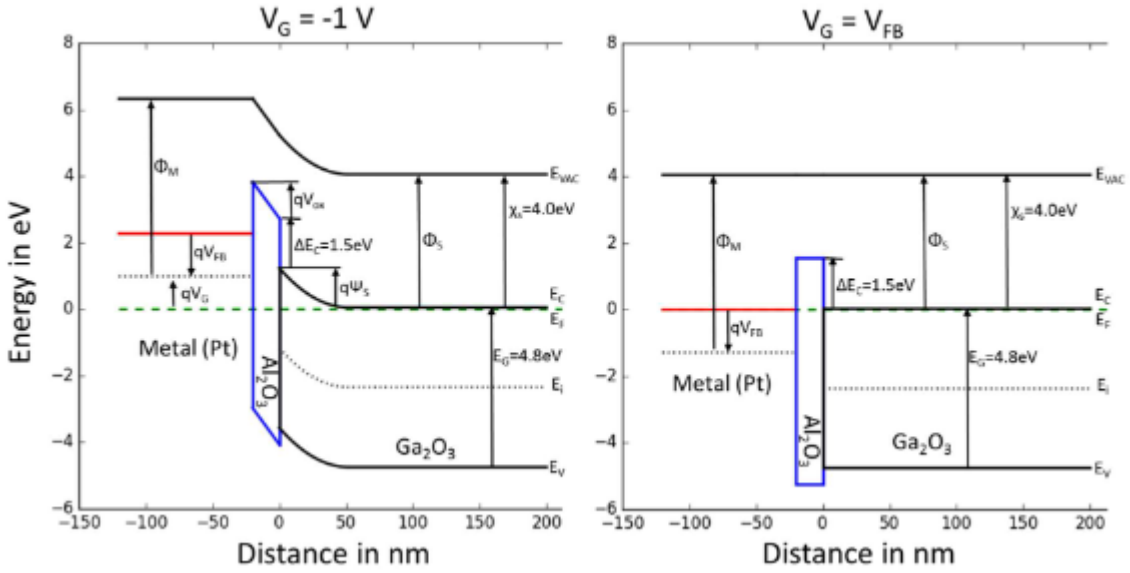

Figure 25: Example band diagrams of a MOS structure where the gate bias is at -1 V and when the gate voltage is equal to the flat band voltage. When V_G is equal to V_{FB}, there is no band bending in the diagram and the vacuum and fermi levels are constant [24].

To calculate the flat-band voltage, V_{FB}, the following equation is used,

$$V_{FB} = \phi_m - \left[\chi_s + \frac{k_b T}{q} ln\left(\frac{N_d}{N_c}\right)\right] \tag{32}$$

Where ϕ_m is the metal work function, χ_s is the electron affinity of the semiconductor, k_b is the Boltzmann constant, T is the temperature in Kelvin, N_d is the doping density, and N_c is the

effective density of states of the conduction band. N_c can be calculated using equation (6). The oxide capacitance is found using the equation,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\kappa_{ox}\varepsilon_0}{t_{ox}} \tag{33}$$

Equation (33) shows that the oxide capacitance is the relative permittivity of the oxide, ε_{ox} over the thickness of the oxide, t_{ox}. It goes on to show that the relative permittivity of a material is the material's dielectric constant, κ, multiplied by the permittivity of free space, ε_0. When the calculation is performed in MATLAB, the off-state voltage is determined to be –0.90 V. This coincides with the electrostatic determinations calculated using a device design workbook [49]. Figure 26 shows the calculated V_{off} from the spreadsheet.

phi,B	**2.35**	**V**	
phi,S	**4.05**	**V**	semiconductor work function
Vfb	**1.05**	**V**	ideal flatband voltage
Cox	**4.43E-03**	**F/m2**	oxide capacitance per unit area
phi,it = Qit/Cox	**0.00**	**V**	built-in voltage from Qit
V,flatband, w/Qit	**1.05**	**V**	non-ideal flatband (w/Qit)
V,off, term2	0.73	V	variable
V,off,term3	1.19	V	variable
V,off, ideal	**-0.87**	**V**	ideal off-state voltage
V,off, w/Qit	**-0.87**	**V**	non-ideal off-state voltage (w/Qit)
V,off, w/ Qti & Backside Vbi	**-0.30**	**V**	non-ideal off-state voltage (w/Qit + backside)

Figure 26: An image of the results from the excel spreadsheet calculations where the off-state voltage calculated is consistent with MATLAB calculations from data.

From equation (32) and equation (33), V_{off} is a function of channel thickness, doping, and oxide thickness. Since in the model, these are fixed values due to experimental data and geometry, it is unclear what factors are causing the significant difference in V_{off} between the experimental data and the electrostatic model.

3.5. Final Model Results

The method to drive the off voltage, V_{off} more negative was not clear. Changing the geometry would change the off voltage, such as increasing the thickness of the epi layer. For obvious reasons, this is not a practical approach as the thickness of the epi layer cannot be changed on the actual device. The ability to add contact resistivity, which was added to COMSOL with the 6.0 update, corrected the slope of the I-V family of curves to match the experimental data. The factor that allowed for better curve matching to the experimental data was adding a boundary condition under the gate called surface charge density, ρ_s. Figure 27 shows the boundary selected to apply the condition.

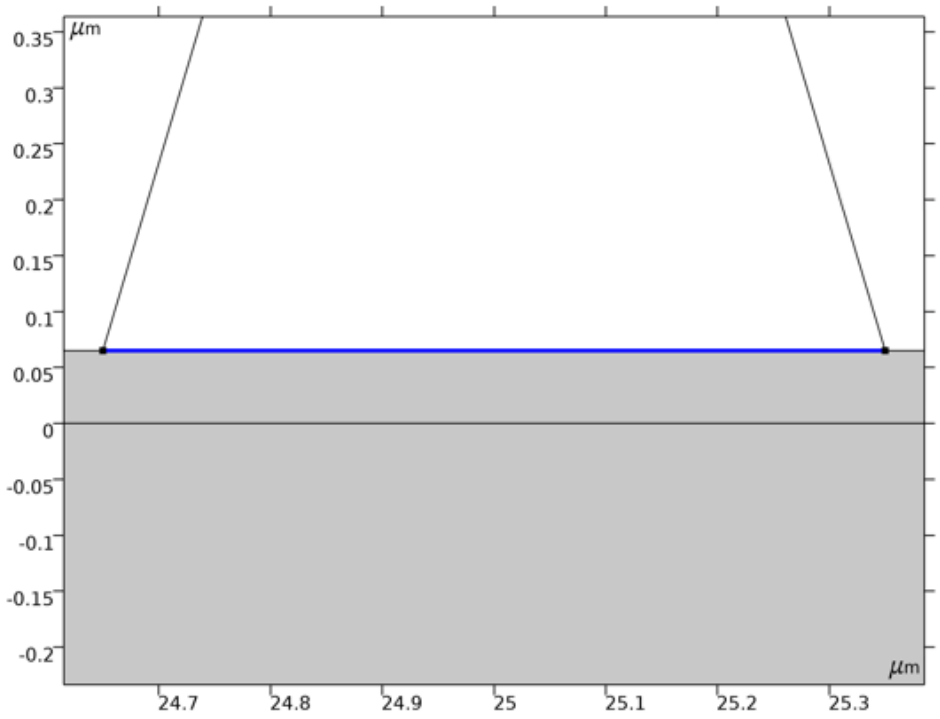

Figure 27: An image of the boundary selection for the surface charge density boundary condition applied under the gate.

The values for surface charge density came from the hall measurement data like the data seen in figure 18. The data is labeled RHs, which is the Hall sheet charge coefficient, it is the inverse of sheet charge density, ρ_s. To get the surface charge density, the inverse of the RHs from hall measurements is used, this is in the correct units of C/m^2. To curve match the experimental data, the value for surface charge density had to increase for each gate voltage step. Table 4 shows the values of sheet charge density used compared to the gate voltage step.

Table 4: The gate voltage, V_G compared to the surface charge density, ρ_s

V_G	ρ_s
0 V	4.0×10^{-3} C/m^2
-1 V	7.05×10^{-3} C/m^2
-2 V	9.2×10^{-3} C/m^2
-3 V	10.9×10^{-3} C/m^2

From Table 4, the surface charge density had to be increased for each gate voltage step. For Vg = -4 V, a value for surface charge density that would allow for iteration convergence was not able to be established. Figure 28 shows the results of the electrostatic model compared to the experimental data. Note that the linear and saturation region of the Vg = 0 V curves are similar while, as the gate voltage decreases, the linear to saturation regions vary more. The linear region of the simulation stays consistent as the gate voltage decreases whereas the experimental data does not. This phenomenon is presumably due to the change in the on-resistance, R_{ON} as a function of the gate bias. In the experimental data, R_{ON} is changing with Vg, whereas in the simulation, R_{ON} stays constant with Vg.

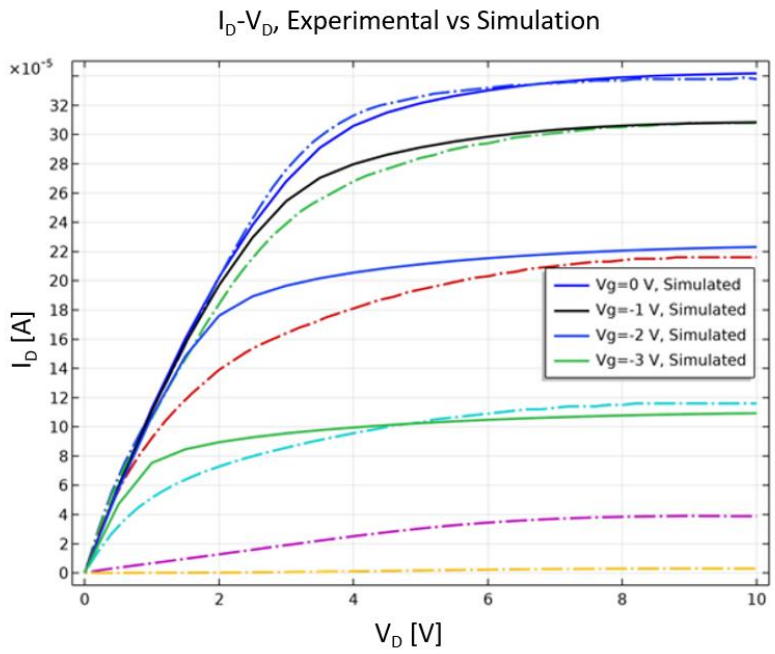

Figure 28: The simulated versus experimental data after the surface charge density boundary condition was added. Each gate voltage step had to be a new study with the value of the surface charge density increases for each gate voltage. As the gate voltage step becomes more negative, the behavior of the experimental curve is more difficult to match.

Chapter 4, Conclusion and Future Work

4.1. Conclusion

Gallium Oxide has shown great potential for Power switching and high-temperature devices. This was reinforced within this thesis with FOM comparison charts and the intrinsic properties of the material. The study also reiterated the need for high-temperature electronics within industrial and defense applications and how gallium oxide may find a fit. This study has shown that Ga_2O_3 transistors can be viable for high-temperature operation. The main issue with testing devices at high temperatures is designing a fixture that can adequately withstand the elevated temperatures and oxidation effects. New packaging that could withstand the heat had to be created to connect the devices electrically. Having a fixture to test gallium oxide devices at high temperature, several tests were performed. The devices have shown stability up to greater than 400 °C with the devices still modulating at 500 °C. Thermionic emission over the metal-oxide-semiconductor barrier as gate leakage is the dominant failure mechanism. The device however returns to normal operation mode without much degradation after the 500 °C dwells. Design for high-temperature devices will come down to material selection for gate and interconnect metals as well as oxide choices. An electrostatic model of the tested device was created in COMSOL to understand the physics involved in semiconductor devices. In creating the model, the device parameters had to be found to enter them into COMSOL. Some of these parameters were found in the literature and calculated empirically. Some of the parameters were found experimentally before and during the fabrication process. The initial model did not reflect the actual device and the experimental mechanisms for device variance were not clear. The use of an interface charge density boundary condition under the gate fixed the model. The interface charge density was increased as the gate voltage bias decreased and allowed the model to curve match the actual data

4.2. Future Work

For testing electronics at high temperature, the fixture could use a few updates. Reducing the number of connections within the furnace will make setup easier and the testing cleaner. On occasion, the connections can loosen and cause the test to reveal false data. This is predominated in the RTD connection as any added resistance will cause the temperature reading to change. A new multimeter/data acquisition controller (DAQ) will be added to take control of the temperature monitoring. This DAQ unit has a built-in Wheatstone bridge and cold junction. These will allow the addition of thermocouple temperature measurements in conjunction with the RTD.

A new coaxial cable designed for high-temperature applications will be added to the system. these cables should help with noise reduction and prevent inductive coupling [50]. A new wider package design will help to reduce inductive coupling as well. The current package is 1 inch wide and more space is needed between the rocker arms.

To design electronic devices for high-temperature operation, a study into gate metal stacks and their stability for long periods at high temperatures should be performed to find an optimal metal stack. Currently only Ni/Au and W/Cr have been tested with only Ni/Au surviving for more than 1 hour at 500 °C. A study of gate dielectrics for high temperatures also needs to be performed. Al_2O_3 is currently the only gate dielectric that has been studied in high-temperature gallium oxide devices. Other oxides such as SiO_2 and HfO_2 may prove to be better choices for high-temperature devices.

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