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CMOS WIDE TUNING GILBERT MIXER WITH CONTROLLABLE IF BANDWIDTH IN UPCOMING RF FRONT END FOR MULTI-BAND MULTI-STANDARD APPLICATIONS

A dissertation submitted in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

By

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2022

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04/27/2022

I HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER MY SUPERVISION BY Jianfeng Ren ENTITLED CMOS Wide Tuning Gilbert Mixer with Controllable IF Bandwidth in Upcoming RF Front End for Multi-Band Multi-Standard Applications BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF Doctor of Philosophy.

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ABSTRACT

Ren, Jianfeng. Ph.D., Department of Electrical Engineering, Wright State University, 2022. "CMOS Wide Tuning Gilbert Mixer with Controllable IF Bandwidth in Upcoming RF Front End for Multi-Band Multi-Standard Applications"

The current global system for mobile communications, wireless local area, Bluetooth, and ultra-wideband demands a multi-band/multi-standard RF front end that can access all the available bandwidth specifications. Trade-offs occur between power consumption, noise figure, and linearity in CMOS Gilbert mixer wide tuning designs. Besides, it is preferable to have a constant IF bandwidth for different gain settings as the bandwidth varies with the load impedance when an RF receiver is tuned to a higher frequency. My dissertation consists of three parts. First, a tunable constant IF bandwidth Gilbert mixer is introduced for multi-band standard wireless applications such as 802.11 a/b/g WLAN and 802.16a WMAN, followed by a design synthesis approach to optimize the mixer to meet the design center frequency range, constant IF bandwidth, and power. A synthesized Gilbert mixer with effective prototype inductors, designed in 180 nm CMOS process, is presented in this dissertation with the tunability of 200 MHz IF, a constant IF bandwidth of 50 MHz, a conversion gain of 13.75 dB, a noise figure of 2.9dB, 1-dB compression point of -15.19 dBm, IIP3 of -5.8 dBm, and a power of 9 mW. Next, mixer inductor loss and equivalent electronic circuit analysis are presented

to optimize the approach to offset center frequency and bandwidth inaccuracy due to the inductance loss between the actual and ideal prototype inductor. The proposed tunable Gilbert mixer simulations present a tunable IF of 177.8 MHz, an IF bandwidth of 87.57 MHz, a conversion gain of 7.4 dB, a noise figure of 3.14 dB, 1-dB compression point of -17.1 dBm, and IIP3 of -19.8 dBm. Last, a CMOS integrated wide frequency span CMOS low noise amplifier is integrated with the tunable Gilbert mixer to achieve a 27.68 dB conversion gain, a 3.47 dB low noise figure, -14.6 dBm 1-dB compression point, and -18.6 dBm IIP3.

TABLE OF CONTENTS

Chapter 1: INTRODUCTION	1
1.1 RF Front End Receiver.....	1
1.2 Mixer	2
1.2.1 Mixer Fundamental.....	2
1.2.2 Mixer Specifications	4
1.3 Motivation	9
1.4 Dissertation Organization.....	10
Chapter 2: GILBERT MIXER ANALYSIS AND COMPARISON.....	11
2.1 Single Balanced Gilbert Cell Mixer	11
2.2 Double Balanced Gilbert Cell Mixer	12
2.3 Tunable Gilbert Cell Mixer	14
2.3.1 Tunable Gilbert Mixer Operation	14
2.3.2 Transconductance Stage.....	15
2.3.3 Switching Stage	16
2.3.4 Current Mirror	17
2.3.5 RLC Resonator	18
Chapter 3: PROPOSED TUNABLE GILBERT MIXER WITH EFFECTIVE PROTOTYPE INDUCTOR	21
3.1 The Proposed Tunable Gilbert Mixer.....	21

3.1.1 DC Simulation for Power Specified	22
3.1.2 Theoretical Analysis for Bandwidth Specified	23
3.1.3 Theoretical Analysis for Center Frequency Specified	24
3.2 Pseudocode for Power Simulation	24
3.3 Simulation Results.....	27
3.3.1 DC Simulation of Power Specification	27
3.3.2 AC Simulation of Center Frequency and Bandwidth Specification	28
3.3.3 Noise Figure.....	29
3.3.4 1- dB Compression Point	29
3.3.5 Third-order Intercept Point (IP3)	30
3.4 Gilbert Mixer Performance of Past Works	30
3.5 Comparison of Proposed Tuning Gilbert Mixer with Previous Mixer Works ..	31
Chapter 4: TUNABLE MIXER LAYOUT INDUCTOR LOSS AND	
EQUIVALENT ELECTRONIC CIRCUIT ANALYSIS.....	34
4.1 Layout Design, Verification, and Simulation Flow	34
4.2 Layout Design Approach	36
4.3 Example of f_{c0} (200 MHz) with a Controllable BW0 (50 MHz)	38
4.4 Layout Performance Analysis	40
4.4.1 DC Simulation of Power Specification.....	40
4.4.2 AC Simulation of Center Frequency and Bandwidth Specification	41
4.5 Effective Prototype Inductance in the Tunable Mixer Design	42
4.6 Equivalent Electronic Circuit for the Square Planar Inductor.....	43

4.6.1 AC Simulation	47
4.6.2 Design Approach	48
4.6.3 Proposed Mixer with Equivalent Electronic Circuit Performance	50
Chapter 5: LOW NOISE AMPLIFIER TOPOLOGY	54
5.1 Low Noise Amplifier Fundamental.....	54
5.2 Common Source Amplifier	57
5.2.1 Common Source Amplifier with Load R_D	57
5.2.2 Common Source Amplifier with Source Degeneration	58
5.2.3 Common Source Amplifier with Active Load.....	59
5.3 Common Drain Amplifier	61
5.4 Common Gate Amplifier.....	62
5.5 Cascode Amplifier.....	63
5.6 Differential Amplifier	65
5.7 Two Stages Operational Amplifier	67
5.8 Noise Cancellation and Reduction Technology	69
5.8.1 Feedforward Noise-canceling Technique	69
5.8.2 Gain-enhanced Noise-canceling Technique	72
5.8.3 CG and CS Combination Noise-canceling Technique.....	76
Chapter 6: TUNABLE GILBERT MIXER INTEGRATED WITH A HIGH-GAIN LOW-NOISE AMPLIFIER.....	80
6.1 The Proposed High-Gain Low-Noise Amplifier	80
6.1.1 Center Frequency and Conversion Gain	84

6.1.2 Noise Figure.....	86
6.1.3 Linearity.....	88
6.2 Tunable Gilbert Mixer and Low-Noise Amplifier Integration.....	89
6.3 Performance of Integrated Circuit.....	90
6.4 Comparison of Different Tunable Gilbert Mixer Technologies.....	93
Chapter 7: CONCLUSION AND FUTURE WORK.....	95
7.1 Conclusion.....	95
7.2 Future Work	95
REFERENCES	97

LIST OF FIGURES

Figure 1.1 Block diagram of RF front end	2
Figure 1.2 The symbol of ideal mixer	2
Figure 1.3 Down-conversion mixer representation	4
Figure 1.4 Up-conversion mixer representation	4
Figure 1.5 Definition of 1-dB compression point	6
Figure 1.6 Example of harmonic sets	7
Figure 1.7 Example of intermodulation	7
Figure 1.8 Example of intermodulation and harmonics products	8
Figure 1.9 Third-order intercept	9
Figure 2.1 Single-balanced mixer	11
Figure 2.2 Single-balanced mixer waveform	12
Figure 2.3 Double-balanced mixer	13
Figure 2.4 Schematic view of tunable Gilbert cell mixer	14
Figure 2.5 Transconductance stage of tunable Gilbert mixer	15
Figure 2.6 Switching stage of tunable Gilbert mixer	16
Figure 2.7 Current sink of tunable Gilbert mixer	17
Figure 2.8 RLC resonator of tunable Gilbert mixer	18
Figure 2.9 Parallel RLC impedance	19
Figure 2.10 Bandwidth of RLC resonator	19

Figure 3.1 Proposed tunable Gilbert mixer	21
Figure 3.2 DC simulation of the proposed Gilbert mixer	27
Figure 3.3 Center frequency and bandwidth of the proposed Gilbert mixer.....	28
Figure 3.4 NF performance of the proposed Gilbert mixer.....	29
Figure 3.5 1-dB compression point performance of the proposed Gilbert mixer ...	29
Figure 3.6 IP3 of the proposed Gilbert mixer	30
Figure 4.1 Design rule check and parasitic extraction flow	34
Figure 4.2 Layout of a tunable mixer operating at IF =200MHz and BW=50 MHz	35
Figure 4.3 Design flow of power optimization	36
Figure 4.4 Design flow of f_{c0} and BW_0 optimization	37
Figure 4.5 DC simulation of power specification	40
Figure 4.6 AC simulation of center frequency and bandwidth specification	41
Figure 4.7 Effective prototype square planar inductor and layout ($L=7.0008\text{nH}$) .	42
Figure 4.8 Effective prototype inductance (Red) vs. Layout inductance (Yellow)	43
Figure 4.9 Equivalent electronic circuit for square planar inductor	44
Figure 4.10 Experimental curve vs. equivalent electronic circuit simulated	44
Figure 4.11 π -model implementation in the tunable mixer	45
Figure 4.12 Tunable mixer with equivalent electronic circuit (π -model)	46
Figure 4.13 DC simulation of the equivalent π -model tunable mixer	51
Figure 4.14 AC simulation of the equivalent π -model tunable mixer	52
Figure 4.15 Noise figure of the equivalent π -model tunable mixer	52
Figure 4.16 1-dB compression point of the equivalent π -model tunable mixer	53

Figure 4.17 IP3 of the equivalent π -model tunable mixer	53
Figure 5.1 Block diagram of low noise amplifier in RF front-end system	54
Figure 5.2 Common source amplifier with R_D	57
Figure 5.3 Small signal model of common source amplifier with R_D	58
Figure 5.4 Common source amplifier with source degeneration	58
Figure 5.5 Small signal model of common source amplifier with source degeneration	59
Figure 5.6 Common source amplifier with active load	60
Figure 5.7 Common drain amplifier (source follower)	61
Figure 5.8 Small signal model of common drain amplifier	61
Figure 5.9 Common gate amplifier	62
Figure 5.10 Small signal model of common gate amplifier	62
Figure 5.11 Cascode amplifier	63
Figure 5.12 Small signal model of cascode amplifier	64
Figure 5.13 Cascode amplifier with adding PMOS transistor	65
Figure 5.14 Differential amplifier	66
Figure 5.15 Approximate small signal model of differential amplifier	66
Figure 5.16 General configuration of Op-amp	67
Figure 5.17 Op-amp feedback network	67
Figure 5.18 Two-stage Op-amp	68
Figure 5.19 Second-order small signal model of two-stage Op-amp	69
Figure 5.20 Matching (a) noise and (b) signal voltage at nodes X and Y	70

Figure 5.21 Wide-band LNA exploiting noise canceling	71
Figure 5.22 Resistive shunt feedback LNA using the gain-enhanced noise-canceling technique	72
Figure 5.23 First noise-canceling LNA using gain-enhanced technique	73
Figure 5.24 Second noise-canceling LNA using gain-enhanced technique	74
Figure 5.25 Noise-canceling stage of second LNA	75
Figure 5.26 Common wideband input matching technique (common gate)	76
Figure 5.27 Common wideband input matching technique (common source) ...	77
Figure 5.28 Common wideband input matching technique	77
Figure 6.1 The proposed high-gain low-noise amplifier	80
Figure 6.2 Center frequency of the proposed LNA	86
Figure 6.3 Noise figure of 1st stage, 1st, and 2nd stage and proposed LNA	88
Figure 6.4 1-dB compression of the proposed LNA	88
Figure 6.5 IP3 of the proposed LNA	89
Figure 6.6 Block diagram of proposed updated mixer.....	89
Figure 6.7 Proposed updated mixer.....	90
Figure 6.8 Center frequency comparison between prototype Gilbert mixer (green) and proposed mixer with LNA (red)	91
Figure 6.9 Noise figure comparison between prototype Gilbert mixer (green) and proposed mixer with LNA (red).....	92
Figure 6.10 1-dB compression of the proposed mixer with LNA.....	92
Figure 6.11 IP3 of the proposed mixer with LNA	93

Figure 7.1 Multi-band multi-standard receiver architecture for wireless applications	
.....	96

LIST OF TABLES

Table 3.1 Summary of Tunable Gilbert Mixer with IF (0.1GHz-1.1 GHz).....	30
Table 3.2 Comparison of the Proposed Tuning Gilbert Mixer with Previous Mixer Works	32
Table 6.1 Comparison of Different Mixer Technologies.....	94

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Chapter 1: INTRODUCTION

1.1 RF Front End Receiver

The RF (radio frequency) communication system has become more critical in recent years. With the development of RF technology, cell phones to base stations are widely used in our daily lives. As a result, the communication industry reformed the way of transmitting and receiving information. Meanwhile, more economical, reliable, and efficient components are required and created during the increasing demand in the competitive industry marketing. In addition, CMOS technology is widely used in RF front-end systems because of its low power dissipation properties, compact size, and very well device modeled.

The RF front end defines everything in a receiver between the antenna and the intermediate frequency (IF) stage, and this includes the low noise amplifier (LNA), Mixer and IF filter, and voltage controlled oscillator (VCO) [1], as shown in Fig.1.1. The RF signals received at the antenna needed to be modulated to process into the baseband analog-to-digital converter (ADC). The LNA is a particular type of component to amplify a weak signal captured by the antenna and feed it to the RF port of the mixer. An amplified RF input signal is mixed with the local oscillator (LO) signal. The difference frequency between the RF input signal and the signal from the LO output is referred to as the intermediate frequency (IF). The IF signal is also the

output signal of the entire RF front-end system, which is then converted to a digital signal by an analog-to-digital converter (ADC). Finally, the bits of data are processed.

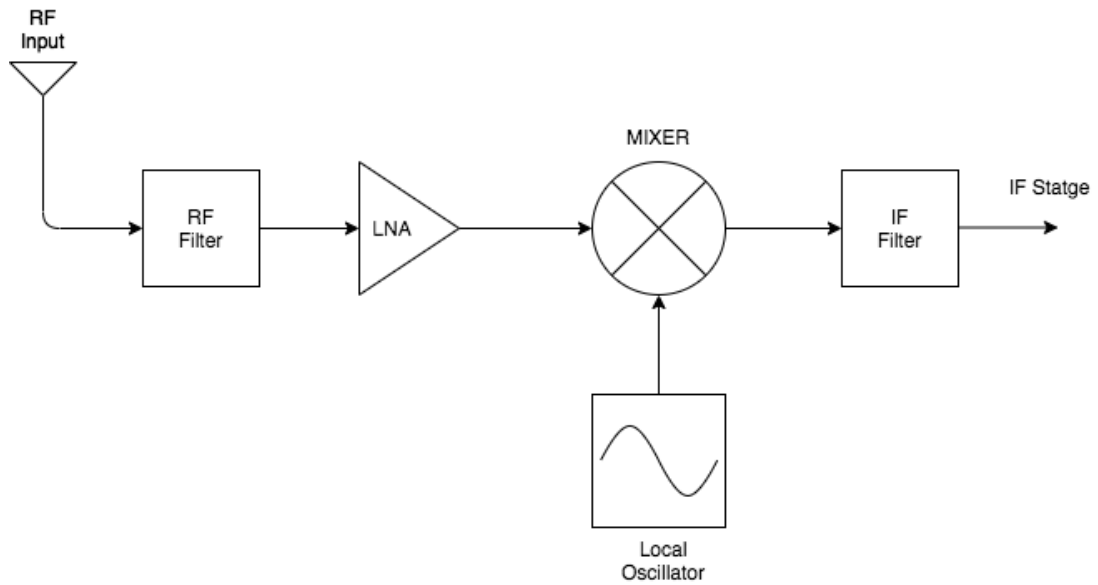


Figure 1.1 Block diagram of RF front end

1.2 Mixer

1.2.1 Mixer Fundamental

The mixer is a critical RF front-end receiver device and performs frequency translation. The function of an ideal mixer is to convert the RF input signal (incoming signal after the LNA amplifies it) to output IF signal by mixing it with the LO signal [2]. An ideal mixer symbol is shown in Fig.1.2.

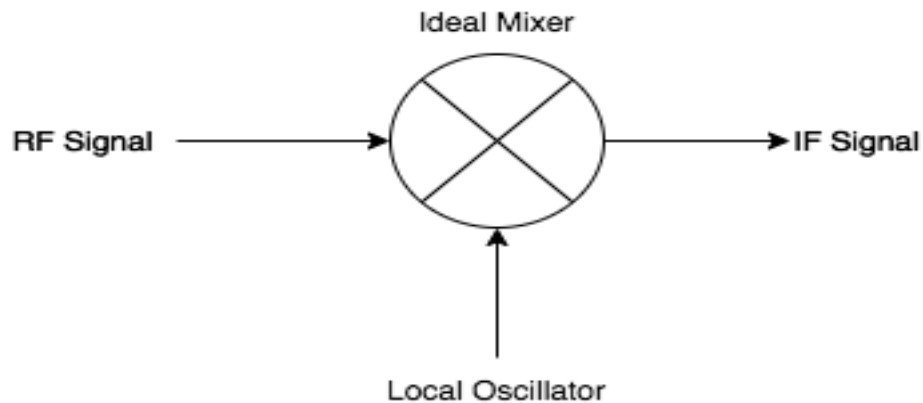


Figure 1.2 The symbol of ideal mixer

The multiplication process in an ideal nonlinear mixer is expressed in the following equations.

$$\text{Signal } a = A * \sin (w_1 t) \quad (1.1)$$

$$\text{Signal } b = B * \sin (w_2 t) \quad (1.2)$$

The equation of multiplying signal a and signal b will be:

$$a * b = A * \sin(w_1 t) * B * \sin(w_2 t) = A * B * \sin(w_1 t) * \sin(w_2 t) \quad (1.3)$$

Based on the trigonometric function:

$$\sin x * \sin y = -\frac{1}{2} [\cos(x + y) - \cos(x - y)] \quad (1.4)$$

Where $x = w_1 t$ and $y = w_2 t$,

$$a * b = -\frac{AB}{2} * [(\cos(w_1 t) + \cos(w_2 t)) - (\cos(w_1 t) - \cos(w_2 t))] \quad (1.5)$$

$$a * b = -\frac{AB}{2} * [\cos(w_1 + w_2) * t - \cos(w_1 - w_2) * t] \quad (1.6)$$

According to Eq.(1.6), the first frequency component $\cos(w_1 + w_2) * t$ is the sum of the RF and LO frequency, and the second frequency component $\cos(w_1 - w_2) * t$ is the difference between RF and LO frequency. Typically, only one signal will be selected based on the selection of the mixing modulation. When the difference between RF and LO and outputting a lower frequency than our input signals, the down-conversion mixer is performed, as shown in Fig.1.3. However, when the sum of the RF and LO frequency component is selected, this type of mixing is referred to as up converting mixer as shown in Fig.1.4.

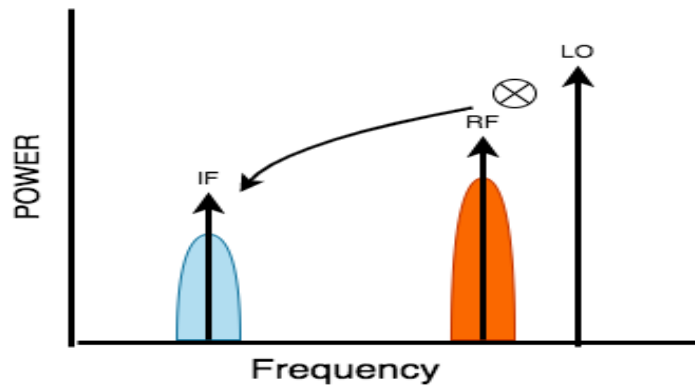


Figure 1.3 Down-conversion mixer representation

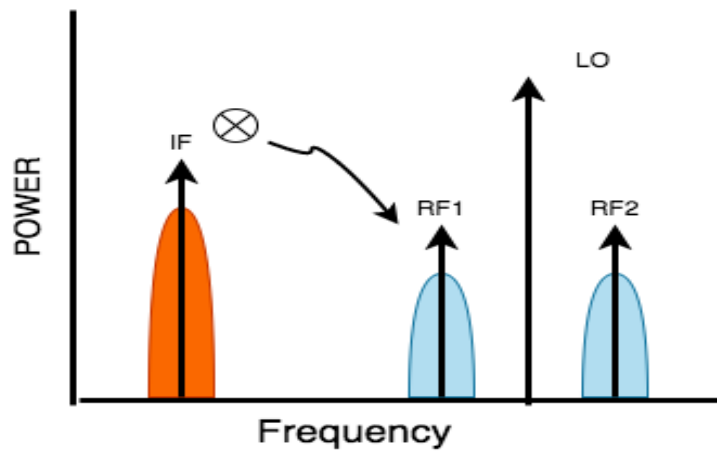


Figure 1.4 Up-conversion mixer representation

1.2.2 Mixer Specifications

1. Gain:

A conversion gain (CG) can be described as the ratio (in dB) between the IF and RF signal, which could be either voltage or power gain, usually the difference frequency between the RF signal and LO signal.

$$\text{Power Gain(dB)} = 10\log_{10} \frac{\text{Power}_{\text{IF}}}{\text{Power}_{\text{RF}}} \quad (1.7)$$

$$\text{Voltage Gain(dB)} = 20\log_{10} \frac{\text{Voltage}_{\text{IF}}}{\text{Voltage}_{\text{RF}}} \quad (1.8)$$

2. Noise Figure:

The noise figure is a parameter by which the noise performance of a mixer can be specified. It is used to evaluate the sensitivity of an RF front-end receiver system. The lower value of the noise figure, the better performance. It is defined as the input (signal-to-noise ratio) SNR ratio (in dB) to output SNR ratio (in dB).

$$\text{Noise Figure (dB)} = 10\log_{10}\left(\frac{\text{SNR}_{\text{RF}}}{\text{SNR}_{\text{IF}}}\right) \quad (1.9)$$

3. 1dB Compression Point:

1-dB compression point is one of the most important specifications for a mixer. It is used to measure the linearity of a mixer. Linear devices produce a constant gain in a specific frequency range. A linear slope is supposed to be observed in a graph of output power versus input power. As the input power increases, the gain begins to curve at a certain point, and the mixer goes into a compression zone with no other output increasing. The gain gets flattened and becomes a non-linear device producing distortion, harmonic, and intermodulation products. As shown in Fig.1.5, The red slope is the theoretical linear slope, and the blue slope is the practical slope. If the gain achieved 1dB reduced from the normal linear gain, that point is called the 1-dB compression point. After the slope gets flattened, the output signal power does not increase with the input signal power increases, which means the mixer starts to saturate. A mixer with a high 1-dB power point will achieve high linearity. 1 dB compression point is when the input power signal starts to change distortions. The mixer should always be operated below the compression point.

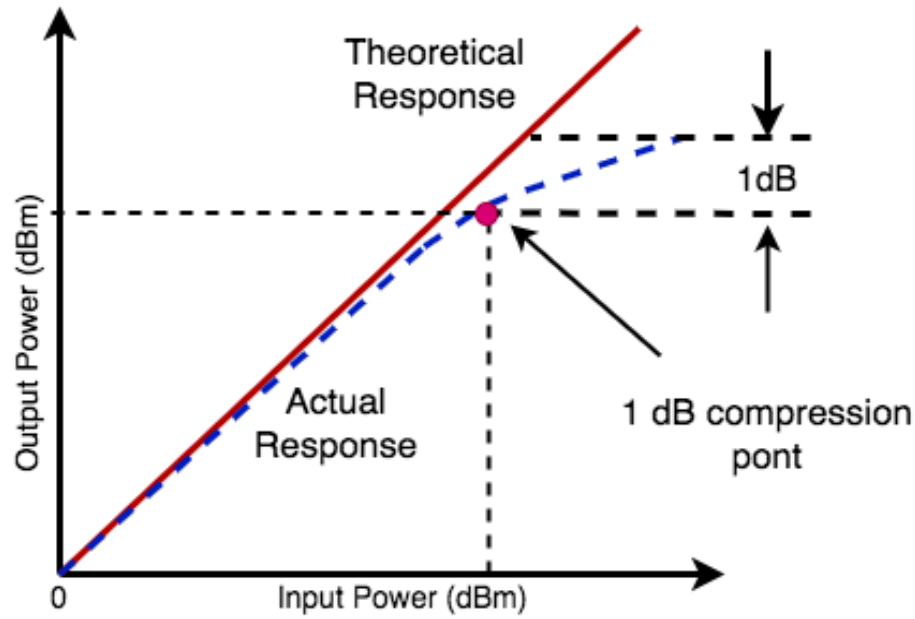


Figure 1.5 Definition of 1-dB compression point

4. Third-Order Intercept (IP3)

Linearity is the device produces an output directly proportional to its input. It is typical for devices to operate linearly only over a specific input power range. For non-linear devices like the mixer, the distortion and intermodulation product is created when operating in the non-linear region. A harmonic signal is a copy of the fundamental signal that appears as an integer multiple. For example, suppose a signal with 100MHz ($f_1=100\text{MHz}$) passes to a non-linear device. In that case, it will produce a set of harmonics, including the first harmonic ($f_1=100\text{MHz}$), the second harmonic ($f_2=200\text{MHz}$), and the third harmonic ($f_3=300\text{MHz}$), the fourth harmonic ($f_4=400\text{MHz}$), and the fifth harmonic ($f_5=500\text{MHz}$). Harmonic amplitudes usually decrease as the harmonic order increases, as shown in Fig.1.6. However, harmonics are

undesirable.

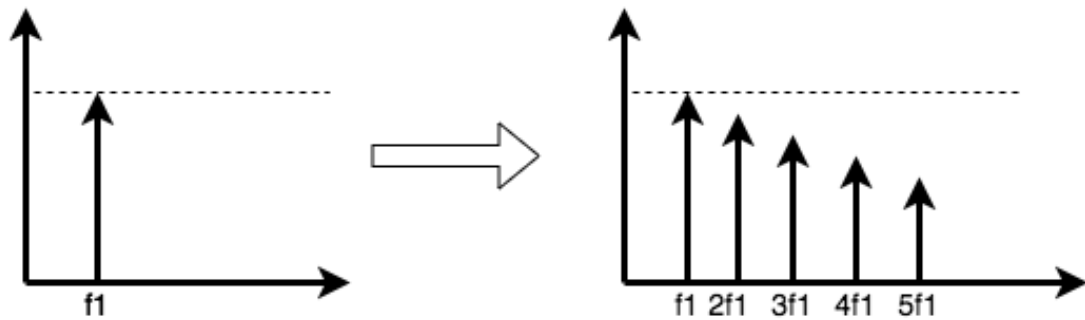


Figure 1.6 Example of harmonic sets

Unlike harmonic, which can be created by one input signal, in a nonlinear device, intermodulation occurs when more than two signals are mixed. For example, when two signals mix, the outputs contain the sum and difference frequencies, as shown in Fig.1.7. If two input signals with $f_1=250\text{MHz}$ and $f_2=450\text{MHz}$, two output intermodulation frequencies will be generated with $f_1+f_2=700\text{ MHz}$ and $f_2-f_1=200\text{MHz}$.

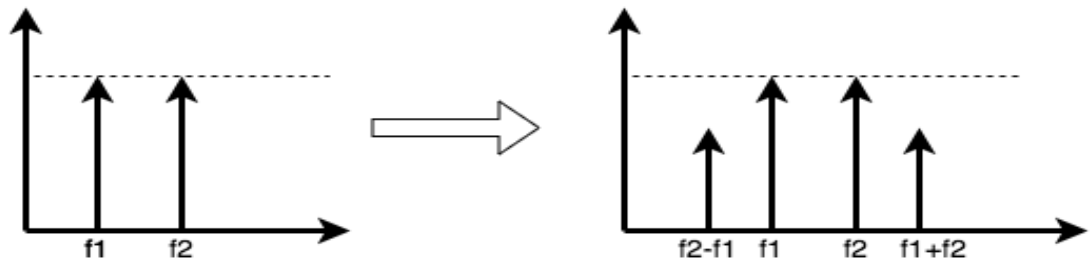


Figure 1.7 Example of intermodulation

f_1 and f_2 can be mixed with other harmonics, like $2f_1$ and $2f_2$. Additional intermodulation products will also be created. In harmonics and intermodulation, the order is determined by the sum of their coefficients.

For example, $2f_1$ is second order, f_1+f_2 is also second order, $3f_1$ is third

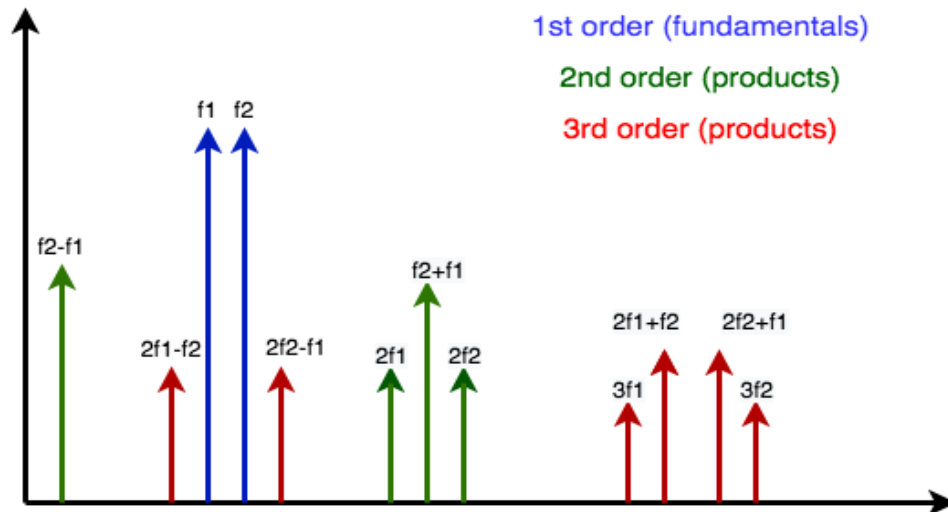


Figure 1.8 Example of intermodulation and harmonics products

order, and $2f_2-f_1$ and $2f_2+f_1$ are both third order. Harmonics and intermodulation produce undesirable signals because they can amplify noise and produce intermodulation distortion in adjacent channels. Some higher-order harmonic and intermodulation products can be ignored because they have very low amplitude and fall outside bandwidth. Still, it will become difficult to deal with when harmonic and intermodulation signals are very close in frequency to the desired signals, such as the two 3rd order signals $2f_1-f_2$ and $2f_2-f_1$, as shown in Fig. 1.8, which are difficult to filter out because they are too close to the fundamentals (f_1 and f_2). In Fig. 1.9, for every 1dB increase in the fundamental (useful) signal (blue), the third-order (unwanted) intermodulation signal (red) increases by 3dB. It would appear these two lines meet at some point. The output power no longer increases linearly with input power at a certain input power. The lines begin to curve as the device enters into compression. However, if the two lines continue to be extended, two lines will meet at the third-order intercept point. The third-order intercept point is commonly used to measure a mixer's linearity.

The higher the third-order intercept, the better the linearity and the lower level of intermodulation distortion.

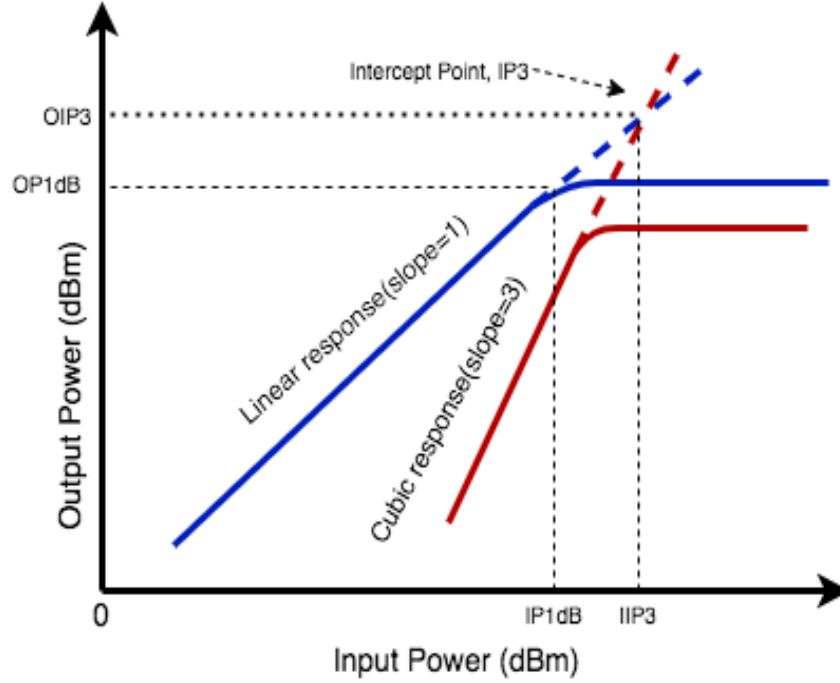


Figure 1.9 Third-order intercept

1.3 Motivation

In a multi-band/multi-standard RF front-end system, a wide tuning Gilbert mixer can be used to access all of the available bandwidth specifications. In CMOS Gilbert mixer wide tuning designs, tradeoffs occur between power consumption, noise figure, and linearity. The proposed tunable Gilbert mixer, with an effective prototype inductor automated design synthesis approach, is used to design a tunable mixer meeting specified requirements. An equivalent electronic circuit of the effective prototype inductor is also introduced to reduce parasitic effects, allowing the proposed mixer to meet the specified specifications.

1.4 Dissertation Organization

The dissertation is organized as follows. Chapter 1 introduced the background and fundamentals of the mixer. Chapter 2 analyzes and compares different mixer designs such as single-balanced mixer, double-balanced mixer, and tunable cell Gilbert mixer. Chapter 3 presents the proposed tunable Gilbert mixer with effective prototype inductor. Chapter 4 presents tunable mixer layout inductor loss and equivalent electronic circuit analysis. Chapter 5 presents different low noise amplifiers and noise cancellation and reduction technology. Chapter 6 presents a tunable Gilbert mixer integrated with a high-gain, low-noise amplifier. Chapter 7 presents the conclusion and future work.

Chapter 2: GILBERT MIXER ANALYSIS AND COMPARISON

2.1 Single Balanced Gilbert Cell Mixer

Gilbert mixer is one of the most popular mixer designs in today's industrial world. It was invented by Howard Jones in 1963. The reason why Gilbert mixer is chosen is that it provides good conversion gain. The balanced operation, port isolation, and linearity at a low power consumption while maintaining a low noise figure. Due to the above advantages, it is widely used in many communication applications in modulators, phase detectors, and multipliers.

The single balanced Gilbert cell mixer has a differential LO signal but a single-ended RF input signal. LO differential signals are applied to switch transistors to combine with an RF input signal to generate an IF output signal. The design of a single balanced Gilbert mixer is shown in Fig.2.1.

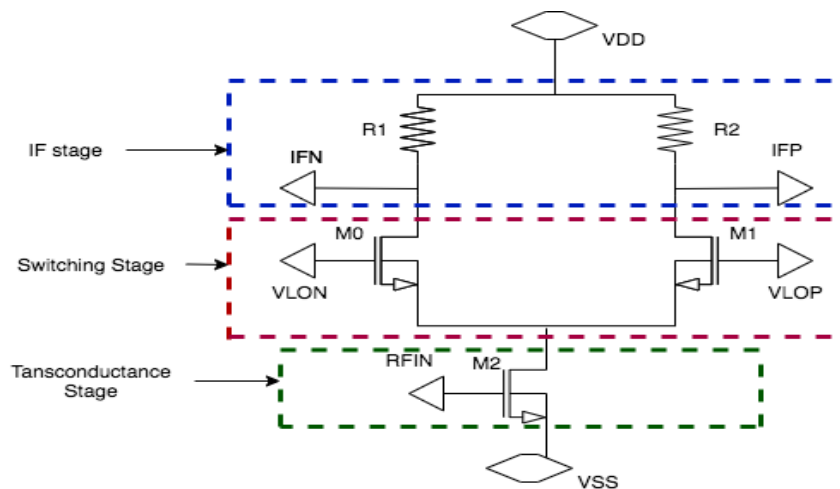


Figure 2.1 Single-balanced mixer

In Fig. 2.1, the single balanced Gilbert mixer consists of three stages (transconductance, switching, and IF). The RFIN voltage signal is converted into a current signal to enter transistor M_2 in the transconductance stage, while the LO signal is separated into transistors M_0 and M_1 . The current signal from the transconductance stage is mixed with LO switching signal in the switching stage. The mixed output current signal is converted to voltage via load resistors R_1 and R_2 in the IF stage. The IF output waveform is shown in Fig.2.2.

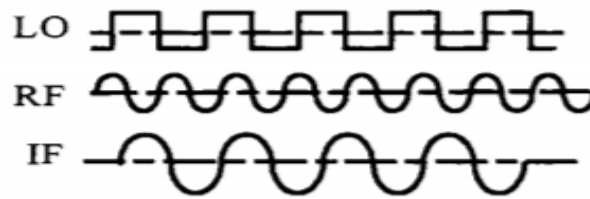


Figure 2.2 Single-balanced mixer waveform

2.2 Double Balanced Gilbert Cell Mixer

Fig.2.3 shows the double-balanced Gilbert cell mixer. The double-balanced mixer is also known as the Gilbert cell mixer. The double-balanced mixer provides a higher level of performance in RF applications than a single-balanced mixer. The RF and local oscillator input signals are balanced using a differential structure. Additionally, differential circuits are applied to their inputs to lower their output. Compared with the conventional single-balanced mixer, the double-balanced mixer has better linearity and isolation performance between all ports.

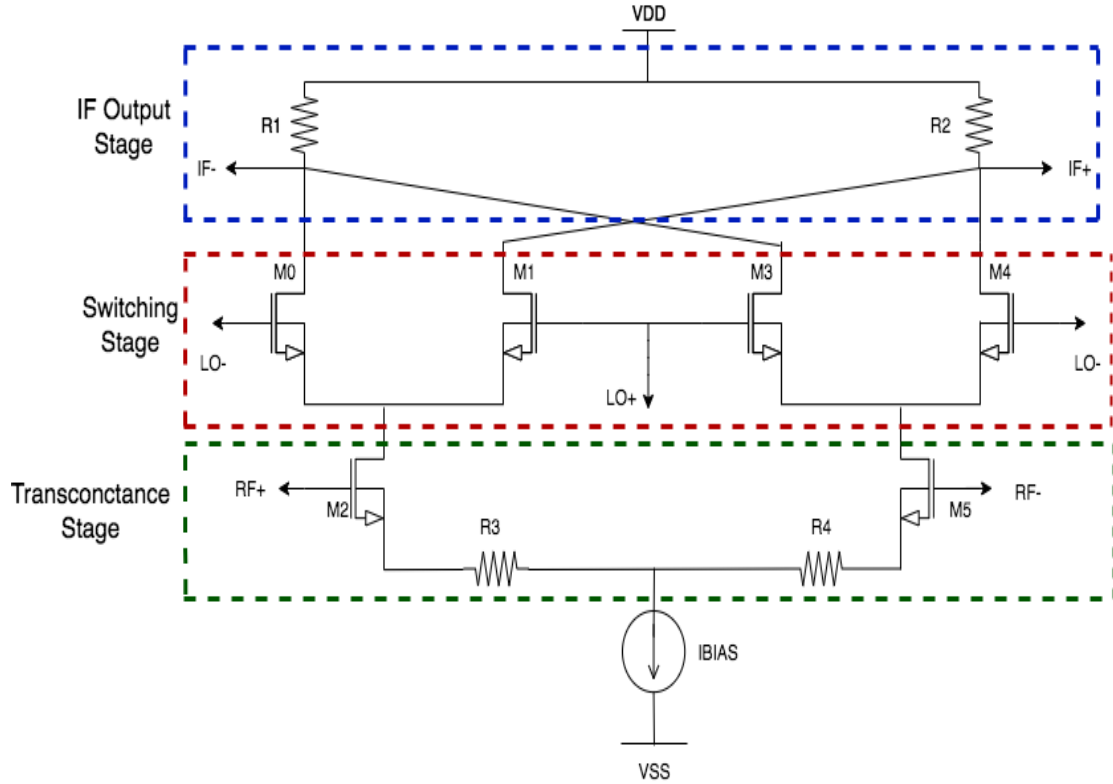


Figure 2.3 Double-balanced mixer

A double-balanced Gilbert mixer comprises two single-balanced mixers with three stages: the transconductance stage, the switching stage, and the IF output stage [1]. Differential RF input signals are received by transistors M_2 and M_5 . The differential LO signals are received by transistors M_0 , M_1 , M_3 , and M_4 . Transistors M_0 and M_4 provide the IF output stage. The current source, called I_{bias} , is used to set the current for the mixer and bias the transistors to remain in the saturation region. In the transconductance stage, different RF input ($RF+$ and $RF-$) voltage signals are converted to a current signal by M_2 and M_5 . Then, the current signal from the transconductance stage is mixed with transistor M_0 , M_1 , M_3 , and M_4 LO switching signals at the switching stage. The mixed output current signal in the IF output stage is converted to a voltage signal by load resistors R_1 and R_2 .

2.3 Tunable Gilbert Cell Mixer

It is desirable to have a cost-effective Gilbert mixer cell that can be tuned to meet the frequency band standards of various RF devices, which are being upgraded to support future standards. For example, the conventional CMOS double-balanced Gilbert mixer cell design has not been easily modified to operate in different frequency bands within a wide frequency range and controllable bandwidth. A tunable Gilbert mixer will be presented in this section to solve this problem. The type of mixer that uses two tunable parallel RLC resonators to replace the load resistors in a double-balanced Gilbert cell mixer.

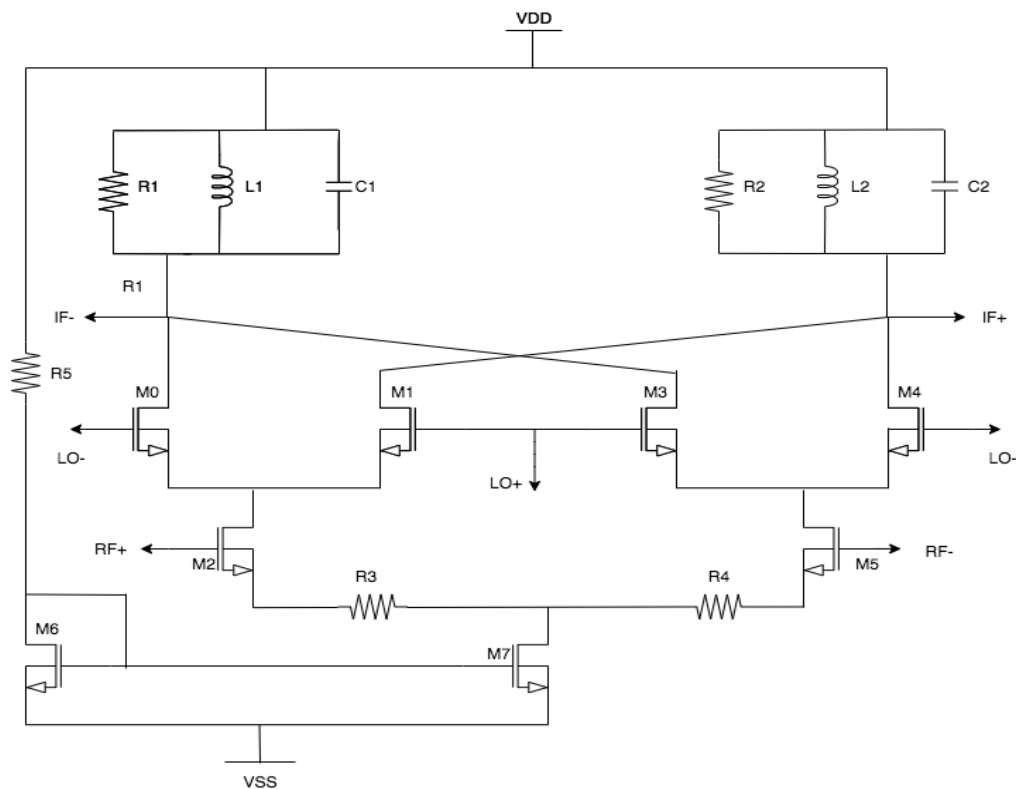


Figure 2.4 Schematic view of tunable Gilbert cell mixer

2.3.1 Tunable Gilbert Mixer Operation

According to Fig.2.4, the tunable Gilbert mixer mainly consists of an RLC parallel resonator, a double-balanced Gilbert mixer cell, and a current source. RF signal (RF+,

RF-) is applied to the differential pair transistors M_2 and M_5 in the transconductance stage to perform a voltage to current conversion, and I_{ds2} and I_{ds5} are produced. Transistors M_0 , M_1 , M_3 , and M_4 operate in a switch stage. When the voltage at LO- is large enough, M_0 and M_4 are turned on, and M_1 and M_3 are turned off due to the small voltage at LO+. As a result, M_0 and M_4 operate as closed switches, so R_1 is connected to M_0 , and R_2 is connected to M_4 . When LO+ is large enough in the next cycle, M_1 and M_3 are turned on.

Meanwhile, M_0 and M_4 are turned off due to small LO-. M_1 and M_3 act as closed switches, so R_1 is connected to M_3 , and R_2 is connected to M_1 . R_1 and R_2 are tunable in the resonator to meet a specified bandwidth. M_6 and M_7 are combined to form a current mirror circuit. Both operate in the saturation region and act as a current sink to provide a constant current to the mixer. Following are the components of the tunable Gilbert mixer.

2.3.2 Transconductance Stage

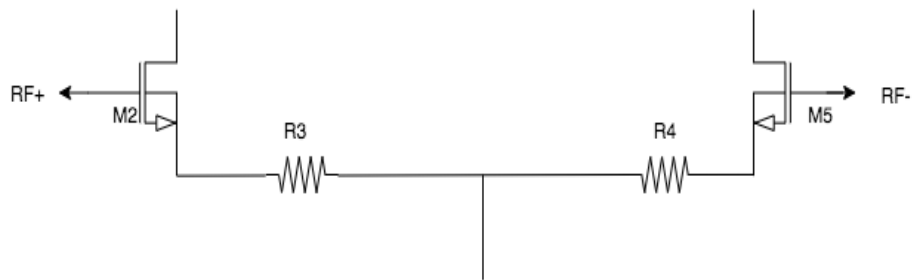


Figure 2.5 Transconductance stage of tunable Gilbert mixer

RF+ and RF- are the input signals to the differential pair in the transconductance stage. It is the first stage of the tunable Gilbert mixer which should have good linearity to handle the power generated by the operational amplifier. The two transistors with the RF terminals act as amplifiers, increasing the signal's gain before mixing [2]. Source

generation resistors R_3 and R_4 can be adjusted to improve linearity or gain. The voltage gain of the mixer with source degeneration is

$$\text{Gain} = \frac{2}{\pi} * \left(\frac{R_1}{R_3 + \frac{1}{gm}} \right) \quad (2.1)$$

The gain is determined by gm is given by

$$gm = \sqrt{\frac{2 * k_n * W_2 * I_{ds2}}{l}} \quad (2.2)$$

The M_2 and M_5 should be biased towards working in the saturation region. Based on Eq. (2.1), increase the width of M_2 and M_3 while maintaining a minimum length to increase the gain. The source degeneration resistors R_3 and R_4 will affect the system output swing range.

2.3.3 Switching Stage

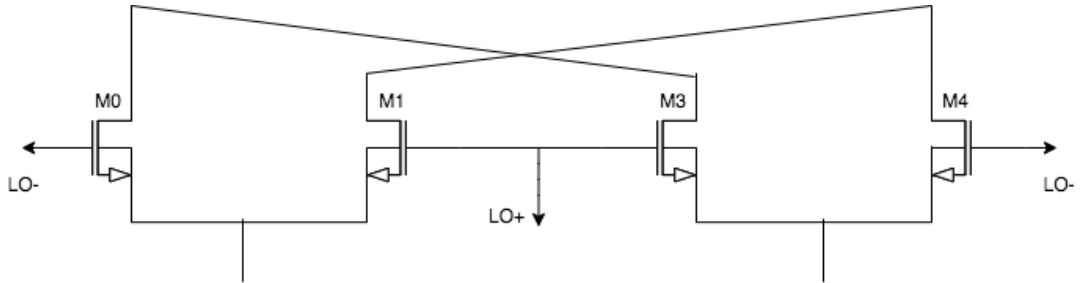


Figure 2.6 Switching stage of tunable Gilbert mixer

The LO signal value should be reasonable to guarantee that the switches (M_0 , M_3) and (M_1 , M_4) work properly. When the LO becomes too large, this leads transistors out of the saturation region. For example, M_0 , M_3 , M_1 , M_4 should operate in the saturation region to keep switching flawlessly. When the pair of M_0 and M_3 is on, it is best for the

other pair M_1 and M_4 to be entirely off. If two pairs are conducting switching simultaneously, it will generate noise.

2.3.4 Current Mirror

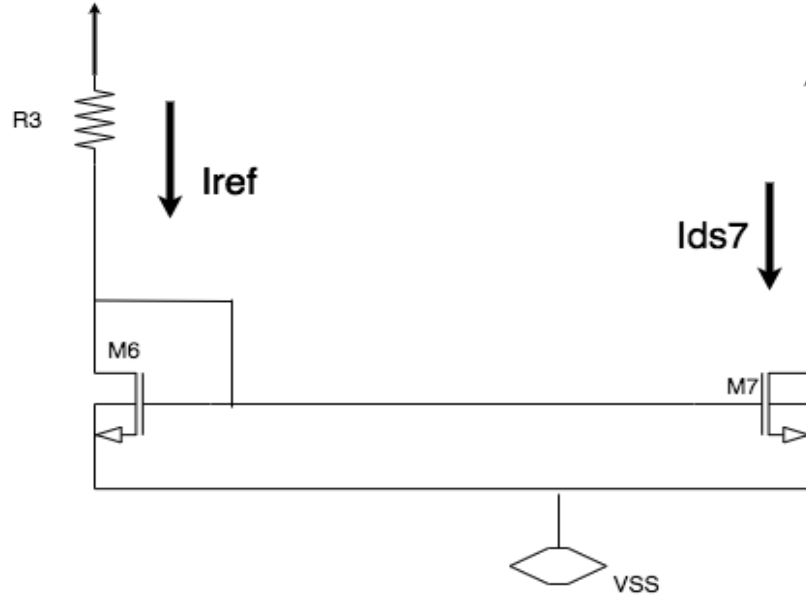


Figure 2.7 Current sink of tunable Gilbert mixer

A current sink of the tunable Gilbert mixer is shown in Fig. 2.7. The current sink consists of two transistors, M_6 and M_7 , to perform by a current mirror. In the current sink, M_6 always operates in the saturation region because the drain is shorted to the gate terminal.

$$V_{ds6} = V_{gs6} > V_{gs6} - V_T \quad (2.3)$$

Therefore, M_6 operates in the saturation region.

$$I_{ds6} = \frac{1}{2} * k_n * \frac{W_6}{L_6} * (V_{gs6} - V_T)^2 \quad (2.4)$$

I_{ds6} can be considered as reference current. V_{DD} supplies it through R_3 .

$$I_{ds6} = I_{ref} = \frac{V_{DD} - V_{gs6}}{R_3} \quad (2.5)$$

Current I_{ds7} is

$$I_{ds7} = \frac{k_n}{2} * \frac{W_7}{L_7} * (V_{gs7} - V_T)^2 \quad (2.6)$$

Because $V_{gs6}=V_{gs7}$, and assume threshold V_T are same. Combine Eq. (2.4) and (2.6).

Then,

$$\frac{I_{ds6}}{I_{ds7}} = \frac{\frac{W_7}{L_7}}{\frac{W_6}{L_6}} \quad (2.7)$$

Keep the length of all transistors identical, so

$$\frac{I_{ds6}}{I_{ds7}} = \frac{W_7}{W_6} \quad (2.8)$$

The current I_{ds6} is controlled by $I_{ds6} = \frac{V_{DD}}{R_3}$ and the width of transistor M_6 . I_{ds6} is proportional with W_6 because current mirror operation, which makes the current independent of V_{out} [38].

2.3.5 RLC Resonator

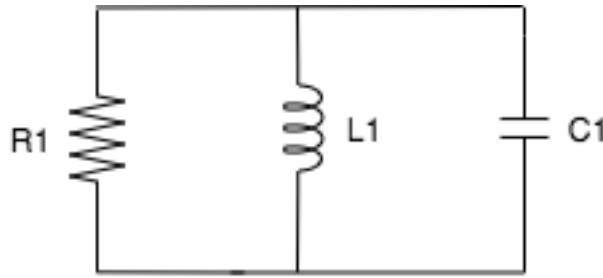


Figure 2.8 RLC resonator of tunable Gilbert mixer

The parallel RLC circuits are used as the core structure for tuning Gilbert mixers to meet specified center frequency and bandwidth. A resonator containing a resistor (R_1), inductor (L_1), and capacitor (C_1), as shown in Fig. 2.8. For a parallel RLC circuit, the resonance occurs at the highest impedance when $Z_L=Z_C$.

$$Z_C = 2\pi * f * L1 = \frac{1}{2\pi * f * C1} \quad (2.9)$$

Then:

$$f^2 = \frac{1}{2\pi * L1 * 2\pi * C1} = \frac{1}{4\pi^2 * L1 * C1} \quad (2.10)$$

$$f = \sqrt{\frac{1}{4\pi^2 * L1 * C1}} = \frac{1}{2\pi * \sqrt{L1 * C1}} \quad (2.11)$$

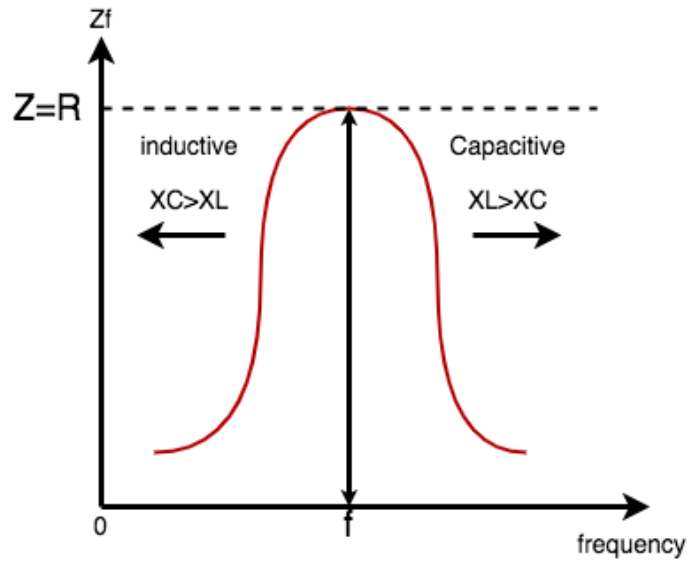


Figure 2.9 Parallel RLC impedance

The bandwidth can be estimated as

$$BW = \frac{1}{2\pi * R1 * C1} \quad (2.12)$$

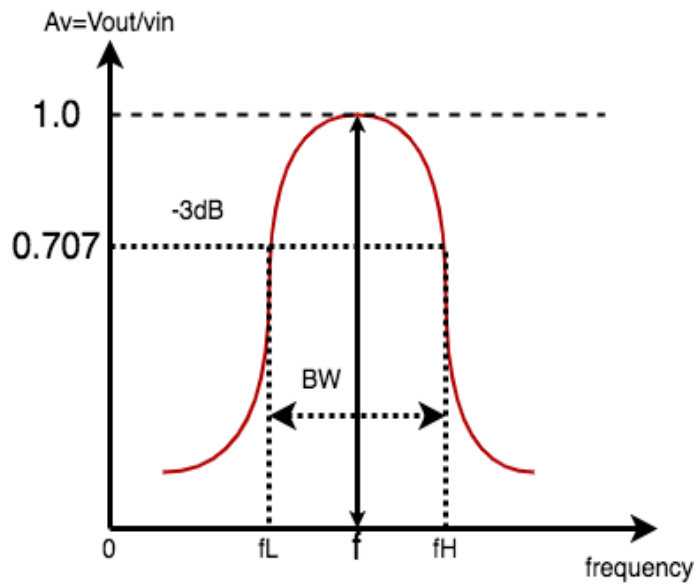
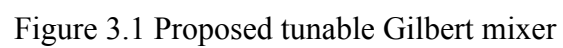


Figure 2.10 Bandwidth of RLC resonator

When $X_c > X_L$, the parallel RLC circuits perform an inductive function, and when $X_c < X_L$, the parallel RLC circuits perform a capacitive function. At the resonance, the impedance (Z) achieves the maximum (R). Fig. 2.9 shows the relationship between

impedance and frequency for a parallel RLC circuit. Fig. 2.10 shows the bandwidth of the parallel RLC circuit.

3.1 The Proposed Tunable Gilbert Mixer



3.1.1 DC Simulation for Power Specified

The short channel equations of the proposed tunable Gilbert mixer design

$$I_{dsn} = \frac{1}{2} * K_{nshort} * \frac{W}{L} * (V_{gs} - V_{tnshort})^2 (1 + \lambda_{nshort} * V_{ds}) \quad (3.1)$$

The corresponding transconductance

$$g_m = \sqrt{2 * \beta * I_{ds} * (1 + \lambda_{nshort} V_{ds})} \quad (3.2)$$

Based upon Eq .(3.1) and Eq .(3.2), then

$$g_m = \frac{2 * I_{ds}}{V_{gs} - V_{tnshort}} \quad (3.3)$$

To find the width of the transistor (M₀-M₇), all transistor widths are initially set as minimum width W₀=W₁=W₂=W₃=W₄=W₅=0.22um, W₆=0.22um and assume W₇ is initially set 10 times of W₆, W₇=10*W₆=2.2um. All transistor lengths are initially set as minimum length L=180nm. The V_{tnshort} is 0.55v in the 180nm CMOS technology considering the short channel effect. The K_{nshort} is the CMOS process factor, and λ_{nshort} is the channel length modulation parameter. To estimate K_{nshort} and λ_{nshort}, V_{bias}=1.1V of M₂ is selected with transistor width W₂=0.22um. From the I_{ds2} verse V_{ds2} of Transistor M₂, two operating points V_{d2}=1V, V_{s2}=34.49mV and V_{d2}=1.5V, V_{s2}=35.3462mV are substituted into Eq. (3.1) to constitute two equations to calculate K_{nshort} and λ_{nshort}. For example, When V_{bias}=1.1V, the corresponding I_{ds2}=64.4uA @ V_{d2}=1V, V_{s2}=34.49mV and I_{ds2}=67.4466uA @ V_{d2}=1.5V, V_{s2}=35.3462mV. The calculated K_{nshort}= 317uA/V², and λ_{nshort}=0.127. Substitute the I_{ds2}=60.84uA, V_{bias}=V_{g2}=1.1V, V_{s2}=33.504mV and V_{tnshort}=0.55V into Eq .(3.3), get g_m=2.356*10⁻⁴. Substitute λ_{nshort} 0.127; K_{nshort}= 317uA/V²; I_{ds2}=60.84uA; V_{d2}=0.641499V; V_{s2}=33.504mV g_m=2.356*10⁻⁴ into Eq .(3.4)

$$W_2 = \frac{L * g_m^2}{2 * K_{nshort} * I_{ds2} * (1 + \lambda_{nshort} * V_{ds2})} = 24\mu m. \quad (3.4)$$

Using $W_0=W_1=W_2=W_3=W_4=W_5=24\mu m$ to estimate new K_{nshort} and λ_{nshort} to find the width of the transistor (M_0 - M_5) works in the saturation region. Finally, $W_2=132\mu m$.

Find the width of M_6 and M_7 to limit Power to < 9 mW. K_{nshort} and λ_{nshort} of M_6 are selected with transistor width $W_7=2.2\mu m$ and $W_6=0.22\mu m$. From the I_{ds7} verse V_{ds7} of Transistor M_7 , two points $V_{ds7}=1V$ and $V_{ds7}=1.5V$, are substituted into Eq. (3.1) to constitute two equations to calculate K_{nshort} and λ_{nshort} . When $V_{bias}=1.1V$, the corresponding $I_{ds7}=1.01565mA$ @ $V_{ds7}=1V$ and $I_{ds7}=1.05193mA$ @ $V_{ds7}=1.5V$. $K_{nshort}=471\mu A/V^2$, and $\lambda_{nshort}=0.08$. Substitute the $I_{ds7}=853.766\mu A$, $V_{gs7}=1.56V$, and $V_{tnshort}=0.55V$ into Eq. (3.3), get $g_m=0.00169$.

Substitute $\lambda_{nshort}=0.08$; $K_{nshort}=471\mu A/V^2$; $I_{ds7}=853.766\mu A$; $V_{ds7}=0.409V$; $g_m=0.00169$ into Eq. (3.2).

$$W_7 = \frac{L * g_m^2}{2 * K_{nshort} * I_{ds7} * (1 + \lambda_{nshort} * V_{ds7})} \text{ Finally, } W_7=61\mu m. W_6=6.1\mu m.$$

Set $W_0=W_1=W_2=W_3=W_4=W_5=132\mu m$, $W_7=61\mu m$, $W_6=6.1\mu m$. After DC simulation, $I_{ds7}=5.1mA$ if $I_{ds6}=0.56mA$. Therefore, $I_{total}=5.1mA+0.56mA=5.66mA$, so $PW=I_{total} * V_{DD}=5.66mA * 1.8V=10.188mW > 9mW$. W_6 and W_7 will be adjusted to meet the DC power requirement in the following pseudocode.

3.1.2 Theoretical Analysis for Bandwidth Specified

Tunable Gilbert mixer operates at a constant IF bandwidth of 50MHz. Assume the conversion gain is 2. In this design, $R_7=R_8=45\Omega$

Then,

$$CG = \frac{2 * R_1}{\pi * (R_7 + \frac{1}{g_m})} = 2 \quad (3.5)$$

Substitute the $I_{ds2}=2.5675\text{mA}$, $V_{gs2}=0.7\text{V}$, and $V_{tnshort}=0.55\text{V}$ into Eq.(3.3), get $g_m=0.034$.

Substitute $g_m=0.034$ into Eq.(3.5), get $R_1=233.6\ \Omega$.

The bandwidth can be calculated as

$$BW = \frac{1}{2*\pi*R_1*C_1} = 50\text{MHz} \quad (3.6)$$

$$C_1 = C_2 = \frac{1}{2*\pi*R_1*BW} = 13.6\text{pF} \quad (3.7)$$

3.1.3 Theoretical Analysis for Center Frequency Specified

The center frequency is given by

$$f_{center} = \frac{1}{2*\pi*(L_1*C_1)^{-2}} = 200\text{MHz} \quad (3.8)$$

Resonator L_1 's and L_2 's can be calculated by the following equation. L is less than 14.25 nH in 180 nm CMOS PDK.

$$L_0 = \frac{1}{(2*\pi*f)^2*C_1} = 46.6\text{nH} \quad (3.9)$$

3.2 Pseudocode for Power Simulation

The following pseudocodes illustrate the tuning flow of the proposed Gilbert mixer to achieve the specified center frequency ($f_c=200\text{MHz}$) and maintain a specified constant bandwidth ($BW=50\text{MHz}$).

Given: Mixer (Fig.3.1) with NMOS (W_0 to W_7), inductors (L_1 , L_2), capacitors (C_1 , C_2), resistor (R_1 , R_2), Current(I_{ds2} , I_{ds7}), and power requirement (pw_0)

Input: V_{inn} and V_{inp}

Objective: Mixer to meet the power requirement, the specified center frequency, and the bandwidth

Output: NMOS (W_0 to W_7) sizes, inductors ($L_{1's}$, $L_{2's}$), capacitors (C_1 , C_2), resistor (R_1 , R_2) values

Design approach: //Mixer meets the specified power requirement//

- 1: Specify power requirement (pw0);
- 2: Calculate I_{ds2} and I_{ds7} by pw0;
- 3: Set width of transistor $M_0, M_1, M_2, M_3, M_4, M_5$ values by $W_0 = \frac{2 * I_{ds0} * L_1}{k_n * (V_{gs0} - V_T)^2}$;
- 4: Set $W_7 = \frac{2 * I_{total} * L_7}{k_n * (V_{gs7} - V_T)^2}$;
- 5: Set $W_6 = 0.1 * W_7$;
- 6: Run DC simulation to find pw;
- 7: While (pw >= pw0)
- 8: $W_7 = 0.9 * W_7$; $W_6 = 0.9 * W_6$;
- 9: Run DC simulation to find pw;
- 10: End While; //Mixer meets the power requirement
- 11: Go to AC simulation

AC simulation: //Design flow to achieve center frequency (fc) and bandwidth (BW) requirement//

- 1: Specify fc0 and BW0;
- 2: Set initial R_1, R_2 by $\frac{CG * \pi * (R_s + \frac{1}{gm})}{2}$;
- 3: Set initial C_1, C_2 by $\frac{1}{(2 * \pi * R_1 * BW)}$;
- 4: Set initial $L_{1's}, L_{2's}$ by $\frac{1}{(2 * \pi * fc)^2 * C_1}$;
- 5: Run AC simulation; //find fc and BW

```

6:   while  $|f_c - f_{c0}| / f_{c0} > 0.03$  then //Macro adjustment of  $f_c$ 

7:   if  $f_c < f_{c0}$  then //  $f_c$  is on left of  $f_{c0}$ 

8:      $L_{1's} = 0.99 * L_{1's}$ ;

9:   else //  $f_c$  is on the right of  $f_{c0}$ 

10:     $L_{1's} = 1.01 * L_{1's}$ ;

11:   end if;

12:   Run AC simulation; //find  $f_c$  and BW

13: end while; //End of Macro adjustment of  $f_c$ 

14: while (  $|f_c - f_{c0}| / f_{c0} > 0.007$  ) or (  $|BW - BW_0| / BW_0 > 0.02$  ) then

           //Macro adjustment of BW; micro adjustment of  $f_c$ 

15:   if  $f_c < f_{c0}$  then //  $f_c$  is on left of  $f_{c0}$ 

16:      $C_1 = 0.995 * C_1$ ;

17:   else //  $f_c$  is on the right of  $f_{c0}$ 

18:      $C_1 = 1.005 * C_1$ ;

19:   end if;

20:   Run AC simulation; //find  $f_c$  and BW

21: end while; //Mixer meets the center frequency ( $f_{c0}$ ); End of macro adjustment
of BW

22: while (  $|BW - BW_0| / BW_0 > 0.002$  ) then //Micro adjustment of BW

23:   if  $BW < BW_0$  then

24:      $R_1 = 0.995 * R_1$ ;

25:   else

```

```

26:   RI=1.005*RI;

27:   end if;

28:   Run AC simulation; //find fc and BW

29:   end while; //Mixer meets the bandwidth (BW0);

```

3.3 Simulation Results

3.3.1 DC Simulation of Power Specification

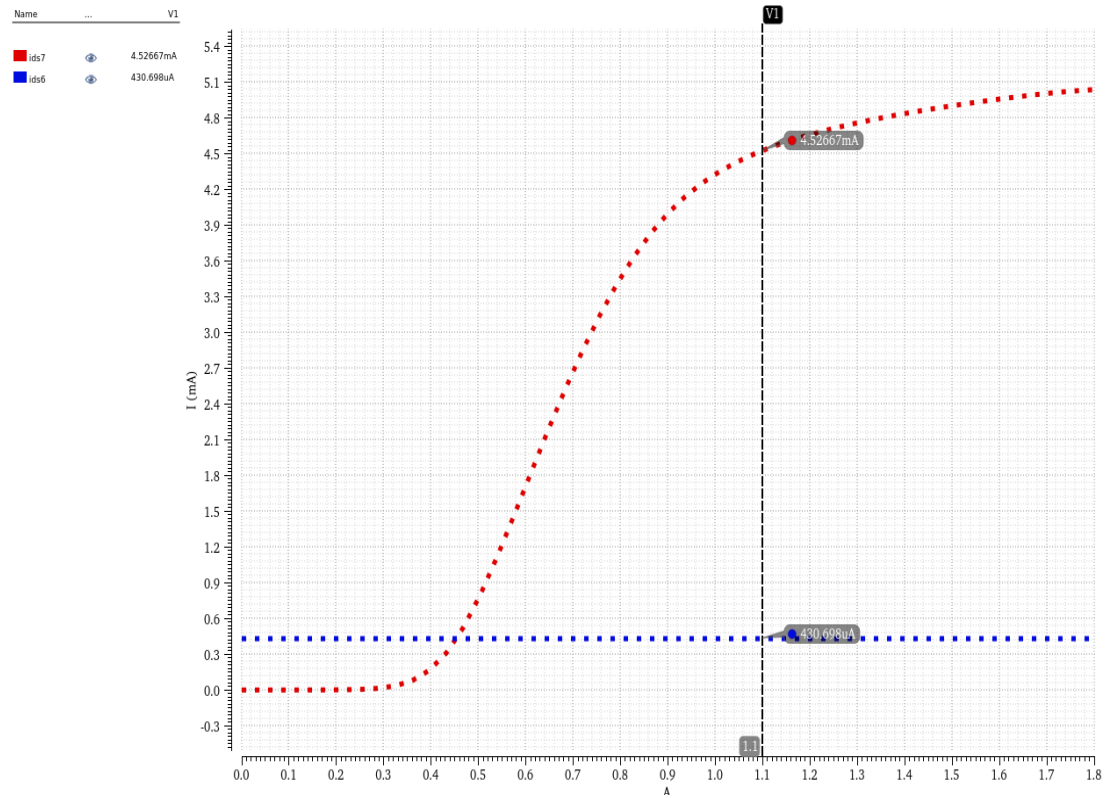


Figure 3.2 DC simulation of the proposed Gilbert mixer

Fig.3.2 shows the DC simulation result for the proposed tuning Gilbert mixer. $I_{ds7}=4.52$ mA (red), and $I_{ds6}=0.1 * I_{ds7}=0.43$ mA(blue), so the total current $I_{total}=4.95$ mA when $V_{bias} = 1.1$ V. As a result, $p_{w0} = V_{DD} * I_{total}=8.91$ mW, which meets the power specification of 9mW.

3.3.2 AC Simulation of Center Frequency and Bandwidth Specification

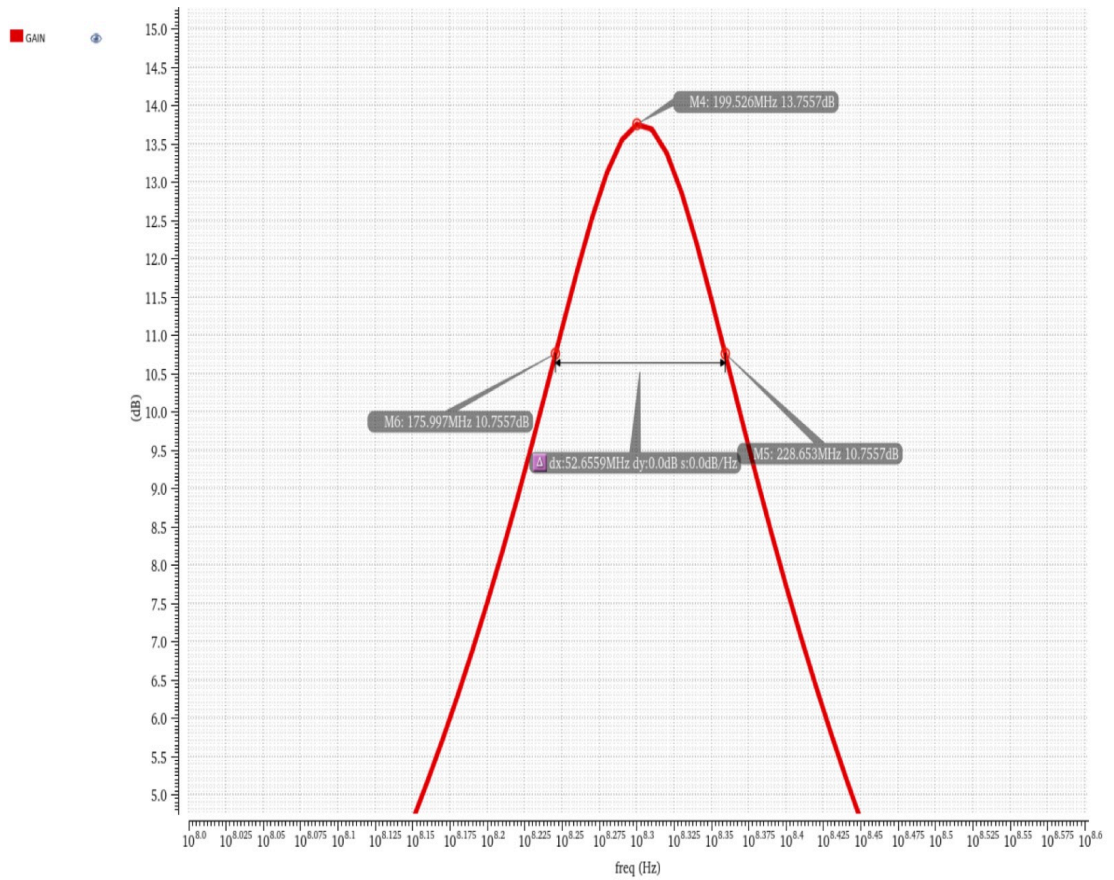


Figure 3.3 Center frequency and bandwidth of proposed Gilbert mixer

Fig.3.3 presents the output IF frequency (200MHz) and bandwidth (50MHz) simulation results for the proposed tuning Gilbert mixer. The output IF frequency $f_c=199.5$ MHz and bandwidth $BW=52.6$ MHz match the design specification. Fig. 3.4 shows the noise figure of the proposed tuning Gilbert mixer. The noise figure is 2.89dB at IF output frequency 199.5 MHz. Fig. 3.5 shows the 1-dB compression point of the proposed tuning Gilbert mixer. The 1-dB compression point is -15.191 dBm. Fig. 3.6 shows the IP3 value of the proposed tuning Gilbert mixer. The IP3 is -5.8 dBm.

3.3.3 Noise Figure

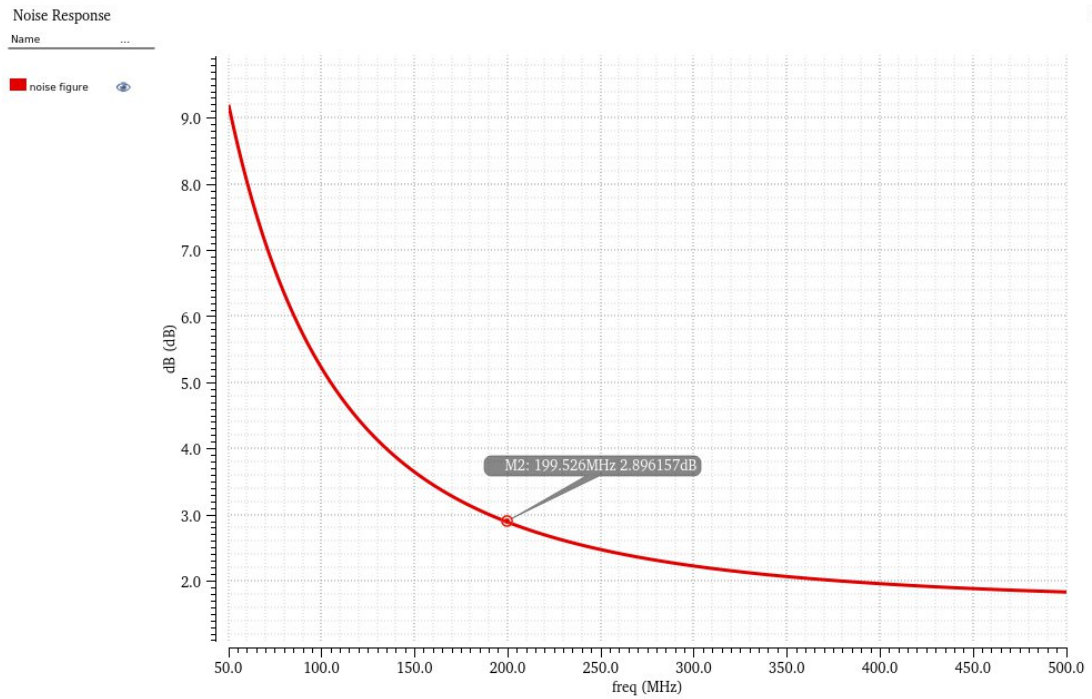


Figure 3.4 NF performance of the proposed Gilbert mixer

3.3.4 1-dB Compression Point

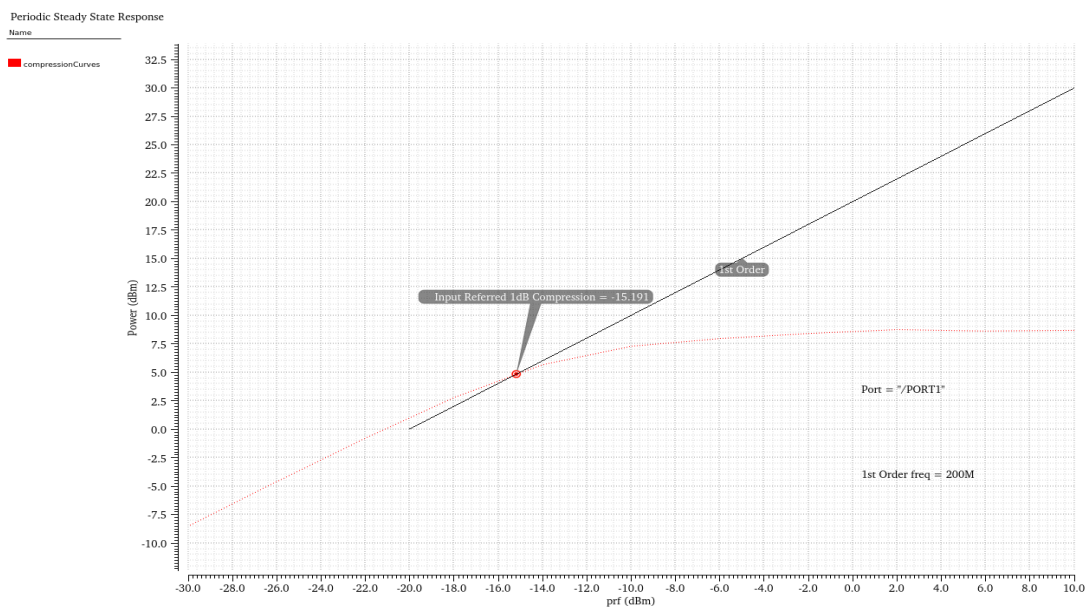


Figure 3.5 1-dB compression point performance of the proposed Gilbert mixer

3.3.5 Third-order Intercept Point (IP3)

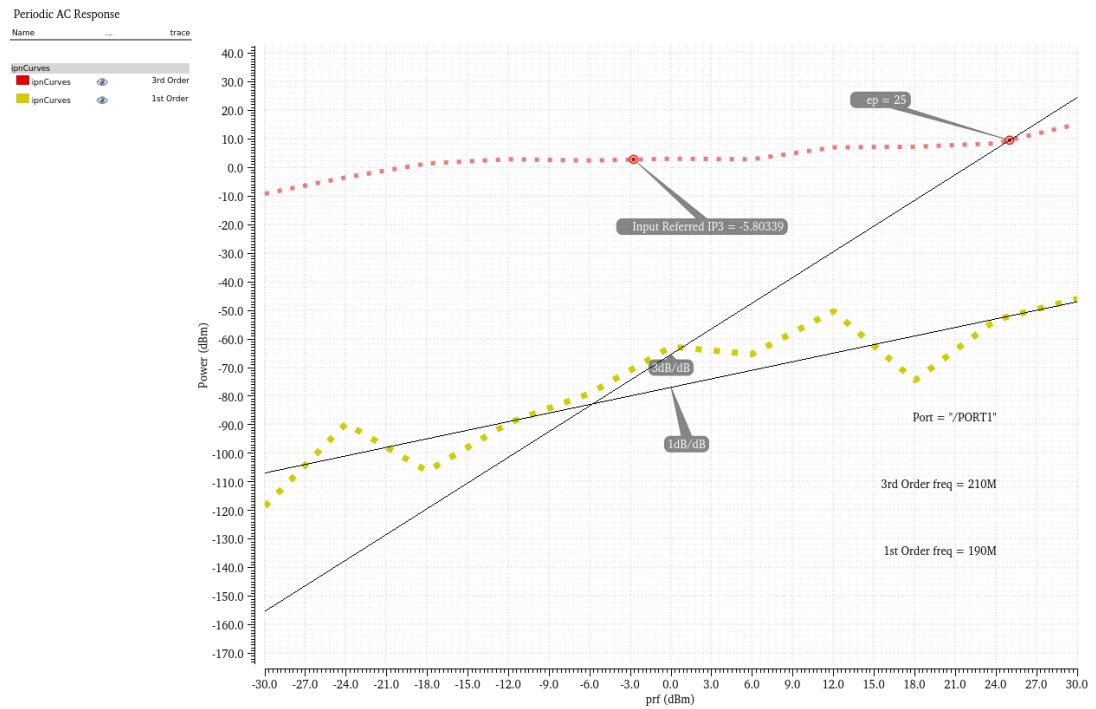


Figure 3.6 IP3 of the proposed Gilbert mixer

3.4 Gilbert Mixer Performance of Past Works

Table 3.1 Summary of Tunable Gilbert Mixer with IF (0.1GHz-1.1GHz)

RF (GHz)	LO (GHz)	IF (MHz)	BW (MHz)	Gain	NF (dB)	1-dB Compression	IIP3
1.1	2	895.3	50.02	8.7	3.7	-13.43	1.06
1.2	2	796.3	50.01	10.5	3.46	-13.29	-5.9
1.3	2	703.9	50.04	11.2	4.02	-13.05	1.09
1.4	2	602.6	50.01	12.2	3.81	-12.59	-4.27
1.5	2	501.2	50.09	12.3	4.1	-12.15	0.98
1.6	2	398.1	50.02	13.7	4.1	-11.3	0.44
1.7	2	301.9	50.08	14.2	4.5	-10.66	0.25
1.8	2	199.53	50.04	14.3	3.96	-10.79	-3.41
1.9	2	100	50.01	9.3	4.47	-10.66	-3.07
2.1	2	100	50.01	9.7	4.5	-10.66	-4.71
2.2	2	199.53	50.04	14.7	3.95	-10.88	-5.02

2.3	2	301.9	50.08	14.2	4.01	-10.76	-4.59
2.4	2	398.1	50.02	13.6	3.98	-11.3	-4.72
2.5	2	501.2	50.09	13	4.21	-12.13	-5.1
2.6	2	602.6	50.01	12.8	3.68	-12.5	-4.6
2.7	2	703.9	50.04	11.6	4.31	-13	-5.4
2.8	2	796.3	50.01	10.5	3.87	-13.32	-5.2
2.9	2	895.3	50.02	9.5	3.56	-13.46	-6.7
3	2	1000	50.01	9.2	3.96	-13.38	-7
3.1	2	1096	50	8.7	3.82	-13.52	-7.2

Table 3.1 shows the performance of a tunable Gilbert mixer designed in 180 nanometer CMOS process in transistor schematics, achieving a wide tuning range from 1.1 to 3.1 GHz and keeping constant IF bandwidth at 50 MHz. It reaches a low noise figure from 3.46 to 4.47 dB, a power of 9 mW, conversion gain from 8.7 to 14.7 dB, and a 1-dB compression point from -10.66 to -13.52 and IIP3 from 1.06 to -8.8 dB.

3.5 Comparison of Proposed Tuning Gilbert Mixer with Previous Mixer Works

Table 3.2 compares the performance of the proposed Gilbert mixer, schematics and effective prototype, and other works [3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18]. A low-power, high-linearity, and high-gain 2.4 GHz RF down conversion Gilbert mixer was introduced in [3], but its noise figure was very high (15 dB). In [4], given a fixed RF and IF, body biasing was introduced to improve linearity and noise figure (8.2dB). A low-power, good linearity common gate Gilbert down-conversion mixer was presented [5], but its noise figure was high (12.87 dB), and conversion gain was low (2 dB). A resistively degenerated wideband passive mixer was presented [6], which had a noise figure (7.7-9.5 dB) within a tuning RF frequency span (1.5-2.3 GHz). A cross-

coupled Gilbert mixer was presented [7] to cover a wideband RF (1-10 GHz), but its noise figure was high (11.3-15 dB). A self-biased mixer in CMOS 0.18 μ m for an ultra-wideband receiver was presented [8], which covers a wideband RF (1-6 GHz), but its noise figure was high (12-18 dB). A CMOS down-conversion mixer was presented [9], which covers a wideband RF (0.9-10.6 GHz), but its noise figure was high (13.1-13.8 dB). In [10], an improved double-balanced CMOS Gilbert mixer is presented with high linearity and gain but with a high noise figure (14.5 dB).

The tunable Gilbert mixer schematic design was verified in a wide tuning range from 1.1 to 3.1 GHz, keeping relatively constant IF bandwidth at 50 MHz. It achieves a low noise figure from 3.46 to 4.47 dB, a power of 9 mW, a conversion gain from 8.7 to 14.7 dB, 1-dB compression point from -10.66 to -13.52 dB, and IIP3 from 1.06 to -8.8 dB. A synthesized Gilbert mixer with effective prototype inductors, designed in 180 nanometer CMOS process, is presented with the tunability of 200 MHz IF, a constant IF bandwidth of 50 MHz, a conversion gain of 13.75 dB, a noise figure of 2.89 dB, 1-dB compression point of -15.19 dBm, IIP3 of -5.8 dBm, and a power of 9 mW.

Table 3.2 Comparison of the Proposed Tuning Gilbert Mixer with Previous Mixer

Works

	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	Mixer Schematics	Effective Prototype
CMOS (nm)	180	130	180	180	130	180	250	180	350	180	180	180
VDD (V)	1.8	1.2	1.8	1.8	1.2	1.8	1.8	1.8	1.2	1.8	1.8	1.8
RF (GHz)	2.4	2.4	2.4	1.55 ~2.3	1~10	1~6	0.9 ~ 10.6	-	0.9	2.4	1.1~ 3.1	2.2

LO (GHz)	2.25	-	0.3	-	-	-	-	-	0.8	2.3	2	2
IF (MHz)	150	50	210 0	-	100~ 1000	170	-	-	100	100	100~ 1100	200
BW (MHz)	-	-	-	-	-	-	-	-	-	-	50	50
CG (dB)	6.78	13.8	2	22.5 ~ 25	3~8	13 ~10		17.8	0.52	25	8.7~ 14.7	13.75
NF (dB)	15	8.2	12.8 7	7.7 ~ 9.5	11.3~ 15	12 ~ 18	13.1~13 .8	14.5	24.3	9.62	3.46~ 4.47	2.89
1-dB (dBm)	-10	-	2	-	-	-	-8	10.2	-8	-24.96	-10.66 ~ -13.52	-15.19
IIP3 (dBm)	-1	-4	12.7 4	>= 7	-7 ~ -4	-4.5	-4	-	1.2	-17.7	1.06 ~ -8.8	-5.8

Chapter 4: TUNABLE MIXER LAYOUT INDUCTOR LOSS AND EQUIVALENT ELECTRONIC CIRCUIT ANALYSIS

4.1 Layout Design, Verification, and Simulation Flow

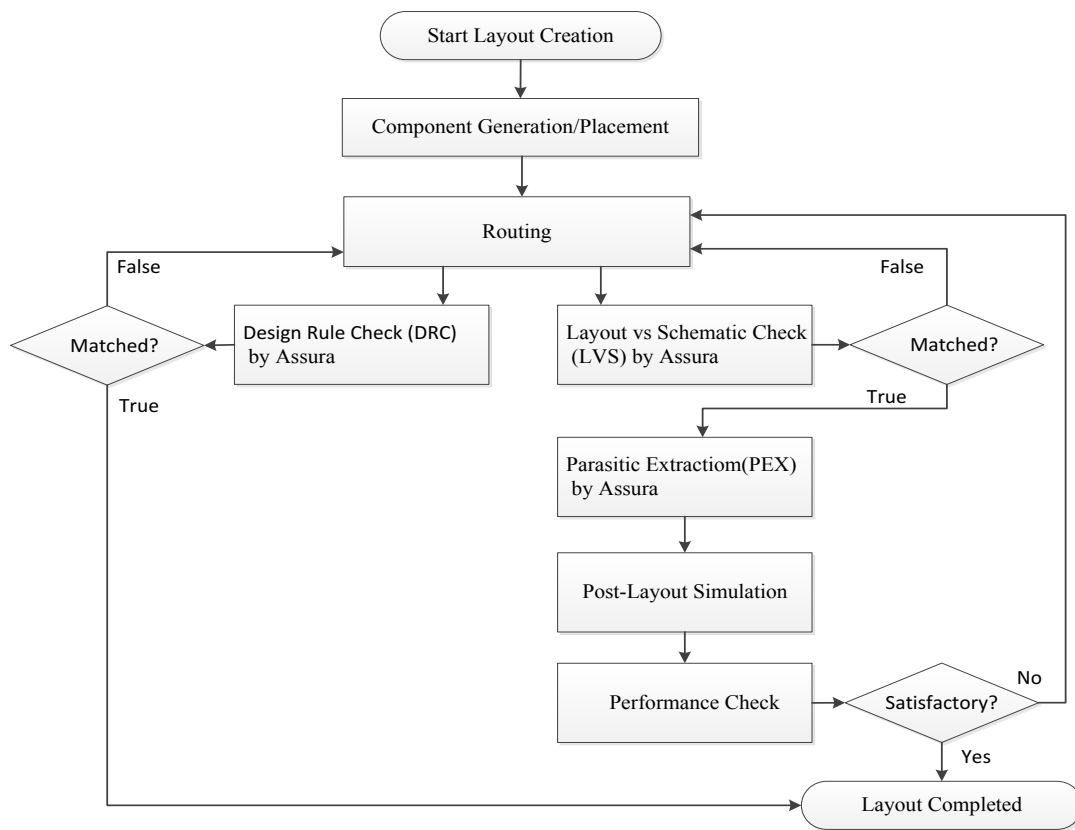


Figure 4.1 Design rule check and parasitic extraction flow

The layout design rule check and parasitic extraction flow are shown in Fig. 4.1. To start layout design, build schematic and symbol view first. Next, generate electronic layout components from the schematic, identify components, and then decide where to place all electronic components in a generally limited amount of space. Next is routing, choosing the exact design of all the wires needed to connect the placed components.

Connecting components based on the schematic view. After routing, verify if the layout follows design rules by Design Rule Check (DRC). Check and correct any routing errors based on the design rule file report. For example, if the layout passes the DRC check, conduct a layout versus schematic (LVS) check. If there are any LVS errors, then check electronic components to see if they are correctly connected or not. Conduct Assura Quantus until LVS passes for parasite extraction and include all parasites in the post-layout simulation. Finally, verify the post-layout performance, and go back to the layout circuit to optimize the placement and route until desirable performance is achieved.

The layout of a tunable mixer operating at output IF = 200MHz, and BW = 50 MHz is shown in Fig. 4.2.

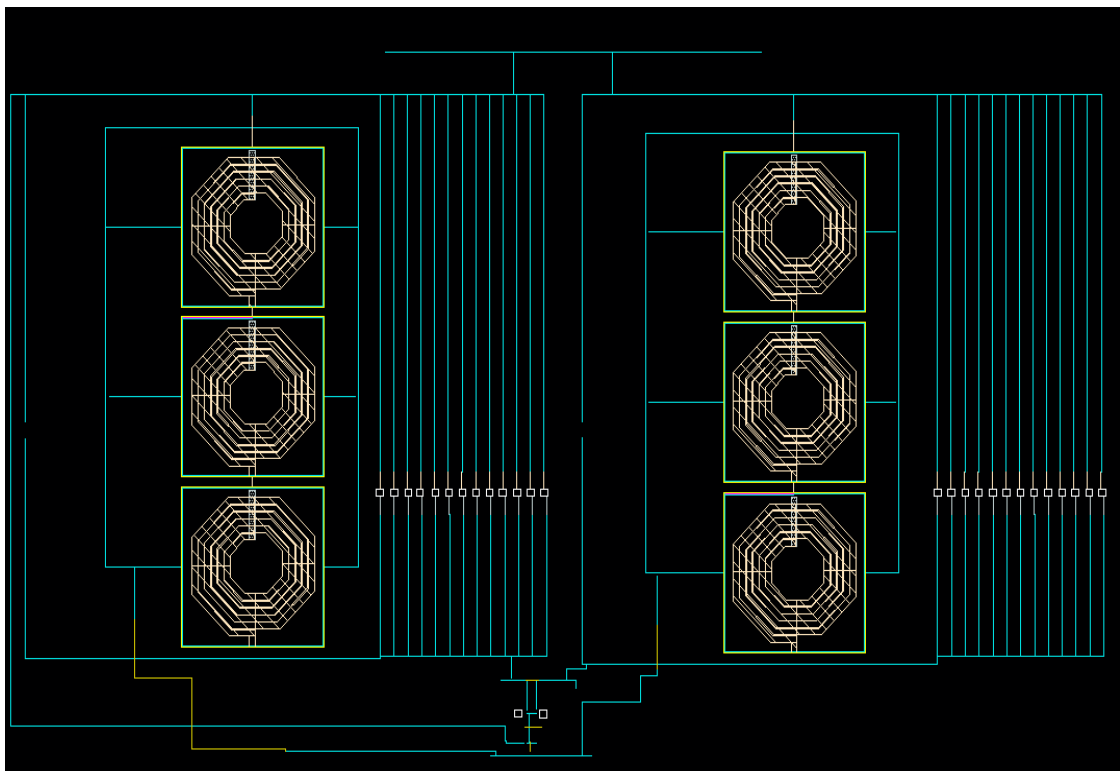


Figure 4.2 Layout of a tunable mixer operating at IF=200MHz and BW=50MHz

4.2 Layout Design Approach

The layout design is generated from the schematic in section.3.1 with the same case ($PW_0 < 9$ mW, $f_c=200$ MHz, and $BW=50$ MHz). Two layout design optimization flowcharts will be presented in Fig.4.3 and Fig.4.4 to explain how to meet specified PW_0 , f_c , and BW .

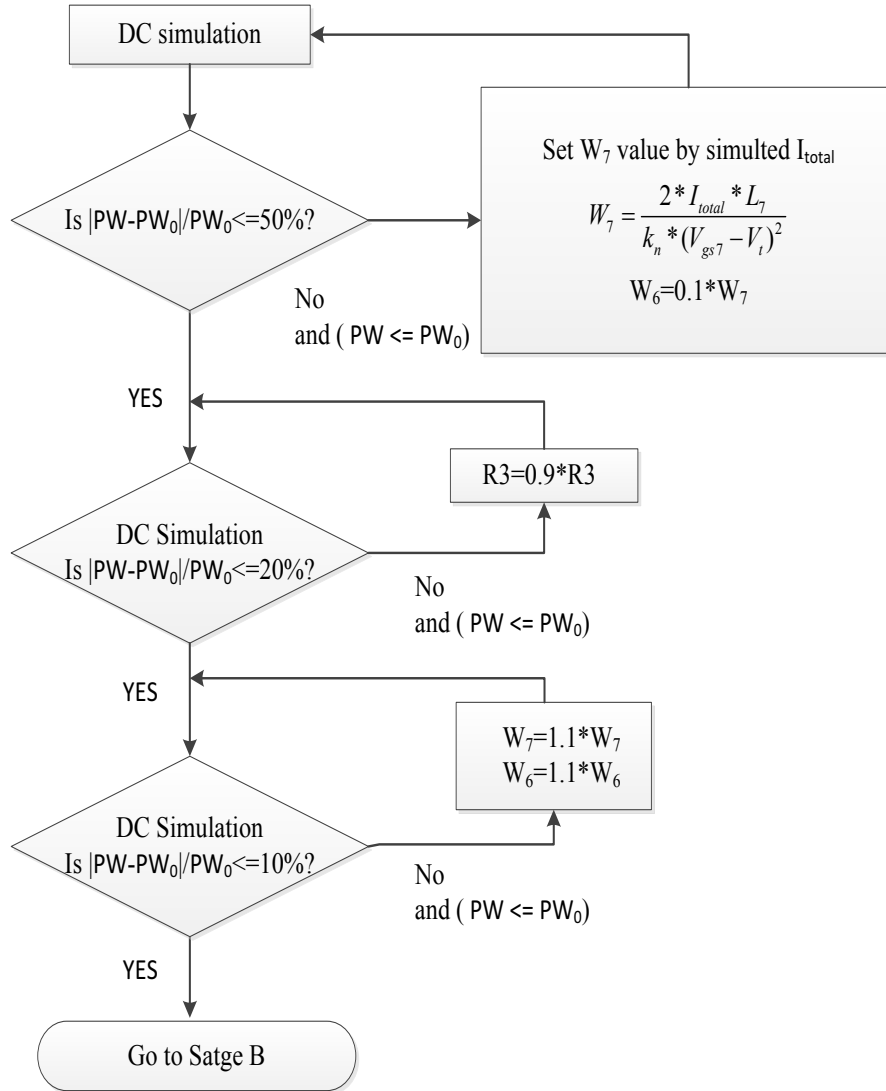


Figure 4.3 Design flow of power optimization

In design stage A (Fig.4.3), PW_0 is optimized to meet power specifications. The layout is generated from the schematic. Keep all sizes are same as the schematic. If the

error ratio of $PW0 > 50\%$, substitute the simulated I_{ds7} into (3.1) to get new W_7 and W_6 values. Using the new W_7 and W_6 to do DC simulation. If $|PW - PW0|/PW0 > 20\%$, decrease R_3 by setting $R_3 = 0.9 * R_3$ in the recursive loop until $|PW - PW0|/PW0 \leq 20\%$. Do DC simulation if $|PW - PW0|/PW0 > 10\%$, W_7 , and W_6 by setting $W_7 = 1.1 * W_7$ and $W_6 = 1.1 * W_6$ in the recursive loop. Repeat the process until $|PW - PW0|/PW0 \leq 10\%$. After the max power condition is met, go to design stage B (Fig. 4.4) to optimize the mixer design to meet center frequency (f_c) and constant IF bandwidth ($BW0$) requirements.

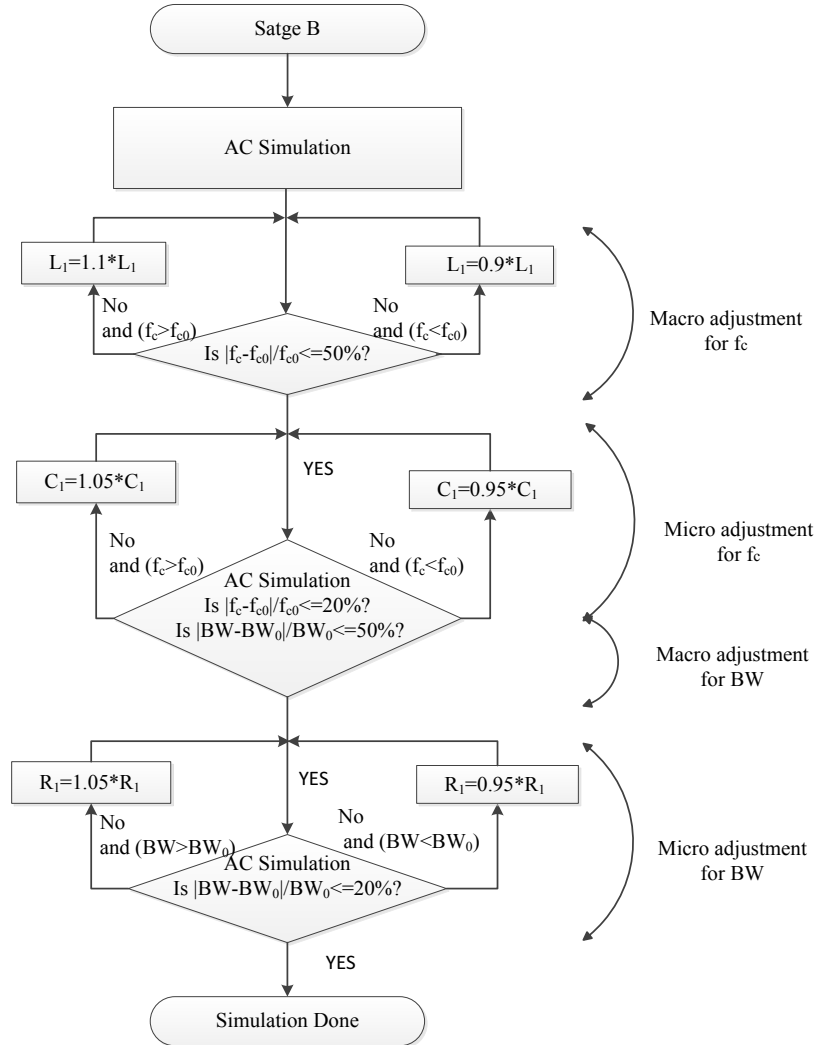


Figure 4.4 Design flow of f_c and $BW0$ optimization

At the beginning of design stage B (Fig.4.4), Conduct AC simulation based on the V_{bias} found in DC simulation of stage A. Since the f_c of the layout differs from the f_c of the schematic due to inductance loss, a macro adjustment of f_c is conducted in design stage B. If the error ratio of f_c is more than 50% and the simulated center frequency is smaller than the specified value, then decrease L_1 by multiplying 0.9. Repeat the same procedure until the error ratio of f_c is smaller than 50%. As a result, the macro corrections for center frequency are completed. Set $L_2 = L_1$ in the design stage B.

Next, conduct AC simulation for micro adjustment of f_c and macro adjustment of BW. If the error ratio of f_c exceeds 20%, the error ratio of BW is more than 50%, and the simulated center frequency is smaller than the specified value, then decrease C_1 by multiplying 0.95. Repeat the same process until the error ratio of f_c is less than 20% and the error ratio of BW is less than 50%. Micro corrections to f_c and macro corrections to BW are completed. Set $C_2 = C_1$ in design stage B.

Perform an AC simulation for micro correction of BW to be closest to BW_0 . If the error ratio of BW is more than 20% and the simulated bandwidth is smaller than the specified value, then decrease R_1 by multiplying 0.95. If the error ratio of BW is more than 20% and the simulated bandwidth is more significant than the specified value, then increase R_1 by multiplying 1.005. Repeat the same process until the error ratio of BW is less than 20%. The micro corrections to BW have been completed. Set $R_2 = R_1$ in design stage B.

4.3 Example of f_{c0} (200 MHz) with a Controllable BW_0 (50 MHz)

For layout design, all transistors' sizes are generated from the schematic. Based on the DC simulation, $I_{ds7}=1.54\text{mA}$ and $I_{ds6}=0.16\text{mA}$. Both values are much less than I_{ds6} and I_{ds7} from schematic DC simulation. Increase W_7 in layout to increase I_{ds7} . Increase I_{ds6} by increasing $W_6=0.1W_7$. Maintain the size as a schematic for W_0 to W_5 . Set $W_0=W_1=W_2=W_3=W_4=W_5=132\mu\text{m}$, $W_7=25\mu\text{m}$ and $W_6=0.1*W_7=2.5\mu\text{m}$. Performing DC analysis, and if the power error ratio is more than 20%, keep decreasing R_3 until the power error ratio is less than 20%. Continue to do DC analysis to check whether the power error ratio is less than 10%. If the error ratio is more than 10%, optimize the transistors' width to meet the power requirement. After the optimization process is complete, W_7 is increased to $45\mu\text{m}$, and W_6 is increased to $4.5\mu\text{m}$. Then, go to design stage B (Fig. 4.4).

$f_c=12.27\text{ MHz}$ and $BW=44.67\text{ MHz}$ are generated from AC simulation for macro adjustment of f_c . Since the error ratio of f_c is more than 50% and the simulated center frequency is smaller than the specified value, both L_1 and L_2 are set to 28.5nH . Following the AC simulation, f_c is determined to equal 12.3 MHz , and BW is determined to be 47.19 MHz .

Next, conduct AC simulation for micro-adjustment of f_c to be closest to f_{c0} and macro adjustment of BW . Since the error ratio of f_c exceeds 20% and BW already meets requirements, C_1 and C_2 are reduced to 11pF . Conduct an AC simulation and obtain $f_c=13.49\text{ MHz}$ and $BW=52.75\text{ MHz}$, which meet the error ratio of bandwidth less than 50%. The macro corrections to BW are completed.

Finally, conduct AC simulation for micro-adjustment of BW to be closest to BW0.

R_1 and R_2 are increased to $15.7\text{k}\Omega$. Run an AC simulation, $f_c = 13.48\text{ MHz}$ and $BW = 49.5\text{ MHz}$, which meets the error ratio of bandwidth below 20%. The micro corrections to BW have been completed. In this case, the error ratio of f_c does not meet the requirement, so the macro correction to f_c is not completed. A solving method will be introduced in Section 4.5.

4.4 Layout Performance Analysis

4.4.1 DC Simulation of Power Specification

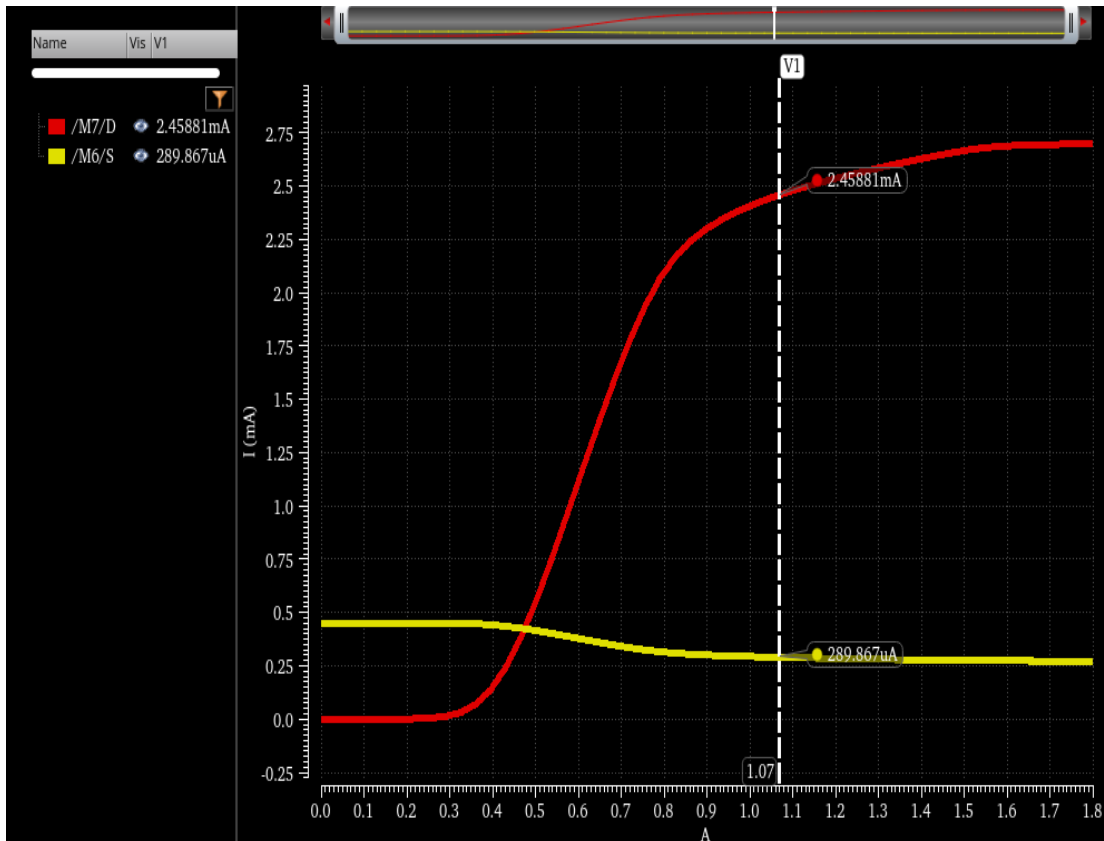


Figure 4.5 DC simulation of power specification

Fig.4.5 shows the DC simulation results for the proposed tuning Gilbert mixer layout power specification. $I_{ds7}=2.45\text{ mA}$ (red), and $I_{ds6}=0.1 * I_{ds7}=0.28\text{mA}$ (yellow), so

the total current $I_{\text{total}}=2.73 \text{ mA}$ when $V_{\text{bias}}=1.07\text{V}$. As a result, $p_{\text{w0}}=V_{\text{DD}}*I_{\text{total}}=4.91\text{mW}$, which meets the power specification of 9mW .

4.4.2 AC Simulation of Center Frequency and Bandwidth Specification

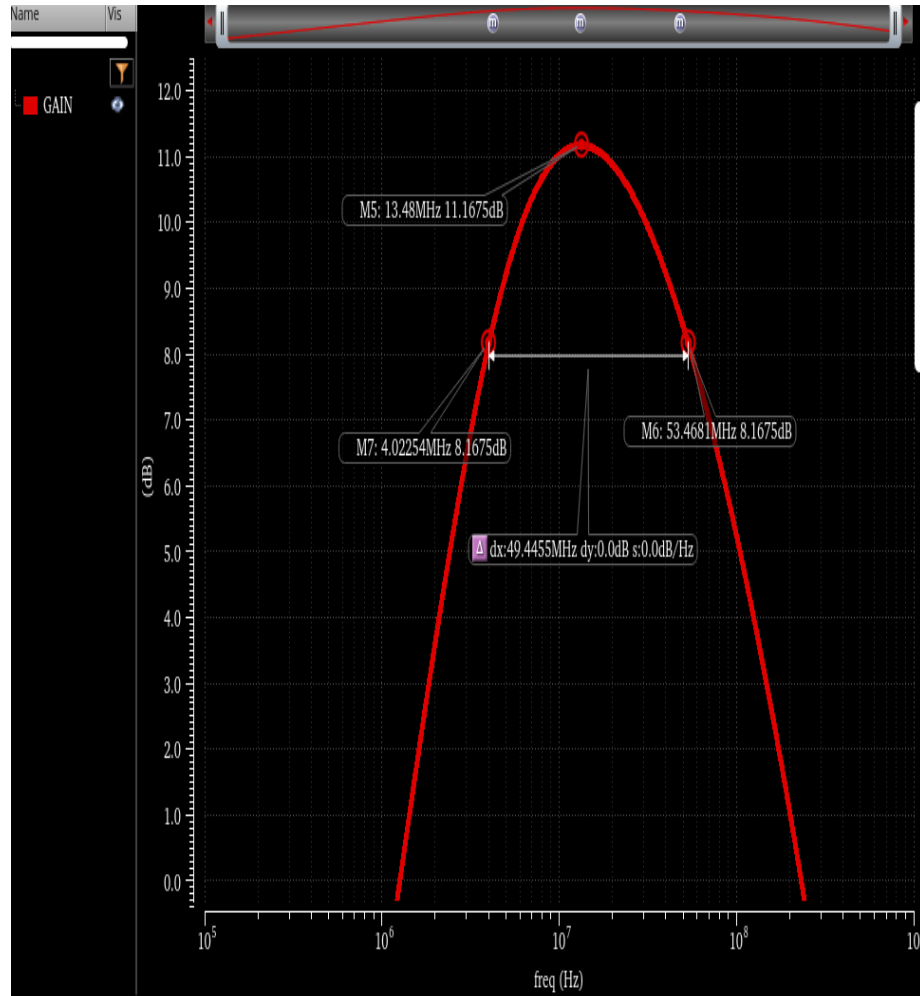


Figure 4.6 AC simulation of center frequency and bandwidth specification

Fig.4.6 shows the output IF frequency (200MHz) and bandwidth (50MHz) simulation results for the proposed tuning Gilbert mixer layout. As a result, the output IF frequency $f_{c0}=13.48 \text{ MHz}$ and bandwidth $BW_0=49.45 \text{ MHz}$, which the bandwidth meets the design specification.

4.5 Effective Prototype Inductance in the Tunable Mixer Design

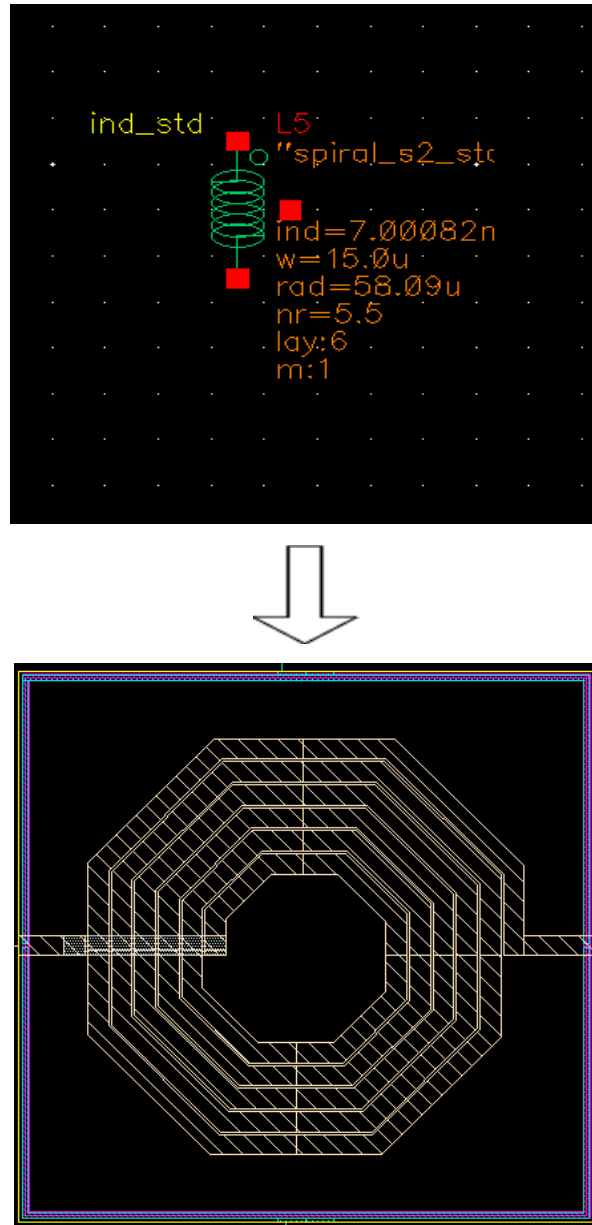


Figure 4.7 Effective prototype square planar inductor and layout ($L=7.00082\text{nH}$)

In this work, the layout of the tunable mixer center frequency f_c does not meet the requirement of $|f_c - f_{c0}|/f_{c0} < 20\%$. The main reasons are mainly due to 1) layout effects due to the substrate, and 2) the resistive loss of the layout inductor often affects the center frequency and bandwidth after it is prototyped [19]. The effective prototype inductor inductance is 7.00082 nH, where the layout is designed by controlling the

inductor width, space, radius, and the number of turns, as shown in Fig. 4.7. The effective prototype inductance is measured as 7.00082 nH at 902.409MHz; the corresponding effective layout inductance is measured as 173.1692 pH at 902.409MHz in Fig.4.8. A significant inductance loss is observed. Later, we will present a methodology to offset the tunable mixer center frequency offset problem due to the difference between the effective prototype inductance and the layout inductance value.

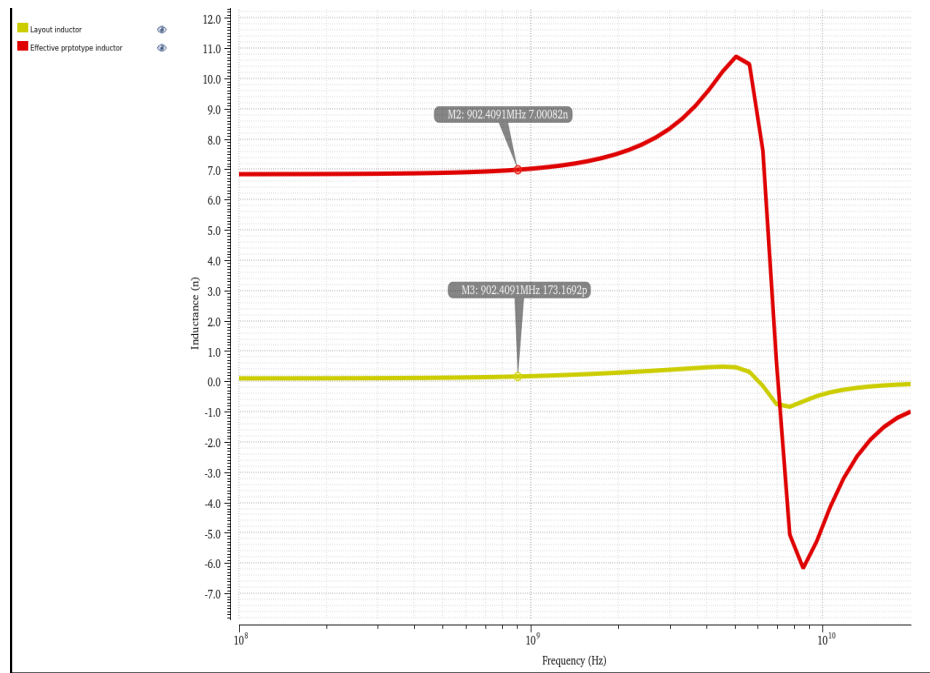


Figure 4.8 Effective prototype inductance (Red) vs. Layout inductance (Yellow)

4.6 Equivalent Electronic Circuit for the Square Planar Inductor

The issue of modeling the inductor for RF applications is complex because it requires knowing the causes of undesirable behavior in the correlation between the circuit and the analytical model. This contribution presents an equivalent electronic circuit attributed to the cause of the degraded performance of the inductor [20]. An equivalent electronic circuit for the square planar inductor is analyzed in Fig. 4.9.

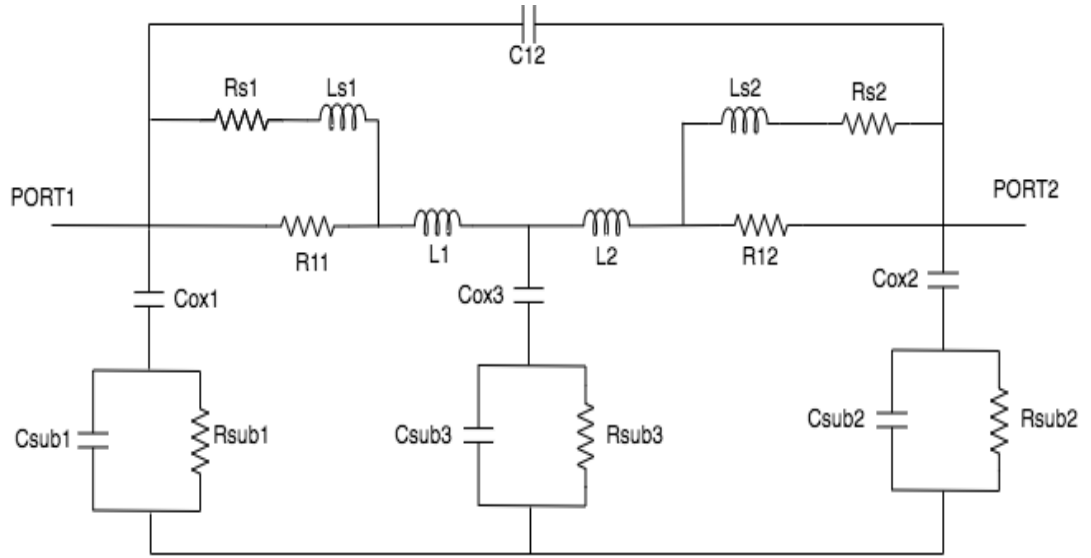


Figure 4.9 Equivalent electronic circuit for the square planar inductor.

Fig. 4.10 shows the simulation of the equivalent electronic circuit obtained and the experimental response.

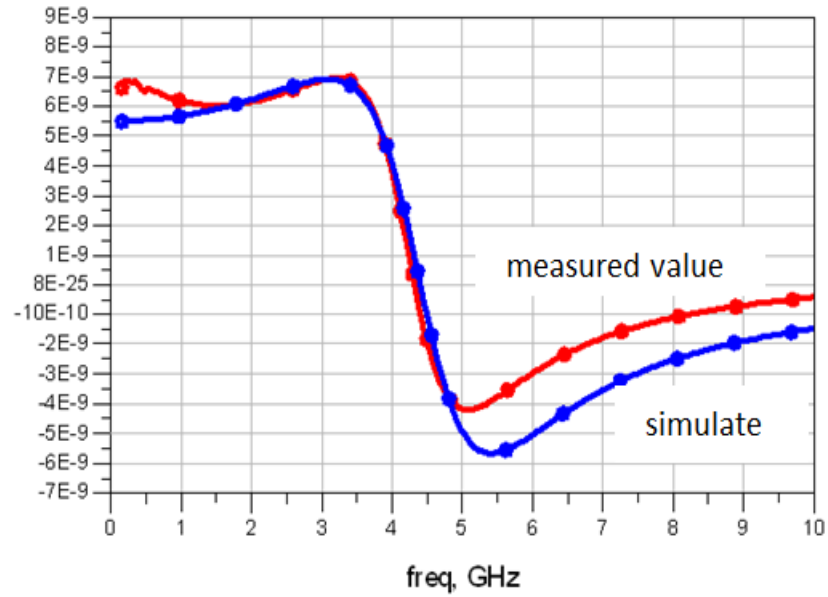


Figure 4.10 Experimental curve vs. equivalent electronic circuit simulated[20]

As shown in Fig. 4.10, a close correlation between experimental and equivalent electronic circuits is observed in the range of 1.5-4.75 GHz; self-resonance is observed in its upper-frequency band. Next, we use this equivalent circuit (π -model) to substitute

the ideal inductor in the tunable mixer schematic of Fig. 4.11 to restore the extracted inductor value to reduce inductance loss. Fig.4.12 shows the tunable Gilbert mixer implemented with an equivalent electronic circuit (π -model). Port 1 of the π -model circuit is connected to V_{DD} , and port 2 is connected to the outputs OUTN and OUTP of the mixer. The setting of all parameters ($L_1, L_2, L_{S1}, L_{S2}, R_{S1}, R_{S2}, R_{I1}, R_{I2}, R_{sub1}, R_{sub2}, R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}$) of an equivalent electronic circuit (π -model) will be introduced in section 4.6.1.

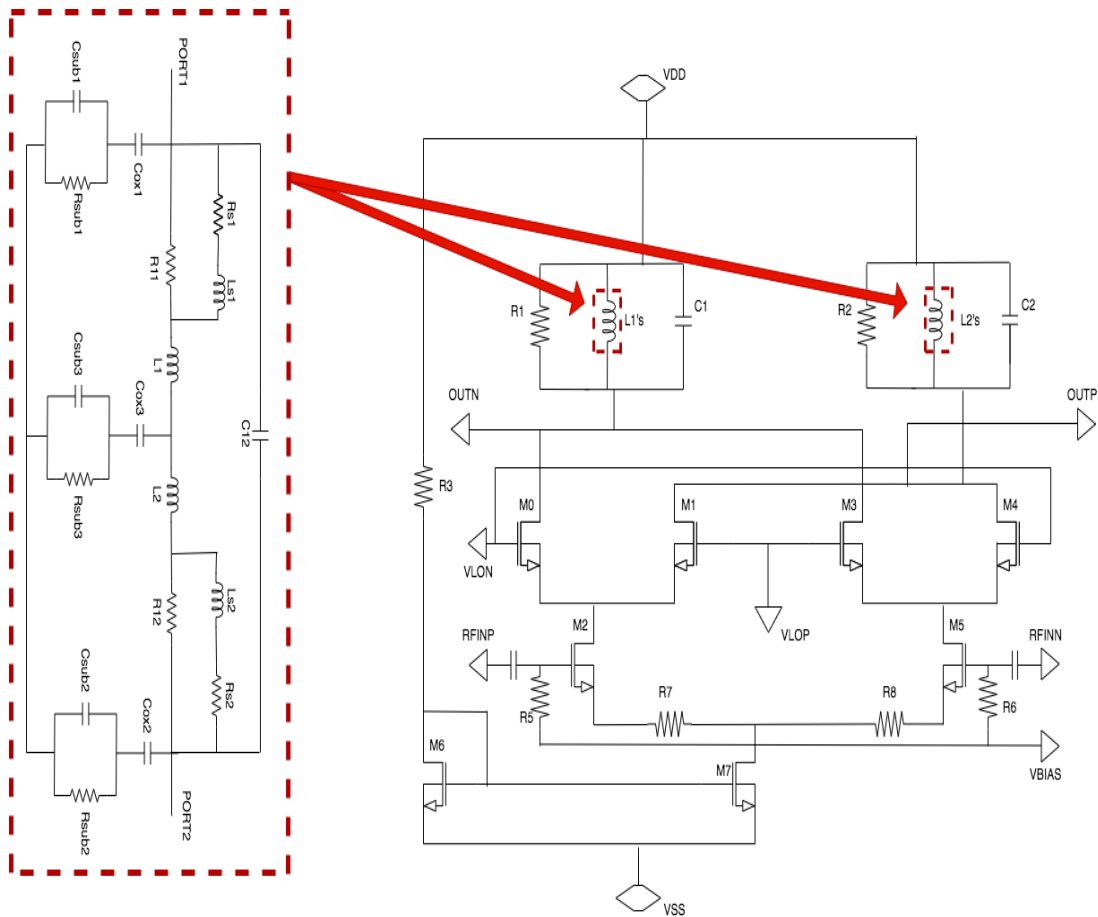
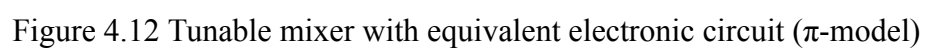


Figure 4.11 π -model implementation in the tunable mixer



4.6.1 AC Simulation

AC simulation: //Mixer design flow to achieve center frequency and the bandwidth requirement //

- 1: Specify f_{c0} and BW_0 ;
- 2: Set initial $R_1 (=R_2)$ by $\frac{CG*\pi*(R_s+\frac{1}{gm})}{2}$;
- 3: Set initial $C_1 (=C_2)$ by $\frac{1}{(2*\pi*R_1*BW)}$;
- 4: Find $L_{S1}, L_{S2}, R_{S1}, R_{S2}, R_{I1}, R_{I2}, R_{sub1}, R_{sub2}, R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}, C_{Sub3}, C_{I2}$ based on layout extracted results
- 5: Set initial $L_1 (=L_2)$ based on C_1 and C_2 ;
- 6: do // Check on L_1 from the lookup table.
- 7: Find ($L_{S1}, L_{S2}, R_{S1}, R_{S2}, R_{I1}, R_{I2}, R_{sub1}, R_{sub2}, R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}, C_{Sub3}, C_{I2}$) according to L_1 in the lookup table
- 8: Run AC simulation; //find f_c and BW
- 9: if ($f_c \leq f_{c0}$) { // f_c is on left of f_{c0}
- 10: Decrease L_1 according to the lookup table ;
- 11: else // f_c is on the right of f_{c0}
Increase L_1 according to the lookup table ;
}
- 12: while $|f_c - f_{c0}| / f_{c0} > 30\%$ //Macro adjustment of f_c
- 13: Run AC simulation; //find f_c and BW
- 14: while ($|f_c - f_{c0}| / f_{c0} > 20\%$) or ($|BW - BW_0| / BW_0 > 30\%$) then

```

//Macro adjustment of BW; micro adjustment of fc

15:  if  $f_c < f_{c0}$  then //fc is on left of  $f_{c0}$ 

16:     $C_1 = 0.995 * C_1$ ;

17:  else //fc is on the right of  $f_{c0}$ 

18:     $C_1 = 1.005 * C_1$ ;

19:  end if;

20:  Run AC simulation; //find  $f_c$  and BW

21:  end while; //Mixer meets the center frequency ( $f_{c0}$ ); End of macro adjustment
      of BW

22:  while (  $|BW - BW_0| / BW_0 > 20\%$  ) then //Micro adjustment of BW

23:    if  $BW < BW_0$  then

24:       $R_1 = 0.995 * R_1$ ;

25:    else

26:       $R_1 = 1.005 * R_1$ ;

27:    end if;

28:    Run AC simulation; //find  $f_c$  and BW

29:  end while; //Mixer meets the bandwidth ( $BW_0$ );

```

4.6.2 Design Approach

Set initial values of C_1 , C_2 , R_1 , R_2 based on the calculation values. Find L_{S1} , L_{S2} , R_{S1} , R_{S2} , R_{11} , R_{12} , R_{sub1} , R_{sub2} , R_{sub3} , C_{ox1} , C_{ox2} , C_{ox3} , C_{Sub1} , C_{Sub2} , C_{Sub3} , C_{12} based on layout extracted. Create a table to list all L_{S1} , L_{S2} , R_{S1} , R_{S2} , R_{11} , R_{12} , R_{sub1} , R_{sub2} ,

$R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}, C_{Sub3}, C_{12}$ values based on corresponding instance values. Perform an AC simulation to determine the first corresponding center frequency f_c . Next, a macro-adjustment of f_c is conducted. For example, if the error ratio of f_c is more than 30% and the simulated center frequency is smaller than the specified value, then decrease L_1 by setting new $L_{S1}, L_{S2}, R_{S1}, R_{S2}, R_{11}, R_{12}, R_{sub1}, R_{sub2}, R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}, C_{Sub3}, C_{12}$. If the error ratio of f_c is more than 30% and the simulated center frequency is larger than the specified value, then increase L_1 by setting new $L_{S1}, L_{S2}, R_{S1}, R_{S2}, R_{11}, R_{12}, R_{sub1}, R_{sub2}, R_{sub3}, C_{ox1}, C_{ox2}, C_{ox3}, C_{Sub1}, C_{Sub2}, C_{Sub3}, C_{12}$. Continue the same process until the error ratio of f_c is less than 30%. The macro correction has been completed for f_c .

Continue to conduct AC simulation. For example, suppose the error ratio of f_c is more than 20%. In that case, the error ratio of BW is more than $> 30\%$, and the simulated center frequency is smaller than the specified value, then decreases C_1 by multiplying 0.995. Suppose the error ratio of f_c is more than 20%. In that case, the error ratio of BW is more than 30%, and the simulated center frequency is larger than the specified value, then increase C_1 by multiplying 1.005. Continue the same process until the error ratio of f_c is less than 20% and the error ratio of BW is less than 30%. The micro correction has been completed for f_c , and the macro correction has been completed for BW. Set $C_2=C_1$.

Conduct an AC simulation to micro correction BW to be closest to BW_0 . If the error ratio of BW is more than 20% and the simulated bandwidth is smaller than the

specified value, then decrease R_1 by multiplying 0.99. If the error ratio of BW is more than 20% and the simulated bandwidth is larger than the specified value, then increase R_1 by multiplying 1.005. Continue the same process until the error ratio of BW is less than 20%. The micro correction has been completed for BW, Set $R_2=R_1$.

4.6.3 Proposed Mixer with Equivalent Electronic Circuit Performance

Fig.4.13 shows the DC simulation results for the proposed mixer with equivalent electronic circuit power specifications. $I_{ds7}=4.12$ mA (red), and $I_{ds6}=0.1 * I_{ds7}=0.45$ mA (blue), so the total current $I_{total}=4.57$ mA when $V_{bias}=1.1$ V. As a result, $pw0 = V_{DD} * I_{total} = 8.23$ mW, which meets the power specification of 9mW.

Fig.4.14 shows the output IF frequency (200MHz) and bandwidth (50MHz) simulation results for the proposed mixer with an equivalent electronic circuit. As a result, the output IF frequency $f_c=177.8$ MHz and bandwidth $BW=87.6$ MHz. Compared with the prototype layout Gilbert mixer circuit, the equivalent π -model tunable mixer optimizes the IF center frequency from 13.48 MHz to 177.8 MHz for the IF=200 MHz case and meets the requirement of $|f_c-f_{c0}|/f_{c0} < 20\%$. The conversion gain is dropped from 13.75 dB to 7.4dB compared with the prototype Layout Gilbert mixer circuit. From the above comparison, the equivalent π -model tunable mixer has resolved the center frequency offset problem in the tunable mixer with prototype L. Still, the conversion gain drops by approximately 3dB. In section 6.1, a low noise high gain mixer will be introduced to optimize the mixer's gain.

As shown in Fig. 4.15, the noise figure of the proposed tuning Gilbert mixer with an equivalent electronic circuit is simulated. The noise figure is 3.14 dB at IF output frequency 177.8 MHz. Fig. 4.16 illustrates the 1-dB compression point of the proposed tuning Gilbert mixer with an equivalent electronic circuit. The 1-dB compression point is -17.18 dBm. Fig. 4.17 shows the IP3 value of the proposed tuning Gilbert mixer with an equivalent electronic circuit. The IP3 is -19.81 dBm.

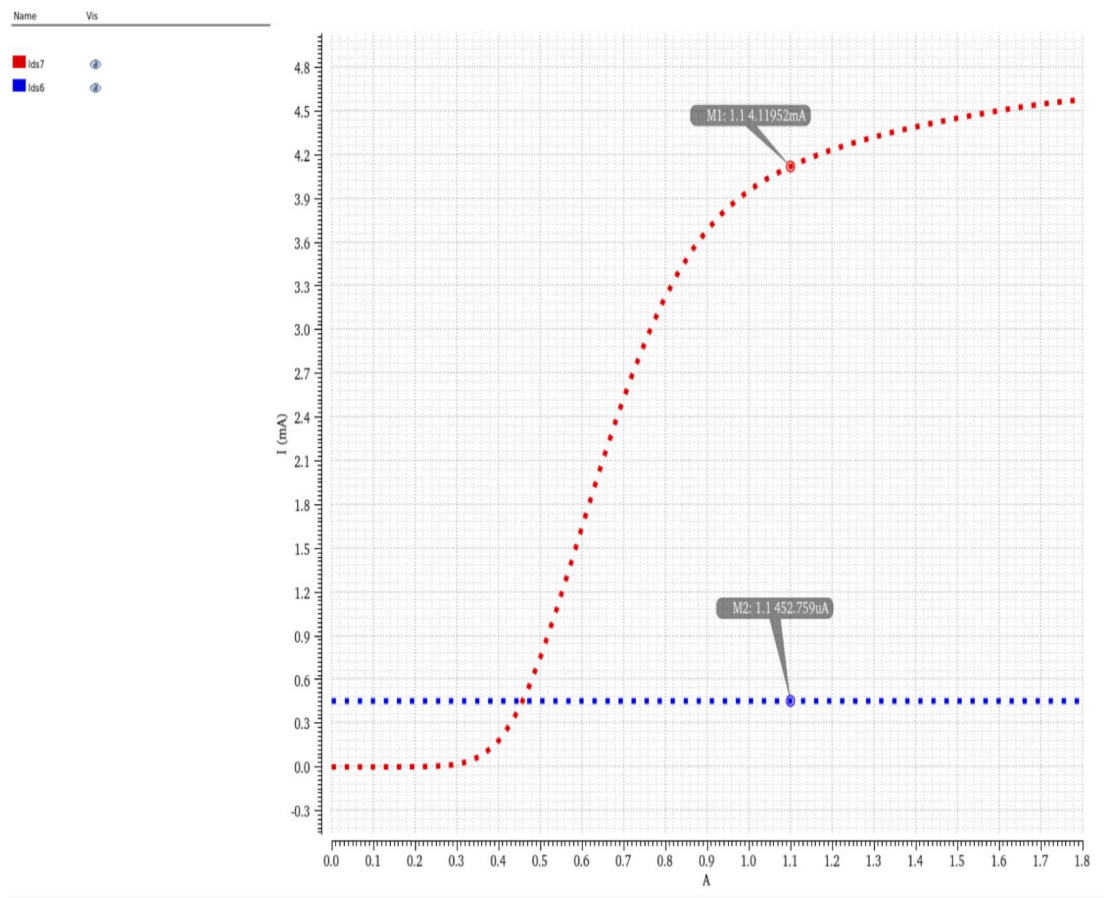


Figure 4.13 DC simulation of the equivalent π -model tunable mixer

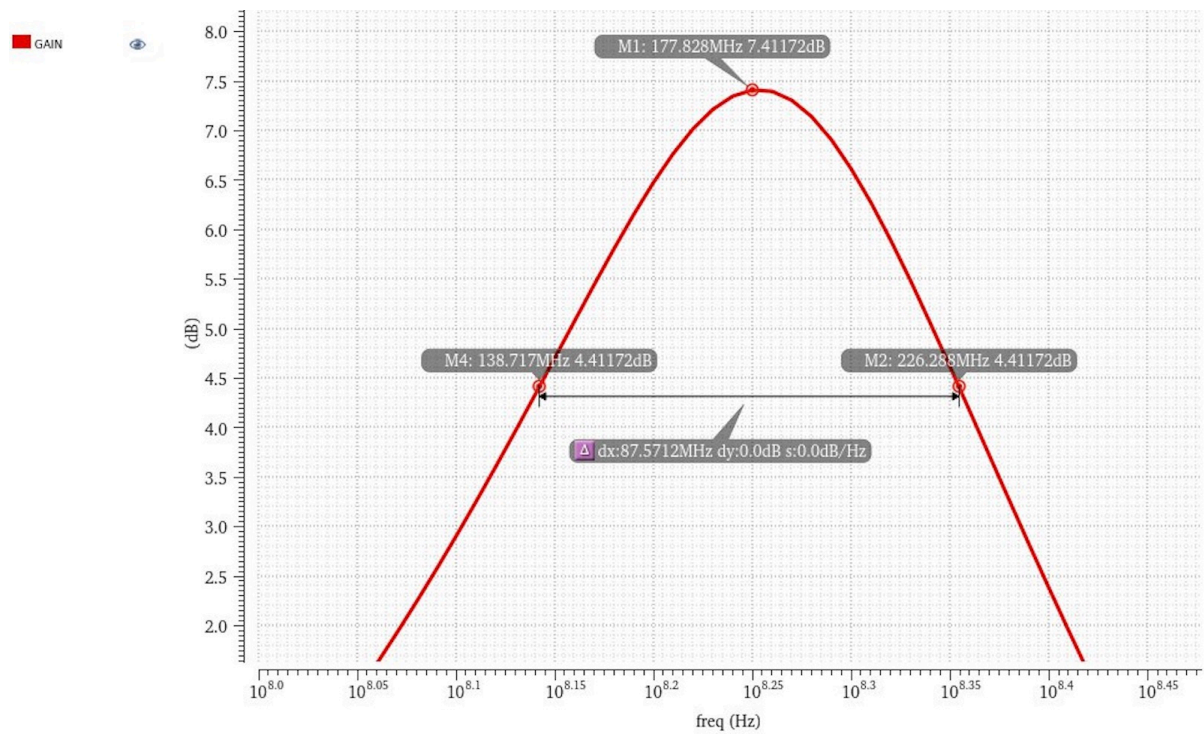


Figure 4.14 AC simulation of the equivalent π -model tunable mixer

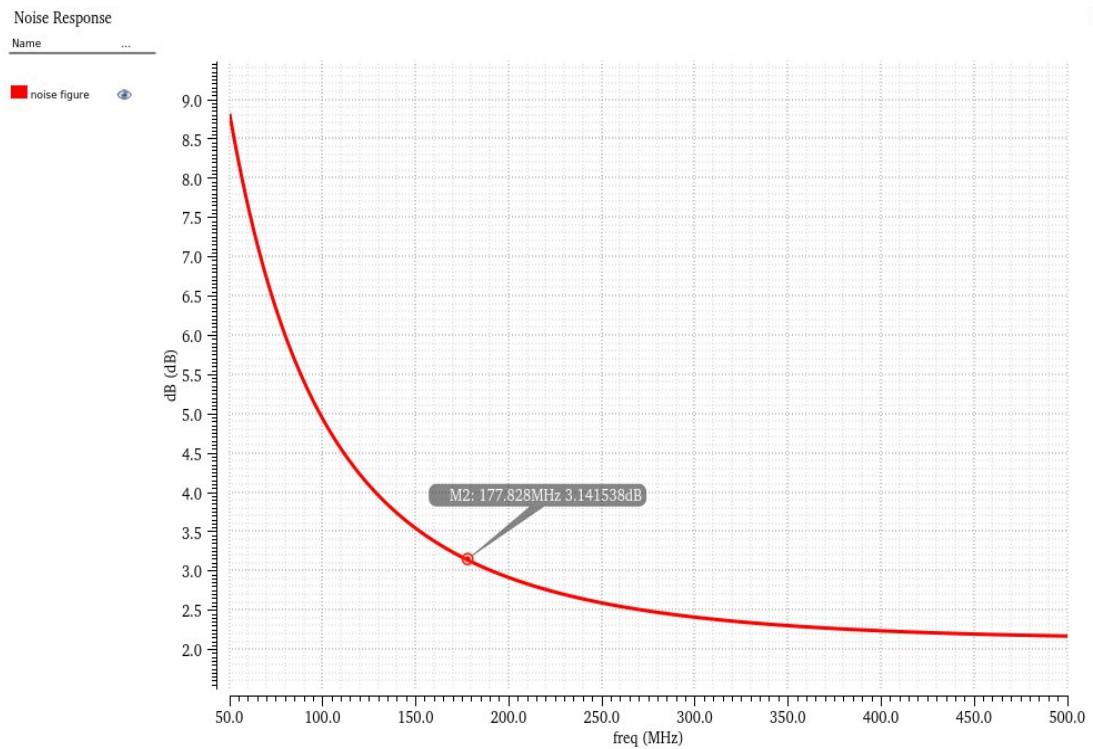


Figure 4.15 Noise figure of the equivalent π -model tunable mixer

Periodic Steady State Response

Name

compressionCurves

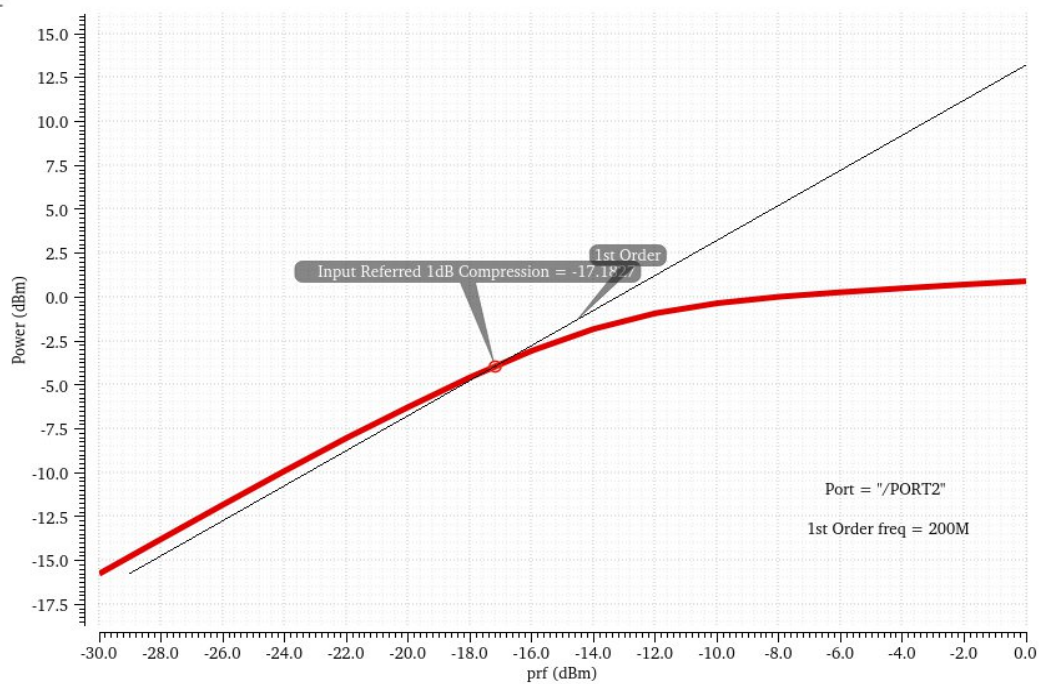


Figure 4.16 1- dB compression point of the equivalent π -model tunable mixer

Periodic AC Response

Name

trace

ipnCurves

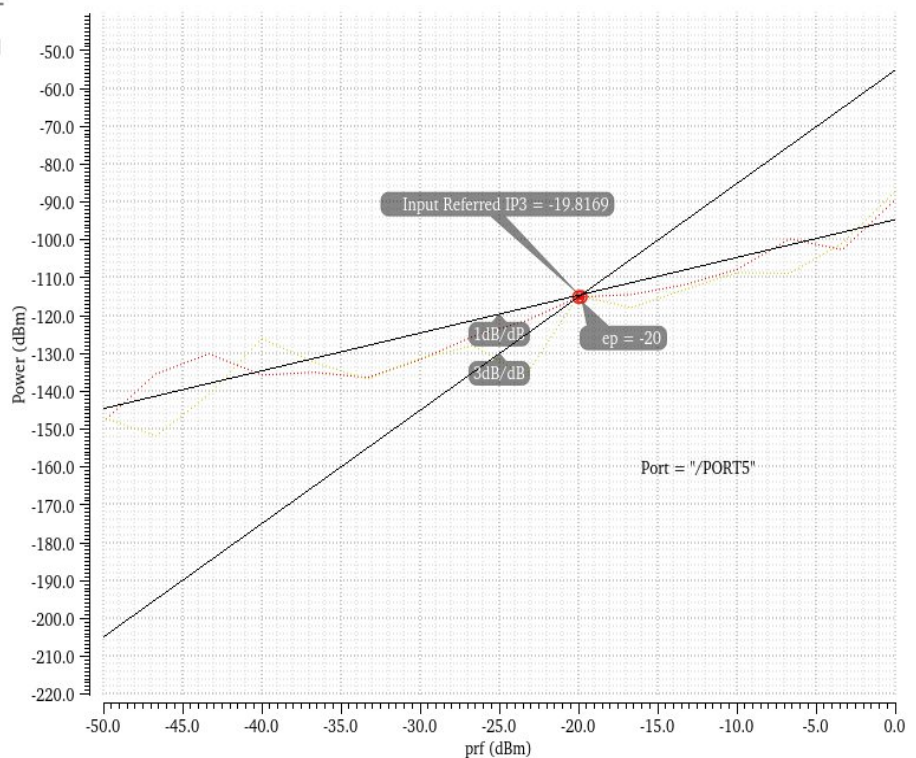


Figure 4.17 IP3 of the equivalent π -model tunable mixer

Chapter 5: LOW NOISE AMPLIFIER TOPOLOGY

5.1 Low Noise Amplifier Fundamental

The low noise amplifier (LNA) is one of the essential components in radio frequency front-end communication systems. The LNA is vital in maintaining the overall noise figure (NF) of the entire system in every front-end receiver section [21]. An LNA is primarily used to amplify the desired signals received by the receiving antenna with minimal noise and distortion. So the design of the LNA should be in such a way that its noise figure must be as minimum as possible [22] [23] [24]. Fig.5.1 shows a block diagram of the LNA in the RF front-end system.

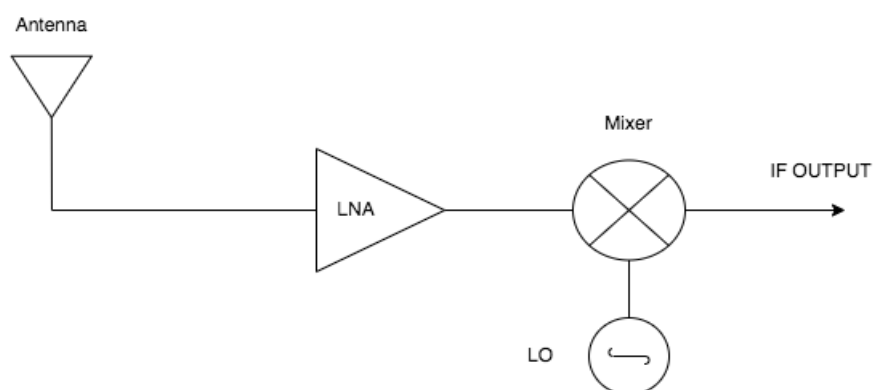


Figure 5.1 Block diagram of low noise amplifier in RF front-end system

The LNA design involves several tradeoffs, including noise figure (NF), gain, linearity, impedance matching, and power dissipation [25]. The parameters of LNA

vary depending on different topologies. An LNA is designed based on the following parameters:

1. Noise Figure (NF)

The noise factor of the amplifier is calculated by comparing its noise output with the noise output of an ideal noiseless device. Due to the inherent noise of electronic components, any LNA always has a noise factor higher than 1. Noise figure (NF) is a parameter related to noise factor (dB), which is calculated by taking $NF = 10 * \log_{10}$ (noise factor) as a decibel number. A noiseless LNA should be capable of exhibiting a noise figure close to 0dB, which is a good indication of LNA's performance. The noise figure indicates the extent of degradation of SNR in an LNA. Therefore, the noise figure of the entire front-end receiver system can be represented by [27].

$$NF_{TOTAL} = NF_{LNA} + \frac{NF_{afterLNA} - 1}{Gain_{LNA}} \quad (5.1)$$

The NF_{TOTAL} represents the noise figure of the first stage of LNA, $NF_{afterLNA}$ represents the noise figure of subsequent stages beyond the first stage, and $Gain_{LNA}$ represents the gain of the LNA.

2. Input Matching

The input impedance of the LNA significantly impacts the noise added to the output signal. A higher impedance results in a higher level of noise. A low input impedance can result in poor measurements when the low signal source has a high impedance. However, these situations may require a higher input impedance.

S-parameters are primarily used for impedance matching. The S-parameters (S_{11} , S_{12} , S_{21} , S_{22}) describe a two-port network's transmission and reflection coefficients under matched conditions. S_{11} is the reflection coefficient at port one, known as the input reflection coefficient, expressed in decibels, which gives the input return loss. At port two, S_{22} is the reflection coefficient known as the output reflection coefficient and when it is expressed in decibels provides the output with return loss [27].

3. Gain

The gain describes the ability of the LNA to boost signals with deficient levels of strength from the antenna. The gain of an LNA can be represented by [26].

$$\text{Gain} = 20\log \frac{V_{\text{OUT}}}{V_{\text{IN}}} \quad (5.2)$$

4. Stability

In the process of designing LNAs, the circuit should be ensured to be stable within the desired frequency range. For a stable circuit, the stability factor (K) should always be greater than 1, and LNA stability can be evaluated by plotting the stability factor (K). The stability of the LNA can be improved by inductive loading and neutralization to cancel coupling affection [28].

5. Linearity

The 1-dB compression point and the third-order intercept point can be plotted to represent the linearity of LNA. The 1-dB compression point is marked by a drop of 1dB in the output signal power from its intended level. The third-order intercept is the point at which the third order's modulation product coincides with the first order's output.

Input intercept point 3 (IIP3) is defined as the level of power input corresponding to IP3.

6. Offset

The offset affects the amplifier's performance in DC analysis. However, due to the inherent limitations of semiconductor devices, the LNA will produce an inaccurate DC offset level.

7. Bandwidth and center frequency

The LNA's bandwidth should cover the range of frequencies from the component connected to it, and its center frequency should also match the center frequency of the component, such as the mixer.

5.2 Common Source Amplifier

5.2.1 Common Source Amplifier with Load R_D

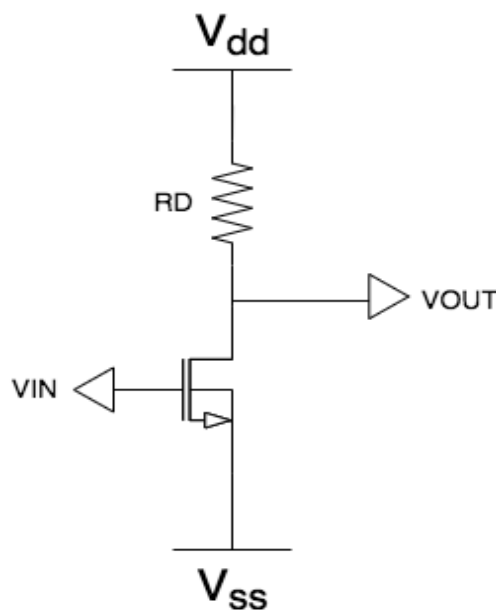


Figure 5.2 Common source amplifier with R_D

Fig. 5.2 shows the structure of a conventional common source amplifier with a passive resistor. The gain expression can be generated from a small signal model, as shown in Fig. 5.3.

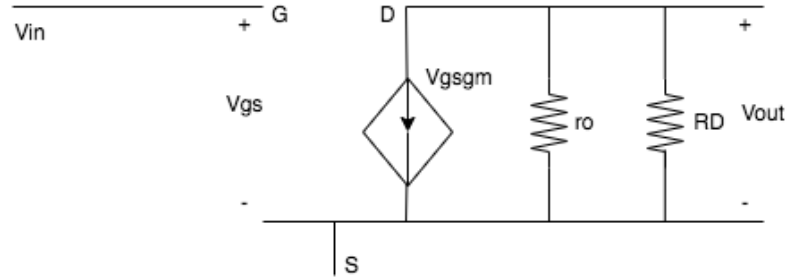


Figure 5.3 Small signal model of common source amplifier with R_D

$$Z_{out} = R_D || r_o \quad (5.3)$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = -(R_D || r_o) * gm \quad (5.4)$$

Due to the $R_D \gg r_o$ considering channel length modulation, the R_D can be neglected; $\text{Gain} = \frac{V_{out}}{V_{in}} = | - r_o * gm |$.

5.2.2 Common Source Amplifier with Source Degeneration

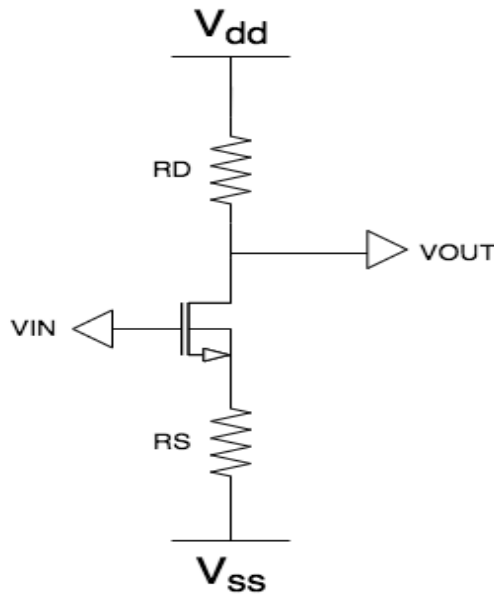


Figure 5.4 Common source amplifier with source degeneration

Fig. 5.4 shows the structure of a common source amplifier with source degeneration. The gain expression can be generated from a small signal model, as shown in Fig. 5.5.

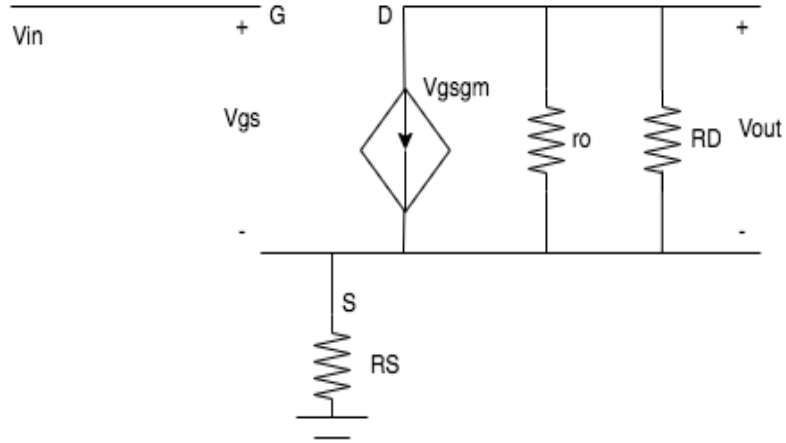


Figure 5.5 Small signal model of common source amplifier with source degeneration

$$Z_{out} = \frac{R_D}{\frac{1}{g_m} + R_S} \quad (5.5)$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{g_m R_D}{1 + g_m R_S} \quad (5.6)$$

The gain is reduced compared to the conventional CS amplifier because of the source of degeneration. Because of the body effect, the output resistance is increased, and the gain is affected by $(1 + \frac{g_{mb}}{g_m})$.

$$Z_{out} = \frac{R_D}{\frac{1}{g_m} + R_S(1 + \frac{g_{mb}}{g_m})} \quad (5.7)$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{g_m R_D}{1 + g_m R_S(1 + \frac{g_{mb}}{g_m})} \quad (5.8)$$

5.2.3 Common Source Amplifier with Active Load

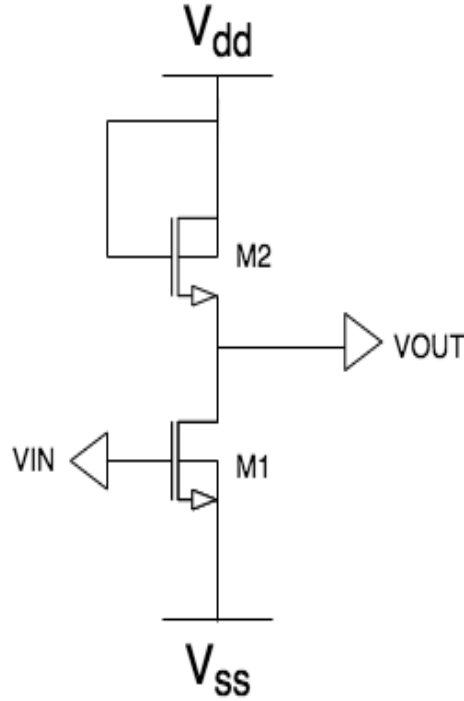


Figure 5.6 Common source amplifier with active load

A transistor is used to replace the passive resistor to ensure that the amplifier always operates in the saturation region. Active load amplifiers produce less distortion. The large signal has become linear, whereas the small signal has always been linear by definition. Large signal models are only dependent on physical dimensions. The ratio of physical dimensions determines the gain. It reduces the dependence on environmental factors such as changes in temperature. Based on the observation from Eq. (5.9), Increasing the width of M_1 and length of M_2 while decreasing the width of M_2 and length of M_1 will increase gain.

$$\text{Gain} = \frac{v_{out}}{v_{in}} = \frac{1}{1 + \frac{g_{mb}}{g_m}} * \sqrt{\frac{W_1}{L_1} * \frac{L_2}{W_2}} \quad (5.9)$$

5.3 Common Drain Amplifier

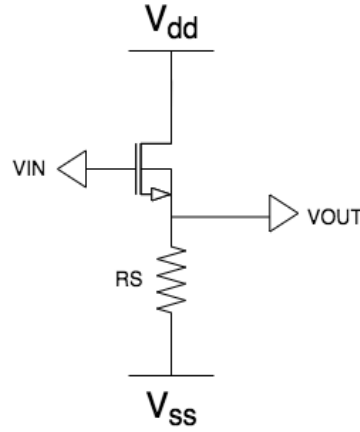


Figure 5.7 Common drain amplifier (source follower)

A common drain amplifier is also referred to as a source follower. The gain is close to unity gain (<1) because of its low output impedance. The gain expression can be generated from a small signal model, as shown in Fig. 5.8.

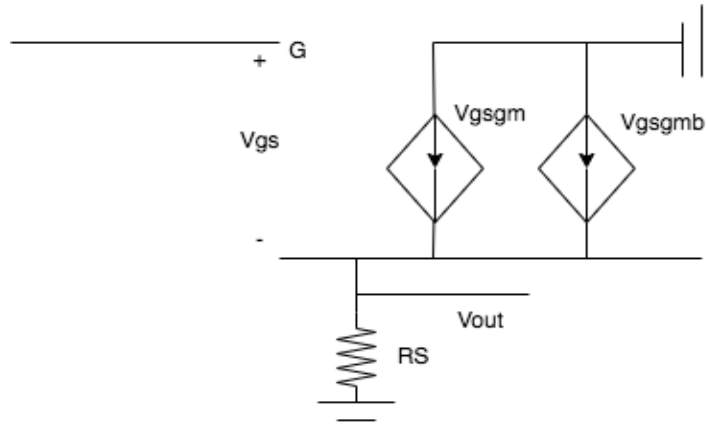


Figure 5.8 Small signal model of common drain amplifier

Output impedance Z_{out} and gain can be represented by

$$Z_{out} = R_s \parallel \frac{1}{\frac{gm}{1 + \frac{gmb}{gm}}} < \frac{1}{gm} \quad (5.10)$$

$$\text{Gain} = \frac{V_{out}}{V_{in}} = \frac{R_s}{\frac{1}{gm} + (1 + \frac{gmb}{gm})R_s} < 1 \quad (5.11)$$

5.4 Common Gate Amplifier

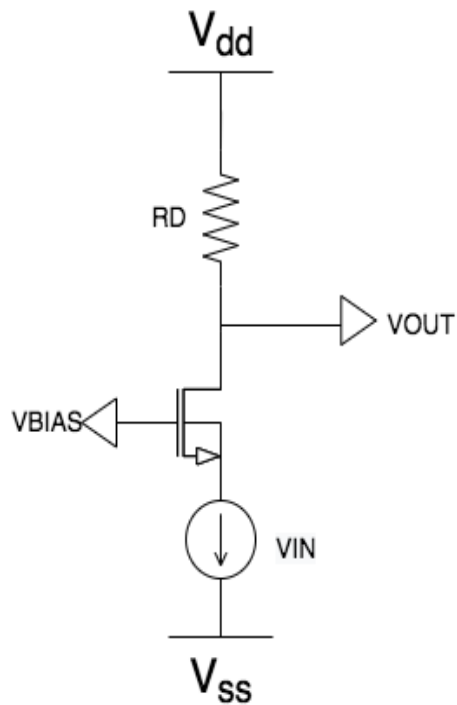


Figure 5.9 Common gate amplifier

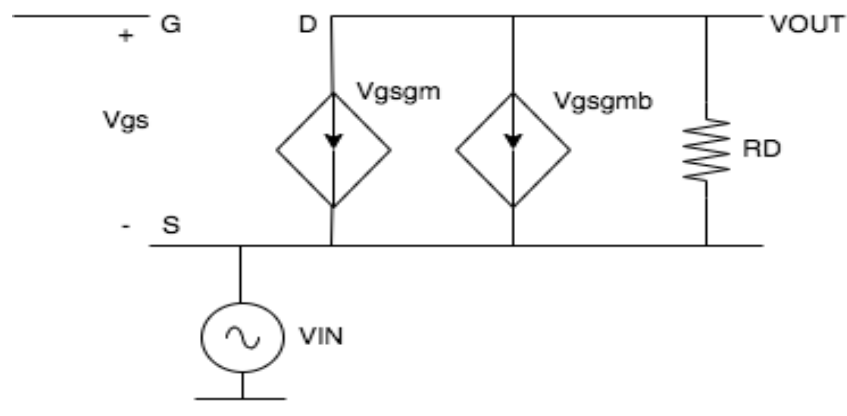


Figure 5.10 Small signal model of common gate amplifier

Fig. 5.9 shows the common gate amplifier in which the input signal is sensed at the source terminal and the output is produced at the drain terminal. The gain expression can be generated from a small signal model, as shown in Fig. 5.10.

A common gate amplifier's gain is positive, and its input impedance is relatively low. In addition, the input impedance of a common gate stage is relatively low only if the load resistance connected to the drain is negligible.

$$Z_{out} = R_D \quad (5.12)$$

$$\text{Gain} = \frac{v_{out}}{v_{in}} = g_m * R_D \left(1 + \frac{g_{mb}}{g_m}\right) \quad (5.13)$$

5.5 Cascode Amplifier

In Fig. 5.11, a cascode amplifier is introduced to increase the gain compared to a common gate amplifier. To achieve higher output impedance, more transistors can be added to the common gate amplifier to achieve higher gain.

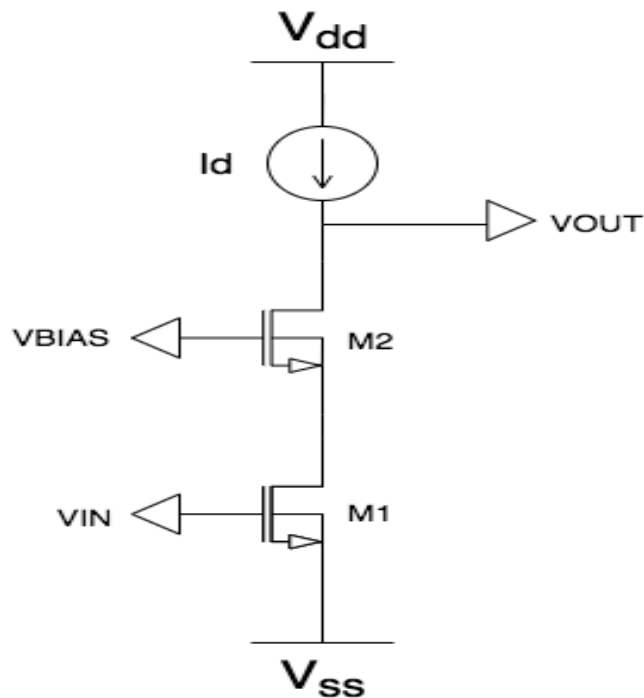


Figure 5.11 Cascode amplifier

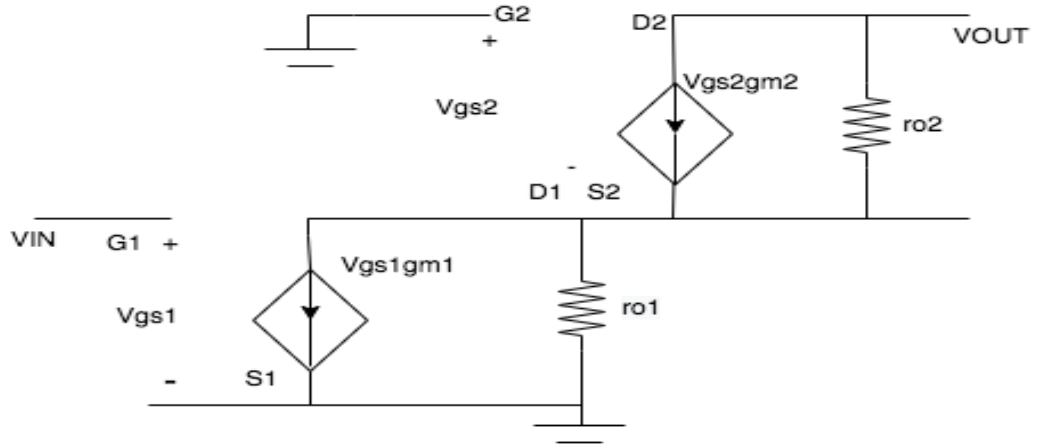


Figure 5.12 Small signal model of cascode amplifier

$$A_{V1} = -g_{m1} * r_{o1} \quad (5.14)$$

$$A_{V2} = -g_{m2} * r_{o2} \quad (5.15)$$

$$A_{Vtotal} = A_{V1} * A_{V2} = -g_{m1} * r_{o1} * g_{m2} * r_{o2} \quad (5.16)$$

Adding PMOS transistor M_2 to increase gain in Fig.5.13. The r_{out} increases to

$$r_{out} = g_{m3} * r_{o3} * r_{o1} || r_{o2} \quad (5.17)$$

The gain is

$$A_{Vtotal} = g_{m1}(g_{m3} * r_{o3} * r_{o1} || r_{o2}) \quad (5.18)$$

Adding the transistor PMOS M_4 ,

$$r_{out} = g_{m3} * r_{o3} * r_{o1} || r_{o2} * r_{o4} * g_{m4} \quad (5.19)$$

The new gain will be

$$A_{Vtotal} = g_{m1}(g_{m3} * r_{o3} * r_{o1} || r_{o2} * r_{o4} * g_{m4}) \quad (5.20)$$

Adding transistors will result in an infinite gain because the r_{out} will be significant;

however, the current will be very small, such as nA. Cascode amplifiers will be out of

saturation because there is insufficient voltage headroom. In section 5.6, a differential amplifier is introduced to solve this problem.

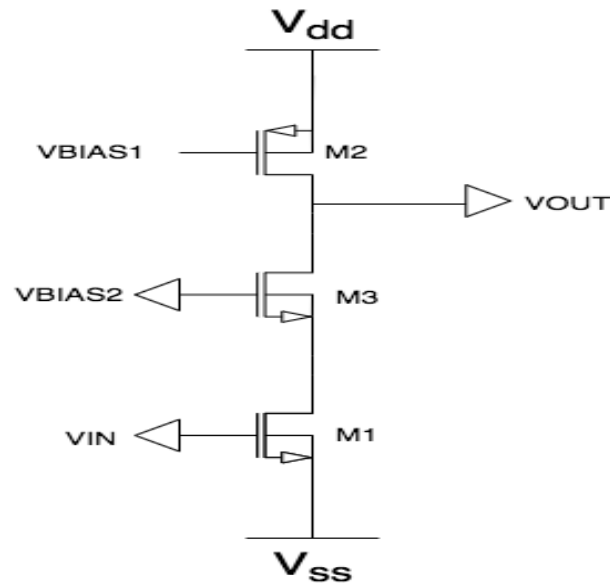


Figure 5.13 Cascode amplifier with adding PMOS transistor

5.6 Differential Amplifier

Unlike cascode amplifiers, differential amplifiers create a folded structure to avoid stacking too many transistors vertically, which is difficult with low power supply voltage. Furthermore, The current source does not change the current I_{ds1} or I_{ds2} ; thus, the V_{OUT+} and V_{OUT-} will remain unchanged since $V_{out} = V_{dd} - I_D R_D$, and the spike signal won't be changed. With an increase in V_1 and a decrease in V_2 , more current is diverted to M_1 , and less current is diverted to M_2 . As a result, V_{OUT-} will decrease while V_{OUT+} increases. The stage will produce differential gain and common mode attenuation. This differential stage is made instead of the single stage. Last, the bulk of M_1 and M_2 are connected to the ground, and the two sources are connected. Transistor M_1 and M_2 share the same V_{bs} . Body effect doesn't affect the V_{T1} and V_{T2} , so $V_{T1}=V_{T2}$. Body effect is

naturally canceled because of the operation of the differential topology. The body effect $(1 + \frac{g_{mb}}{g_m})$ won't affect the gain. Fig. 5.14 shows the structure of the differential amplifier.

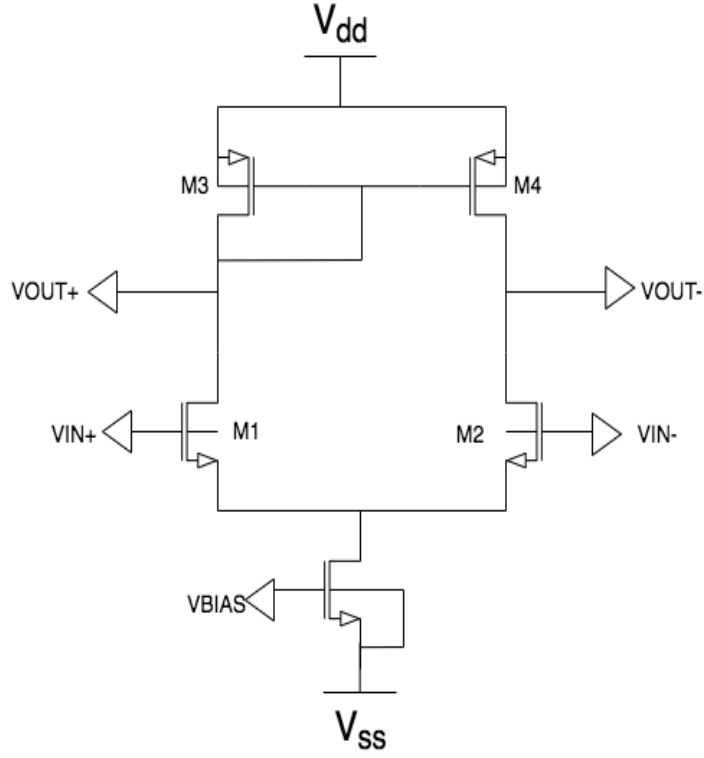


Figure 5.14 Differential amplifier

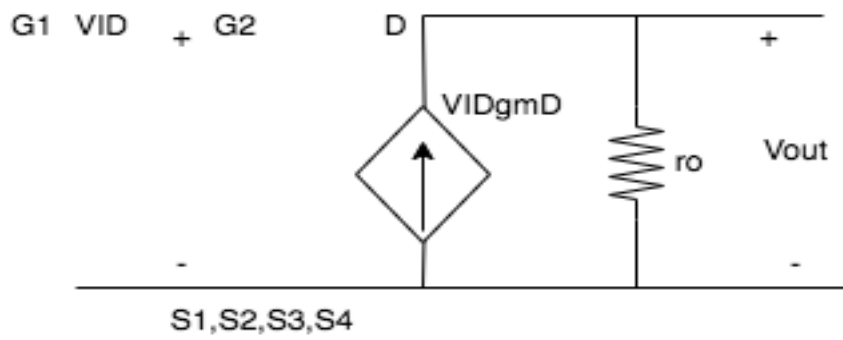


Figure 5.15 Approximate small signal model of the differential amplifier

$$r_{out} = r_{ds2} || r_{ds4} = \frac{1}{g_{ds2} + g_{ds4}} \quad (5.21)$$

$$g_{mD} = \sqrt{2\beta_1 I_{DS1}} \quad (5.22)$$

$$\text{Gain} = \frac{v_{out}}{v_{ID}} = g_{mD} * r_{out} \quad (5.23)$$

5.7 Two Stages Operational Amplifier

Operational amplifiers (Op-amps) are integral to many analog and mixed-signal systems. Op-amps with vastly different levels of complexity are used to realize functions ranging from dc bias generation to high-speed amplification or filtering. [29].

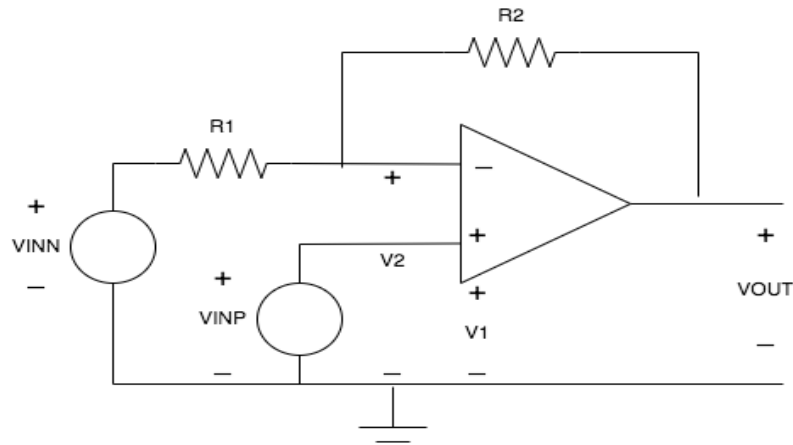


Figure 5.16 General configuration of Op-amp

Op-amps have sufficiently high forward gain so that when negative feedback is applied, the closed loop transfer function is practically independent of the gain of the op-amp.

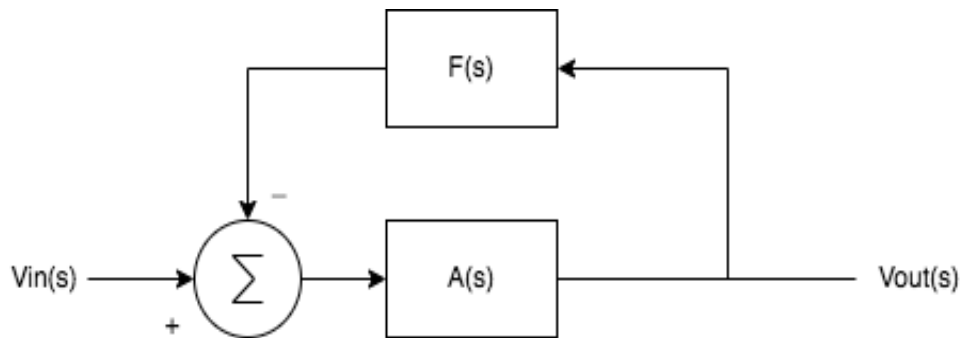


Figure 5.17 Op-amp feedback network

Loop gain can be represented by

$$L(S) = -A(S) * F(S) \quad (5.24)$$

Forward transfer function

$$\frac{V_{out}}{V_{in}} = \frac{A(j\omega)}{1 + A(j\omega) * F(j\omega)} \quad (5.25)$$

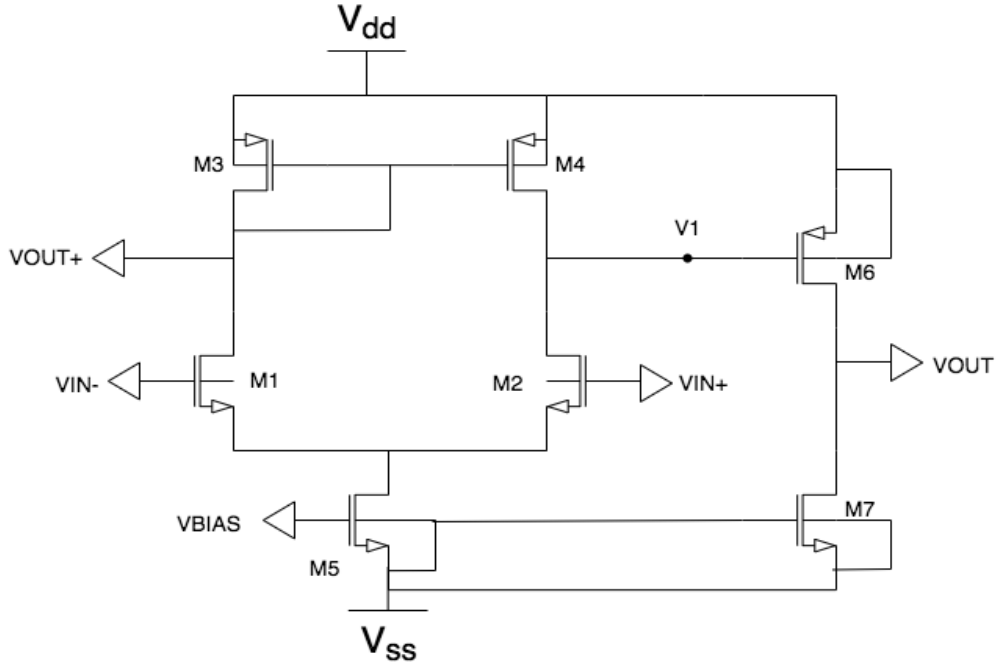


Figure 5.18 Two-stage Op-amp

Fig.5.18 shows the schematic of two stages Op-amp. It consists of a differential amplifier and a cascode amplifier with voltage to current (transconductance stage) and current to voltage (load stage) converting stages. Differential input pairs M₁ and M₂ convert the differential input voltage to a differential current if apply the common mode. M₅ and M₇ are current sources to present a high output impedance. M₅ copies the current through M₇, based on Vbias ($I_{ds5} = W * I_{ds7}$). The common mode will not change if a good source is applied because some are forced to be constant. For example, M₃

and M_4 are combined to perform a current mirror, and the current is copied from M_3 to M_4 . The second order Op-amp small signal model is shown in Fig. 5.19.

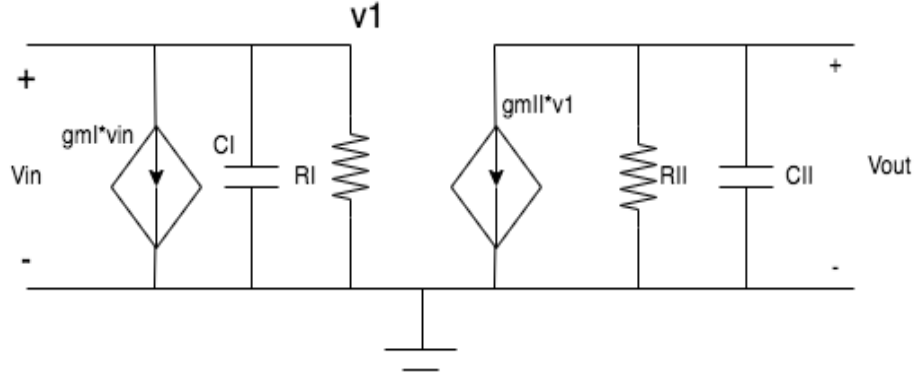


Figure 5.19 Second-order small signal model of the two-stage Op-amp

According to the small signal model of the two-stage amplifier, R_I is the output resistance of the first stage, and R_{II} is the output resistance of the second stage. C_I is the output capacitance of the first stage, and C_{II} is the output capacitance of the second stage. V_1 is the output of the first stage.

The first stage gain A_{vI} is

$$A_{vI} = \frac{V_1}{V_{in}} = -g_{mI} * \frac{\frac{1}{sC_I} * R_I}{\frac{1}{sC_I} + R_I} \quad (5.26)$$

The second stage gain A_{vII} is

$$A_{vII} = \frac{V_{OUT}}{V_I} = \frac{g_{mII} * R_{II}}{\frac{s}{\omega_2} + 1} \quad (5.27)$$

The total gain A_{vtotal} is

$$A_{vtotal} = A_{vI} * A_{vII} = g_{mI} * R_I * \left(\frac{1}{\frac{j\omega}{\omega_1} + 1} \right) * g_{mII} * R_{II} * \left(\frac{1}{\frac{j\omega}{\omega_2} + 1} \right) \quad (5.28)$$

5.8 Noise Cancellation and Reduction Technology

5.8.1 Feedforward Noise-canceling Technique

The feed-forward noise-canceling technique allows simultaneous noise and impedance to be matched simultaneously while canceling the noise and distortion of the matching device. High sensitivity applications require sufficient gain, good isolation, and a noise figure ($NF=10 \cdot \log_{10}(F)$) below 3dB over a wide frequency range [31]. This technique can make wide-band impedance-matching amplifiers work well with NF below 3dB.

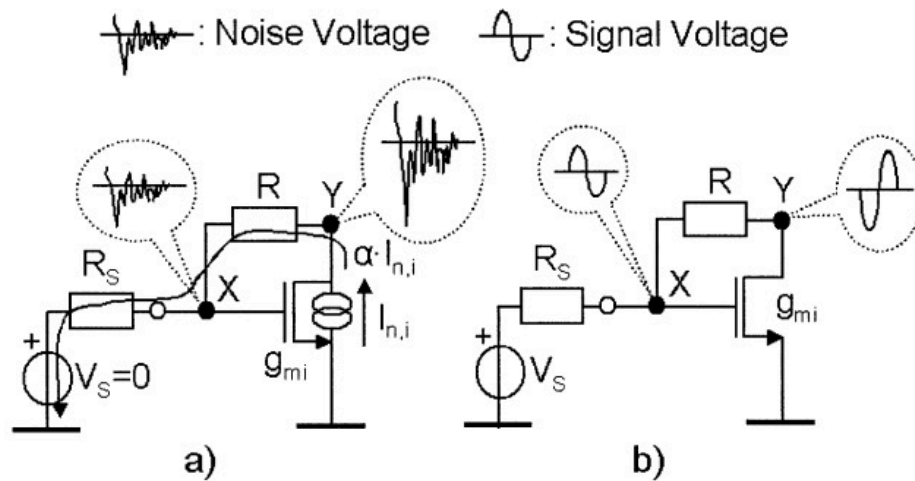


Figure 5.20 Matching (a) noise and (b) signal voltage at nodes X and Y [30]

Fig.5.20 presents a low-noise wide-band technique for decoupling noise factor F from $Z_{in}=R_s$ without global negative feedback or compromising the source match. The matching device's output noise is canceled without affecting the signal transfer quality. For example, the voltage signal at nodes X and Y have opposite phases In Fig. 20 (b) because the gain $A_{VF,MS}=1- g_{mi}R_0 < 0$, assuming $g_{mi}R_0 > 1$. Due to the difference in sign between noise and signal, the noise of the matching device can be canceled while the signal is added simultaneously. The new output is created by adding the voltage at node Y to the scaled negative replica of the voltage at node X. To cancel the thermal noise

generated by the matching device, a proper value should be determined for this scaling factor noise canceling at the output node.

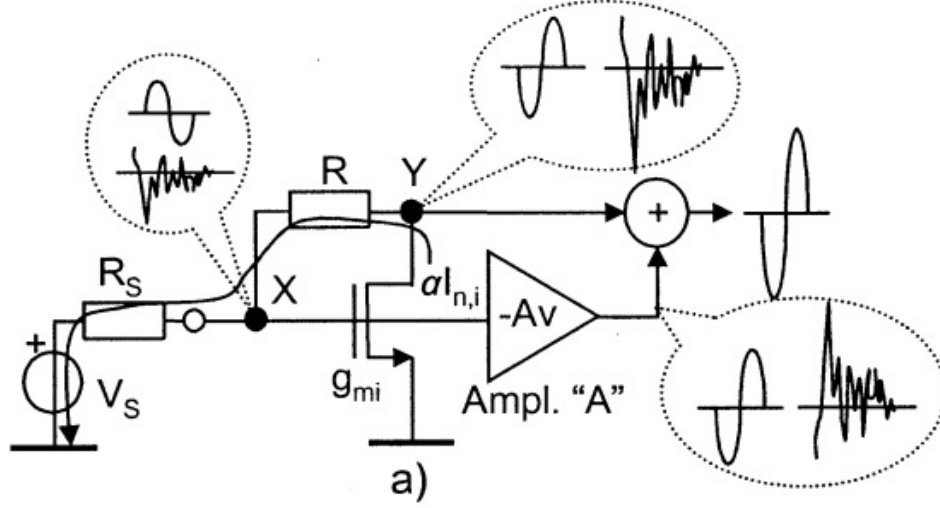


Figure 5.21 Wide-band LNA exploiting noise canceling [30]

Fig. 5.21 shows a straightforward implementation using an ideal feedforward voltage amplifier A with a gain ($A_V > 1$). The matching device noise voltages, $V_{X,n,i}$ at node X is [30]

$$V_{X,n,i} = \alpha(R_S, g_{mi}) * I_{n,i} R_S \quad (5.29)$$

The matching device noise voltages, $V_{Y,n,i}$ at node Y is

$$V_{Y,n,i} = \alpha(R_S, g_{mi}) * I_{n,i} (R_S + R) \quad (5.30)$$

The output noise voltage is

$$V_{OUT,n,i} = V_{Y,n,i} - V_{X,n,i} * A_V \quad (5.31)$$

The gain A_V, c for output noise cancellation equal to

$$A_V, c = \frac{V_{Y,n,i}}{V_{X,n,i}} = 1 + \frac{R}{R_S} \quad (5.32)$$

Two characteristics of noise canceling can be observed from Eq.(5.32). 1) Noise canceling depends on the absolute value of the actual impedance of the source. 2) The cancellation is independent of $\alpha(R_s, g_{mi})$ and the quality of the source impedance match. This is because of any change of g_{mi} equally affects the noise voltages $V_{X,n,i}$ and $V_{Y,n,i}$ [30].

5.8.2 Gain-enhanced Noise-canceling Technique

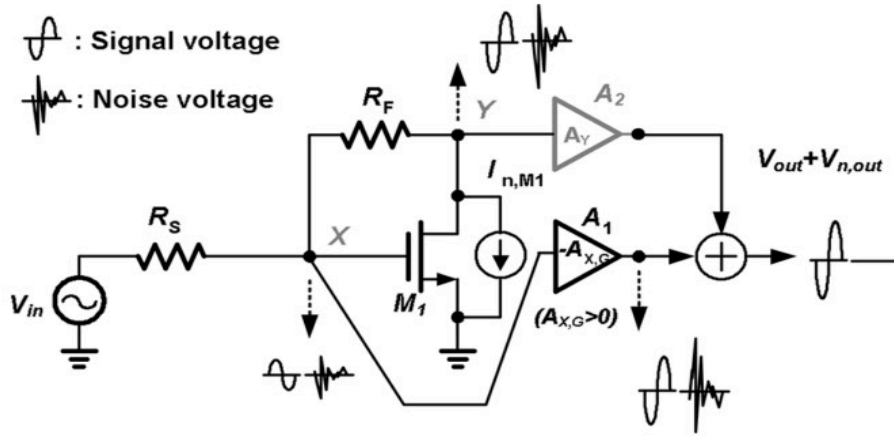


Figure 5.22 Resistive shunt feedback LNA using the gain-enhanced noise-canceling technique [32]

Fig. 5.22 shows a simplified resistive shunt feedback LNA using the gain-enhanced noise-canceling technique to cancel output noise voltage. Two paths to implement a gain-enhanced noise-canceling technique. The first is to increase the overall voltage gain, $A_{V,G}$, and the other is to match the phase delay for two paths. An additional gain of A_Y is used in the upper feedforward path. By using the following calculations, the output noise voltage is canceled.

The output noise voltage $V_{n,out}$ is

$$V_{n,out} = I_{n,M1}(R_S + R_F - A_X R_S) \quad (5.33)$$

$$A_X = 1 + \frac{R_F}{R_S} \quad (5.34)$$

The overall voltage gain is

The gain at node X can be expressed as:

The overall voltage gain A_V can be calculated when noise voltage $V_{n,out}$ is canceled.

[illegible]

Fig. 5.23 shows the schematic of the first noise-canceling LNA. It consists of two stages: the noise-canceling stage and the output buffer. $R_{S,A}$ is a 50Ω source impedance connected to the input via a large capacitor $C_{in,A}$. In the noise-canceling stage, A shunt

feedback resistor $R_{F1,A}$ is used to match the signal and noise generated from the input transistors $M_{1,A}$, $M_{2,A}$, and $M_{3,A}$ are used to combine the signal and subtract the noise of $M_{1,A}$. $R_{D1,A}$, and $R_{D2,A}$ are load resistors. The polarities of the signals at the drains of $M_{1,A}$ and $M_{2,A}$ must be in phase to subtract the noise at the drain of $M_{2,A}$ [32]. The noise factor for each device is

$$F_{M2,A} = \frac{\frac{\gamma}{\alpha} g_{m2,A} R_{L2,A}^2}{R_{S,A} A_{NC,A}^2} \quad (5.38)$$

$$F_{M3,A} = \frac{\frac{\gamma}{\alpha} \frac{g_{m3,A}}{(1+g_{m3,A} R_{L1,A})^2} R_{L2,A}^2}{R_{S,A} A_{NC,A}^2} \quad (5.39)$$

$$F_{RF1,A} = \frac{(\frac{g_{m3,A} R_{L1,A}}{1+g_{m3,A} R_{L1,A}})^2 R_{L2,A}^2}{R_{F1,A} R_{S,A} A_{NC,A}^2} \quad (5.40)$$

$$F_{RD1,A} = \frac{(\frac{g_{m3,A} R_{L1,A}}{1+g_{m3,A} R_{L1,A}})^2 R_{L2,A}^2}{R_{D1,A} R_{S,A} A_{NC,A}^2} \quad (5.41)$$

$$F_{RD2,A} = \frac{R_{L2,A}^2}{R_{D2,A} R_{S,A} A_{NC,A}^2} \quad (5.42)$$

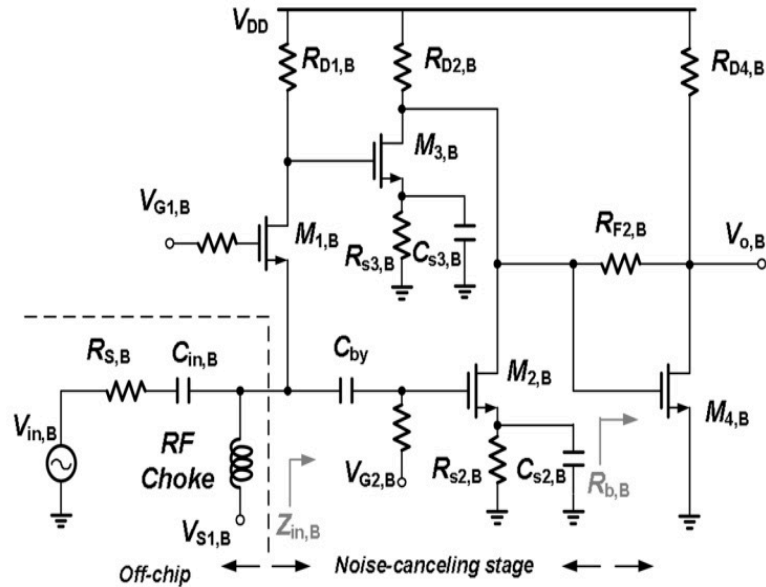


Figure 5.24 Second noise-canceling LNA using gain-enhanced technique [32]

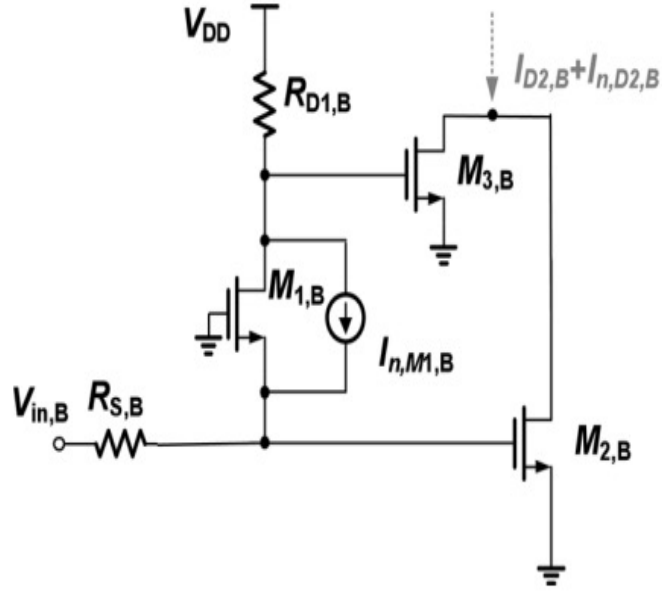


Figure 5.25 Noise-canceling stage of second LNA [32]

The second noise-canceling LNA is shown in Fig. 5.24. $M_{1,B}$ provides wideband input matching and voltage gain in the noise-canceling stage. For input matching, the input impedance $Z_{in,B}=50 \Omega$. $M_{2,B}$ and $M_{3,B}$ are used to combine the signal and subtract the noise of $M_{1,B}$. $R_{D1,B}$ and $R_{D2,B}$ are load resistors [32]. The noise factor for each device is

$$F_{M2,B} = \frac{\frac{\gamma}{\alpha} g_{m2,B}}{R_{S,B} * G_{m,NC,B}^2} \quad (5.43)$$

$$F_{M3,B} = \frac{\frac{\gamma}{\alpha} g_{m3,B}}{R_{S,B} * G_{m,NC,B}^2} \quad (5.44)$$

$$F_{RD1,B} = \frac{R_{D1,B} g_{m3,B}^2}{R_{S,B} * G_{m,NC,B}^2} \quad (5.45)$$

$$F_{RD2,B} = \frac{1}{R_{D2,B} * R_{S,B} G_{m,NC,B}^2} \quad (5.46)$$

The gain of two stages noise canceling stages can be expressed as

$$\frac{A_{NC,B}}{A_{NC,A}} = \frac{g_{m3,B} R_{L1,B}}{4 g_{m1,A} R_{F1,A}} \quad (5.47)$$

5.8.3 CG and CS Combination Noise-canceling Technique

Two common wideband matching techniques (a common source stage with resistive shunt feedback (Fig.5.26) and a common gate stage (Fig.5.27)) are compared to perform CG and CS combination noise-canceling technique with the input matching requirement. The resistive shunt feedback structure is selected to meet the wideband input matching requirement in the common source stage; however, it produces high power consumption. A common gate amplifier combines with a common source stage to implement wideband impedance matching. Moreover, the CG LNA has better linearity, low power consumption, and better input-output isolation [33]. A popular method for reducing the noise figure (NF) is the noise cancelation structure which eliminates the channel thermal noise of the CG structure by using a common source (CS) transistor [37].

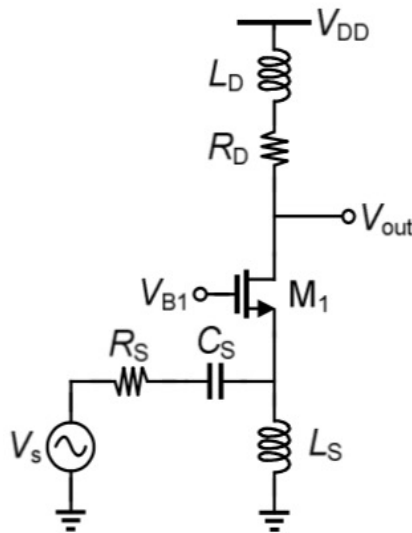


Figure 5.26 Common wideband input matching technique (common gate) [36]

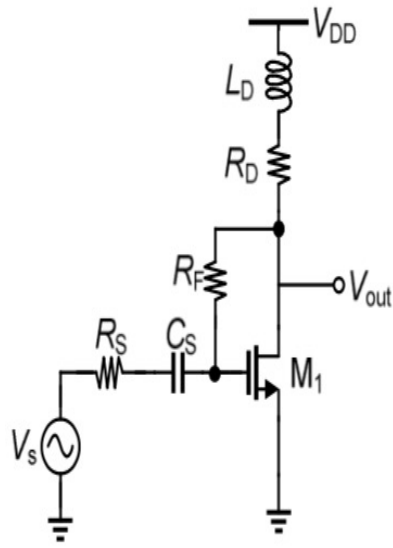


Figure 5.27 Common wideband input matching technique (common source) [36]

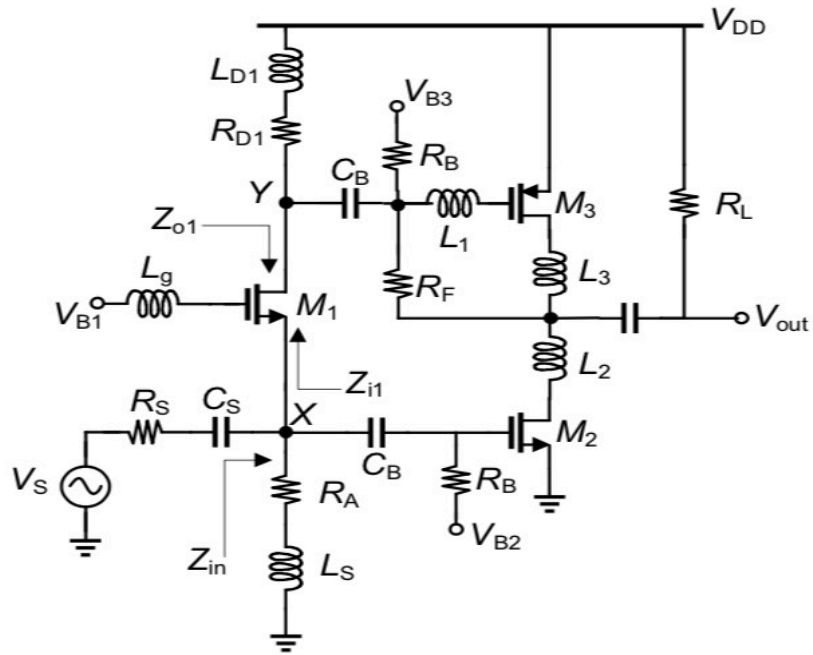


Figure 5.28 Common wideband input matching technique [36]

The proposed LNA with common wideband input matching techniques is shown in Fig. 5.28. The first stage is a common gate structure in this structure, and transistor M_1 is used to implement wideband input matching. The second stage is a common

source structure. The transistor M_2 is used to cancel the channel noise produced by the transistor M_1 . The PMOS transistor M_3 is selected to re-use the current of M_2 and improve linearity. The resistor R_A is applied to extend the bandwidth of M_1 at low frequencies and reduce flicker noise. In addition, L_s is used to cancel the degrading effect of the parasitic capacitances of transistors M_1 and M_2 . Finally, L_g dampens the parasitic capacitor C_S of M_1 to enhance the input return loss. L_1 , L_{D1} , L_2 , and L_3 control the center frequency. R_L is parallelized at the output node to reduce the variation in output impedance and achieve a reasonable gain. The negative feedback R_F is used to prevent variations in the output voltage due to the high impedance of the output node. The value of R_F is mainly selected to ignore its effect in the analysis.

The input impedance with R_A is

$$Z_{in} = \frac{R_A + sL_s}{C_x L_s s^2 + (R_A C_x + g_{m1} L_s) s + (g_{m1} R_A + 1)} \quad (5.48)$$

Output impedance Z_{out} can be calculated as

$$Z_{out} = (r_{ds2} + sL_2) \parallel (r_{ds3} + sL_3) \parallel R_L \parallel \frac{1}{sC_{out}} \quad (5.49)$$

The total voltage gain A_v is calculated as

$$A_v = \left| \frac{Z_{in}}{Z_{in} + R_s} \right| * (g_{m1} g_{m3} |Z_Y| + g_{m2}) |Z_{out}| \quad (5.50)$$

According to the noise cancellation technique, the most significant noise sources are the thermal noise of R_{D1} and R_A and the channel noise of M_2 and M_3 . They are calculated as follows,

The thermal noise of R_{D1} is

$$NF_{RD1} = \frac{R_{D1} R_s}{|Z_{O1} + R_{D1}|^2} \quad (5.51)$$

The thermal noise of R_A is

$$NF_{RA} = \frac{R_S}{R_A} \quad (5.52)$$

Channel noise of M_2 is

$$NF_{M2} = \frac{1}{R_S g_{m2}} \frac{\gamma}{\alpha} \quad (5.53)$$

Channel noise of M_3 is

$$NF_{M3} = \frac{R_S}{Z_Y^2 g_{m3}} \frac{\gamma}{\alpha} \quad (5.54)$$

The total noise figure is

$$NF = \frac{R_{D1} R_S}{(Z_{o1} + R_{D1})^2} + \frac{1}{R_S g_{m2}} \frac{\gamma}{\alpha} + \frac{R_S}{Z_Y^2 g_{m3}} \frac{\gamma}{\alpha} + \frac{R_S}{R_A} \quad (5.55)$$

Chapter 6: TUNABLE GILBERT MIXER INTEGRATED WITH A HIGH-GAIN LOW-NOISE AMPLIFIER

6.1 The Proposed High-Gain Low-Noise Amplifier

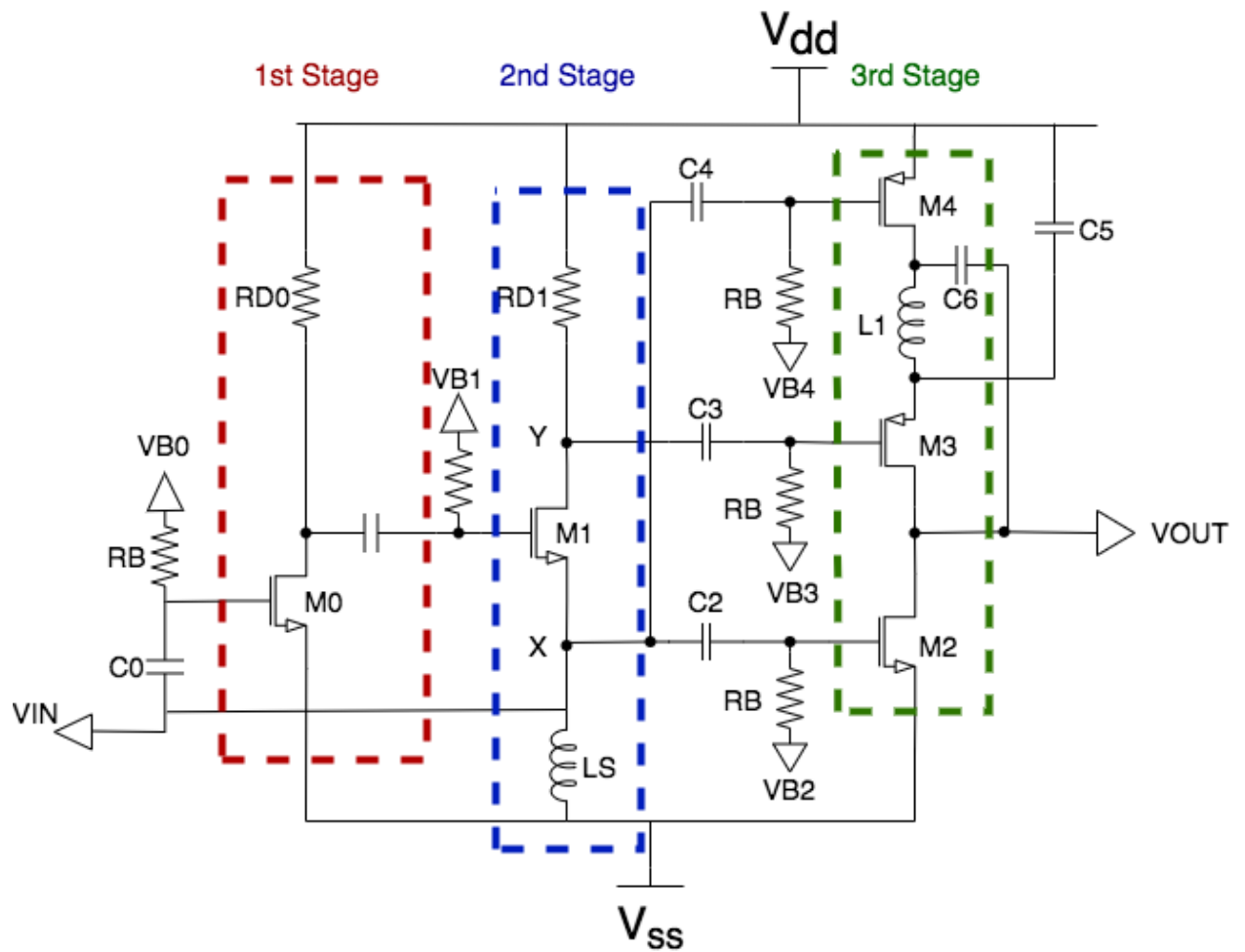


Figure 6.1 The proposed high-gain low-noise amplifier

To perform a high level of integration, the Gilbert mixer must meet sufficient gain with wide bandwidth to fulfill the multiband requirement and maintain a low noise figure. To solve this problem, a high-gain, low-noise amplifier is presented to be

cascaded with the mixer. The integration is to optimize the conversion gain of the proposed tunable mixer, compress the noise, and keep the required IF center frequency and bandwidth for multiband, multi-standard applications.

The proposed high-gain, low-noise amplifier is shown in Fig. 6.1. It consists of three stages to simultaneously achieve a high conversion gain and noise cancellation. The first stage is a common-source amplifier offering a conventional gain. The second stage is a common-gate amplifier selected as a primary stage to match a broadband 50 Ω input impedance without using extra components [34]. A common-gate amplifier has two advantages over the common-source amplifier for selecting it as a primary stage. First, the common-gate amplifier has higher input-output isolation than a shunt-feedback common-source amplifier because the parasitic gate-drain capacitor is AC grounded [35]. Second, the common-gate structure has better linearity than the common-source amplifier since the input source resistance further contributes to source degeneration.

For a conventional common-gate design, the input impedance is $\frac{1}{g_{mb} + g_m}$ and the noise factor is $F = 1 + \frac{\gamma}{\alpha g_m R_S} + \frac{4}{g_m R_D}$ [35], in which γ represents the excess noise factor in short-channel devices and α represents the ratio $\frac{g_m}{g_{ds}}$ between the small-signal transistor transconductance g_m and the zero-bias drain conductance g_{ds} where g_{mb} is the small-signal substrate transconductance. However, the second stage common-gate structure's noise performance is poor since its total input impedance $\frac{1}{g_m} = 50 \Omega$, which means g_m should be 20 mA/V to meet the input-matching condition. To resolve this

issue, a third-stage common-source structure is introduced as a noise cancellation technique that can remove the channel noise generated from the common gate amplifier [30]. Thermal noise generated from M_1 is canceled through M_2 and M_3 . The M_4 is parallel with M_2 to boost g_{m2} and optimize thermal noise in the common source stage. The third stage operates like a cascade PMOS current sink inverter amplifier. The third stage can be seen as a current source inverter amplifier from the Y node. The third stage can be seen as a current sink amplifier from the X node. To produce a high gain, signals from X and Y are combined and amplified at the outputs. Inductor L 's provides a DC path to the ground and reduces the parasitic capacitance at the input node. However, due to PMOS transistors at the output node, increasing parasitic capacitances leads to a higher variation in Z_{out} at high frequencies. The proposed LNA bandwidth is limited at high frequencies mainly because of these reasons. L_1 is used as inductive shunt and series peaking techniques to solve this problem. Shunt inductive peaking causes resonance at the output of each stage when the gain starts to drop off at higher frequencies [36]. Additionally, L_1 also can reduce the parasitic capacitance at the output node.

To determine the size of all transistors, widths are initially set as a minimum value of $W_0=W_1=W_2=W_3=W_4=0.22 \mu\text{m}$. All transistor lengths are initially set as a minimum length of $L=180 \text{ nm}$. Considering the short channel effect, $V_{tnshort}$ in 180nm CMOS technology is 0.55V. The K_{nshort} is the CMOS process factor, and λ_{nshort} is the channel length modulation parameter. As discussed in Section 3.1.1, $K_{nshort}= 317\mu\text{A}/\text{V}^2$ and

$\lambda_{nshort}=0.127$ for the NMOS; $K_{pshort}= 157\mu A/V^2$ and $\lambda_{pshort}=0.132$ for the PMOS.

For power specified constraints $p_{w0} < 9 \text{ mW}$, the sum of three branches I_{ds} must be smaller than 5mA. Assume each branch I_{ds} equals 1.5mA. For the 1st stage, the equation of I_{ds0} for the short channel effect is

$$I_{DS0} = K_{nshort} * W_0 * (V_{GS0} - V_{Tnshort})(1 + \lambda_{nshort} * V_{DS0}) \quad (6.1)$$

The transconductance of the short channel equation is

$$g_{m0} = -K_{nshort} * W_0 * (1 + \lambda_{nshort} * V_{DS0}) \quad (6.2)$$

Set initial $W_0 = 0.22\mu m$, and run the DC simulation, I_{DS0} is much less than 1.5mA. Increasing W_0 from $W_0 = 0.22\mu m$ to $11\mu m$, repeat the same procedure to find $I_{DS0} = 1.5\text{mA}$ @ $V_{DS0} = 0.65\text{V}$ when $V_{bias0} = V_{G0} = 0.878\text{V}$. $V_{DS0} > V_{GS0} - V_{tnshort}$ satisfies the saturation requirement. So, R_{D0} and r_{ds0} can be derived based on the above simulated values.

$$R_{D0} = \frac{V_{DD} - V_{DS0}}{I_{DS0}} = \frac{1.8\text{V} - 0.65\text{V}}{1.5\text{mA}} = 766 \Omega \quad (6.3)$$

$$r_{ds0} = \frac{1 + \lambda_{nshort} V_{DS0}}{\lambda I_{DS0}} = \frac{1 + 0.127 * 0.65\text{V}}{0.127 * 1.5\text{mA}} = 5.7\text{k} \Omega \quad (6.4)$$

Due to $r_{ds0} \gg R_{D0}$, r_{ds0} is not considered. The total output resistance $r_{out} = R_{D0}$. So, the gain of the first stage A_{V1} is

$$A_{V1} = -g_{m0} * R_{D0} = -K_{nshort} * W_0 * (1 + \lambda_{nshort} * V_{DS0}) * \frac{V_{DD} - V_{DS0}}{I_{DS0}} \quad (6.5)$$

Substitute Eq.(6.1) into Eq. (6.5).

$$|A_{V1}| = \frac{V_{dd} - V_{ds0}}{V_{gs0} - V_{tnshort}} \quad (6.6)$$

From Eq.(6.6), it can be observed the gain $|A_{V1}|$ is relevant to V_{bias0} . The simulated gain is 9.48 @ $V_{bias0} = 0.878\text{V}$. The analysis of the second stage is similar to the first

stage. W_1 is increased from 0.22 μm to 7 μm to satisfy the saturation requirement $V_{DS1} > V_{GS1} - V_{tnshort}$. $I_{DS1} = 1.5\text{mA}$ @ $V_{DS1} = 1.1\text{V}$ when $V_{bias1} = V_{g1} = 1.05\text{V}$. $R_{D1} = \frac{V_{DD} - V_{DS1}}{I_{DS1}} = 466\Omega$. The second stage is a common gate amplifier with a wideband input matching 50Ω and a positive gain $A_{V2} = g_{m1} * R_{D1}$. From simulated, $A_{V2} = 4.78$. For the third stage analysis, keep I_{DS2} , I_{DS3} and I_{DS4} equal to 1.5 mA, and set $W_2 = W_3 = W_4 = 0.22\mu\text{m}$. Repeat the same DC analysis as the first stage, and $W_2 = 19.6\mu\text{m}$, $W_3 = 9.8\mu\text{m}$, and $W_4 = 20\mu\text{m}$ are found. The total gain of the proposed LNA is 18.73, as presented in Fig.6.2. Calibrate the L_c , C_5 , and C_6 values to ensure the center frequency of the proposed LNA is close to the proposed mixer, and it is shown that L_c slightly affects the gain. Last, the $L_c = 11\text{nH}$, $C_5 = C_6 = 1\text{pF}$. L_s are set as 5 nH to ensure that parallel L_s do not degenerate the common-gate amplifier's input impedance.

6.1.1 Center Frequency and Conversion Gain

The impedance from the input to node Y is Z_Y , where R_{D1} is the load resistor of M_1 , C_X is the total parasitic capacitance at node X, and C_Y is the total parasitic capacitance at node Y.

$$Z_Y = R_{D1} || [r_{ds1} + (\frac{1}{sC_X} || sL_s)(1 + G_{m1}r_{ds1})] || \frac{1}{sC_Y} \quad (6.7)$$

So, the gain of transistor M_1 can be expressed as follows

$$A_{v1} = A_{VY} = g_{m1} * Z_Y \quad (6.8)$$

$$A_{V1} = A_{VY} = g_{m1} * R_{D1} || [r_{ds1} + (\frac{1}{sC_X} || sL_s)(1 + G_{m1}r_{ds1})] || 1/sC_Y \quad (6.9)$$

The output impedance is determined by Z_{out} , which can be calculated as follows. The C_{out} is the total output parasitic capacitance observed by V_{out} .

$$Z_{out} = r_{ds2} || r_{ds3} || r_{ds4} || 1/sC_{out} \quad (6.10)$$

The gain of transistor M_3 can be calculated as

$$A_{V3} = g_{m3} * Z_{out} = g_{m3} * r_{ds2} || r_{ds3} || r_{ds4} || 1/sC_{out} \quad (6.11)$$

The gain of transistor M_3 is derived from node Y, so the gain from Y mode to output can be represented as

$$A_{VY} = A_{V1} * A_{V3} = g_{m1} * Z_Y * g_{m3} * Z_{out} \quad (6.12)$$

The gain of transistors M_2 and M_4 can be represented as

$$A_{v2} = g_{m2} * Z_{out} \quad (6.13)$$

$$A_{v4} = g_{m4} * Z_{out} \quad (6.14)$$

The gain of transistors M_2 and M_4 is derived from node X, and the total gain from node X to output is

$$\begin{aligned} A_{VX} &= A_{V2} + A_{V4} = (g_{m2} + g_{m4}) * Z_{out} \\ &= (g_{m2} + g_{m4}) * (r_{ds2} || r_{ds3} || r_{ds4} || \frac{1}{sC_{out}}) \end{aligned} \quad (6.15)$$

The total gain of the proposed LNA is the sum value of each gain from node X and node Y.

$$A_{Vtotal} = A_{VX} + A_{VY} = A_{V1} * A_{V3} + A_{V2} + A_{V4} \quad (6.16)$$

Fig.6.2 shows the output IF frequency (200MHz) and bandwidth (50MHz) simulation results for the proposed LNA. As a result, the output IF frequency $f_c=175.6$ MHz with 18.73 dB gain is close to the proposed mixer center frequency of 177.8MHz. The bandwidth spans 8.27MHz to 996MHz, fully covering the proposed mixer case.

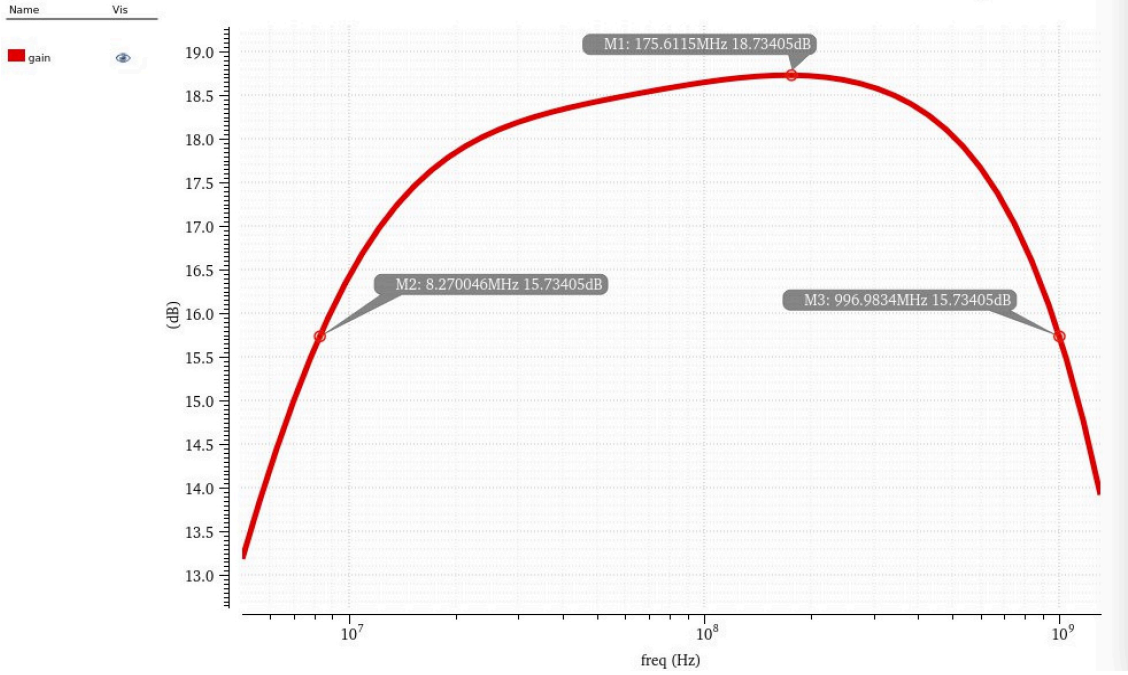


Figure 6.2 Center frequency of the proposed LNA

6.1.2 Noise Figure

According to the proposed LNA, the current noise I_{nM1} from the input transistor flows into node X, but flows out through node Y. The channel noise of the main transistor M_1 develops two noise voltages at node Y, V_{nY} , and node X, V_{nX} , which have two opposite phases. V_{nY} and V_{nX} can be calculated as

$$V_{nY}^2 = Z_Y^2 * I_{nM1}^2 \quad (6.17)$$

$$V_{nX}^2 = Z_X^2 * I_{nM1}^2 \quad (6.18)$$

In the 3rd stage, V_{nY} is converted into current I_{nM3} via M_3 . At the same time, V_{nX} is converted into currents and combined to form I_{nM24} via M_2 and M_4 [37].

I_{nM3} and I_{nM24} can be calculated as

$$I_{nM3} = V_{nY}^2 * g_{m3} \quad (6.19)$$

$$I_{nM24} = V_{nX}^2 * (g_{m2} + g_{m4})^2 \quad (6.20)$$

At the output node of the 3rd stage, the two currents with opposite phases are canceled by the equation

$$I_{\text{nout}}^2 = V_{\text{nX}}^2 (g_{m2} + g_{m4})^2 - V_{\text{nY}}^2 g_{m3}^2 = 0 \quad (6.21)$$

Relation between transconductance and impedance can be generated from the equation

$$\frac{g_{m2} + g_{m4}}{g_{m3}} = \frac{Z_Y}{Z_X} \quad (6.22)$$

For this noise cancellation scheme, the primary noise sources are the thermal noise of R_{D1} and the channel thermal noise of transistors M_2 , M_3 , and M_4 .

The noise factor of R_{D1} can be expressed by

$$F_{RD1} = \frac{4kTR_D (g_{m3} |Z_{out}|)^2 \left(\frac{Z_{O1}}{Z_{O1} + R_{D1}} \right)^2}{4KTR_S A v^2} = \frac{R_S}{R_{D1}} \quad (6.23)$$

The noise factor of M_2 , M_3 , and M_4 can be expressed by

$$F_{M2} = \frac{4kTg_{m2}|Z_{out}|^2}{4KTR_S A v^2} * \frac{\gamma}{\alpha} = \frac{g_{m2}}{R_S (g_{m2} + g_{m4})^2} * \frac{\gamma}{\alpha} \quad (6.24)$$

$$F_{M3} = \frac{4kTg_{m3}|Z_{out}|^2}{4KTR_S A v^2} * \frac{\gamma}{\alpha} = \frac{1}{R_D (g_{m2} + g_{m4})} * \frac{\gamma}{\alpha} \quad (6.25)$$

$$F_{M4} = \frac{4kTg_{m4}|Z_{out}|^2}{4KTR_S A v^2} * \frac{\gamma}{\alpha} = \frac{g_{m4}}{R_S (g_{m2} + g_{m4})^2} * \frac{\gamma}{\alpha} \quad (6.26)$$

The total noise factor is

$$F_{total} = 1 + \frac{R_S}{R_{D1}} + \frac{\gamma}{\alpha R_S (g_{m2} + g_{m4})^2} + \frac{\gamma}{\alpha R_D (g_{m2} + g_{m4})} \quad (6.27)$$

Fig. 6.3 shows the noise figure comparison between the 1st, 1st, and 2nd combined stages and the proposed LNA. The second stage's noise figure (red) is 25.45dB at 175.6MHz. The first and second combined stage's noise figure (green) is 13.5479dB at 175.6MHz. The proposed LNA noise figure (yellow) is 8.76dB at 175.6MHz. The effect of the third stage on the cancellation of thermal noise is observed.

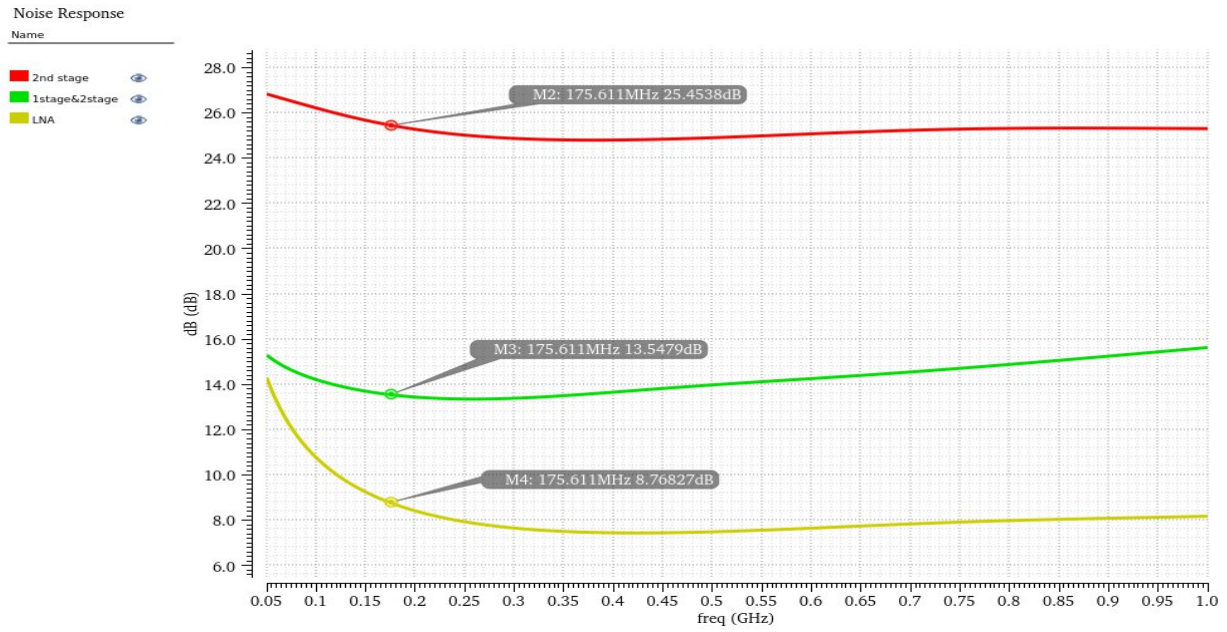


Figure 6.3 Noise figure of 1st stage, 1st, and 2nd stage and proposed LNA

6.1.3 Linearity

As shown in Fig. 6.4, the 1-dB compression point equals -33.98 dBm. As shown in Fig 6.5, the input value of IP3 is -21.6 dBm.

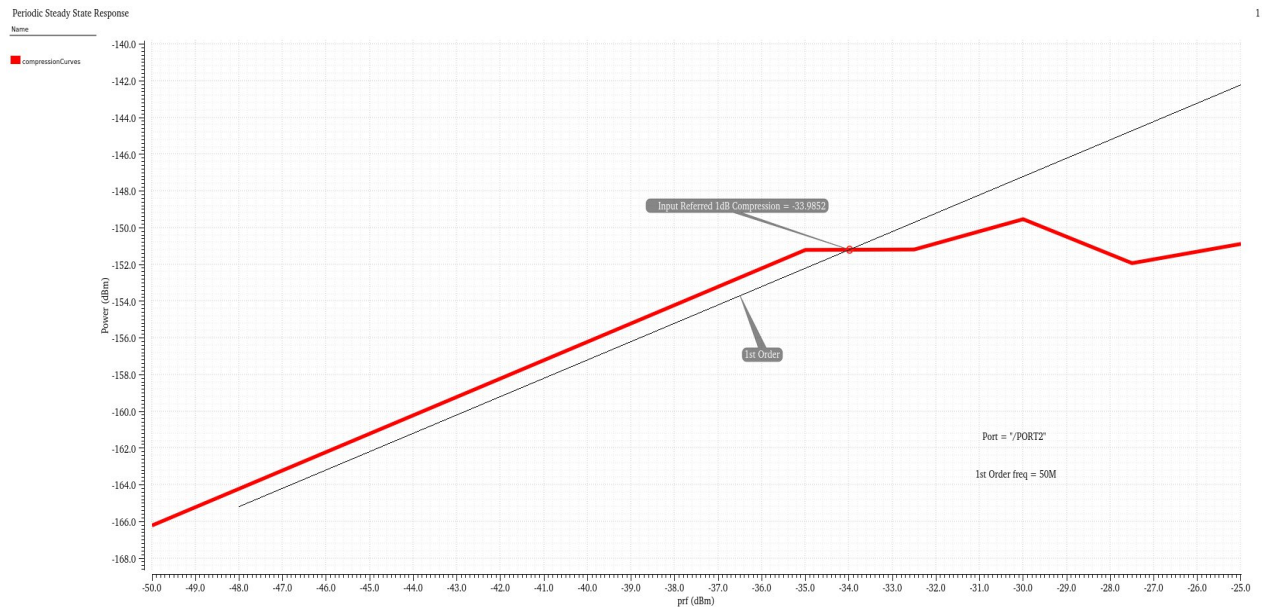


Figure 6.4 1-dB compression of the proposed LNA

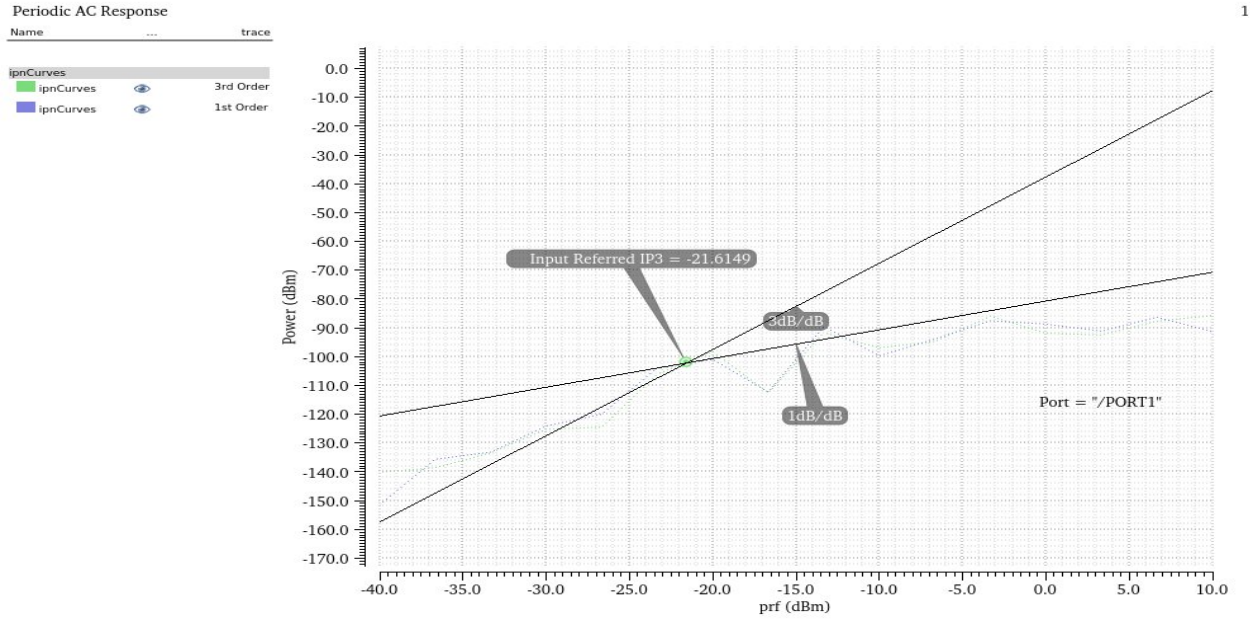


Figure 6.5 IP3 of the proposed LNA

6.2 Tunable Gilbert Mixer and Low-Noise Amplifier Integration

In this section, A high-gain, low-noise amplifier presented in section 6.1 is cascaded with the mixer with an equivalent electronic circuit (π -model) as shown in Fig.6.6 and Fig.6.7 to optimize the conversion gain of the proposed tunable mixer, compress the noise, and keep the required IF center frequency and bandwidth for multi-band multi-standard applications.

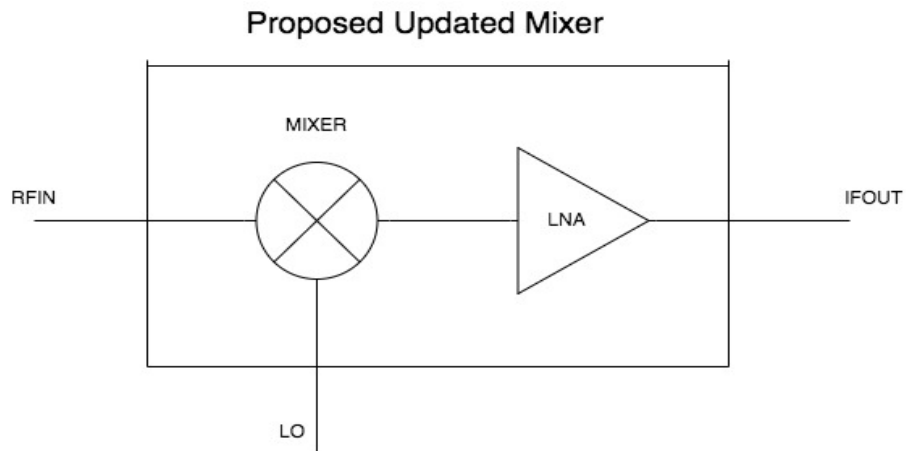


Figure 6.6 Block diagram of proposed updated mixer

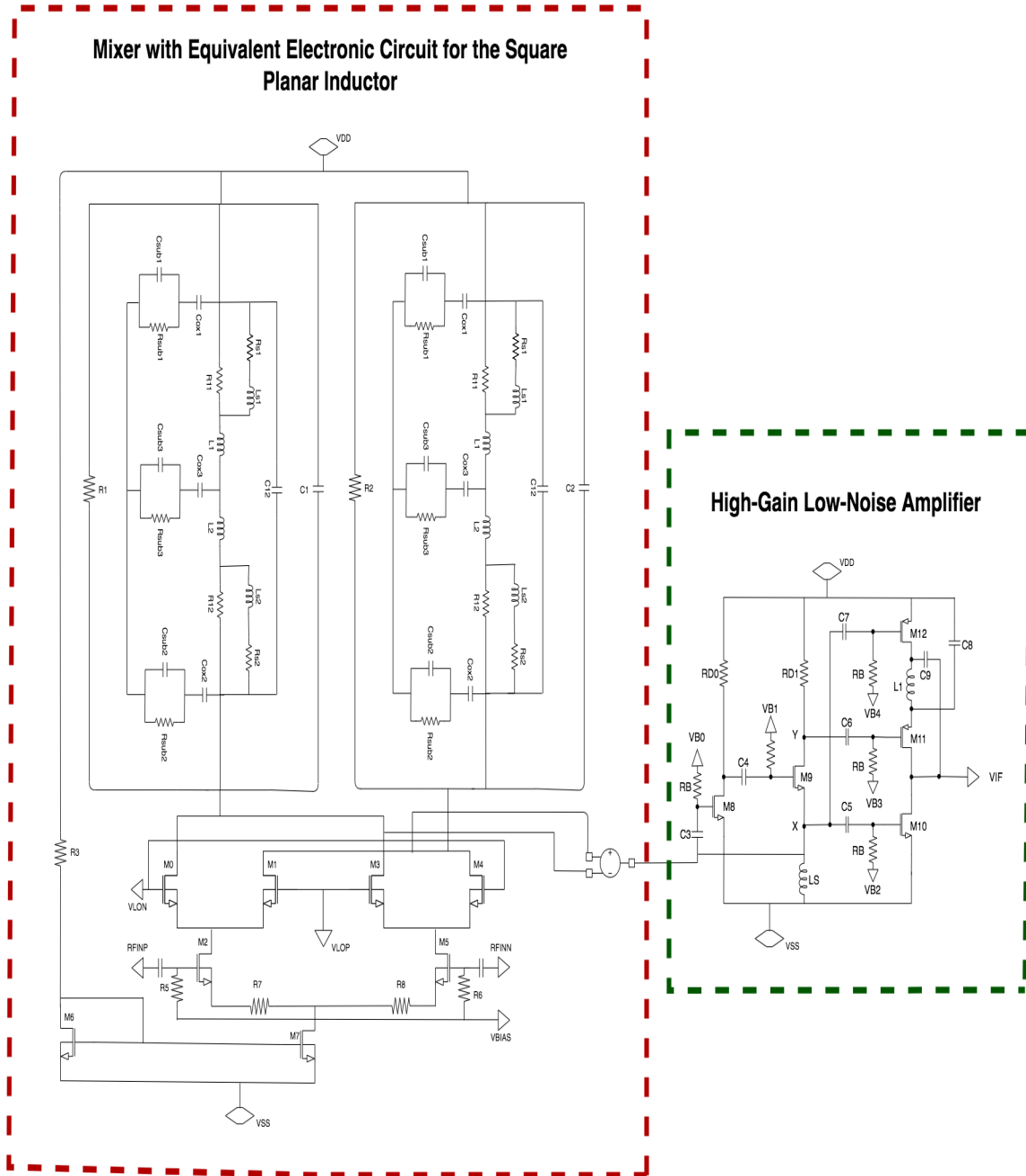


Figure 6.7 Proposed updated mixer

6.3 Performance of Integrated Circuit

In section 4.6, the mixer with an equivalent electronic circuit (π -model) is designed to present a conversion gain of 7.4dB @ a tunable IF center frequency of 177.8 MHz with an IF bandwidth of 87.57 MHz. After integration with the proposed high-gain low-noise amplifier, the conversion gain increases from 7.4 dB to 27.68 dB with 87 MHz

bandwidth @ IF=176MHz, as shown in Fig. 6.8. Compared with the proposed mixer, the bandwidth and center frequency remain unchanged. Fig.6.9 shows the noise figure comparison between the mixer with an equivalent electronic circuit and the integrated mixer with LNA. The noise figure changes from 3.14 dB (red) to 3.47 dB (green) at IF frequency 177.8 MHz. A slight change in the noise figure is observed. Fig. 6.10 shows the 1-dB compression point comparison; the 1-dB compression point changed from -17.1dBm to -14.6 dBm, compared with Fig.4.16. As shown in Fig.6.11, the IP3 changed from -19.8 dBm to -18.6 dBm, compared with Fig.4.17.

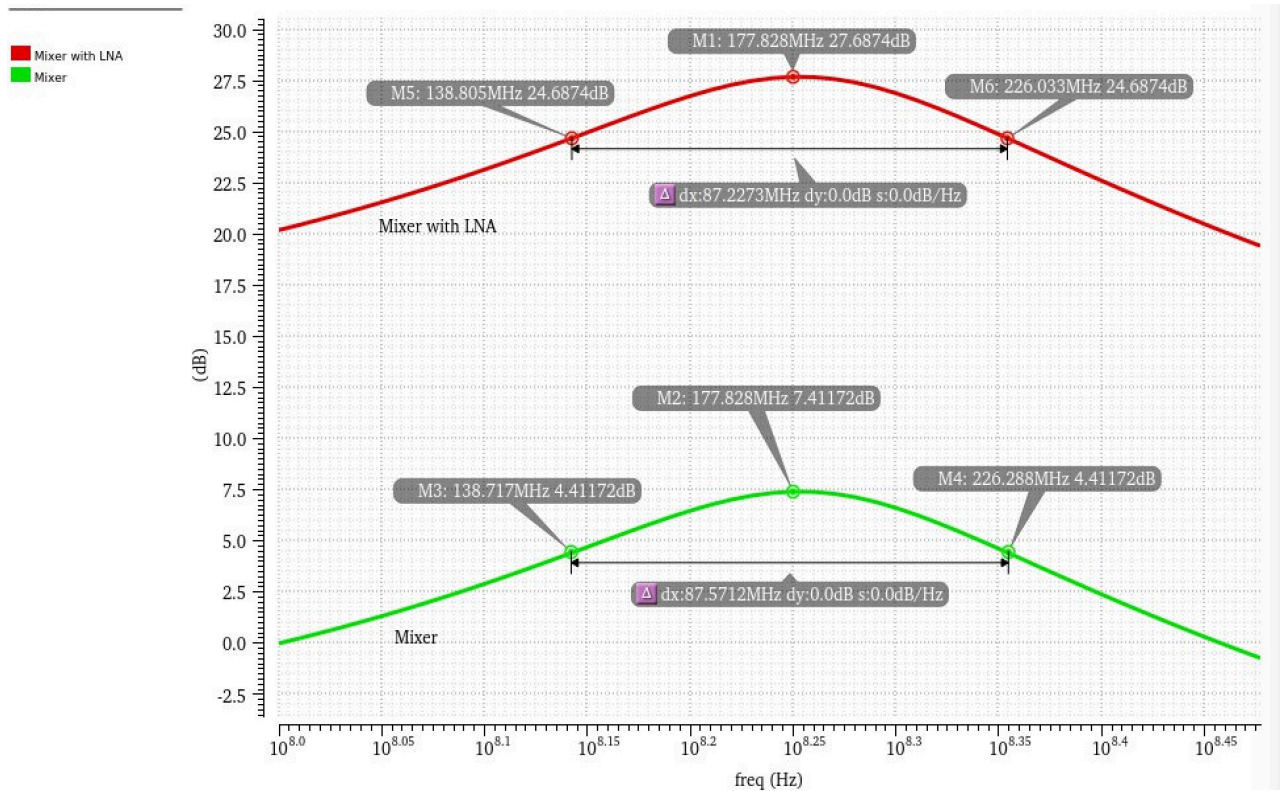


Figure 6.8 Center frequency comparison between prototype Gilbert mixer (green) and proposed mixer with LNA (red)

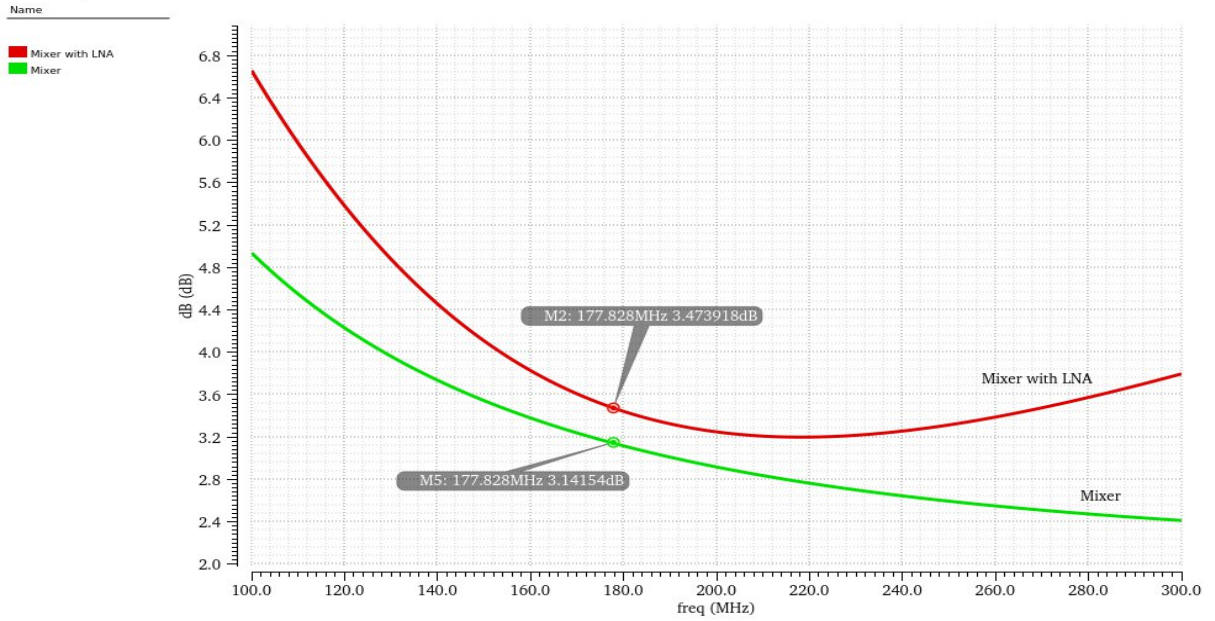


Figure 6.9 Noise figure comparison between prototype Gilbert mixer (green) and the integrated mixer with LNA (red)

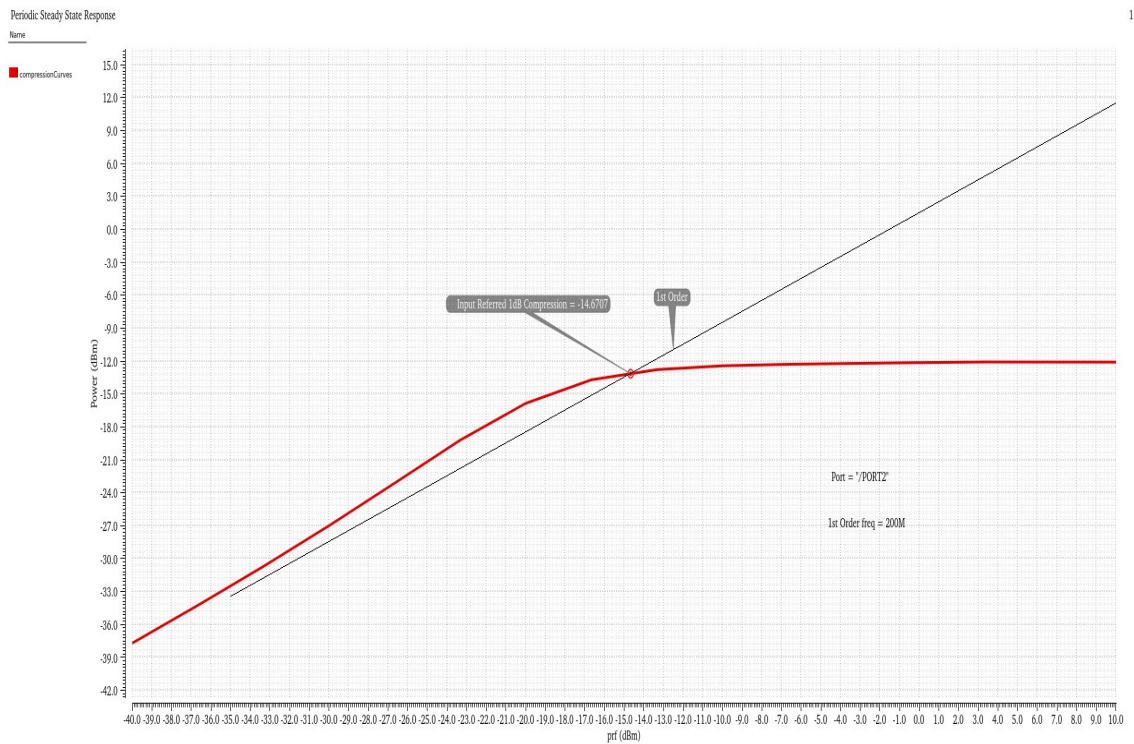


Figure 6.10 1-dB compression of the proposed mixer with LNA

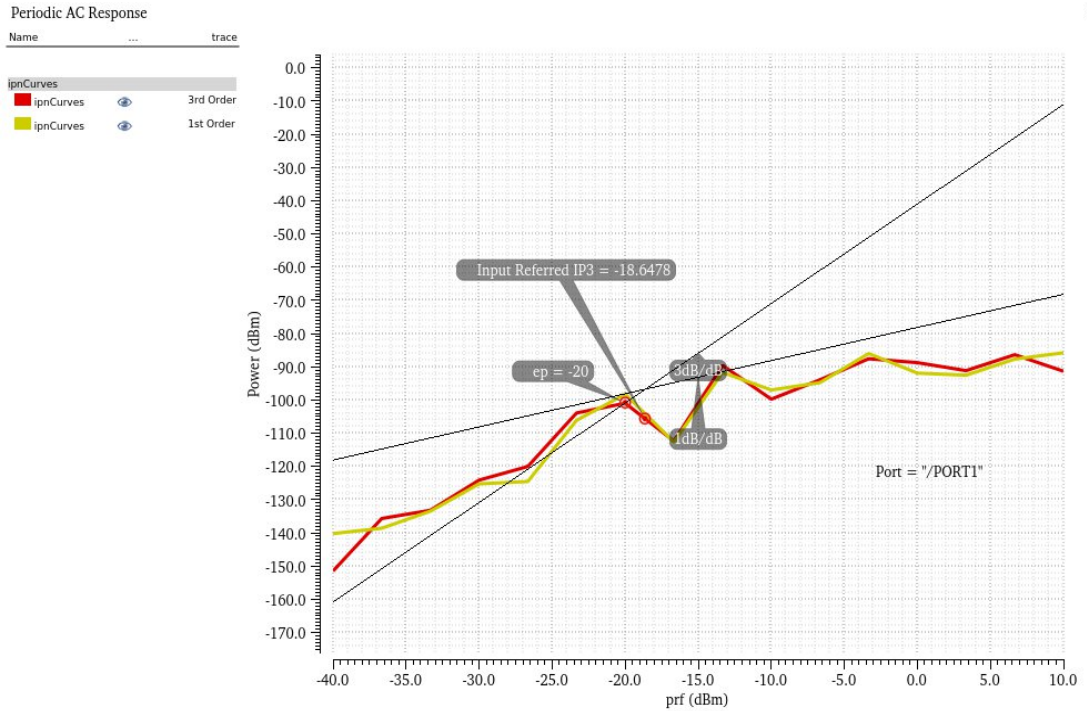


Figure 6.11 IP3 of the proposed mixer with LNA

6.4 Comparison of Different Tunable Gilbert Mixer Technologies

Table 6.1 shows the performance and comparison of different tunable Gilbert mixer technologies where the input frequency $RF=2.2\text{GHz}$, $LO=2\text{GHz}$, and the output IF center frequency $IF=200\text{ MHz}$ having a constant 50MHz IF bandwidth. The past work of a tunable Gilbert mixer with a tunability of 200 MHz IF, and a regular IF bandwidth of 50 MHz , achieves a noise figure of 3.95dB , a conversion gain of 14.7dB , a 1-dB compression point -10.88 dBm , and an $IP3$ -5.02 dBm . Tunable Gilbert mixer with Effective Prototype Inductor has a tunability of 199.5 MHz IF, a constant IF bandwidth of 52 MHz , and achieves a noise figure of 2.89 dB , a conversion gain of 13.75 dB , a 1-dB compression point -15.19 dBm , and an $IP3$ -5.8dBm . A Tunable Gilbert mixer with electronic circuits (π -model) has a tunability of 177.8 MHz IF and IF

bandwidth of 87.57 MHz. It achieves a noise figure of 3.14 dB, a conversion gain of 7.41dB, 1-dB compression point of -17.18 dBm, and IP3 of -19.8 dBm. Tunable Gilbert mixer with Electronic Circuits (π -model) integrated with LNA has a tunability of 177.8 MHz IF and IF bandwidth of 87.22 MHz. It achieves a noise figure of 3.47dB, a conversion gain of 27.68 dB, a 1-dB compression point of -14.6 dBm, and an IP3 of -18.6 dBm.

Table 6.1 Comparison of Different Mixer Technologies

	Tunable Gilbert Mixer with ideal inductor	Tunable Gilbert Mixer with Effective Prototype Inductor	Tunable Gilbert Mixer with Electronic Circuits (π -model)	Tunable Gilbert Mixer with Electronic Circuits (π -model) integrated with LNA
CMOS (nm)	180	180	180	180
VDD (V)	1.8	1.8	1.8	1.8
RF (GHz)	2.2	2.2	2.2	2.2
LO (GHz)	2	2	2	2
IF (MHz)	200	199.5	177.8	177.8
BW (MHz)	50	52	87.57	87.22
Gain (dB)	14.7	13.75	7.41	27.68
NF (dB)	3.95	2.89	3.14	3.47
1-dB compression (dBm)	-10.88	-15.19	-17.18	-14.6
IP3 (dBm)	-5.02	-5.8	-19.8	-18.6

Chapter 7: CONCLUSION AND FUTURE WORK

7.1 Conclusion

A proposed tunable Gilbert mixer with effective prototype inductor tunable Gilbert mixer cell is first introduced. The design synthesis of a wide tuning with a constant IF bandwidth is presented. Mixer design parameters calculations, macro and micro adjustments, and convergent flow to optimize design parameters to meet the desired center frequency 200MHz and constant IF bandwidth is explained and demonstrated by examples. An equivalent π -model tunable mixer is also introduced to solve the inductor loss caused by the effective prototype inductor. Last, a wide frequency span CMOS high-gain low-noise amplifier is designed and connected with the proposed tunable Gilbert mixer to achieve a high gain. A design example further illustrates how the tunable Gilbert mixer works and complies with the design requirements to function as expected. Finally, the design synthesis approach can be adopted to design wide frequency span CMOS tunable mixers for multi-band/multi-standard wireless applications, a promising candidate for low-cost and a small occupied die area.

7.2 Future Work

The above sections have demonstrated research and industry trends on the fully integrated mixer, past work, current fulfillment, and problem statement. Next, the study will focus on two directions:

1) An effective prototype design case (RF = 2.2 GHz, LO = 2 GHz, IF = 200 MHz, BW = 50 MHz) of tunable Gilbert mixer with effective prototype inductor is presented. A wide frequency span of 2 GHz (RF=1.1 ~ 3.1 GHz) with controllable bandwidth of 50 MHz will be further analyzed to optimize the design synthesis approach to offset the inaccuracy of center frequency and bandwidth, the discrepancy between the actual and ideal prototype inductor.

2) A multi-band, multi-standard receiver architecture for wireless applications will be further analyzed, such as 802.11a/b/g WLAN and 802.16a WMAN. The targeted frequency bands include licensed bands: 2.3 GHz, 2.5 ~ 2.7 GHz, and 3.5~ 3.7 GHz, and un-licensed bands – ISM 2.4 GHz and U-NII 5 GHz [39].

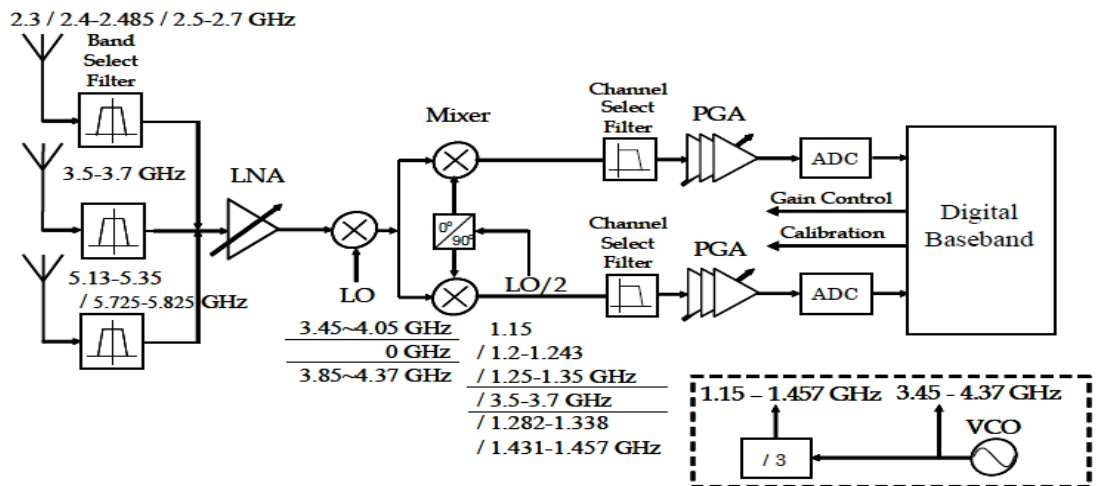


Figure 7.1 Multi-band multi-standard receiver architecture for wireless applications [39]

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